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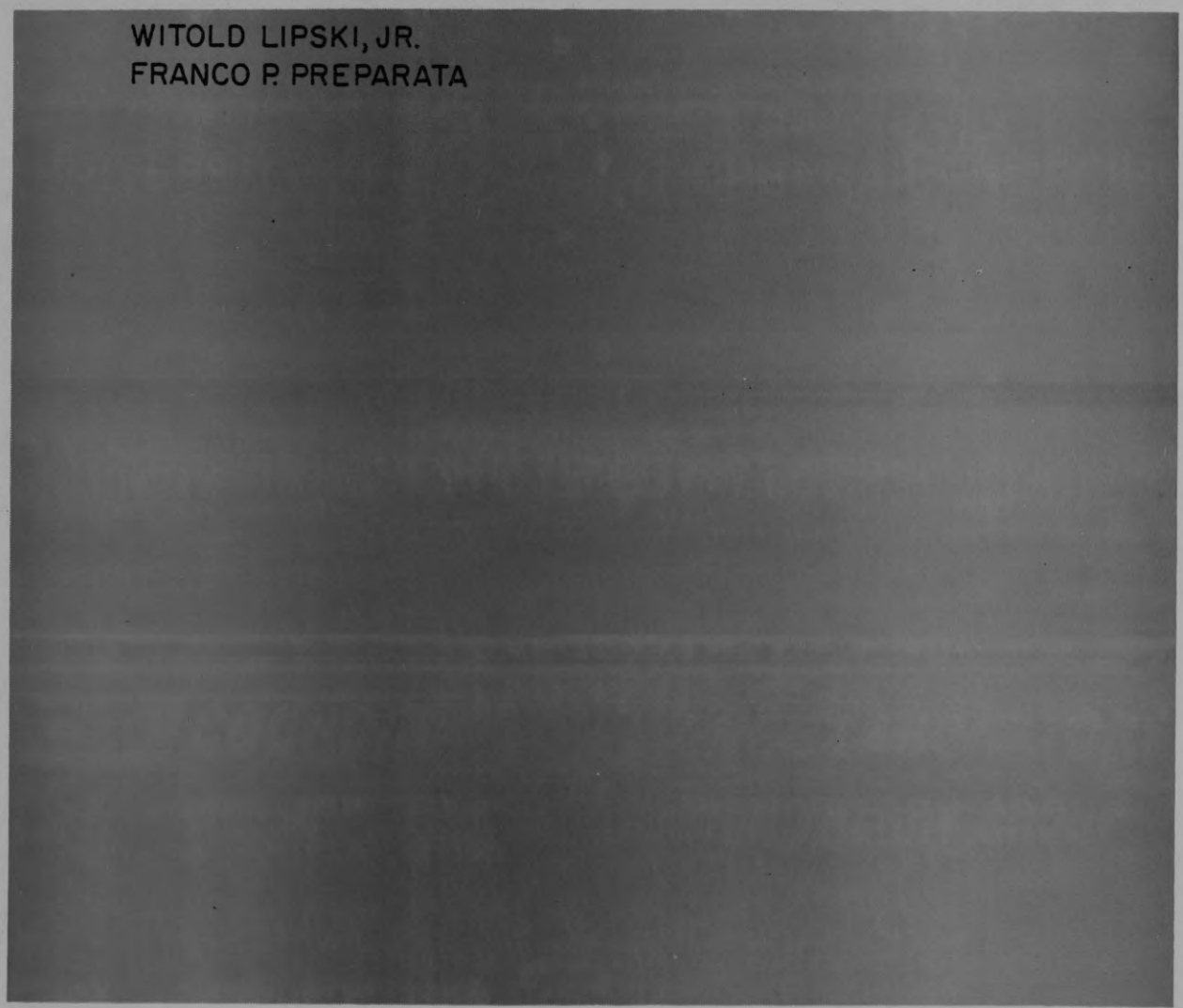

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AN ELEMENTARY THEORY OF LAYOUT WIRABILITY

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Abstract. We consider the problem of wiring planar knock-knee mode layouts. We present a systematic approach to this problem and develop a unified framework that also applies to layouts using grids that are more general than the usual square grid. We determine all possible grids that satisfy some natural regularity criteria. We also develop some specific techniques for wiring of layouts in the square grid. As one of the applications of these techniques, we give a simple characterization of two-layer wirability of an arbitrary layout.

Key Words: VLSI, layout, conducting layer, wiring, two-layer wirability, knock-knee mode, layout grid, tessellations of the plane.

1. *Introduction*

An important aspect of VLSI layout research is the conversion of a network layout in the plane to an actual (three-dimensional) configuration of wires. Since any nontrivial network results in layouts having crossings, it is clear that their wiring cannot be realized in a single plane. Normally, there is a small number of conducting layers, and each wire is realized by a sequence of strips in different layers, with a vertical connection, called *via*, at each (vertically aligned) layer change.

Several results on layout wiring have been obtained in recent years for layouts in square grids allowing crossings and knock-knees (points where two wires bend). First, that a two-terminal-net channel routing problem is solved with two layers using nearly twice as many layers as the minimum ([RBM], see also [BB1, PL1, PL2]); second, that three layers are sufficient to solve a two-terminal-net

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channel routing problem with the minimum number of tracks [PL1, PL2]; third, that to decide if a (two-terminal-net) layout is three-layer wirable is NP-complete [Lip], while every plane layout is wirable with at most four layers [BB2].

The purpose of this paper is to present a systematic approach to layout wiring, by developing a unified framework that also applies to grids that are more general than the square grid. We determine all possible grids that satisfy some natural regularity criteria. We also develop some specific techniques for wiring of layouts in the square grid. As one of the applications of these techniques, we give a simple characterization of two-layer wirability of an arbitrary layout.

2. *Tessellations and Grids*

By a ***tessellation of the plane*** we shall mean any partition of the plane into (domains whose boundaries are) regular polygons, referred to as ***tiles***, where each side is shared by exactly two tiles (all polygons have the same side length, but not necessarily the same number of sides). Consider the ***dual graph*** of a tessellation of the plane, i.e. the graph whose vertices (***grid points***) are centers of the tiles, and edges join grid points belonging to neighboring tiles (i.e., tiles sharing a side). Since we shall use such dual graphs to route wires, it is reasonable to restrict our considerations to the case where the degree of each grid point is even, or equivalently, to tessellations where each tile has an even number of sides (every wire entering a tile leaves the tile). Such tessellations will be called *even*, and their dual graphs will be called *uniform grids*.

Lemma 1. There exist exactly four essentially different uniform grids:

(a) the square grid, where all tiles are squares, see Fig. 1,

(b) the hexagonal grid, where all tiles are hexagons, see Fig. 2,

(c) the octo-square grid, where the tiles are octagons and squares, see Fig. 3,

(d) the dodeco-hexo-square grid, where the tiles are dodecagons, hexagons and squares, see Fig. 4.

Proof. Let p be any vertex of a tile, and consider all tiles surrounding p. Let there be k of them. Each of the tiles is a regular polygon with at least four sides, and consequently $k \leq 4$. On the other hand, obviously $k \geq 3$. If $k = 4$ then all tiles meeting at p are squares, as in the square grid.

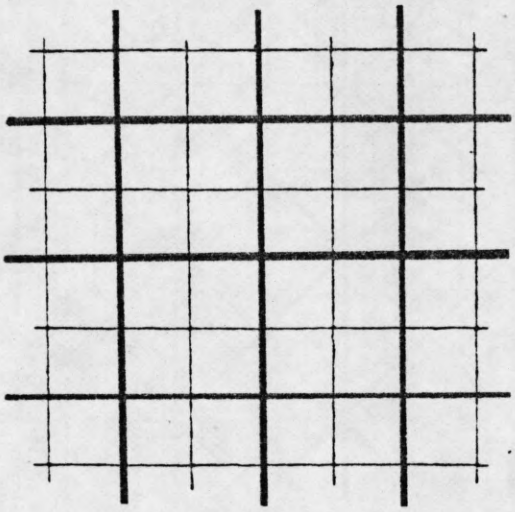


Figure 1. The square grid.

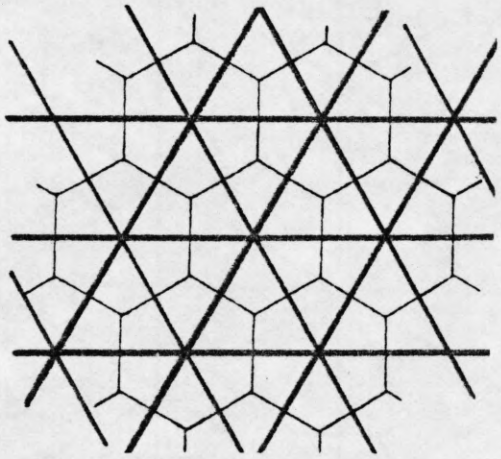


Figure 2. The hexagonal grid.

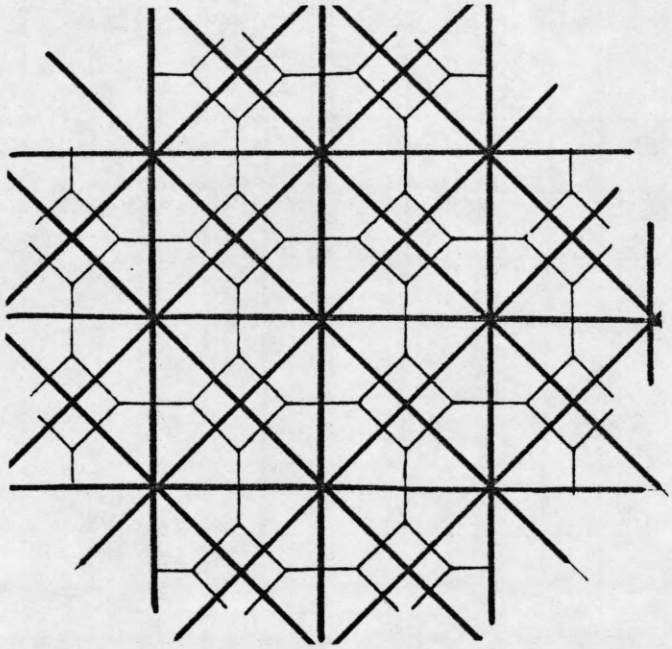


Figure 3. The octo-square grid.

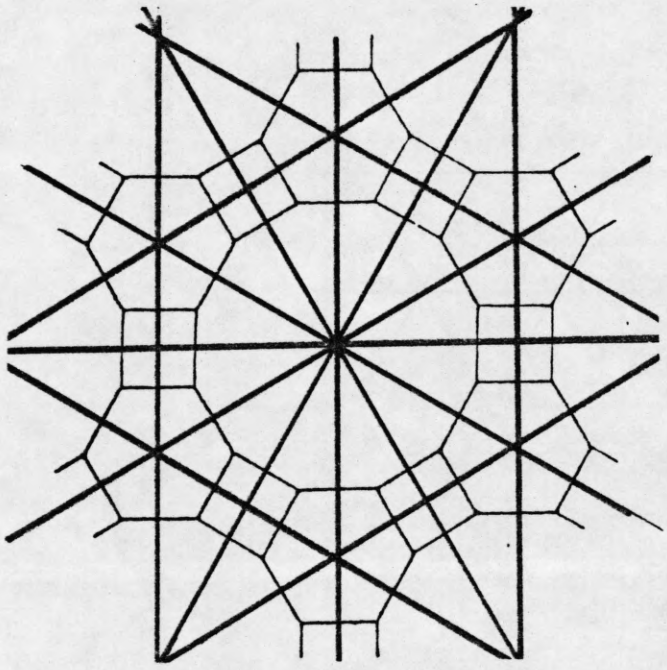


Figure 4. The dodeco-hexo-square grid.

Consider now the case of $k = 3$, and suppose that the tiles meeting at p have n_1, n_2, and n_3 sides, respectively, with $n_1 \leq n_2 \leq n_3$. Since each angle of a regular n-gon is equal to $(n-2)\pi/n$, we have

$$\frac{(n_1-2)\pi}{n_1} + \frac{(n_2-2)\pi}{n_2} + \frac{(n_3-2)\pi}{n_3} = 2\pi,$$

i.e.,

$$\frac{1}{n_1} + \frac{1}{n_2} + \frac{1}{n_3} = \frac{1}{2}.$$

If $n_1 = 4$, then clearly $n_2 \geq 6$, and we have two solutions:

$$n_2 = 6, \quad n_3 = 12,$$

as in the dodeco-hexo-square grid, and

$$n_2 = 8, \quad n_3 = 8,$$

as in the octo-square grid.

Finally, trying the next possible value of n_1, $n_1 = 6$, we obtain the unique solution $n_1 = n_2 = n_3 = 6$, as in the hexagonal grid. Clearly, $n_1 > 6$ is impossible.

It is easy to see that in each of the four cases a single vertex with surrounding tiles uniquely determines a tessellation, which completes the proof. □

Notice that the four uniform grids correspond to two, three, four, and six directions uniformly distributed on the plane, respectively.

In fact, the tessellations (a), (b) are two of the three *regular tessellations*, i.e. tessellations where each of the tiles is the same regular polygon (the third regular tessellation is given by the dual graph of (b)). The tessellations (c), (d) are two of the eight *semiregular (Archimedean) tessellations*, i.e. tessellations where all tiles are regular polygons, and where the cyclic sequence of tiles surrounding every vertex is the same, see [FT].

One can also consider other types of grids for routing wires, for instance by imposing some regularity conditions directly on the grid . For example, if we require that the grid itself determine a semiregular tessellation with an even number of tiles surrounding each grid point, then we get two additional grids (e), (f) shown in Fig. 5 and 6. Note that both grids are dual graphs of (generalized) tessellations of the plane into nonregular quadrangles. Grid (e) corresponds, as the hexagonal grid, to three directions in the plane, but now every grid point has degree four, as in the square grid; e.g., each grid point corresponds to either a crossing or a knock-knee (or a situation involving at most one wire).

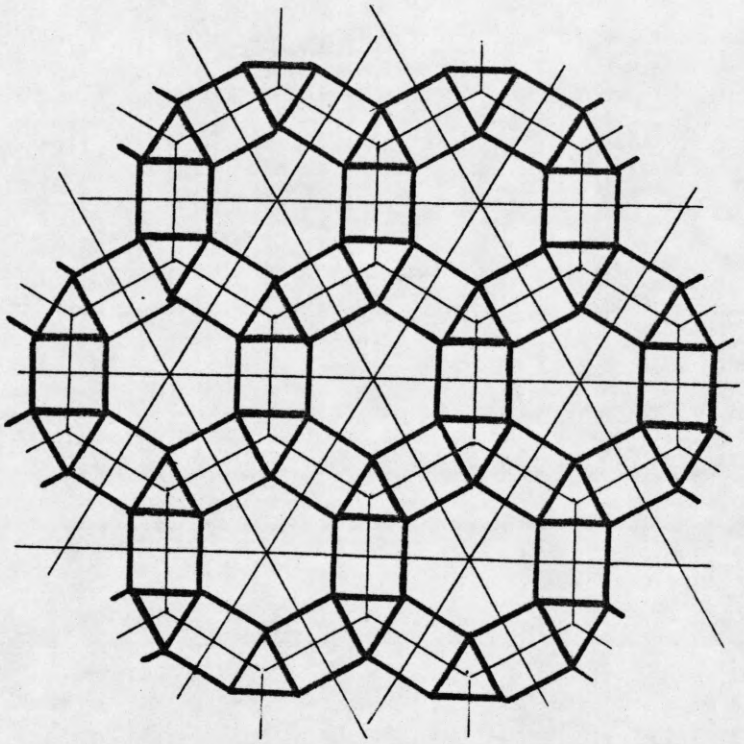


Figure 5. The first of the additional grids corresponding to tessellations with non-regular tiles.

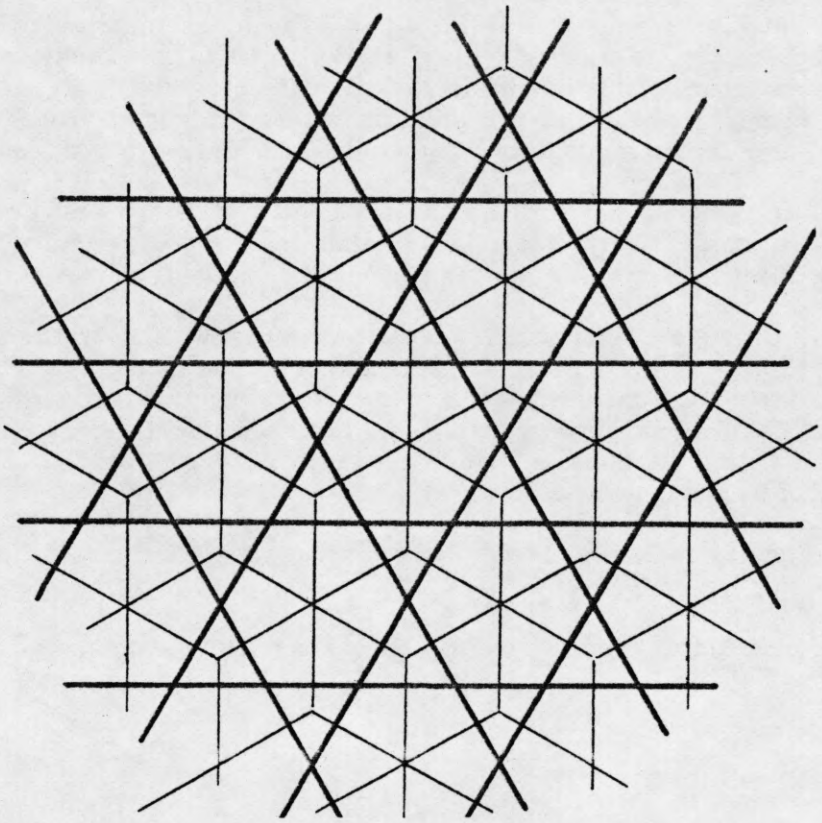


Figure 6. The second of the additional grids corresponding to tessellations with non-regular tiles.

3. *Layouts and Wirings*

Let us consider a fixed grid on the plane. A *layout domain* is any collection D of tiles of the tessellation corresponding to the grid. By the *grid points of* D we shall mean all grid points *inside* tiles of D, and by the *grid edges of* D all edges of the grid incident with *at least one* grid point of D.

A *wire* in D is any connected subgraph w of the grid such that (i) every edge of w is a grid edge of D, and (ii) no grid point of D is a *terminal* (i.e. vertex of degree 1) of w. Note that we allow a wire, or portion thereof, to be a cycle, although usually such wires do not occur in practice. By a (*planar*) *layout in* D we mean any finite collection $W = \{w_1,\ldots,w_n\}$ of wires in D. A *knock-knee mode layout* is a layout whose wires are edge-disjoint. Often the layout domain D will not be explicitly specified, when it is clear from the context.

A (*conducting*) *layer* is a copy of the grid. The layers are denoted $L_1,\ldots,L_\nu$. We think of the layers as laid one upon the other, where the index denotes their vertical order, L_1 and L_ν being the bottommost and the topmost layers,

respectively. We write $L_i \prec L_j$ if $i < j$, and $L_i \preccurlyeq l_j$ if $i \leq j$.

A (*ν-layer*) *wiring* of layout $W = \{w_1,\ldots,w_n\}$ in D is an assignment, for $k = 1,\ldots,n$, of each edge e of w_k to a layer $\Phi(e,w_k) \in \{L_1,\ldots,L_\nu\}$ so that Condition (C) below is satisfied. Intuitively, this condition says that if we establish a contact, or *via*, between all edges of w_k that are incident with a grid point v of D, for every choice of w_k and v, then no contact between distinct wires of W will result:

(C) If edges e_1, e_2 of w_k incident with a grid point v of D are assigned to layers L_i, L_j, respectively, where $L_i \preccurlyeq L_j$, then for every edge e of w_l, $l \neq k$, incident with v, $\Phi(e,w_l)$ is not any of the layers L, for $L_i \preccurlyeq L \preccurlyeq L_j$.

Notice that if an edge e appears in two distinct wires, w_k and w_l, then (C) guarantees that $\Phi(e,w_k) \neq \Phi(e,w_l)$. Clearly, if W is a knock-knee mode layout then we may think of a wiring as a mapping Φ that associates a unique layer $\Phi(e)$ with any edge e appearing in the layout. A layout W is *ν-layer wirable* if there exists a ν-layer wiring of W. The least number ν such that W is ν-layer wirable is called the *layer number* of W, and is denoted by $\nu(W)$.

Notice that Condition (C) allows two different wires to share the same layer *at a grid point outside* D.

An example of a four-layer wiring of a (knock-knee) layout in the grid of type (e) is shown in Fig. 7.

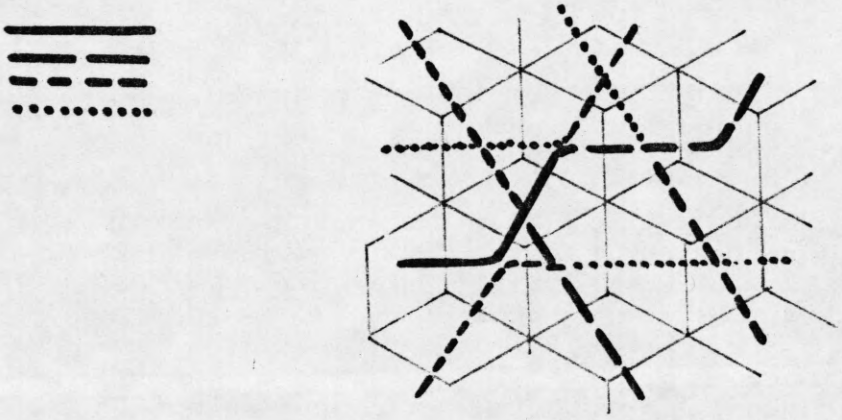


Figure 7. A four layer wiring of a layout.

In the rest of this paper we restrict ourselves to knock-knee mode layouts, referred to simply as layouts.

4. *Full Layouts*

A layout W in D is called ***full*** if every edge of D belongs to a (unique) wire of W. Notice that every layout W can be defined in a "local manner", by specifying, for every tile T of D, one of the finite number of patterns (arrangements of *halves* of wire edges with explicitly specified contacts between some of them) induced by W on T. Such a pattern, together with the tile containing it, will be called a ***layout tile***. Any layout tile induced by a full layout is called ***full***. In the case of full layouts the choices of full layout tiles can be done independently of each other, i.e. there is a one-to-one correspondence between full layouts and arbitrary choices of full layout tiles. (Strictly speaking, this is true only if we allow the situation where two edges of the same wire incident with a grid point v of D, and connected by a path avoiding v, are not connected by a via at v: this intuitively corresponds to the presence of self-intersecting wires.) This fact will often be used, sometimes implicitly, by the techniques described in this paper.

If we insist on considering layout domains of arbitrary shape, it is not because we think a domain composed of an arbitrary collection of tiles can arise in practice, but rather because we shall now show that the problem of wiring an arbitrary layout W in D can be reduced to wiring another, in general simpler, full layout in a (perhaps irregular) subset of D.

Given an arbitrary layout W in D, call a grid point v of D ***trivial*** (*with respect to* W) if there exist edges of at most one wire of W incident with v. A tile T in D containing a trivial grid point will also be called *trivial*. Let D* be the set of nontrivial tiles in D. By the *core* of W, denoted by core(W), we mean the layout W* in D* obtained by deleting from the wires of W all edges that are not grid edges of D*. Note that a wire of W can be broken into several wires of core(W).

An example of a layout and its core is shown in Fig. 8.

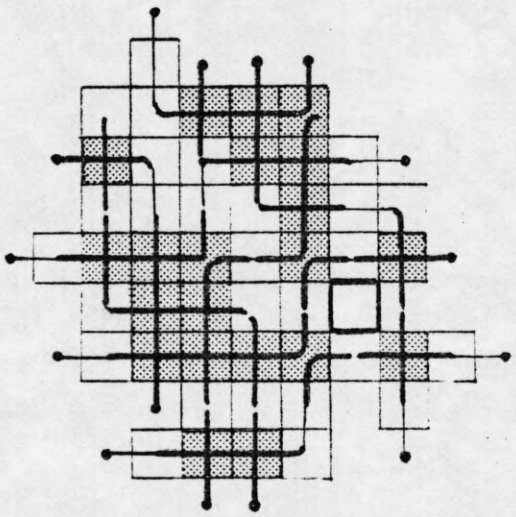


Figure 8. A layout in a domain D. The tiles of the core are shown shaded. The core wires are shown with heavy lines.

Theorem 2. $\nu(W) = \nu(\text{core}(W))$.

Proof. Clearly $\nu(\text{core}(W)) \leq \nu(W)$, since a ν-layer wiring of core(W) can be obtained from a ν-layer wiring of W by simply deleting from the wires those edges that are not grid edges of D*. Conversely, suppose that we have a ν-layer wiring of the core. Let us assign the wire edges of W missing in W* (i.e. exclusively the edges of W joining pairs of trivial grid points of D) to any layers, say all to L_1. For any trivial grid point v we establish, if necessary, a via joining all wire edges incident with v. Obviously, the result is a ν-layer wiring of W, which proves $\nu(W) \leq \nu(\text{core}(W))$. □

In the rest of the paper we shall restrict ourselves to layouts using the square grid. By Theorem 2 we may also restrict ourselves to full layouts. The results obtained should prove useful to the development of an analogous framework for the other grids described in Section 2.

5. *Square Grids: Wiring of Full Layouts*

In the case of the square grid, there are fifteen possible layout tiles, shown in Fig. 9. Only the first three of them, corresponding to the crossing and the two possible knock-knees, are nontrivial. Notice that for layouts in the square grid, core(W) is always full. On the other hand, a full layout may contain the trivial tile ⊞. However, by virtue of the construction given in the proof of Theorem 2, we may always replace the layout by its core, thus eliminating the trivial tiles. In what follows, we shall always consider full layouts without trivial tiles.

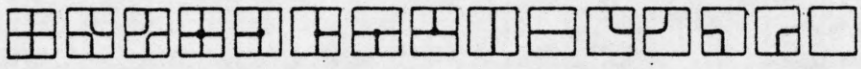


Figure 9. The catalog of the layout tiles for the square grid.

Suppose that a full layout (without trivial tiles) has been wired with ν layers. We now examine this wiring tile by tile, and classify each tile, or portion thereof, on the basis of the layer assignment of its wire edges. The basic idea is to consider regions of two types:

V, where vertical wire edges lie above horizontal ones, and

H, where horizontal wire edges lie above vertical ones.

Classifying a crossing tile (layout pattern ⊞) with respect to our wiring is obvious, and all portions of the tile receive identical classification. For a knock-knee tile (layout pattern ⧅ or ⧄), we divide the tile by the (unique) diagonal that bisects both wires. It is clear that the two resulting half tiles are of opposite types: indeed, to mantain insulation, both edges of one wire must occupy higher layers than both edges of the other wire. In summary, each tile of D is classified into one of the six distinct types, called *wiring tiles*, shown in Fig. 10.

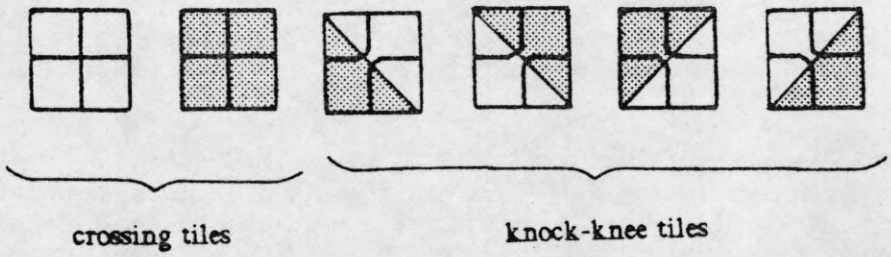


Figure 10. Wiring tiles for the square grid (type H = shaded; V = unshaded).

For a given full layout W in D, the arrangement of diagonals bisecting both wires in any of the knock-knee tile of D is called the *diagonal diagram* of W. Since the diagonal diagram of W uniquely determines W, we shall often identify a layout with its diagonal diagram.

The wiring tiles induced on D by a given wiring uniquely determine a partition of the whole region occupied by D into regions of two types, V and H. Before we investigate the properties of this partition in more detail, let us establish some terminology related to a fixed layout domain D, which we shall now assume to be composed of a finite number of tiles. The sides and vertices of these tiles will be referred to as *tile edges* (not to be confused with grid edges) of D, and *vertices* (not to be confused with grid points) of D, respectively. A vertex that is shared by less than four tiles is called a *boundary vertex*, and an edge that is a side of a single tile is called a *boundary edge*. Other vertices and tile edges of D are called *internal*. The boundary vertices and edges define the *boundary* of D, which is clearly a vertex disjoint collection of (possibly self-intersecting) cycles.

Let M be any collection of diagonals and internal tile edges of D (they will all be referred to as *edges* of M). Clearly, M divides D into some number of connected regions (two regions whose boundaries have only a finite number of common points are considered disconnected). We say that M is a *two-colorable map* on D, if there exists an assignment of two colors to the regions, such that each edge of M separates two regions of different colors.

We now give the following characterization of two-colorable maps on D that is a generalization of the well-known characterization for the case where D is the whole plane (see e.g. [SK]). Its proof will give us some insight into the structure of two-colorable maps on D.

Lemma 3. A collection M of diagonals and internal tile edges of D is a two-colorable map if and only if

(M1) Every internal vertex of D is incident with an even number of edges of M.

(M2) Every connected component of the boundary of D is incident with an even number of edges of M (i.e., the total number of edges of M incident with vertices of this connected component is even).

Proof. [Necessity] If M is two-colorable then clearly (M1) and (M2) are satisfied: (M1) is proved by considering the regions of the map surrounding an internal vertex; (M2) is proved by traversing the boundary of a component, and taking into account that each edge corresponds to a change of the color of a region.

[Sufficiency] Suppose now that (M1) and (M2) are satisfied. Let H be the graph whose vertices are the vertices of D, and whose edges are the edges of M and the boundary edges of D. We first identify all the vertices of a given connected component of the boundary of D (and delete the boundary edges), and thereby transform H into H'. In the latter all vertices have even degree, so that every connected component of H' is eulerian and H' can be decomposed into an edge-disjoint collection of elementary cycles. We now restore the original boundary of H, i.e. expand each of the previously collapsed boundary components. Every cycle in our decomposition of H' is expanded into an elementary cycle of H by replacing every boundary vertex (there may be none) of the cycle by a suitable elementary path in the connected component of the boundary of D corresponding to that vertex. Notice that every edge of M occurs in exactly one (expanded) cycle.

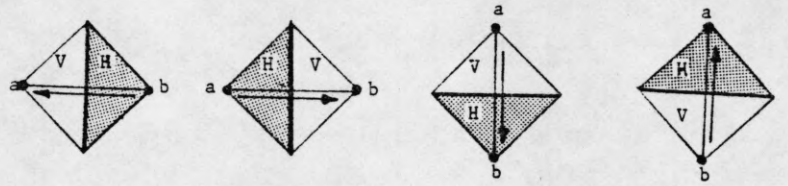
We now begin the coloring. We start with one color assigned to all regions. We then add the (expanded) cycles one by one, at each step changing the color to the opposite for all regions inside the cycle. It is easy to see that at the end each edge of M separates two regions of opposite colors. □

Notice that since in any graph the sum of all degrees is even, it is sufficient to verify condition (M2) for all components except one. In particular, (M2) is always satisfied if the boundary of every connected piece of D is connected (here two pieces sharing at least one vertex may be considered connected); that is, if D does not contain holes. Notice also that a connected component of the boundary may be any self- intersecting cycle corresponding to any complicated (nested) structure of pieces of D and holes whose boundaries touch each other in a finite number of points. However, to verify the conditions of the theorem we do not have to analyze this structure. We simply construct a graph containing all boundary edges (tile edges that are not shared by two tiles) and find its connected components.

Let us now return to the partition of D into regions of type V and type H induced by a wiring Φ of a layout W. We shall denote by $M(\Phi)$ the two-colorable map corresponding to this partition. Clearly, the set of diagonals in $M(\Phi)$ coincides with the set of diagonals in (the diagonal diagram of) W; this becomes obvious if we look at the set of possible wiring tiles shown in Fig. 10. Now call *any* two-colorable map on D with this property a *two-colorable map for* W. The natural question that arises here is whether any two-colorable map for W is induced by some wiring of W. It turns out that this is not the case, even if we put no restriction on the number of layers that can be used by the wiring. However, there is a simple method to verify if a given two-colorable map is realizable and, if so, to determine the minimum possible number of layers in a wiring inducing it. To describe this method, we now introduce a directed graph associated with any two-colorable map.

Let M be any two-colorable map on D, with some fixed assignment of types, V and H, to its regions. The *layer graph* of M, denoted by G(M), is a directed graph whose vertices are the grid points of D, and whose edges are suitably

oriented internal grid edges crossing (i.e. dual to) nondiagonal edges in M. To explain the idea behind the orientation of the edges of G(M), consider, say, a horizontal grid edge e, with left and right endpoints a and b, respectively, and crossing a nondiagonal edge c in M, see Fig. 11(a). Note that the triangle defined by a or b and the edge c (called an *e-wedge*) is entirely contained in one region of the map.



(a) (b) (c) (d)

Figure 11. Orienting the edges of the layer graph G(M).

Think of e as a wire edge assigned to a layer L = Φ(e) by some wiring Φ inducing M. Suppose that the left e-wedge lies in a region of type V. Since e is horizontal, this means that the two edges of the other wire passing by a must lie in layers above L. Indeed, no matter whether a is a crossing or knock-knee, there is at least one of those two wire edges that is vertical and has the half incident with a included in region of type V. For the same reason, the two edges of the other wire passing by b must lie in layers below L. We represent this situation by means of a directed edge (*arc*) with origin b and terminus a (i.e., we give an orientation to e). The intuition behind the other three cases shown in Figure 11 is analogous: In every wiring inducing M, any arc of G(M) corresponds to a wire edge lying above the other wire at its origin and below the other wire at its terminus.

Note that we are not quite precise in using the notation G(M) for a graph that depends also on the particular assignment of colors to the regions of M. However, changing the assignment of colors (in the case where D is connected) simply reverses the orientation of each of the arcs (in some of the connected components of G(M)), which will be immaterial to our considerations.

If G(M) does not contain cycles, we define the *layer number* of M as

$$\nu(M) = (\text{the maximal length of a directed path in } G(M)) + 2.$$

If G(M) contains cycles then we may put $\nu(M) = \infty$. An example of such a two-colorable map is shown in Fig. 12; however, in this paper we shall no longer consider maps M for which $\nu(M) = \infty$.

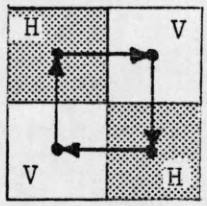


Figure 12. A two-colorable map M with $\nu(M) = \infty$.

Theorem 4. A two-colorable map M for a full layout W in D is induced by some k-layer wiring of W if and only if $\nu(M) \leq k$.

Proof. [Necessity] Let M be a two-colorable map induced by some k-layer wiring Φ of W. Consider a (directed) path $e_1e_2 \ldots e_p$ in G(M), where the terminus of e_i coincides with the origin of e_{i+1}, $1 \leq i < p$. By the definition of the orientation of arcs of G(M), in the wiring Φ the terminus of e_i has the other wire above it, and the origin of e_{i+1} has the other wire below it, which clearly means that e_i and e_{i+1} belong to distinct wires, and e_{i+1} lies above e_i. Consequently, $e_1e_2 \ldots e_p$ forms a rising staircase configuration: $\Phi(e_1) < \Phi(e_2) < \ldots < \Phi(e_p)$. Taking into account that there is in addition an edge below the origin of e_1, and an edge above the terminus of e_p, we obtain $p + 2 \leq k$. If $e_1e_2 \ldots e_p$ is a maximal length path in G(M), we get $\nu(M) \leq k$.

[Sufficiency] Conversely, suppose that M is a two-colorable map for W with $\nu(M) \leq k$, with some fixed assignment of types, H and V, to its regions. We shall show how to construct a k-layer wiring Φ inducing M (in fact, Φ will use $\nu(M)$ layers, but any ν-wiring can trivially be transformed into a ν'-wiring, $\nu' > \nu$, by simply adding superfluous layers). Let us label the layers as $B < M_1 < \ldots < M_{\nu(M)-2} < T$. For all those wire edges e that occur in G(M) we define

$$\Phi(e) = M_{h(e)},$$

where

h(e) = the length of the longest path in G(M) terminating with e.

For the other edges —clearly, each of them lies entirely in a region of one type —we put

$$\Phi(e) = \begin{cases} B & \text{if e horizontal lying in region of type V, or} \\ & \quad \text{e vertical lying in region of type H} \\ T & \text{if e horizontal lying in region of type H, or} \\ & \quad \text{e vertical lying in region of type V} \end{cases}$$

We now show that the function Φ satisfies Condition (C) of a wiring (see Section 3). Consider first the case where all four wire edges incident with v occur in G(M). Figure 13 shows all possible cases, up to a relabeling of the regions, which

reverses the orientation of all edges. We see that we can always label the two wires passing through v as w_i and w_j in such a way that for any choice of edges e,f incident with v, of w_i and w_j, respectively, ef forms a directed path in G(M). This means that $\Phi(e) < \Phi(f)$, i.e. both edges of w_j lie above both edges of w_i. For the cases involving wire edges not appearing in G(M) the condition is verified in a similar way. □

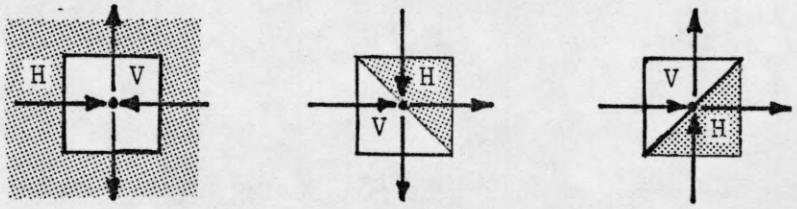


Figure 13. To the proof of Theorem 4.

The proof of the sufficiency of Theorem 4 provides an explicit method to construct a $\nu(M)$-layer wiring for a given two-colorable map M. Such wiring, using the minimum number of layers, is called a *standard wiring* of M.

We note below several immediate consequences of Theorem 4.

Corollary 5. A full layout W is k-layer wirable if and only if there exists a two-colorable map M for W such that $\nu(M) \leq k$; that is

$$\nu(W) = \min_{\substack{M \text{ is a} \\ \text{two-colorable} \\ \text{map for } W}} \nu(M). \quad \square$$

Corollary 6 [PL1,PL2]. A necessary and sufficient condition for three-layer wirability of an arbitrary layout is that there exist a two-colorable map for its core not containing any of the eight patterns shown in Fig. 14.

Figure 14. The eight forbidden patterns in the two-colorable map M with $\nu(M) \leq 3$ (a dotted diagonal is *not* in M).

Proof. Indeed, the above eight patterns are exactly those corresponding to paths of length 2 in G(M). If no such pattern exists, then all paths of G(M) have length at most 1, whence $\nu(M) \leq 1 + 2 = 3$. □

Corollary 7 [BB2]. Any layout can be wired with at most four layers.

Proof. The proof of this result [BB2] is a construction showing that, in our terminology, given a layout W, we can always find a two-colorable map M for W such that G(M) contains no path of length greater than 2; this implies $\nu(W) \leq \nu(M) = 2 + 2 = 4$. □

6. *A Characterization of Two-Layer Wirability*

Every nondiagonal edge of a two-colorable map M contributes an edge to G(M), thus implying $\nu(M) \geq 3$. An immediate consequence of this fact, using the theory developed in the preceding sections is the following theorem.

Theorem 8. A necessary and sufficient condition for two-layer wirability of an arbitrary layout W in D is that any grid point incident with an odd number of diagonals of core(W) be a boundary vertex of the layout domain D* of core(W), and that there be an even number of such vertices at every connected component of the boundary of D*. □

An example of a layout that is two-layer wirable, and of another one that is not (but *is* three-layer wirable) are shown in Fig. 15.

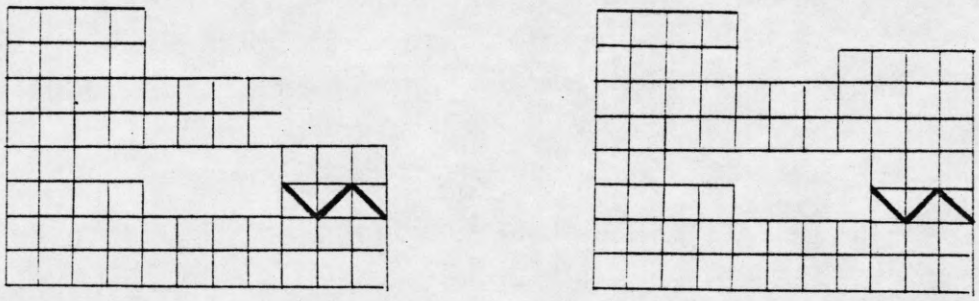


Figure 15. (a) A two-layer wirable layout. (b) A layout that is not two-layer wirable (but is three-layer wirable).

Trivially, a sufficient condition for two-layer wirability of W is that it contain no knock-knee; in this case the diagonal diagram of core(W) is empty and the conditions of Theorem 8 are clearly satisfied. This is exactly what happens with *Manhattan layouts*, which are the subclass of knock-knee layouts from which knock-knee grid points are forbidden. Indeed, in a Manhattan layout all horizontal wires are wired in one layer and all vertical wires in the other, with vias established where wires bend.

It is clear that under any reasonable representation of W, all the operations necessary to verify the conditions of Theorem 8 can be implemented in

linear time. Hence we obtain the following corollary.

Corollary 9. Two-layer wirability of an arbitrary layout W in D can be tested in time linear in the number of tiles in D. □

This result should be contrasted with the fact that testing for three-layer wirability is NP-complete [Lip].

Let W be any layout in D, and consider a horizontal straight line P composed of horizontal tile edges. By a *horizontal elementary stretching* along P we shall mean the operation that modifies the layout in the following way: We cut D along P, move its pieces vertically one tile space apart, and insert, at every place where a wire of W was crossing P, a layout tile ⊞. A *vertical elementary stretching* is defined in a similar way (P is now vertical, and the layout tiles added are ⊟). By a *stretching* of W we shall mean the result of applying any sequence of horizontal and vertical elementary stretching operations.

Let E be the set of those internal vertices of the layout domain of core(W) that are incident with an odd number of diagonals. (Incidentally, note that the "odd number" means here in fact "one", since if v is a vertex incident with three diagonals, then the fourth of the tiles surrounding v involves edges of a single wire, and hence it is not included in the layout domain of core(W).) Consider any stretching W' along a collection of horizontal and vertical lines covering E. Clearly, W' satisfies the first part of Theorem 8, since every vertex in E has been split into two boundary vertices of the layout domain D* of core(W'). To satisfy the second part it is sufficient to further stretch W' along a set of lines that touch all those connected components of the boundary of D* that violate this second part.

It may be noted that the problem of finding a minimum cardinality set of horizontal and vertical lines covering E is equivalent to the classical combinatorial problem of covering all ones in a (0,1)-matrix by a minimum number of lines (rows and columns). This minimal number is equal to the maximal number of ones, no two in a line. This problem, being closely related to maximum matchings in bipartite graphs, can be solved efficiently, see e.g. [LLLMP].

Corollary 10. Given any layout W in an m × n rectangle of tiles, there exist (2m−1) × n and m × (2n−1) stretchings of W that are two-layer wirable.

Proof. It is sufficient to consider the stretchings along a collection of m − 1 horizontal lines separating all rows, and n − 1 vertical lines separating all columns of the rectangle, respectively. In each of the two resulting stretchings, every diagonal joins two vertices on the same connected component of the boundary, hence Theorem 8 applies. □

We observe that the wiring schemes of Rivest *et al.* [RBM] for channel routing and of Mehlhorn and Preparata [MP] for rectangle routing are covered by Corollary 10.

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