IN-SENSOR INFORMATION PROCESSING FOR RESOURCE-LIMITED PLATFORMS ON FLEXIBLE EPIDERMAL SUBSTRATES

BY

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THESIS

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ABSTRACT

Moving towards the age of big data, the demand for embedded processing has been drastically increasing to make inference and intelligent decisions at lower architectural layers. The myriad of health conditions that can be treated and analyzed via low-energy embedded information processing kernels drives the demand for biomedical circuits, with optimized performance and cost. A large class of these healthcare applications require digital signal processing algorithms to be implemented with strict resources, such as energy and silicon area. Shrinking technology nodes produce both higher computing performance and energy efficiency. However, energy delivery and communication circuitry have not benefited significantly from technology scaling due to different sets of figures of merit. In-sensor information processing can be utilized to lower the energy consumption of such systems by eliminating the redundant volume of data traffic between the sensors and the central processing station. This work focuses on embedding intelligence on the epidermal flexible substrates to extract and analyze critical biomedical information for in-situ diagnosis. The primary objective of this work is illustrating the advantages of epidermal electronics combined with robust information processing systems, at system and application level. The major challenge is the design of robust and efficient algorithms for reliable operation on resource limited hardware platforms and flexible substrate non-idealities. To do so, we developed the first in-sensor ECG and PPG processors on flexible epidermal substrates. The systems are first prototyped using discrete components, followed by an ASIC implementation. Measurement results show that the in-sensor information processing has reduced the transmitted data traffic by $150X$, and the system energy consumption by $3.56X$.

To my parents, for their love and support.

ACKNOWLEDGMENTS

First and foremost, I would like to express my sincere gratitude to my advisor, Professor Naresh R. Shanbhag, for continuous guidance and invaluable comments. I would also like to acknowledge the SONIC center for funding and support of this research. This work would have not been possible without the help of Professor John A. Rogers for designing and providing access to flexible epidermal electronics platforms.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 Motivation

In the age of big data, the demand for embedded processing applications has been drastically increasing to collect information via networked sensors and make intelligent decisions [1], [2]. Emerging sensory-based technologies such as the Internet-of-things and wearable biomedical devices are examples of this trend [3]. A large class of battery-powered embedded processioning applications require digital signal processing (DSP) algorithms and architectures to be implemented under strict energy constraints [4]. This is because standby time is a crucial specification that directly affects the user experience as well as the effectiveness and reliability of these systems. Moreover, the silicon area factors directly in the manufacturing cost of such systems and needs to be reduced in order to increase revenue.

Technology scaling leads to smaller and faster transistors that result in both higher computing performance and energy efficiency [6]. However, electronics that process energy (i.e., power converters) and radio communication circuitry have not benefited from technology scaling due to their reliance on different sets of figures of merit [1]. Therefore, the power electronics and radio communication circuitry components are consuming increasingly higher energy and area. As predicted by the ITRS 2011 [5] (see Fig. 1.1) the power density of computing platforms will be continuously increasing. The demand for keeping up with such standards requires a paradigm shift in the design and implementation of the information processing and peripheral circuitry. One way to enhance energy efficiency is to increase the computational capacity at sensory layers [1], [7]. Figure 1.2 compares the network architecture of central and an embedded processing configurations. The key idea of such in-sensor computing is to design a system to achieve in-situ robust

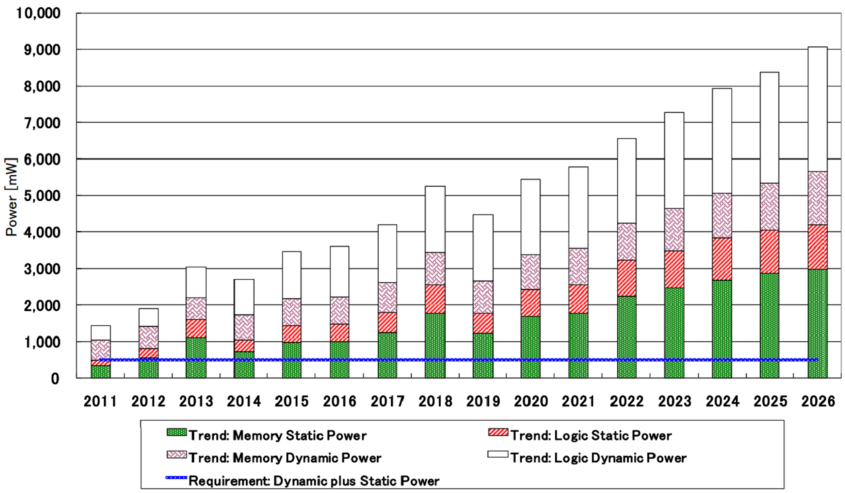

Figure 1.1: Power density trend of computing platforms [5].

and energy-efficient computing by means of reducing data traffic and eliminating the need for a more complex central processing. This development is oriented towards investigating the idea of employing in-situ information processing and transferring the maximum amount of intelligence to the sensor level, in order to minimize the volume of processed and transmitted data off of the sensory platform. The algorithms are designed to identify and transmit specific health-related features and partially processed data instead of raw data for a low power and reliable in-situ diagnosis.

The myriad of health conditions that can be analyzed via electronic devices [8], [9] drives the demand for portable embedded processing applications as they clearly provide valuable information for medical diagnosis. In particular, digital signal processing (DSP) systems in health monitoring, such as monitoring and analysis of electrocardiogram (ECG) [10] biopotential for detecting early stages of cardiovascular diseases (CVD), have gained popularity in recent years. The limited bandwidth of biopotential signals in the order of 1 MHz or less [11] and the low data rate make it possible to use embedded platforms for in-situ reliable and energy efficient information processing. The key innovation of this work is integration of resource-limited information processing systems on flexible epidermal substrates for wearable biomedical applications.

A typical block diagram of an embedded biomedical electronic device is shown in Fig. 1.3. At the front-end, the data acquisition layer consists of sensors, multiplexers, amplifiers, analog filters and data converters which feed

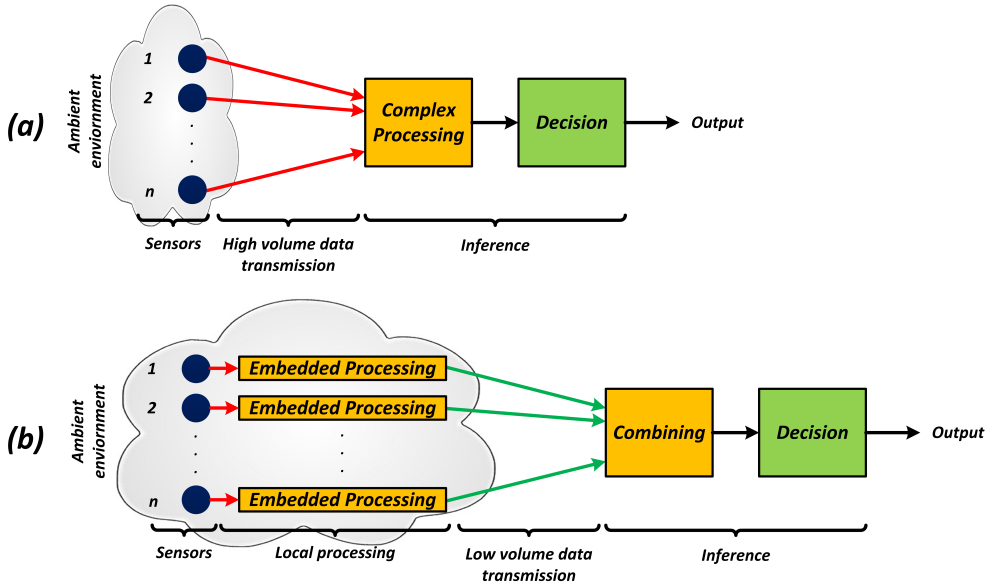

Figure 1.2: Sensors network architecture: (a) central processing, and (b) embedded processing.

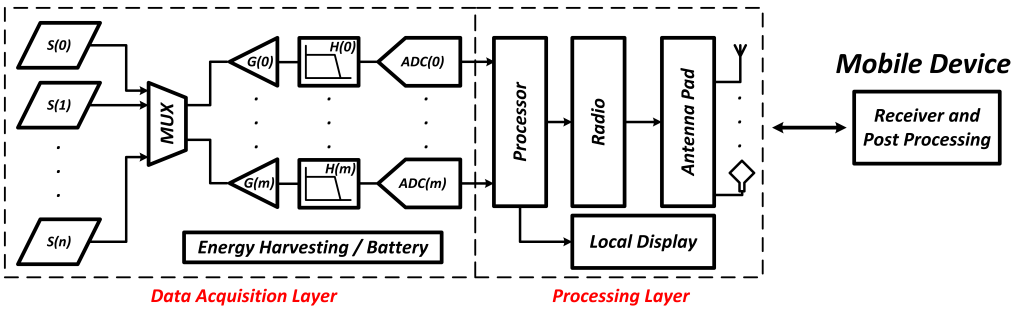

Figure 1.3: Conventional embedded electronics system.

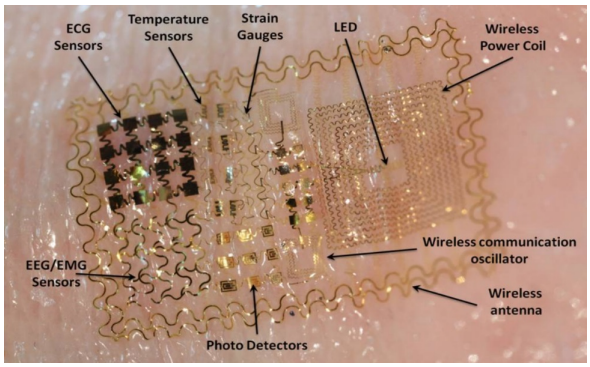

Figure 1.4: The ECG sensor built on flexible epidermal substrates [3].

the processing layer with a suitable biosignal for inference and information extraction [11]. The extracted information can be utilized locally for further actions and diagnosis such as applying treatments or transmitted over a channel [2] to a remote receiver for further analysis and monitoring. The designed ECG information processing system in this work follows a similar architecture.

The recent development of skin-conformal epidermal electronics [3] has the potential to revolutionize medical science. The technology is attractive for embedded biomedical system development because of its unique capability to integrate sensors and processors on the same substrate, while providing properties that allow the system to be conformal [12] with human skin, as shown in Fig. 1.4. Clinical studies have shown that similar or even better signal quality can be achieved using the flexible epidermal substrates [3] compared with conventional sensors. The main disadvantage of this technology is the lack of flexible energy storage devices. The energy delivery is conventionally realized through implantable nano-batteries or active energy harvesting systems. One of the objectives of this work is silicon integration of the proposed system architecture on the flexible epidermal substrates.

1.2 ECG Processor using Pan-Tompkins Algorithm

Real-time monitoring and analysis of ECG biopotential signal is expected to have a significant impact on personal healthcare by enabling expert intervention in early stages of CVD. The ECG biopotential signal consists of periodic Q, R and S (QRS) wave complex [11], [13]. Accurate real-time QRS-complex

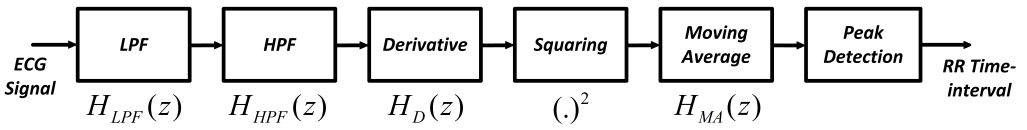

Figure 1.5: PTA signal chain.

detection and beat-to-beat (RR-interval) extraction are the basis for heart monitoring devices and CVD classification algorithms. Several algorithms have been proposed for RR-interval feature extraction, such as genetic algorithms, neural networks, wavelet transform and derivative-based methods. The Pan-Tompkins Algorithm (PTA) [13] is a derivative-based method that has gained popularity because of its robustness and simplicity for VLSI implementation.

The PTA consists of noise-removal filters, a derivative and squaring pre-emphasis filter, a moving average filter and a RR-interval peak detection block, as shown in the signal chain of Fig. 1.5. In order to maximize the QRS-complex detection probability, the signal is filtered through a noise removal 5 Hz to 15 Hz bandpass filter, realized by cascading highly selective IIR lowpass $H_{LPF}(z)$ and highpass $H_{HPF}(z)$ filters with cutoff frequencies at 15 Hz and 5 Hz, respectively. It is important to note that the filters should impose minimum phase distortion on the QRS-complex signal. This noise removal process improves the QRS-complex signal SNR by removing noise components, such as motion artifacts, flicker noise, 60 Hz noise and their harmonics [14]. The derivative stage is a pre-emphasis highpass filter $H_D(z)$, which amplifies the high frequency components of the ECG signal in order to amplify the R-peak for a more accurate RR-interval detection and attenuation of other ECG waves. The signal is then squared and lowpass filtered using a moving average $H_{MA}(z)$ operation to attenuate the unwanted frequency bands. This signal chain can be directly employed to design a VLSI architecture. For simplicity of design and enabling low-power operation, the filters are designed using mostly adders. The transfer functions of all stages of the PTA signal-chain [13], [10] are presented in Table 1.1 for a sample rate of 200 samples/sec.

The time-domain filtered signal is then passed through a RR-interval peak detection block, with a predefined optimal threshold, to accurately extract the RR-interval times. The PTA does not require data segmentation and

Table 1.1: Transfer functions of the signal chain blocks in PTA architecture of Fig. 1.5.

Block	**Transfer function**
HPF Stage	$H_{LP}(z) = \frac{1-2z^{-6}+z^{-12}}{1-2z^{-1}+z^{-2}}$
LPF Stage	$H_{HP}(z) = \frac{-1+32z^{-16}+z^{-32}}{1+z^{-1}}$
Derivative Stage	$H_{D}(z) = \frac{-z^{-2}-2z^{-1}+2z^{1}+2z^{2}}{8}$
Moving Average Stage	$H_{MA}(z) = \frac{1}{32}\sum_{i=0}^{31} z^{-i}$

training; however, it satisfies the detection metrics commonly used in evaluation of the biomedical procedures [13]. The metrics involved in selection of optimum threshold value consist of the of true positivity rate Se and sensitivity ${}^{+}P$, defined by:

$$Se = \frac{TP}{TP + FN}$$
$${}^{+}P = \frac{TP}{TP + FP}$$

where TP, FP and FN are the true-positive, false-positive, and false-negative events, respectively. Clinical requirements set the minimum level of detection and positivity rate at 95% [13]. Thus, the algorithms and system architectures should be designed to satisfy the clinical requirements. The extracted RR-interval times are then utilized to classify abnormal heart-rate activities. The set of thresholds applied to the filtered ECG biopotential signal in the peak detection block are computed by the following equations:

$$SPK[n] = 0.125PEAK[n-1] + 0.875SPK[n-1]$$
$$NPK[n] = 0.125PEAK[n-1] + 0.875NPK[n-1]$$
$$TR1[n] = NPK[n-1] + 0.25(SPK[n-1] - NPK[n-1])$$
$$TR2[n] = 0.5TR1[n]$$

where SPK is the running estimate of the signal peak, $PEAK$ is the local maximum detected peak, NPK is the running estimate of the noise peak which included any peak that is not related to QRS-complex (e.g., the T wave), $TR1$ is the first applied threshold and TR is the second applied threshold. When a new peak is detected, it must first be classified as a noise peak or a signal peak. A signal peak is detected as the peak that must exceed

$TR1$ or $TR2$ if searchback is required to find the QRS-complex. When the QRS-complex is found using the second threshold, then SPK is computed using the following equation:

$$SPK[n] = 0.25PEAK[n-1] + 0.75SPK[n-1]$$

For irregular heart rates, the first threshold is reduced by half to increase detection sensitivity and to avoid missing beats. The coefficients used in the computation of threshold are designed to achieve the highest Se and ${}^{+}P$ for the set of test vectors provided by the MIT/BIH database, which consists of 24 hours of ECG biopotential signal recording of 48 patients. Table B.1 shows the performance of PTA with overall 0.675% detection failure rate [13] using this database, which sets both Se and ${}^{+}P$ above 99%. However, the coefficients can be recomputed for specific sets of test-vectors to achieve even higher performance. Table B.1 is used as a performance benchmark in evaluating a modified PTA ECG processor for real-time operation on resource-limited hardware platforms.

1.3 Optical PPG Processor for Systolic Blood-Pressure

Systolic blood-pressure is a critical parameter in monitoring the health state of patients with significant impact on preventing healthcare [11]. The changes in systolic blood-pressure can be analyzed through indirect measurements of blood velocity [15]. As shown in Fig. 1.6, the blood velocity can be measured by time delay estimation (TDE) between two photoplethysmogram (PPG) biopotential signals [16], which are collected through placement of two optical sensors spatially apart by distance $L1$ on top of the same blood stream. The PPG biopotential signals $x_1(t)$ and $x_2(t)$ are non-stationary signals with periodic components. The PPG biopotential signal measured at every heartbeat cycle can be used in a recursion to compute the absolute systolic blood-pressure, where the initial seed is required by cuff blood-pressure measurement [16]. The equations below show this recursive relation:

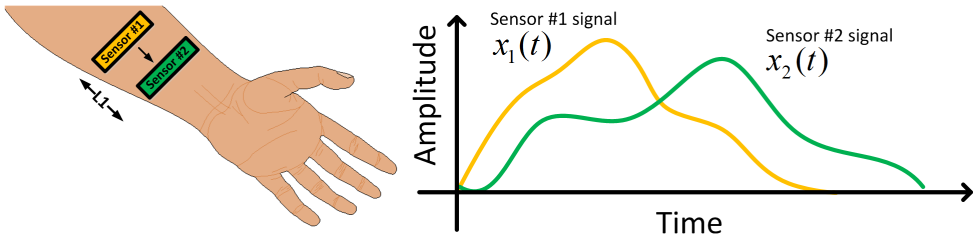

Figure 1.6: PPG biopotential signal test-setup with sensors placed spatially apart at distance L1.

$$P[n] = P[n-1] + \delta P[n]$$
$$\delta P[n] = f(T_{delay}[n], T_{delay}[n-1])$$
$$T_{delay}[n] = Delay(x_1(t), x_2(t))$$

where $P[0]$ is the initial cuff blood-pressure measurement, $P[n]$ is the running systolic blood-pressure, $P[n-1]$ is the systolic blood pressure from last heartbeat cycle, $\delta P[n]$ is detected change, $T_{delay}[n]$ and $T_{delay}[n-1]$ are the current and previous heartbeat cycle TDE between the PPG biopotential signals $x_1(t)$ and $x_2(t)$. The function $f(T_{delay}[n], T_{delay}[n-1])$, as found in literature [16] [15], relates TDE to $\delta P[n]$ with a first order linear relation of physical and biological parameters including the distance $L1$ between the sensors and blood vessels stiffness. Figure 1.7 shows the continuous estimation of systolic blood-pressure using the conventional pulse arrival time method [16] for TDE calculation, which requires high sampling rate and resolution of the PPG biopotential signals. However, resource limited hardware platforms, running under strict power requirements, lack the capability of sampling and processing at high rates and resolution. The requirement of accurate TDE calculation can be accommodated using variety of approaches. Adaptive filer channel delay extraction [17], parametric methods such as template matching and, derivative-based [18] and non-parametric methods such as neural network [19] are reported in the literature. However, they all suffer from high computational complexity for real-time operation on resource-limited hardware platforms. Thus, this work develops a computationally low complexity, and yet accurate, cross-correlation based algorithm compatible with the limited available resources to achieve in-sensor detection of the changes in systolic blood-pressure $\delta P[n]$ in real-time.

The proposed method for TDE calculation of the PPG biopotential signals

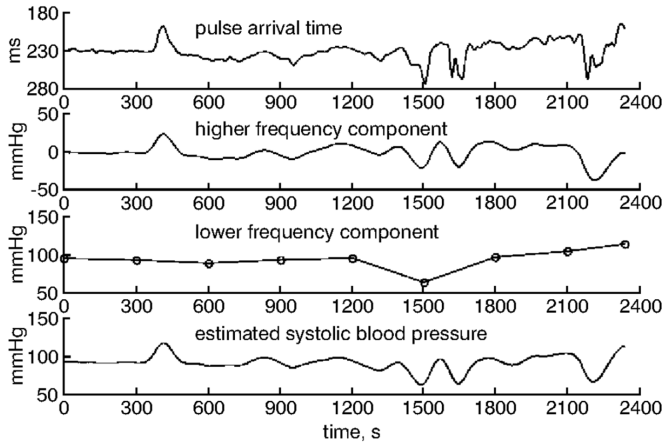

Figure 1.7: Continuous estimation systolic blood-pressure [16] using the pulse arrival time method for TDE calculation.

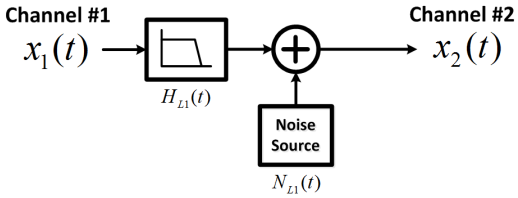

Figure 1.8: PPG biopotential signal noisy channel model.

developed in this work is based on modeling the blood vessels as a noisy communication channel shown in Fig. 1.8. Thus, signals $x_1(t)$ and $x_2(t)$ are related using the following equation:

$$x_2(t) = x_1(t) * H_{L1}(t) + N_{L1}(t)$$

where $H_{L1}(t)$ is the time-domain response of the blood vessel, $N_{L1}(t)$ is the coupled noise and $*$ represents the convolution of the $x_1(t)$ signal. As shown in Fig. 1.9, the raw PPG biopotential signals are collected through optical measurements of reflected light incident from the blood vessels using two sensors with sampling rate of 4 kS/s and $L1 = 2$ cm. The upstream sensor emits red light and the downstream sensor uses IR radiation. The selection of radiation sources with different wavelengths is critical to minimize the sensed leakage noise across the two sensors.

Figure 1.9 shows that the PPG biopotential has a significant noise and DC-offset drift in the time. Thus, a real-time filtering and scaling of the signal is required. The PPG biopotential signal frequency spectral content has a

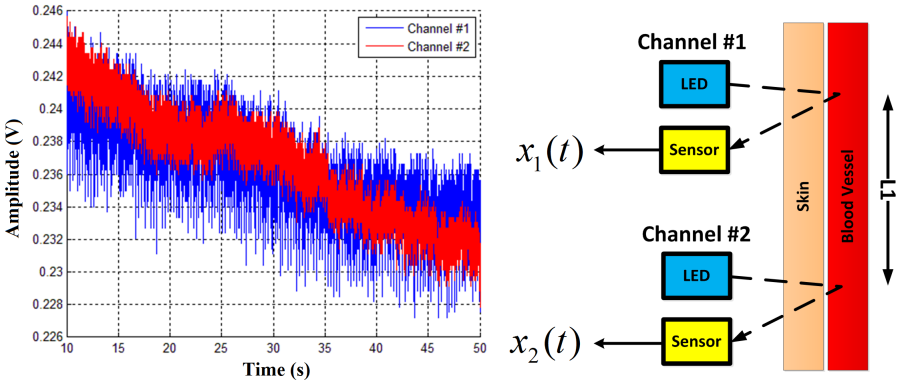

Figure 1.9: Recording of raw PPG biopotential signals.

bandwidth of 0.05 Hz to 4 Hz [16]. The lack of a reliable PPG biopotential signals application for calculating the systolic blood-pressure in the literature has limited the performance benchmarking of the designed system. Thus, the performance evaluation of this work is limited to use of PPG biopotential signals collected in the lab.

1.4 Thesis Organization

The first chapter introduced the basis of PTA and optical systolic blood-pressure measurement and the motivations for designing a system capable of in-sensor information processing. Chapter 2 focuses on implementation of a modified PTA and optical systolic blood-pressure processor using resource limited discrete components on flexible epidermal substrates. Chapter 3 focuses on ASIC implementation of the designed optical systolic blood-pressure system, including the analog front-end, digital back-end processing and a passive near-field communication (NFC) transmitter. Finally, Chapter 4 concludes this work with proposed future directions for the design and improvement of a fully on-chip optical systolic blood-pressure ASIC.

CHAPTER 2

DESIGN AND DISCRETE IMPLEMENTATION OF IN-SENSOR ECG AND PPG PROCESSORS

2.1 Introduction

This chapter focuses on the design, implementation and testing of the in-sensor ECG and PPG processors using off-the-shelf components. The systems are prototyped and tested on the flexible epidermal substrates for performance benchmarking. The main focus of this chapter is feasibility study and development of the proposed systems for further ASIC implementation discussed in Chapter 3.

2.2 ECG Processor

This section focuses on the design and implementation of a simplified PTA for real-time operation on flexible epidermal substrate to meet application requirements.

2.2.1 Application Requirements

The ECG processor system for R-peak detection has to be designed to meet the required clinical standards of achieving Se and ^{+}P detection rates of 95% or higher and RR-interval time resolution of 10 ms or less [13]. Additionally, the system clinical test-setup requires wireless power delivery through coupled coils at maximum distance of 30 cm. The operating frequency should be chosen at an unlicensed band, such as 13.56 MHz of NFC systems. The number and footprint of discrete components mounted on the flexible epidermal substrate should be limited in order to increase the reliability and lifetime of the system, as they go through mechanical stress. The RF430FRL152H

NFC chip [20], made by Texas Instruments, has been chosen because it is capable of receiving and transmitting information through the same coil that powers the chip. This feature helps shrink the form factor of the flexible epidermal substrate by only implementing a single loop-antenna. The NFC chip specifications are listed in Table 2.1.

Table 2.1: RF430FRL152H specifications.

Feature	Specification
Power Supply	13.56 MHz H-Field Supply
Supply Voltage	1.45 V to 1.65 V
Power Consumption	140 μA/MHz (1.5 V)
Architecture	16-Bit RISK
CPU System Clock	1 MHz
ADC	14-Bit Sigma-Delta
SRAM	4kB

Given the limited computational capability of NFC chip, the PTA should be tailored for real-time operation at 200 S/s, corresponding to 5 ms RR-interval resolution [10], while satisfying the required clinical Se and ^{+}P detection rates. This sample rate is also chosen because it is twice the bandwidth of an ECG biopotential signal [11]. The discrete-time filters of PTA are designed to use powers of 2 coefficients at 200 S/s, which makes them multiplierless and hence suitable for VLSI implementation [10]. The effective streaming data buffer-length of PTA is found to be as large as 89, excluding the peak detection block. The effective buffer-length is defined as the largest memory depth used for a single computation of the PTA signal-chain. As a result, the presented MCU architecture is not suitable for computation of long buffer lengths, because of its limited working registers. Therefore, frequent RAM access and consequently lower system real-time throughput is expected. To achieve real-time information processing, the filtering blocks have to be redesigned to approximate the PTA transfer functions at a minimum sample rate of 200 S/s. Doing so will degrade the QRS-complex SNR and increase the detection failure rate, yet guarantee Se and ^{+}P clinical requirements. In the next sections, the NFC chip computational capability is characterized for real-time operation at the rated throughput, followed by design of the modified PTA for real-time operation on the NFC chip.

2.2.2 NFC Chip Characterization for Real-time Operation

The two critical parameters in achieving real-time filtering on the NFC chip are the data type used in the implementation of discrete-time filters, and the overall effective buffer-length. The data type used in the implementation of the for-loop should be strictly limited to 16-bit fixed-point *int* data type, while 32-bit floating-point *double* data type should be reserved only for sensitive blocks, such as stable IIR filtering, because of its significantly higher computational cost in a 16-bit RISC processor. Because the NFC chip datasheet has not provided detailed architectural specification of the CPU, the hardware limitations are investigated through experimental procedures. A simple for-loop can be used to determine the NFC effective buffer-length for real-time operation at 250 S/s, which is the closest available sample rate above 200 S/s. This for-loop should include the end-to-end kernels needed in implementation of PTA, which includes ADC read, addition, multiplication and memory read/wright. Table 2.2 shows the maximum allowed buffer-length under different configurations of a FIR filter implementation. It is important to note that the IIR filter implementation has similar computational cost depending on the type of configuration used in its recursive and non-recursive blocks.

Table 2.2: Maximum allowable buffer-length for real-time operation.

Configuration	*int* Add	*double* Add	*int* Mult	*double* Mult	Bit-Shift Mult	Buffer-Length
#1	N	Y	N	Y	N	11
#2	Y	N	Y	N	N	27
#3	Y	N	N	N	Y	58

Table 2.2 can be used to assign computational costs to each of the operations needed in the design of the modified PTA. Note that use of working resisters is a direct function of implemented functions and coding style. The developed system is programmed using TI-Assembly, and maximum use of working registers has been made. It is expected to have variations in architecture complexity and performance among different coding styles. Table 2.3 shows an approximate normalized cost per operation derived from Table 2.2. Additional coding structures presented in 2.3, such as ADC read conditional statements and NFC data transmission, can be characterized using a similar experimental procedure.

Table 2.3: Normalized cost of PTA kernels.

Function	FIR/IIR (*double*)	FIR/IIR (*int*)	FIR/IIR (*int* Bit-Shift)	NFC	ADC	Conditional
Normalized cost	0.091	0.037	0.017	0.003	0.002	0.002

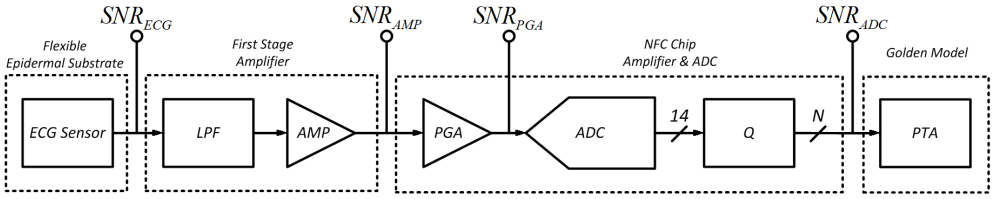

Figure 2.1: AFE signal-chain.

2.2.3 Modified PTA for Real-time Operation

The hardware implementation of PTA has been shown to be compatible with the clinical requirements of achieving Se and ^{+}P values of 95% or above [10]. Therefore, any custom analog-front-end (AFE) and digital-back-end (DBE) processing hardware implementation of PTA should be optimally designed to harvest the algorithm capabilities. In this section, the PTA is redesigned to make its real-time operation compatible with the clinical requirements, given the computational costs of Table 2.3. The design cycle is initiated by identifying and characterizing the AFE followed by DBE processing architectures. Finally, the design is optimized to make use of maximum available resources, and prototyped on the flexible epidermal substrate for performance benchmarking.

Analog-Front-End:

Architectural complexity of the DBE processing is directly dependent on the performance metrics of the AFE, including the linearity, phase distortion, SNR of the processed analog QRS-complex analog signal [14] over the AFE effective bandwidth and selection of appropriate output swing sensible by ADC. Thus, the AFE is as important as the DBE to satisfy the clinical requirements. The initial step in characterizing the AFE is calculation of the link-budget. Figure. 2.1 shows the complete signal-chain of AFE starts from the ECG sensor directly connected to the first-stage amplifier followed by the programmable gain amplifier (PGA) and ADC of the NFC chip.

Given the fact that the flexible epidermal ECG sensors have been shown

to have similar or better performance compared with the conventional ECG sensors, the signal-chain analysis begins by making the assumption of 0 dB gain of flexible epidermal ECG sensors. An ECG biopotential signal database of 20 recordings, with each recording running up to 1 min, is collected using both the conventional and flexible epidermal ECG sensors. The database is collected with careful placement of both the conventional and flexible epidermal ECG sensor on the left side of the chest, directly above the heart. This database includes the artifacts due to loosely connected sensors [12], in order to stimulate the worst-case scenario. Figure 2.2 compares the distribution of ECG biopotential signals maximum peak-to-peak swing, as well as the QRS-complex signal SNR. The SNR is defined as the ratio of the QRS-Complex signal power on the 5 Hz to 15 Hz frequency band to the ECG biopotential signal of 0.5 Hz to 100 Hz frequency band [11]. The ECG biopotential signals peak-to-peak swing is marked by the vertical lines to indicate the average and limits of motion artifact outliers. The plots suggest a higher mean envelop peak-to-peak swing for the conventional ECG sensor, which is because of greater sensor area and stronger electrical connectivity to skin [11]. In order to capture the ECG biopotential signals with highest resolution, a portion of abnormally large envelope peak-to-peak swings, corresponding to motion artifact, were ignored in order to increase the AFE voltage gain. As shown in Fig. 2.2, the captured QRS-complex SNR from both types of ECG sensors are comparable, where the flexible epidermal ECG sensor has an average of 1.6 dB lower SNR.

The ECG biopotential signals should be filtered and amplified to the maximum voltage scale allowable, with minimum SNR distortion, prior to being sampled by the NFC chip embedded ADC. The first-stage amplifier is a cascade of BPF followed by a gain stage with effective -3 dB bandwidth of 0.5 Hz to 100 Hz. This BPF acts as a loose anti-aliasing filter for the ADC as well. An automatic gain control scheme has not been used because it will require a larger number of external discrete components on the flexible epidermal substrate. In addition, the ECG biopotential signal envelope can provide critically important information in health monitoring of patients [11].

The INA333 [21] precision rail-to-rail instrumentation amplifier, made by Texas Instruments, is used for this purpose. Table 2.4 lists the key features of this amplifier. This chip is equipped with an internal RF frequency filter, which makes it suitable for operating in high noise environments, such as the

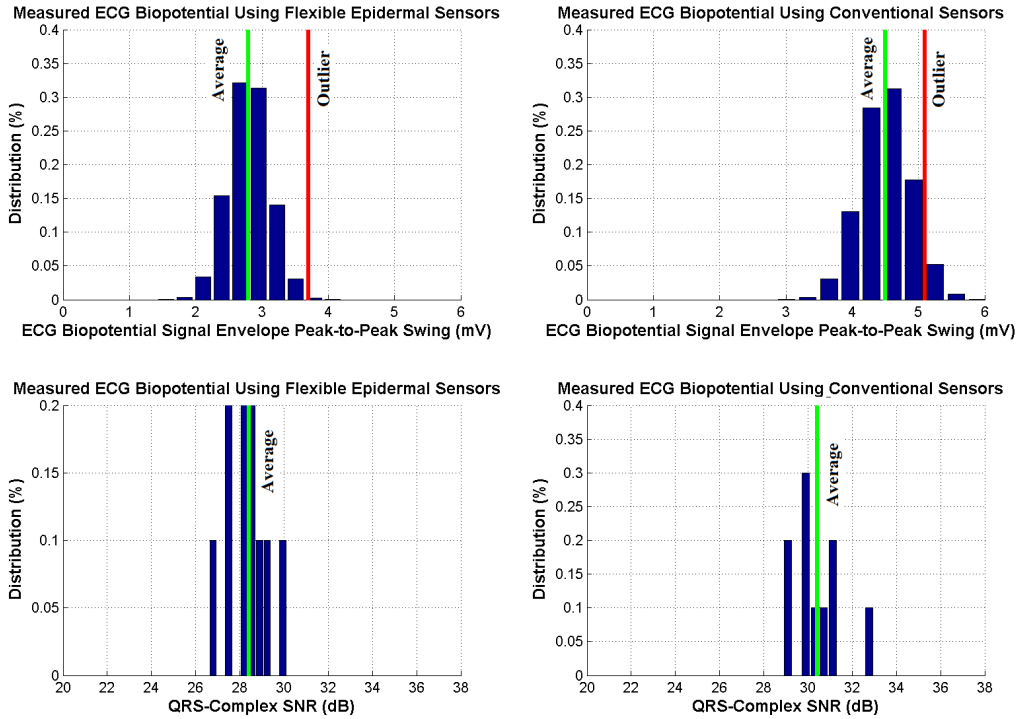

Figure 2.2: The captured ECG biopotential signal envelope peak-to-peak swing and SNR using conventional and flexible epidermal ECG sensors.

proposed NFC 13.56 MHz system.

Table 2.4: INA333 amplifier specifications.

Feature	Specification
Supply Voltage	1.8 V to 5.5 V
Power Consumption	50 μA
Low Noise	50 nV/sqrtHz
Low Offset Voltage	25 μV
Low Input Bias Current	200 pA
High CMRR	100 dB

Both the first-stage amplifier and the PGA have negligible rated noise-figure (NF) of 1.8 dB and 1.1 dB, respectively, at the frequency band of interest. To obtain the lowest NF in the AFE signal-chain, the first-stage should have a significantly larger gain compared with the PGA. The PGA is set to the maximum voltage gain of 8 because of its extremely low NF. Considering the maximum ECG biopotential signal envelop peak-to-peak swing of 3.7 mV, measured using the flexible epidermal ECG sensor, a gain of approximately 30 is required by the first-stage amplifier to obtain a maximum

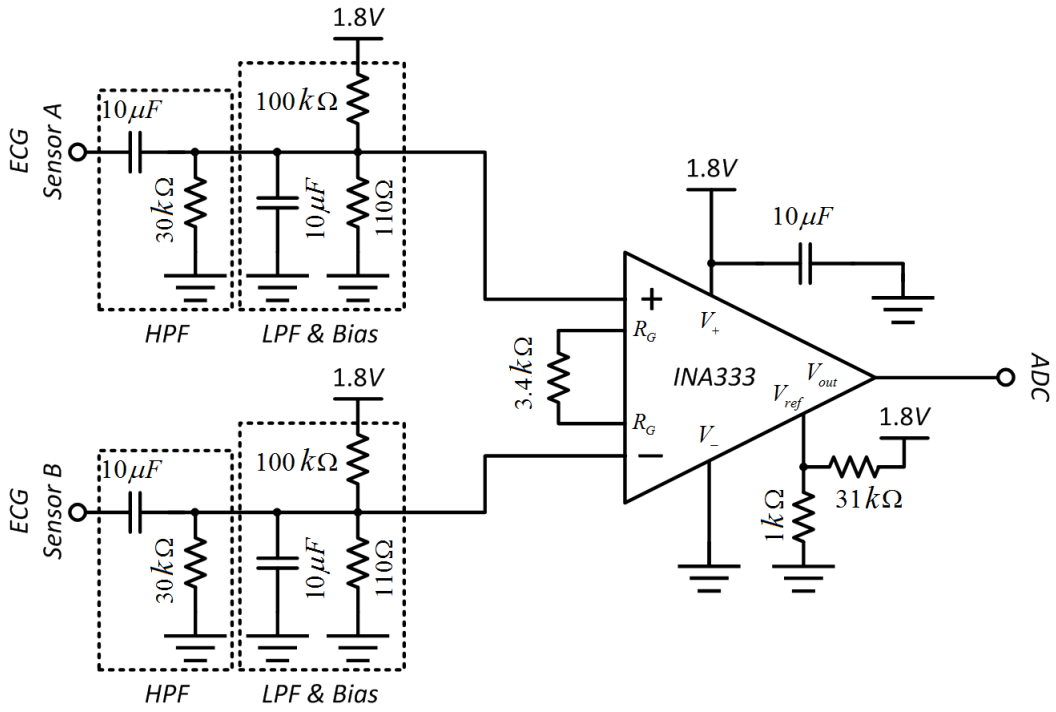

Figure 2.3: First-stage amplifier circuit schematic.

peak-to-peak voltage swing at 900 mV of the ADC reference voltage. This is an overall gain of 2400. The first-stage amplifier and its input BPF are shown in Fig. 2.3.

The input BPF of the first-stage amplifier consists of a HPF and LPF with -3 dB cut-off frequencies at 0.5 Hz and 100 Hz. The input resistive voltage-bias networks are tuned to 1.8 mV, half of the desired ECG biopotential signal envelope peak-to-peak swing, in order to prevent the collected signal from clipping to ground rail voltage. The V_{ref} signal is connected to a resistive bias network to set the output DC-offset at 56 mV. This bias voltage is half of the ADC 900 mV reference voltage divided by PGA gain of 8 to obtain maximum symmetrical signal swing at the output. The 1.8 V supply of the first-stage amplifier is provided by the NFC chip V_{DDH} terminal. Fine adjustments will be required when the system is transferred to the flexible epidermal substrate in order to obtain the best results. The largest available bypass capacitor of 10 μF in 0402 MLCC packaging was used to provide a stable bias network at the input and -68 dB of PSRR for the first-stage amplifier. The amplifier was tested under 10 recordings, each running up to 1 min of ECG biopotential signal with motion artifacts. Figure 2.4 shows the

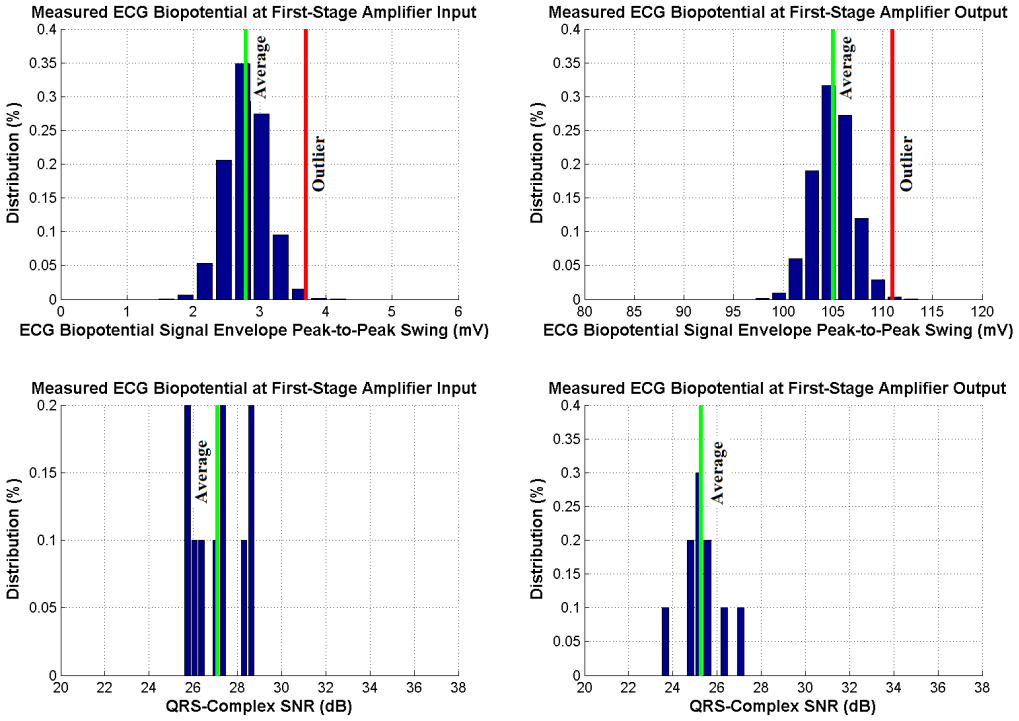

Figure 2.4: The captured ECG biopotential signal envelop peak-to-peak swing and SNR using flexible epidermal ECG sensor at input and output of the first-stage amplifier.

input and output ECG biopotential signal envelope peak-to-peak swing and the QRS-complex SNR distributions. The QRS-complex SNR was degraded by 2.1 dB to mean value of 27.1 with 1.2 dB standard deviation.

In the next step, the NFC chip with PGA and ADC is used to sample the amplified ECG biopotential signal. The relatively high resolution of the 14-bit embedded ADC that provides SQNR=76.4 dB as calculated in the equation below:

$$SQNR = 6B_{ADC} + 4.8 - PAR_{ECG}$$

where B_{ADC} is the ADC 14-bit quantization and PAR_{ECG} is the peak-to-average (PAR) power ratio of ECG biopotential signal at 10.4 dB at the output of the PGA. The ADC quantization noise can be ignored when compared with the QRS-complex SNR. The amplified ECG biopotential signal is sampled and analyzed for the DBE processor design. Figure 2.5 shows the sampled envelope peak-to-peak swing and SNR of ECG biopotential signal using the NFC chip. The output of PGA is expected to suffer from a

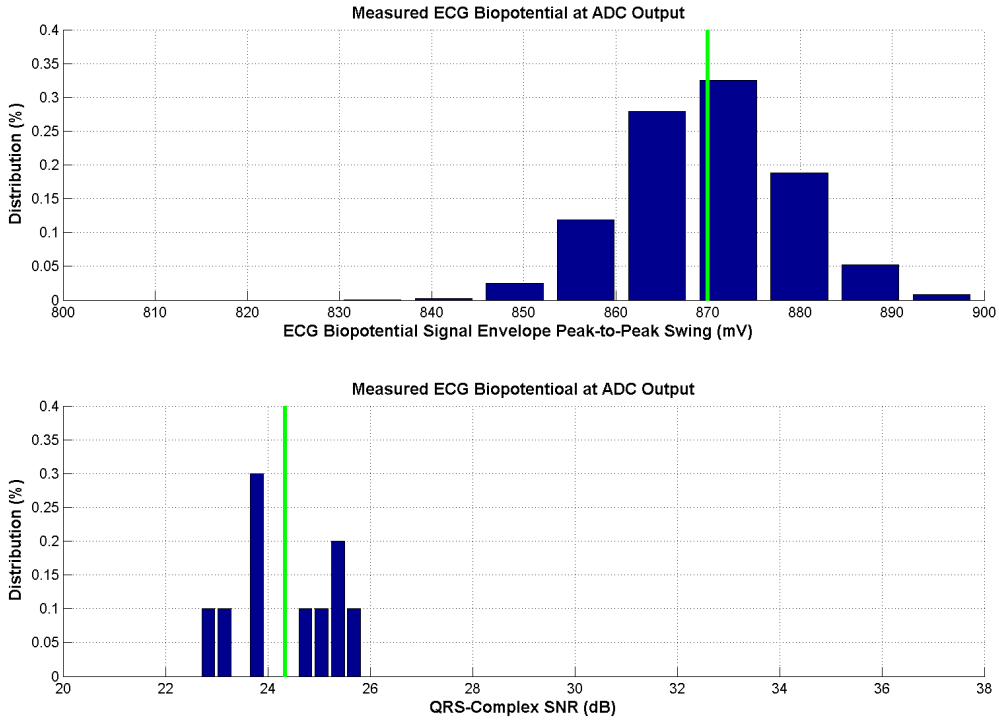

Figure 2.5: The captured ECG biopotential signal envelop peak-to-peak swing and SNR using flexible epidermal ECG sensor at output of the NFC chip embedded ADC.

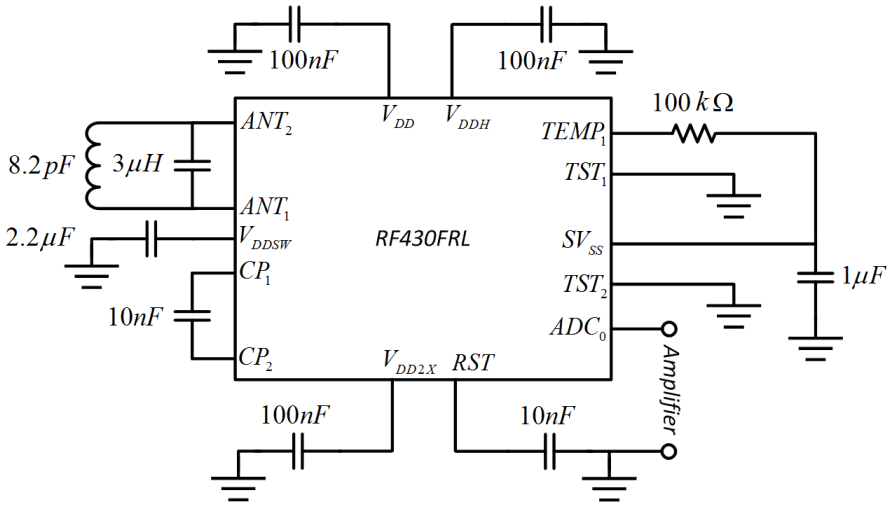

Figure 2.6: NFC chip circuit schematic.

small SNR degradation because of its 1.1 dB NF and moderate gain. With a symmetrical peak-to-peak swing of 870 mV and 450 mV DC-offset, then the QRS-complex signal SNR of 23.8 dB is available for DBE processing. The embedded ADC of NFC chip has maximum sampling rate of 2 kS/s. The ADC is equipped with a programmable sampling frequency and CIC filter stages. The ADC setup registers are set to bypass the CIC filter stage and sampling frequency of 250 S/s. Figure 2.6 shows the circuit schematic of the NFC chip. Figure 2.7 shows the prototyped ECG processor system on flexible epidermal substrate.

Reduced Complexity Digital-Back-End Processing for Real-time PTA:

In this section, the reduced complexity DBE processing of the PTA is designed and implemented on the NFC chip. The PTA algorithm is characterized in order to identify the conditions when implemented on a fixed-point hardware platform.

This characterization is initialized by evaluating the PTA performance based on the noise removal filter output QRS-complex SNR. The synthetic ECG biopotential signals were used for this characterization. The synthetic ECG biopotential signal is quantized to 14-bit, in order to replicate the maximum resource utilization of the NFC chip. Each test vector includes 1000 heartbeats of a healthy adult with sample rate of 200 S/s. In total, 5 test vectors have been generated to cover the failure, marginal and satisfactory

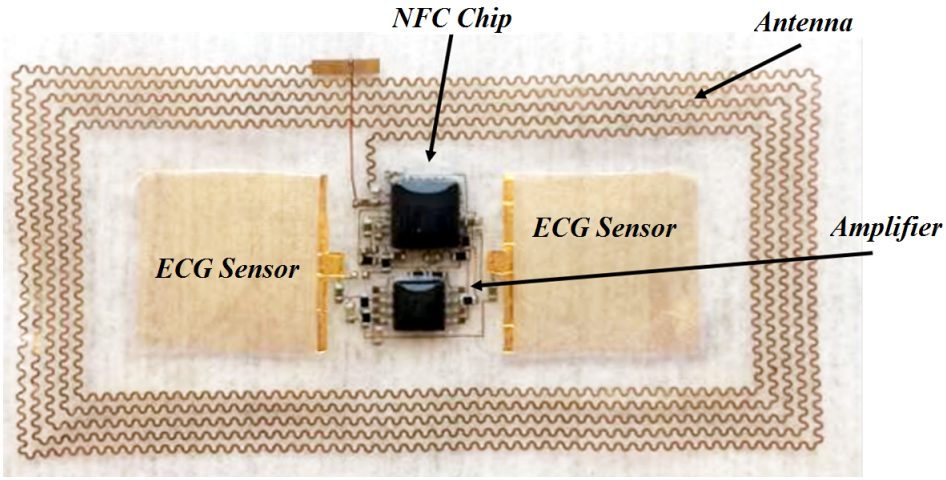

Figure 2.7: Prototyped ECG processor system on flexible epidermal substrate.

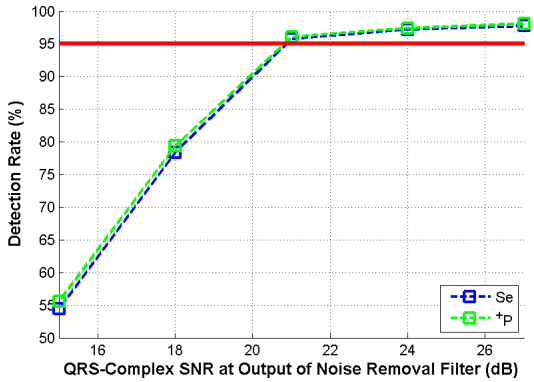

Figure 2.8: PTA detection rate versus the QRS-complex SNR at the output of noise removal filter.

conditions of the required clinical detection rates.

As shown in Fig. 2.8, the minimum QRS-complex SNR of approximately 19.8 dB is required to achieve clinical requirements of Se and ^{+}P at 95% or above. This result provides an estimate for the design of the modified reduced complexity PTA for real-time operation. Next, the PTA stages are replaced in sequence by their reduced complexity equivalents and tested for clinical requirements to achieve the DBE processor signal-chain configuration shown in Fig. 2.9. This signal-chain satisfies the computational costs derived in the previous section, in order to guarantee real-time operation of the NFC chip.

The accuracy of R-peak detection from ECG biopotential signal is a strong function of QRS-complex SNR at the output noise removal filter. Thus,

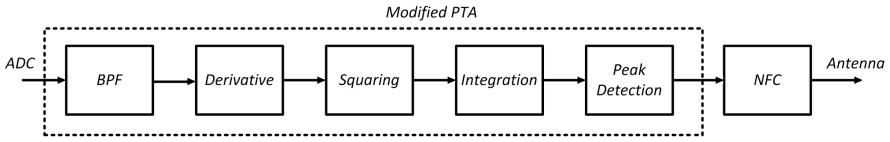

Figure 2.9: Modified PTA signal chain for NFC chip implementation.

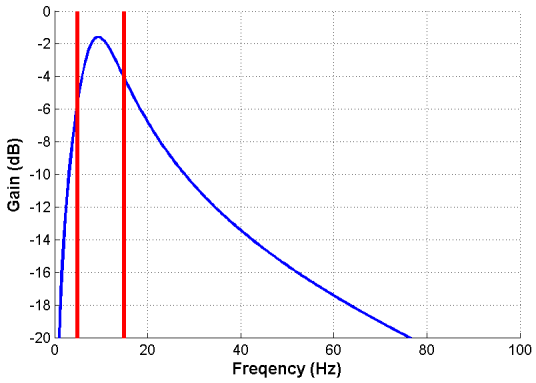

Figure 2.10: Frequency response of the designed noise removal BPF.

appropriate resources should be allocated in the design of this filter. The LPF and HPF stages of the PTA are replaced with a reduced complexity BPF, implemented using an IIR filter. The designed BPF has an attenuation gain of -5 dB at the stop-band frequencies of 5 Hz and 15 Hz and an approximate unity gain of -2 dB at its 10 Hz center frequency. The frequency response and transfer function of this filter are shown in Fig. 2.10 and the equation below:

$$H_{BPF}(z) = \frac{0.0625 - 0.0625z^{-2}}{1 - 1.83z^{-1} + 0.85z^{-2}}$$

The BPF computational cost function consists of a non-recursive (FIR) stage with buffer-length 3 of configuration #3 and recursive (IIR) stage with buffer length 3 of configuration #1 as shown by the transfer function. This results in a normalized cost function of 0.324, based on Tables 2.2 and 2.3.

The generated synthetic test-vector with minimum 19.8 dB QRS-complex SNR is quantized from 4-bit to 14-bit resolution to verify the required clinical performance of PTA at different fixed-point implementations. Figure 2.11 shows the worst-case scenario of this comparison. As shown, the input quantization resolution of 7-bit satisfies the clinical requirements. Therefore, the fixed-point noise removal filter is implemented based on a 7-bit input quan-

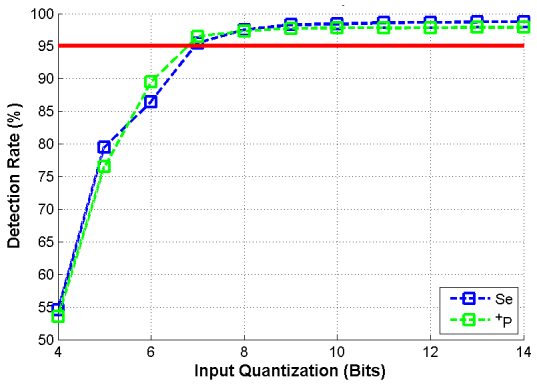

Figure 2.11: Fixed-point quantization of input ECG biopotential signal versus PTA clinical performance.

tization that achieves QRS-complex SNR of 21.7 dB. The designed filter was also tested with the recorded ECG biopotential signals by flexible epidermal ECG sensors, which resulted in $Se = 97.3\%$ and ${}^{+}P = 97.6\%$ satisfactory detection rates.

The next two stages in the PTA are the derivative $H_D(z)$ and squaring blocks. The derivative stage of the PTA is implemented using a 2^{nd} order central-difference differentiator. The modified PTA noise removal filter has a more relaxed highpass behavior. The highpass behavior of the 2^{nd} order central-difference differentiator amplifies the unwanted out-of-band frequencies. Thus, a 1^{st} order central-difference differentiator is employed with transfer function shown in the equation below:

$$H(z) = \frac{1 - z^{-2}}{2}$$

Output of the derivative stage should be scaled down by a factor of 16 with bit-shifting prior to being squared. However, using a 16-Bit fixed-point *int* data type reduces the detection rate severely to $Se = 83.6\%$ and ${}^{+}P = 85.4\%$. Therefore, a 32-bit floating-point *double* data type was used followed by a down scaling factor of 16. The selection of scaling factor of 16 is discussed in the optimization of the integrating LPF block. The normalized cost function of these two stages is equivalent to a non-recursive (FIR) stage with buffer-length 4 of configuration #3 and recursive (IIR) stage with buffer length 1 of configuration #1. This is a total computational cost function of 0.159 for the derivative and squaring stages. This adds up to 0.483 overall cost function including the noise removal stage. The modified PTA has detection rate

of $Se = 96.1\%$ and ${}^{+}P = 96.7\%$ at the output of squaring stage using the synthetic data. In the next step, the moving average LPF block, with effective buffer-length of 33, is replaced with two backward-recursive integrators. This modification increases the false-positive rate by identifying the amplified Q and S components of QRS-complex as false R-peaks. This trade-off can be partially recovered by modification of the real-time thresholding computing. The transfer function of each stage of the integrating LPF is shown in the equation below:

$$H_{INTEG}(z) = \frac{\alpha}{1 + \beta z^{-1}}$$

where α is the pre-scaling factor and β is the memory depth of integrator. The integrator memory depth coefficient β is selected to reduce the number of false peaks, while keeping the integrator bounded with the pre-scaling factor α. Selecting a large pre-scaling factor also helps to lower false-positive probability, and a minimum bound has to considered to prevent false-negative probability of R-peaks with severe distortion. Table 2.5 shows the optimization process for α and β selection to achieve the required clinical performance.

Table 2.5: The α and β selection for optimum Se and ${}^{+}P$ detection rate performance.

Coefficients	$\alpha = \frac{1}{4}$	$\alpha = \frac{1}{8}$	$\alpha = \frac{1}{16}$	$\alpha = \frac{1}{32}$	$\alpha = \frac{1}{64}$
$\beta = 0.83$	N	N	N	N	N
$\beta = 0.86$	N	N	N	N	N
$\beta = 0.89$	N	Y	Y	N	N
$\beta = 0.92$	N	N	Y	Y	N
$\beta = 0.95$	N	N	N	N	N

Table 2.5 shows that $\alpha = \frac{1}{16}$ used in the down scaling of the squaring block, and integration memory depth of $\beta = 0.92$ provide approximately a unity gain, while satisfying the required detection rates. The normalized cost function of the two integrators is equivalent to non-recursive (FIR) stage with buffer-length 2 of configuration #3 and recursive (IIR) stage with buffer length 2 of configuration #1. This is a total computational cost function of 0.216 for the integrators. This adds up to 0.699 overall cost function including the noise removal, derivative and squaring stages. The modified PTA has detection rate of $Se = 95.8\%$ and ${}^{+}P = 96.1\%$ at the output of the integration LPF block. In the next step, the PTA peak detection stage

is replaced and optimized by the reduced complexity peak detection criteria shown in the equations below:

$$SPK[n] = \gamma PEAK[n-1] + (1-\gamma)SPK[n-1]$$
$$THRESHOLD[n] = \phi SPK[n]$$

The modified implementation of the real-time peak detection block does not track the noise peaks and searchback. This is because a significant performance improvement can be justified, while more than three times the allocation of computational resources is required. However, the threshold computing coefficients need to be recalculated to satisfy the clinical requirements. Table 2.6 shows the optimization process of γ and ϕ selection.

Table 2.6: Results of evaluating the real-time R-peak detection algorithm using the MIT/BIH database

Coefficients	$\phi = 0.05$	$\phi = 0.15$	$\phi = 0.25$	$\phi = 0.35$	$\phi = 0.45$
$\gamma = 0.05$	N	N	N	N	N
$\gamma = 0.10$	N	N	N	N	N
$\gamma = 0.15$	N	N	Y	N	N
$\gamma = 0.20$	N	Y	Y	N	N
$\gamma = 0.25$	N	N	N	N	N

Table 2.6 shows that $\gamma = 0.15$ and $\phi = 0.25$ provide a marginally better detection rate of $Se = 95.4\%$ and ${}^{+}P = 95.8\%$. Note that the original PTA coefficients do not satisfy the clinical requirements of the modified PTA implementation. The peak detection algorithm is designed to register local extrema of the integrator LPF output as the $PEAK[n]$ value in the recursive $SPK[n]$ calculation if it is more than the threshold. The local extrema detection is triggered using a triple-point maximum tracking algorithm that uses a first-in-first-out (FIFO) buffer of length 3 directly fed from the integrator LPF output. The normalized cost function of the peak detection is equivalent to non-recursive (FIR) stage with buffer-length 1 of configuration #2, non-recursive (FIR) stage with buffer-length 4 of configuration #3, recursive (IIR) stage with buffer length 2 of configuration #1, conditional statement buffer-length 3 and NFC transmission of the detected peak. This leads to total computational cost function of 0.296 for the peak detection block. This adds up to overall cost of 0.997 including the ADC read that has been tested

for real-time operation on the flexible epidermal patch shown in the Fig. 2.7 at sample rate of 250 S/s.

2.2.4 ECG Processor Performance Benchmarking

With the implementation of the in-sensor information processor, the transmitted data traffic from the NFC chip was reduced by an average factor of approximately $120X$ to $150X$ given the average adult normal heart rate between 60 and 100 heartbeats per second. This is equivalent to $2.74X$ to $3.56X$ improvement in energy-consumption indicated by the datasheet of the NFC chip. Direct measurement of the NFC chip power was not possible because of its packaging design. The overall maximum detection rate of $Se = 95.4\%$ and ${}^{+}P = 95.8\%$ was achieved that satisfies the clinical requirements using the synthetic and recorded database while an off-line implementation of PTA resulted in $Se = 98.1\%$ and ${}^{+}P = 98.7\%$ detection rates. In the next step, the algorithm is tested using the MIT/BIH database. Table B.1 shows the PTA performance as a benchmarking tool for the comparison of the designed modified PTA in real-time operation. The modified PTA has an overall detection rate of 93.4% that is lower than the clinical requirements. This is mainly because of certain test-vectors, such as 108 and 222, where the R-peak amplitudes are significantly small compared with the Q and S peaks. This condition results in significant increase in the false-positive rate.

2.3 PPG Processor

This section focuses on the design and implementation of a PPG processor for real-time operation on a flexible epidermal substrate.

2.3.1 Application Requirements

The PPG processor is designed using the same guidelines employed in the design of the modified PTA of the ECG processor, in order to extract and utilize the maximum amount of information from the sensors for real-time operation. The lack of reliable benchmarking data sets in the literature for the optical systolic blood-pressure measurement method makes the accuracy

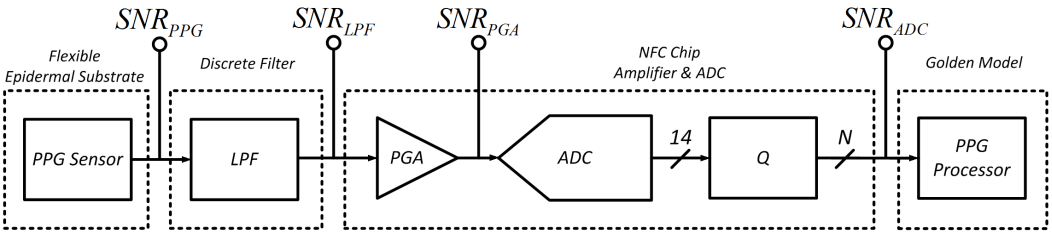

Figure 2.12: AFE of the PPG biopotential processor.

requirement hard to obtain. Therefore, data is collected with the flexible epidermal PPG sensors carefully placed on the forearm. The hardware setup requires simultaneous NFC chip reading of its two ADC channels for red light and IR radiation reflections through photodiode sensors.

Analog-Front-End:

The PPG biopotential signal bandwidth should be limited to 0 Hz to 4 Hz [16], where most of the frequency spectral content exists. The relatively large envelope of PPG biopotential signals compared with the ECG biopotential signals eliminates the need for a first-stage amplifier. Thus, the only components in the design of the PPG processor AFE are the anti-aliasing and PPG biopotential signal band-limiting LPF followed by the PGA and ADC of NFC chip, as shown in Fig. 2.12.

The significantly large SNR of the PPG biopotential signals, on the order of 28 dB to 35 dB as measured in the bandwidth of 0 Hz to 4 Hz over the biopotential signal spectrum of 0 Hz to 100 Hz, relaxes the requirements on AFE design. Thus, the NF calculation of AFE is skipped and the PGA gain followed by SQNR value of ADC are selected to achieve the best results given the recorded PPG biopotential signals using the flexible epidermal PPG sensors. Figure 2.13 shows the PPG biopotential signal SNR of the two photodiode sensors sampled at 1 kS/s and 14-bit quantization using the embedded ADC of NFC chip. The main consideration in the design of the AFE is to increase the photodiode sensors' gain as high as possible while maintaining the linearity and low phase distortion. Figure 2.14 shows the circuit schematic of the flexible epidermal PPG sensors connection in the AFE signal-chain.

The bias-network of LPF filters is designed so as to prevent signal satura-

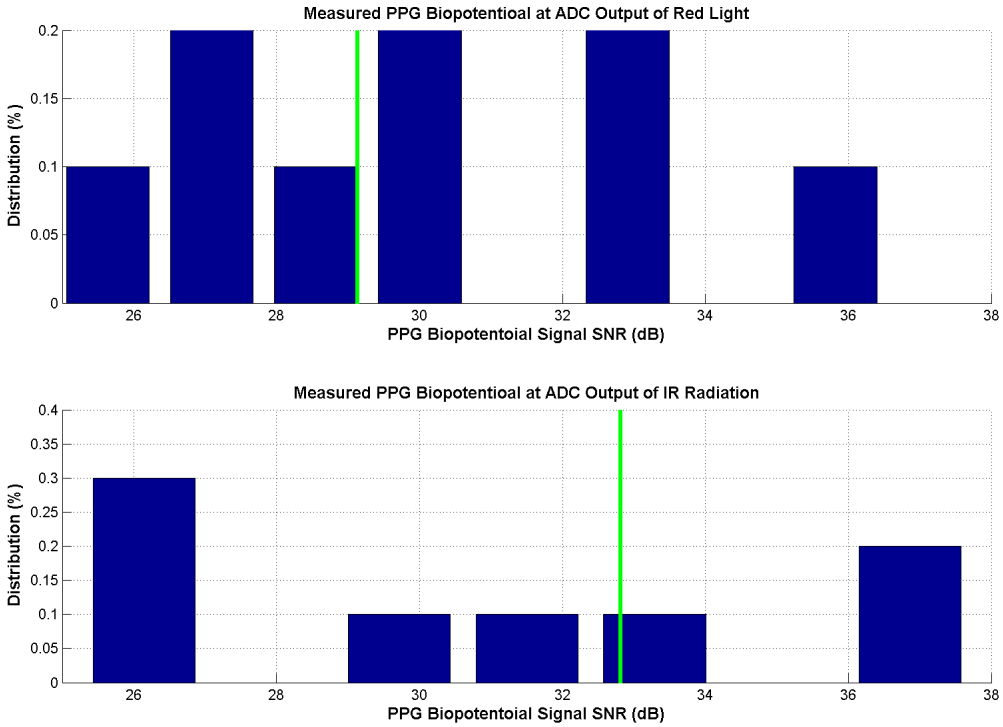

Figure 2.13: PPG biopotential signal SNR of the two photodiode sensors.

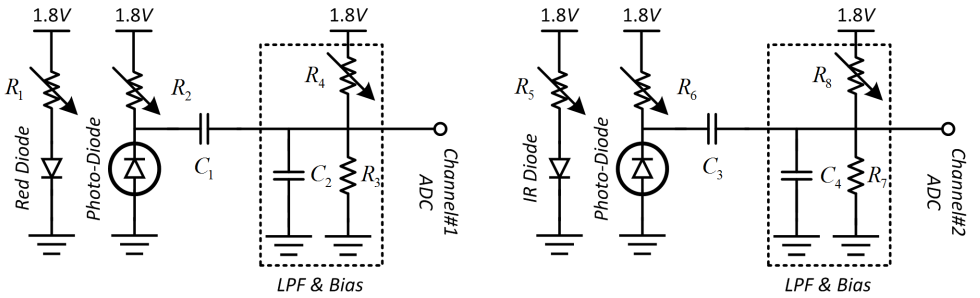

Figure 2.14: Circuit schematic of the flexible epidermal PPG sensor.

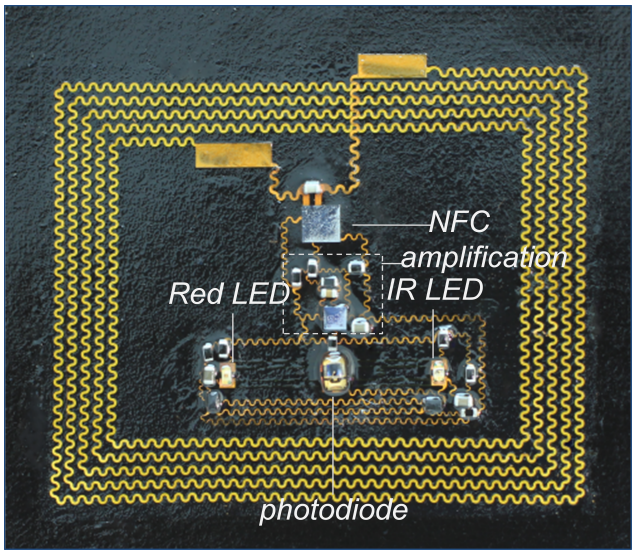

Figure 2.15: Underdevelopment sample of flexible epidermal PPG sensor.

tion if the maximum gain of PGA is used and to satisfy the -3 dB bandwidth. The values of resistors and capacitor in the design of AFE are not reported because of flexible epidermal PPG sensor immaturity and large sample-to-sample variations. Figure 2.15 shows a sample of the flexible epidermal PPG sensor.

Digital-Back-End PPG Processing:

The PPG biopotential signals $x_1(t)$ and $x_2(t)$ collected through $Channel\#1$ and $Channel\#2$, respectively, are reformulated using a memoryless communication channel with an attenuation factor α shown by the equations below:

$$x_1(t) = s_1(t) + n_1(t)$$
$$x_2(t) = \alpha s_1(t + T_{delay}) + n_2(t)$$

where $s_1(t)$, $n_1(t)$ and $n_2(t)$ have been assumed to be real and jointly stationary random processes and $s_1(t)$ is uncorrelated with noise signals $n_1(t)$ and $n_2(t)$. These imply that the cross-correlation can be used to determine

the variable T_{delay} as shown in the equations below:

$$R_{x_1x_2}(\tau) = E[x_1(t)x_2(t-\tau)]$$
$$T_{delay} = arg\underset{\tau}{max}\, R_{x_1x_2}(\tau)$$

where for a finite observation the short-time cross-correlation can be calculated as follows:

$$\hat{R}_{x_1x_2}(\tau) = \int_{-\infty}^{\infty} \hat{G}_{x_1x_2}(f)e^{j2\pi f\tau}df$$
$$\hat{G}_{x_1x_2}(f) = \alpha\hat{G}_{s_1s_1}(f)e^{-j2\pi fT_{Delay}} + \hat{G}_{n_1n_2}(f)$$
$$T_{delay} = arg\underset{\tau}{max}\, \hat{R}_{x_1x_2}(\tau)$$

where it is assumed that $\hat{G}_{n_1n_2}(f) = 0$. To increase the accuracy of estimated T_{delay} from the short-time cross-correlation $\hat{R}_{x_1x_2}(\tau)$, the signals $x_1(t)$ and $x_2(t)$ should be filtered to increase the SNR. The cross-correlation of filtered signals $y_1(f)$ and $y_2(f)$ using $H_1(f)$ and $H_2(f)$, respectively, is shown by equation below:

$$\hat{R}_{y_1y_2}(\tau) = \int_{-\infty}^{\infty} H_1(f)H_2^*(f)\hat{G}_{x_1x_2}(f)e^{j2\pi f\tau}df$$

The smoothed coherence transform [22] states that a match-filtering operation of $x_1(t)$ and $x_2(t)$ is required using the $H_1(f)$ and $H_2(f)$ filters satisfying the following constraints:

$$H_1(f)H_2^*(f) = \sqrt{\frac{1}{G_{x_1x_1}(f)G_{x_2x_2}(f)}}$$
$$H_1(f) = \sqrt{\frac{1}{G_{x_1x_1}(f)}}$$
$$H_2(f) = \sqrt{\frac{1}{G_{x_2x_2}(f)}}$$

In the first step, the frequency spectrum content of recorded PPG biopotential signals is investigated and matched filters $H_1(f)$ and $H_2(f)$ are designed based on the Tables 2.2 and 2.3. The following equation shows the transfer

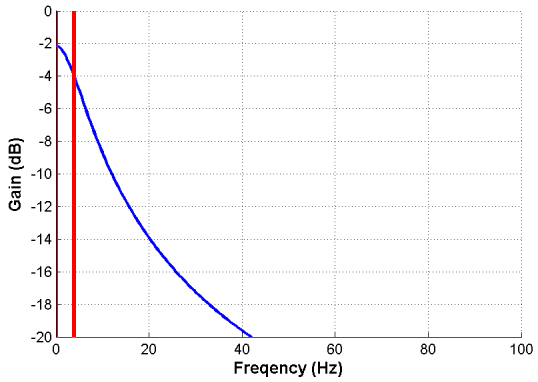

Figure 2.16: Frequency response of the $H_1(z)$ and $H_2(z)$ filters.

function of these filtering operations for sampling rate of 250 S/s:

$$H_1(z) = H_2(z) = \frac{0.0625}{1 + 0.92z^{-1}}$$

The frequency response of these filters is shown in the Fig. 2.16. The filters have attenuation gain of -5 dB at 4 Hz bandwidth, -20 dB bandwidth of 42 Hz and passband of gain of -2 dB. The normalized cost function of the two integrators is equivalent to non-recursive (FIR) stage with buffer-length 2 of configuration #3 and recursive (IIR) stage with buffer length 2 of configuration #1. This is a total computational cost function of 0.216 for the filters. Figure 2.17 shows the raw and filtered PPG biopotential signal frequency spectrum using the $H_1(z)$ and $H_2(z)$ filters. The filtering operation has increased the PPG biopotential signal SNR of the two photodiode sensors by 5.8 dB and 6.1 dB for red light and IR radiation, respectively.

In the next step, the operating principle of the proposed cross-correlation based TDE is explained. Given the filtered PPG biopotential signals $y_1[n]$ and $y_2[n]$ at the output of the matched filters, three delayed copies of $y_1[n]$ are generated as follows (see Fig. 2.18):

$$\begin{aligned} y_{1,a}[n] &= y_1[n - d_{peak}[n-1] + \Delta[n-1] \\ y_{1,b}[n] &= y_1[n - d_{peak}[n-1] - \Delta[n-1] \\ y_{1,c}[n] &= y_1[n - d_{peak}[n-1]] \end{aligned}$$

where d_{peak} is the estimated delay between discrete-time signals $y_1[n]$ and $y_2[n]$. The estimated delay has an absolute finite estimation error of $error_{d_{peak}}$,

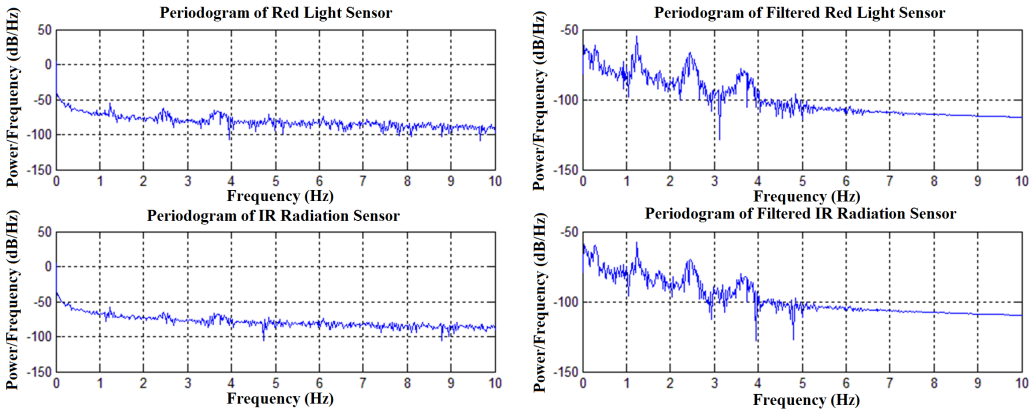

Figure 2.17: Raw and filtered PPG biopotential signals using $H_1(z)$ and $H_2(z)$ filters.

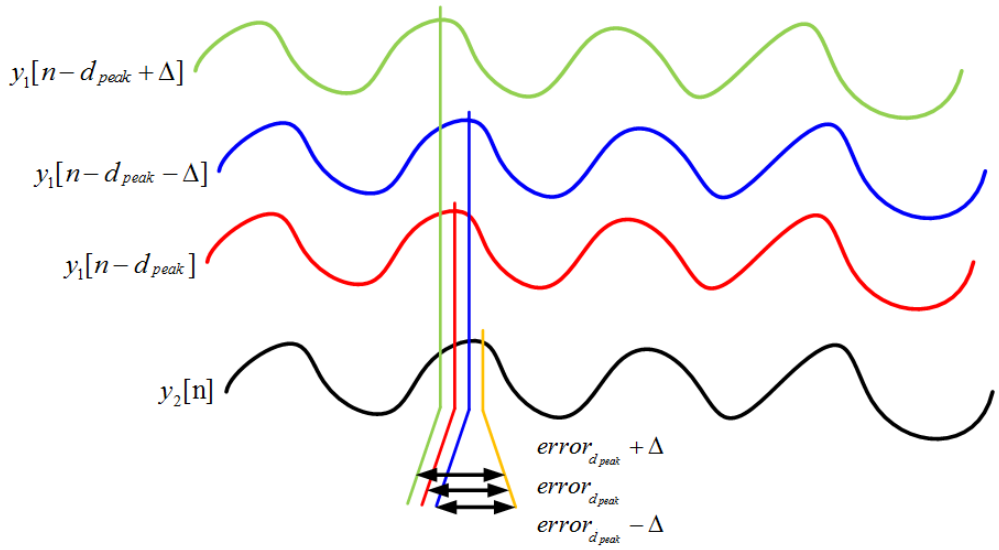

Figure 2.18: Generation of delayed versions of $y_1[n]$ versus $y_2[n]$.

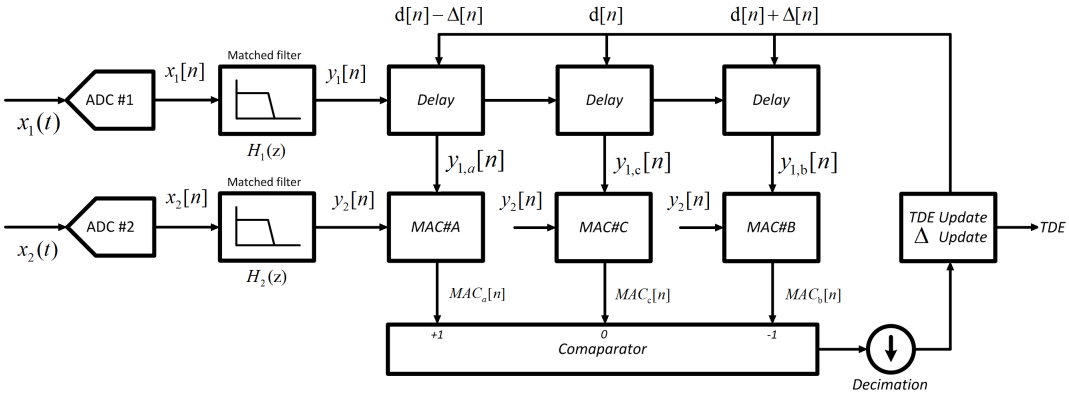

Figure 2.19: The proposed real-time TDE algorithm for systolic blood-pressure measurement.

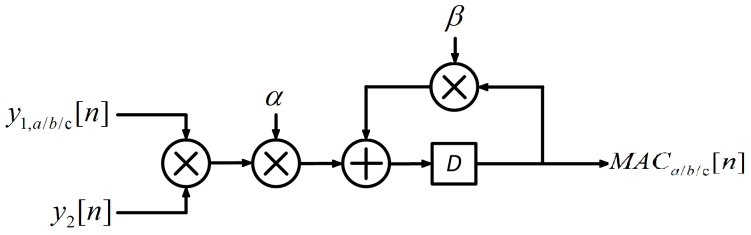

Figure 2.20: MAC unit of the TDE algorithm.

which is a function of SNR and sampling rate, as shown in Fig. 2.18. The parameter Δ is the dynamic search step of the algorithm with minimum value of 1 sample and maximum value of 8 samples. This corresponds to an average minimum $error_{d_{peak}}$ of 2 ms for the sample rate of 250 S/s. Figure 2.19 shows the proposed real-time TDE algorithm.

The proposed architecture uses three multiply and accumulate (MAC) units, which integrates the products of $y_2[n]$ with three delayed copies of $y_1[n]$ in real-time. The MAC unit backward-recursive integrators have a memory depth and scaling factor of $\beta = 0.96$ and $\alpha = \frac{1}{32}$, respectively, as shown in Fig. 2.20 and defined by the transfer function below:

$$H_{INTEG}(z) = \frac{\alpha}{1 + \beta z^{-1}}$$

The normalized cost function of the three integrators is equivalent to non-recursive (FIR) stage with buffer-length 3 of configuration #3, non-recursive (FIR) stage with buffer-length 3 of configuration #2 and recursive (IIR) stage with buffer length 3 of configuration #1. This is a total computational

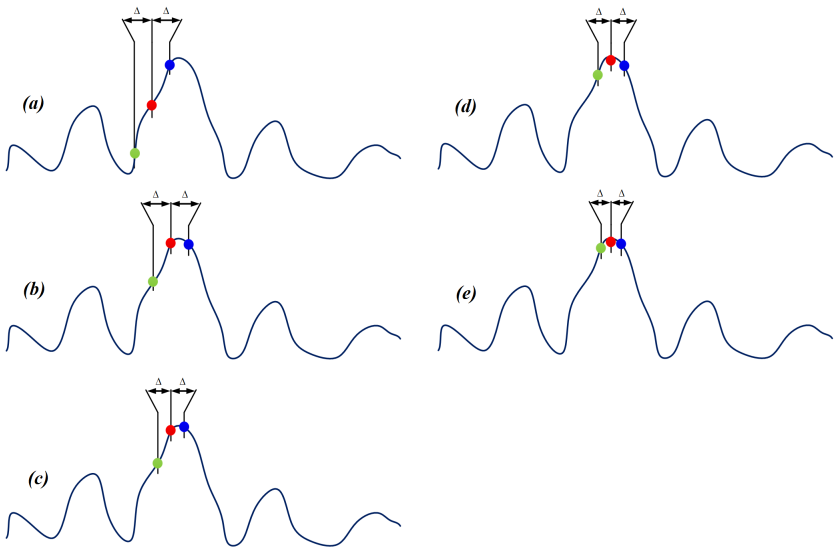

Figure 2.21: Example locking sequence of the proposed real-time TDE algorithm.

cost function of 0.435 for MAC units and 0.651 including the filters for real-time operation. The comparator block outputs $\kappa = \{+1, 0, -1\}$ depending on the maximum value detected between MAC_a, MAC_c or MAC_b values, respectively. The comparator output is down-sampled by a factor of M and a new $d_{peak}[n]$ is calculated using the recursive equation as shown below:

$$d_{peak}[n] = d_{peak}[n-1] + \kappa\Delta[n]$$

The down-sampling factor M sets the $d_{peak}[n]$ update rate at $\frac{250}{M}$ S/s. Once the MAC_c is detected as the maximum with $\kappa = 0$, the $\Delta[n-1]$ dynamic search step is reduced by factor ω to decrease $error_{d_{peak}}$ and refine the estimated $d_{peak}[n]$. The step decrease in $\Delta[n-1]$ might alter the condition of MAC_c being the maximum value. Therefore, a $\Delta[n]$ searchback and refine is required to satisfy the $MAC_c > \{MAC_a, MAC_b\}$ condition. This process is described by the equation below:

$$\Delta[n] = \begin{cases} \frac{\Delta[n-1]}{\omega} & \kappa = 0 \\ \lambda & else \end{cases}$$

where λ is a variable to be optimized for the best transient response and ω to reduce the settling time. Figure 2.21 shows a sample sequence of the

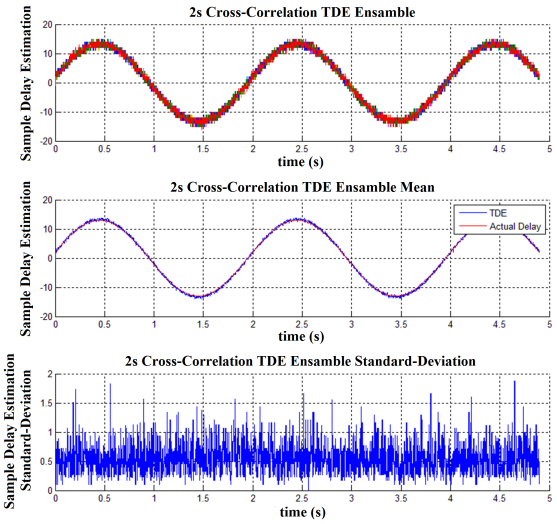

Figure 2.22: The ensemble performance of real-time TDE algorithm using slow varying sinusoidal delay.

TDE algorithm locking mechanism. The comparator and update blocks have the equivalent normalized cost function of non-recursive (FIR) stage with buffer-length 3 of configuration #3 and non-recursive (FIR) stage with buffer-length 5. This is a total computational cost of 0.085 for MAC units and 0.736 including the filters and MAC units for real-time operation. The ADC readings and NFC transmissions require additional normalized cost function of 0.007 which leaves the total normalized cost function of 0.257 for data buffering of $y_{1,a/b/c}[n]$ streams in real-time operation. A simple calculation based on Tables 2.2 and 2.3 sets the maximum effective buffer-length of 16 per $y_{1,a/b/c}[n]$ copies. This is equivalent to 64 ms when a sample rate of 250 S/s is used. Thus, the PPG optical sensor spacing $L1$ and blood velocity should be considered to prevent any sensed PPG biopotential signal delay of 64 ms or more. The recorded PPG biopotential signals, collected using the manufactured flexible epidermal PPG sensor, do not indicate any delay values of 31 ms or greater. Thus the allocated memory space satisfied the test-setup of the PPG processor.

In the next step, the synthetic PPG biopotential data with delay functions of 0.5 Hz sinusoidal and unit step are employed to test the dynamic response and functionality of the real-time algorithm. An arbitrary 12-bit function generator is used to generate the synthetic signals. Figure 2.22 and 2.23 show the results of the two tests.

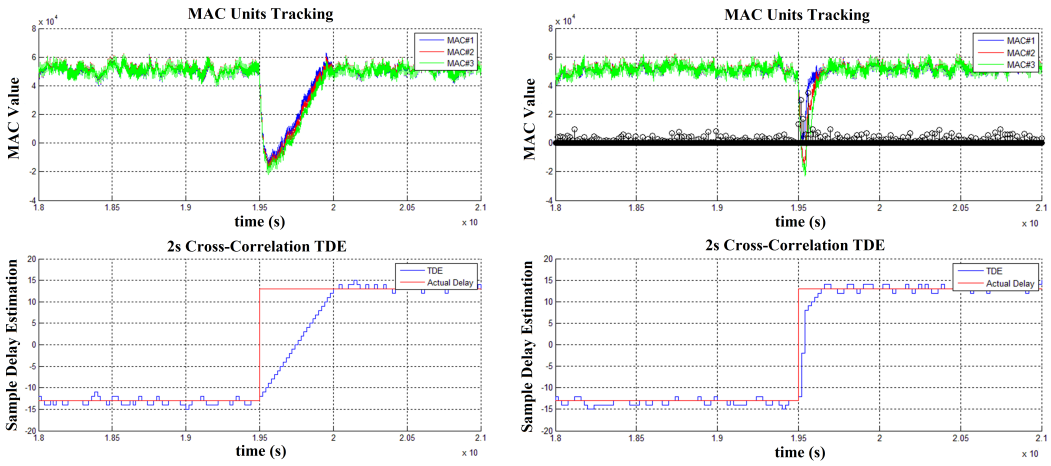

Figure 2.23: The step performance of real-time TDE algorithm.

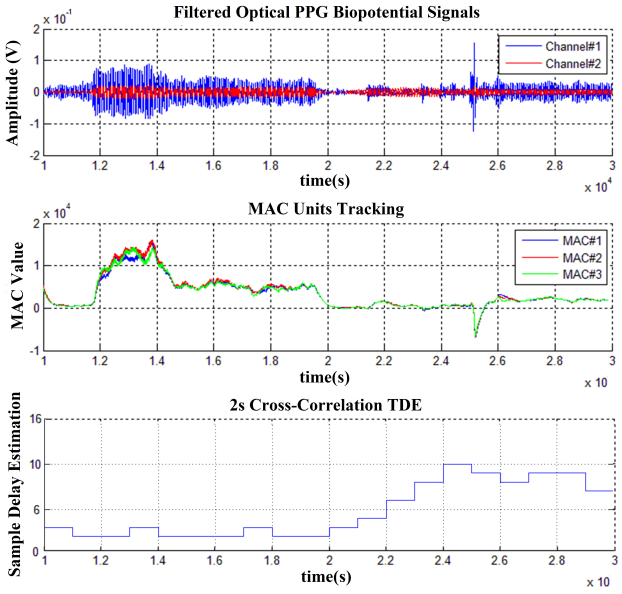

Figure 2.24: The real-time systolic blood-pressure measurement using PPG biopotential signals on a flexible epidermal substrate.

As shown in Fig. 2.22, the TDE is tested across multiple synthetic PPG data test-vectors and a statistical ensemble tracking of TDE is shown. The standard deviation of TDE tracking error barely passes 1 sample, which confirms the designed resolution of 4 ms $error_{d_{peak}}$. As shown in Fig. 2.23 the proposed algorithm is tested under two λ and ω values. The left plot is for $\lambda = 1$ and $\omega = 1$ when the right plot is for optimized $\lambda = 3$ and $\omega = 2$. In the next step, for validating the real-time performance of the TDE algorithm, the NFC chip was used to collect a real-time PPG biopotential signal for tracking the changes in the systolic blood-pressure on an adult human. The participating adult was asked to increase the respiration rate at time 18 s, thus increasing the heart rate and the systolic blood-pressure. Give that the human body is a spline system, it took 6 s to observe a slow step change in the systolic blood-pressure, as shown in Fig. 2.24. The system is robust to motion artifacts [23] as shown in Fig. 2.24.

2.3.2 PPG Processor Performance Benchmarking

As mentioned earlier there is no previous work on systolic blood-pressure using flexible epidermal PPG optical sensors. Thus, a comparison of PPG processor performance cannot be made. However, it has been shown that the system can estimate the PPG biopotential delay with a resolution of 4 ms, which is enough to detect the changes in the systolic blood-pressure of an adult human when the respiration rate is changed. More clinical studies are required for further system optimization and performance improvement.

CHAPTER 3

DESIGN AND ASIC IMPLEMENTATION OF IN-SENSOR OPTICAL SYSTOLIC BLOOD-PRESSURE SYSTEM

3.1 Introduction

This chapter focuses on the design of an ASIC for the proposed optical systolic blood-pressure system. The ASIC is designed as a stand-alone system with a few external components. The system includes a multi-channel amplifier and an ADC for AFE processing, a digital PPG processor and a passive NFC transmitter. The energy harvesting using the external loop-antenna has been left out for future development. The ASIC is designed in a TSMC 65nm-GP CMOS process.

3.2 System Architecture

Figure 3.1 shows the top-level architecture of the ASIC. The major blocks include two single-stage amplifiers, a time-interleaved ADC, digital PPG processor and the NFC passive transmitter. The system AFE blocks are designed to be compatible for future development of an on-chip NFC receiver with a carrier frequency of 13.56 MHz. Thus, the NFC standards are considered in the design and implementation of the AFE. The power supply is provided externally by two voltage rails of 1.8 V and 1.0 V for analog and digital circuitry, respectively. The digital and analog grounds are separated for better noise isolation. The amplifier feedback gain network, input DC-offset bias network and the input LPF are implemented using external discrete components because of the immature flexible epidermal substrate and the need for more control over its parameters as discussed in Chapter 2. Similarly the loop-antenna and its matching network for passive NFC transmission are implemented using external discrete components. In the following sections,

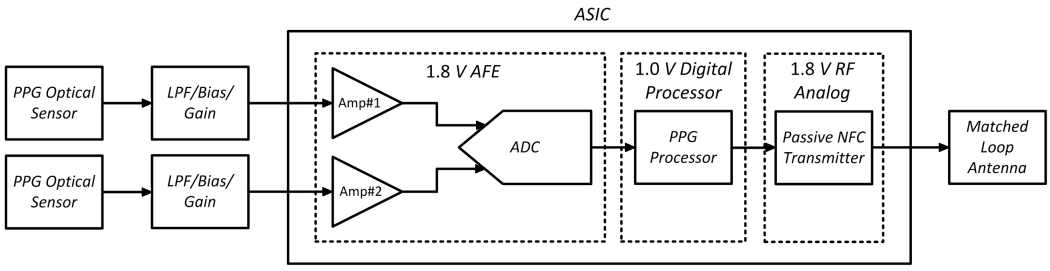

Figure 3.1: Hierarchical architecture of the designed ASIC and external components.

each of the system blocks is designed and simulated to evaluate performance metrics required for the optical systolic blood-pressure system designed in Chapter 2.

3.2.1 Amplifier

The amplifier designed in this work is implemented with the objective of being used in a NFC receiver [24]. Thus, a high closed-loop bandwidth of 150 MHz is required with total harmonic distortion (THD) and DC-loop gain of -70 dB and 72 dB, respectively, for a reliable communication. Given the relatively high SNR of PPG biopotential and NFC RF signals in a range of 20 dB to 40 dB, the NF constraints are relaxed in the design of the amplifier. The power consumption should be minimized with a PSRR of -60 dB or below. These specifications are compatible with the AFE block design requirements of the implemented optical systolic blood-pressure system in Chapter 2. The amplifier design is the most challenging and sensitive block in the design of the ASIC. The amplifier design is initiated with implementation of a unity gain buffer.

The design of the unity gain buffer is a trade-off between gain, bandwidth and output swing. The target is to meet all of the given specifications, then strive for minimum power consumption. There are two major topologies for differential amplifier design: telescopic and folded cascode. Telescopic topology offers higher gain with less power, but the output swing could be very limited due to the large number of cascoded transistors. One possible solution to resolve this problem is cascading of a second-stage for larger output swing. However, a multi-stage amplifier usually has limited bandwidth and phase margin performance, and adding frequency compensation capaci-

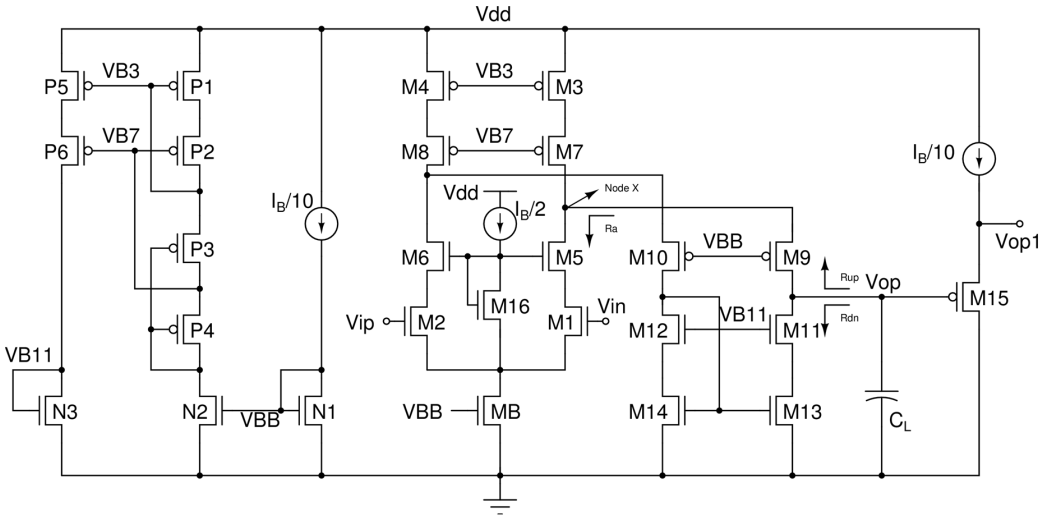

Figure 3.2: Transistor level implementation of the designed amplifier, using a modified folded cascode architecture.

tors could be bothersome and more stability issues should be considered. In comparison, a single-stage folded cascode amplifier can provide better swing with the trade-off of less DC gain and more power consumption. However, considering the output swing being the most challenging requirement, then a basic folded cascode topology [25] is designed, as shown in Fig. 3.2, with the two following adjustments.

1. Increasing R_{up} of R_{out} by cascoding $M7$ and $M8$:

The value of R_{out} is first dominated by R_{up}, since there are two branches in parallel looking up from $M9$ and $M10$ and the impedance is low. Moreover, the current flowing through $M3$ and $M4$ is larger, which causes even lower impedance since $r_{ds} = 1\frac{1}{\lambda I_d}$. To increase R_{up}, PMOS $M7$ and $M8$ is cascoded. Then, R_{out} is dominated by R_{dn} or R_a, which are considered afterwards.

2. Increasing the usable g_m (G_m) by cascoding $M5$ and $M6$:

Without $M5$ and $M6$, the DC impedance looking up from $M1$ is calculated using the equation below:

$$g_{m7}r_{ds7}r_{ds3}||\frac{1}{g_{m9}}(1+\frac{g_{m11}r_{ds11}r_{ds12}}{r_{ds9}})$$

which is roughly equal to r_{ds}. However, there is a current divider between this impedance and r_{ds1}, so only half of the current generated by $M1$ will flow to the output or G_m is halved in this case. To address this problem, $M5$ and $M6$ are cascoded to decrease the impedance looking up from $M1$ to $\frac{2}{g_m}$ and let most of the current flow to the output. Another benefit is that now we can have a minimum length device to reduce the capacitance at node x for better phase margin. $M5$ and $M6$ also help to increase R_{up}, so that R_{out} is much less dominated by R_a.

Amplifier Design

1. Determining Overdrive Voltage V_{ov}:

The lower the overdrive V_{ov}, the higher the input common range and output swing. However, the lower the V_{ov}, the larger the dimension of W/L required. This means there will be higher parasitic capacitance, which causes lower second pole frequency and deteriorates the phase margin. Because of that, $V_{ov} = 150$ mV is chosen.

2. Determining Transconductance g_{m1} and bias current I_B:

Considering the relation $g_{m1} = 2\pi f_0 C_L$, then g_{m1} is determined by the required bandwidth, f_0, and load capacitance, C_L. For the worst-case, to drive the largest possible load, $C_L = 2.5$ pF is set as the starting point of the design. Notice that f_0 is set to be close to 150 MHz rather than overdesigning it. Otherwise, the phase margin requirement cannot be met due to the second pole at the source of $M9$ and $M10$. After g_{m1} is determined, I_B can be derived using $g_{m1} = \frac{2I_B}{V_{ov}}$ and the pre-determined V_{ov} value.

3. Determine Transistor Dimensions W/L:

Based on the required DC loop gain, $A_{dc} = g_{m1}R_{out}$ and $R_{out} = R_{up}||R_{dn}$, the intrinsic gain of each transistor can be determined. Larger length will be chosen to achieve larger gain.

4. Increasing R_{dn} of R_{out} by adjusting the folded branch current:

In simulations, R_{dn} or r_{ds13} is found much smaller than from calculations. The main reason is that r_{ds} drops a lot with V_{ds}. The r_{ds13} is small because V_{ds13} is small due to the cascoded topology. From $g_m r_{ds} = \frac{2I_d}{V_{ov}\frac{1}{\lambda I_d}} = \frac{2}{\lambda V_{ov}}$, the intrinsic gain of $g_{m11}r_{ds11}$ is independent of its bias current. To increase r_{ds13} (therefore R_{dn}), we can decrease its current. However, the trade-off is that g_{m9} will decrease as well, which lowers the second pole frequency and thus degrades the phase margin, shown by the equation below:

$$\omega_{p2} \approx \frac{1}{R_{x2}C_{x2}} \approx \frac{g_{m2}}{C_{gd5} + C_{gd7} + C_{gs9}}$$

5. Improving Phase-Margin by using Minimum Length for $M5$, $M7$ and $M9$:

To increase the second pole frequency as high as possible, the lengths for $M5$, $M7$ and $M9$ are chosen to be the minimum to reduce parasitic capacitance. R_{up} will be degraded, and R_{out} will not have too much change since the modified folded cascode is now dominated by R_{dn}.

6. Improve the Matching between V_{icm} and V_{ocm}:

A common-drain amplifier or level shifter is added to increase approximately $V_T + V_{ov}$ from V_{op1} to V_{op}. Its bias current is chosen to be large in avoidance of lower additional pole frequency.

Table 3.1 lists the final transistors sizing and operating region of each transistor in the modified folded cascode design of Fig. 3.2 for input common mode voltage (V_{ICM}) of 1.4 V. As shown in Table 3.1, all transistors are in the correct region of operation, while satisfying the design constraints as described in the amplifier parameters calculation.

Designed Amplifier Performance Evaluation:

Table 3.2 compares the performance of the required amplifier design constraints and the post-layout simulations with inclusion of R, C and CC parasitic components.

Table 3.1: Modified folded cascode amplifier transistor sizing and region of operation

Transistor	WŁ	Current (μA)	g_m (mA/V)	$\lvert V_{ov}\rvert$ (mV)	Region
MB	89.19/0.5	638.6	7.30	158	Saturation
M1/M2	25.66/0.315	213.2	2.79	121	Saturation
M3/M4	69.06/0.225	229.8	2.53	133	Linear
M5/M6	7.72/0.18	213.2	2.10	158	Saturation
M7/M8	26.02/0.18	229.8	2.27	176	Saturation
M11/M12	2.57/0.315	16.57	0.246	101	Saturation
M13/M14	3.90/0.45	16.57	0.238	111	Saturation
M15	50.00/0.18	42.41	0.839	32	Saturation
M16	1.48/0.18	212.1	0.699	424	Saturation
N1	5.95/0.5	42.41	0.486	158	Saturation
N2	6.49/0.5	46.82	0.486	155	Linear
N3	0.27/0.315	4.84	0.024	348	Saturation
P1	13.81/0.225	46.82	0.518	134	Linear
P2	5.2/0.18	46.82	0.461	177	Saturation
P3	1.73/0.18	46.82	0.135	423	Saturation
P4	5.20/0.18	46.82	0.451	175	Linear
P5	1.26/0.225	4.82	0.052	146	Linear
P6	2.73/0.18	4.84	0.043	201	Saturation

Figure 3.3 shows the loop-gain AC response of the designed amplifier, with DC gain of 75.1 dB, bandwidth of 178 MHz, and phase margin of 62.1^o evaluated at $V_{ICM} = 1.4$ V and $C_L = 2$ pF.

Figure 3.4 shows the DC loop-gain versus differential output swing. The amplifier has common mode (CM) gain above 72 dB for an output swing of 384 mV and 66 dB for an output swing of 608 mV. Note that the output swing for the modified folded cascode amplifier has been sacrificed by more transistors cascading to achieve higher gain. The maximum CM ranges at input and output of the amplifier are given by the equations below:

$$2V_{ov} + V_T \leq V_{ICM} \leq V_{dd} - 3V_{ov} + V_T$$
$$2V_{ov} \leq V_{OCM} \leq V_{dd} - 3V_{ov}$$

The step response of the amplifier with capacitive load of $C_L = 2$ pF has been simulated for the range of V_{ICM} with a DC loop gain of 66 dB and above, shown in Fig. 3.4. This consists of the boundary conditions of $V_{icm1} = 1.0$ V and $V_{icm2} = 1.6$ V with the worst settling time of 59.5 ns as shown in Fig.

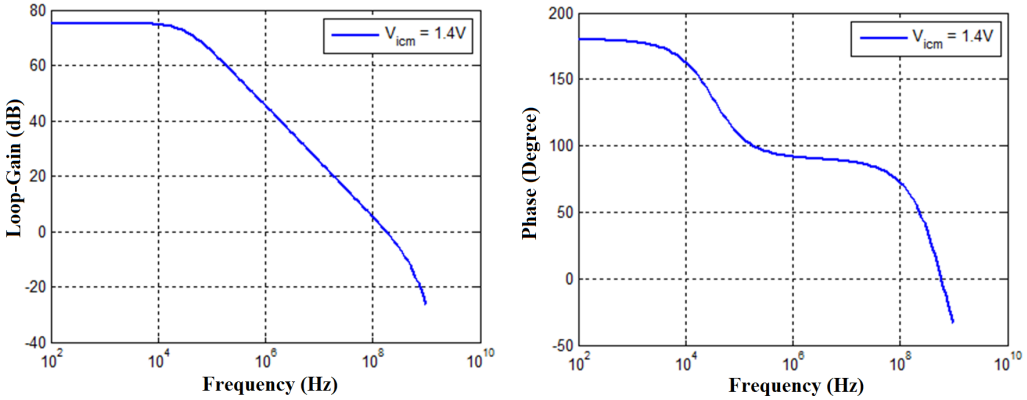

Figure 3.3: Loop-gain AC response and phase margin of modified folded cascode amplifier.

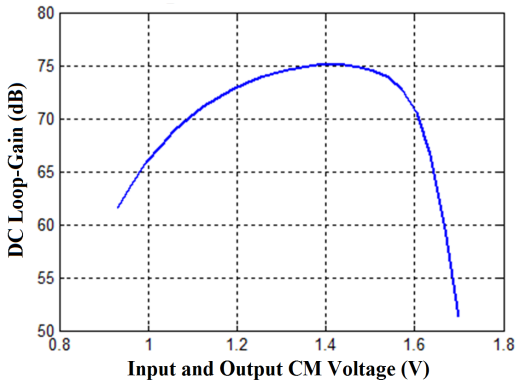

Figure 3.4: DC loop-gain versus differential output swing of the modified folded cascode amplifier.

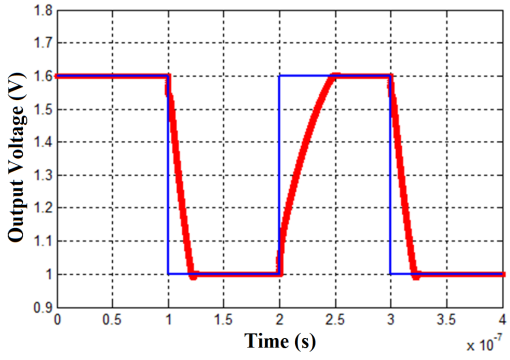

Figure 3.5: The worst case settle time at $V_{icm1} = 1.0$ V and $V_{icm2} = 1.6$ V of the modified folded cascode amplifier.

Table 3.2: Amplifier post-layout performance comparison.

Specifications	Design Requirement	Post-Layout Simulation
Supply Voltage V_{dd}	≤ 1.8 V	1.8 V
Closed-Loop Bandwidth f_0	≥ 150 MHz	≥ 178 MHz
Output Swing	≥ 0.6 V_{pp}	≥ 0.6 V_{pp} (Open-Loop Gain) ≥ 0.384 V_{pp} (Closed-Loop Gain)
DC-Loop Gain	≥ 72 dB	≥ 66 dB (@ 0.6 V_{pp} (Open-Loop Gain) ≥ 72 dB (@ 0.384 V_{pp} (Closed-Loop Gain)
Loop Phase-Margin	$\geq 65^o$	$\geq 57^o$ ($C_L = 2$ pF)
Load Capacitance (C_L)	2 pF	2 pF
THD	≤ -70 dB	-84.3 dB ($f_{in} = 1$ MHz)
Low Frequency PSRR	≤ -60 dB	≤ -120 dB
Power Consumption	Minimum	1.13 mW

3.5. Table 3.3 shows the settling error and DC loop gain for this test.

Table 3.3: Settling error and DC gain of the modified folded cascode amplifier step-response.

V_{ICM} (V)	V_{output} (V)	Settling Error (%)	DC Loop Gain (dB)
1.0	1.000050	5.00E-03	86
1.1	1.100001	5.29E-03	126
1.2	1.199975	2.11E-03	94
1.3	1.299958	3.23E-03	90
1.4	1.399944	4.00E-03	88
1.5	1.499930	4.67E-03	87
1.6	1.599907	5.81E-03	85

The single-tone test of the amplifier is performed at $f_{in} = 1$ MHz and $f_{in} = 40$ MHz to evaluate the THD of the designed amplifier. The output frequency spectrum of the amplifier is shown in Fig. 3.6. The $f_{in} = 1$ MHz tone has THD of -84.3 dB with 32 harmonics included. The $f_{in} = 40$ MHz tone has THD of -11.5 dB with 10 harmonics included. The sampling rates of $f_s = 100$ MHz and $f_s = 1000$ MHz are chosen for the capture of 1 MHz and 40 MHz tones. This behavior conforms with the results obtained earlier; as the input frequency increases, the loop gain decreases. This means the loop-gain will not be high enough to behave like a unity-gain buffer.

Table 3.4 lists the $PSRR^+$ of the designed amplifier for $C_L = 2$ pF as the ratio of A_{vdd} and A_{dm}, shown by the equation below:

$$PSRR^+(dB) = A_{vdd}(dB) - A_{dm}(dB)$$

The A_{vdd} is very low since there is current source implemented by cascode

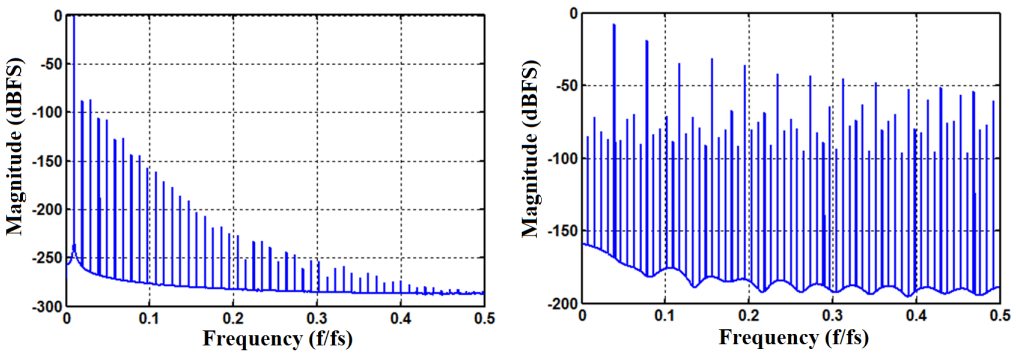

Figure 3.6: Output spectrum of modified folded cascode amplifier for $f_{in} = 1$ MHz and $f_{in} = 40$ MHz tones.

bias network of $M3$, $M4$, $M7$ and $M8$, which blocks the noise from V_{dd} to V_{output}.

Table 3.4: $PSRR^{+}$ of modified folded cascode amplifier.

V_{ICM} (V)	A_{vdd} (dB)	A_{dm} (dB)	$PSRR$ (dB)
1.0	-54.6	66.1	-120.7
1.2	-72.6	72.9	-145.5
1.4	-66.9	75.1	-142.0
1.6	-71.1	70.9	-142.0

The CM voltage of 1.4 V with output maximum swing of 600 mW was chosen for operation of the modified folded cascode amplifier, in order to utilize the best operating point of post-layout simulation.

3.2.2 ADC

The ADC is designed with the consideration of future system architecture development, where multi-channel sensing is required for acquisition of both PPG biopotential and NFC RF signals. The NFC receiver requires high sampling rate of 40 MS/s or more. The required effective number of bits N is set at 6-bit, with one bit reserved for noise power given the 600 mV output swing of the amplifier and SQNR requirements for both PPG processor and NFC standards. Thus, a flash ADC is preferred over low-power SAR or sigma-delta implementation, in order to utilize a single time-interleaved ADC for multi-channel read. For the given $V_{ocm} = 1.4$ V and amplifier output swing of 600 mV, then the flash ADC resistive voltage reference ladder is designed

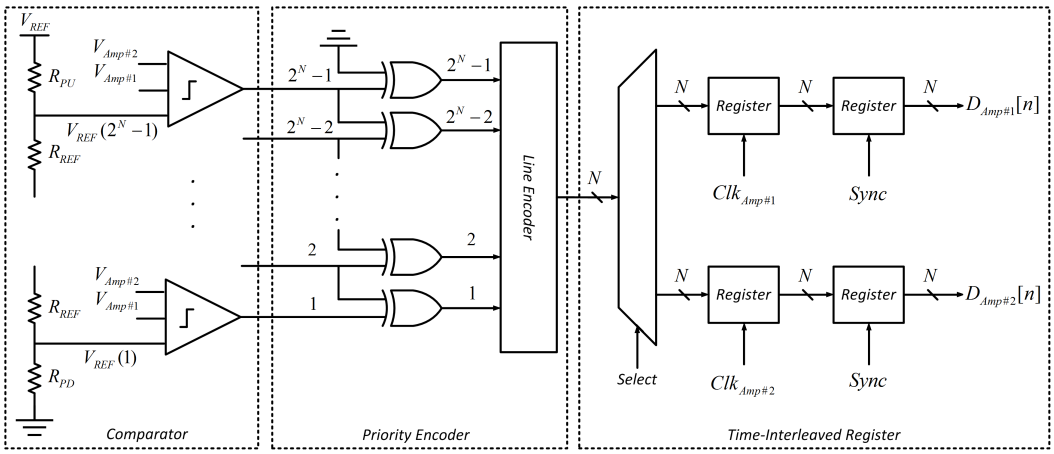

Figure 3.7: Dual-channel flash ADC architecture.

to provide 63 equally spaced reference voltages in the range of 1.4 ± 0.3 V, which is equivalent to 9.5 mV resolution. Fine adjustments can be made to amplifier V_{ICM} using external resistive bias network to compensate for the mismatch of ADC voltage reference ladder. This reference voltage selection sets the input-referred offset voltage and noise below the least significant bit (LSB). The dual-channel flash ADC consists of a comparator stage followed by an encoding stage and a data demultiplexer, as shown in Fig. 3.7. The demultiplexer registers are positive-edge triggered.

Mixed-Signal Comparator:

The dual-channel flash ADC uses a mixed-signal comparator based on a zero cancellation circuit [26], as shown in Fig. 3.8. The control signal sequence required for the operation of the ADC is shown in Fig. 3.9, generated by a synthesized digital rotator circuit with input frequency of 320 MHz. For layout considerations, the ADC conversion signals S_0 through S_4 and their complements should be buffered using digital repeater because of long interconnect signal paths, in order to preserve the signal integrity.

The dual-channel digital comparator uses 5 transmission gates, a single flying capacitor C_{FLY} and 2 digital inverters. The comparators are designed using minimum sized 2.5 V I/O devices and flying capacitor of 80 fF, implemented in DNW for the propose of noise isolation. The digital comparators are supplied by a 1.0 V external voltage rail. The resistive ladder network resistor sizing is calculated to achieve to the sampling frequency of 40 MS/s,

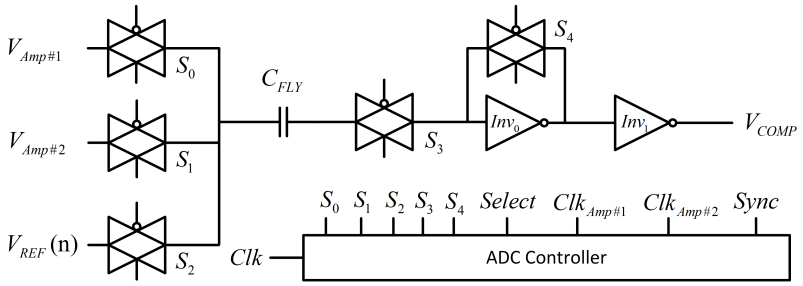

Figure 3.8: Dual-channel digital comparator based on zero-cancellation circuit.

considering the equivalent RC time constant of the post-layout comparators. The worst-case effective resistive path seen by the C_{FLY} includes layout interconnect parasitic resistance, two TG ON resistance, resistive reference ladder and inverter Inv_0 equivalent resistance, when signals S_2, S_3 and S_4 are high. This sets the required resistive voltage divider resistor sizes of Table 3.5 with $V_{REF} = 1.8$ V.

Table 3.5: Reference voltage ladder resistor selection.

Resistor (V)	Value (Ω)
R_{PU}	215
R_{PD}	20.5
R_{REF}	2.37K

Decimation Block:

The sampling rate conversion of 160000 is required to achieve the output sampling rate of 250 S/s required for the PPG processor. The down-sampling can be performed using a CIC filter. However, the significant additional architectural complexity of such high conversion rate CIC filter compared with the PPG processor is not justified. Therefore, a decimation block of 2^{17} is utilized to achieve a sample rate of 305 S/s, given the amplifiers input LPF of 4 Hz bandwidth, and a CIC filter should be implemented for future development of a zero-front-end NFC receiver block. Figure 3.10 shows the implementation of the decimation block, with negative-edge triggered registers for a half-time pipelining with the demultiplexer block. The clock divider of 2^{17} is implemented using a D flip-flop (DFF) chain to generate Clk_{PPG} from the

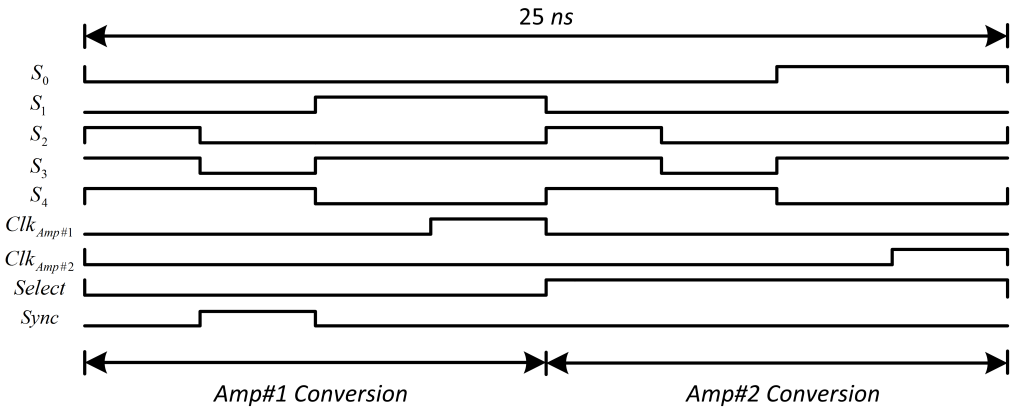

Figure 3.9: Dual-channel control signal sequence.

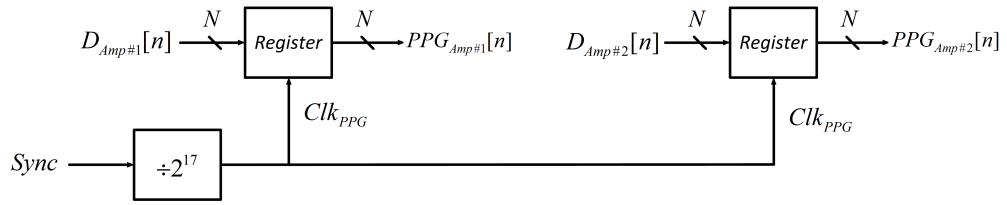

Figure 3.10: Decimation and buffering of discrete-time PPG biopotential signals.

Sync signal. The positive-edge of Clk_{PPG} is used for the PPG processor for a half-time pipelining with the decimation block.

ADC Performance Evaluation:

The single-tone test of the ADC is performed at 10 Hz and 13.56 MHz frequencies, with 34.8 dB and 27.6 dB measured SQNR, respectively. The measured SQNR satisfies both PPG processor and NFC standards requirements. The ADC power consumption of 3.72 mW was measured using post-layout simulation with R, C and CC parasitic components.

3.2.3 Digital Processor

The digital processor is implemented based on the PPG processor design of Chapter 2. The digital processor is synthesized and optimized for 305 S/s operation by the Clk_{PPG} clock signal. Figures 3.11 and 3.12 show the fixed-point architecture of the $H_1(z)$, $H_2(z)$ and MAC units of the proposed

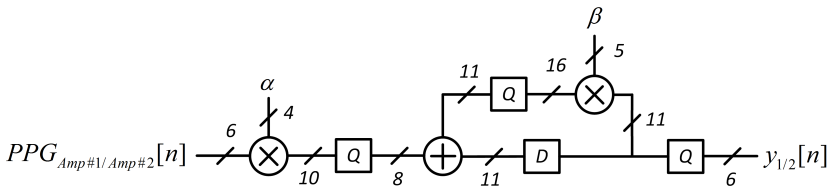

Figure 3.11: Fixed-point architecture of $H_1(z)$ and $H_2(z)$ discrete-time filters.

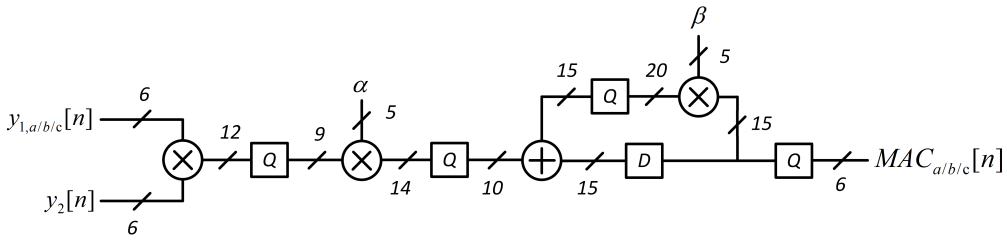

Figure 3.12: Fixed-point architecture of the MAC units.

algorithm.

For the delayed copy $y_{1,a/b/c}[n]$ generation of $y_1[n]$, a FIFO shift register buffer of length 32 is designed. Three multiplexers with parallel access to the registers of the FIFO buffer are designed to access the $y_{1,a/b/c}[n]$ delayed stream using the 15-bit $Select_{1,a/b/c}$ address bar. The 15-bit $Select_{1,a/b/c}$ are equally distributed between the three multiplexers, each 5-Bits, for 32 delayed value access. The delay generation block is shown in Fig. 3.13. The comparator and feedback update blocks of the PPG processor, as discussed in Chapter 2, are simply implemented and synthesized using conditional statements. The cross-correlation time of 2 s was chosen, as discussed in Chapter 2. A 4-bits TDE value, equivalent to maximum 48 ms, is computed and transmitted using the passive NFC transmitter at BaudRate of 9765 bit/s.

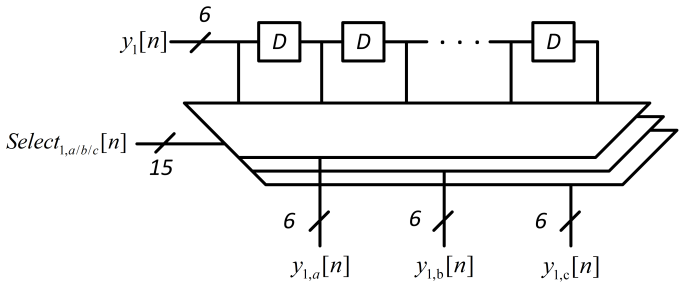

Figure 3.13: Delay generation block.

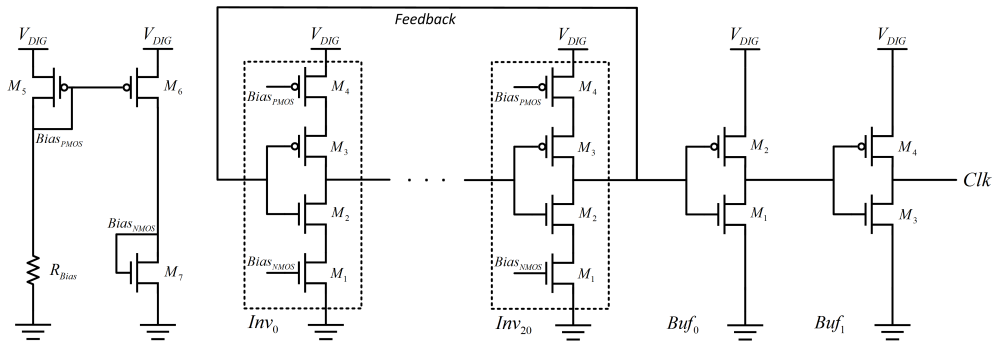

Figure 3.14: Ring-oscillator and current-starved inverter cells.

The PPG processor is implemented inside a DNW for noise isolation and supplied by a 1.0 V voltage rail. The power consumption of the passive NFC transmitter is measured to be 485 μW using post-layout simulations with R, C and CC parasitic components.

3.2.4 Clock Generator

The clock generator is designed using a ring-oscillator with current-starved inverter cells, which can be tuned externally using a bias resistor R_{Bias}. Figure 3.14 shows the ring-oscillator and the current-starved inverter cells and the bias network. The ring-oscillator is implemented using minimum-sized 1.0 V devices in a DNW for noise isolation. The bias network is a current mirror of transistors $M5$, $M6$ and $M7$ with the same W/L size as the current-starved inverter cells $M1$ and $M4$ transistors. The current limiting PMOS (M4) and NMOS (M1) devices of current-starved inverter cells are sized to W/L = 1.58/0.06 and 0.52/0.06 in order to enable Clk clock frequency of 320 MHz in post-layout simulations. The ring-oscillator is implemented with 21 stages of current-starved inverter cell, followed by a minimum-sized buffer stage. The clock jitter and delay are not critically important in the design of system blocks, and only a network of clock buffers is utilized to deliver the clock signal Clk. The power consumption of the clock generator is measured to be 245 μW using post-layout simulations with R, C and CC parasitic components.

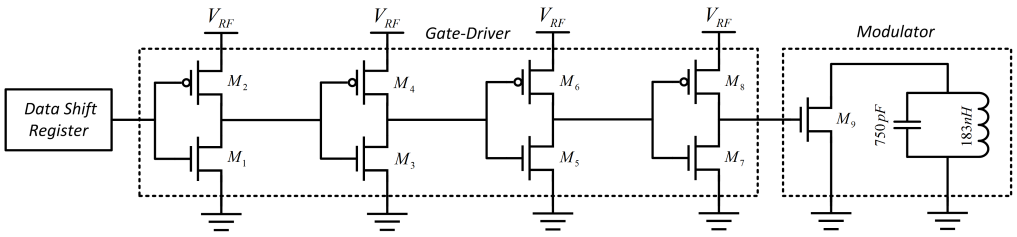

Figure 3.15: The passive NFC transmitter gate-driver and modulator blocks.

3.2.5 Passive NFC Transmitter

The passive NFC transmitter is used to transmit the processed information through the loop-antenna. Passive NFC transmission is based on changing the characteristic impedance of the loop-antenna [24] for a amplitude shift-keying (ASK) modulation scheme. The transmitter consists of a gate-driver and power switch controlled by the PPG processor. The power switch is simply used as a modulator to either short or open the terminals of the loop-antenna. The gate-driver and power switch are implemented using 3.3 V devices in order to protect them from voltage stress induced on the loop-antenna, as well as switching ringing. The power switch has an equivalent W/L size of 11200/0.5. The equivalent loop-antenna resistance and inductance is measured across multiple flexible epidermal substrate samples to be at 36 mΩ and 183 nH. The power switch has an equivalent $r_{ds}(ON)$ resistance of 56 mΩ with a 4-stage inverter chain gate-driver of tapering-factor 10 to limit the switching ringing to 180 mV when a 3.1 V_{pp} sinusoid is induced across the loop-antenna. For the maximum near-field antenna loading effect and consequently maximum ASK modulation depth, the tank circuit of the loop-antenna should be tuned to 13.56 MHz of NFC systems with a 750 pF capacitor. The gate-driver is directly connected to a parallel to serial shift register, as shown in Fig. 3.15. The shift register loads the 4-bit computed TDE value in an 10-bit data packages for serial communication. The data package is shown in Fig. 3.16 with Start-Bit, Stop-Bit and no Parity-Bit. Given the clock frequency of 320 MHz, a clock division of 2^{16} using serial chain DFF is used to achieve bit rate of 9765 bit/s for the data shift register. The data is transmitted at the end of each 2 s cross-correlation period. The power consumption of the passive NFC transmitter is measured to be 837 μW using post-layout simulations with R, C and CC parasitic components.

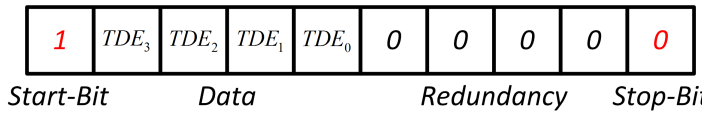

Figure 3.16: The passive NFC transmitter data package for 10-bit serial communication with no Parity-Bit.

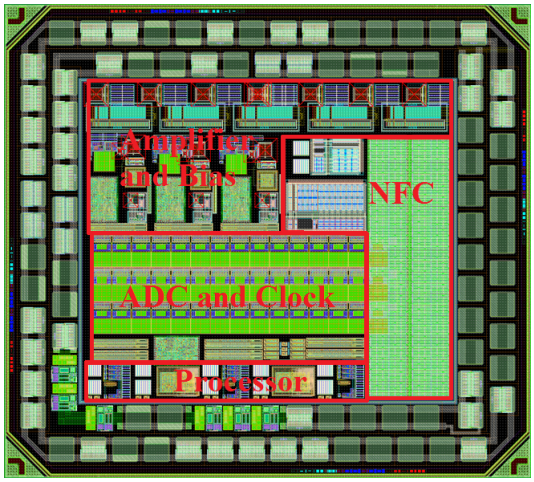

Figure 3.17: Designed ASIC for in-sensor optical systolic blood-pressure processing on flexible epidermal substrates.

3.2.6 Energy Harvesting and Start-up

The energy harvesting and start-up circuitry have been left out for future development. Therefore, supply voltages of 1.8 V and 1.0 V are to be supplied using external linear regulators for the current ASIC design.

3.3 ASIC Layout

The system is implemented in a TSMC 65nm-GP process with a total area of 1.15 mm^2. Figure 3.17 shows the final layout without metal-fill and top metals for visibility. The area and power breakdown of the ASIC is provided in Fig. 3.18. The layout uses metals 1 through 9. The total of 80 pins are used for $QFP80$ packaging. The layout also includes experimental parts of input LPF, bias/gain networks, NFC amplifier and CIC filtering stages, which can be bypassed, to test building blocks of future developments.

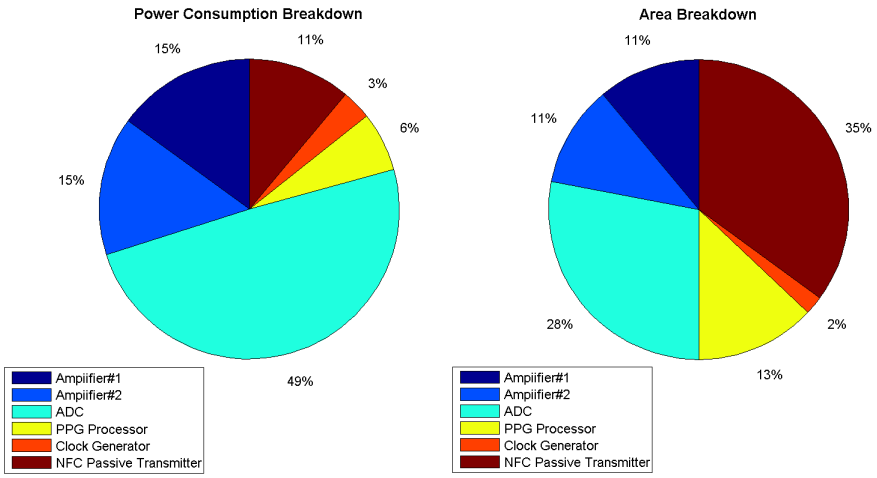

Figure 3.18: Power consumption and area breakdown of the designed ASIC.

3.4 ASIC Performance

The designed ASIC testing and benchmarking on flexible epidermal substrate is planned for future work, with the addition of an energy harvesting block. A post-layout full system simulation with synthetic PPG biopotential signals is performed. The full system post-layout simulation uses the reduced R, C and CC parasitic components to allow long functional simulations. Figure 3.19 shows the performance of the designed ASIC with synthetic PPG signals of 0.5 Hz sinusoid and step delay functions. The ASIC performance is comparable with the PPG processor designed in Chapter 2.

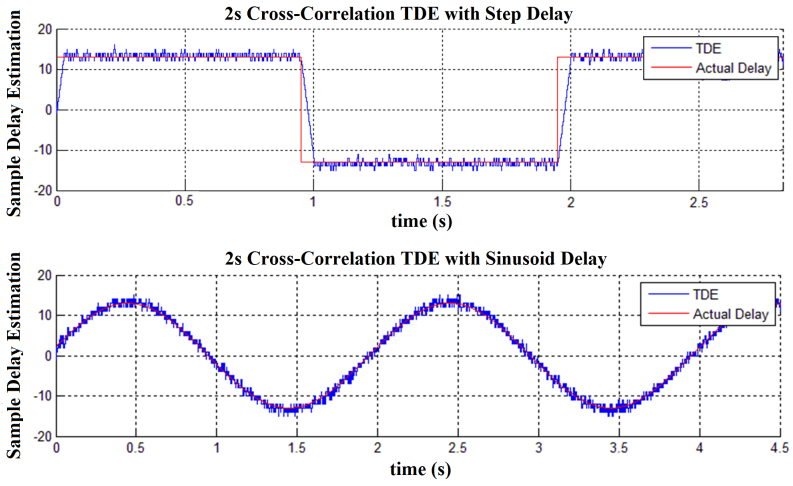

Figure 3.19: TDE performance of the designed ASIC with synthetic sinusoid and step delay functions.

CHAPTER 4

CONCLUSIONS AND FUTURE WORK

This work demonstrated the first in-sensor ECG and PPG processor implementations on flexible epidermal substrates using resource limited hardware platforms, as well as an ASIC development of the PPG processor. The implemented discrete component system has been successfully tested on an adult human and achieved the required performance standards. The next steps include fabrication and testing of the designed ASIC, inclusion of more complex algorithms for EMG, PPG and ECG signals, and a zero-front-end NFC receiver. In addition, the current implementation can be further optimized and improved by the use of machine learning kernels.

APPENDIX A

FIXED-POINT FILTER DESIGN

Practical digital filter implementations require finite-precision representation that includes input, output, coefficient, and internal signal quantization. This process is under the assumption of statistical independence between unquantized numerical value and the quantization noise, which can be modeled as an additive model shown in Fig. A.1 and described by the following equation:

$$y\left[n\right] = y_c\left[n\right] + q_y\left[n\right]$$

where $y[n]$, $y_c[n]$, and $q_y[n]$ are the quantized value, unquantized value, and the quantization noise, respectively. The two's complement numeric system is the conventional method of choice for DSP systems finite-precision representation. The decimal value $-1 \leq y\left[n\right] < 1$ in the binary form of $\left[b_0.b_1b_2\ldots b_{B_y-1}\right]$ is calculated using the following equation:

$$y[n] = -b_0 + \sum_{i=1}^{B_y-1} b_i 2^{-i}$$

The quantization noise is modeled as an additive uniform distribution, under the assumption of B_y being large enough, and $q_y[n]$ independent of $y[n]$. This is shown using the following equations:

$$-\frac{\Delta}{2} \leq q_y\left[n\right] \leq \frac{\Delta}{2}$$

$$\Delta = \frac{V_{max} - V_{min}}{2^{B_y}}$$

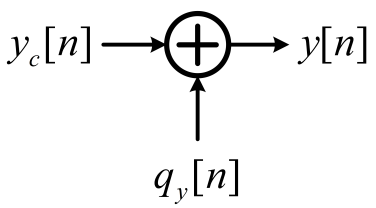

Figure A.1: Additive quantization noise model.

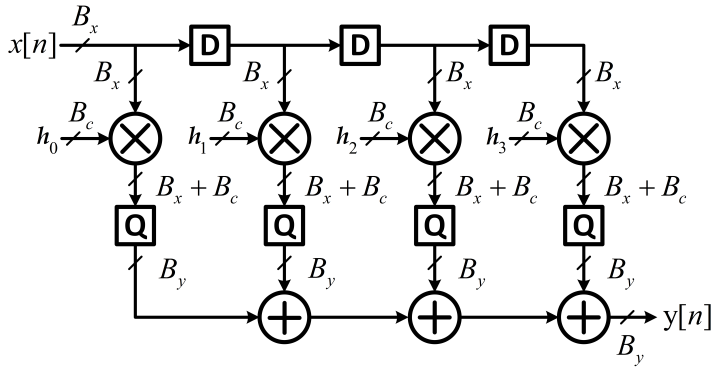

Figure A.2: A 3-tap discrete-time FIR filter.

Thus, the quantization error of input the signal is calculated using the following equation:

$$\sigma_{q_x}^2 = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} \frac{1}{\Delta} x^2 dx = \frac{\Delta^2}{12}$$

Similarly, the filter coefficient quantization noise can be calculated using the following equation:

$$\sigma_{q_c}^2 = \sigma_x^2 \sum_{k=0}^{N-1} q_h^2 [k]$$

where $q_h = (H_{float-norm} - H_{fx})$ is the fixed-point filter coefficient error. The fixed-point filter coefficients are calculated using the following equations:

$$H_{float-norm}(z) = \frac{H_{float}(z)}{\max(|h[k]|)}$$

$$H_{fx}(z) = \min\left(\frac{round\left(H_{float-norm}(z)\, 2^{B_h-1}\right)}{2^{B_h-1}}, 1 - \frac{1}{2^{B_h-1}}\right)$$

The FIR filter, see Fig. A.2, conventionally employs round-off blocks after the coefficient multiplications from B_x+B_c to B_y, where the additional round-off noise of $\sigma_{q_e}^2$ induced for the N-tap filter is calculated using the following equation:

$$\sigma_{q_e}^2 = N\frac{2^{-2B_y}}{12}$$

Thus, the final output noise due to quantization is calculated using the following equation:

$$\sigma_{q_y}^2 = \sigma_{q_x}^2 + \sigma_{q_c}^2 + \sigma_{q_e}^2$$

APPENDIX B

PTA PERFORMANCE USING MIT/BIH DATABASE

Table B.1: Results of evaluating the real-time R-peak detection algorithm using the MIT/BIH database

Tape (No.)	Total (Beats)	FP (Beats)	FN (Beats)	Failed Detection (%)
100	2273	0	0	0
101	1865	5	3	0.43
102	2187	0	0	0
103	2084	0	0	0
104	2230	1	0	0.04
105	2572	67	22	3.46
106	2027	5	2	0.05
107	2137	0	2	0.09
108	1763	199	22	12.54
109	2532	0	1	0.04
111	2124	1	0	0.05
112	2539	0	1	0.04
113	1795	0	0	0
114	1879	3	17	1.06
115	1953	0	0	0
116	2412	3	22	1.04
117	1535	1	1	0.13
118	2275	1	0	0.04
119	1987	1	0	0.05
121	1863	4	7	0.59
122	2476	1	1	0.08
123	1518	0	0	0
124	1619	0	0	0
200	2601	6	3	0.35
201	1963	0	10	0.51
202	2136	0	4	0.19
203	2982	53	30	2.78
205	2656	0	2	0.08
207	1862	4	4	0.43
208	2956	4	14	0.60
209	3004	3	0	0.10
210	2647	2	8	0.38
212	2748	0	0	0
213	3251	1	2	0.09
214	2262	2	4	0.26
215	3363	0	1	0.03
217	2208	4	6	0.45
219	2154	0	0	0
220	2048	0	0	0
221	2427	2	0	0.08
222	2484	101	81	7.33
223	2605	1	0	0.04
228	2053	25	5	1.46
230	2256	1	0	0.04
231	1886	0	0	0
232	1780	6	1	0.39
233	3079	0	1	0.03
234	2753	0	0	0
48 patients	116137	507	277	0.675

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