DIGITAL ENHANCEMENT TECHNIQUES
FOR FRACTIONAL-N FREQUENCY SYNTHESIZERS

BY

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DISSERTATION

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ABSTRACT

Meeting the demand for unprecedented connectivity in the era of internet-of-things (IoT) requires extremely energy efficient operation of IoT nodes to extend battery life. Managing the data traffic generated by trillions of such nodes also puts severe energy constraints on the data centers. Clock generators that are essential elements in these systems consume significant power and therefore must be optimized for low power and high performance. The focus of this thesis is on improving the energy efficiency of frequency synthesizers and clocking modules by exploring design techniques at both the architectural and circuit levels.

In the first part of this work, a digital fractional-N phase locked loop (FNPLL) that employs a high resolution time-to-digital converter (TDC) and a truly $\Delta\Sigma$ fractional divider to achieve low in-band noise with a wide bandwidth is presented. The fractional divider employs a digital-to-time converter (DTC) to cancel out $\Delta\Sigma$ quantization noise in time domain, thus alleviating TDC dynamic range requirements. The proposed digital architecture adopts a narrow range low-power time-amplifier based TDC (TA-TDC) to achieve sub 1ps resolution. Fabricated in 65nm CMOS process, the prototype PLL achieves better than -106dBc/Hz in-band noise and 3MHz PLL bandwidth at 4.5GHz output frequency using 50MHz reference. The PLL achieves excellent jitter performance of 490fs$_{\text{rms}}$, while consumes only 3.7mW. This translates to the best reported jitter-power figure-of-merit (FoM$_{\text{J}}$) of -240.5dB among previously reported FNPLLs.

Phase noise performance of ring oscillator based digital FNPLLs is severely compromised by conflicting bandwidth requirements to simultaneously suppress oscillator phase and quantization noise introduced by the TDC, $\Delta\Sigma$ fractional divider, and digital-to-analog converter (DAC). As a consequence, their FoM$_{\text{J}}$ that quantifies the power-jitter tradeoff is at least 25dB worse than their LC-oscillator based FNPLL counterparts. In the second part of this thesis,

we seek to close this performance gap by extending PLL bandwidth using quantization noise cancellation techniques and by employing a dual-path digital loop filter to suppress the detrimental impact of DAC quantization noise. A prototype was implemented in a 65nm CMOS process operating over a wide frequency range of 2.0GHz-5.5GHz using a modified extended range multi-modulus divider with seamless switching. The proposed digital FNPLL achieves $1.9\text{ps}_{\text{rms}}$ integrated jitter while consuming only 4mW at 5GHz output. The measured in-band phase noise is better than -96 dBc/Hz at 1MHz offset. The proposed FNPLL achieves wide bandwidth up to 6MHz using a 50 MHz reference and its FoM_J is -228.5dB, which is at about 20dB better than previously reported ring-based digital FNPLLs.

In the third part, we propose a new multi-output clock generator architecture using open loop fractional dividers for system-on-chip (SoC) platforms. Modern multi-core processors use per core clocking, where each core runs at its own speed. The core frequency can be changed dynamically to optimize for performance or power dissipation using a dynamic frequency scaling (DFS) technique. Fast frequency switching is highly desirable as long as it does not interrupt code execution; therefore it requires smooth frequency transitions with no undershoots. The second main requirement in processor clocking is the capability of spread spectrum frequency modulation. By spreading the clock energy across a wide bandwidth, the electromagnetic interference (EMI) is dramatically reduced. A conventional PLL clock generation approach suffers from a slow frequency settling and limited spread spectrum modulation capabilities. The proposed open loop fractional divider architecture overcomes the bandwidth limitation in fractional-N PLLs. The fractional divider switches the output frequency instantaneously and provides an excellent spread spectrum performance, where precise and programmable modulation depth and frequency can be applied to satisfy different EMI requirements. The fractional divider has unlimited modulation bandwidth resulting in spread spectrum modulation with no filtering, unlike fractional-N PLL; consequently it achieves higher EMI reduction. A prototype fractional divider was implemented in a 65nm CMOS process, where the measured peak-to-peak jitter is less than 27ps over a wide frequency range from 20MHz to 1GHz. The total power consumption is about 3.2mW for 1GHz output frequency. The all-digital implementation of the divider occupies the smallest area of 0.017mm^2 compared to state-of-the-art designs.

As the data rate of serial links goes higher, the jitter requirements of the clock generator become more stringent. Improving the jitter performance of conventional PLLs to less than ($200\text{fs}_{\text{rms}}$) always comes with a large power penalty (tens of mWs). This is due to the PLL coupled noise bandwidth trade-off, which imposes stringent noise requirements on the oscillator and/or loop components. Alternatively, an injection-locked clock multiplier (ILCM) provides many advantages in terms of phase noise, power, and area compared to classical PLLs, but they suffer from a narrow lock-in range and a high sensitivity to PVT variations especially at a large multiplication factor (N). In the fourth part of this thesis, a low-jitter, low-power LC-based ILCM with a digital frequency-tracking loop (FTL) is presented. The proposed FTL relies on a new pulse gating technique to continuously tune the oscillator's free-running frequency. The FTL ensures robust operation across PVT variations and resolves the race condition existing in injection locked PLLs by decoupling frequency tuning from the injection path. As a result, the phase locking condition is only determined by the injection path. This work also introduces an accurate theoretical large-signal analysis for phase domain response (PDR) of injection locked oscillators (ILOs). The proposed PDR analysis captures the asymmetric nature of ILO's lock-in range, and the impact of frequency error on injection strength and phase noise performance. The proposed architecture and analysis are demonstrated by a prototype fabricated in 65 nm CMOS process with active area of 0.25mm^2. The prototype ILCM multiplies the reference frequency by 64 to generate an output clock in the range of 6.75GHz-8.25GHz. A superior jitter performance of $190\text{fs}_{\text{rms}}$ is achieved, while consuming only 2.25mW power. This translates to a best FoM$_{\text{J}}$ of -251dB.

Unlike conventional PLLs, ILCMs have been fundamentally limited to only integer-N operation and cannot synthesize fractional-N frequencies. In the last part of this thesis, we extend the merits of ILCMs to fractional-N and overcome this fundamental limitation. We employ DTC-based QNC techniques in order to align injected pulses to the oscillator's zero crossings, which enables it to pull the oscillator toward phase lock, thus realizing a fractional-N ILCM. Fabricated in 65nm CMOS process, a prototype 20-bit fractional-N ILCM with an output range of 6.75GHz-8.25GHz consumes only 3.25mW. It achieves excellent jitter performance of $110\text{fs}_{\text{rms}}$ and $175\text{fs}_{\text{rms}}$ in integer- and fractional-N modes respectively, which translates to the best-reported FoM$_{\text{J}}$ in both integer- (-255dB) and fractional-N (-252dB)

modes. The proposed fractional-N ILCM also features the first-reported rapid on/off capability, where the transient absolute jitter performance at wake-up is bounded below 4ps after less than 4ns. This demonstrates almost instantaneous phase settling. This unique capability enables tremendous energy saving by turning on the clock multiplier only when needed. This energy proportional operation leverages idle times to save power at the system-level of wireline and wireless transceivers.

To my parents, my wife, my beloved kids: Nour and Omar.

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All gratitude to Allah

Pursuing my doctoral degree was mainly motivated by a genuine passion for research and innovation. During this long journey of dedication to accomplish world-class research contributions, I gained more insight and better understanding of many aspects of life, and I acquired invaluable skills and qualities personally and professionally. This was made possible only with the unconditional support and help that I have received from my family, friends, and colleagues. For that, I would like to thank all the people who made my Ph.D. journey enjoyable and such a pleasant experience.

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CHAPTER 1

INTRODUCTION

The internet is shaping our life today, where billions of cell phones, tablets, wearables, and internet of thinks (IoT) sensors are connected together. With this unprecedented connectivity, an energy bottleneck emerges at both ends: the battery operated mobile platforms and the data centers that support these bandwidth-intensive applications (see Fig. 1.1). In mobile platforms energy efficiency is essential to save the battery life, while in data centers energy efficiency is critical to save the electric power and cooling costs. Improving energy efficiency of data centers' network components is extremely important to sustain their growth. Fig. 1.2 shows a block diagram of a typical serial link architecture with embedded clocking used in data centers networks. At the transmitter side, parallel data stream is serialized into a high speed stream using a clean high frequency clock. A clock generator synthesizes this clock relying on an external crystal reference clock. At the receiver side, the clock and data recovery (CDR) extracts clock and data from the equalized received signal, then data is de-serialized into a low frequency parallel data stream. Clock generation at TX and clock and data recovery (CDR) at RX are major sources of power consumption in a link, and typically consume 35-50% of the total link power. This is mainly driven by the clock jitter requirements, which distorts both transmitted and recovered data and can limit the link bit-error rate.

On the other hand, mobile platforms have many modules with diverse functionalities. Typically, different radios including 4G-LTE, Bluetooth, and WiFi are major sources of power consumption. A typical RF front-end of a WiFi radio is shown in Fig. 1.3 as an example. The role of the frequency synthesizer is very critical as it synthesizes the RF carrier of the transmitted signal, and it synthesizes the down-conversion signal at the receiver. Typically, the synthesizer consumes half of the total transceiver power. Other modules in
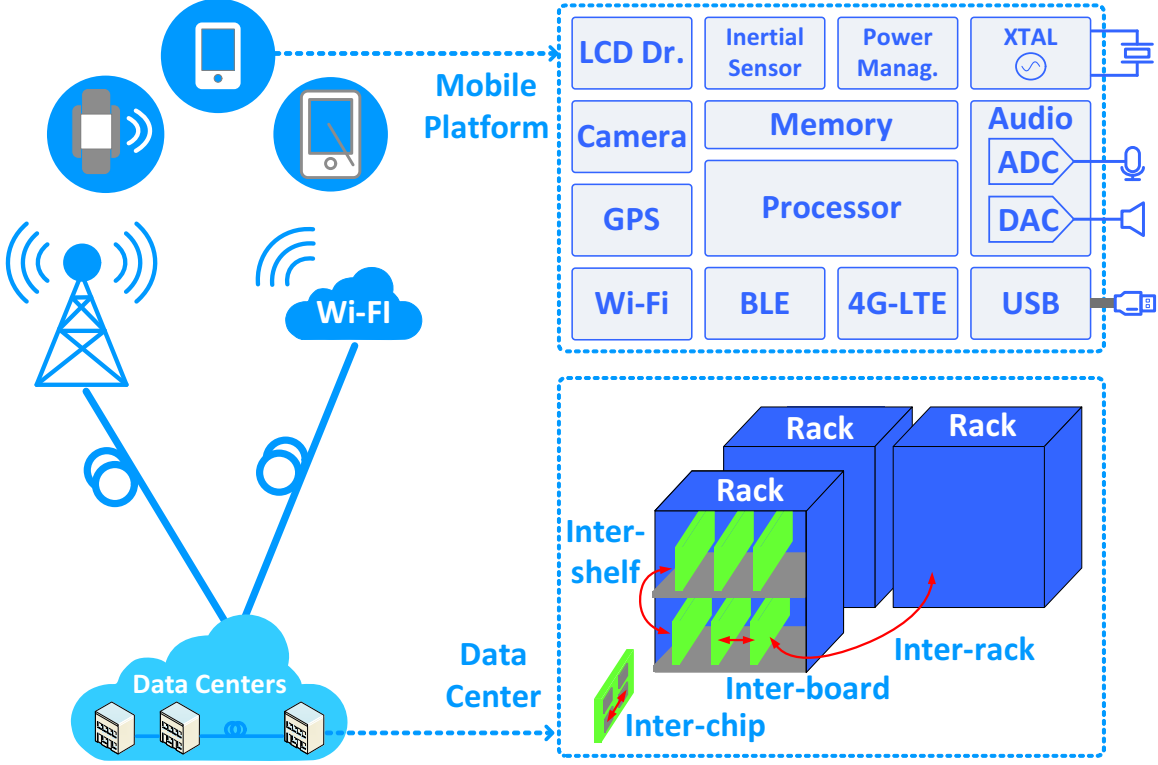
Figure 1.1: Applications of clock generators in the era of internet of thinks (IoT).
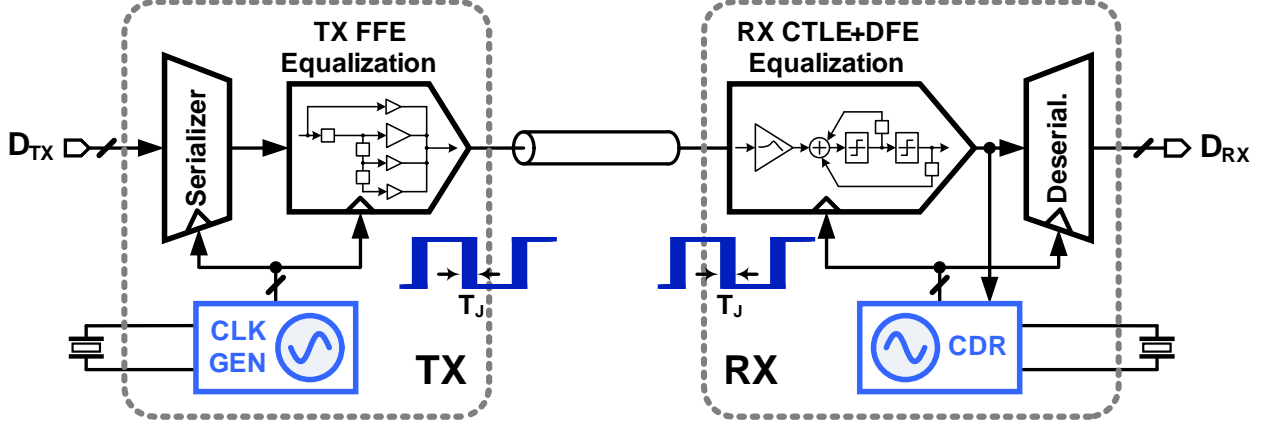
Figure 1.2: Block diagram of a serial link with embedded clocking.

the mobile platform like audio data converters, processors, and memory need clocks. We can clearly see that clock and frequency synthesizers play a critical role in different modules, and can limit their overall performance and power consumption. Therefore, enhancing the energy efficiency of frequency synthesizers is highly desirable.
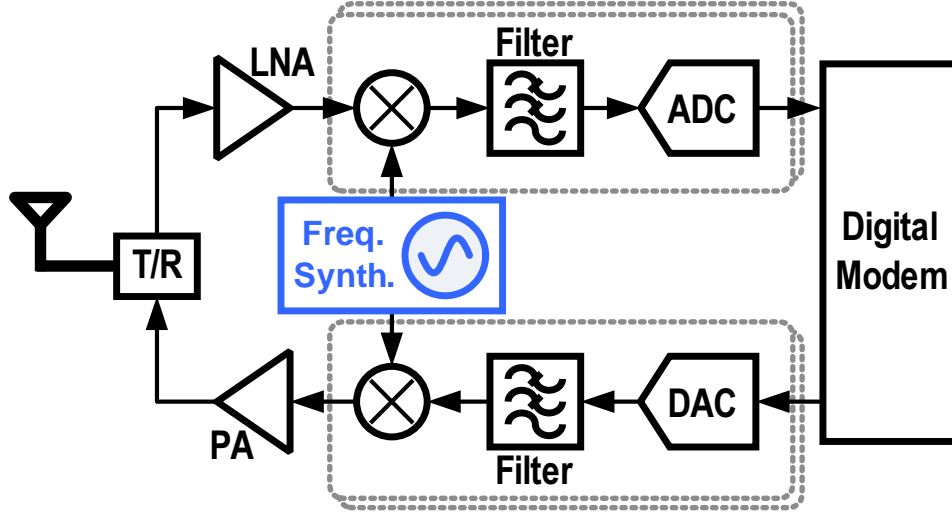
Figure 1.3: Block diagram of a typical wireless transceiver.

1.1 Frequency Synthesizers Applications

1.1.1 Fractional-N Frequency Synthesizers for Wireless Transceivers

Wireless transceivers require a fractional-N frequency synthesizer with a very fine frequency resolution. By multiplying the reference frequency by a fractional factor $(N+\alpha)$, defined by the frequency control word (FCW), the carrier frequency of different channels is synthesized as shown in Fig. 1.4. Ideally, the synthesizer generates a perfect single tone, but in reality, its output spectrum has undesired phase noise and spurious tones. This corrupts the phase-modulated signals in the process of up-conversion or down-conversion. Another effect occurs in the receiver path in the presence of a large interferer signal as illustrated in Fig. 1.4. The spurs may down-convert the interferer signal into the signal bandwidth, degrading the receiver noise figure. For example, if the interferer is 60dB above the desired signal, then with a 70dBc spur, the corruption is only 10dB below the signal.

1.1.2 Multi-standard Flexible SerDes

Wireline transceivers (or SerDes) usually use integer-N PLLs to meet the tight constraints on the clock jitter for various standards as depicted in Fig. 1.2. Recently, there is a growing demand for multi-standard-compliant transceivers integrated into a single chip with a wide
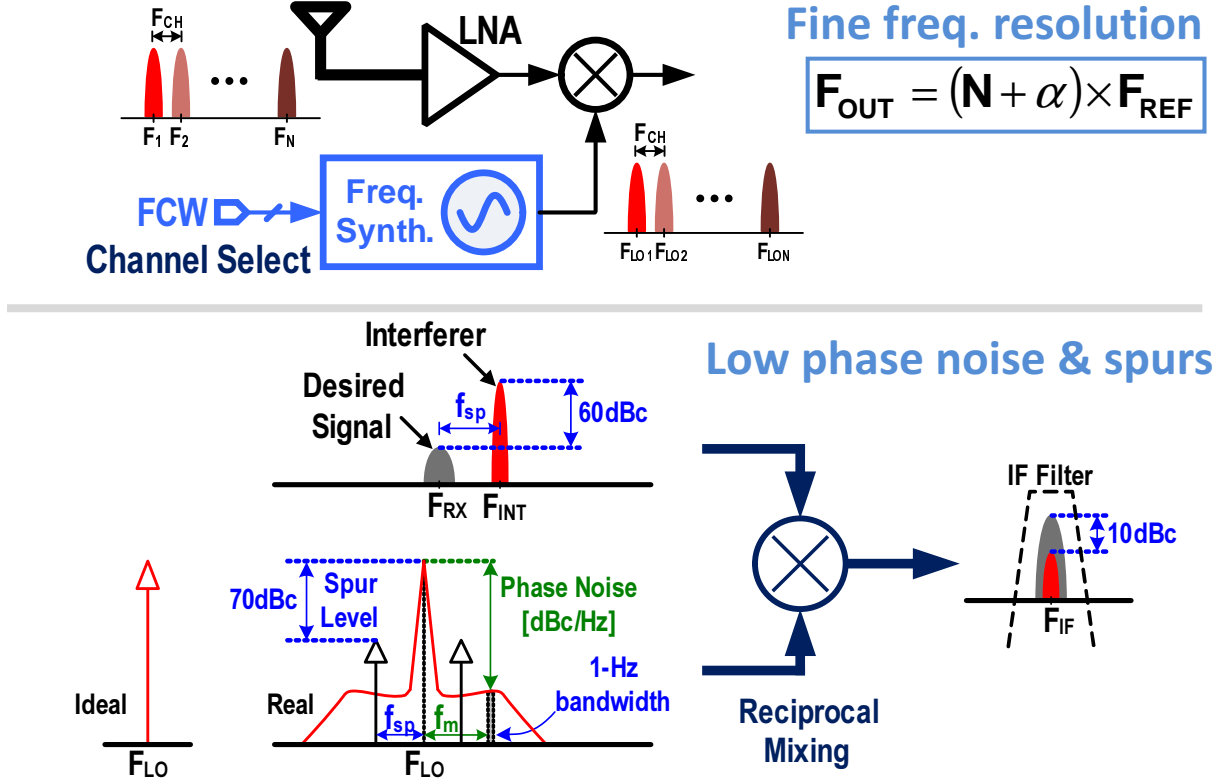
Figure 1.4: The role of frequency synthesizer in wireless transceivers illustrating the impact of its phase noise and spurious tones.

and continuous range of data-rates. To save the cost of multiple input crystal references, fractional-N frequency synthesis is highly desirable in both the transmitter and the receiver. A flexible fractional-N clock generator has to cover wide frequency range with fine frequency resolution to serve various standards. It has to provide multiple phases with stringent jitter performance with minimum power and area.

1.1.3 Fractional-N Clocking for Micro-Processors

Modern multi-core processors use per core clocking (see Fig. 1.5(a)), where each core runs at its own speed [1]. The power manager takes input from environmental sensors, performance counters, and software requests, and continuously adjusts the frequencies of different cores as shown in Fig. 1.5(b). The core frequency can be changed dynamically to optimize for performance or power dissipation using a dynamic frequency scaling (DFS) technique. Changing

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the core clock frequency rapidly is required to enhance the energy efficiency. However, this process has to be carefully managed to ensure code execution without any interruption. Therefore, the frequency transitions have to be very smooth and well controlled with no undershoots. The second main requirement in processor clocking is the capability of spread spectrum frequency modulation. By spreading the clock energy across a wide bandwidth, the electromagnetic interference (EMI) is dramatically reduced as demonstrated in Fig. 1.5(b). Processors use programmable spread-spectrum clocking (SSC) to satisfy the electromagnetic compatibility (EMC) regulations.

1.2   Frequency Synthesizers Architectures

1.2.1   Analog Integer-N PLL

Phase locked loop (PLL) is a feedback system that is used to obtain a highly stable output frequency. Analog charge pump PLL, shown in Fig. 1.6, has been the dominant architecture for frequency multiplication. It consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a feedback divider. Adding a divide-by-N block in feedback enables frequency multiplication. The PFD detects the phase/frequency error between the reference clock and the feedback clock, and correspondingly generates a pair of digital pulses to drive the CP. The CP then converts the digital pulses into current pulses that get filtered and converted into voltage through passive LF network. The simplest LF network consists of a resistor and a capacitor connected in series. The resulting control voltage (V_{CTRL}) drives the VCO towards phase and frequency lock.

The negative feedback loop forces the divided-down VCO output phase to follow the reference clock phase. In steady state, the phase of the feedback clock is locked to the phase of the reference clock, where the phase error remains constant and ideally zero. This is why it is referred to as a phase locked loop. We use a feedback system based on phase rather than frequency to assure zero frequency error and exact frequency multiplication [2]. The

POWER7™ Microprocessor
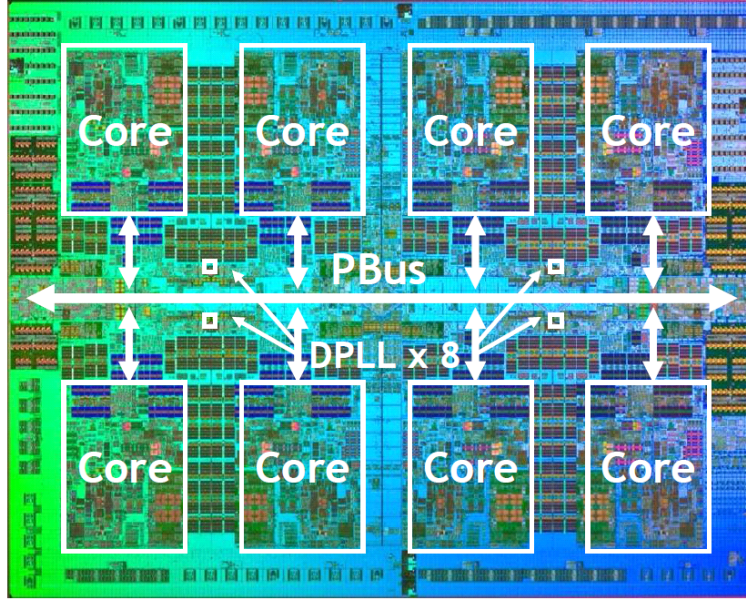
(a)
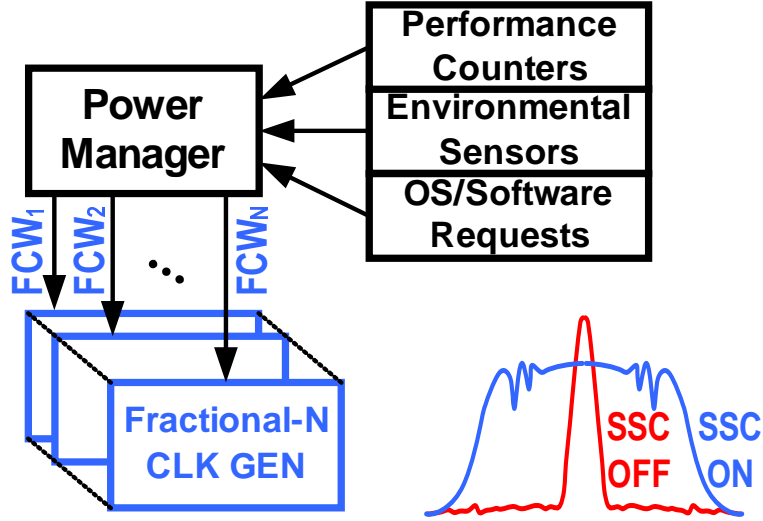
(b)

Figure 1.5: (a) Die photo of an eight-core POWER7 microprocessor using per-core clocking [1]. (b) Simplified block diagram of microprocessor frequency control.

output frequency is a multiple of the reference frequency:

$$F_{OUT} = N \times F_{REF} \tag{1.1}$$

Like any other feedback system, PLL system has to be analyzed and designed carefully to guarantee loop stability. Ignoring the sampling nature of the PFD and the non-linear transient behavior of PLLs, a basic s-domain linear model is usually used for stability analysis. Each block is replaced by a linear representation of its function. PFD/CP is replaced by a difference block followed by a gain factor K_{PD}. The LF is replaced by its transfer function $Z(s)$. The VCO is represented by a transfer function that simply relates its output F_{OUT} with V_{CTRL}, as:

$$F_{OUT} = F_O + K_{VCO} \times (V_{CTRL} - V_O) \tag{1.2}$$

where F_O is the VCO frequency when $V_{CTRL} = V_O$, and K_{VCO} is the VCO gain. Since phase is the integral of frequency, then the VCO can be replaced by a gain and an integrator K_{VCO}/s. A simple linear model of the PLL is shown in Fig. 1.7. In addition to stability analysis, this model is also used to study open and closed loop response, settling time, and phase noise of PLLs. Loop dynamics affect how the noise of each block appears at the output; for example, the VCO noise is high-pass filtered while reference, divider, and PFD/CP noise are low-pass filtered. Usually, the PLL bandwidth is chosen to optimize the overall jitter performance. While an integer-N PLL can achieve excellent jitter, its frequency resolution is limited by the reference frequency due to the nature of integer-N multiplication.
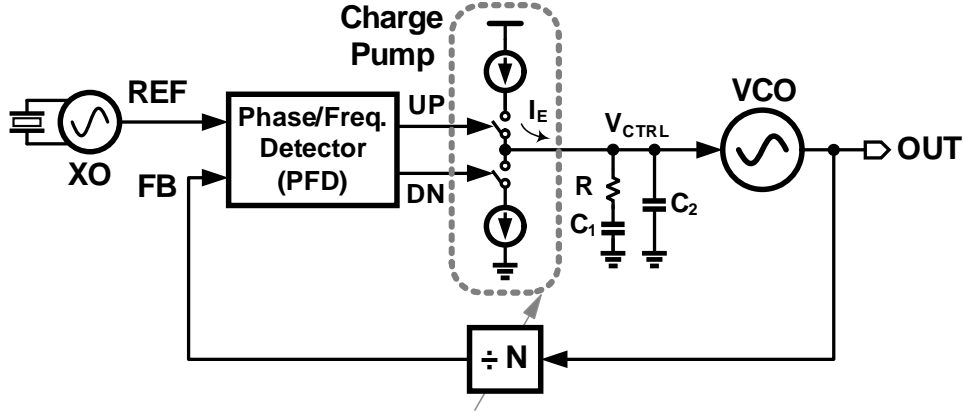
Figure 1.6: Simplified block diagram of integer-N charge pump PLL.
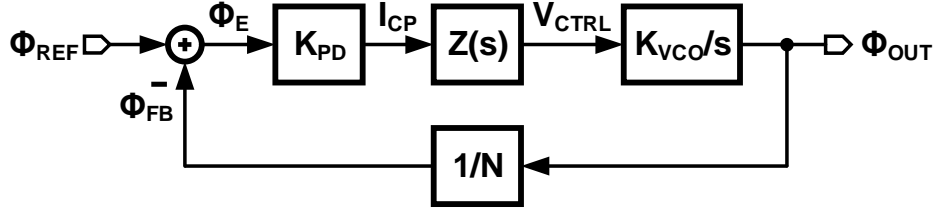
Figure 1.7: Linear model of charge pump PLL.

1.2.2 Analog Fractional-N PLL

A fractional-N PLL (FNPLL) is an extension to integer-N PLL to perform fractional-N frequency multiplication with very fine frequency resolution (see Fig. 1.8), thus it can be used for phase modulation/frequency modulation (FM). Since the feedback divider is a digital circuit, it can only divide by an integer number. However, if the division factor is alternated between N and $N + 1$, effectively a fractional division is achieved. For example, $N = 4$ is used for 3 division cycles and $N = 5$ is used for 1 division cycle. On average, the input frequency is divided by 4.25. The simplest way to control the divider is passing a k-bit fractional control value α to a k-bit digital accumulator. Then use the 1-bit carry out $n_F[n]$ as a modulus control of the divider. The PLL still can lock in an average sense and the output frequency is related to the reference frequency by:

$$F_{OUT} = (N + \text{avg}(n_F[n])) \times F_{REF} = (N + \alpha) \times F_{REF} \qquad (1.3)$$

Although switching the division ratio instantaneously is simple to realize, this technique exhibits instantaneous frequency errors and introduces quantization noise $e_q[n]$ into the loop. $e_q[n]$ is low-pass filtered by the PLL feedback loop before appearing at the output as a deterministic jitter (DJ). Fig. 1.9 demonstrates the timing waveform of a fractional division of 4.25. A deterministic jitter of $0.25 \times T_{OUT}$ appears in the feedback clock in the first cycle and accumulates to $0.75 \times T_{OUT}$ by the third cycle. In the fourth cycle, the output clock aligns with the ideal clock. The deterministic jitter pattern repeats every four cycles and it is directly related to $e_q[n]$ by $DJ[n] = -e_q[n] \times T_{OUT}$. This deterministic jitter will be filtered by the low-pass PLL transfer function before appearing at the output. Noise shaping techniques are commonly used to suppress in-band quantization noise in high resolution

digital-to-analog converters (DACs). Similarly, noise shaping using digital delta-sigma ($\Delta\Sigma$) modulators can reduce fractional divider quantization noise in FNPLL (which acts as a digital-to-frequency converter). By replacing the accumulator (which resembles a 1st order $\Delta\Sigma$ modulator) by a higher order $\Delta\Sigma$ modulator, $e_q[n]$ is high-pass shaped, and exhibits more suppression by the same low-pass PLL transfer function.
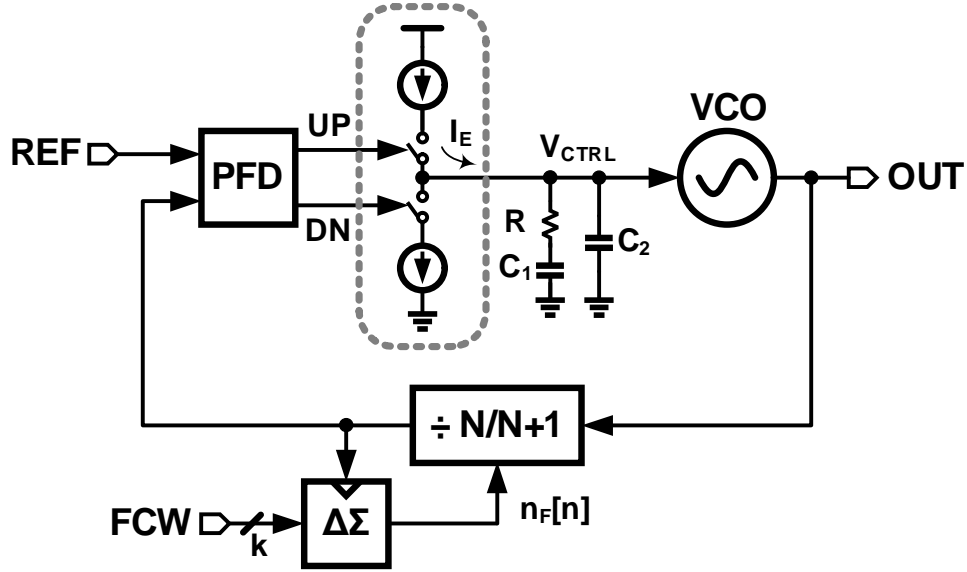
Figure 1.8: Simplified block diagram of analog FNPLL.
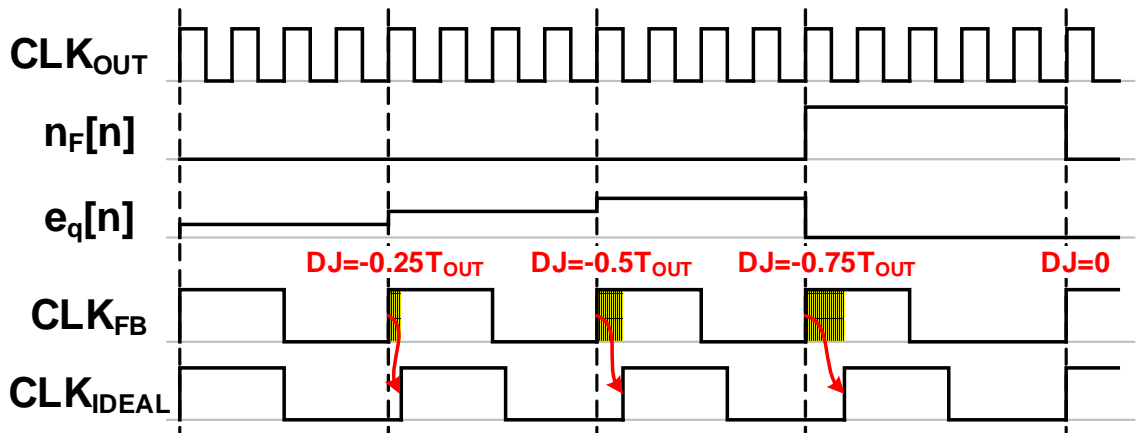
Figure 1.9: Timing diagrams illustrating the fractional divider operation.

In many applications, suppressing $e_q[n]$ by lowering the PLL bandwidth is undesirable, as it will increase the settling time and the VCO noise contribution. Because the fractional divider quantization noise is deterministic, conceptually it can be cancelled prior to the loop filter

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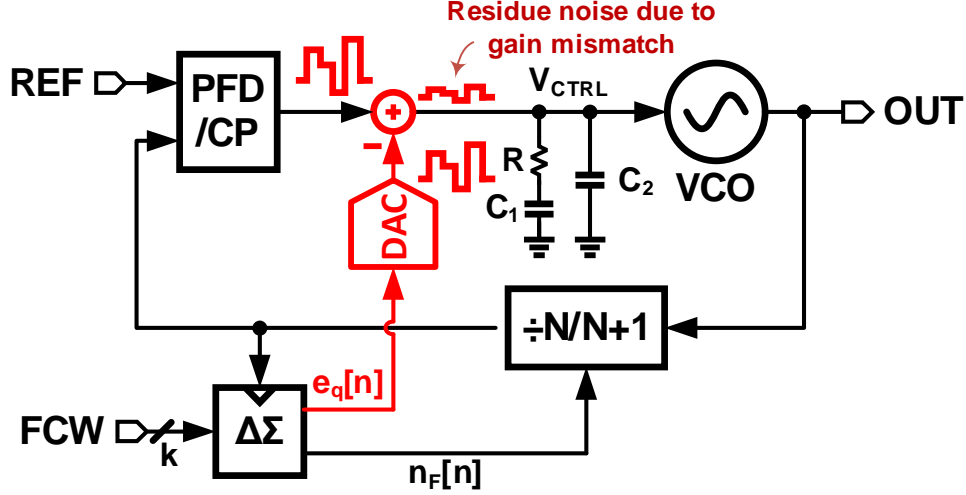
Figure 1.10: Simplified block diagram of analog FNPLL with QNC.

using a current DAC (see Fig. 1.10), thus eliminating the need for a narrow PLL bandwidth. The quantization noise cancellation (QNC) path extracts $\Delta\Sigma$ quantization error $e_q[n]$, then converts it into a current pulse of duration T_{DAC} and amplitude $-e_q[n] \times T_{VCO} \times I_{CP}/T_{DAC}$ for perfect QNC. However, in practice the gain of the DAC is never perfectly matched to the gain of the signal path through the PFD/CP as illustrated in Fig. 1.10. In [3], a sign-error least-mean-square (LMS) algorithm is used to adaptively calibrate the DAC gain to minimize the leaked quantization noise. Because of its high complexity and sensitivity to PVT variations, this technique does not provide an attractive solution.

1.2.3 Digital Fractional-N PLL

With the advancement of CMOS technology, the performance of digital circuits is improved in terms of speed, power, and area. On the other hand, analog blocks do not really benefit from process scaling and usually encounter several design issues. Conventional charge-pump PLLs will suffer from capacitor leakage, current mismatch, and limited dynamic range. Recently, significant research efforts have focused on developing digital FNPLLs that obviate the need for large capacitors. Due to their highly digital nature, loop dynamics are easier to reconfigure and they are also easier to port from one process generation to other. For complex SoCs, developing a low jitter reconfigurable digital/synthesizable FNPLL with minimum area

is highly desirable. However, like any mixed-signal feedback loop, the presence of an analog-to-digital and a digital-to-analog conversion, represented by the time-to-digital converter (TDC) and the digitally controlled oscillator (DCO) respectively, introduces quantization errors in the loop. As a result, jitter performance of digital FNPLLs, especially those using ring oscillators, is grossly inferior to their analog counterparts.

In this dissertation, we developed novel injection locking and quantization noise cancellation techniques to mitigate the impact of quantization errors of the fractional divider, TDC, and DCO. We also implemented highly-scalable, digitally-enhanced realizations of frequency synthesis and clocking modules that can leverage the advancement of CMOS technology to minimize the power consumption.

1.3   Dissertation Organization

The focus of this dissertation is on developing digital enhancement, injection locking, and noise cancellation techniques to realize low jitter, low power, fractional-N clocking schemes. The dissertation consists of seven chapters organized as follows:

Chapter 2 discusses the design of a low power LC digital FNPLL for wireless and wireline transceivers. It leverages a high resolution digital-to-time converter (DTC) to alleviate the TDC dynamic range requirements of conventional DPLLs. The proposed digital architecture uses a narrow range low-power time-amplifier based TDC (TA-TDC) with sub-1ps resolution to achieve wide PLL bandwidth and excellent jitter performance at a low power consumption.

Chapter 3 seeks to close the performance gap of ring-based PLLs compared to their LC counterparts, in order to leverage ring VCO merits of wide-range, multi-phases, and small area. The proposed digital FNPLL features a dual-path digital loop filter architecture to resolve the DAC quantization noise challenge, which is stressed by the large gain of ring VCOs. This maximizes the suppression of ring VCO phase noise. This chapter also discusses and analyzes the design details of a new, extended range, multi-modulus divider that enables seamless switching at the boundaries extension.

Chapter 4 presents a new multi-output clock generator architecture using open loop fractional dividers. The open loop architecture overcomes the bandwidth limitation in fractional-

N PLLs. It enables flexible per-core clocking in modern multi-core processors with instantaneous dynamic frequency scaling with no overshoots, and unrestricted spread spectrum modulation to satisfy different EMI requirements.

Injection-locked clock multipliers (ILCMs) provide many advantages in terms of phase noise, power, and area compared to classical PLLs, but they suffer from a narrow lock-in range and a high sensitivity to PVT variations especially at a large multiplication factor (N). In Chapter 5, the design and analysis of low-jitter LC-based ILCM with a digital frequency-tracking loop (FTL) is presented. It also introduces an accurate theoretical large-signal analysis for phase domain response (PDR) of ILCMs.

Chapter 6 seeks to extend the merits of ILCM to fractional-N and overcome its fundamental limitation to integer-N operation. The proposed architecture relies on DTC-based quantization noise cancellation (QNC) techniques to align the injected pulses to the oscillator's zero crossings, and hence ensures its phase locking. This chapter will discuss the means to realize rapid on/off operation, by which considerable energy saving is achieved by turning on the clock multiplier only when needed.

Finally, Chapter 7 concludes the discussion about the proposed design techniques, open loop fractional divider architecture, and rapid on/off injection locking clock multiplication architectures presented in this dissertation.

CHAPTER 2

LOW POWER LC-BASED DIGITAL FRACTIONAL-N PLL

2.1 Introduction

Fractional-N phase locked loops (FNPLLs) are key building blocks in many systems-on-chips (SoCs) and wireless transceivers [4–14]. FNPLLs offer flexibility in frequency planning using only a single-crystal reference clock and are therefore well-suited for realizing single-chip multi-standard solution in wireline applications. In all these applications, a wide PLL bandwidth is desirable as it helps improve both system- and circuit-level performance in multiple ways. For instance, it helps to improve jitter tolerance of wireline receivers [15, 16] and increase data modulation bandwidth and settling time in wireless transmitters [12, 14]. At circuit level, wide bandwidth results in: (a) larger suppression of oscillator phase noise, which helps to reduce the power, (b) better immunity to pulling [17], and (c) faster settling time. However, achieving low jitter (<1ps$_{\text{rms}}$) and wide bandwidth (2MHz - 5MHz) using less than 50MHz reference frequency is challenging mainly because of the presence of quantization error from feedback fractional divider and time-to-digital converter (TDC). For example, [11] suffers from degraded jitter performance when bandwidth is increased to 5MHz due to its band-bang phase detector (BBPD) quantization noise, while [10] relies on a high performance TDC with extensive calibration to achieve 3MHz bandwidth at the expense of large power and area.

Analog charge-pump PLL has been the most preferred architecture to implement fractional-N frequency generation. Using bandwidth extension techniques typically based on divider

quantization noise cancellation (QNC), analog PLLs were shown to achieve wide bandwidth, excellent jitter and spurious performance as reported in [12–15]. However, an analog PLL loop filter occupies large area and is difficult to reconfigure. To overcome these drawbacks, digital DPLLs that obviate the need for large capacitors have been proposed [4]. Due to their highly digital nature, loop dynamics are easier to reconfigure and they are also easier to port from one process generation to other.

A digital FNPLL is most commonly implemented using one of the two architectures depicted in Fig. 2.1. The main difference between the two architectures is in the way the phase error is calculated. In the so called *phase domain* PLL, the phase of the oscillator is determined by counting the number of zero-to-one output transitions while the reference phase is obtained by accumulating the frequency control word (FCW) on every rising edge of the synchronized reference clock [4]. A simple arithmetic logic determines the phase error by subtracting the oscillator phase from the reference phase. Because counter-based phase detection provides an estimate of the phase only with an accuracy of one oscillator period, a high resolution TDC is used to measure the residual phase error. In the architecture shown in Fig. 2.1(b), the feedback divider implicitly accumulates the oscillator phase and the phase error between the reference clock and the divider output is determined by using a TDC [5]. In both the architectures, a high performance TDC with sub-ps resolution and at least one oscillator period measurement range is needed. Hence, we refer to both of them as TDC-based digital FNPLLs.

Recently, digital-to-time converter (DTC)-based digital FNPLLs were proposed to ease the resolution requirements of the TDC [9, 18]. Based on the assumption that a high resolution DTC can be designed more power efficiently and with less hardware complexity compared to a TDC, a high resolution DTC is cascaded with a bang-bang phase detector (BBPD) to implement a digital FNPLL that behaves more over like an integer-N PLL [9]. However, BBPD, digitally controlled oscillator (DCO), and fractional divider introduce quantization errors at different points in the loop and their contribution to output phase noise increases with the loop bandwidth. Hence, a wide bandwidth PLL requires higher resolution TDC along with quantization noise cancellation techniques to mitigate fractional divider quantization noise, as described in Section 2.2. In other words, digital FNPLLs suffer from conflicting band-
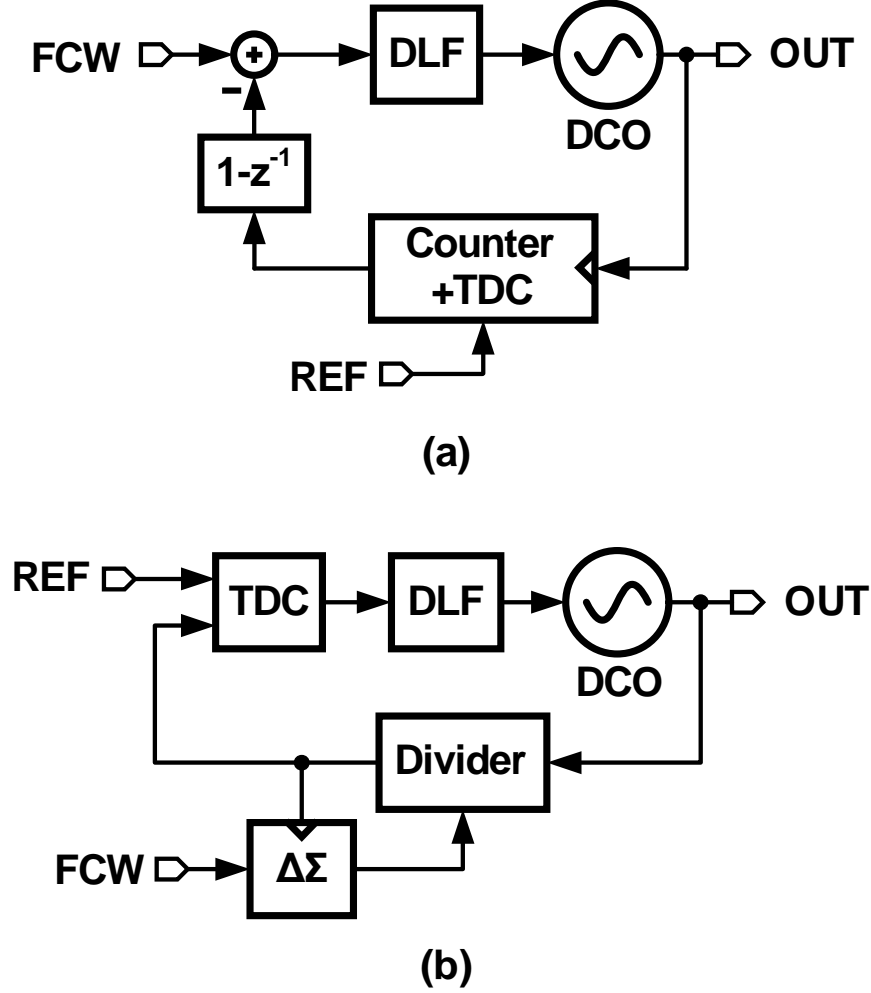
Figure 2.1: Block diagram of conventional digital FNPLL implementation using (a) counter-based divider-less architecture, and (b) $\Delta\Sigma$ fractional divider.

width requirements imposed by oscillator phase noise and the quantization error introduced by the TDC and fractional divider.

In this chapter, we present digital enhancement techniques to increase the bandwidth of DTC-FNPLLs [19]. Using a high resolution low-power time-amplifier (TA) based TDC (TA-TDC) in combination with a DTC, the FNPLL achieves an in-band noise of -106dBc/Hz and integrated jitter of 490fs$_{rms}$ at 4.5GHz output frequency and has a bandwidth higher than 3MHz ($F_{REF}/16$). The entire PLL consumes 3.7mW from 1V supply and achieves an FoM of -240.5dB.

The rest of the chapter is organized as follows. After a brief overview of state-of-the-art digital FNPLLs in section 2.2, the proposed architecture is presented in section 2.3. The

circuit implementation of critical building blocks is illustrated next in section 2.4. The measured results from the test chip are shown in section 2.5. Finally, the key contributions of this chapter are summarized in section 2.6.

2.2 TDC- and DTC-based Digital Fractional-N PLLs

A TDC-based digital FNPLL is obtained from a conventional charge-pump FNPLL by replacing the phase detector/charge-pump, analog loop filter, and VCO by TDC, digital loop filter, and DCO, respectively (see Fig. 2.1(b)). The TDC acts as a digital phase detector and its output is filtered by a digital loop filter and then used to control the DCO. Fractional-N operation is achieved by dithering the multi-modulus divider using a delta-sigma ($\Delta\Sigma$) modulator. The most challenging aspect of designing a low noise, wide bandwidth, low power digital FNPLL is the design of a wide dynamic range, high resolution TDC. The dynamic range of the TDC must be large enough to measure the time difference between the reference clock and the dithered feedback clock. Consequently, the TDC range must be at least one DCO period when the fractional divider is dithered by a first order $\Delta\Sigma$ modulator and several DCO periods for higher order modulators.
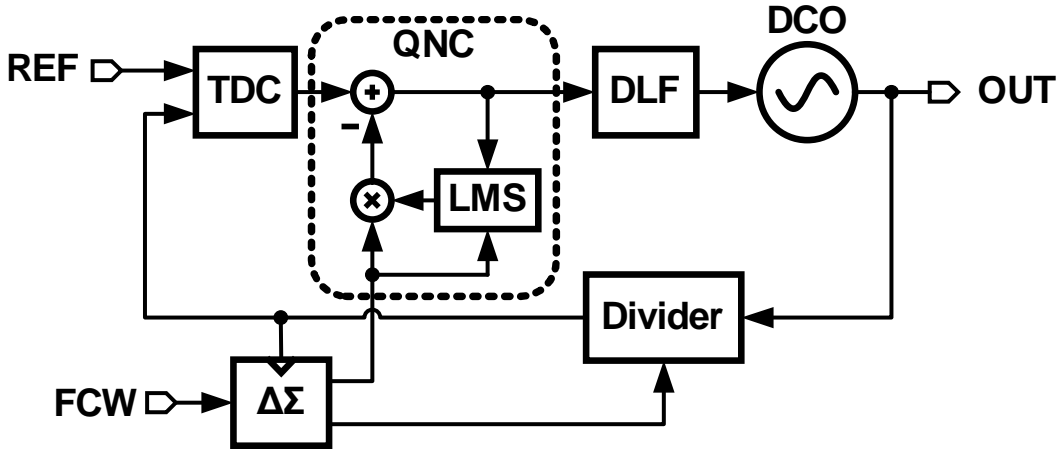
Figure 2.2: Digital FNPLL architecture with $\Delta\Sigma$ quantization noise cancellation (QNC).

Because TDC quantization noise is low-pass filtered by the PLL's feedback loop, it limits in-band phase noise of the PLL. For instance, achieving -110dBc/Hz in-band phase noise of a

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4GHz PLL operating with 40MHz reference requires the TDC resolution to be less than 3ps. Assuming second order $\Delta\Sigma$ modulator in the fractional divider, the TDC has to cover at least 2 DCO periods ($\backsim$500ps), which is very difficult to achieve in practice. Additionally, nonlinearity of the TDC further exacerbates in-band noise by folding the shaped quantization noise of the $\Delta\Sigma$ divider [7]. It is also shown to introduce in-band fractional spurs that are difficult to predict and hence are difficult to suppress. The detrimental impact of TDC quantization error on in-band noise and fractional spurs increases at wider PLL bandwidth, which puts even more stringent requirements on the TDC.

The $\Delta\Sigma$ fractional divider quantization noise, E_Q, impacts both analog and digital PLLs alike. Because E_Q is low-pass filtered by the PLL feedback loop, it can only be suppressed by lowering the PLL bandwidth, which is undesirable in many applications. As a result, several bandwidth extension techniques based on quantization noise cancellation (QNC) were proposed for both analog [12, 13, 20] and digital PLLs [5]. A digital QNC scheme, shown in Fig. 2.2, seeks to cancel E_Q by extracting the $\Delta\Sigma$ quantization error, scaling it with a calibrated gain and subtracting it from the TDC output [5]. The digital implementation makes this technique insensitive to analog inaccuracies and PVT variations present in analog charge-pump PLLs. However, cancelling divider quantization noise after the TDC requires a high-performance wide-range TDC. Hence, high performance TDC is critical to the implementation of low noise wide bandwidth digital FNPLLs. Consequently, over the past decade, significant research efforts have focused on the design of wide dynamic range, high resolution, and highly linear TDCs. Several architectures have been proposed that mimic the operation of ADCs: flash (delay line [4], vernier lines [8], parallel delay lines [7]), two-step [21], pipelined [22], and noise shaped [5, 23]. Most of these techniques adopt analog-intensive design approaches with complex calibration schemes to achieve sub-gate delay resolution. As a result, they occupy large area and consume high power.

A DTC-based digital FNPLL shown in Fig. 2.3 was proposed as a power efficient alternative to TDC-based FNPLLs [7, 9, 24]. The DTC in the feedback path is used to cancel the $\Delta\Sigma$ quantization noise at the output of the fractional divider. As a result, the TDC dynamic range requirement is relaxed. For instance, in [7], 4-bit DTC is implemented using 16-stage delay locked loop and a phase selection multiplexor to reduce E_Q by 1/16 and
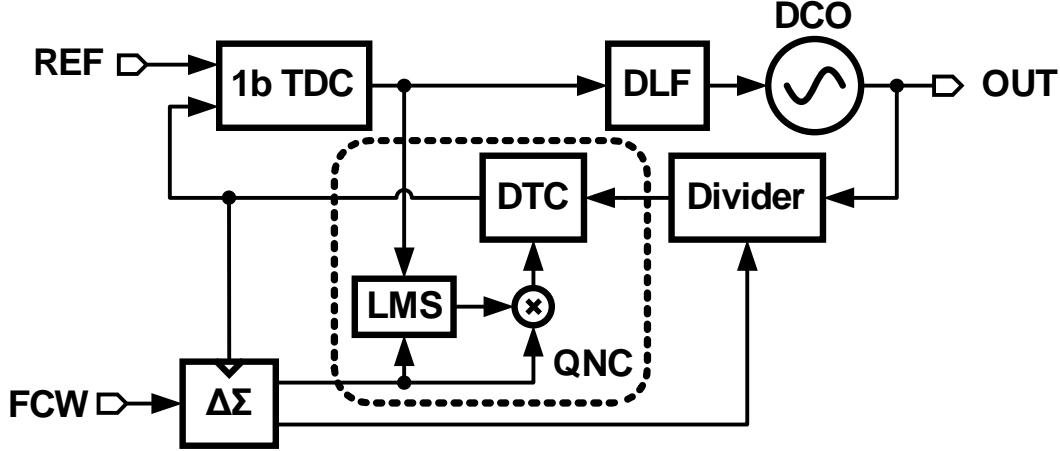
Figure 2.3: A DTC-based bang-bang phase detector (BBPD) digital FNPLL implementation.

consequently relax the TDC requirements to 4-bit. However, the non-linearity of the DTC caused by mismatch between delay cells and routing paths severely degrades the spurious and in-band noise performance of the PLL. To mitigate these non-linear errors, complex background non-linearity calibration techniques such as those reported in [7] were employed at the expense of large area, high power, and long settling time. To overcome these drawbacks, a 10-bit DTC implemented using a digitally controlled delay line (DCDL) whose gain is accurately calibrated using a least-mean square (LMS) technique to implement a truly fractional divider was proposed in [9]. The high resolution DTC limits the input range of TDC to within the random noise range, as the reference and feedback clocks are now aligned as in the case of an integer-N PLL. Consequently, the wide range requirement of the TDC is alleviated and a simple 1-bit TDC or bang-bang phase detector (BBPD) is adequate [9].

A BBPD can be implemented power efficiently using a single flip-flop (FF). However, its large quantization error and grossly non-linear behavior limit its use in wide bandwidth PLLs. In [25], the non-linear dynamics of second-order BB-PLL are analyzed to find the condition for loop stability. The behavior of BB-PLLs is a strong function of loop gain and delay. If the loop gain is made large to achieve wide bandwidth, the steady-state of the BB-PLL becomes a bounded limit cycle, which manifests as undesirable fractional spurs and large peaking in the phase noise [26]. If the loop gain is reduced, BBPD operates in a random-noise limited regime and the PLL exhibits linear response. In [26], it was illustrated that there is optimal

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loop gain and consequently loop bandwidth that minimizes the PLL's overall noise. This optimum noise performance is usually achieved at relatively low PLL bandwidth (312kHz in [9]). Furthermore, the gain of BBPD operating in noise-limited regime depends on the noise at its input, which not only makes the loop dynamics difficult to control but also makes the PLL bandwidth sensitive to reference clock jitter [25].

In addition to the BBPD-related issues, the non-idealities of the DTC also have significant impact on the performance of the FNPLL. The integral non-linearity (INL) of the DTC causes imperfect QNC and appears as a periodic error at the BBPD input. If the magnitude of DTC INL is larger than random noise, it reduces BBPD gain and leads to an increase in the in-band phase noise and generation of spurious tones [24]. Finally, the architecture in [9] also suffers from long settling time for DTC gain calibration, as 1-bit is used only in LMS correlation. In view of these drawbacks, we propose a digital fractional-N PLL architecture that employs a narrow range high resolution TDC in addition to a truly fractional divider to achieve low jitter, wide bandwidth, and low power consumption.

2.3   Proposed Wide-Bandwidth Digital FNPLL Architecture

The block diagram of the proposed fractional-N PLL is shown in Fig. 2.4. It employs the proposed narrow range high resolution TA-TDC along with a DTC-based fractional divider, a programmable digital loop filter, and LC-based DCO. The TDC detects the phase difference between the reference and feedback clocks with a resolution of 1ps and drives 4-bit digital output into a programmable digital loop filter. The filtered TDC output controls the DCO and drives it toward frequency/phase lock. The true fractional divider, implemented using a multi-modulus divider (MMD) and a DTC, generates the feedback clock input to the TDC. Because DTC alleviates the dynamic range requirement of TDC, it is designed only to have large enough range ($\pm$8ps) to cover jitter in the reference and feedback clocks and the non-zero DTC INL. Leveraging time amplification techniques, sub 1ps resolution is achieved at low power consumption [19]. The circuit implementation details of the proposed TA-TDC are provided in section 2.4.1.

By using a TA-TDC in place of a BBPD, the proposed digital FNPLL overcomes the

drawbacks of [9] discussed earlier. First, the limit cycle behavior that usually plagues BB-PLLs is greatly suppressed by the TA-TDC. Because instantaneous time difference between the reference clock and DCO output caused by random noise is larger than TA-TDC step size, the TA-TDC's transfer characteristic is linearized and the DCO control is also scrambled. As the TA-TDC range is designed to be larger than noise-induced input time difference at any moment, even a large loop gain does not saturate the TA-TDC. As a result of its linear behavior, the TA-TDC eliminates the limit cycle behavior across a wide range of loop gain (and bandwidth) settings. In other words, TA-TDC extends the random-noise limited regime of BB-PLLs by nearly the time-amplifier gain (K_{TA}). Second, low quantization error of the TA-TDC leads to lower in-band phase noise compared to a BB-PLL. Alternatively, for the same in-band phase noise, PLL bandwidth can be extended, which relaxes DCO phase noise requirements. Third, the proposed architecture is less susceptible to DTC INL as long as it does not saturate the TA-TDC. Transistor-level simulations of the DTC show that its INL (<3ps) can be managed to be less than TA-TDC range of ± 8ps relatively easily. Fourth, because gain of the TA-TDC is independent of reference clock jitter, the proposed architecture exhibits well-controlled loop dynamics. Finally, TA-TDC improves settling and tracking behavior of the PLL by preventing slewing across a larger input time difference compared to a BBPD.

2.3.1 DTC-based Fractional Divider

A fractional divider is realized by dithering the frequency divider between integer values using a $\Delta\Sigma$ modulator. The truncation error of the $\Delta\Sigma$ modulator appears as phase quantization error, Φ_{E_q}, at the output of the divider, which can be computed by subtracting the output of the $\Delta\Sigma$ from its input and accumulating it to account for the phase integration in the divider. The magnitude of Φ_{E_q} depends on the order of $\Delta\Sigma$ modulator. It can be as large as one DCO period (T_{DCO}) in case of first order $\Delta\Sigma$ modulator and several DCO periods for higher order modulators.

Phase quantization error can be cancelled at the output of MMD in time domain, which obviates the need for a high resolution TDC [9]. This can be implemented by feeding properly
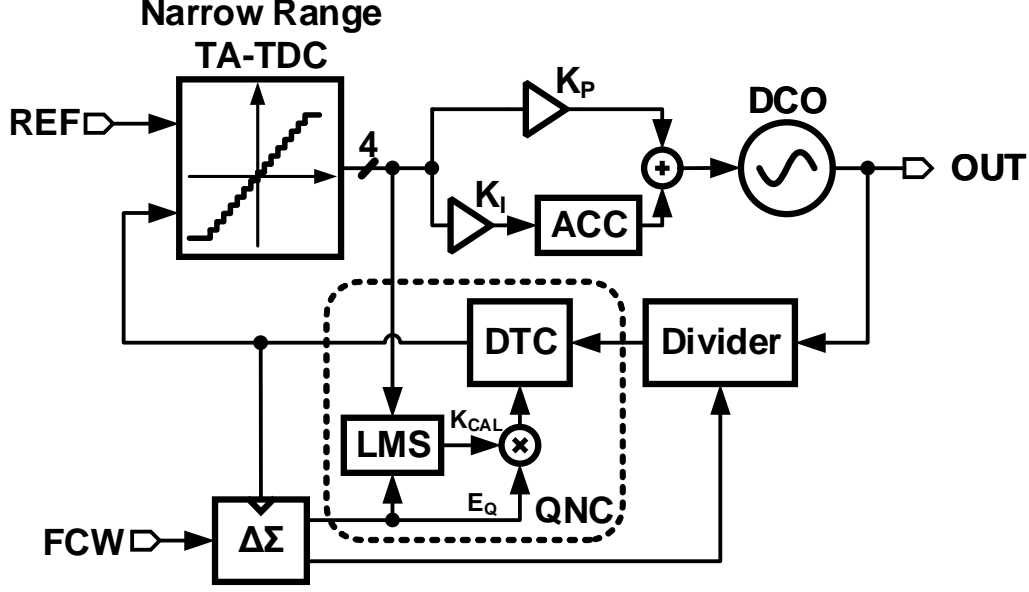
Figure 2.4: Block diagram of the proposed digital FNPLL.

scaled E_Q into a DTC, as shown in Fig. 2.4. The DTC performs digital-to-time conversion and subtracts quantization error from the MMD output. As a result, this approach does not suffer from path mismatches present in analog PLLs QNC techniques [12], and is hence employed in our implementation. A key consideration in the design of DTC-based cancellation approach is the gain accuracy and non-linearity of the DTC, both of which cause quantization error leakage and degrade the spurious and noise performance of the PLL.

A DTC can be implemented using either a phase interpolator (PI) or digitally controlled delay line (DCDL). A PI-based implementation has the advantage of well defined gain but suffers from poor linearity [7, 24]. Complex digital calibration techniques are needed to correct for PI non-linearity, which often incur large power and area penalties [7]. On the other hand, DCDL-based DTC can achieve very fine resolution (< 0.5ps) but its gain is not well defined and sensitive to process, voltage, and temperature (PVT) variations [9, 27]. Because of its scaling friendly properties, a DCDL-based DTC is employed in our implementation. Digital background calibration is used to accurately set the DTC gain independently of PVT variations and DCO output frequency.

The DTC gain scaling factor K_{CAL} is computed in a background manner using a least mean square (LMS) algorithm [9]. Based on the observation that any residual phase quan-

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tization error due to imperfect cancellation appears at the TDC output, DTC gain error can be estimated digitally by correlating $E_q[k]$ with TDC output as shown in Fig. 2.4. The accumulated digital correlator output, after scaling by LMS algorithm step-size μ_{LMS}, provides K_{CAL}. By scaling $E_q[k]$ by K_{CAL} prior to controlling the DTC, its input range is scaled such that its output range is equal to T_{DCO} [9]. Once the quantization error is completely cancelled, the correlation becomes zero and the accumulator output equals the optimal K_{CAL} value. The LMS step-size μ_{LMS} must be carefully chosen considering the tradeoff between convergence time and K_{CAL} accuracy [28]. A large μ_{LMS} leads to faster convergence at the expense of larger noise in the steady-state value of K_{CAL}. The convergence time is improved by more than an order of magnitude because of the extra error information provided by the TA-TDC.

2.3.2   Digital FNPLL System Analysis

Fig. 2.5 shows the discrete-time phase-domain linear model of the digital FNPLL. The DCO is modeled as an integrator in z-domain with gain $2\pi K_F T_R$, where K_F [Hz/LSB] is the DCO gain and $T_R = 1/F_{REF}$ is the reference period [29]. The fractional divider effectively divides the DCO phase Φ_{OUT} by its nominal division factor $N = N_{int} + \alpha$, where N_{int} and α are the integer and fractional division parts, respectively, as modeled in [30]. The output of the $\Delta\Sigma$ modulator has two more components: zero-mean signal ($s_{DS}[k]$), and zero-mean quantization noise ($q_{DS}[k]$). The divider control is modeled as an accumulator with 2π gain factor to account for the frequency-to-phase conversion. The divider output phase Φ_{DIV} is equal to the DCO phase divided by the nominal division factor (N) after subtracting the phase due to modulus control.

The DTC delays the feedback clock by $DCW[k] \times K_{DTC}$, where K_{DTC} [s/LSB] is the DTC gain and $DCW[k]$ is the DTC delay control word. So DTC can be modeled as a combination of summing block and a gain $2\pi K_{DTC}/T_R$. The function of TA-TDC is modeled as a gain factor of $T_R/2\pi$ to account for phase-to-time conversion followed by a gain K_{TA}/t_{del}, where K_{TA} is the gain of the time-amplifier and t_{del} [s] is the resolution of the delay-line TDC. Finally, the loop filter is modeled by its discrete-time transfer function H(z), and the loop
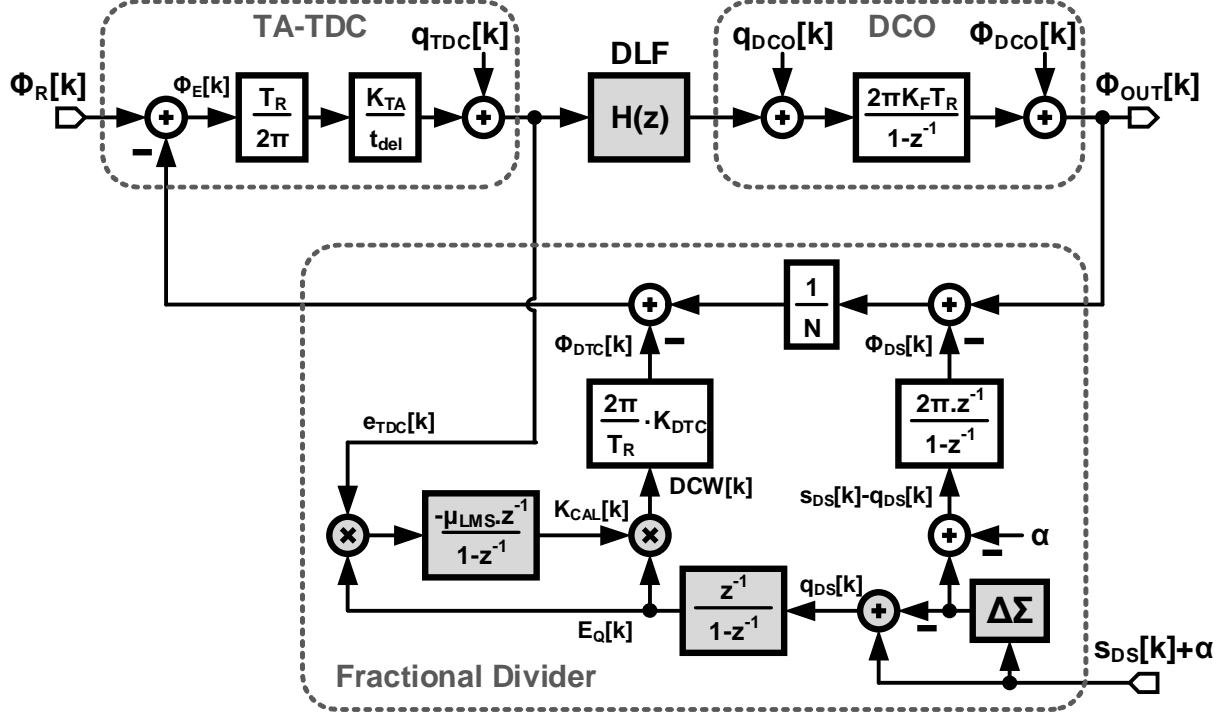
Figure 2.5: Simplified discrete-time linear phase-domain model of the FNPLL.

gain transfer function can be defined as:

$$LG(z) = \frac{T_R^2 \, K_{TA} \, K_F}{N \, t_{del}} \cdot \frac{H(z)}{1 - z^{-1}} \tag{2.1}$$

This linear model is used for stability and noise analysis of the FNPLL system. All of the noise sources in the digital FNPLL, namely the reference phase noise, TDC quantization error, DCO frequency quantization error, and DCO phase noise are represented by their respective power spectral densities $S_{\Phi_{REF}}$, $S_{q_{TDC}}$, $S_{q_{DCO}}$, and $S_{\Phi_{DCO}}$. The total output phase noise $S_{\Phi_{OUT}}$ can be calculated using:

$$S_{\Phi_{OUT}} = \left| \frac{2\pi \, t_{del}}{T_R \, K_{TA}} \cdot N \cdot G(z) \right|^2 S_{q_{TDC}} + \left| \frac{2\pi \, K_F \, T_R(1 - G(z))}{1 - z^{-1}} \right|^2 S_{q_{DCO}}$$
$$+ \left| N \cdot G(z) \right|^2 S_{\Phi_{REF}} + \left| 1 - G(z) \right|^2 S_{\Phi_{DCO}} \tag{2.2}$$

where $G(z) = LG(z) / (1 + LG(z))$. Assuming uniform distribution for the quantization error, it can be easily shown that $S_{q_{TDC}} = T_R/12$ [LSB^2/Hz]. Equation (2.2) shows that the in-

band phase noise (IBPN) is dominated by reference and TDC noise. This emphasizes the benefit of adding the time-amplifier in order to suppress the TDC quantization noise by its gain factor K_{TA}.

Fractional divider quantization error $q_{DS}[k]$ is cancelled using DTC in the feedback path. The LMS algorithm is used to determine the optimal K_{CAL} that minimizes the mean square value of $\Phi_E[k]$ (or equivalently $e_{TDC}[k]$). When the PLL is locked, the output phase Φ_{OUT} is given by:

$$\Phi_{OUT} = (N_{int} + \alpha) \cdot \Phi_R = N \cdot \Phi_R \tag{2.3}$$

Then we can write $\Phi_E[k] = \Phi_{DS}[k]/N + \Phi_{DTC}[k]$ as a function of $E_Q[k]$ and $S[k]$, where $E_Q[k]$ is the integration of $\Delta\Sigma$ quantization error $q_{DS}[k]$ and $S[k]$ is the integration of the $\Delta\Sigma$ modulator input signal $s_{DS}[k]$. Therefore $\Phi_E[k]$ is given by:

$$\Phi_E[k] = \frac{2\pi}{N}\left(S[k] - E_Q[k]\right) + \frac{2\pi\,K_{DTC}}{T_R} \cdot K_{CAL}[k]\,E_Q[k] \tag{2.4}$$

Since output period $T_{DCO} = T_R/N$ and $e_{TDC}[k] = \Phi_E[k] \cdot K_{TDC}\,T_R/(2\pi)$, where $K_{TDC} = K_{TA}/t_{del}$ is the effective TDC gain, then the TDC output is equal to:

$$e_{TDC}[k] = T_{DCO}\,K_{TDC}\,S[k] - (T_{DCO} - K_{DTC}\,K_{CAL}[k]) \cdot K_{TDC}\,E_Q[k] \tag{2.5}$$

This means the optimum K_{CAL} is equal to T_{DCO}/K_{DTC}. Based on the analysis in [28], the recursive equation of LMS algorithm is used for convergence analysis as follows:

$$K_{CAL}[k+1] = K_{CAL}[k] - \mu_{LMS}\,E_Q[k]\,e_{TDC}[k] \tag{2.6}$$

By substituting (2.5) into (2.6), we get:

$$K_{CAL}[k+1] = K_{CAL}[k]\left(1 - \mu_{LMS}K_{TDC}K_{DTC}E_Q^2[k]\right) + \mu_{LMS}K_{TDC}T_{DCO}\left(E_Q^2[k] - E_Q[k]S[k]\right) \tag{2.7}$$

Assuming $K_{CAL}[k]$ and $E_Q[k]$ are independent, then the expectation $E\left\{K_{CAL}[k]\,E_Q^2[k]\right\} = E\left\{K_{CAL}[k]\right\} \cdot E\left\{E_Q^2[k]\right\}$, where $E\left\{E_Q^2[k]\right\}$ is the variance σ_{EQ}^2 of $E_Q[k]$. Since $E_Q[k]$ and $S[k]$

are uncorrelated, then $\mathrm{E}\left\{\mathrm{E_Q}[k]\,\mathrm{S}[k]\right\} = 0$ and the expectation $\mathrm{E}\left\{\mathrm{K_{CAL}}[k+1]\right\}$ is given by:

$$\mathrm{E}\left\{\mathrm{K_{CAL}}[k+1]\right\} = \mathrm{E}\left\{\mathrm{K_{CAL}}[k]\right\}\left(1 - \mu_{\mathrm{LMS}}\,\mathrm{K_{TDC}}\,\mathrm{K_{DTC}}\,\sigma_{\mathrm{EQ}}^2\right) + \mu_{\mathrm{LMS}}\,\mathrm{K_{TDC}}\,\mathrm{T_{DCO}}\,\sigma_{\mathrm{EQ}}^2 \quad (2.8)$$

So the solution will be in the form of $\mathrm{K_{CAL}}[k+1] = \mathrm{K_{CAL}}[0] \cdot \left(1 - \mu_{\mathrm{LMS}}\,\mathrm{K_{TDC}}\,\mathrm{K_{DTC}}\,\sigma_{\mathrm{EQ}}^2\right)^{k}$, which means to guarantee loop stability μ_{LMS} has to satisfy $0 < \mu_{\mathrm{LMS}}\,\mathrm{K_{TDC}}\,\mathrm{K_{DTC}}\,\sigma_{\mathrm{EQ}}^2 < 2$.

2.3.3 Performance Comparison

Time-domain mixed-signal simulations were performed to compare the performances of the proposed TA-TDC- and BBPD-based PLLs. In all the simulations reference clock frequency is equal to 50MHz and output frequency is 5.01GHz. The phase noise of the reference clock and the DCO at 1MHz offset are -150dBc/Hz and -107dBc/Hz, respectively. The simulated output phase noise plots of the BB-PLL with a bandwidth of 2MHz and 4MHz are shown in Fig. 2.6(a). Peaking in the phase noise plot caused by limit cycle behavior is clearly visible and as expected is more pronounced in the wider bandwidth case. The simulated output phase noise plots of the proposed PLL for two different bandwidth conditions are shown in Fig. 2.6(b). Because of its linear loop dynamics, no peaking was observed and the integrated jitter is about 0.45ps$_{\mathrm{rms}}$ and 0.58ps$_{\mathrm{rms}}$ for a bandwidth of 2MHz and 4MHz, respectively. At 4MHz bandwidth condition, this represents an improvement of more than $2\times$ compared to the BB-PLL.

Sensitivity of loop bandwidth to reference clock jitter is quantified by plotting the output phase noise for two different clock jitter conditions (see Fig. 2.7). Because BBPD gain is inversely proportional to input jitter, loop gain and hence the loop bandwidth reduces from 2MHz to about 0.5MHz when the input jitter is increased from 0.8ps$_{\mathrm{rms}}$ to 3.2ps$_{\mathrm{rms}}$. On the other hand, the gain of the TA-TDC is independent of input jitter and as a result the bandwidth remains almost constant even when the reference clock jitter is varied.

The settling behavior of the proposed PLL is compared to the BB-PLL in Fig. 2.8. Shown on the top is the settling of DCO control word when the PLLs are started with an initial phase offset of 750ps. As the phase error accumulates beyond the random noise limited

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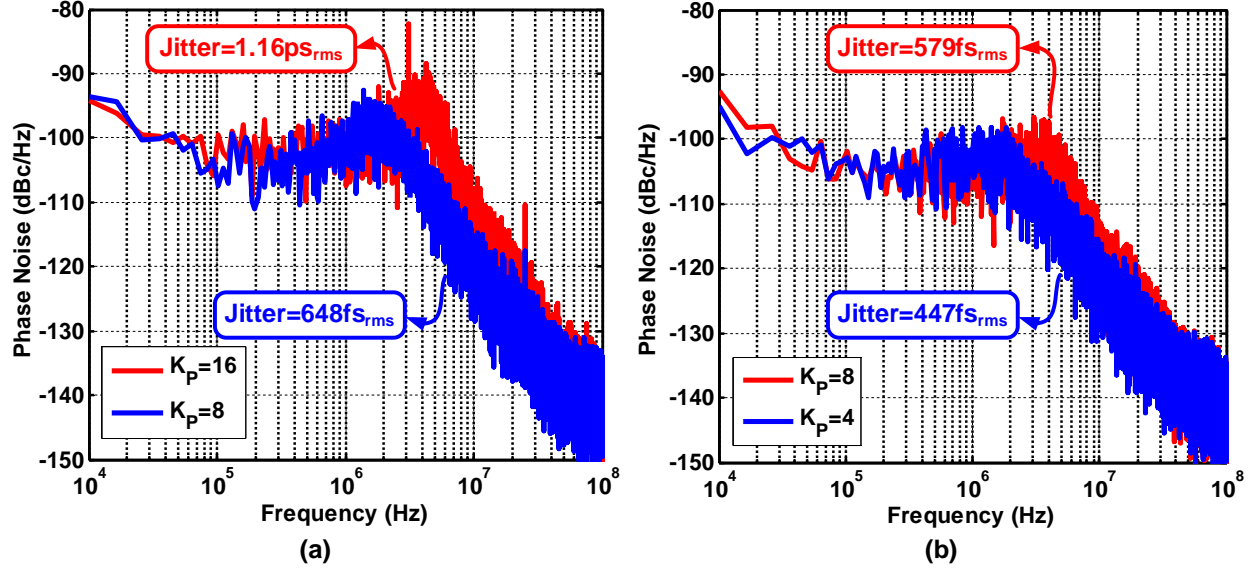
Figure 2.6: Simulated output phase-noise spectrum, 5.003GHz output using 50MHz reference, with different proportional gain settings for (a) conventional BBPD, and (b) proposed narrow range TA-TDC.
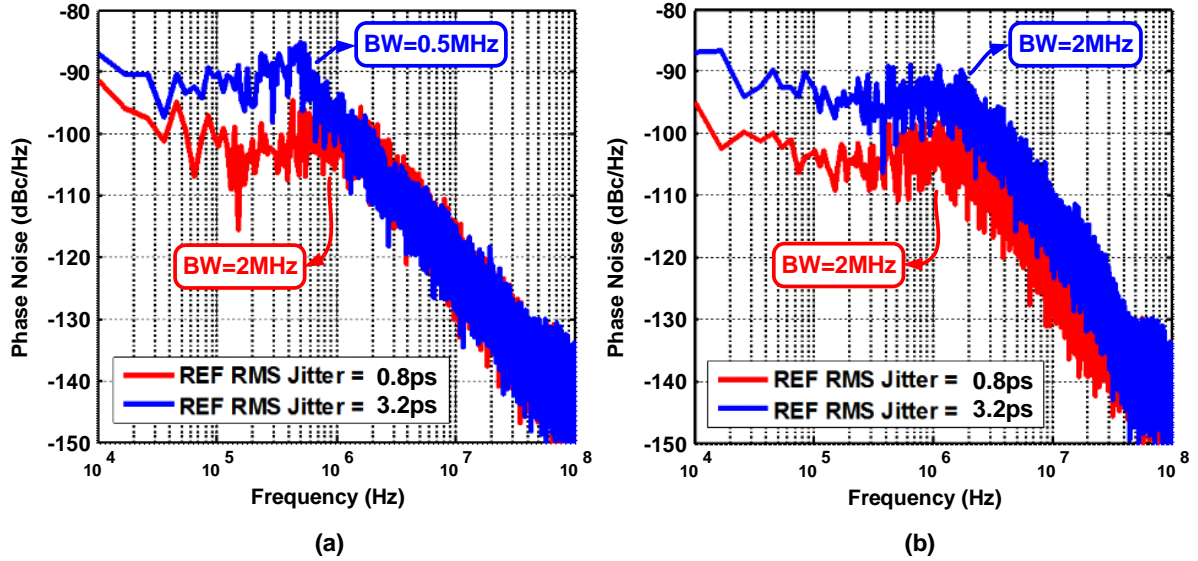
Figure 2.7: Simulated output phase-noise spectrum, 5.003GHz output using 50MHz reference, with different reference noise jitter for (a) conventional BBPD, and (b) proposed narrow range TA-TDC.

regime, the BBPD slews, which greatly increases the settling time. On the other hand, the proposed PLL achieves lock in much less time due to the higher gain and wider range of the TA-TDC. Using the output of the TA-TDC in LMS DTC gain calibration loop improves the

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convergence time, compared to BBPD. As shown in Fig. 2.8, K_{DTC} settles in about $270\mu s$ in case of BBPD which reduces to about $38\mu s$ when the TA-TDC is employed. In both cases, the LMS step-size parameter μ_{LMS} is set to achieve the same mean squared error in K_{CAL}. This speed improvement is attributed to the improved LMS correlation process using multi-bit error signal.
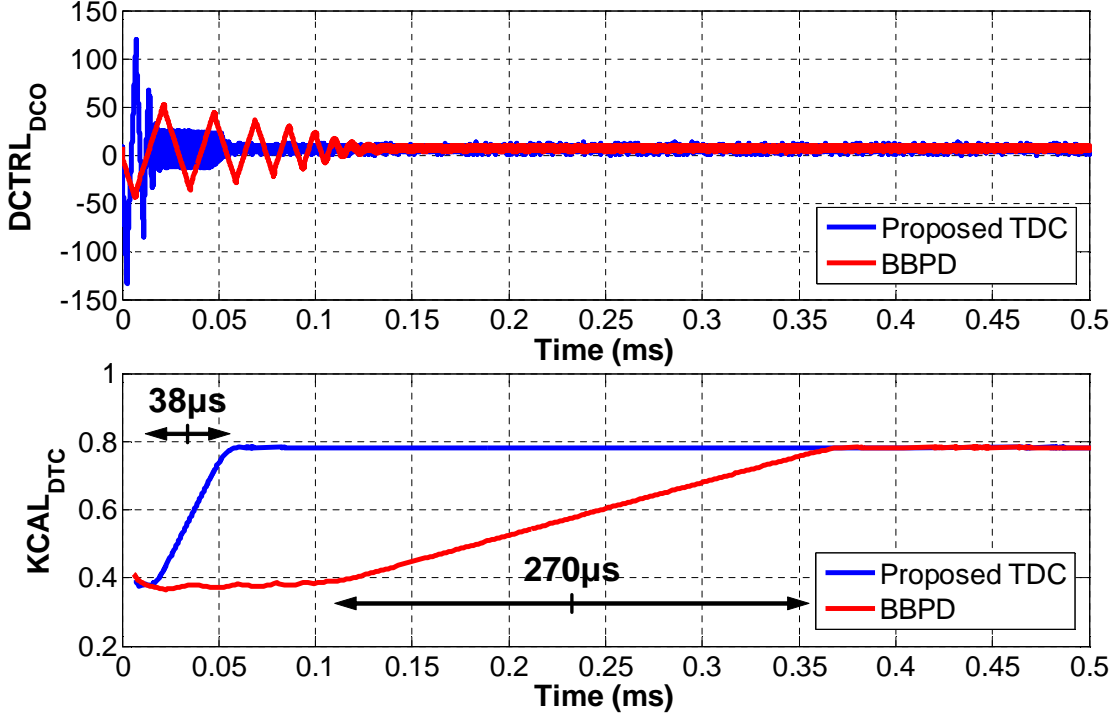
Figure 2.8: Simulated settling behavior of (a) DCO control word and, (b) DTC calibration factor.

2.4 Building Blocks

2.4.1 TA-TDC

Time amplification provides an attractive alternative to implement high resolution TDCs [21,31]. Similar to a voltage amplifier in pipelined ADCs, time-amplifier (TA) amplifies the time residue to enhance the resolution of pipelined TDCs. For instance, TA is employed in a two-step TDC in [21] and a sub-exponent TDC in [31]. However, the requirement for

accurate amplification gain (K_{TA}) in these architectures limits their practical usage in a high performance fractional-N PLL. In view of this, we propose a one-step TA-based TDC whose performance does not directly depend on K_{TA}.
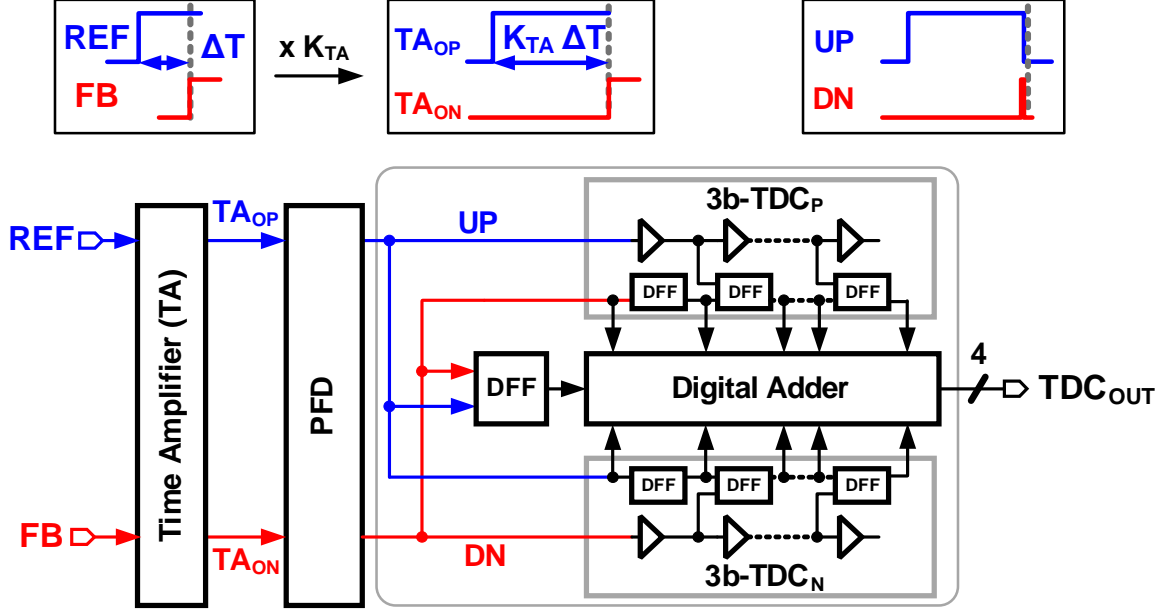
Figure 2.9: Bock diagram of the proposed narrow range time-amplifier based TDC.

The block diagram of the proposed narrow range high resolution TDC is shown in Fig. 2.9. It consists of a time-amplifier (TA) that amplifies the input time difference by a gain of K_{TA} and a conventional flash TDC that digitizes the TA output into 4 bits. The flash TDC is implemented using a 3-state phase frequency detector (PFD) followed by a 4-bit delay line based TDC that quantizes the phase difference between the UP and DN outputs of the PFD with a resolution of one inverter delay t_{del}. Because minimum inverter delay is about 12 to 15ps in 65nm CMSOS technology, K_{TA} must be equal to 16 to achieve 1ps resolution for the entire TA-TDC. With 4-bit output the linear range of the TA-TDC is equal to ± 8ps.

The TA shown in Fig. 2.10 is similar to the 2$\times$ gain stage reported in [31]. This fully-symmetric architecture consists of cross-coupled inverters wherein each inverter has two pull-down paths (main and dependent) to discharge the output node. Early input makes the late input of the cross-coupled inverters slower by reducing the strength of the dependent path, resulting in an amplified time difference. The strength of the dependent path is made programmable to achieve gain ranging from 1$\times$ to 16$\times$ using the 5-bit input control
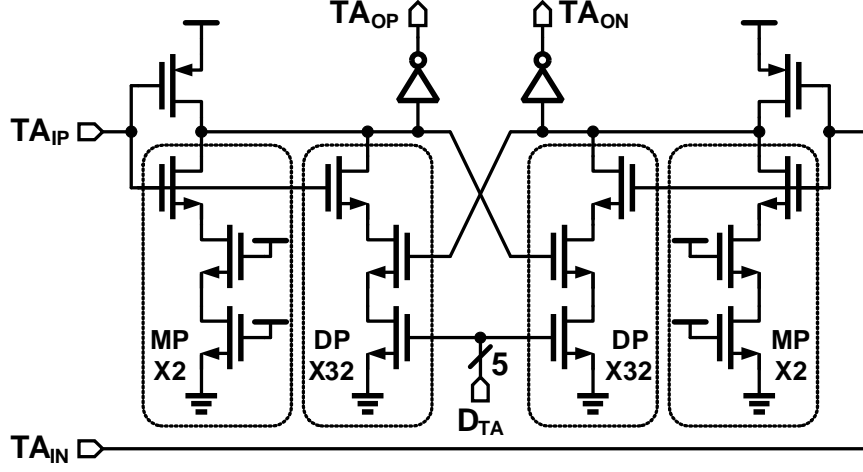
Figure 2.10: Schematic of the proposed fully-symmetric time-amplifier (TA).

word, D_{TA}. The linear input range of the TA is determined by the fall time of cross-coupled inverters and can be easily designed to achieve higher than ± 50ps linear input range. However, increased linear range comes at the expense of more noise. Post-layout phase noise simulations of the TA indicate a noise floor better than -160dBc/Hz at 50MHz reference clock. Transient noise simulation shows less than 10fs$_{rms}$ input-referred jitter. Monte-Carlo post-layout simulation results show the standard deviation of the input referred time offset is around 0.75ps. Beyond the linear range, the TA gain will drop gradually to reach unity, as the dependent path will be switched-on during transition. As a result, the TA will function as a buffer during the PLL settling process and will not impact the operation.

A 4-bit TDC is implemented using delay line TDC architecture [4]. The TDC is designed to have fully-symmetric characteristics with zero input referred time offset. Two identical 3-bit TDCs, TDC_P and TDC_N, digitize $T_{UP} - T_{DN}$ and $T_{DN} - T_{UP}$, respectively. The difference between TDC_P and TDC_N outputs yields the magnitude of the input time difference, while a separate BBPD determines the sign. The final TA-TDC output ranges from -7.5 to +7.5 with a step size of 1, which allows the PLL to lock without phase offset. This will assure that TA operates in the center of its linear range in steady state. Each of the 3-bit TDCs is implemented using a conventional 7-stage inverter-based delay line in addition to 7 BBPDs as time quantizers. The TDC resolution is equal to one inverter delay, which is about 15ps in 65nm technology. TDC nonlinearity is reduced by making rise/fall times small and matching

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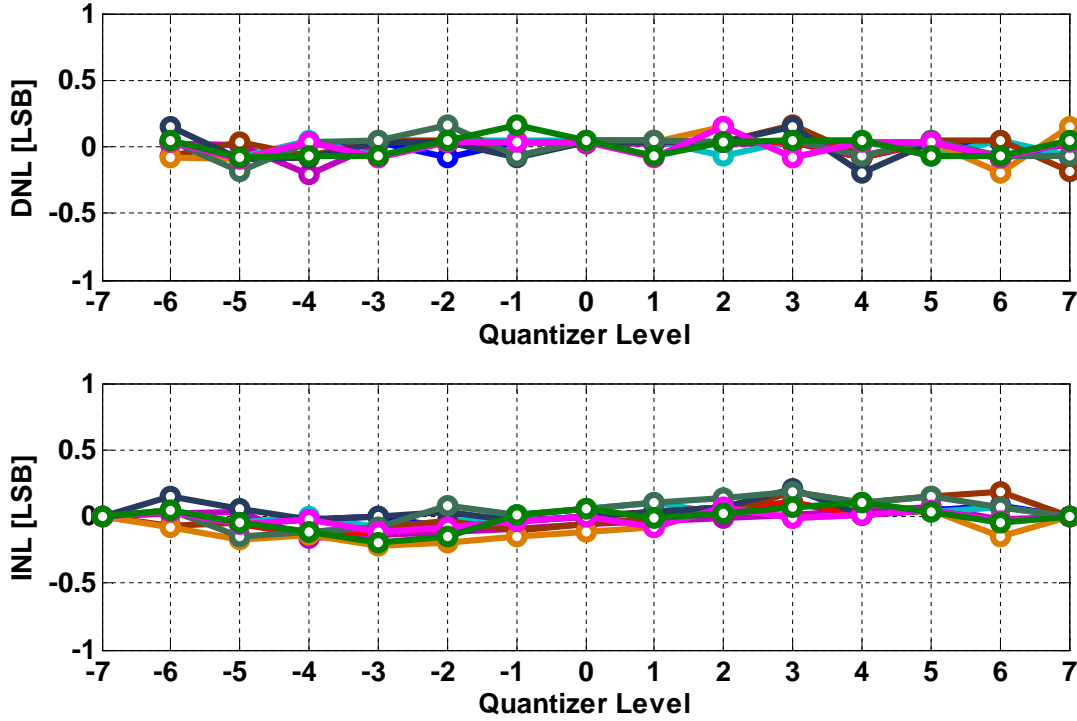
Figure 2.11: Monte-Carlo post-layout simulated DNL and INL of TA-TDC: DNL [0.2LSB] and INL [0.25LSB].

t_{LH} and t_{HL} propagation delays.

Non-linearity of the TA-TDC is a result of the non-linearity introduced either by the TA or TDC. Quantization noise cancellation in the DTC greatly reduces the input range of the TA-TDC. As a result, linearity requirements of the TA are greatly alleviated. The non-linearity of TDC resulting from systematic and random offsets of BBPDs in the TDC is minimized by using sense-amplifier based DFFs similar to [31]. High gain of the TA further suppresses non-linear errors of the TDC when referred to the TA input. Monte-Carlo post-layout simulation results show the standard deviation of BBPD input referred time offset is less than 0.35ps. Fig. 2.11 shows Monte-Carlo simulation results of the linearity performance of the entire TA-TDC (post-layout). The DNL and INL are 0.2LSB and 0.25LSB, respectively. TA-TDC performance summary and comparison to state-of-the-art high resolution TDCs are shown in Table 2.1. The proposed architecture leverages a high gain TA and simple TDC architecture, to achieve sub-1ps resolution at low power consumption.

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Table 2.1: TDC Performance Summary

	This Work	Lee [32] JSSC'08	Vercesi [33] JSSC'10	Zanuso [7] JSSC'11	Kim [34] JSSC'13	Kim [22] JSSC'14
Architecture	TA+DL	Two-step	2D Vernier	Flash	Two-step	Pipelined
Technology [nm]	65	90	65	65	65	65
Supply [V]	1	1	1.2	1.2	1.2	1.2
F_s [MS/s]	50	10	50	40	200	250
N_{bits}	4	9	7	4	7	9
Resolution [ps]	0.9	1.25	4.8	3	3.7	1.1
DNL [LSB]	0.2	0.8	1	0.5	0.9	0.6
INL [LSB]	0.25	3	3.3	0.5	2.3	1.7
N_{linear} [bits]*	3.68	7	4.9	3.41	5.28	7.57
Power [mW]	0.2	3	1.7	8	3.6	15.4
FoM**	0.31	2.34	1.14	18.81	0.46	0.32
Area [mm^2]	0.045	0.6	0.02	0.04	0.02	0.14

*$N_{linear} = N_{bits} - \log_2(\text{INL} + 1)$,   **FoM = Power$/(2^{N_{linear}} \times F_s)$ [pJ/conv.step]

The simulated gain variation of the TA-TDC across PVT variations is ±25%. This variation will impact the loop gain of PLL and DTC calibration loop. The LMS step size (μ_{LMS}) is chosen to guarantee loop convergence as explained in section III-B. If the variation of PLL bandwidth resulting from TA-TDC gain variations is high, bandwidth calibration techniques reported in [35, 36] can be used to overcome the variations.

2.4.2   Digitally Controlled Oscillator (DCO)

While the DTC-based fractional divider and TDC are the key elements in achieving wide PLL bandwidth, the DCO presents its own design challenges to realize high performance digital FNPLL. In this work, we exploit a hybrid DCO approach which is realized as the combination of a DAC and a LC-VCO with a linear varactor. The schematic of the 14-bit
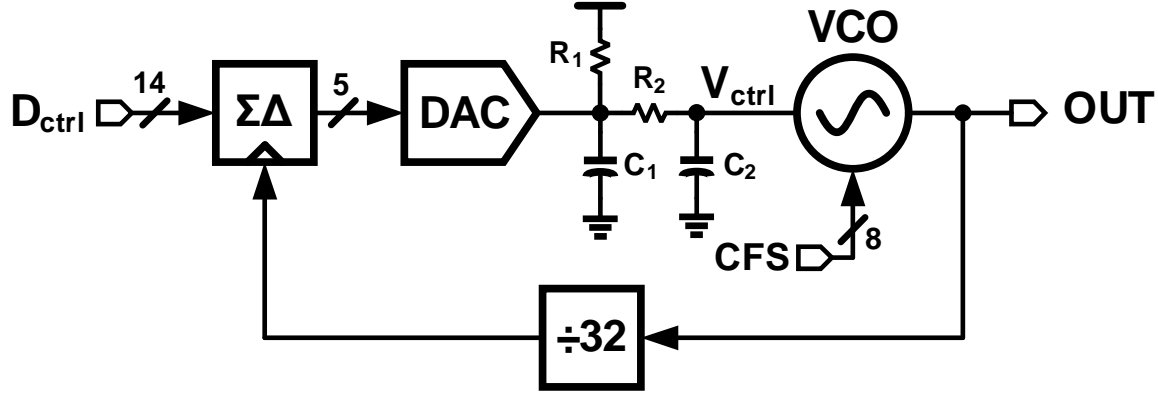
Figure 2.12: LC-based DCO implementation.

LC DCO is shown in Fig. 2.12. A second order $\Delta\Sigma$ modulator truncates the 14-bit control word (D_{CTRL}) to control 5-bit thermometer-coded current DAC. A second order RC post filter suppresses the shaped quantization noise of the DAC and controls VCO varactors. The effective resolution of the DCO is around 5kHz/LSB which is equivalent to less than 10ppm. Unlike [9], which uses low VCO gain (K_{VCO}) of only 3MHz/V, this design employs a K_{VCO} of 100MHz/V to ensure that the PLL does not lose lock across a wide range of voltage and temperature variations. However, larger K_{VCO} increases the contribution of $\Delta\Sigma$ DAC quantization noise to output phase noise. To mitigate this, the in-band quantization error of the $\Delta\Sigma$ modulator is reduced by: (a) increasing oversampling ratio of the $\Delta\Sigma$ modulator by clocking it at a frequency of $\sim$ 150MHz, which is obtained by dividing the DCO output by 32, (b) using a 5-bit (as opposed to 1-bit) current-mode DAC. Unit cells in the DAC are sized to improve static linearity while dynamic non-linearity is reduced by using thermometer coding, adding a DFF in each cell, and matching clock routing. The poles of the RC filter are set to 16MHz and 32MHz to suppress the shaped noise with minimum impact on the PLL stability even at wide bandwidth setting of 3MHz.

The VCO is implemented using CMOS cross-coupled architecture and is optimized for low power as the phase noise requirement is relaxed by the wide loop bandwidth. The VCO core power consumption is less than 1mA. The 1.4nH inductor is implemented using 2 turns of top thick metal and has a simulated quality factor of 16. The output frequency is tuned from 4.4 to 5.2GHz using two scaled banks of capacitors; 4-bit MIM capacitor bank provides the coarse control while 4-bit MOS capacitor bank provides the fine control, resulting in a

nominal coarse and fine step of around 70MHz and 10MHz, respectively. This segmentation guarantees 50% overlap between the coarse and fine banks to cover process variations. The resolution of the fine capacitor bank is chosen to be much less than the frequency tuning by the $\Delta\Sigma$ DAC, so that the PLL locks near $\Delta\Sigma$ DAC mid-range. This will allow more range for VCO temperature and supply variations after the PLL is locked.

2.4.3 Fractional Divider
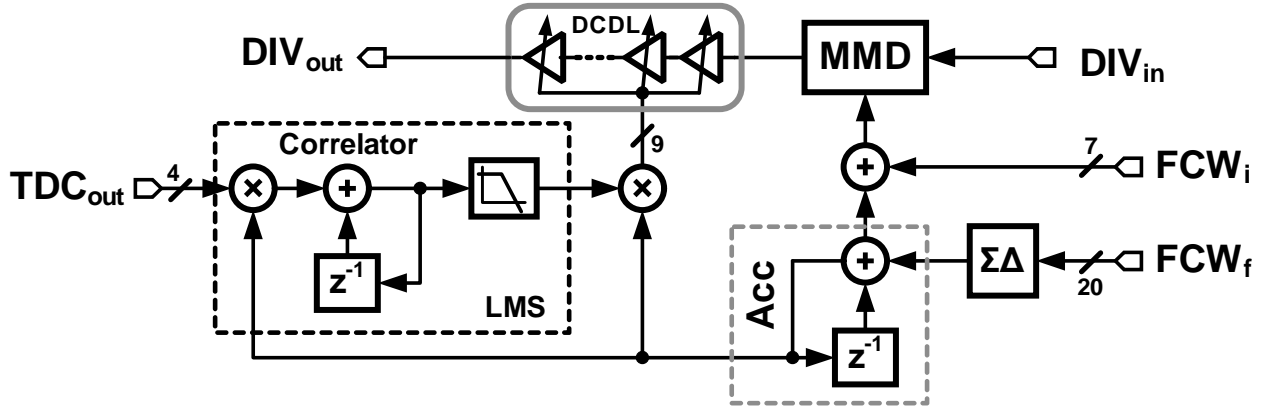
Figure 2.13: Proposed truly fractional divider.

The DCO output is divided using a 27-bit fractional divider, 7-bit integer FCW_I and 20-bit fractional FCW_F shown in Fig. 2.13. It is composed of a 6 stage multi-modulus divider (MMD) with extended division range from 32 to 127. The first divide-by-2/3 cell is implemented using TSPC DFFs to reduce the power consumption, while the other five cells are implemented using standard CMOS latches. The MMD is followed by a 9-bit DTC implemented using an 8-stages digitally controlled delay line (DCDL). The 20-bit fractional word, FCW_F, is truncated to 9-bit using second-order $\Delta\Sigma$ modulator cascaded by a 9-bit first-order $\Delta\Sigma$ modulator. A first-order error feedback modulator is adopted because it reduces the required DTC range to only one T_{DCO} without affecting fractional spur level [7]. Error feedback architecture simplifies the digital implementation as it provides the divider control directly as the accumulator carry output, and it provides directly the accumulated quantization error $E_q[k]$ as the accumulator sum output. The TDC output is correlated with $E_q[k]$, then accumulated to find the optimum DTC scale factor. An IIR low-pass filter is used

to further smooth the scale factor signal. Using a single range DTC instead of coarse-fine DTC architecture in [9] simplifies the implementation of QNC.
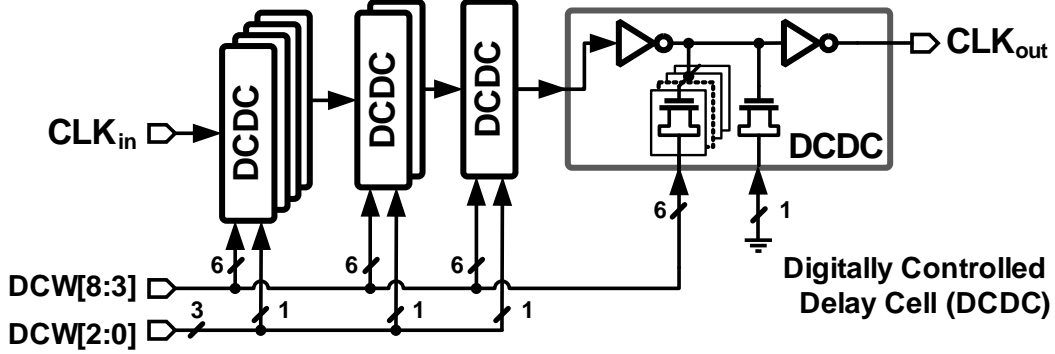
Figure 2.14: The 9-bit digitally controlled delay line (DCDL) block diagram.
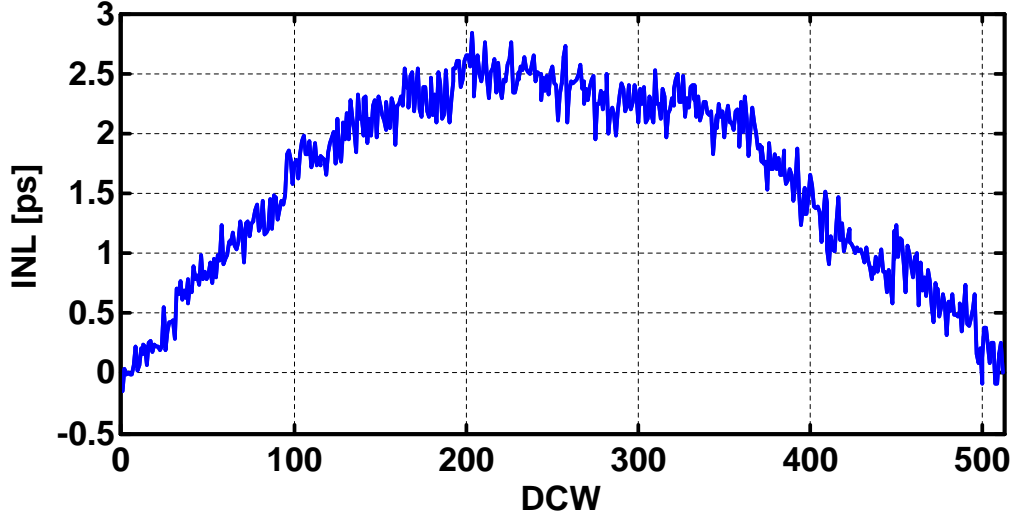
Figure 2.15: Post-layout Monte-Carlo simulations for the DCDL integral nonlinearity (INL).

A 9-bit DCDL is implemented using a cascade of 8 identical digitally controlled delay cells [27] shown in Fig. 2.14. It provides about 256ps incremental delay, to cover the minimum operating frequency of 4.4GHz across PVT variations. Eight delay stages are used instead of one large delay cell as in [9] to ensure fast rise and fall times and to reduce DCDL noise and sensitivity mismatches. Each delay cell consists of a CMOS inverter loaded with a tunable 64-unit capacitor bank followed by another inverter to restore fast rise and fall times. As shown in Fig. 2.14, the 6MSBs of the delay control word drives 63 capacitors in all delay

cells, while each of the 3LSBs control one unit capacitor in different delay cells. Post-layout Monte-Carlo simulations shown in Fig. 2.15 indicate maximum INL of less than 3ps of delay deviation, where the LSB resolution equals to about 0.5ps.

2.5   Measurement Results
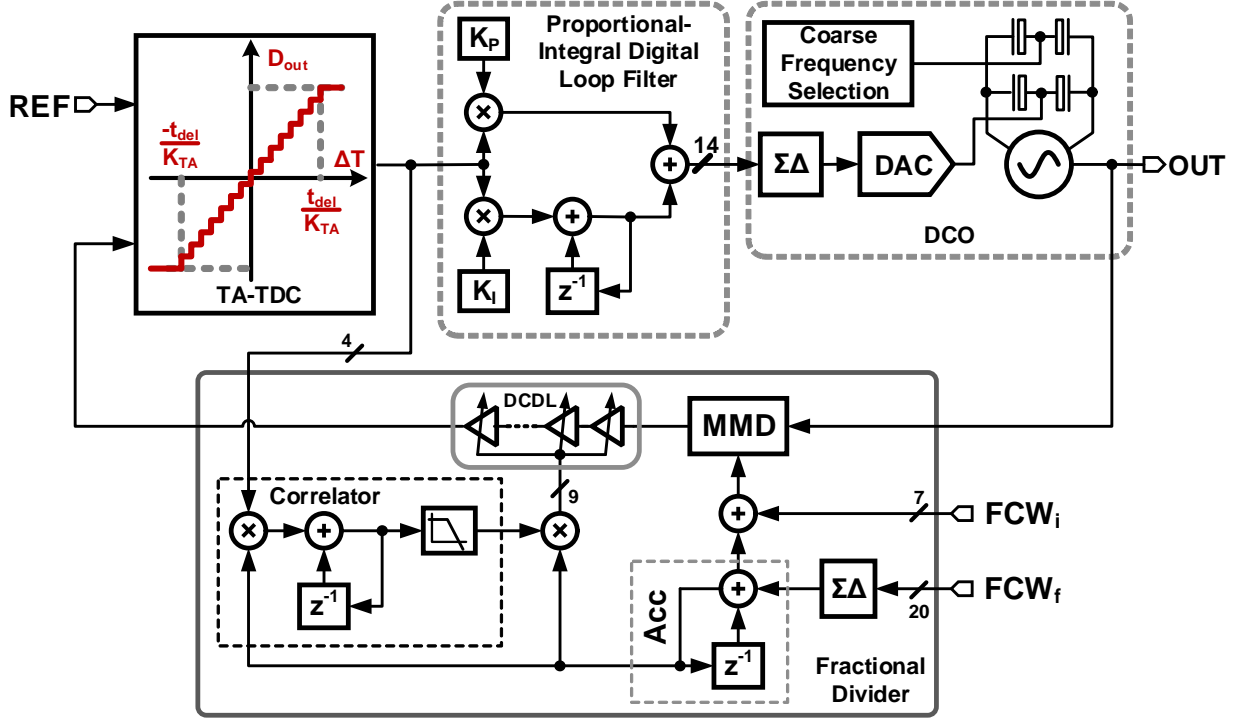
Figure 2.16: Detailed block diagram of the proposed digital FNPLL.

The proposed digital FNPLL depicted in Fig. 2.16 was fabricated in 65nm CMOS process and its die photograph is shown in Fig. 2.17. It occupies 0.22mm^2 active area, of which the proposed TA-TDC occupies only 0.045mm^2. The overall power consumption is less than 3.7mW of which the TA-TDC consumes less than 0.2mW while operating from 1V supply voltage. A 50MHz external reference clock has been used in testing. It has an integrated jitter of $0.8\text{ps}_{\text{rms}}$ and a noise floor of -147dBc/Hz. The measured phase-noise of the digital FNPLL at 4.5GHz is shown in Fig. 2.18 for a conventional BBPD and the proposed TA-based TDC. Using the proposed TA-TDC, the PLL achieves an integrated jitter of $0.44\text{ps}_{\text{rms}}$ which is 2x lower than a conventional BBPD of $0.84\text{ps}_{\text{rms}}$. This result also shows that about
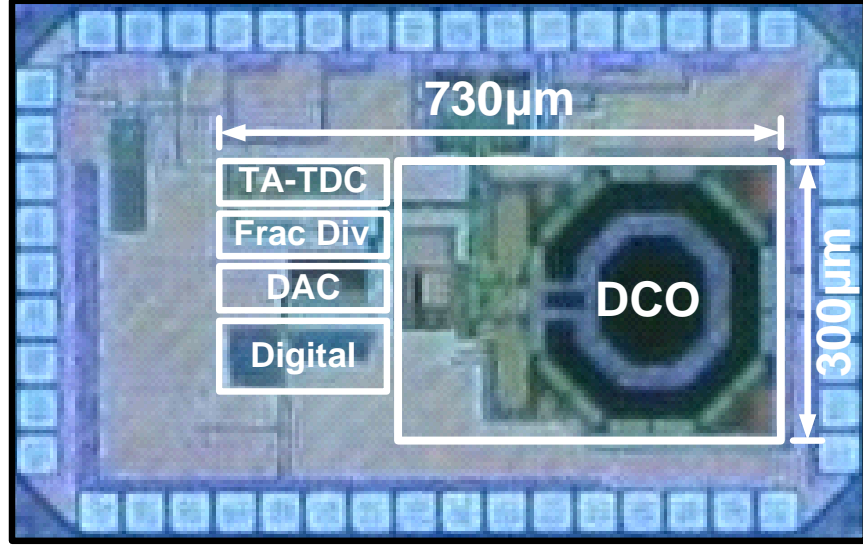
Figure 2.17: Die photograph.

9dB in-band phase-noise improvement is achieved while using the TA-TDC.
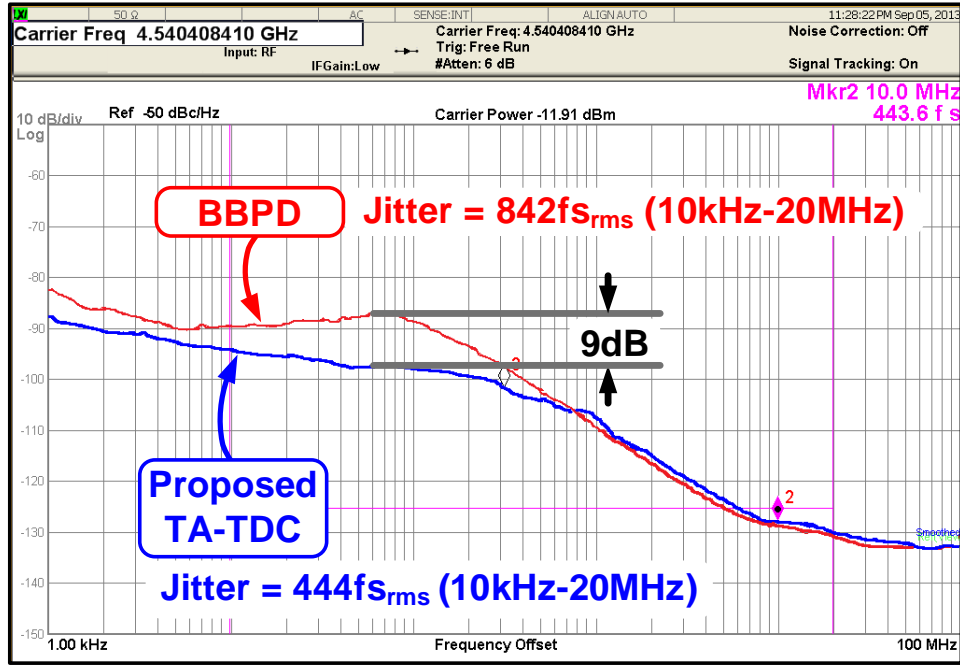
Figure 2.18: Measured phase noise of the digital FNPLL at 4.5GHz for (a) conventional BBPD, and (b) proposed TA-TDC.

Fig. 2.19 shows the measured phase-noise for different bandwidth settings, from 0.75MHz to 3MHz, at 4.5GHz output. The bandwidth is controlled by changing the gain of the proportional path K_p. Even for a wide bandwidth setting of 3MHz ($\backsim$ Fref/16), no peaking

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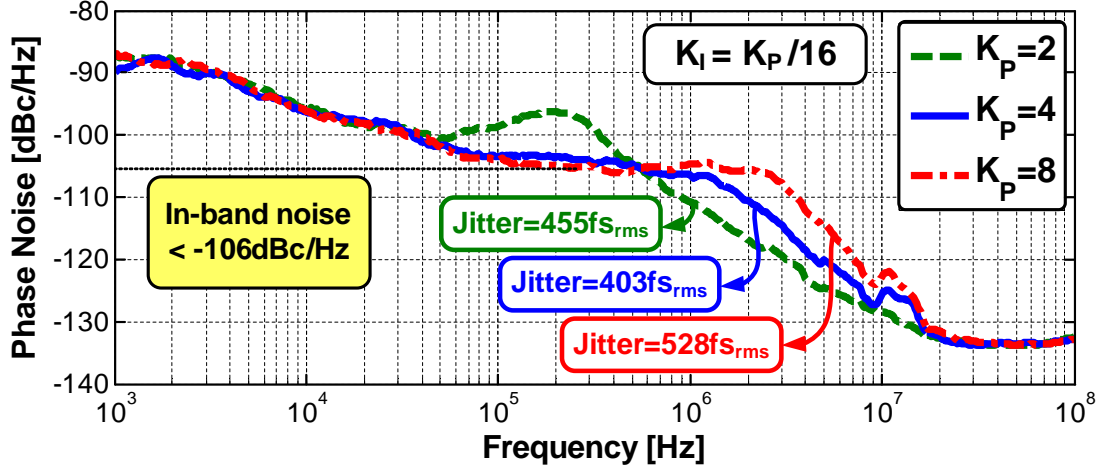
Figure 2.19: Measured phase noise for different BW settings (0.75MHz to 3MHz) at 4.5GHz output using 50MHz reference, obtained by varying the proportional path (K_p) settings.
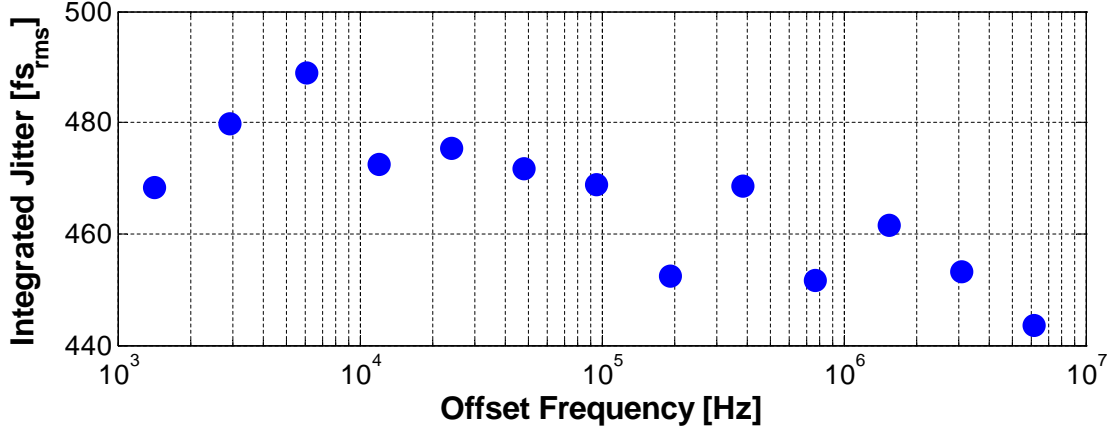
Figure 2.20: Measured rms integrated jitter as a function of output fractional frequency offset.

or limit cycle behavior is observed in the output spectrum, and the proposed TA-TDC achieves an in-band noise of -106dBc/Hz. At 1.5MHz BW, an excellent integrated jitter of $0.4ps_{rms}$ is achieved which slightly increases to $0.45ps_{rms}$ and $0.53ps_{rms}$ for bandwidth of 0.75MHz and 3MHz, respectively. For the low bandwidth setting (K_p=2), the DCO noise is not adequately filtered. As a result, it exceeds the in-band noise floor which should be limited by reference and TDC noise. The measured in-band noise floor is better than -106dBc/Hz at 4.5GHz output frequency. The measured integrated jitter is plotted as a function of output fractional frequency offset, shown in Fig. 2.20, indicating a worst-case jitter less than

0.49ps$_{\text{rms}}$. The slight increase in jitter at small fractional frequency offsets is due to in-band fractional spurs generated due to DCDL integral non-linearity (INL).
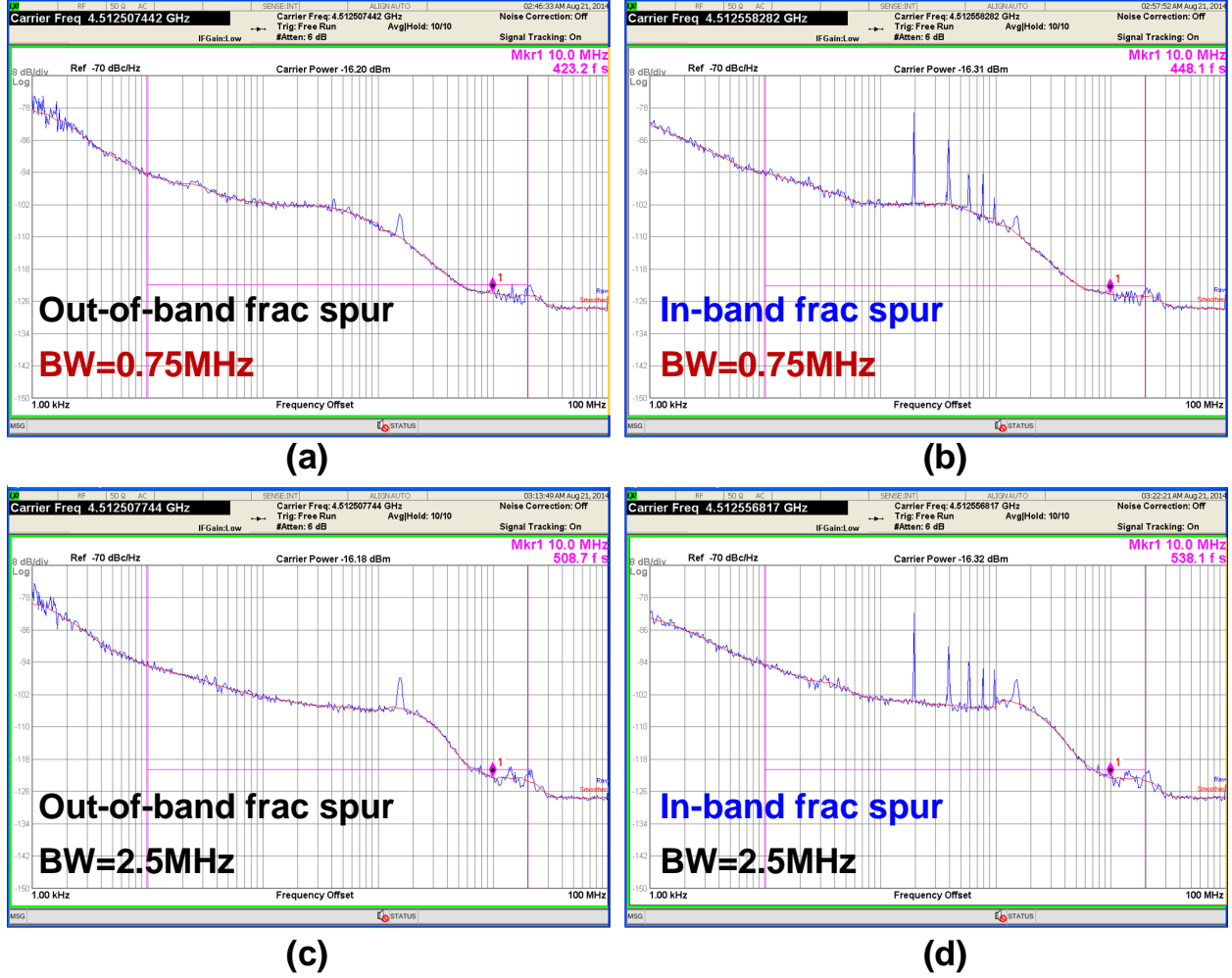
Figure 2.21: Measured output spectra for (a) out-of-band fractional spurs and 0.75MHz bandwidth, (b) in-band fractional spurs and 0.75MHz bandwidth, (c) out-of-band fractional spurs and 2.5MHz bandwidth, and (d) in-band fractional spurs and 2.5MHz bandwidth.

The measured phase noise spectra for 0.75MHz and 2.5MHz bandwidths are shown in Fig. 2.21 for the in-band and out-of-band fractional spurs. For 0.75MHz bandwidth, the proposed fractional-N DPLL achieves an integrated jitter of 423fs$_{\text{rms}}$ and 448fs$_{\text{rms}}$, for out-of-band and in-band spurs, respectively. When the bandwidth is increased to 2.5MHz, the integrated jitter increases only by about 85fs, thanks to the fine resolution of the proposed TA-TDC. Fig. 2.22 shows the measured output spectrum of the proposed PLL with 392kHz in-band fractional spurs. The in-band fractional spur is -52.2dBc. This excellent spurious
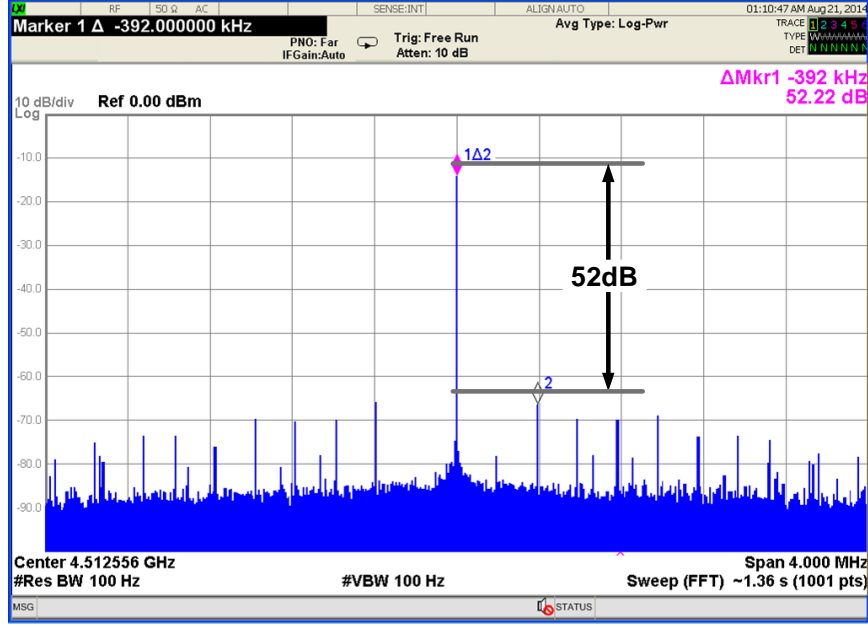
Figure 2.22: Measured output spectrum at 4.5GHz output frequency and 392kHz fractional offset.

performance, compared to [9], is achieved due to the better linearity of the proposed DTC architecture, without using complex non-linearity calibration [37]. The measured reference spur is less than -69dBc. The integrated jitter was measured for different values of the output frequencies from 4.4GHz to 5.2GHz, and the results are shown in Fig. 2.23 for different bandwidth values. The integrated rms jitter varies by less than 100fs over the output frequency range.

The performance summary and comparison with state-of-the-art low jitter fractional-N PLLs are shown in Table 2.2. The proposed architecture achieves the best reported jitter of $0.55\text{ps}_{\text{rms}}$ at 3MHz BW compared to [7, 10]. Plotted in Fig. 2.24 is the worst-case integrated jitter performance versus power consumption which is reflected in a figure of merit (FoM$_{\text{J}}$) [38] . The proposed digital FNPLL achieves the best FoM$_{\text{J}}$ of -240.5dB compared to state-of-the art digital and analog FNPLLs. It achieves at least 8dB better than other reported digital FNPLLs when the in-band phase noise is included in FoM$_{\text{IBPN}}$. The proposed architecture achieves excellent spurious performance along with the best power efficiency of 0.82mW/GHz.

Table 2.2: LC-based Digital FNPLL Performance Summary

	Hsu [5] JSSC'08	Temporiti [10] JSSC'10	Yao [39] VLSI'11	Zanuso [7] JSSC'11	Tasca [9] JSSC'11	Nonis [24] JSSC'13	This Work
Architecture	TDC	TDC	TDC	PI+TDC	DTC+BBPD	PI+BBPD	DTC+TDC
Technology [nm]	130	65	55	65	65	130	65
Supply [V]	1.5	1.2	1.2	1.2	1.2	1.5	1.0
Output Freq. [GHz]	3.67	2.8-3.8	5.9-8.0	3.6	2.9-4.0	0.84-1.032	4.4-5.2
Ref. Freq. [MHz]	50	35	2×40	40	40	25	50
Power [mW]	39	8.7	36	80	4.5	7.5	3.7
Ref. Spur [dBc]	-64	-61	-94	-61	-72	-70	-69
In-band Frac. Spur [dBc]	-53	-58	-70	-57	-42	N/A	-51.5
Bandwidth [MHz]	0.5	3.4	0.5	3.2	0.312	1	0.75 3
In-band PN [dBc/Hz]*	-108	-101	-107	-104	-101	-95	-102 -108
Integrated Jitter [ps$_{rms}$]	0.3 1k-40MHz	1.07 10k-10MHz	0.19 1k-10MHz	0.89 10k-30MHz	0.56 3k-30MHz	2.1 1k-10MHz	0.49 0.55 10k-20MHz
FoM$_{IBPN}$ [dB]**	-283.2	-282.7	-282.8	-276.1	-285.1	-277.4	-287.4 -293.4
FoM$_J$ [dB]*	**-234.5**	**-230**	**-238.9**	**-222**	**-238.3**	**-224.8**	**-240.5 -239.5**
Power Eff. [mW/GHz]	10.82	2.29	6.1	22.22	1.13	7.5	0.82
Area [mm²]	0.95	0.44	0.68	0.4	0.22	0.25	0.22

* *Normalized IBPN to 3.6GHz,*

** FoM$_{IBPN}$ = IBPN + 10log $\left[\left(\frac{1Hz}{F_{out}}\right)^2 \frac{P}{1mW}\right]$,

*** FoM$_J$ = 10log $\left[\left(\frac{\sigma_{rms}}{1sec}\right)^2 \frac{P}{1mW}\right]$,
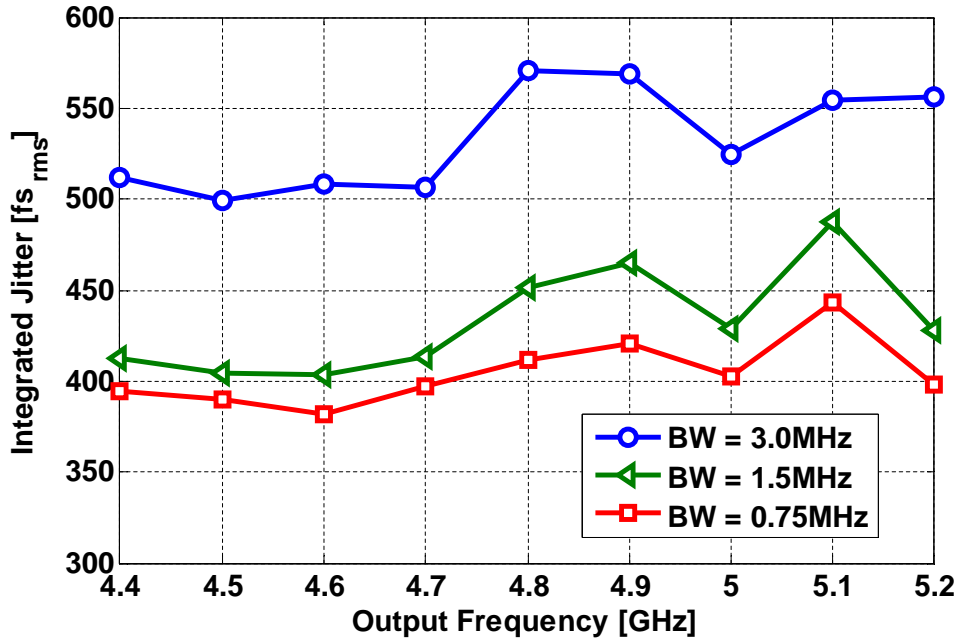
Figure 2.23: Measured rms integrated jitter as a function of the output frequency for different bandwidth settings.
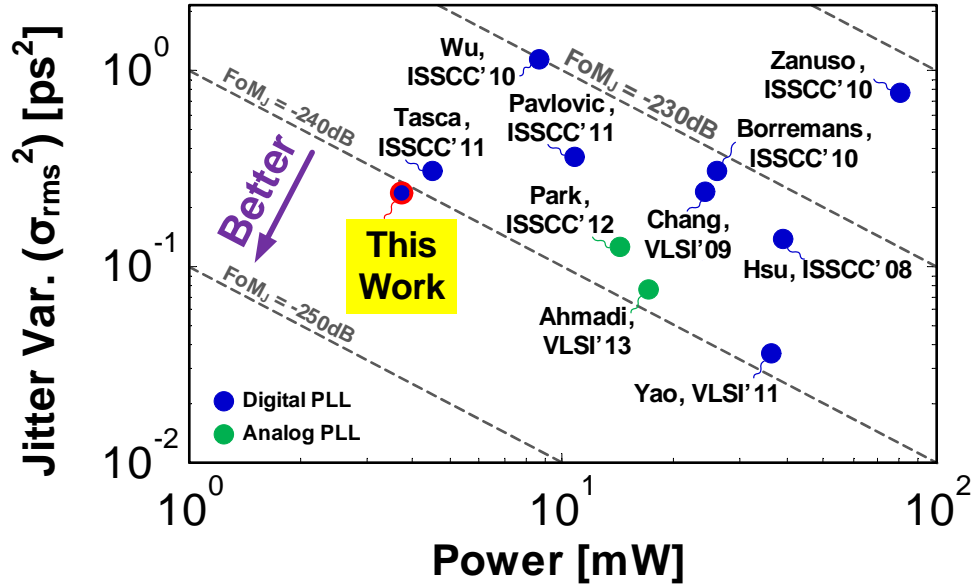
Figure 2.24: FoM comparison.

2.6 Conclusion

A digital fractional-N PLL that achieves wide bandwidth and low jitter is presented. The proposed PLL employs a 9-bit DTC-based fractional divider that alleviates TDC dynamic

range requirements. A high-resolution low-power time-amplifier-based TDC (TA-TDC) is used to achieve low in-band noise and PLL wide bandwidth. The proposed TDC maintains linear loop dynamics with programmable PLL BW and faster DTC-gain calibration. The measured results indicate an excellent jitter performance at low power consumption, low in-band phase noise and wide PLL BW with no limit cycles.

CHAPTER 3

A 2.0-5.5 GHZ RING-BASED DIGITAL FNPLL WITH EXTENDED RANGE MMD

3.1 Introduction

Fractional-N phase locked loops (FNPLLs) are widely used in large digital systems such as modern processors and in almost all wireless and wireline transceivers. FNPLLs can synthesize output frequency, F_{OUT}, that is a fractional multiple, $N + \alpha$ (N is an integer, α is a fraction $0 < \alpha < 1$), of fixed reference crystal oscillator frequency, F_{REF} ($F_{OUT} = (N + \alpha)F_{REF}$). By varying N and α, FNPLLs are used to generate variable frequency clocks needed to implement finely granular dynamic frequency scaling in energy efficient processors [40], to generate local oscillator signals in wireless transceivers [4], to perform clock and data recovery [41], or to implement single-chip multi-standard-compliant wireline transceivers capable of operating across a wide and continuous range of data-rates [42–45].

Typically, FNPLLs are implemented using the classical analog charge pump PLL architecture to meet jitter and spurious performance requirements. However, they require a large capacitor to implement the loop filter, which incurs a large area penalty. Further, low supply voltage and transistor imperfections in deeply scaled CMOS process also detrimentally impact the performance of the charge pump and degrade FNPLL performance. To alleviate these drawbacks, FNPLLs are being implemented using highly digital architectures that obviate the need for large capacitors and charge pumps. A digital FNPLL is obtained from a conventional charge-pump FNPLL by replacing the phase detector/charge-pump, and the analog loop filter, by a time-to-digital converter (TDC), and a digital loop filter (DLF),

respectively. A digital-to-analog converter (DAC) converts output of the DLF (D_C) to a control voltage (V_C) of the VCO as depicted in Fig. 3.1(a).
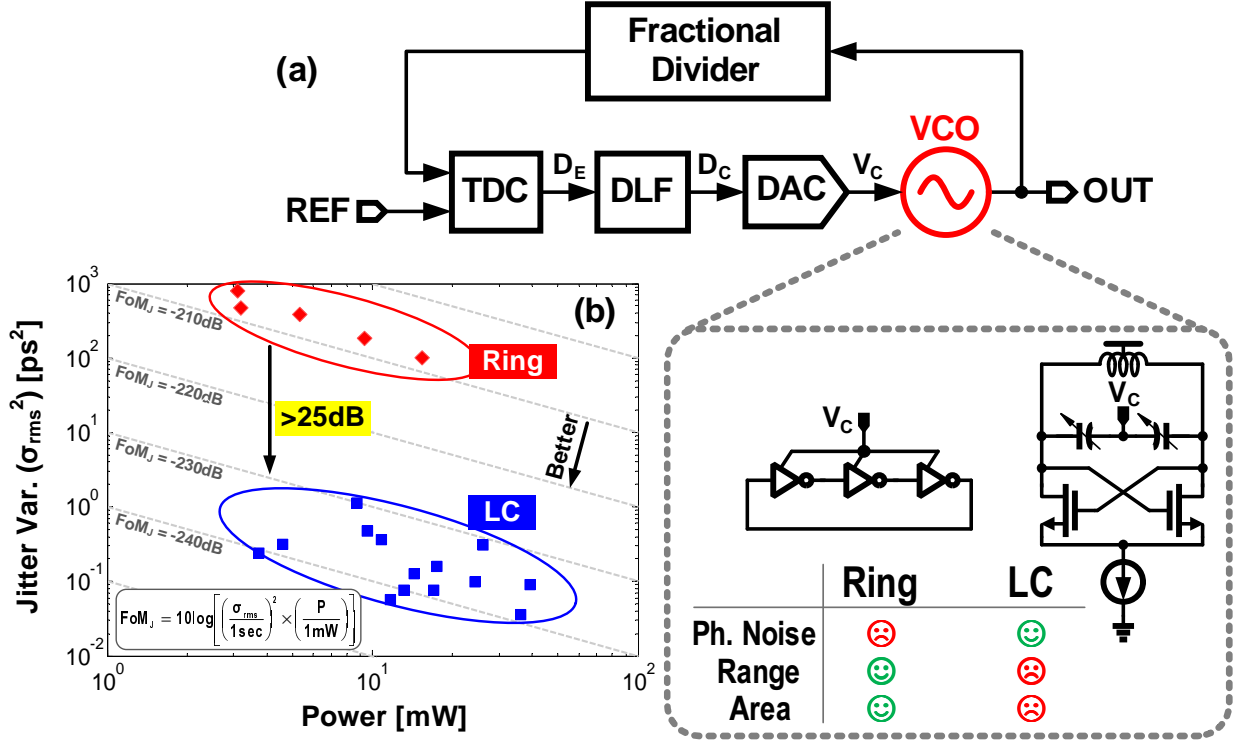
Figure 3.1: (a) Digital FNPLL architecture using either ring- or LC-VCO. (b) Figure-of-merit (FOM_J) of state-of-the-art LC- and ring-based digital FNPLLs.

A digital FNPLL, in principle, offers several advantages over its analog counterpart in terms of loop dynamics reconfigurability, scalability to newer process, and smaller silicon area. As a result, digital FNPLLs are particularly well suited for variable and flexible clock generation in area-sensitive application such as multi-core processors, chip-to-chip I/O interfaces, and SoCs platforms [40]. However, in practice, quantization errors introduced by the fractional divider (FDIV), TDC, and DAC degrade digital FNPLL performance. As a result, jitter performance of digital FNPLLs, especially those using ring oscillators, is grossly inferior to their analog counterparts [40, 46–50]. Ring oscillators are extremely low-cost, scalable, and can inherently provide multiple phases with a wide tuning range. A compact ring-based FNPLL with a wide output frequency range can be independently utilized per a microprocessor core [40] or a full flexible I/O transceiver lane [43]. However, ring voltage controlled oscillators (VCOs) fundamentally have poor phase noise performance

compared to LC VCOs. While fractional-N multiplying delay locked loops (MDLLs) [51] can achieve wider bandwidth (BW) than FNPLLs, they have speed limitation due to the use of selection logic which limits the maximum frequency range.

In view of this, we seek to improve the performance of ring oscillator based digital FNPLLs using a combination of architectural- and circuit-level techniques. To this end, a wide BW ring-based digital FNPLL with a wide output frequency range is presented. The proposed FNPLL achieves low power, low jitter performance, by using highly digital/synthesizable enhancement techniques [52]. The quantization errors of TDC and FDIV are suppressed by using a time amplifier (TA) [53] and digital-to-time converter (DTC)-based FDIV noise cancellation [9, 53], respectively. Furthermore, a dual-path digital loop filter architecture is proposed to resolve the DAC quantization noise challenge, which is stressed by the large gain of ring VCOs. This architecture also helps to mitigate the limit cycle behavior, typically associated with digital PLLs, and achieves wide PLL BW ($> 0.1F_{REF}$) to maximize suppression of ring VCO phase noise. To attain a wide output range of 2.0-5.5GHz, a multi-modulus divider (MMD) with wide programmable division range is required. However, using a conventional extended range MMD [54], the fractional operation fails at boundaries extension with a division factor changing between N and $N + 1$. In this work, we propose a modified extended range MMD that enables seamless switching at the boundaries extension. The prototype digital FNPLL achieves 1.9ps$_{rms}$ integrated jitter while consuming only 4mW at 5GHz. It achieves a jitter-power figure-of-merit (FoM$_J$) of -228.5dB, which is the best among all reported ring-based FNPLLs.

The rest of the chapter is organized as follows. Section 3.2 entails the design trade-offs of ring-based digital FNPLLs. Design details of the proposed ring-based FNPLL are described in section 3.3. Design and analysis of an extended range multi-modulus divider is presented in section 3.4. The circuit implementation of critical building blocks of the digital FNPLL is illustrated in section 3.5. The measured results from the test chip are shown in section 3.6. Finally, the key contributions of this chapter are summarized in section 3.7.

3.2 Ring-Based Digital FNPLL Design Tradeoffs

There are four primary sources of output jitter in a digital FNPLL, namely, quantization error of TDC, DAC, $\Delta\Sigma$ fractional divider (FDIV) and phase noise of VCO. The impact of these quantization errors can be mitigated by noise cancellation or suppression techniques. Suppressing quantization errors introduces conflicting bandwidth (BW) requirements, which typically results in an increase in the power consumption. To elucidate this further, the TDC and FDIV quantization errors are low-pass filtered, while VCO phase noise is suppressed by a high pass transfer function. Due to this conflicting BW requirement, low noise digital FNPLLs either employ a high resolution TDC or a low noise oscillator, both of which increase power dissipation. In view of this, all digital FNPLLs with reasonable output jitter have employed LC VCOs [5, 9, 53] as they exhibit superior phase noise performance and power efficiency compared to ring-based VCOs. This can be quantified by a widely used VCO figure-of-merit (FoM$_{\text{OSC}}$) defined as:

$$\text{FoM}_{\text{OSC}} = -\mathcal{L}\left(\Delta\omega\right) + 10\log\left[\left(\frac{\omega_{\text{o}}}{\Delta\omega}\right)^2 \cdot \frac{1}{\text{P}_{\text{mW}}}\right] \tag{3.1}$$

where ω_{o} is the VCO frequency, $\mathcal{L}\left(\Delta\omega\right)$ is the phase noise at offset $\Delta\omega$, and P$_{\text{mW}}$ is the oscillator power consumption in mW. FoM$_{\text{OSC}}$ of LC VCOs is fundamentally higher than ring VCOs [55], which is manifested by about 20dB performance gap in a recent survey [56]. This translates to a similar performance gap of at least 25dB in the FoM$_{\text{J}}$ of state-of-the-art ring- and LC-based FNDPLLs (see Fig. 3.1(b)). However, LC VCOs have several drawbacks: first, they require thick metal layers, large silicon area, and do not scale with CMOS process. Second, LC VCOs with high quality factor (Q) have a very narrow tuning range. Additionally, generation of multiple clock phases requires additional circuitry of quadrature VCOs [57], I/Q dividers [44], poly-phase filters [45], or delay locked loops (DLLs) [42]. Therefore, LC VCOs are not preferred for area-sensitive applications that require multiple clock phases and/or wide output frequency range.

Fig. 3.2(a) shows the simulated phase noise of a ring-based digital FNPLL when the PLL BW was chosen low enough to make the contribution of quantization errors to the output
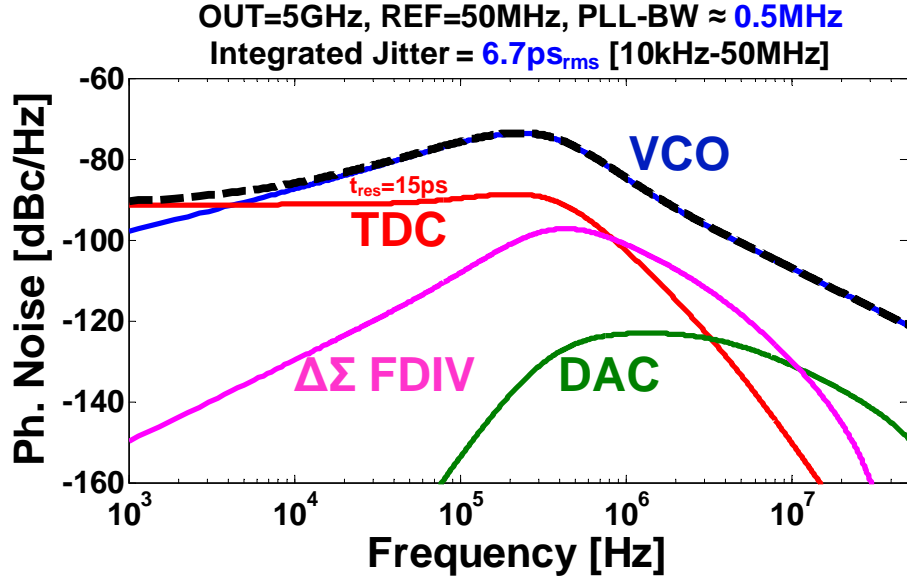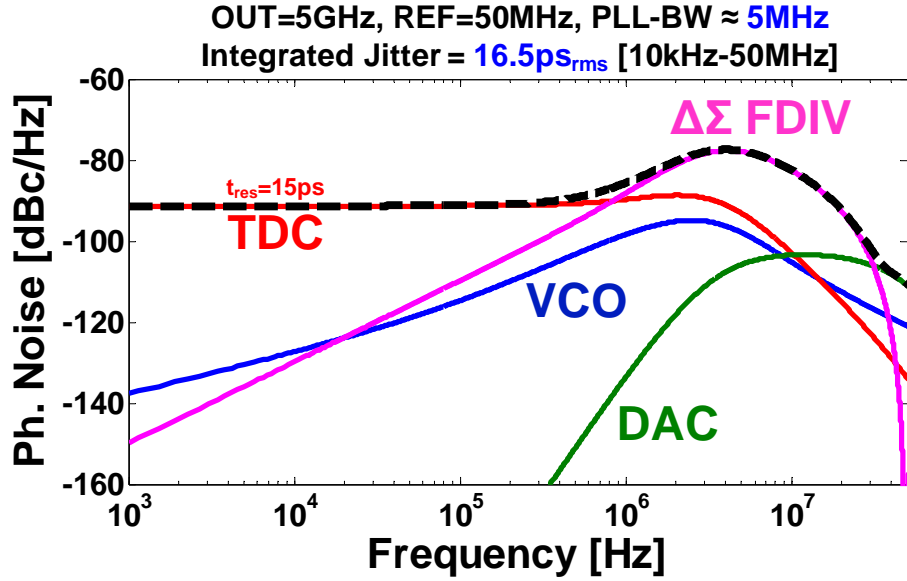
Figure 3.2: Simulated digital FNPLL phase noise plots for two cases of bandwidths: (a) low bandwidth to suppress quantization error, and (b) high bandwidth for VCO phase noise suppression.

phase noise negligible. In this particular example, we assumed a second order $\Delta\Sigma$-based FDIV, a conventional TDC with a 15ps resolution, a 5-bit DAC driven by a second order

$\Delta\Sigma$ modulator clocked at 156MHz, and a K_{VCO} of 1GHz/V. The BW is chosen to be about 500kHz and the reference frequency is 50MHz with the free running ring VCO phase noise of -87dBc/Hz at 1MHz offset. Due to the low BW, the total output phase noise is dominated by the VCO phase noise, resulting in a large integrated jitter of about 6.7ps$_{rms}$. In the other extreme case, when the PLL BW is increased to as high as 5MHz ($\approx F_{REF}/10$), VCO phase noise is sufficiently suppressed as depicted in Fig. 3.2(b). However, output phase noise is dominated by quantization errors from TDC, FDIV, and DAC. The integrated jitter is larger than 16ps$_{rms}$ in this case. The large frequency drift across temperature of ring VCOs mandates a large gain ($K_{VCO} \approx 1$GHz/V) to maintain lock across temperature. This leads to a higher impact of DAC quantization noise at the PLL output.

3.2.1   Quantization Noise Cancellation

Digital quantization noise cancellation (QNC) techniques are used to cancel FDIV quantization error at the output of the TDC [5], thereby greatly reducing its impact. For accurate cancellation, the cancellation gain is computed in background using an all-digital least-mean square (LMS) correlation technique. In this architecture, the wide dynamic range requirement of the TDC increases its power consumption and compromises its linearity performance, and consequently degrades jitter and spurious performance of the digital FNPLL. Additionally, the TDC must have fine effective resolution (t_{res}) to achieve low in-band phase noise. Assuming the TDC quantization noise ($S_{q_{TDC}}$) is uniformly distributed, the output phase noise due to TDC ($S_{\Phi_{TDC}}$) can be calculated as [53]:

$$S_{\Phi_{TDC}} = |NTF_{TDC}(f)|^2 \, S_{q_{TDC}} = \left[\frac{2\pi \, t_{res} \, N \, G(f)}{T_{REF}}\right]^2 \cdot \left(\frac{1}{12 \, F_{REF}}\right) \tag{3.2}$$

where $NTF_{TDC}(f)$ is the noise transfer function of TDC noise to the output, and $G(f)$ is the unity-gain PLL close loop transfer function. Our objective is to develop low power BW extension techniques to suppress ring-VCO phase noise and leverage its merits of wide range, multi-phases, and low cost, while achieving performance close to LC-based PLLs. The proposed architecture with DTC-based fractional divider, narrow range high resolution TDC,

and dual-path loop filter architecture mitigates quantization errors in digital fractional-N PLLs. It enables wide BW operation up to $F_{REF}/8$ to suppress ring VCO phase noise.

3.3   Proposed Digital FNPLL Architecture

The detailed block diagram of the proposed digital fractional-N PLL (FNPLL) is depicted in Fig. 3.3. A time amplifier (TA) magnifies the input phase difference between reference and feedback clocks, which is then digitized using a 4-bit coarse delay-line based TDC. The implementation details of the TA-TDC are similar to [53]. The PLL has a type-II response using a proportional-integral loop filter structure. The thermometer-coded TDC output directly controls the digitally controlled ring oscillator (DCRO) and implements a fast proportional control. The slow integral control path accumulates the 4-bit binary TDC output, which is synchronized to the $\Delta\Sigma$ DAC clock (F_{DS}), and scaled by K_I. The DTC is added in the feedback path to cancel $\Delta\Sigma$ quantization noise in time domain and implement a truly fractional divider [9]. This limits input range of the TDC and as a result, it operates in the random noise limited region, as the reference and feedback clocks are now aligned as in the case of an integer-N PLL. Consequently, the wide dynamic range requirement of the TDC is alleviated, and a low power, high resolution, narrow range TDC can be used [52,53]. The output of the TDC is used in a LMS correlation algorithm to scale the DTC gain needed to implement precise QNC. Using the QNC scheme and a high resolution TDC ($\sim$2ps), both in-band and out-of-band phase noise performance are greatly enhanced. As a result, at a wide PLL BW of $F_{REF}/10$, which is about 5MHz in this example, the output integrated jitter is reduced to about 2.5ps$_{rms}$. Further improvement in jitter performance is possible by mitigating DAC quantization noise, which dominates phase noise above 10MHz offsets.

3.3.1   Dual-Path DAC

The conventional implementation of a digital loop filter encompasses adding the proportional and integral paths in digital domain as illustrated in Fig. 3.4(a). The output of the loop filter is mapped using a DAC to control the VCO frequency. The output phase noise due to

Figure 3.3: Detailed block diagram of the proposed ring-based digital FNPLL.

Figure 3.4: (a) Conventional DAC and (b) proposed dual-path DAC.

DAC ($S_{\Phi_{DAC}}$) can be calculated using:

$$S_{\Phi_{DAC}} = |NTF_{DAC}(f)|^2 \, S_{q_{DAC}} = \left[\frac{V_{DAC} \, \text{sinc} \, (f/F_S)}{2^{m_{DAC}}} \cdot \frac{K_{VCO} \, (1 - G(f))}{f} \right]^2 \cdot \left(\frac{1}{12 \, F_S} \right) \quad (3.3)$$

where $\text{NTF}_{\text{DAC}}(f)$ is the band-pass noise transfer function of DAC noise to the output, S_{qDAC} is the DAC quantization noise, V_{DAC} is DAC full-scale voltage range, m_{DAC} is DAC number of bits, and F_S is DAC sampling frequency. The $\text{sinc}(f/F_S)$ term is due to the DAC zero-order hold for discrete-time to continuous-time conversion. As the required VCO frequency range increases, larger K_{VCO} is used, and so a higher resolution DAC is needed to reduce the impact of its quantization noise. In order to reduce the hardware complexity of high resolution DACs [5, 58], $\Delta\Sigma$ DAC architecture is typically employed in DPLLs [40, 59, 60], where a digital $\Delta\Sigma$ modulator with order (p), usually clocked at a higher sampling frequency F_{DS}, drives a single- or a multi-bit DAC (m_{DAC}) to shape the quantization noise as shown in Fig. 3.4. The output phase noise due to quantization error of $\Delta\Sigma$ DAC can be expressed as:

$$S_{\Phi_{\text{DAC}}} = \left[\frac{V_{\text{DAC}} \, \text{sinc} \, (f/F_{\text{DS}}) \, H_{\text{LPF}}(f)}{2^{m_{\text{DAC}}}} \cdot \frac{K_{\text{VCO}} \, (1 - G(f))}{f} \right]^2 \cdot \left(\frac{1}{12 \, F_{\text{DS}}} \right) \cdot \left[2 \sin \left(\frac{\pi f}{F_{\text{DS}}} \right) \right]^{2p}$$

(3.4)

A low-pass filter, $H_{\text{LPF}}(f)$, helps to suppress DAC shaped noise. Fig. 3.5(a) shows the magnitude response of $\text{NTF}_{\text{DAC}}(f)$. But $H_{\text{LPF}}(f)$ adds loop latency and may impact PLL stability at wide BW setting. To quantify this, behavioral simulations were performed at 5GHz output using a 50MHz reference, and the following parameters: 5MHz PLL BW, K_{VCO} =1GHz/V, V_{DAC} =0.7V, m_{DAC} =5bits, F_{DS} =156MHz, and second order filter $H_{\text{LPF}}(f)$ with poles at 16MHz and 32MHz. The limit cycle behavior increases the output integrated jitter to 3.5ps$_{\text{rms}}$ as opposed to 2.5ps$_{\text{rms}}$ calculated using the linear model. Increasing the oversampling clock frequency F_{DS} by four times to 624MHz reduces DAC noise and a 2ps$_{\text{rms}}$ integrated jitter can be achieved. But this increases DAC power consumption by four times. Besides, it may degrade the dynamic linearity performance of the DAC. Static and dynamic DAC non-linearity folds shaped quantization noise into in-band, and may limit the overall PLL phase noise performance. Fig. 3.5(b) plots the simulated output integrated jitter versus DAC non-linearity.

Reducing the low-pass filter, $H_{\text{LPF}}(f)$, bandwidth helps to reduce the impact of DAC imperfections, but as mentioned earlier, it also increases loop delay. To circumvent this, VCO control is split into two paths: a fast proportional control path with a small VCO gain
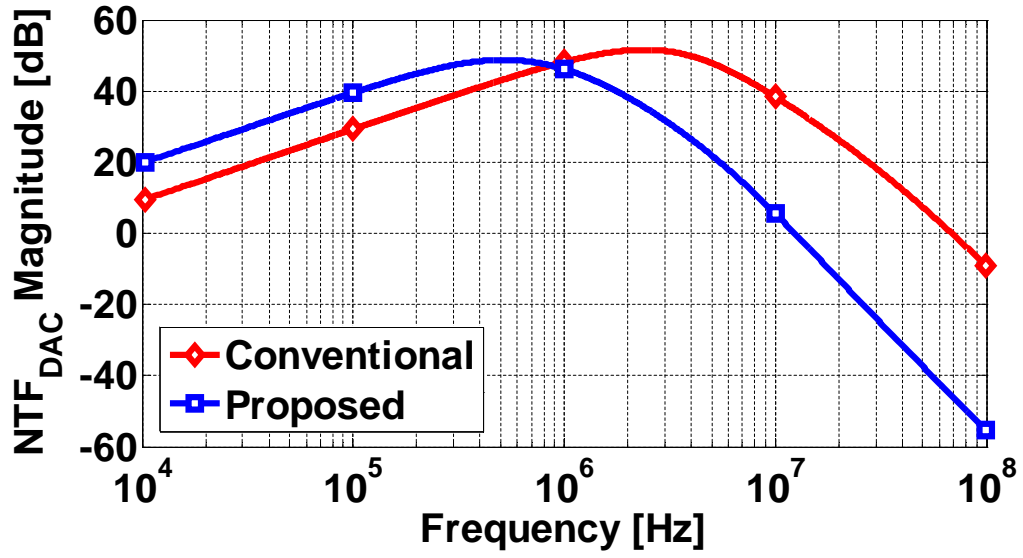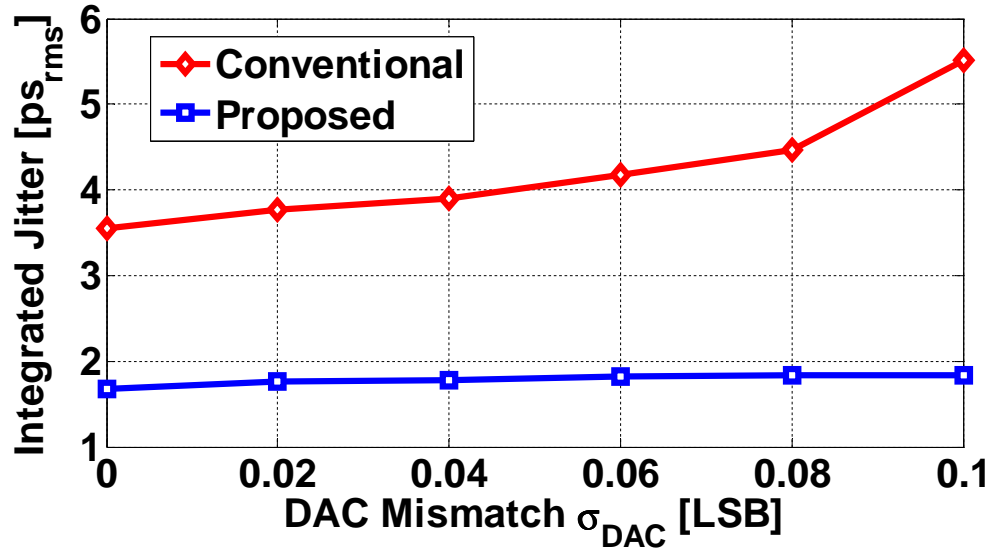
Figure 3.5: (a) Simulated noise transfer function (NTF) of conventional and proposed DACs. (b) Simulated integrated jitter of digital FNPLL using conventional and proposed DACs.

K_{PP}, and a slow integral control path with a large K_{VCO} as shown in Fig. 3.4(b). A fast 4-bit Nyquist DAC_P directly controlled by TDC output helps to minimize loop latency and eliminates any limit cycle behavior. This limits jitter peaking even with a very wide BW of $F_{REF}/8$. The PLL loop BW is mainly defined by the proportional control K_{PP} as expressed
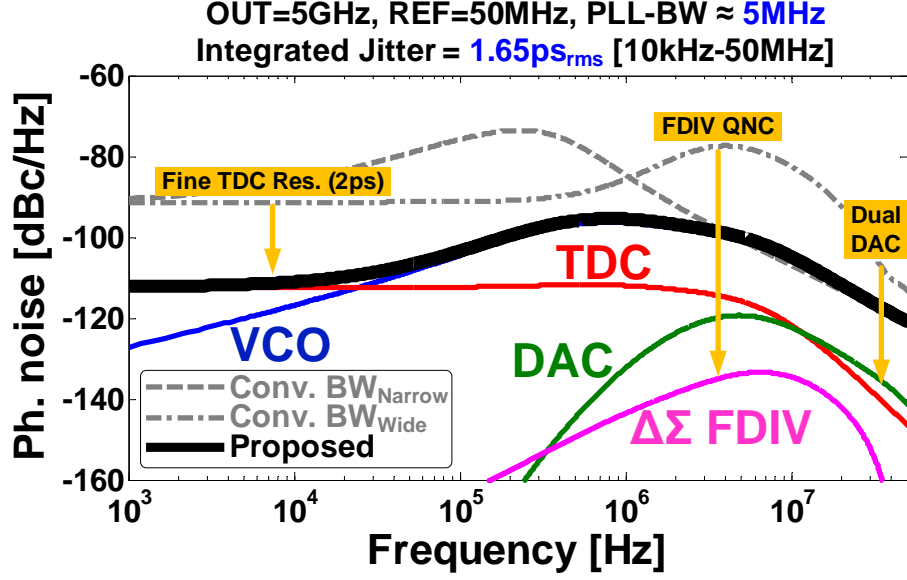
Figure 3.6: Simulated phase noise of the proposed ring-based digital FNPLL.

by loop gain transfer function:

$$LG(s) \approx \frac{T_{REF} \, K_{PP}}{s \, N \, t_{res}} \cdot \left(1 + \frac{K_I}{s \, T_{REF}} \cdot \frac{V_{DAC}}{2^{m_{DAC}}} \cdot \frac{H_{LPF}(s) \, K_{VCO}}{K_{PP}} \right) \qquad (3.5)$$

This architecture decoupled DAC_I filtering from loop BW. Hence, DAC_I quantization noise can be aggressively filtered as illustrated by the $NTF_{DAC}(f)$ in Fig. 3.5(a). Dual-path loop filter architecture was used in the context of analog PLLs [61–65] to set the integral and proportional path gains independently. In [60], dual-path was exploited to implement integral path in digital domain in a hybrid PLL architecture. Both these architectures are susceptible to static phase offset due to mismatch between integral and analog proportional paths. In our architecture, both proportional and integral paths are implemented digitally and are driven by the same TDC. This greatly reduces the phase offset between the two paths.

Using the dual-path DAC structure, where the filter poles are set at 1MHz and 10MHz, and a PLL BW of 5MHz, DAC quantization noise is greatly filtered well below VCO phase noise. This aggressive filtering also helps to reduce the impact of DAC non-linear errors as demonstrated in Fig. 3.5(b). Output phase noise of the proposed fractional-N PLL is plotted in Fig. 3.6, where it is now only dominated by VCO phase noise. The simulated

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output integrated jitter is about 1.65ps$_{rms}$. Further improvement in jitter performance is only possible by further increasing PLL BW at the expense of a higher reference frequency. Next, we will discuss the implementation details of the proposed extended range MMD and other key building blocks.

3.4   Extended Range Multi-Modulus Divider (MMD)

The proposed fractional-N PLL provides a wide range of output frequencies (2.0-5.5GHz) and can operate with a reference clock in a frequency range of 50MHz-100MHz. A programmable divider with a wide division range (20-110) is needed to achieve this. The pulse swallow divider architecture [66] can provide such a wide programmable division range [67] using a dual-modulus prescaler and two synchronous counters. However, it consumes high power as it relies on high speed synchronous counters. In [68], a multi-modulus divider (MMD) architecture was proposed, in which a series of divide-by-2/3 cells are connected similar to a ripple counter. The power consumption is reduced significantly because: (a) clock frequency scales down through the divider chain and (b) there is no need for any intermediate clock buffers. Further, the modular nature of the MMD also helps to minimize design time and to optimize layout floor-plan. The division range of MMD can be expressed as:

$$N = 2^0P_0 + 2^1P_1 + ... + 2^{n-1}P_{n-1} + 2^n \qquad (3.6)$$

where n is the number of divide-by-2/3 cells and P is the n-bit division control signal. The division range of this conventional MMD is limited to 2^n to $2^{n+1} - 1$ (e.g. for n = 6, division range is from 64 to 127), which is not sufficient for PLLs with a wide output range. The division range can be extended by deactivating the last stage using OR gates [54]. However, this approach is susceptible to erroneous division operation when the division factor is dynamically changed as is the case in a fractional-N PLL. For example, when division factor switches from 63 (5-stages) to 64 (6-stages), the six divide-by-2/3 stage needs to be activated back and forth. Under this condition, undefined state of the deactivated cell may cause fractional operation to fail. We further elucidate this particular issue next and

present an alternate MMD architecture to overcome it.
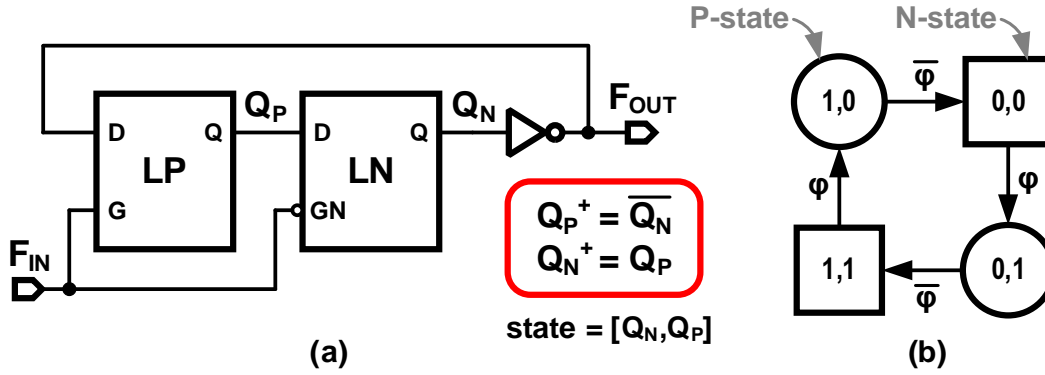
Figure 3.7: Divide-by-2 cell: (a) block diagram and (b) its associated state diagram.
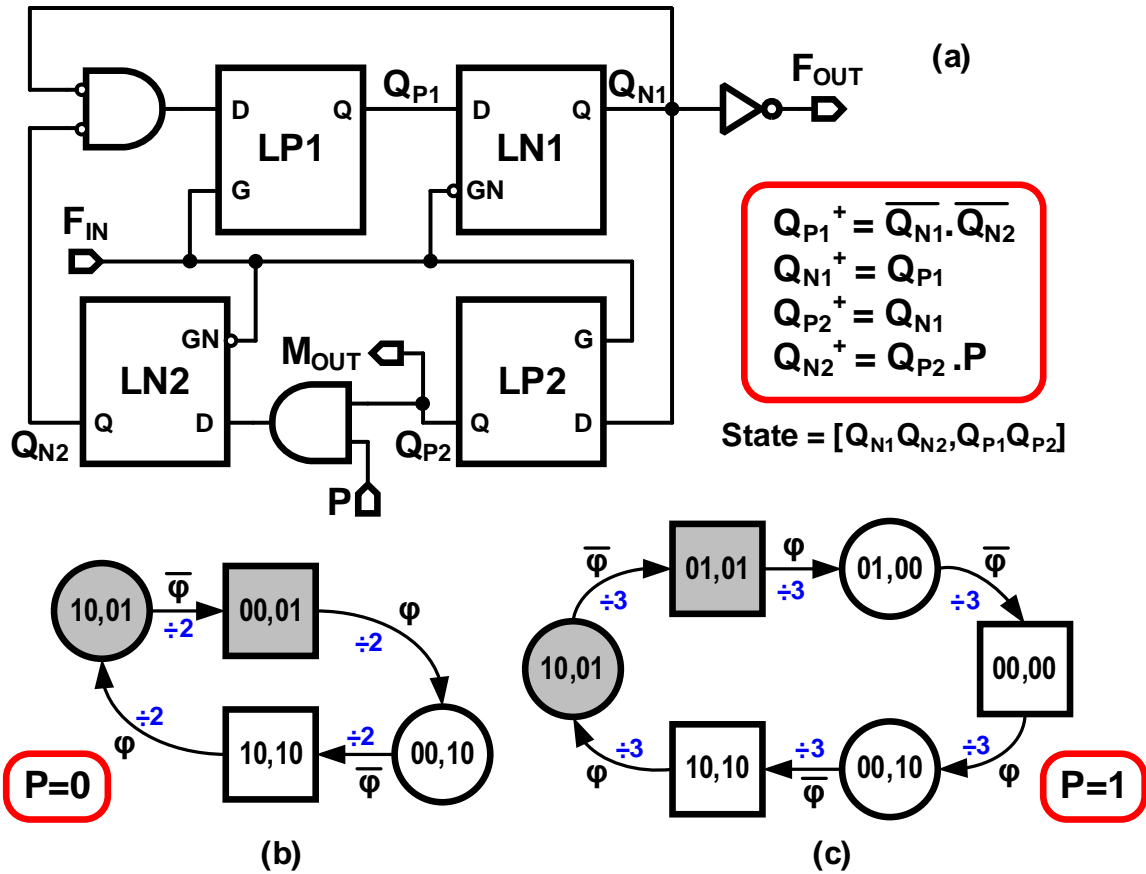
Figure 3.8: (a) Block diagram of a divide-by-2/3 cell. State diagrams: (b) in case of $P = 0$ and (c) $P = 1$.

To arrive at the proposed MMD architecture, it is interactive to first consider the operation of a standard divide-by-2 circuit shown in Fig. 3.7(a). It is composed of a positive D-latch

(LP) and a negative D-latch (LN) connected in a feedback configuration. The outputs of LP and LN latches are denoted by Q_P and Q_N, respectively. Each latch can be in zero, one, or transparent state, and the divider state, defined as $[Q_N,Q_P]$, is determined by the state of non-transparent latches [67, 69]. There are two P-states when clock is high (φ) and two N-states when clock is low ($\overline{\varphi}$). Input clock signal (F_{in}) triggers state transitions as illustrated in the state diagram of Fig. 3.7(b). Next states can be found using: $Q_P^+ = \overline{Q_N}$, and $Q_N^+ = Q_P$. The cycle repeats after four state transitions (i.e. two clock cycles) resulting in both Q_N and Q_P to represent a divide-by-2 clock output but with quadrature phase difference.

A basic divide-by-2/3 circuit depicted in Fig. 3.8(a) divides by 2 when the control signal P = 0, and by 3 when P = 1. The divide-by-2/3 circuit consists basically of two positive latches, namely LP1 and LP2, and two negative latches, namely LN1 and LN2. The latches' outputs are defined as Q_{P1}, Q_{P2}, Q_{N1}, and Q_{N2} and the divider state is defined as $[Q_{N1}Q_{N2},Q_{P1}Q_{P2}]$, where the next state is calculated using: $Q_{P1}^+ = \overline{Q_{N1}} \cdot \overline{Q_{N2}}$, $Q_{N1}^+ = Q_{P1}$, $Q_{P2}^+ = Q_{N1}$, and $Q_{N2}^+ = Q_{P2} \cdot P$. In case of P = 0, latch LN2 input is set to zero, and the circuit behaves as a standard divide-by-2 circuit. The output signal $M_{OUT} = Q_{P2}$, is just a delayed version of Q_{N1} (by half clock cycle). There are four allowed states; the shaded states represent states with $M_{OUT} = 1$. In case of P = 1, latch LN2 is active, Q_{N2} is a delayed version of Q_{N1} (one clock cycle). As a result, a slower feedback is added to the main feedback signal Q_{N2} using a NOR gate, and latch LP1 input is held zero for two clock cycles (as opposed to one). The state diagram is illustrated in Fig. 3.8(c), where division cycle repeats after six state transitions (i.e. three clock cycles). The output signal $M_{OUT} = 1$ represents a divide-by-3 clock with 33% duty cycle.

The divide-by-2/3 circuit used in MMD [54] has a modulus control (M_{IN}) as shown in Fig. 3.9(a). It uses an extra AND gate, such that it divides-by-3 only when both control inputs P and M_{IN} are high. The next state of LP2 is updated as: $Q_{P2}^+ = Q_{N1} \cdot M_{IN}$. When $M_{IN} = 0$, the lower feedback path is disabled and the circuit behaves as a divide-by-2 circuit (i.e. $F_{OUT} = F_{IN}/2$) and output signal M_{OUT} is set to zero. Fig. 3.9(b) shows a complete state diagram of the divide-by-2/3 circuit. It combines the state diagrams in Fig. 3.8 and adds an extra state $[Q_{N1}Q_{N2},Q_{P1}Q_{P2}]=[10, 00]=[2, 0]$ to account for $M_{IN} = 0$ case. By dynamically controlling M_{IN} signal, higher division factors can be realized by exploiting the inner loop

$$Q_{P1}^+ = \overline{Q_{N1}} \cdot \overline{Q_{N2}}$$
$$Q_{N1}^+ = Q_{P1}$$
$$Q_{P2}^+ = Q_{N1} \cdot M_{IN}$$
$$Q_{N2}^+ = Q_{P2} \cdot P$$

$$\text{State} = [Q_{N1}Q_{N2}, Q_{P1}Q_{P2}]$$

(a)

(b)
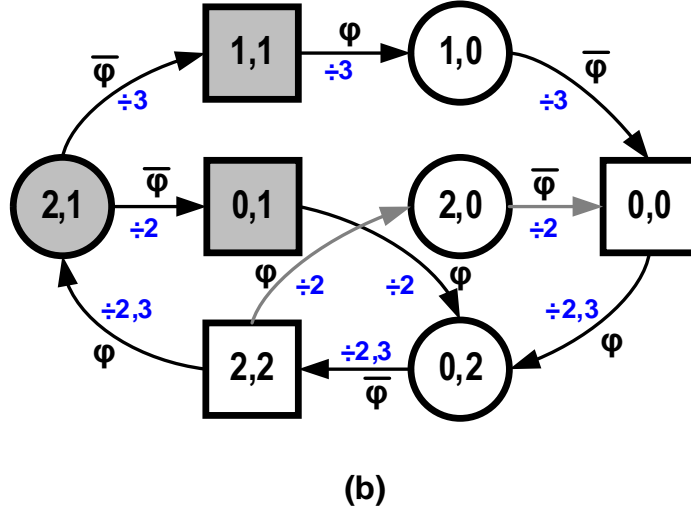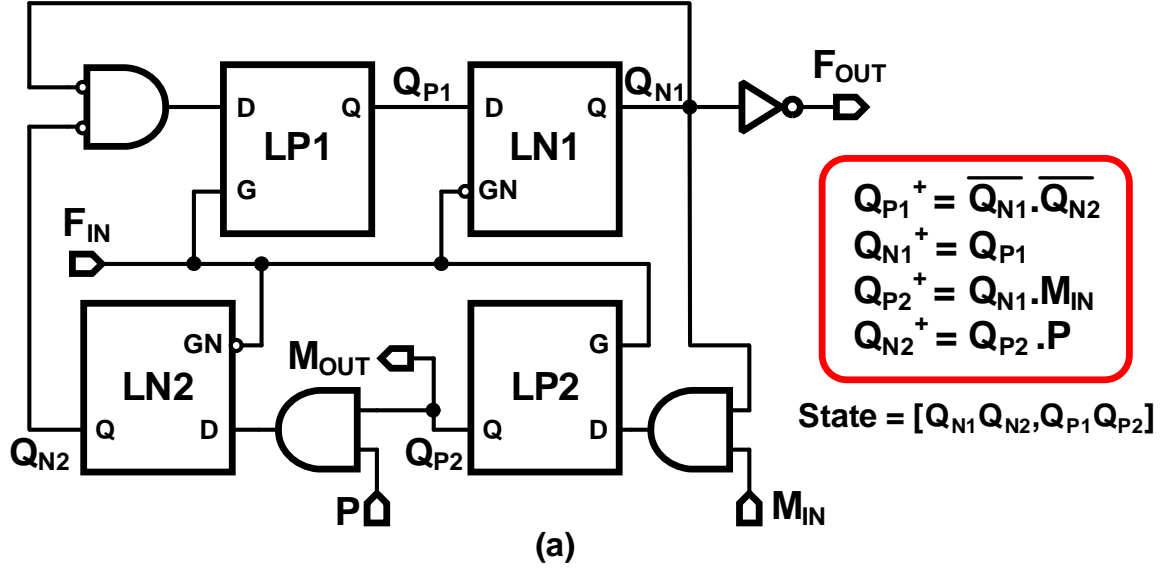
Figure 3.9: (a) Block and (b) state diagrams for a divide-by-2/3 cell with modulus control M_{IN}.

entailing states $[2, 0]$, $[0, 0]$, $[0, 2]$, and $[2, 2]$. Division range from 4 to 7 can be realized by cascading two divide-by-2/3 cells. To extend division range from 2 to 7, an OR gate is inserted to bypass the second stage [54] in case of divide-by-2 or 3 as shown in Fig. 3.10(a). In this case, MSB of the 3-bit control signal ($P_2 = 0$) sets the modulus control $M_1 = 1$. The detailed timing diagrams for division operations from 2 to 7 are shown in Fig. 3.11, where the states of both stages are highlighted around their input clocks (CLK_{IN} and F_1). For example, during divide-by-4 operation, control signal is ($P_2P_1P_0 = 100$) and the state
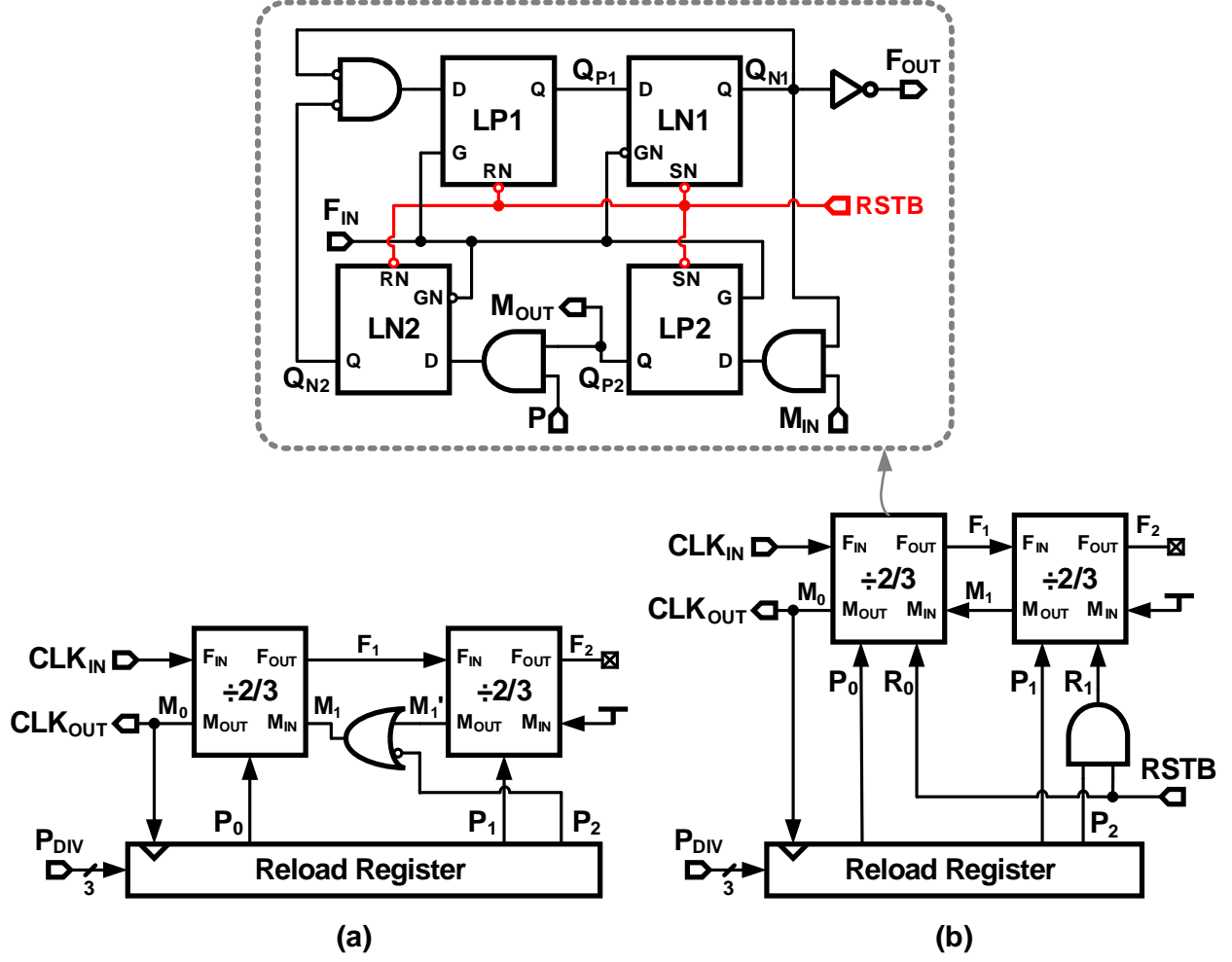
Figure 3.10: (a) Conventional two-stage extended range MMD, and (b) proposed two-stage extended range MMD with seamless switching.

transition path of first stage repeats with the following sequence: $[2,1]$, $[0,1]$, $[0,2]$, $[2,2]$, $[2,0]$, $[0,0]$, $[0,2]$, $[2,2]$.

In fractional-N PLLs, MMD division factor changes dynamically according to the output of $\Delta\Sigma$ modulator. Hence, it is critical to load the P-control signal on the positive edge, such that it remains fixed during the whole division operation as shown in Fig. 3.10(a). As mentioned earlier, when the division factor changes across extension boundaries (e.g. P changes from 3 to 4), the first division operation fails as illustrated by the timing diagram in Fig. 3.12(a). Because the bypassed second stage is dividing F_1 by 3, its state keeps changing and is not controlled each time extension is enabled. Therefore, modulus control signal M_1 changes incorrectly and starts the divide-by-4 operation from an unknown state ($[2,0]$ in
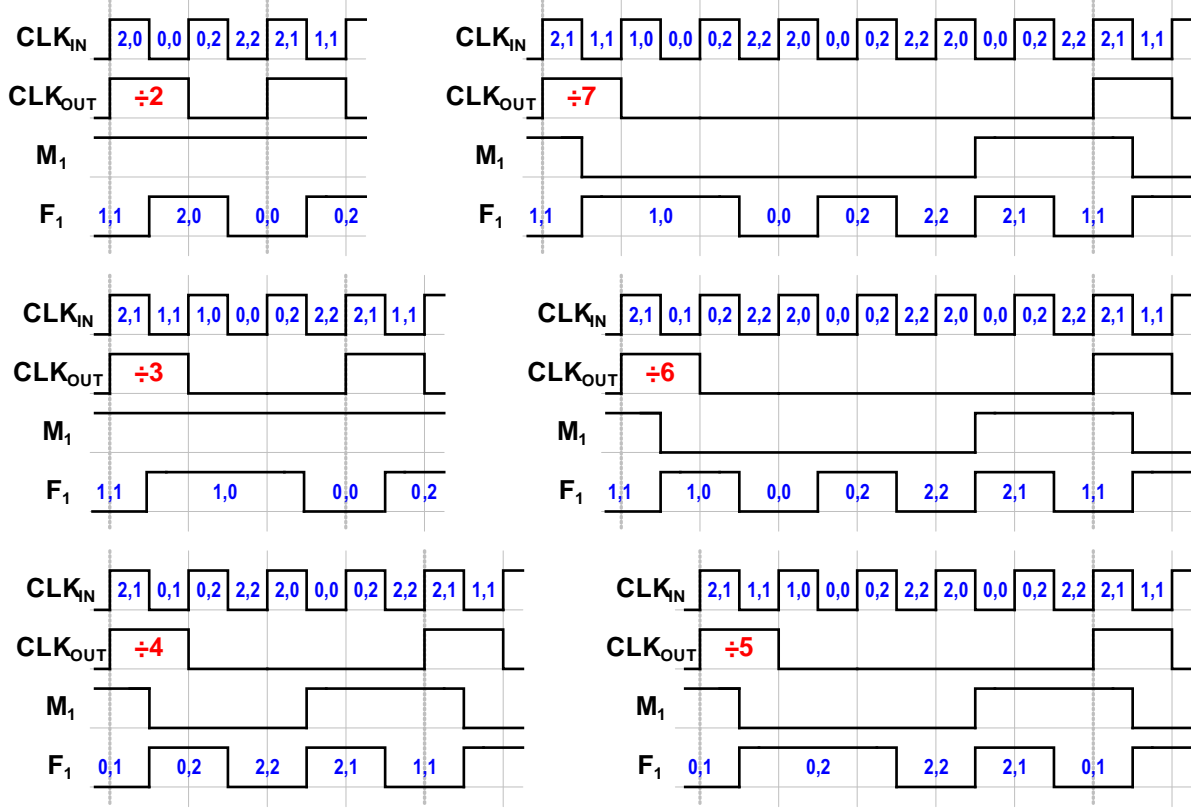
Figure 3.11: Timing diagrams of the two-stage MMD for different division operations from 2 to 7.

this example), instead of state $[2, 1]$. As a result, the first half of the divide-by-4 operation (i.e. two clock cycles) is bypassed, resulting in a glitch and effectively a wrong divide-by-5 operation.

By observing the second stage behavior during division operations from 4 to 7 (see Fig. 3.11), we identify that state $[2, 1]$, which indicates the start of division operation, is common to all four cases. This state resides before CLK_{OUT} goes high and the new P control factor is loaded. Therefore, when the second stage is bypassed, we resets its state to $[2, 1]$, so as to achieve seamless switching when the extension is enabled. The proposed MMD with a division range from 2 to 7 is shown in Fig. 3.10(b), where a reset port (RSTB) is added to deactivate the second stage when the lower division range (2 to 3) is used (RSTB = P_2). The same modified cell can also be used in the first stage to ensure that the first division operation on start-up is correct. Fig. 3.12(b) shows the timing diagram of the proposed MMD when the division factor is switched from 3 to 4. Now, the state of the second stage
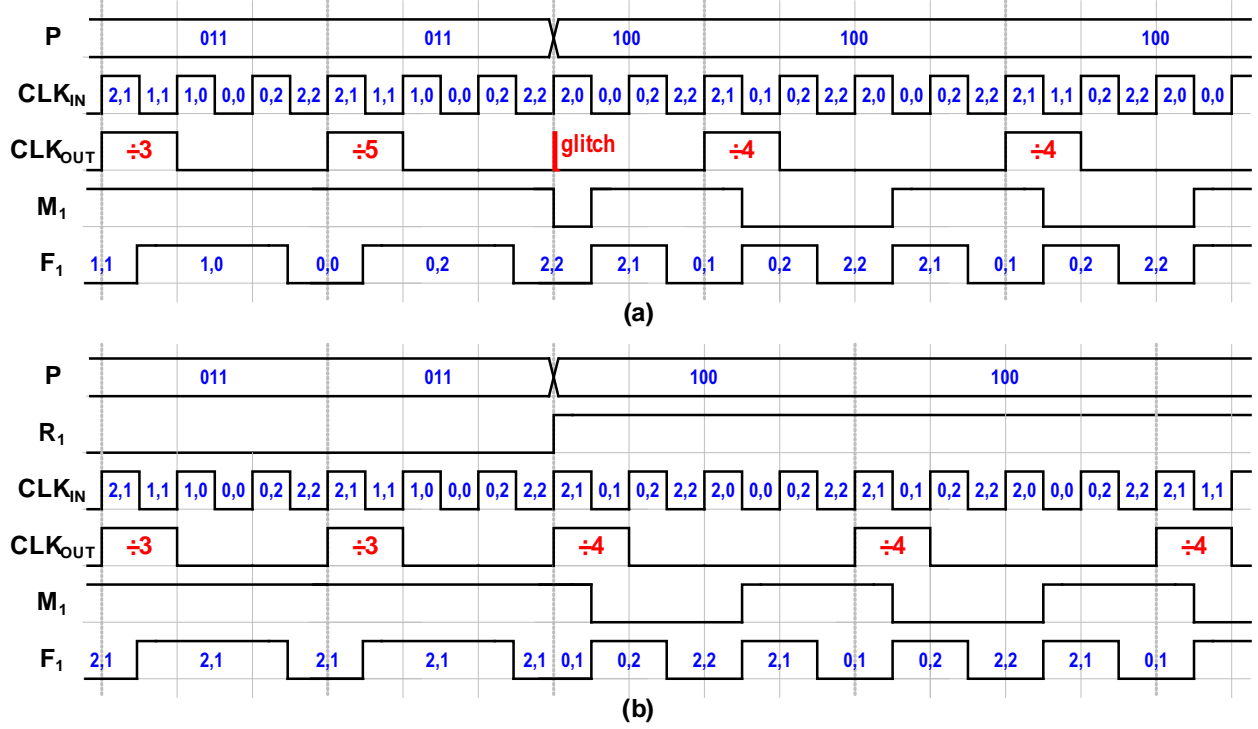
Figure 3.12: Timing diagrams of the two-stage MMD when division factor changes from 3 to 4 in case of (a) conventional MMD, and (b) proposed MMD with seamless switching.
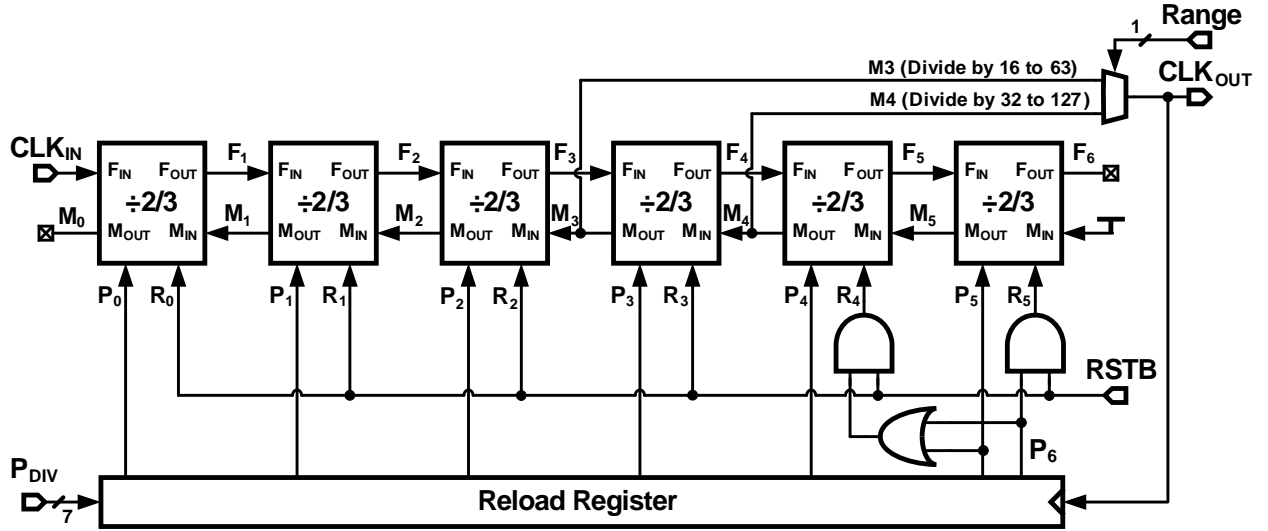
Figure 3.13: Detailed block diagram of the proposed MMD with seamless switching across a wide division range from 16 to 127.

remains fixed to $[2, 1]$ during the divide-by-3 operation. When P changes from 3 to 4, the second stage is activated (RSTB = 1) to perform a divide-by-2 operation. In this example, its state is changed to $[0, 1]$ as $P_1 = 0$ and to $[1, 1]$ if $P_1 = 1$ for divide-by-6 or 7 operation.

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Compared to solutions [69, 70] that use multiplexers and extra logic to ensure seamless switching across only one extension boundary, the proposed solution has minimum added hardware and can be generalized to realize seamless operation across multiple extension boundaries. Fig. 3.13 shows a detailed block diagram of the proposed extended range MMD. It is composed of six divide-by-2/3 cells with a reset port plus extension control logic with a reload register. It is crucial to use proper clock signal to update the new P control factor as described before. Therefore, for a division range from 16 to 63, the fifth stage can be switched back and forth, and the modulus M_3 clock is used to reload the new P control factor. The modulus M_4 clock is used for a division range from 32 to 127. A 2x1 multiplexer is used to select the output clock according to the required range. The MMD operates with an input clock frequency of up to 6GHz, where the first divide-by-2/3 cell is implemented using true single phase clocked (TSPC) DFFs to reduce the power consumption, while the other five cells are implemented using standard-cell CMOS latches.

3.5 Building Blocks

3.5.1 Digitally Controlled Ring Oscillator (DCRO)

The schematic of the proposed split-tuned digitally controlled ring oscillator (DCRO) is shown in Fig. 3.14. The ring-VCO core is composed of four pseudo-differential delay cells. Each delay cell is implemented using two current-starved CMOS inverters with a resistor feed-forward coupling (R_F) for differential operation. The current drawn by the delay cells combines the proportional and integral paths to control the oscillator frequency. For the fast proportional path, the 15-level thermometer-coded TDC output (D_P) directly controls the DCRO frequency through a 4-bit current-mode DAC_P. The cell current can be varied to control the PLL bandwidth. The 14-bit accumulator output, D_I, of the slow integral path is truncated to 5-bits using a second order error-feedback based digital $\Delta\Sigma$ modulator. The output of $\Delta\Sigma$ modulator is converted to 31-levels thermometer-code to minimize the differential non-linearity (DNL) of the 5-bit current DAC_I. Unit cells in the DAC are sized to improve static linearity, while adding a DFF in each cell and matching clock routing

improves dynamic linearity. The output control current of DAC_I is converted to voltage by programmable resistor R_1, where the voltage control range is maximized. The frequency range of the integral control has to be large enough to maintain DPLL lock across temperature variations. At 5GHz, simulation results show the VCO frequency varies about 300MHz (6%) as temperature changes from $-40°C$ to $125°C$. The current source transistor M_1 is sized to realize a large K_{VCO} of 1GHz/V to maintain lock across temperature. A third order low pass filter with the third pole located at the drain of current source transistor, M_1, suppresses the shaped quantization error. The bandwidth of the third order low pass filter of the integral path can be lowered aggressively to less than 1MHz with no stability concerns even for a wide DPLL bandwidth of $F_{REF}/10 = 5MHz$.
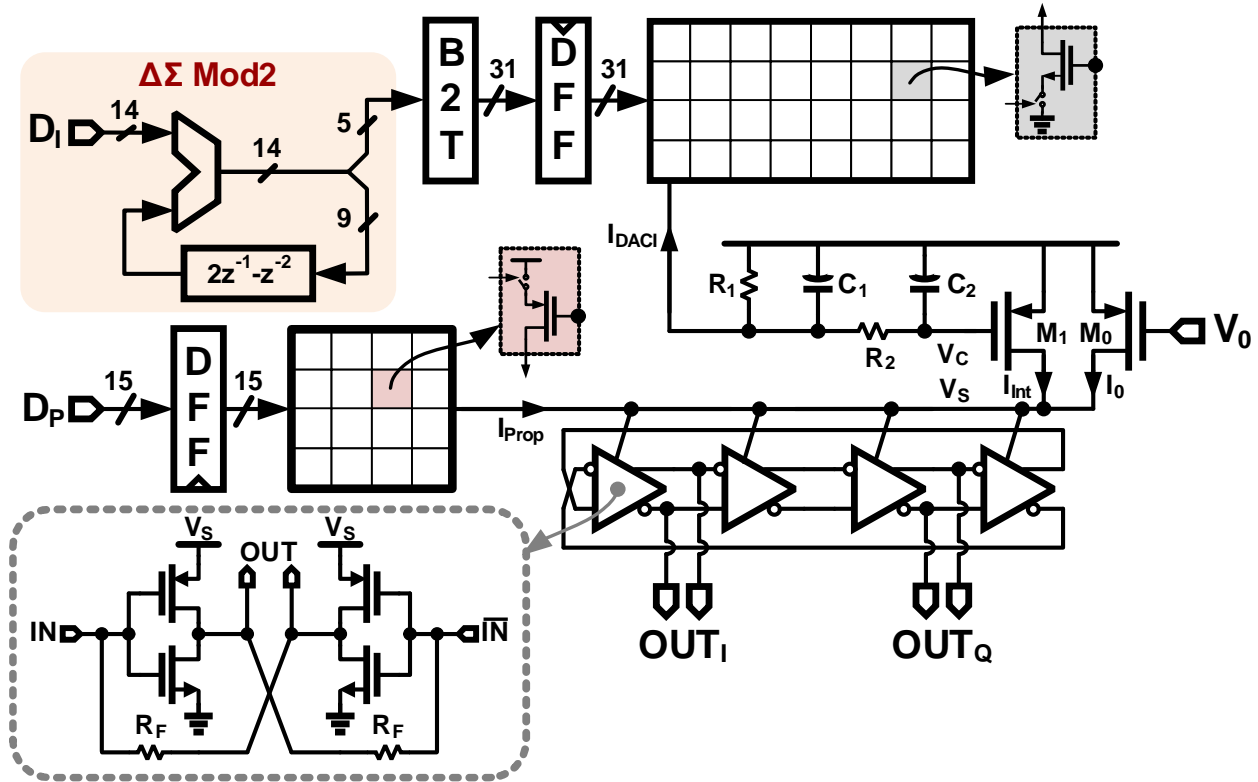
Figure 3.14: Schematic of the digitally controlled ring oscillator (DCRO) with dual-path control.
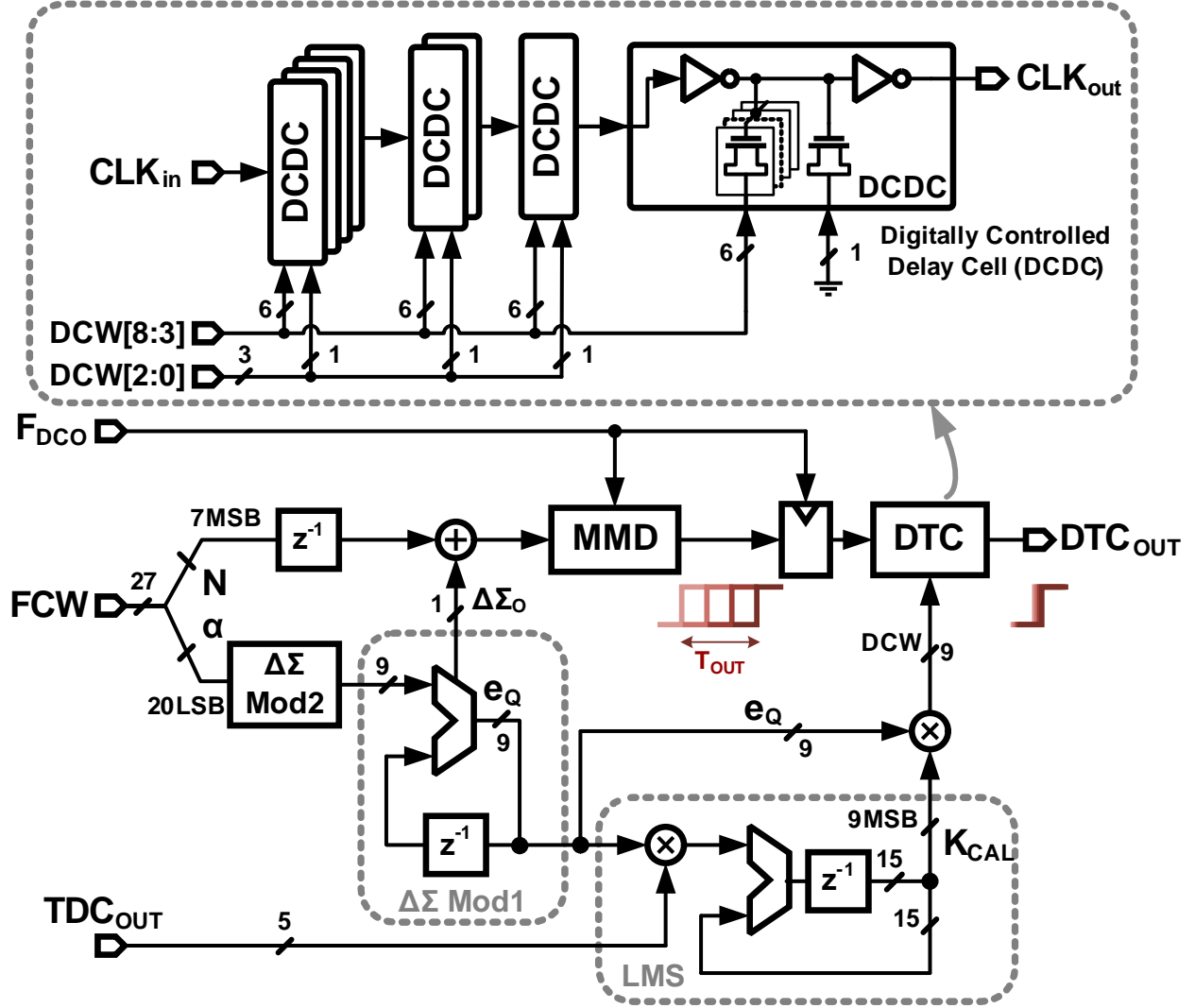
Figure 3.15: Implementation details of the fractional divider with LMS calibrated DTC quantization noise cancellation scheme.

3.5.2 Fractional Divider

The detailed implementation of the fractional divider is shown in Fig. 3.15. The output frequency is controlled using a 27-bit input frequency control word (FCW), where the 7-MSBs represent the integer part (N) and the remaining 20-LSBs denote the fractional part (α) of the division ratio, $N + \alpha$. The 20-bit fractional bits are truncated to 9-bits using a second order $\Delta\Sigma$ modulator, which is implemented using an error-feedback architecture. A 15-bit linear feedback shift register (LFSR) generates a dither signal that can be added to the LSBs. The 9-bit $\Delta\Sigma$ output drives an accumulator that acts as a first order $\Delta\Sigma$ modulator, where the

accumulator carry, $\Delta\Sigma_O$, is added to the integer control (N) to control the MMD. As a result, MMD is dithered between N and $N+1$ such that the average division ratio is $N+\alpha$. The error resulting from truncating 20-bits to 1-bit, denoted as e_Q, appears as phase quantization error at the output of the MMD. The accumulator sum represents the quantization error signal, e_Q, which is converted to an equivalent phase quantization error using a DTC to realize a QNC scheme in time domain [9, 53]. The gain of DTC is PVT-sensitive and is calibrated using a background LMS algorithm based on the correlation between TDC_{OUT}, which contains residual e_Q, and e_Q itself [9]. The 9-bit DTC is implemented using an 8-stage digitally controlled delay line (DCDL), with a 0.5ps resolution, similar to the one in [27, 53].
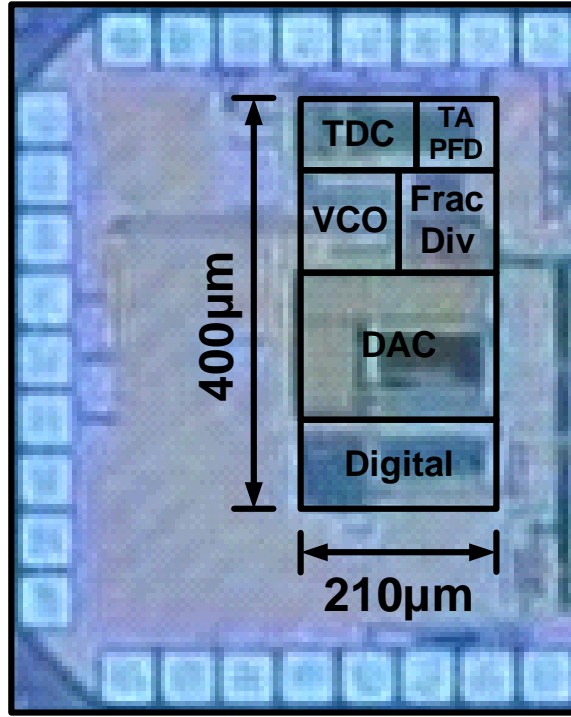
Figure 3.16: Die photograph.

3.6 Measurement Results

A prototype ring-based digital FNPLL was fabricated in 65nm CMOS process and its die photograph is shown in Fig. 3.16. It occupies an active area of 0.084mm^2. A standard 50MHz external crystal oscillator was used to provide a reference clock that has about
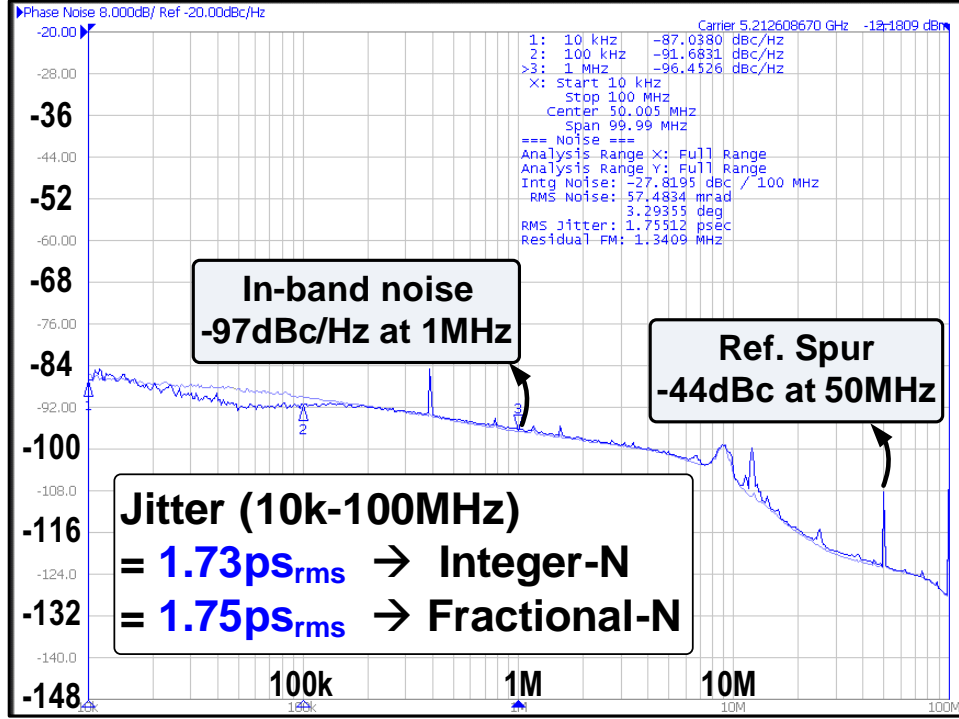
Figure 3.17: Measured phase noise at 5.2GHz output frequency for integer-N and fractional modes.

0.8ps$_{rms}$ measured integrated jitter from 10kHz to 20MHz and a noise floor of -147dBc/Hz. The output frequency can be tuned from 2.0GHz to 5.5GHz using a 27-bit FCW, with an approximate frequency resolution of 50Hz. At 5GHz output frequency, the total power consumption is less than 4mW at a supply voltage of 0.9V, while at 2.5GHz the FNPLL consumes about 1.35mW from a supply voltage of 0.7V. The chip is characterized using Agilent N9000A spectrum analyzer (SA) and Agilent E5052B signal source analyzer (SSA). The measured phase noise of the digital FNPLL at 5.2GHz is shown in Fig. 3.17. With a wide bandwidth of 5MHz, integrated jitter from 10kHz to 100MHz is about 1.75ps$_{rms}$ in both integer and fractional-N modes, while the reference spur is about -44dBc. The relatively high reference spur is attributed to the wide BW and the reduced filtering in the proportional path. An in-band phase noise of -97dBc/Hz is achieved at 1MHz offset. To illustrate effectiveness of DTC-based quantization noise cancellation, digital FNPLL phase noise is measured with and without DTC calibration. When DTC calibration is turned off, $\Delta\Sigma$ quantization noise is not completely cancelled and the residual error saturates the

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narrow range TDC. This dramatically increases in-band phase noise resulting in an increase of integrated jitter from 1.8ps_{rms} to about 8.9ps_{rms}.
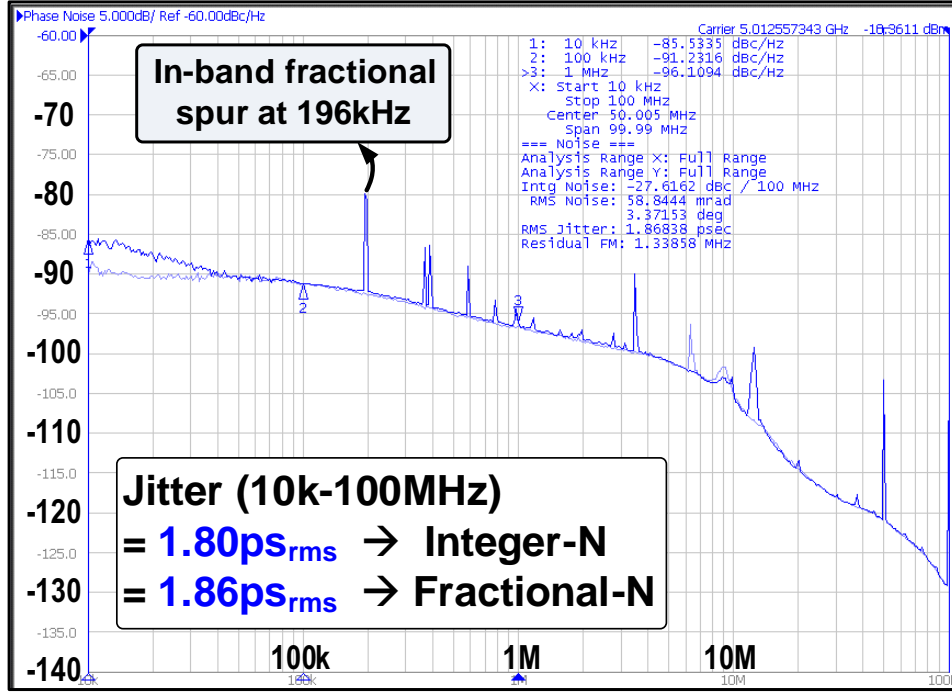
Figure 3.18: Measured phase noise at 5GHz output frequency with in-band fractional spur at 196kHz offset.

The measured phase noise at 5GHz with in-band fractional spurs is shown in Fig. 3.18. Fig. 3.19 shows the measured output spectrum where the worst case fractional spur is less than -41.6dBc at 196kHz fractional offset frequency. Measured fractional spur and integrated jitter are plotted as a function of output fractional frequency offset in Fig. 3.20. This indicates a worst-case jitter of less than 1.9ps_{rms}. Fig. 3.21 shows the measured phase noise for two different BW settings at 5GHz output. The bandwidth is controlled by changing the proportional DAC$_P$ current. In case of a narrow BW setting of 0.3MHz, phase noise is dominated by the VCO resulting in a relatively high integrated jitter of 3.45ps_{rms}. On the other hand, an excellent jitter of 1.85ps_{rms} is achieved with a wide BW setting of 6MHz (around F$_{REF}$/8). No jitter peaking or limit cycle behavior was observed. Measured integrated jitter, plotted as a function of loop bandwidth in Fig. 3.22, illustrates that greater than 3MHz bandwidth is needed to achieve integrated jitter <1.9ps_{rms}.

The performance summary and comparison with state-of-the-art ring-based digital FN-
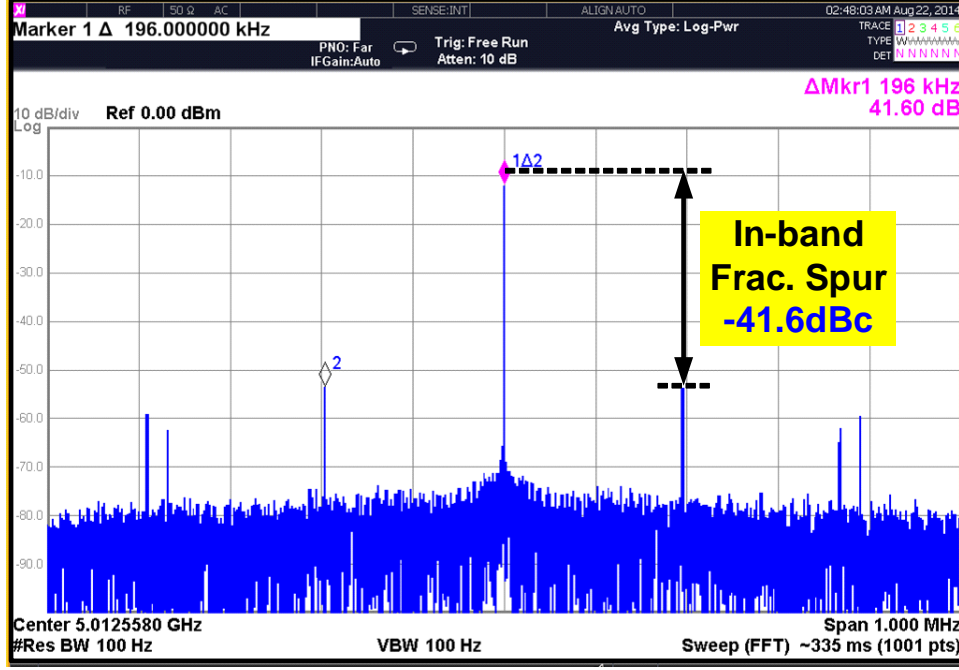
Figure 3.19: Measured output spectrum at 5GHz output frequency and 196kHz fractional offset.

PLLs are shown in Table 3.1. The proposed architecture achieves the lowest normalized in-band noise by about 21dB. It achieves the best-reported jitter performance of 1.9ps$_{rms}$, along with the best power efficiency of 0.8mW/GHz. This work achieves performance comparable to LC-based FNPLLs while maintaining the merits of ring VCOs. As shown in Fig. 3.23, the proposed digital FNPLL achieves the best FoM$_J$ of -228.5dB that reflects jitter and power trade-off. It also outperforms the best reported ring-based analog FNPLL [71] by about 3dB, while occupying 8x less area.

3.7 Conclusion

Ring-based digital FNPLL clock generation offers several advantage in area sensitive applications such as multi-core processors, chip-to-chip I/O interfaces, and SoCs platforms. Ring oscillators are extremely low-cost, compact, scalable, and can inherently provide multiple phases with a wide tuning range, but they suffer from poor phase noise performance. In this chapter, we developed PLL bandwidth extension techniques to suppress ring VCO phase

Table 3.1: Ring-based Digital FNPLL Performance Summary

	Chen [46] JSSC'10	Grollitsch [47] ISSCC'10	Li [40] ISSCC'12	Jang [48] ISSCC'13	Liu [49] ISSCC'14	Tsai [72] ISSCC'15	This Work	
Technology [nm]	65	65	22	28	20	16	65	
Freq. Range [GHz]	0.6-0.8	0.3-4.0	0.6-3.6	0.032-2.0	0.8-1.6	0.25-4.0	2.0-5.5	
Ref. Freq. [MHz]	26	25	25-200	30	25	200	50	
Supply [V]	1.1-1.3	1.1/1.3	1	1	0.9	0.52-0.8	0.7	0.9
Power [mW]	3.2	9.3	18.4	5.3	3.1	9.3	1.35	4
Out Freq. [GHz]	0.8	3.0	3.2	2	1.6	3	2.5	5
Bandwidth [MHz]	1	0.7	0.003-4	4	4	2	5	5
In-band PN [dBc/Hz]*	-72.1	-74.6	-63.6	-75.7	-74.1	N/A	-91.5	-97
Integrated Jitter [ps$_\text{rms}$]	21.5 (1k-100MHz)	13.5 (1k-20MHz)	10 (N/A)	19.3 (20k-40MHz)	28 (20k-40MHz)	3.3 (10k-1GHz)	3.6	1.9 (10k-100MHz)
FoM$_J$ [dB]	**-208.3**	**-207.7**	**-207.4**	**-207**	**-206.1**	**-219.8**	**-227.6**	**-228.5**
Power Eff. [mW/GHz]**	4	3.1	5.1	2.65	1.94	3.1	0.54	0.8
Area [mm^2]	0.027	0.038	0.03	0.026	0.012	0.029	0.084	

* Normalized In-band PN to 5GHz,   **FoM$_J$ = $10\log\left[\left(\frac{\sigma_\text{rms}}{1\text{sec}}\right)^2 \cdot \frac{P}{1\text{mW}}\right]$
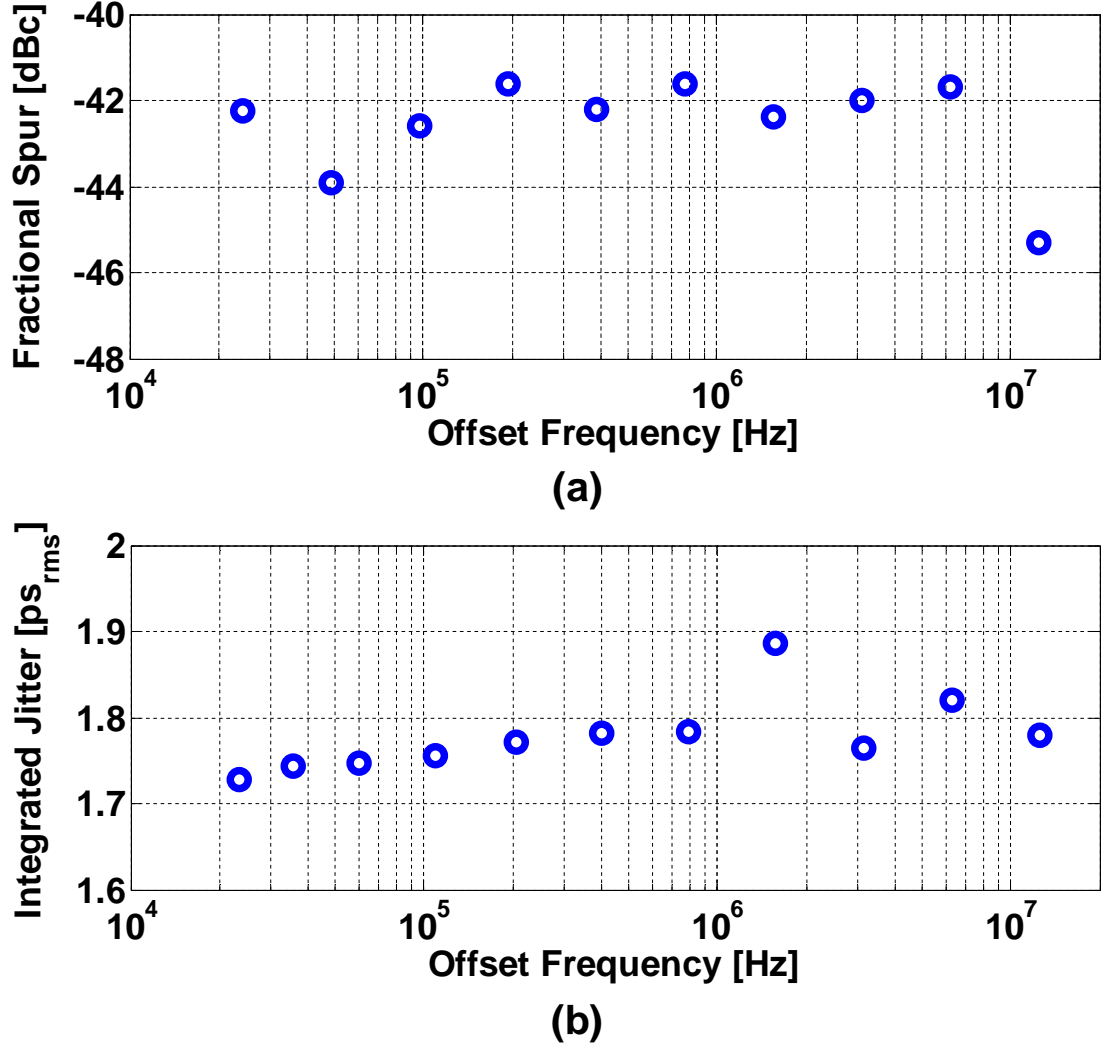
Figure 3.20: (a) Measured fractional spur and (b) rms integrated jitter as a function of output fractional frequency offset.

noise to leverage its merits, while achieving performance close to LC-based PLLs. A low power, wide bandwidth ring-based digital FNPLL with excellent jitter performance and wide output frequency range is demonstrated. It employs a 9-bit DTC-based fractional divider that alleviates TDC dynamic range requirements and a low power, high resolution 4-bit TDC to achieve low in-band phase noise. A dual-path loop filter architecture is used to suppress DAC noise and minimize loop latency. A modified extended range multi-modulus divider (MMD) is proposed that enables seamless switching at extension range boundaries. As a result, a wide output frequency range is realized at low power consumption. The mea-
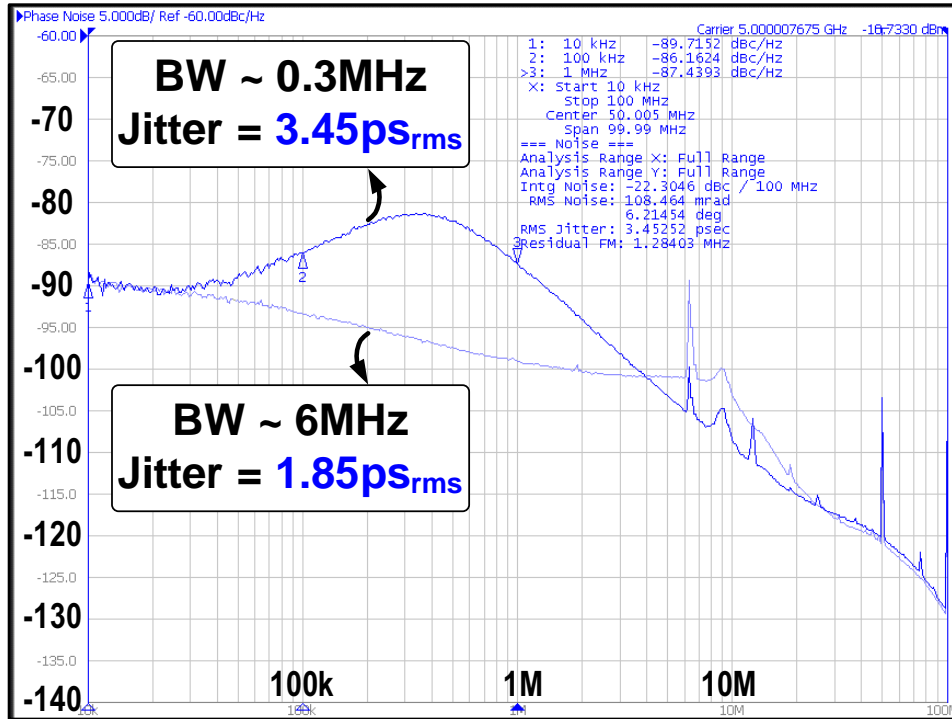
Figure 3.21: Measured phase noise for narrow (0.3MHz) and wide (6MHz) BW settings at 5GHz output using 50MHz reference.
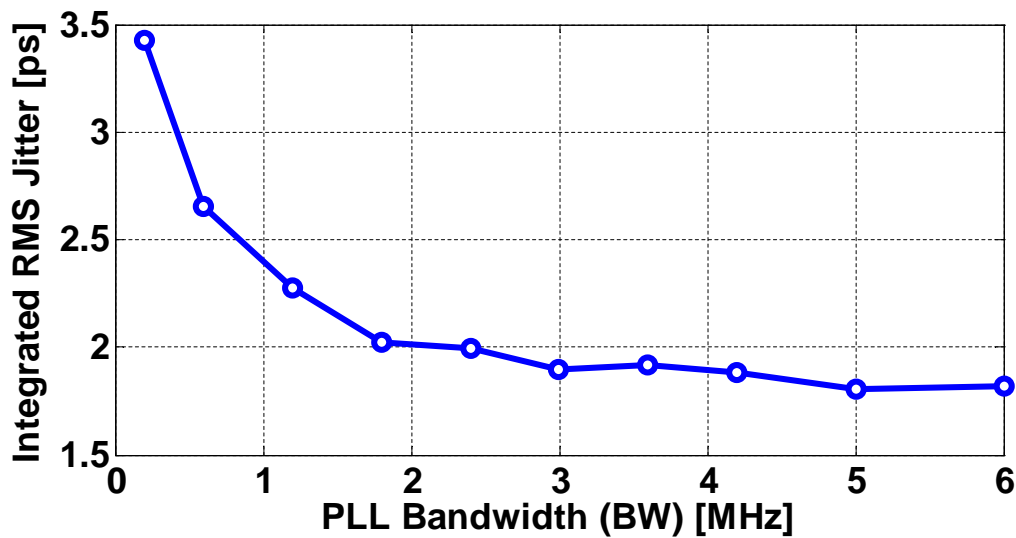
Figure 3.22: Measured rms integrated jitter across different bandwidth settings at 5GHz output frequency.

sured results indicate an excellent jitter performance, low in-band phase noise, and wide PLL bandwidth of $F_{REF}/8$ with no limit cycles.
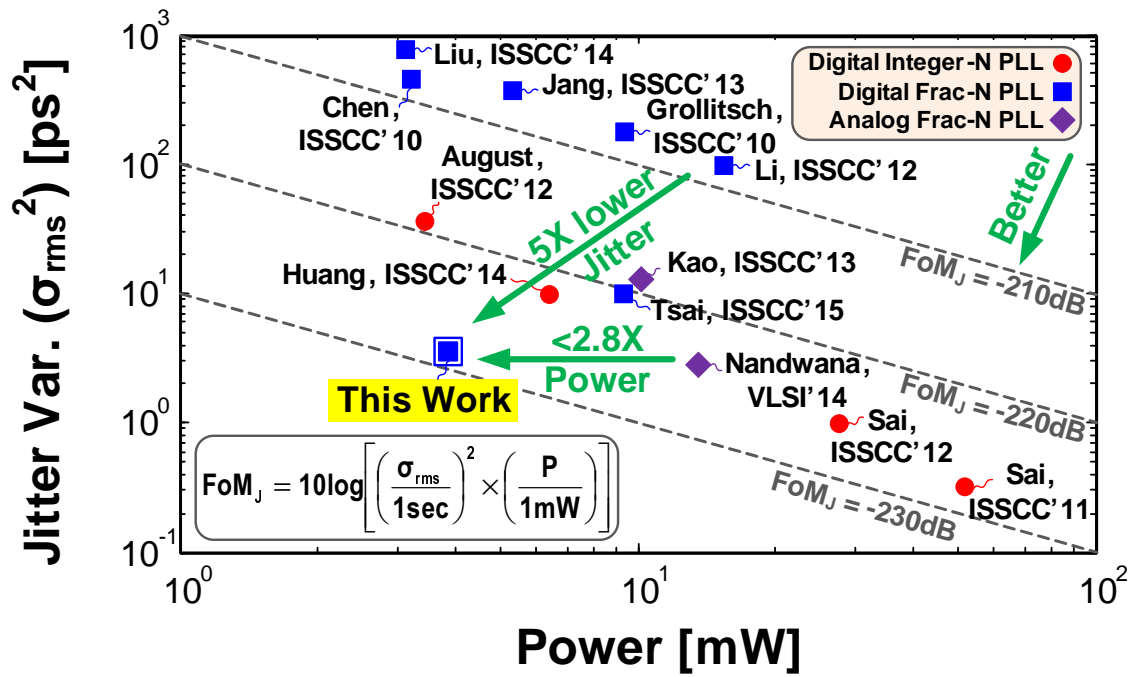
Figure 3.23: FoM$_J$ comparison.

CHAPTER 4

LOW JITTER OPEN LOOP FRACTIONAL DIVIDERS

4.1 Introduction

Advanced systems-on-chips (SoCs) perform many diverse analog, digital, mixed-signal, and often radio-frequency (RF) functions. A single SoC may include a wide variety of modules such as multicore processors, memories, I/O interfaces, power management, and wireless transceivers [73]. Each of these modules has its own clock domains with specific requirements. For example, I/O interfaces require low jitter high frequency clocks, while core-clocking of a processor may require spread spectrum clocking (SSC) to reduce electromagnetic interference (EMI) or using dynamic frequency scaling (DFS) to save power. Integer-N phase locked loops (PLLs) are usually used in I/O interfaces to meet the tight constraints on the clock jitter for various standards [43]. Recently, there is a growing demand for multi-standard-compliant transceivers integrated into a single chip with a wide and continuous range of data-rates [43, 45]. To save the cost of multiple input crystal references, fractional-N frequency synthesis is highly desirable in both the transmitter and the receiver [45]. As discussed in Chapter 3, a flexible fractional-N clock generator has to cover wide frequency range with fine frequency resolution to serve various standards. It has to provide multiple phases with stringent jitter performance with minimum power and area.

Fractional-N PLLs are also commonly used in multicore processor clocking [1, 40] for flexible frequency scaling and spread spectrum modulation. The DFS technique trades off power with performance [74, 75], based on the observation that processors rarely operate at their peak utilization levels. For flexible power management, dynamically adjustable, per

core clock generators are highly desirable [1]; this imposes tight power and area constraints in the clock generator design. For an effective DFS, frequency control has to be adaptive and on-the fly according to the utilization levels. The clock frequency has to be dynamically switched, while the core is executing with no glitches and without skipping any cycles [75]. No undershoots are allowed in frequency switching events to prevent timing hazards and usually a controllable frequency slew rate is used to limit the power supply drop caused by di/dt [1]. Proper behavior of clock frequency during frequency switching is challenging because of the closed loop nature of PLLs.

The increased complexity of SoCs results in an increased concern of the EMI, produced by high-speed digital clock drivers and the associated circuitry [76]. Spread spectrum clocking (SSC) is a widely used, cost effective, technique to reduce the EMI level due to I/O interfaces [77] and multicore processors clocking [40, 73]. The clock energy is spread over a given bandwidth by frequency modulation of the clock with a predefined modulation profile [78]. A fractional-N PLL is usually used to generate SSC by digitally modulating the $\Delta\Sigma$ feedback divider. However, this approach suffers from distortion of the frequency modulation profile because of the restricted PLL bandwidth. As a result, the reduction in EMI level is limited.
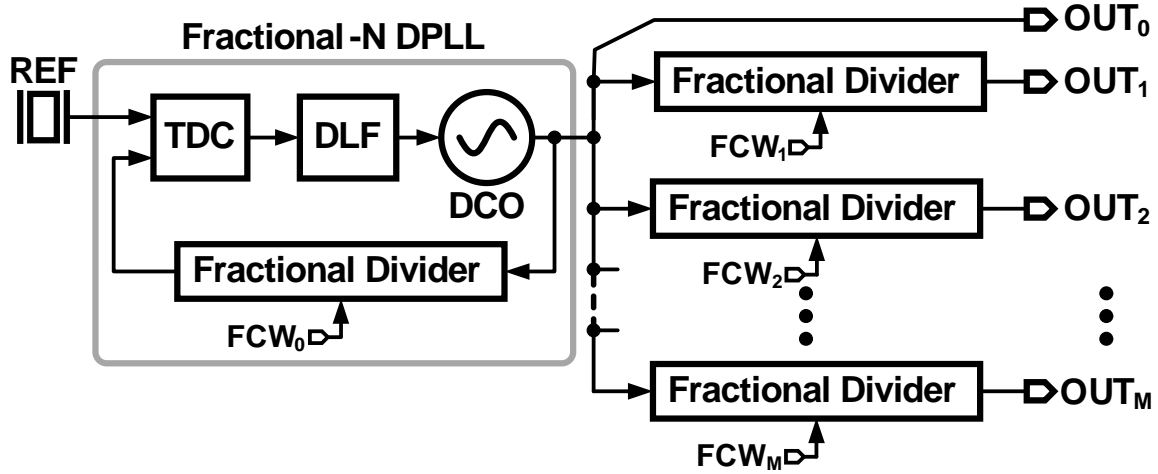
Figure 4.1: Block diagram of the proposed multi-outputs all-digital clock generation unit using open loop fractional dividers.

In this chapter, we propose an all-digital clock generation unit (CGU) to overcome the aforementioned limitations. Fig. 4.1 shows the block diagram of the proposed CGU, where
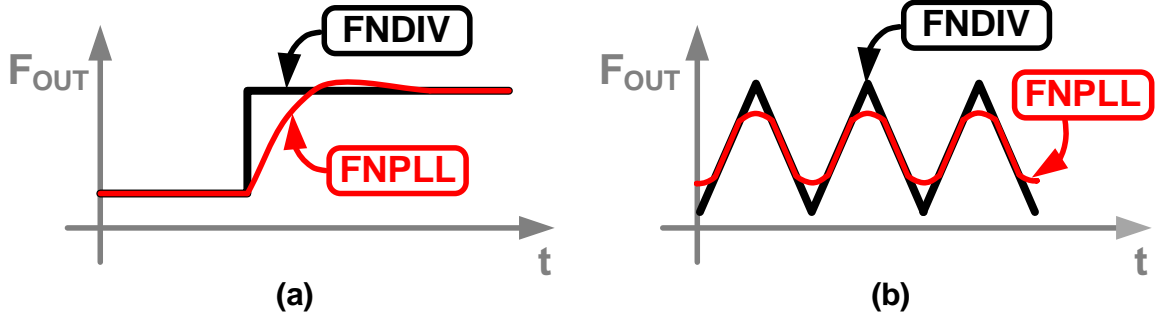
Figure 4.2: Time-domain illustration comparing the proposed fractional divider to a conventional FNPLL in case of (a) instantaneous frequency switching, and (b) spread spectrum modulation.

multiple novel open loop fractional dividers (FDIVs) use a low jitter high frequency clock from a ring-based digital FNPLL to generate multiple independent output clocks with a frequency range of 20-1000MHz [27]. The open loop architecture overcomes the bandwidth limitation in fractional-N PLLs. The proposed open loop FDIV can switch the output frequency instantaneously, compared to a slow settling behavior in FNPLLs, as depicted in Fig. 4.2(a). Moreover, the FDIV provides an excellent spread spectrum performance, where precise and programmable modulation depth and frequency can be applied to satisfy different EMI requirements. The FDIV has unlimited modulation bandwidth, unlike FNPLL, resulting in spread spectrum modulation with no filtering, as demonstrated in Fig. 4.2(b). The rest of the chapter is organized as follows. The proposed open loop FDIV is presented in section 4.2. The circuit implementation of critical building blocks is illustrated in section 4.3. The measured results from the test chip are shown in section 4.4. Finally, the key contributions of this chapter are summarized in section 4.5.

4.2 Open Loop Fractional Synthesis

4.2.1 Prior-Art

In fractional-N PLLs, the feedback division ratio is alternated dynamically (e.g. $N/N + 1$) such that effectively a fractional division is achieved. The PLL loop dynamics helps to filter out the quantization noise of this dithering process. Open loop frequency synthesis and

modulation techniques were proposed to mitigate the modulation bandwidth limitation of the closed loop system of fractional-N PLLs [79–81]. Fractional-N synthesis can be realized by dynamically selecting the right clock phase among M-clock signals $[p_1, p_2, ..., p_M]$ that have the exact same frequency (F_O) but with different phases equally spaced by $2\pi/M$ [rad]. A digital phase accumulator uses the fractional frequency control word (FCW_F) to generate precisely the phase control sequence of the phase multiplexor to realize a fractional part (α) as illustrated in Fig. 4.3(a). The resolution of this fractional synthesis depends on the number of available phases (M), hence the output period of the phase switching modulator equals to $T_O \cdot (1 + \alpha)$. For example, when M = 16 and $\alpha = 1/16$ the phase multiplexor is controlled according to the following cyclic sequence: $[p_1, p_2, ..p_M, p_1, ..]$. The multiple clock phases are usually generated using an integer-N PLL with ring oscillators [79]. Multiple clock phases can be also generated using standard quadrature generation techniques [81], which can be followed by phase interpolators to enhance resolution [24, 82].

The non-linearity of the digital-to-phase conversion degrades the spurious and phase noise performance of the output. The VCO delay cells and the routing paths have to be precisely matched to minimize performance degradation. The need to drive multiple high frequency clocks significantly increases the power consumption of this approach. Furthermore, the fractional frequency resolution is limited by the phase resolution and practically insufficient to produce an appropriate modulation signal. Using a digital $\Delta\Sigma$ modulator to drive the phase accumulator, a finer frequency resolution can be achieved [81], as shown in Fig. 4.3(b). The $\Delta\Sigma$ modulator shapes the quantization error, which can be filtered from the power amplifier (PA) output filter in wireless transmitter applications [81]. However, this filtering may not be sufficient or available for many applications. In [82], a quantization noise cancellation (QNC) technique is proposed by directly modulating the VCO of the multi-phase clock generator to precisely cancel the shaped quantization error as depicted in Fig. 4.3(c). Consequently, open loop modulation and low phase noise performance can be achieved simultaneously. However, it requires relatively accurate knowledge of the VCO gain (K_{VCO}) for perfect QNC; therefore, it can be sensitive across PVT variations. Besides, this approach cannot provide multiple independent outputs, as the multi-phase clock generator cannot be shared anymore.
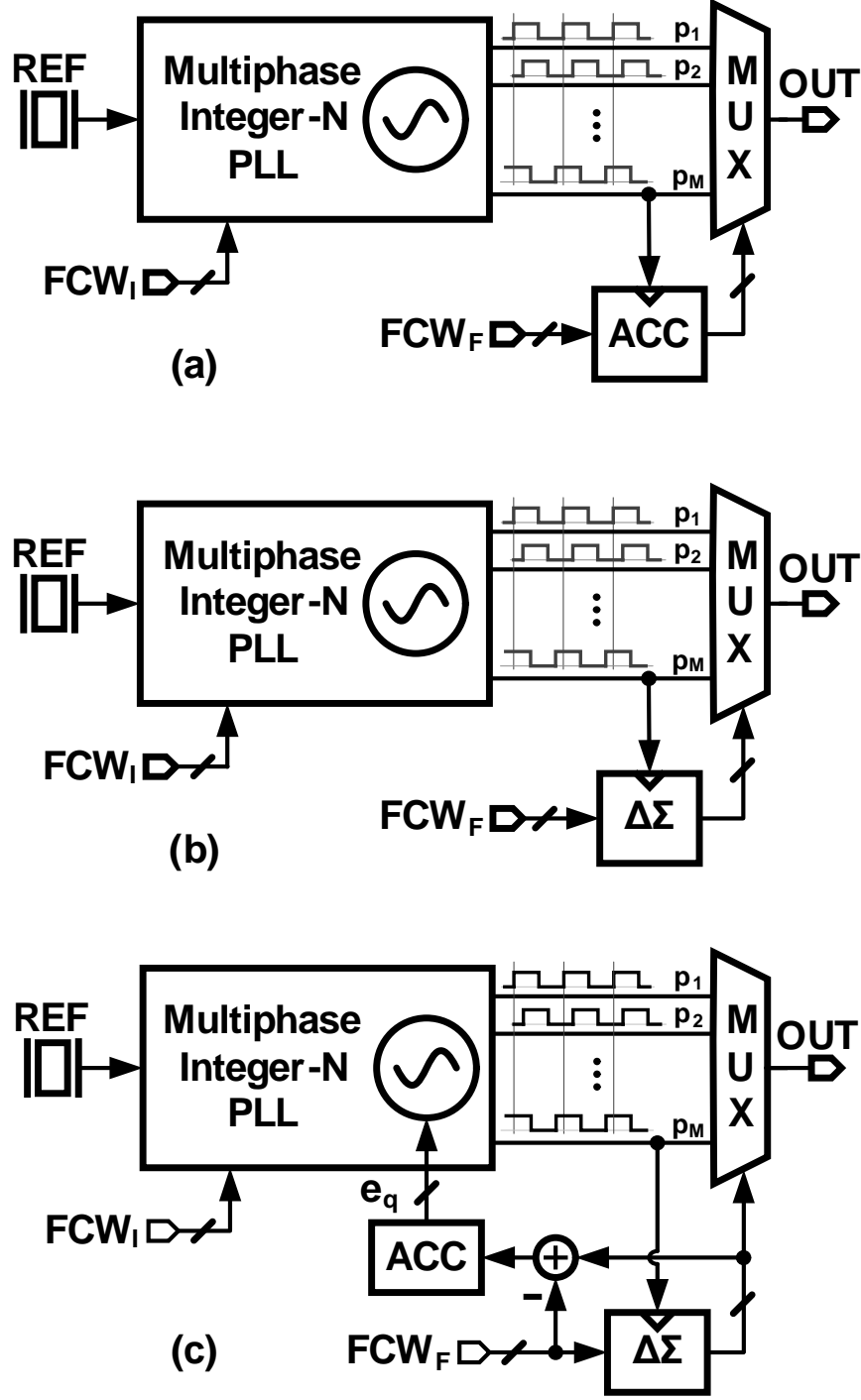
Figure 4.3: Block diagram of open loop fractional-N synthesizers using (a) phase switching, (b) $\Delta\Sigma$-based phase switching, and (c) $\Delta\Sigma$-based phase switching with VCO-based QNC.

4.2.2 Proposed Open Loop Fractional Divider

A conventional $\Delta\Sigma$ fractional divider (FDIV), in its simplest form, consists of a first order $\Delta\Sigma$ modulator controlling a dual modulus divider $(N/N+1)$. For example, if the divider

divides by 4 three times, then divides by 5 only one time, an average division ratio of 4.25 is achieved. However, due to the open loop behavior, the truncation error ($e_q[k]$) introduced by the $\Delta\Sigma$ modulator is not filtered and it directly appears as an output jitter as illustrated by the timing diagram in Fig. 4.4. The resulting jitter is deterministic and can be as large as one input period (T_{IN}). By comparing the output clock to an ideal clock, $0.25T_{IN}$ deterministic jitter (DJ) appears in the first cycle and accumulates to $0.75T_{IN}$ by the third cycle. In the fourth cycle, the output clock aligns with the ideal clock. The DJ pattern repeats every four cycles and the maximum DJ is $0.75T_{IN}$ in this example, which is directly related to $\Delta\Sigma$ truncation error (e_q) by $DJ[k] = -e_q[k] \cdot T_{IN}$. When FDIV is used in the feedback path of a fractional-N PLL, $\Delta\Sigma$ quantization noise can be filtered by lowering the PLL bandwidth or cancelled using complex techniques based on a reference clock with the same frequency as the divider output [5, 9, 53]. However, for a stand-alone fractional divider with open loop architecture, these techniques cannot be applied.
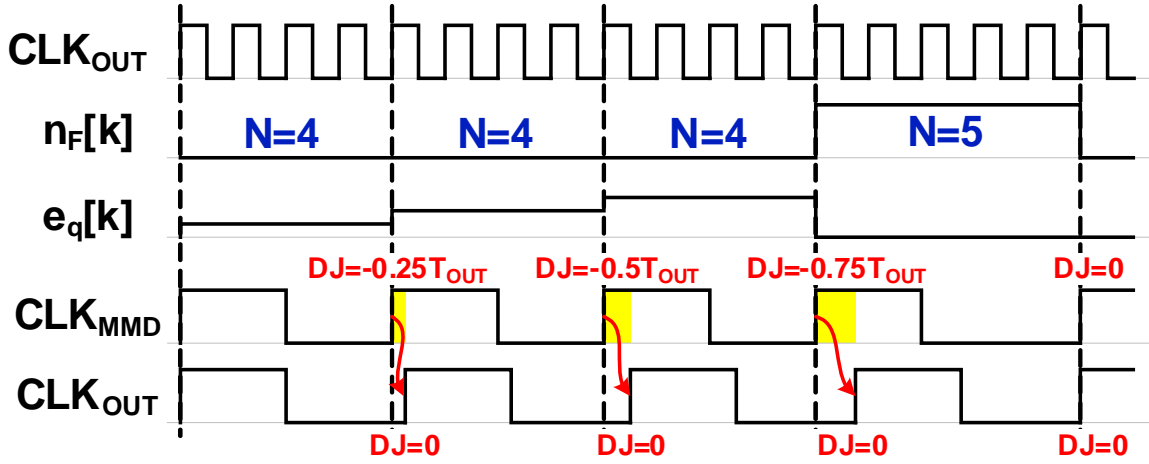
Figure 4.4: Timing diagram of $\Delta\Sigma$ fractional divider.

In order to cancel the DJ due to the $\Delta\Sigma$ quantization error, a digitally controlled delay line (DCDL) (i.e. digital-to-time converter (DTC)) is inserted to provide a phase shift $T_{QNC}[k]$ equal and opposite to the deterministic jitter and it can be expressed as

$$T_{QNC}[k] = e_q[k] \cdot T_{IN} \tag{4.1}$$

A simplified block diagram of the proposed open loop fractional divider is shown in Fig. 4.5.

It consists of a multi-modulus divider (MMD) followed by a DCDL for QNC. An SSC generator produces a triangular modulation waveform, which is added to the frequency control word (FCW). The FCW is then split into integer (FCW_I) and fractional (FCW_F) parts. A first order $\Delta\Sigma$ modulator is used, with a high resolution input FCW_F. The $\Delta\Sigma$ modulator output ($\Delta\Sigma_O[k]$) is added to FCW_I to control the MMD. The timing diagram in Fig. 4.4 shows the added phase shift by the DCDL, where the output clock matches the ideal clock and the DJ is completely cancelled. To perfectly cancel the $\Delta\Sigma$ quantization noise, the DCDL gain has to be calibrated to match the input clock period (T_{IN}) using a digital calibration unit. The DCDL gain is calibrated by digitally scaling its input $e_q[k]$ by a calibration factor K_G.
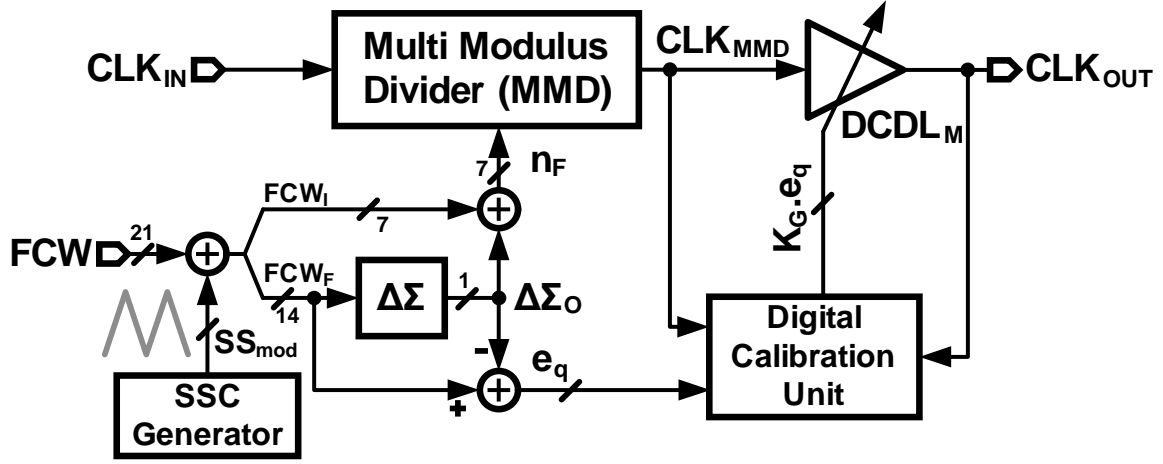
Figure 4.5: Simplified block diagram of the stand-alone open loop $\Delta\Sigma$ fractional divider.

4.2.3 DCDL Calibration

The proposed digital calibration unit is based on a digital delay locked loop (DLL) and it does not require any external reference clocks. The basic concept of the proposed digital calibration technique is shown in Fig. 4.6. A D-flip-flop (DFF_S) is added to synchronize the MMD output with the input clock (CLK_{IN}). A second (DFF_R) delayed the synchronized clock with one input clock cycle (T_{IN}). The time difference between DFF_S and DFF_R outputs, namely CLK_S and CLK_R respectively, is used as a T_{IN} time reference, as shown in the timing diagram in Fig. 4.6. A simple digital DLL composed of a bang-bang phase
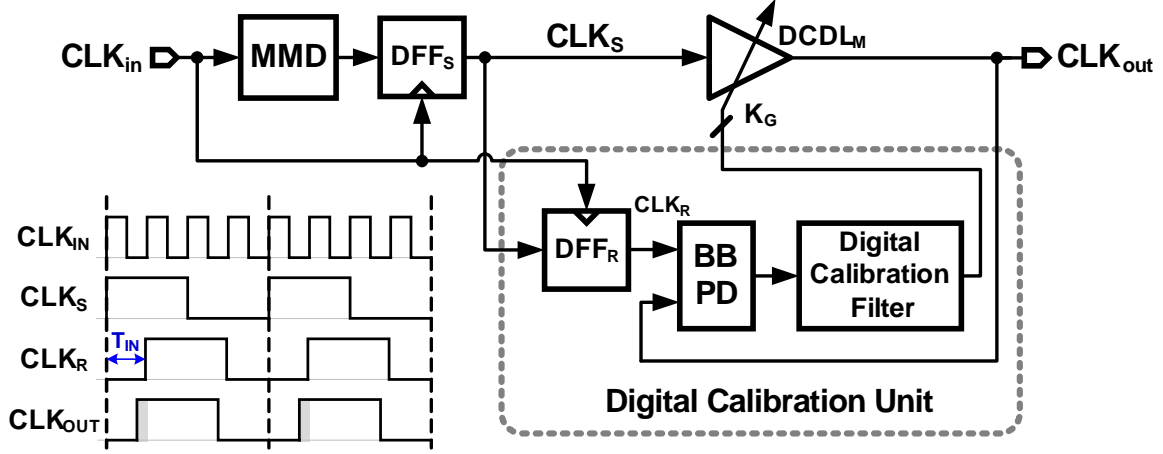
Figure 4.6: Block and timing diagrams of the open loop FDIV with a DCDL foreground calibration.

detector (BBPD) and a digital accumulator is used to lock the DCDL delay to T_{IN}. The accumulator output can be used as an estimated value of the calibration gain factor K_G in a foreground manner. Consequently, the $\Delta\Sigma$ error signal $e_q[k]$ is digitally scaled by K_G to control the DCDL in normal operation. However, the DCDL gain changes with supply and temperature variations. Therefore, the $\Delta\Sigma$ quantization noise is not cancelled perfectly in different operating conditions and jitter performance degrades across supply and temperature variations. To mitigate this, the calibration can be achieved in a background manner by introducing a complementary delay line ($DCDL_C$) in the DLL feedback path. The main delay line ($DCDL_M$) is controlled by a delay control word ($DCW_M = K_G \cdot e_q[k]$), while the complementary $DCDL_C$ is controlled by $DCW_C = K_G \cdot (1 - e_q[k])$. In steady state, the DLL establishes the sum of $DCDL_M$ and $DCDL_C$ delays to be equal to one T_{IN} time period as follows:

$$e_q[k] \cdot K_G \cdot T_{DCLDM} + (1 - e_q[k]) \cdot K_G \cdot T_{DCLDC} = T_{IN} \qquad (4.2)$$

where T_{DCLDM} and T_{DCLDM} represent the full-scale delays of $DCDL_M$ and $DCDL_C$ respectively. The optimum calibration gain (K_G) to calibrate $DCDL_M$ gain is attained across PVT variations by matching the two delay lines ($T_{DCLDM} = T_{DCLDC}$).

$$K_G \cdot T_{DCLDM} = T_{IN} \qquad (4.3)$$

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Because for zero input code the DCDLs have a non-zero delay, denoted as T_O, an equal delay is introduced in the reference time path using an offset delay line ($DCDL_{OFF}$) to cancel the T_O delay of $DCDL_M$ and $DCDL_C$. An initial offset calibration step is done by bypassing DFF_R using a multiplexor (MUX_{CAL}) and setting $K_G = 0$ so that the inputs to the main and complementary DCDLs are zero. After the DLL is locked, the delay from the $DCDL_{OFF}$ will match the offset delays of the $DCDL_M$ and $DCDL_C$. Then the offset delay control word (DCW_{OFF}) is held to be used in normal operation. The detailed block diagram of the proposed open loop FDIV with a DCDL background calibration is shown in Fig. 4.7. By employing a wide division range multi-modulus divider (MMD), a wide frequency range is achieved. A first order $\Delta\Sigma$ modulator is used for fractional synthesis to achieve fine frequency resolution with low power consumption. The output frequency range is 20MHz to 1GHz controlled by a 21-bit frequency control word (FCW), where the 7MSBs controls the integer division ratio (N) from 4 to 127, and the 14LSBs controls the fractional part (α), resulting in a division ratio of $N + \alpha$. The digital calibration unit of the DCDL gain is used to achieve low jitter performance that is insensitive to PVT variations.

Figure 4.7: Detailed block diagram of the open loop FDIV with a DCDL background calibration.

A spread spectrum generator is used to modulate the FCW with a programmable triangle-

wave. The proposed open loop architecture achieves excellent EMI reduction and instantaneous frequency switching. Additionally, the divider has instantaneous power-cycling capability between idle and active states by simply gating the input clock (CLK_{IN}), thus it allows an energy-proportional operation [83].

4.3 Building Blocks

4.3.1 Multi-Modulus Divider (MMD)

The block diagram of the extended range MMD is shown in Fig. 4.8. It is composed of six divide-by-2/3 cells with a reset feature plus extension control logic with a reload register. It is similar to the MMD presented in section 3.4, but with a wider division range from 4 to 127 with seamless switching at extension boundaries.
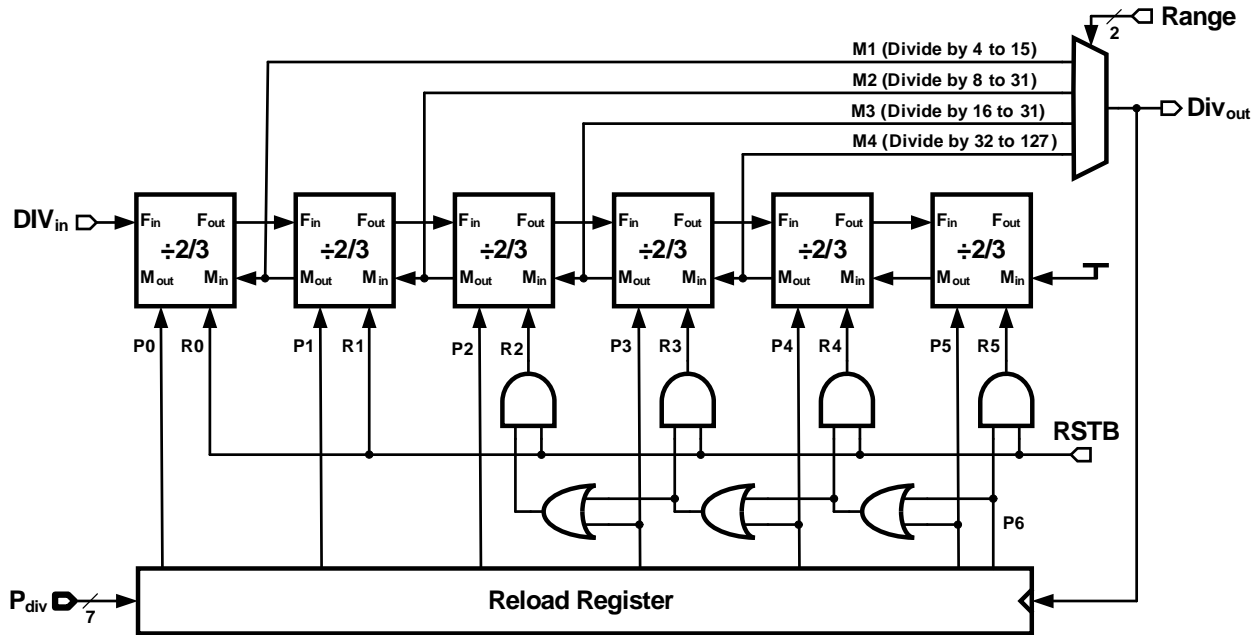
Figure 4.8: Detailed block diagram of the proposed MMD with seamless switching across a wide division range from 4 to 127.

4.3.2 Digitally Controlled Delay Line (DCDL)

A 7-bit DCDL is implemented using a cascade of 8 identical digitally controlled delay cells as demonstrated in Fig. 4.9. The design details are similar to those of the DCDL presented in section 2.4.3. Post-layout Monte-Carlo simulations, depicted in Fig. 4.10, show the maximum integral non-linearity of less than 1.25LSB of delay deviation, where the LSB resolution equals to about 2ps.
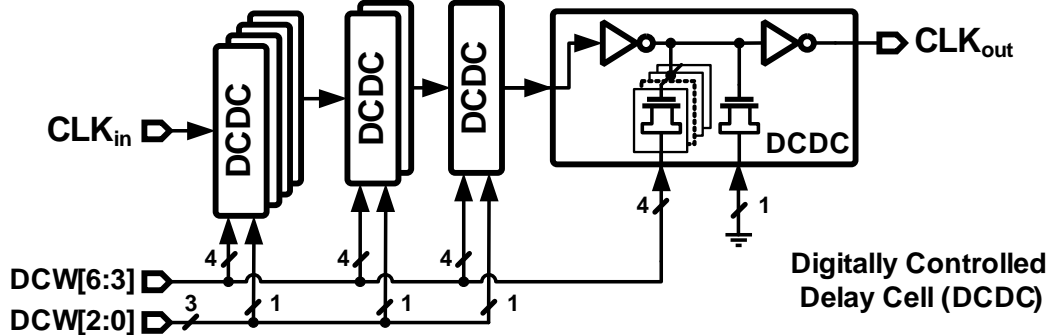
Figure 4.9: The 7-bit digitally controlled delay line (DCDL) block diagram.
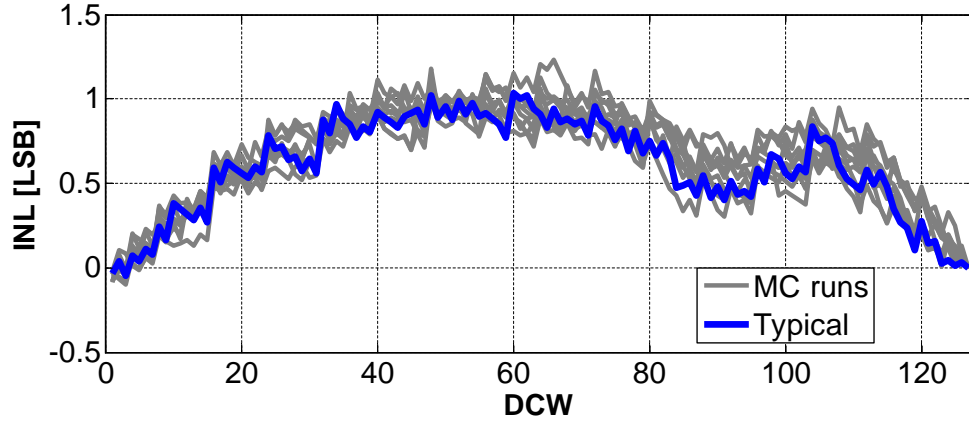
Figure 4.10: Post-layout Monte-Carlo simulations for the DCDL integral nonlinearity (INL).

4.3.3 Ring-based DPLL

The implementation details of the integer-N digital PLL, used to generate the high frequency clock driving the FDIVs, is shown in Fig. 4.11. It is based on the ring-based digital FNPLL

presented in section 3.3. The PLL multiplies a 50MHz reference frequency by 100 to provide a 5GHz output.

Figure 4.11: Detailed block diagram of the ring-based digital PLL.

4.4 Measurement Results

The die photograph is shown on the left of Fig. 4.12, and the detailed layout for the fractional divider is shown on the right of Fig. 4.12. The chip was fabricated in 65nm CMOS process and occupies roughly $0.12mm^2$ active area. Each fractional divider occupies only about $0.017mm^2$, while the integer-N digital PLL occupies $0.084mm^2$. The measured phase noise of the digital PLL at 5GHz is shown in Fig. 4.13. With a 6MHz PLL bandwidth, the phase noise is -99dBc/Hz at 1MHz offset. The proposed digital PLL achieves excellent integrated RMS jitter of $1.73ps_{rms}$ while consuming less than 4mW using a 0.9V supply voltage.

Using a 5GHz clock and fractional division of 5.125, the output frequency is about 975MHz.

Figure 4.12: Die micrograph of the clock generation unit and zoomed-in FDIV layout.
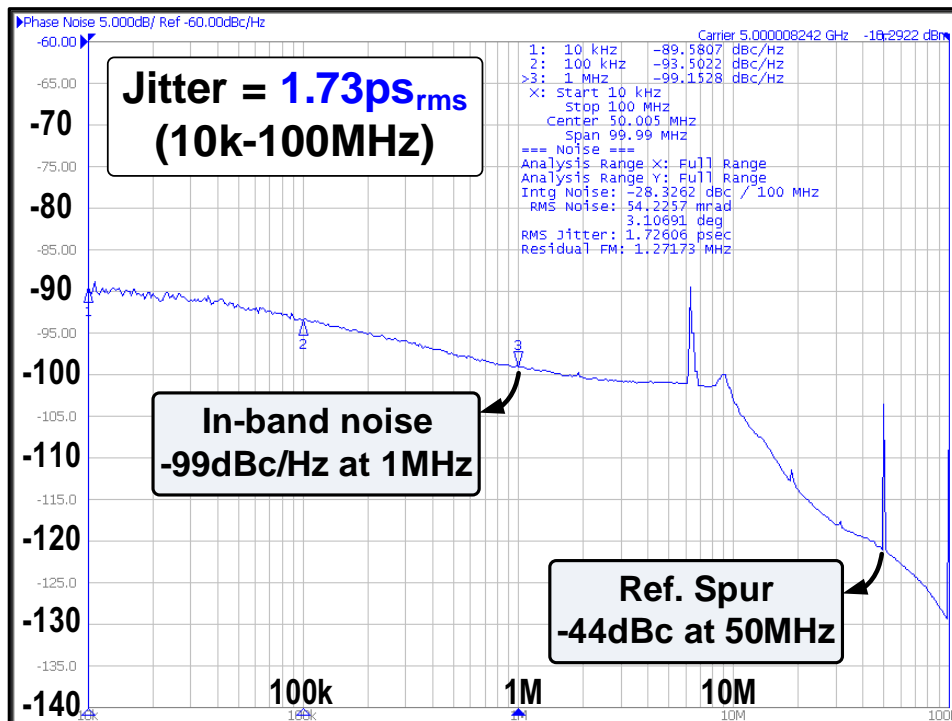
Figure 4.13: Phase noise measurements of the digital PLL at 5GHz output frequency.
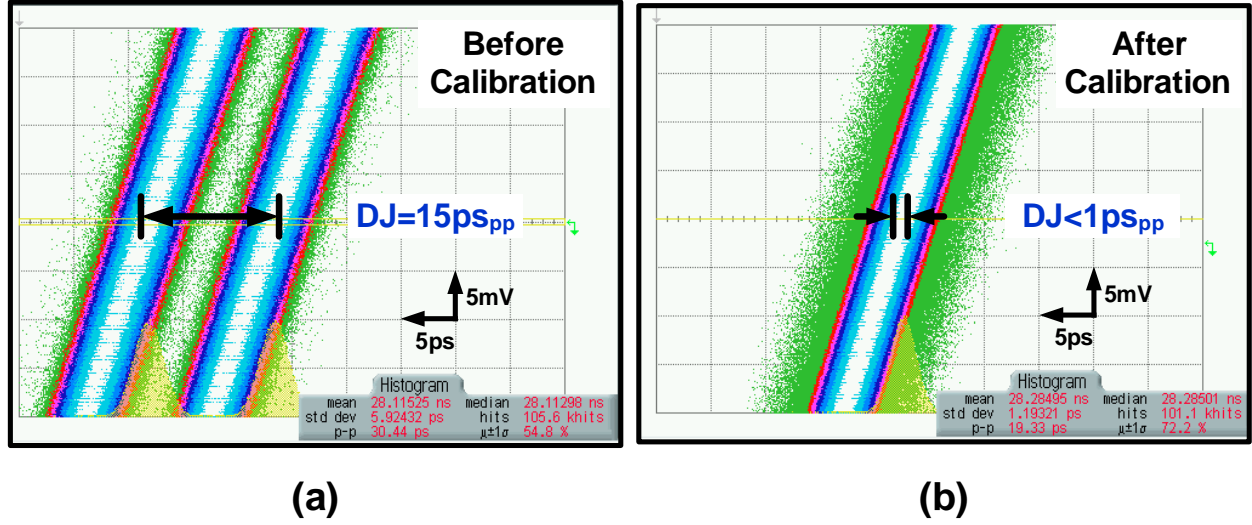
Figure 4.14: Measured jitter histograms at 975MHz FDIV output frequency (a) before and (b) after DCDL calibration.
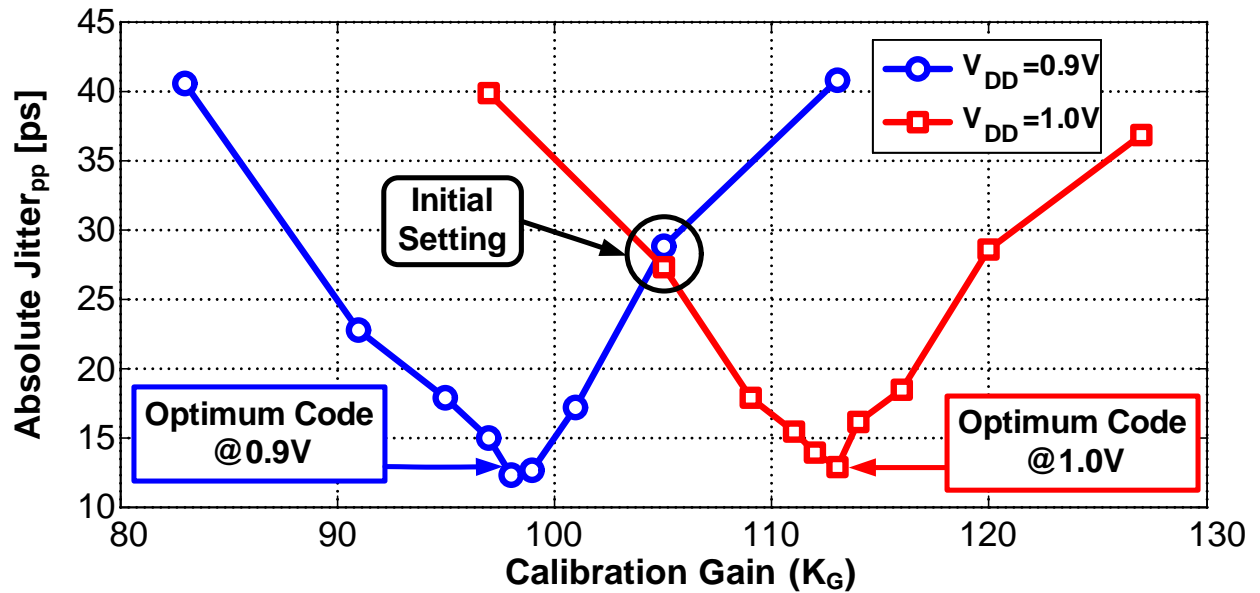
Figure 4.15: Measured absolute peak-to-peak jitter as a function of the gain calibration code (K_G) for different supply voltages.

Fig. 4.14 shows the measured jitter histograms for before and after the DCDL calibration. With no DCDL gain calibration, the delta-sigma quantization noise is not cancelled perfectly, and a deterministic jitter of 15ps is shown on the Fig. 4.14(a). When DCDL gain calibration is enabled, perfect quantization noise cancellation is achieved with less than 1ps deterministic jitter as illustrated in Fig. 4.14(b). Fig. 4.15 plots the peak-to-peak jitter
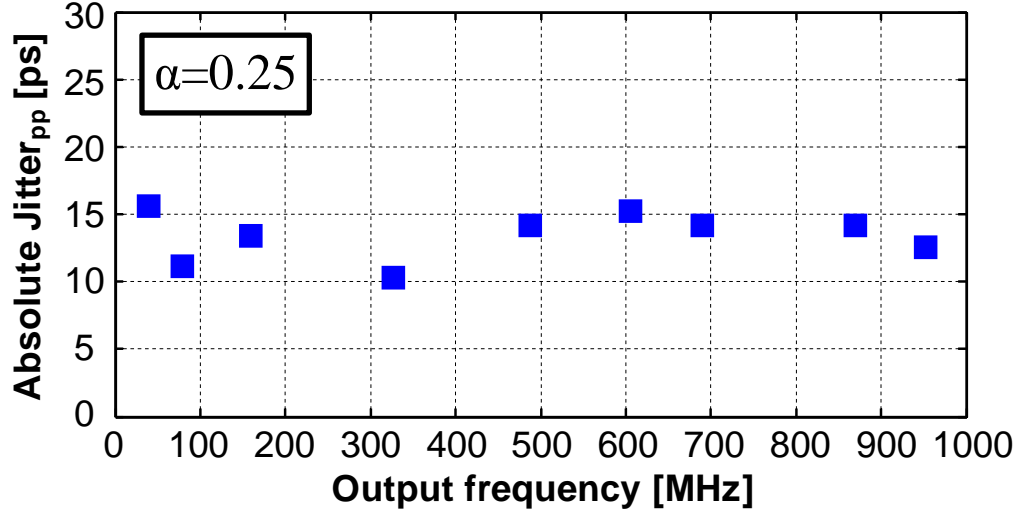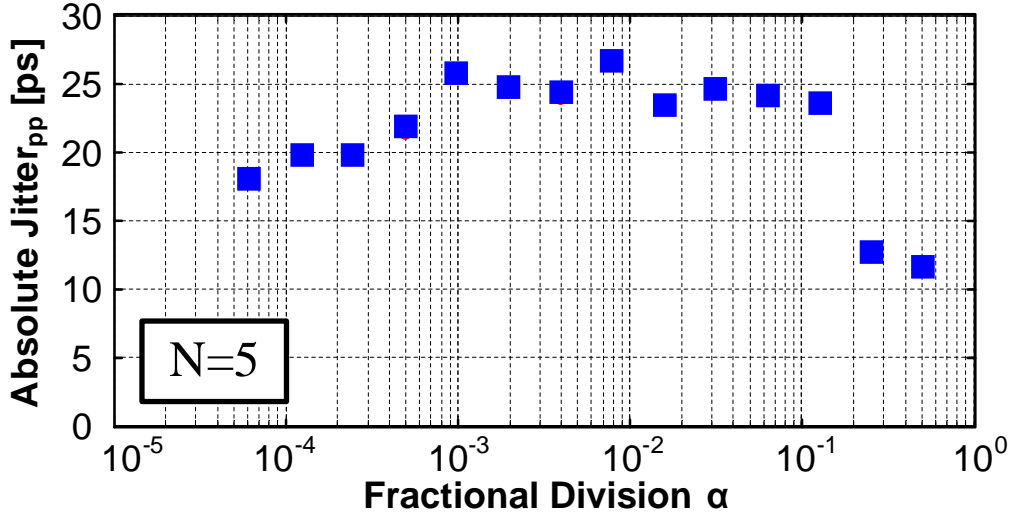
Figure 4.16: Measured peak-to-peak absolute jitter as a function of (a) output frequency, and (b) fractional division ratio (α).

as a function of the gain calibration code for different supply voltages. The DCDL gain decreases as supply voltage (VDD) increases, and the optimal calibration code (K_G) shifts from 98 at VDD of 0.9V to 113 at VDD of 1.0V. The calibration loop always converges to the optimum calibration code regardless of the output frequency. The peak-to-peak jitter is 13ps with optimum calibration. Absolute output jitter is measured for different output frequencies, when the integer division ratio is varied, with fixed fractional part (α) of 0.25
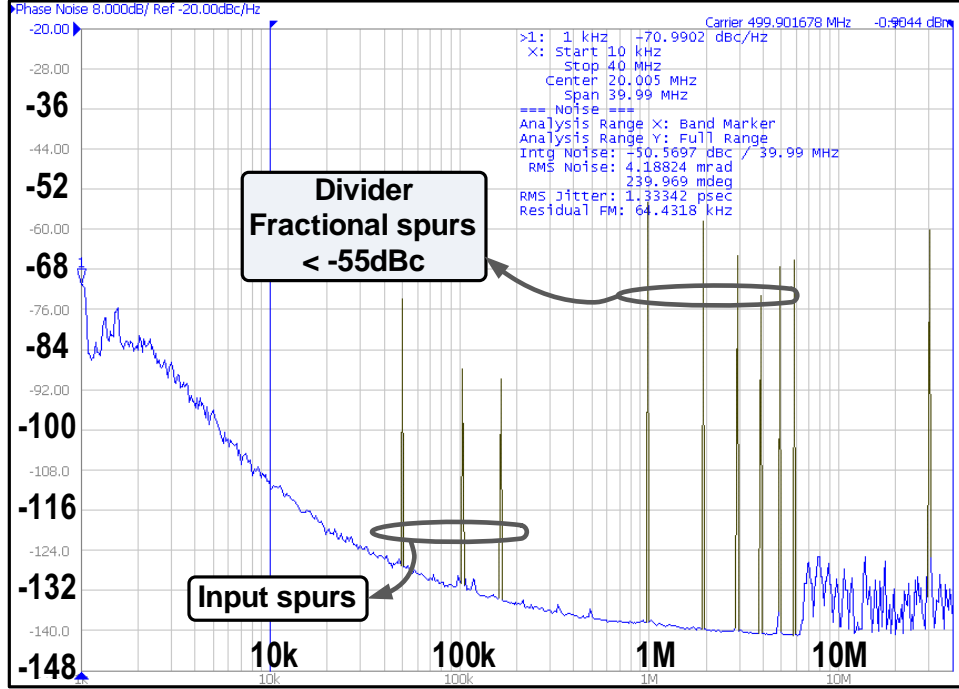
Figure 4.17: Measured phase noise performance of the stand-alone FDIV when $\alpha = 2^{-10}$.

(see Fig. 4.16(a)). The peak-to-peak jitter of the divider output is less than 20ps over a wide frequency range from 20MHz to 1GHz. When the 14-bit fractional part (α) is varied, with fixed integer division of 5, the peak-to-peak jitter is less than 27ps as shown in Fig. 4.16(b). The increased jitter is attributed to the DCDL integral non-linearity.

In order to evaluate the phase noise performance of the stand-alone FDIV, the FDIV is characterized using Agilent E5052B signal source analyzer (SSA) where a 5GHz external clean clock is used as an input clock for the FDIV. The 5GHz clock has about $0.2\text{ps}_{\text{rms}}$ measured integrated jitter from 10kHz to 40MHz. Fig. 4.17 shows the measured phase noise of the FDIV (after divide-by-2) using an integer divide ratio of 5, and a fractional part α of 2^{-10}. The added noise by the FDIV is deterministic in nature, mainly attributed to the DCDL INL. The worst-case fractional spur is better than -55dBc. The measured integrated jitter from 10kHz to 40MHz is about $1.3\text{ps}_{\text{rms}}$. The worst-case phase noise performance occurs when the fractional part α approaches 0 or 1. When an α of 2^{-14} is used, the measured integrated jitter is increased to about $1.44\text{ps}_{\text{rms}}$ as demonstrated in Fig. 4.18.

The spread spectrum modulation capability of the FDIV is characterized in both time

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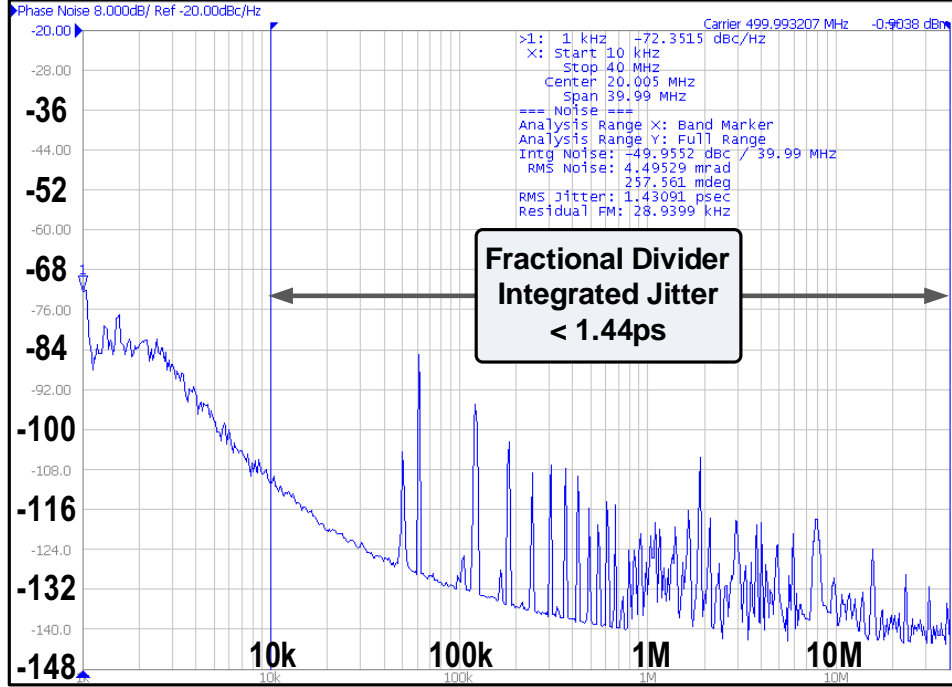
Figure 4.18: Measured phase noise performance of the stand-alone FDIV when $\alpha = 2^{-14}$.

and frequency domains. Fig. 4.19(a) plots the measured output frequency as a function of time, when a 5.5MHz triangle wave with 0.5% modulation depth is used for spread spectrum modulation. Because of the open loop architecture of the FDIV, the modulation bandwidth is unlimited, and the triangle wave in the plot has a very sharp transition indicating no filtering even with this very wide-BW modulation signal. This improves EMI performance for the proposed spread spectrum clocking (SSC), compared to conventional fractional-N PLL which has limited bandwidth. The modulation depth can be varied precisely to control the amount of EMI reduction depending on the application, unlike spread spectrum clock generators that uses direct VCO modulation technique. Fig. 4.19(b) shows the measured output frequency as a function of time, using a standard 33kHz triangle modulation and a modulation depth of 2%. The output spectrum measurements is done using Agilent N9000A spectrum analyzer (SA). The FDIV output spectrum (after divide-by-2) is shown in Fig. 4.20 when the spread spectrum modulation is turned on and off. Using a 33kHz triangle wave with 2% modulation depth, a peak EMI reduction better than 22dB is achieved. This excellent reduction is realized due to the unlimited modulation bandwidth of the open loop fractional

divider. This translates to a flat spread spectrum and improved EMI reduction.

To demonstrate the instantaneous frequency switching capability of the FDIV, the fractional part α is changed from 1/8 to 7/8. Fig. 4.21 shows the measured output frequency as a function of time, where the frequency switches with about 125MHz step. The switching time is only one output cycle, which is about 1ns. A switching time less than 100ns is illustrated in Fig. 4.21, which is limited by the instrument. The measured power consumption of the prototype fractional divider versus output frequency is plotted in Fig. 4.22. The total power consumption is about 3.2mW for a 1GHz output frequency. The power of all the blocks scales almost linearly with output frequency except for the multi-modulus divider (which scales with the input clock). Table 4.1 shows the performance summary and comparison with state-of-the-art designs. The proposed fractional-N clock generator achieves excellent jitter performance of 3ps$_{rms}$, while consuming the lowest power of 3.2mW/GHz. The all-digital implementation of the divider occupies the smallest area compared to state-of-the-art designs.

4.5   Conclusion

In conclusion, an all-digital generic multi-output clock generator is proposed to meet diverse clocking requirements in SoCs. The proposed open loop fractional divider architecture achieves excellent jitter performance by cancelling $\Delta\Sigma$ quantization using a digitally controlled delay line (DCDL). A robust performance is achieved across PVT variations by a background calibration technique of the DCDL gain. A wide range multi-modulus divider with seamless switching is demonstrated to achieve wide output range. The measured results indicate a low peak-to-peak jitter, excellent spread spectrum EMI reduction, and instantaneous frequency switching.

Table 4.1: Fractional Divider Performance Summary

	Li [84] ISSCC'12	Park [85] ISSCC'12	Damphousse [86] JSSC'07	De Caro [87] JSSC'10	De Caro [76] JSSC'15	This Work
Architecture	Frac-N DPLL	Frac-N MILO	Digital Period Synthesizer	Digital Period Synthesizer	Digital Period Synthesizer	Frac-N Divider
Technology [nm]	22	65	150	65	28	65
Supply [V]	1	1	N/A	1.2	1	0.9
Output Freq. [MHz]	0.6-3.6	580	27	180-1270	200-3300	20-1000
RMS Jitter [ps]	10	8.05	N/A	12.8	3.16	3
Peak-to-Peak Jitter [ps]	N/A	N/A	N/A	93	28.1	27
Instantaneous Switching	No	No	N/A	Yes	Yes	Yes
SSC Capability	Yes	No	Yes	Yes	Yes	Yes
EMI Reduction	N/A	N/A	13dB @ 3% of 148MHz [RBW=100kHz]	20.5dB @ 6% of 750MHz [RBW=100kHz]	27dB @ 10% of 1GHz [RBW=100kHz]	22.3dB @ 2% of 1GHz [RBW=24kHz]
Power Consumption	18.4mW @3.6GHz	10.5mW @580MHz	7.1mW @27MHz	19.8mW @1.27GHz	10.3mW @1GHz	3.2mW @1GHz
Power Eff. [mW/GHz]	5.1	18.1	263	15.6	10.3	3.2
Area [mm^2]	0.03	0.03	0.06	0.044	0.031	0.017
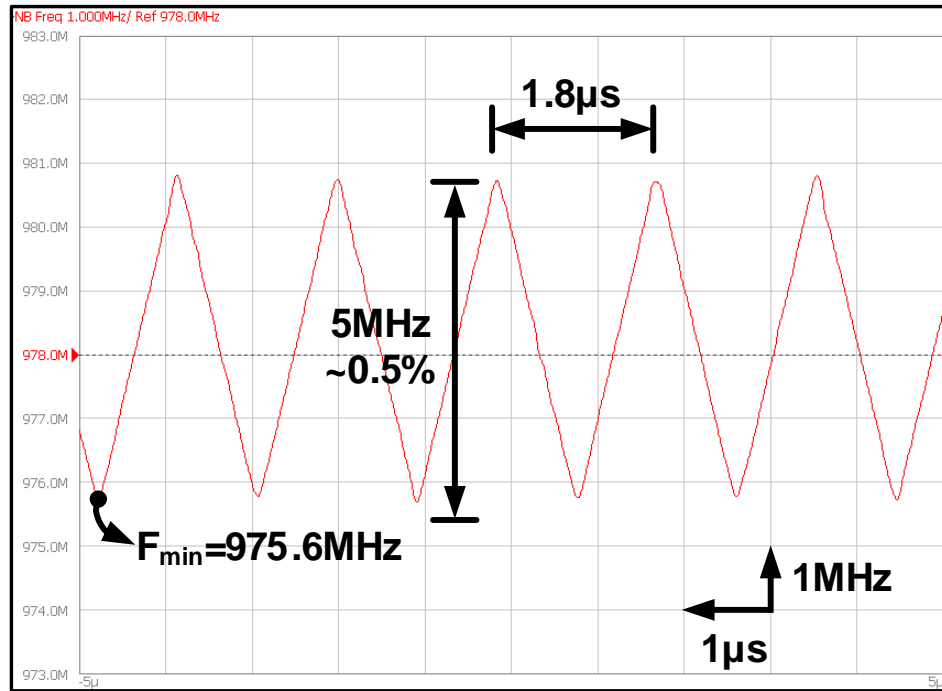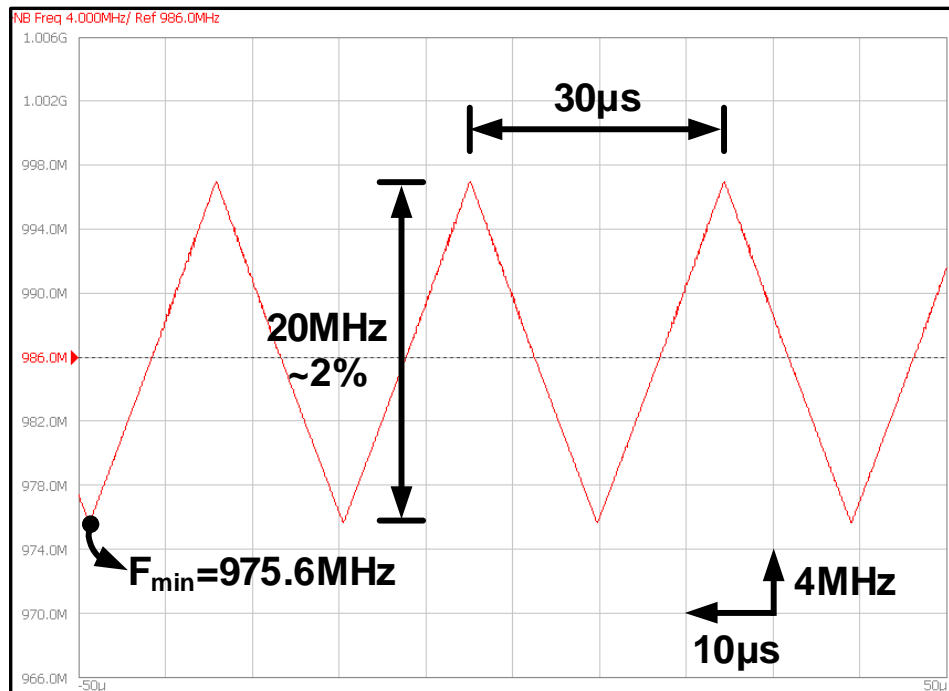
Figure 4.19: Measured spread spectrum frequency modulation of the FDIV output in time-domain in case of: (a) 5.5MHz triangle wave with 0.5% modulation depth, and (b) 33kHz triangle wave with 2% modulation depth.
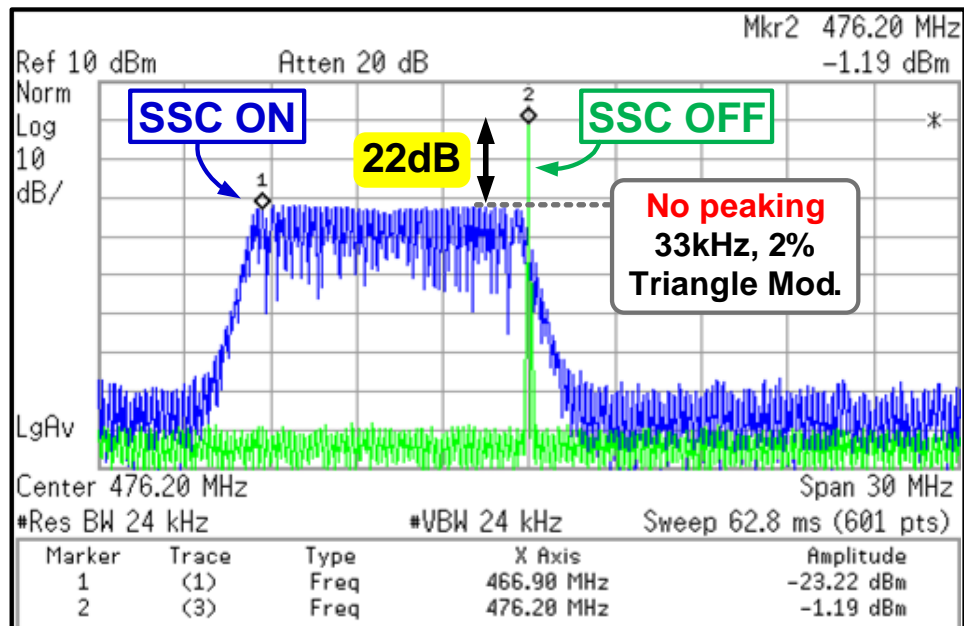
Figure 4.20: Measured FDIV output spectrum with and without SSC.
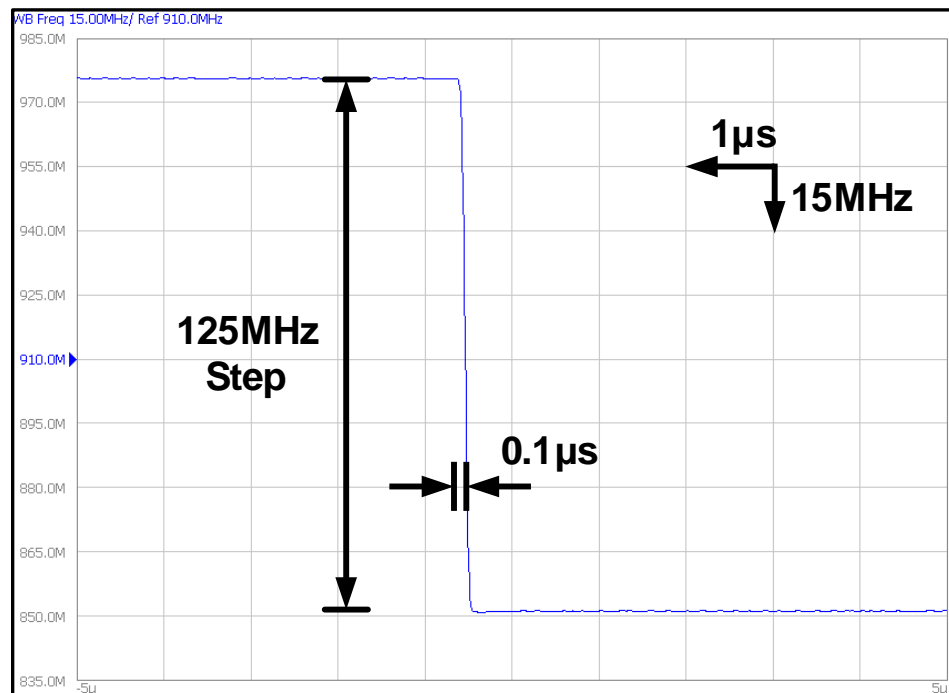
Figure 4.21: Measured instantaneous frequency switching of the FDIV.
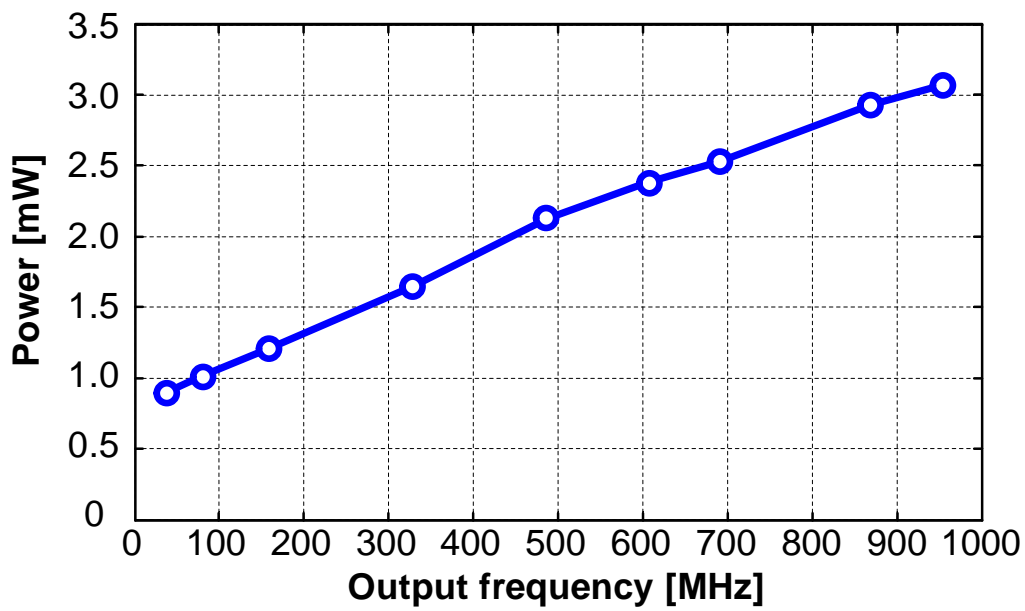
Figure 4.22: Measured power consumption of the stand-alone FDIV as a function of the output frequency.

CHAPTER 5

INJECTION-LOCKED CLOCK MULTIPLIERS WITH FREQUENCY TRACKING LOOP

5.1 Introduction

Phase-locked loops (PLLs) are most commonly used for high frequency clock generation from a low frequency clock provided by crystal oscillator. While they have been optimized for low power consumption and small area, their noise performance is fundamentally limited by the coupled noise bandwidth tradeoff. The oscillator noise is high-pass shaped whereas noise of the other loop components such as the charge pump and divider is low-pass filtered by the PLL bandwidth. Assuming a clean reference clock, optimum jitter performance is achieved at a loop bandwidth where the oscillator and loop noise contributions to the output jitter are equal. Because of this tradeoff, achieving superior jitter performance ($<200\text{fs}_{\text{rms}}$) with conventional PLLs mandates stringent noise performance of the oscillator and/or loop components, thus resulting in high power consumption (tens of mWs) [57, 88, 89]. A sub-sampling (SS)-PLL architecture alleviates these tradeoffs. The feedback divider is omitted and the charge pump noise is suppressed by a high gain sub-sampling phase detector (SSPD) [90]. Consequently, excellent in-band phase noise and figure-of-merit (FoM) were achieved [90, 91]. However, the SSPD has a limited capture range especially at low supply voltage, and more importantly a large loop filter capacitor is needed because of high phase detector gain.

Another commonly used approach for low noise clock generation is based on directly resetting jitter accumulation in the oscillator. This is done by replacing the noisy oscillator

edge with a clean reference clock edge, and this architecture is referred to as a multiplying delay locked loop (MDLL) [92, 93]. This architecture also alleviates the conflicting noise filtering requirements of conventional PLLs and is shown to be capable of achieving low jitter and low power [94, 95]. However, MDLL by nature is suitable only for ring-based voltage controlled oscillators (VCOs) and its frequency is usually limited to a few GHz because of the timing constraints in its selection logic. Sub-harmonic injection locking works, in principle, similar to an MDLL. A free-running oscillator can be *injection* locked to the Nth harmonic of the reference clock by injecting narrow pulses at the reference frequency into the oscillator ($F_{OUT} = N\,F_{REF}$) as depicted in Fig. 5.1(a). As a result, this technique provides a simple means for implementing very low-jitter integer-N clock multiplication using either ring [96–98] or LC VCOs [99–104]. When injection locked, the oscillator tracks the reference clock and its oscillator phase noise is greatly suppressed as illustrated in Fig. 5.1(b). Unlike MDLLs, injection locked clock multipliers (ILCMs) have no selection logic, so they are suitable for very high frequency clock generation using LC-VCOs [102–104].

However, in practice, any frequency error (F_{ERR}) between the oscillator free-running frequency (F_o) and the target frequency ($N\,F_{REF}$) will degrade the clock multiplier performance as shown in Fig. 5.1(c). F_{ERR} occurs due to drift in oscillator free-running frequency across supply and temperature, and can easily exceed the lock-in range (ΔF_L) especially when ΔF_L is narrow (a few hundreds of ppms) as is the case when either a high-Q LC oscillator or large multiplication factor N is used. Dedicated frequency-tracking loop (FTL) is needed to correct F_{ERR} [97], [99].

In this chapter, we present a digital frequency-tracking loop (FTL) to continuously tune the oscillator's free-running frequency (F_o) to be $N\,F_{REF}$ [105]. The proposed FTL, implemented using a low power digital feedback loop, ensures robust operation of the ILCM across process, voltage and temperature (PVT) variations even when the lock-in range ($\Delta F_L < 500ppm$) is narrow, multiplication factor N is large, and the oscillator Q is high. The prototype ILCM generates output clock in the range of 6.75GHz-8.25GHz by multiplying F_{REF} by 64 and achieves $190fs_{rms}$ integrated jitter. The entire ILCM consumes 2.25mW from 0.9V supply and achieves an FoM of -251dB.

The rest of the chapter is organized as follows. Section 5.2 illustrates the basic concepts
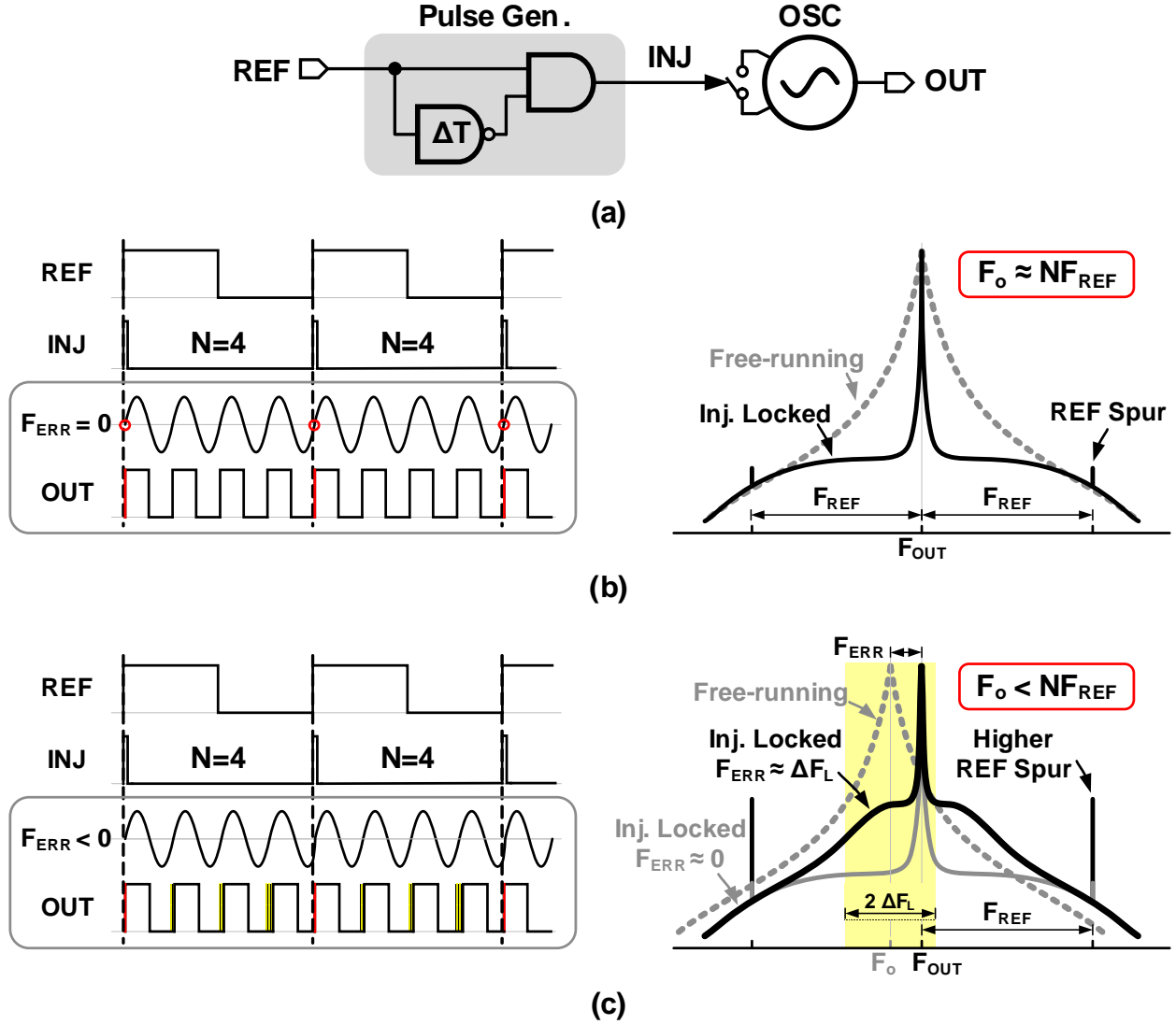
Figure 5.1: (a) Sub-harmonic injection-locked oscillator. Timing diagram and output spectrum of ILCM when (b) $F_{ERR} = 0$, and (c) $F_{ERR} \approx \Delta F_L$.

of injection locking highlighting frequency tracking challenges followed by a brief overview of state-of-the-art ILCMs. The proposed architecture is then presented in section 5.3, in addition to a detailed analysis of sub-harmonic injection locking dynamics. The circuit implementation of critical building blocks is presented in section 5.4. The measured results from the test chip are shown in section 5.5. Finally, the key contributions of this work are summarized in section 5.6.

5.2 Injection-Locked Clock Multiplication

5.2.1 Basic Concept

Injection locking has many applications in frequency division [57, 106], phase de-skew [107], quadrature generation [108], and clock multiplication [96–105]. Our focus is on injection-locked clock multiplication, wherein a free-running oscillator is locked to the Nth harmonic of the injected signal. In this case of so-called sub-harmonic injection ($F_{REF} = F_{INJ}$), the injection signal is in the form of narrow pulses to increase the power of Nth harmonic [109]. These narrow periodic injected pulses adjust the oscillator phase and if the oscillator free-running frequency F_o is within the lock-in range, the oscillator gets phase-locked to the injected signal. Under this condition, the oscillator runs at F_o for $(N-1)$ cycles, while the injection pulse changes the period of the Nth cycle so that the average frequency equals to $N F_{REF}$ (see the timing diagram in Fig. 5.1(c)). In other words, phase error accumulated in $(N-1)$ cycles is compensated by an excess phase equal to $2\pi N F_{ERR}/F_o$ due to pulse injection in the Nth cycle. This periodic correction appears as deterministic jitter ($DJ \approx (N-1) \alpha_E T_{OUT} \approx \alpha_E T_{REF}$) where $\alpha_E = F_{ERR}/F_{OUT}$ is the relative error. This translates to a reference spur ($Spur_{dBc} \approx 20 \log(DJ/T_{OUT}) \approx 20 \log(\alpha_E N)$) [99]. Figure 5.2 shows the impact of frequency error and the multiplication factor N on the deterministic jitter and reference spur performance. Phase noise performance is also degraded by $N F_{ERR}$ because of the reduced filtering bandwidth as shown in Fig. 5.1(c). Thus, the random and deterministic jitter performance of ILCMs greatly depends on $N F_{ERR}$, which mandates continuous tuning of the oscillator frequency to not only maintain phase lock but also to achieve excellent jitter/spur performance across voltage and temperature variations.

5.2.2 Conventional ILCM Architectures

A conventional injection-locked PLL is shown in Fig. 5.3. The PLL is introduced to tune the VCO free-running frequency F_o to be close to the center of the lock-in range. However, it is difficult to detect the drift in F_o at the phase detector input because the accumulated phase difference is almost reset at every reference cycle by the fast injection path as illustrated by
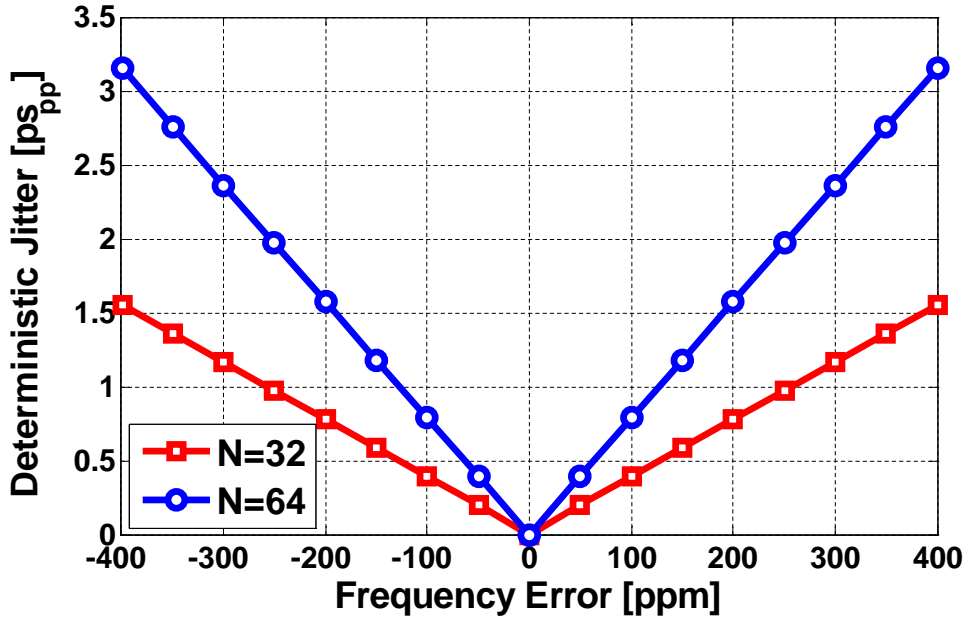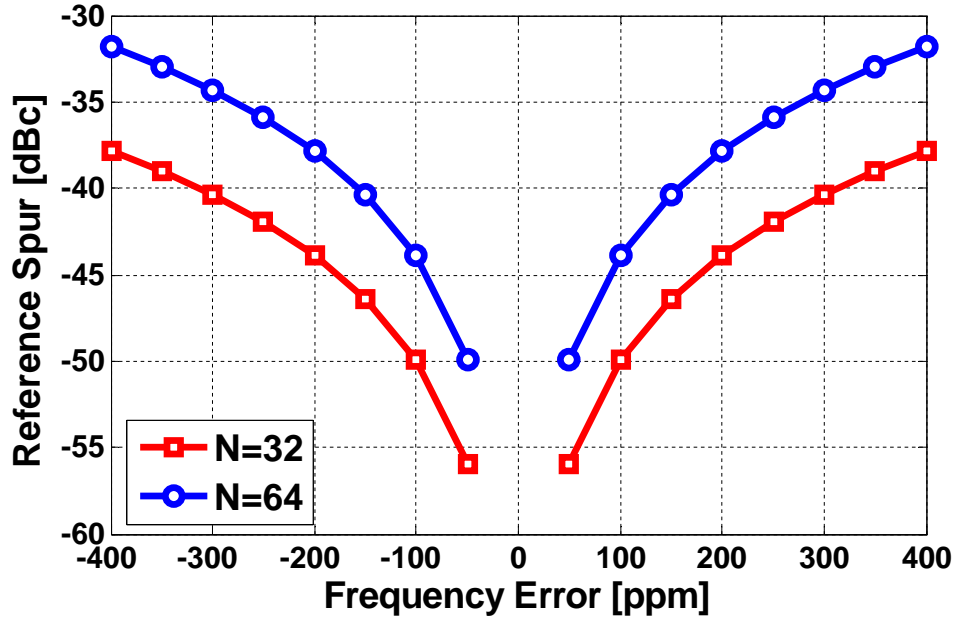
Figure 5.2: (a) Deterministic jitter and (b) reference spur as a function of F_{ERR} for N=32 and 64.

the timing diagram in Fig. 5.3. Further, since the VCO phase is adjusted simultaneously by the injection and PLL paths, injection-locked PLL also has to contend with the resulting race condition. Calibration of the injection timing is needed to overcome such a race condition. In

[100], calibration is done in a foreground manner, so it cannot track voltage and temperature variations, while in [104] calibration is done in background using an analog delay locked loop (DLL). In [96, 101], the injection timing is matched relying on a time-adjusted sub-sampling phase detector with high gain. However, these techniques are susceptible to charge pump current mismatch, and vulnerable against voltage and temperature, which limit the multiplication factor (N) and may degrade jitter and spurious performance.
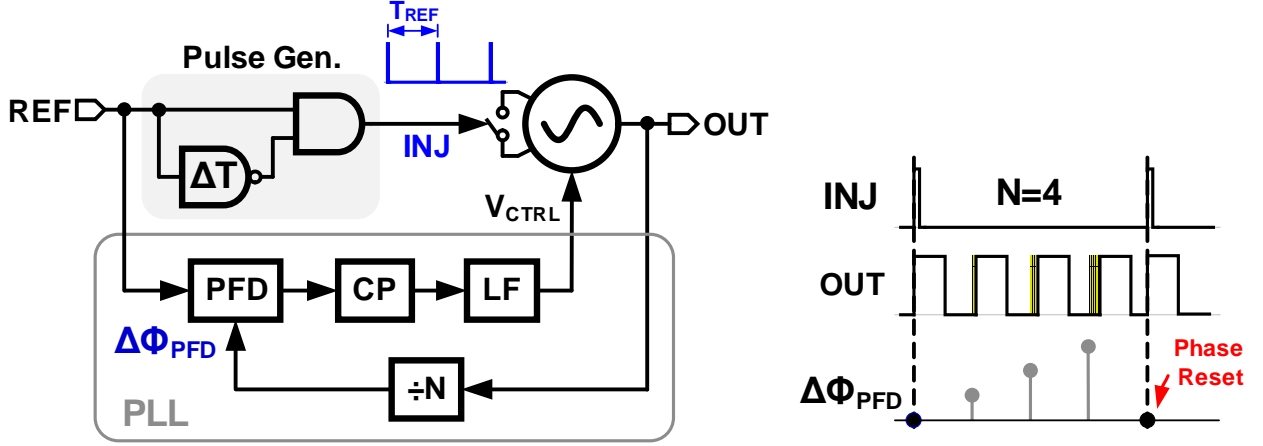
Figure 5.3: A block diagram of conventional injection-locked PLL with an illustrating timing diagram.

The drawbacks of injection-locked PLL can be alleviated by a using a replica DCO locked in a digital FLL [104]. The main DCO placed outside the loop shares the same control word with the replica DCO to track any frequency drift to the extent the two oscillators are matched as shown in Fig. 5.4(a). However this approach requires two matched oscillators, which doubles both power and area, and its effectiveness is limited by DCO gain (K_{DCO}) mismatch. Another approach proposed by Helal [99] uses a high resolution TDC as depicted in Fig. 5.4(b). The TDC measures the oscillator period when perturbed by the injection pulse and compares it to the measured free-running period. A correlator generates an error signal Δ as the difference between the two measurements as a direct representation of F_{ERR}. By accumulating Δ, the frequency error F_{ERR} can be corrected by continuously tuning the oscillator frequency to be in the middle of the lock-in range. However, the use of a high resolution TDC incurs a large power and area penalty.
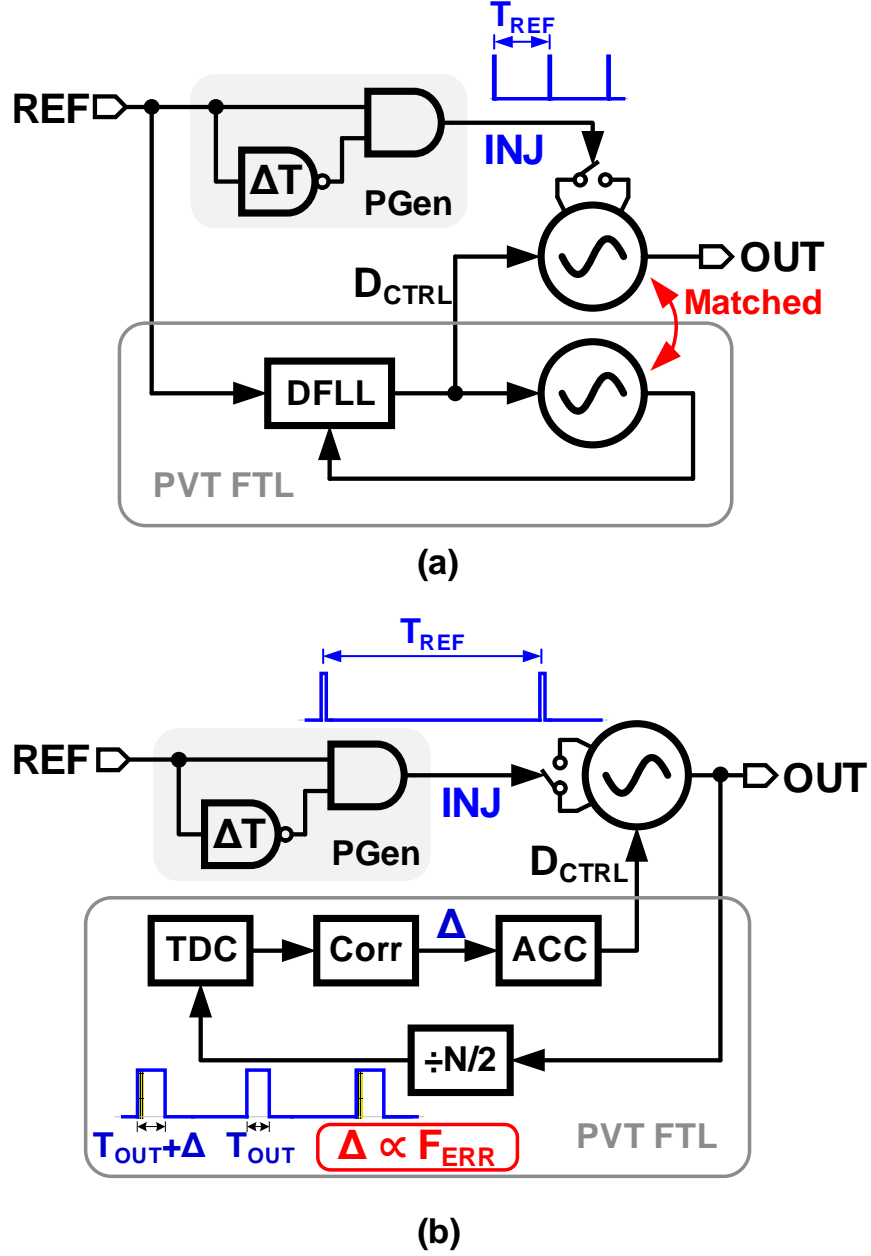
Figure 5.4: Block diagram of ILCM with (a) replica-based FTL [97], and (b) TDC-based FTL [99].

5.3   Proposed ILCM with Continuous Frequency Tracking Loop

5.3.1   Basic Concept of the proposed FTL

The proposed continuous frequency tracking loop (FTL) is based on a pulse gating technique shown in Fig. 5.5(a). Because injection pulses reset oscillator phase and make it difficult to

detect the phase error caused by frequency error, F_{ERR}, we propose to disable or gate the injection pulse periodically, and measure the accumulated phase error, Δ_{Gated}, as depicted in the timing diagram shown in Fig. 5.5(b). When a pulse is gated the oscillator continues to run at its free-running frequency (F_o). Consequently, a phase detector can be used to detect the frequency error F_{ERR} without the need for a power hungry high resolution TDC. In this example, every 4th reference edge is not injected, which results in a large Δ_{Gated} that can be easily measured using a simple phase detector. We then use this error information to correct F_{ERR} using a simple digital feedback loop. Injection gating resolves the race condition present in IL-PLLs, as it decouples the frequency tracking loop from the injection path. As a result, the phase locking condition now is only determined by the injection path.
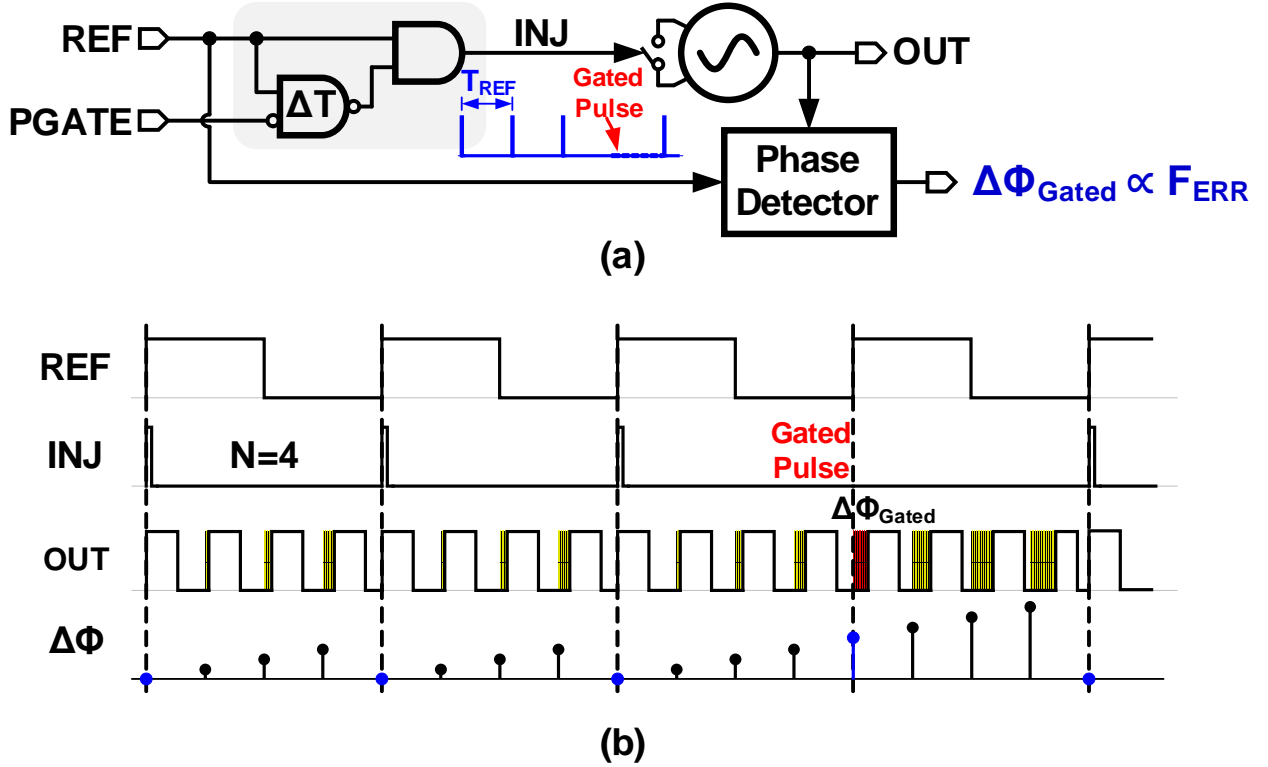
Figure 5.5: (a) Conceptual diagram of the proposed pulse getting frequency error detection. (b) Timing diagram.

The sign of F_{ERR} is detected simply by detecting the sign of Δ_{Gated} using a sub-sampling bang-bang phase detector (BBPD). The measured error is integrated using a digital accumulator whose output updates the frequency of the injection-locked DCO incrementally at

every pulse gating event as demonstrated in Fig. 5.6. This simple approach is similar to a bang-bang FLL and it corrects F_{ERR} accurately and continuously tunes the DCO frequency to the center of the lock-in range. The proposed FTL ensures robust operation across supply and temperature variations and helps achieve excellent jitter and spurious performance.
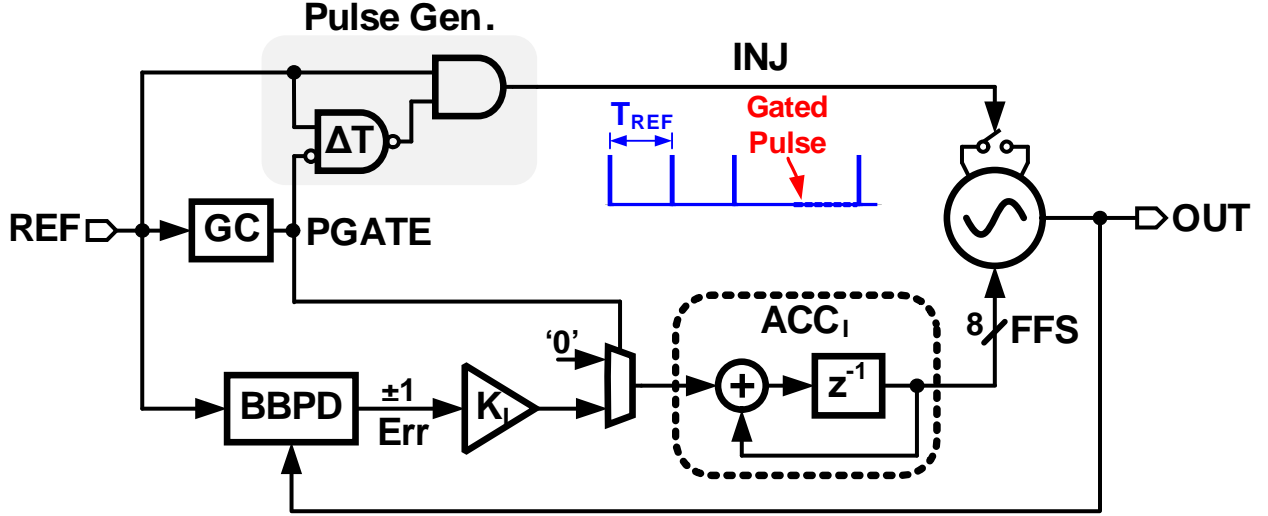
Figure 5.6: Block diagram of the proposed frequency tracking loop (FTL).

5.3.2 Complete Architecture

The complete block diagram of the proposed injection locked clock multiplier (ILCM) is shown Fig. 5.7. It consists of an injection-locked LC-DCO, a programmable pulse generator, and a digital frequency tracking loop (FTL). The operation proceeds as follows. First, at start-up, the DCO free-running frequency (F_o) is coarsely tuned to be within the lock-in range. Because of the sub-sampling nature of the architecture, coarse frequency selection is also used to set the target multiplication factor (N). The coarse frequency selection is done only during start-up. Consequently, the power and noise associated with the divider are eliminated in normal operation. Injection path, enabled in the second step, locks DCO phase to the injected pulse (INJ) with a time constant proportional to the injection strength.

Once initial phase lock is achieved, FTL is used to maintain lock by correcting the frequency drift caused by voltage and temperature variations. To this end, the proposed FTL measures the accumulated phase error due to F_{ERR} when the injection pulse is gated. How-
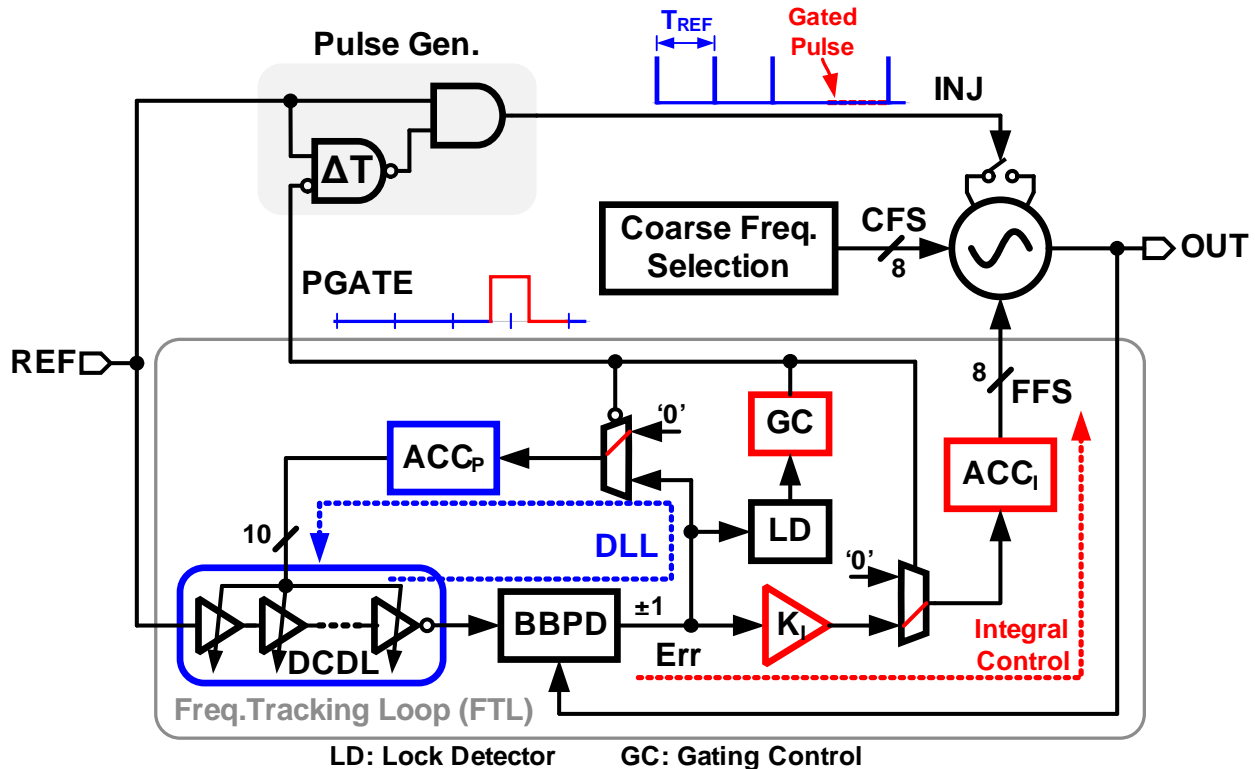
Figure 5.7: Block diagram of the proposed injection locked clock multiplier (ILCM).

ever, because of the unknown delay T_D in the pulse generator and DCO buffer, there is no pre-defined phase relationship between the DCO output and the reference (REF). Consequently, the resulting phase error, Δ_{Gated}, cannot be directly attributed to F_{ERR}. To mitigate this, a delay locked loop (DLL) consisting of the sub-sampling BBPD and accumulator (ACC_P) tunes the delay of a digitally controlled delay line (DCDL) such that BBPD inputs are aligned. The frequency tracking path is enabled after the DLL is locked and the BBPD output is integrated only when the injection path is gated. Note that because the same BBPD is used in the DLL and FTL, its offset is not critical.

The proposed FTL architecture resembles a delay/phase-locked loop (D/PLL) architecture [110] in which the proportional control is implemented in phase domain using accumulator ACC_P and integral control using accumulator ACC_I. Both control paths operate simultaneously but in an orthogonal manner; the integral control is updated only when injection is gated, while the DLL accumulator is updated when injection pulses are applied. The DLL has to be faster than the frequency tracking path for accurate frequency error

detection and to guarantee stable operation. The gating rate is made programmable and can take three values in the prototype (1/2, 1/4, 1/8). Lower gating rate is sufficient because FTL needs only to track slow variations caused by changes in voltage and temperature.

5.3.3   Phase Domain Response (PDR) Analysis

Pulse injection into an oscillator will perturb both amplitude and phase of the oscillator. Because of the amplitude limiting dynamics of the oscillator, amplitude variations due to pulse injection will decay rapidly in a couple of oscillator cycles. On the other hand, phase fluctuations persist indefinitely as was shown in [111]. It can be shown that an injection pulse that is in the form of small current impulse will only change the voltage across the capacitor (V_c) and will not affect the current through the inductor [111]. The resultant oscillator phase change will depend on the position of the pulse with respect to the oscillator phase. For example, a pulse injected near the zero crossing of V_c will have a strong effect on phase and negligible effect on amplitude. Injection when V_c is near its peak will mainly cause amplitude change and minimal phase shift. This means pulse injection into oscillator is a time variant process as described by the impulse sensitivity function (ISF) introduced by Hajimiri in [111] for phase noise analysis. In [112], a phase domain model for injection locked oscillator (ILO) based on ISF is introduced. Dunwell [113] shows that the ISF approach is limited to small-signal analysis and cannot model ILO under large-signal injection.

In [113, 114], transient simulations were used to describe ILO's large-signal phase domain response (PDR) under different injection conditions. A closed-form expression for PDR when the injection pulse is narrow was reported in [100]. These expressions become inaccurate under strong injection especially when the injection pulse width (D) is comparable to the oscillator period. Furthermore, the asymmetric nature of ILO described in [113] is not captured. In view of these drawbacks, we seek to develop accurate analysis for large-signal PDR under different injection conditions.

The oscillator can be represented by the half circuit shown in Fig. 5.8(a) where the injection switch is modeled by its on resistance (R_{sw}). The tank losses are represented by parallel resistance (R_p) and the oscillator free-running frequency is equal to $\omega_o = 1/\sqrt{LC}$. The
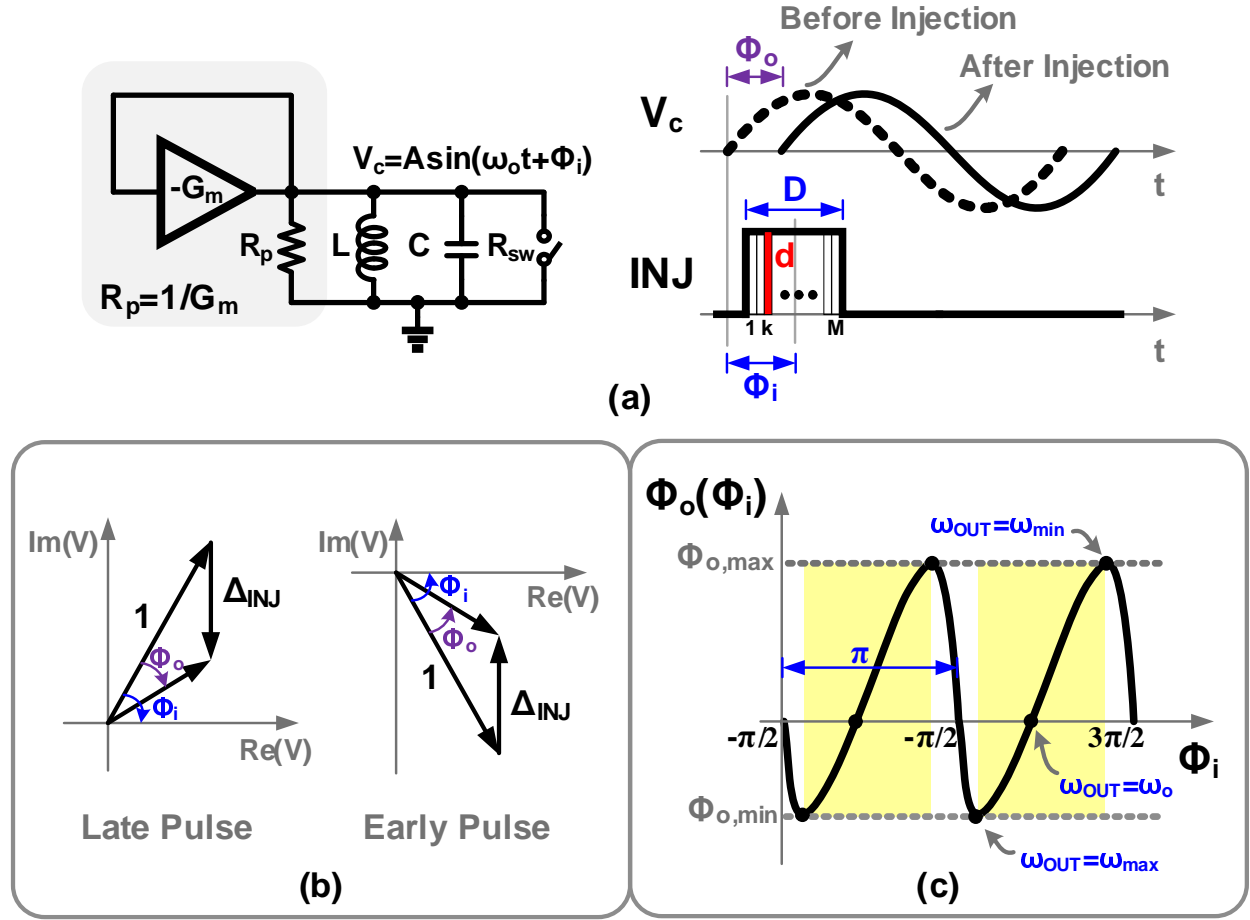
Figure 5.8: PDR analysis. (a) LC oscillator simplified half circuit with an illustrating timing diagram, (b) voltage phasor diagram, and (c) PDR diagram.

injection pulse whose width is D will cause the switch to turn on and change the voltage across the capacitor (V_c). Assuming $R_{sw} \ll R_p$, this circuit can be further simplified as a simple RC circuit because current through the inductor is not affected and R_p can be ignored [99, 111]. Input phase (Φ_i) is defined as the phase difference between the center of the injection pulse and the oscillator phase, and the output phase (Φ_o) represents the change in oscillator phase after it is pulled towards the injection pulse as illustrated by Fig. 5.8(a). The voltage change across the capacitor due to injection will depend on the time constant ($\tau = R_{sw}C$), the capacitor voltage (V_c) during injection, and pulse width (D). Without injection, the capacitor voltage can be expressed as $V_c(t) = A\sin(\omega_o t + \Phi_i)$, where A is the oscillation amplitude. When the injection pulse width is much less than the oscillator period (i.e. $D\omega_o \ll 2\pi$), the capacitor voltage can be approximated by a constant during injection

(i.e. from $-D/2$ to $D/2$) as $V_{c,inj} = V_c(0) = A\sin(\Phi_i)$. Consequently, the voltage change due to injection can be approximated as $\Delta V = V_{c,inj}(1 - e^{-D/\tau})$ as in [100].

However, this narrow pulse analysis is not accurate because it ignores the change of $V_c(t)$ during the duration of the injection pulse. In order to account for the effect of the pulse width correctly, we divide the injection pulse into M infinitesimally small pulses, each having a width of $d = D/M$ (see Fig. 5.8(a)). Each of the kth pulse causes a change in V_c by δv_k. By summing the changes δv_k from each pulse, the total change in capacitor voltage can be calculated accurately. As $d\omega_o \ll 2\pi$, δv_k can be expressed as:

$$\delta v_k = V_{c,k}\left(1 - e^{-d/\tau}\right) \approx V_{c,k}\frac{d}{\tau} \tag{5.1}$$

where $V_{c,k}$ is the capacitor voltage when pulse k is applied. The phase component of $V_{c,k}$ will depend on the position (x) of pulse k, and as x increases the phase difference between thin pulse k and oscillator zero crossing decreases. So when pulse position x changes from 0 to D, $V_{c,k}$ phase will change from $\Phi_i + 0.5\,\omega_o D$ to $\Phi_i - 0.5\,\omega_o D$ as illustrated in Fig. 5.8(a). $V_{c,k}$ can be expressed as follows:

$$x = 0 \quad \Rightarrow \quad V_{c,0} = A\sin(\Phi_i + 0.5\,\omega_o D) \tag{5.2}$$

$$x = d \quad \Rightarrow \quad V_{c,1} = A\,e^{-d/\tau}\sin(\Phi_i + 0.5\,\omega_o D - \omega_o d) \tag{5.3}$$

$$x = kd \quad \Rightarrow \quad V_{c,k} = A\,e^{-kd/\tau}\sin(\Phi_i + 0.5\,\omega_o D - \omega_o kd) \tag{5.4}$$

Consequently, we can express the normalized total change in capacitor voltage due to injection as:

$$\Delta_{INJ} = \frac{1}{A}\sum_k \delta v_k \cos(\omega_o kd) = \frac{1}{A}\sum_k V_{c,k}\frac{d}{\tau}\cos(\omega_o kd)$$

$$= \sum_k e^{-kd/\tau}\sin(\Phi_i + 0.5\,\omega_o D - \omega_o kd)\cos(\omega_o kd)\frac{d}{\tau} \tag{5.5}$$

The $\cos(\omega_o kd)$ term is added to account for the phase difference between pulses, as δv_k are summed as vectors. As $d \to 0$, the summation can be transformed into integration from

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$x = 0$ to $x = D$ where $x = kd$.

$$\Delta_{\mathrm{INJ}}(\Phi_i) = \frac{1}{\tau} \int_0^D e^{-x/\tau} \sin(\Phi_i + 0.5\,\omega_o D - \omega_o x)\cos(\omega_o x)\,dx \tag{5.6}$$

$$\Delta_{\mathrm{INJ}}(\Phi_i) = \frac{1}{2}\sin(\Phi_i + \frac{\omega_o D}{2})(1 - e^{-D/\tau}) - \frac{1}{2 + 8\omega_o^2 \tau^2} \times$$
$$\left[2\omega_o\tau\cos(\Phi_i + \frac{\omega_o D}{2}) - \sin(\Phi_i + \frac{\omega_o D}{2}) - e^{-D/\tau}\left(2\omega_o\tau\cos(\Phi_i - \frac{3\omega_o D}{2}) - \sin(\Phi_i - \frac{3\omega_o D}{2})\right)\right] \tag{5.7}$$

Once $\Delta_{\mathrm{INJ}}(\Phi_i)$ is obtained, a phasor diagram for the oscillator under injection can be drawn as shown in Fig. 5.8(b) as in [100, 115]. The center of the pulse is assumed as the reference phase. Using simple trigonometry the phase domain response (PDR) that defines the relation between input phase (Φ_i) and output phase (Φ_o) can be deduced as follows:

$$\Phi_o = \Phi_i - \tan^{-1}(\tan(\Phi_i) - \Delta_{\mathrm{INJ}} \times \sec(\Phi_i)) \tag{5.8}$$

Figure 5.8(c) illustrates an example of a PDR diagram where Φ_o is drawn as a function of Φ_i. A few insightful observations can be deduced from this diagram. First, PDR is a periodic function with a period of π. This indicates that pulse injection stimulates positive and negative edges of the oscillator equally. Consequently, the pulse can be locked to either positive or negative edges depending on the initial input phase $\Phi_{i,init}$. This may create a $\pm\pi$ phase ambiguity in the output phase, which has to be taken into consideration in applications that require output phase to be deterministic. Second, we can observe that Φ_o goes to zero when Φ_i gets close to $\pm\pi/2$. At these points, the oscillator output voltage will be at peaks or troughs where injection pulse will cause minimal phase change, but can cause significant change in amplitude. The injection strength (β) defined as the slope of the PDR and can be expressed as follows:

$$\beta(\Phi_i) = \frac{d\Phi_o}{d\Phi_i} = 1 - \frac{\sec(\Phi_i)^2 - \Delta'_{\mathrm{INJ}}\sec(\Phi_i) - \Delta_{\mathrm{INJ}} \times \sec(\Phi_i)\tan(\Phi_i)}{1 + (\tan(\Phi_i) - \Delta_{\mathrm{INJ}}\sec(\Phi_i))^2} \tag{5.9}$$

where Δ'_{INJ} is the first derivative of (5.6). From the PDR, we can intuitively understand the dynamics of injection locking. When $F_{\text{ERR}} = 0$, pulses injected at reference rate with an initial phase of $\Phi_{\text{i,init}}$ will pull the oscillator phase by $\Phi_{\text{o}}(\Phi_{\text{i,init}})$, so that the next injection pulse will have a smaller Φ_{i}. In steady state, Φ_{o} reaches zero and the settling behavior depends on $\Phi_{\text{i,init}}$ and Δ_{INJ}. In case $F_{\text{ERR}} \neq 0$, the accumulated phase error ($2\pi\alpha_{\text{E}}N$), where $\alpha_{\text{E}} = F_{\text{ERR}}/F_{\text{OUT}}$, in each injection period has to be compensated to maintain the lock condition, in steady state. By treating each period of the injected signal as a discrete-time event [92, 113], sub-harmonic ILO behavior can be described using:

$$\Phi_{\text{i}}[n+1] = \Phi_{\text{i}}[n] - \Phi_{\text{o}}[n] - 2\pi\alpha_{\text{E}}N \tag{5.10}$$

where in steady state, the injection pulse will be locked with the oscillator, and their phase difference will be fixed and reach a steady state value (i.e. $\Phi_{\text{i}}[n+1] = \Phi_{\text{i}}[n] = \Phi_{\text{i,ss}}$). The steady state condition $\Phi_{\text{i,ss}}$ depends on the amount of excess phase required to compensate for frequency error as $\Phi_{\text{o}}(\Phi_{\text{i,ss}}) = -2\pi\alpha_{\text{E}}N$. From the PDR, we can find $\Phi_{\text{o,max}}$ and $\Phi_{\text{o,min}}$ where there is no injection strength $\beta(\Phi_{\text{i}}) = 0$ (see Fig. 5.8(c)). Then the lock-in boundaries can be deduced from $\alpha_{\text{E,max}} = -\Phi_{\text{o,min}}/(2\pi N)$ and $\alpha_{\text{E,min}} = -\Phi_{\text{o,max}}/(2\pi N)$.

To validate the accuracy of the proposed analysis, PDR is extracted using transient simulations, similar to [113, 114], for an 8GHz LC oscillator under injection. As shown in Fig. 5.9, the PDR simulation results match theoretical analysis for various pulse widths (D) and switch resistances (R_{sw}). Even in case of a very strong injection ($R_{\text{sw}}=10\Omega$ and $\beta \to 1$) as shown in Fig. 5.9(c), the analysis captures ILO's non-linear behavior accurately. The asymmetric nature of the PDR can be readily observed especially as D increases (see Fig. 5.9(b)). Because of the finite width of the pulse, pulse injection ability in delaying the oscillator phase is higher than advancing it. This asymmetry is captured accurately using the proposed analysis compared to the analysis with thin pulse assumption [100].
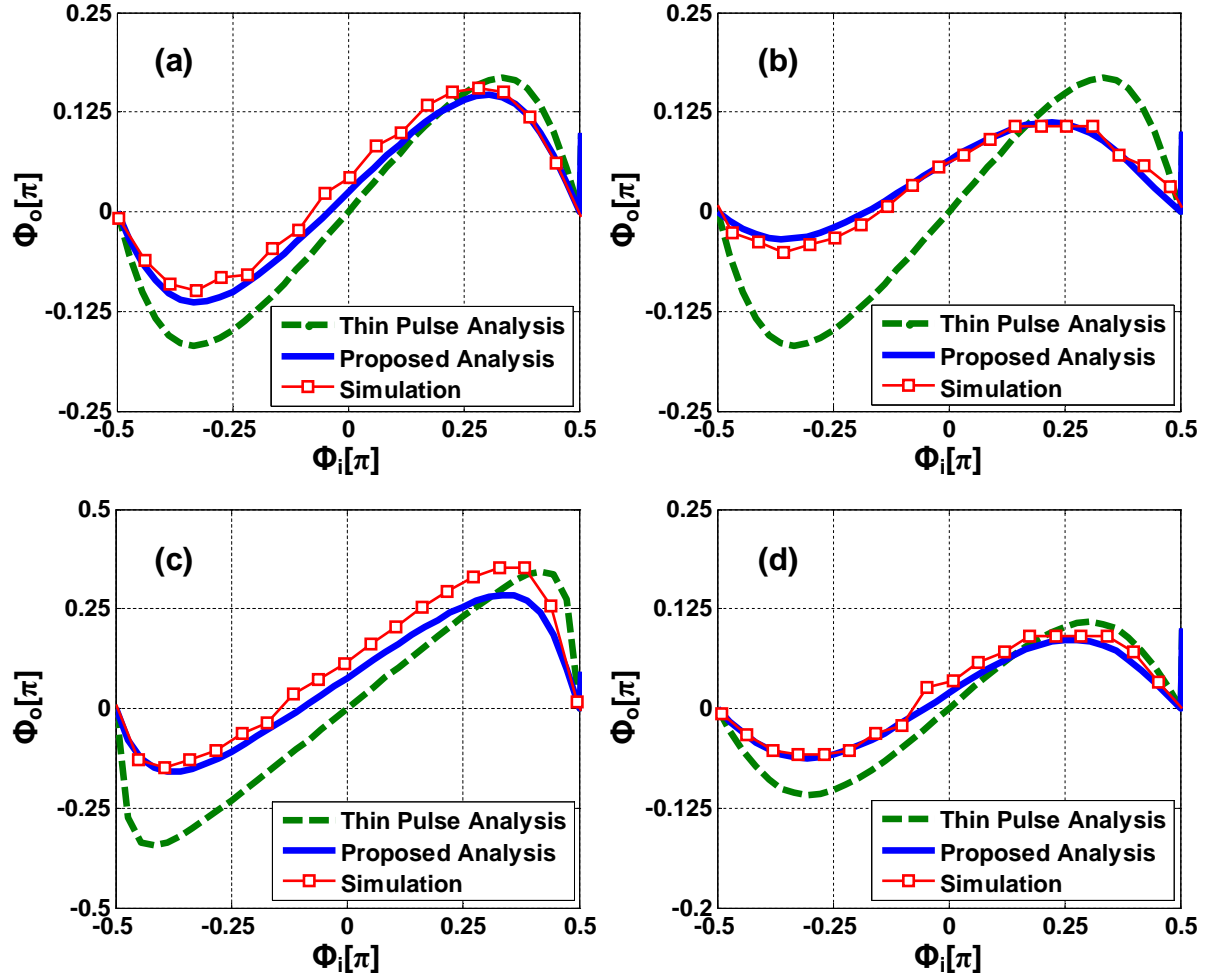
Figure 5.9: PDR analysis and simulation results in case (a) R_{sw}=20Ω, D=20ps, (b) R_{sw}=40Ω, D=40ps, (c) R_{sw}=10Ω, D=25ps, and (d) R_{sw}=40Ω, D=25ps.

5.3.4 Phase Noise Analysis

In this section, we will analyze the phase noise behavior of sub-harmonic ILO, then employ it in a complete linear model for the whole ILCM architecture. Fig. 5.10(a) depicts a phase domain model of sub-harmonic ILO based on (5.10) [92, 113]. For the purpose of noise analysis, the non-linear PDR can be substituted by its slope $\beta(\Phi_{i,ss})$ where $\Phi_{i,ss}$ is a function of frequency error α_E. Reference clock and DCO phase noise are represented by their respective power spectral densities $S_{\Phi_{nR}}$ and $S_{\Phi_{nDCO}}$. The total output phase noise

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$S_{\Phi_{OUT}}$ can be calculated using:

$$S_{\Phi_{OUT}} = \left| \frac{N \, \beta(\alpha_E)}{1 - (1 - \beta(\alpha_E)) \, z^{-1}} \right|^2 S_{\Phi_{nR}} + \left| 1 - \frac{\beta(\alpha_E) \, z^{-1}}{1 - (1 - \beta(\alpha_E)) \, z^{-1}} \right|^2 S_{\Phi_{nDCO}} \qquad (5.11)$$

where reference phase noise is low-pass filtered and DCO phase noise is high-pass filtered before they appear at the output. The filter bandwidth depends on the injection strength $\beta(\alpha_E)$. From the PDR analysis, as frequency error deviates from zero, $\beta(\alpha_E)$ drops and accordingly the filtering bandwidth drops and the phase noise performance is degraded. Recently, rigorous phase noise analysis of ILO in [114] predicts the existence of the additional contribution due to power spectrum folding of oscillator phase noise. This arises from the sub-sampling of noise operated by pulse injection and it degrades the output phase noise over free-running phase noise at offset frequencies near F_{REF} by almost 3dB [114].

Fig. 5.10(b) shows the discrete-time phase-domain linear model of the ILCM. This linear model is used for stability and noise analysis of the ILCM system. Unlike a PLL, the oscillator tracks the reference clock through two paths: injection path and tuning path. The sub-harmonic ILO model is simplified as a discrete-time integrator and a delay element. The frequency tracking loop (FTL) behaves as a bang-bang DFLL. The frequency tuning of DCO is modeled as an integrator in z-domain with gain $2\pi K_F T_R$, where K_F [Hz/LSB] is the DCO gain and $T_R = 1/F_{REF}$ is the reference period. The BBPD is represented by its linearized gain (K_{BBPD}). As the DCDL delays the reference clock before BBPD, it can be modeled as a combination of a summing block and a gain K_{DL} [rad/LSB]. The DLL and frequency tuning accumulators have transfer functions of $H_p(z)$ and $H_i(z)$ respectively. The DLL random and quantization noise sources are modeled as input-referred phase noise with power spectral density $S_{\Phi_{nDLL}}$, while DCO quantization noise has a power spectral density $S_{Q_{DCO}}$. The total output phase noise $S_{\Phi_{OUT}}$ can be calculated using:

$$S_{\Phi_{OUT}} = |NTF_R(z)|^2 \, S_{\Phi_{nR}} + |NTF_{DCO}(z)|^2 \, S_{\Phi_{nDCO}} + \left| NTF_{DCO}(z) \times \left(\frac{2\pi K_F T_R}{1 - z^{-1}} \right) \right|^2 S_{Q_{DCO}}$$

$$+ \left| NTF_{DCO}(z) \, H_{DLL}(z) \, H_i(z) \times \left(\frac{2\pi K_F T_R}{1 - z^{-1}} \right) \right|^2 S_{\Phi_{nDLL}} \quad (5.12)$$

(a)

(b)
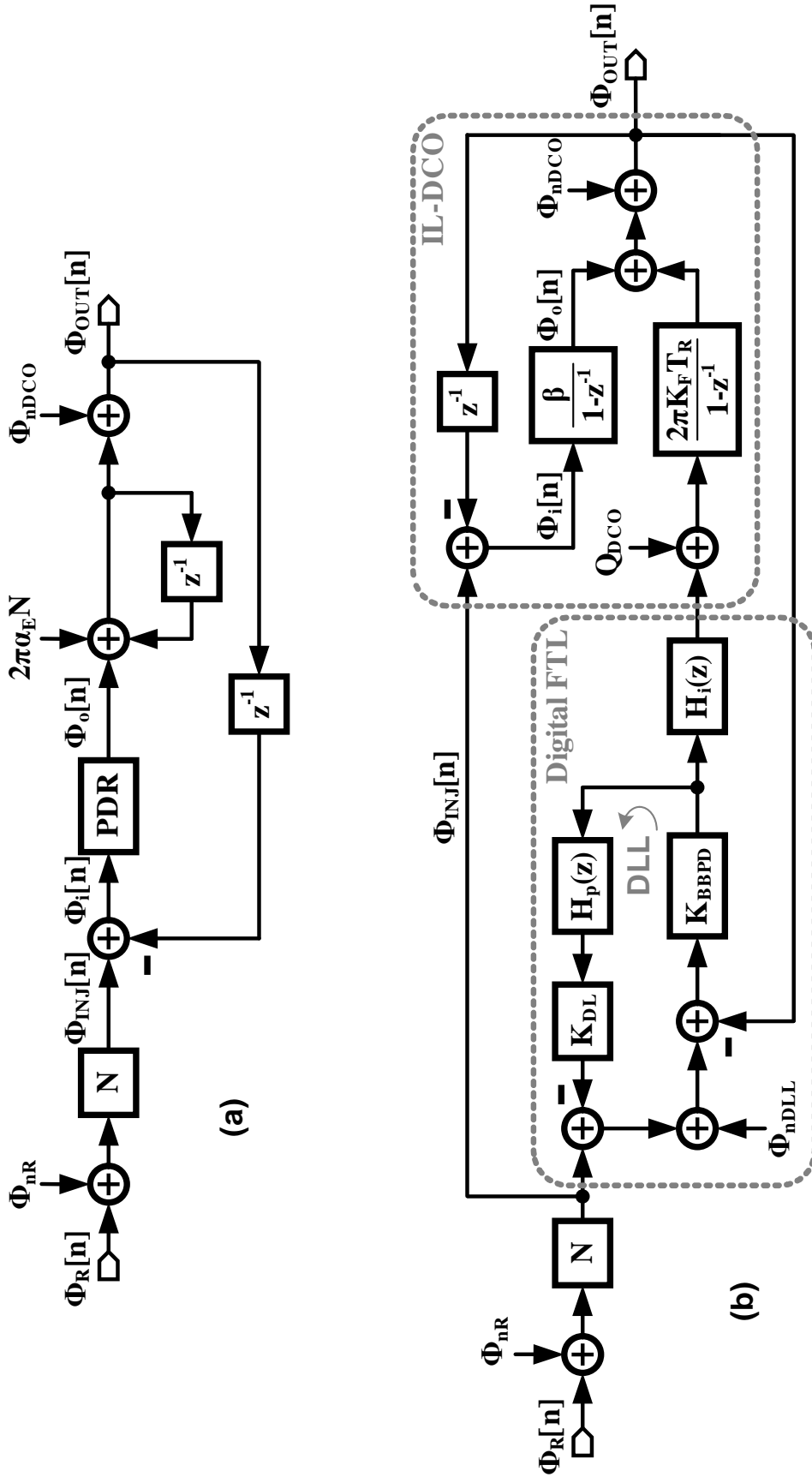
Figure 5.10: (a) Phase-domain model of sub-harmonic ILO, and (b) discrete-time phase-domain model of the proposed ILCM.

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where $\text{NTF}_\text{R}(z)$ and $\text{NTF}_\text{DCO}(z)$ are the noise transfer functions of reference and DCO phase noise respectively. Because the injection path has a much higher bandwidth than the tuning path, $\text{NTF}_\text{R}(z)$ and $\text{NTF}_\text{DCO}(z)$ can be approximated as in (5.11). The $\text{H}_\text{DLL}(z)$ represents a high-pass transfer function of the DLL:

$$H_\text{DLL}(z) = \frac{K_\text{BBPD}}{1 + K_\text{BBPD}\, K_\text{DL}\, H_\text{p}(z)} \tag{5.13}$$

Because of the low bandwidth of the frequency tuning path, the FTL noise is filtered, such that the output phase noise is mainly determined by reference and oscillator phase noise. The analysis shows the great dependence of ILCM phase noise performance on the relative frequency error (α_E). As $\text{NTF}_\text{R}(z)$ and $\text{NTF}_\text{DCO}(z)$ depend on the injection strength ($\beta(\alpha_\text{E})$), the phase noise performance is degraded considerably as α_E deviates from zero. This illustrates the importance of the proposed FTL to achieve robust operation and excellent performance across voltage and temperature variations.

5.4   Building Blocks

5.4.1   DCO

The schematic of the 16-bit LC DCO is shown in Fig. 5.11. It consists of an NMOS cross-coupled pair, a resistive bias network, a PMOS injection switch, and a high Q LC tank. A single-turn center-tapped 425pH inductor is implemented using ultra-thick metal layer to maximize its quality factor. This helps to reduce DCO's power consumption and temperature sensitivity. The tail bias current is controlled digitally by RDAC[2:0]. Frequency tuning is realized using two MOS capacitor banks (8-bit coarse and 8-bit fine). The coarse capacitor bank is implemented using binary weighted MOS capacitors to tune the frequency from 6.75GHz to 8.25GHz with a step size of about 6MHz. The fine capacitor bank is implemented using minimum size devices to achieve fine resolution of 17ppm/LSB at 6.8GHz. Two dimensional (4x4) binary-to-thermometer decoder is used to achieve good tuning linearity with reasonable number of control lines [116]. The 4-LSBs (FFS[3:0]) are decoded to

control 16-rows via R[15:0], while the 4-MSBs (FFS[7:4]) are decoded to control 16-columns via C[15:0] and A[15:0]]. R, C, and A controls are latched outside the varactor array, to avoid any coupling between RF lines and reference clock. Even and odd local decoders with matrix switching are used to realize zigzag switching order with only one (R, C or A) control line changing at a time to eliminate any glitch. The proposed varactor control scheme guarantees monotonicity and helps to achieve excellent linearity.
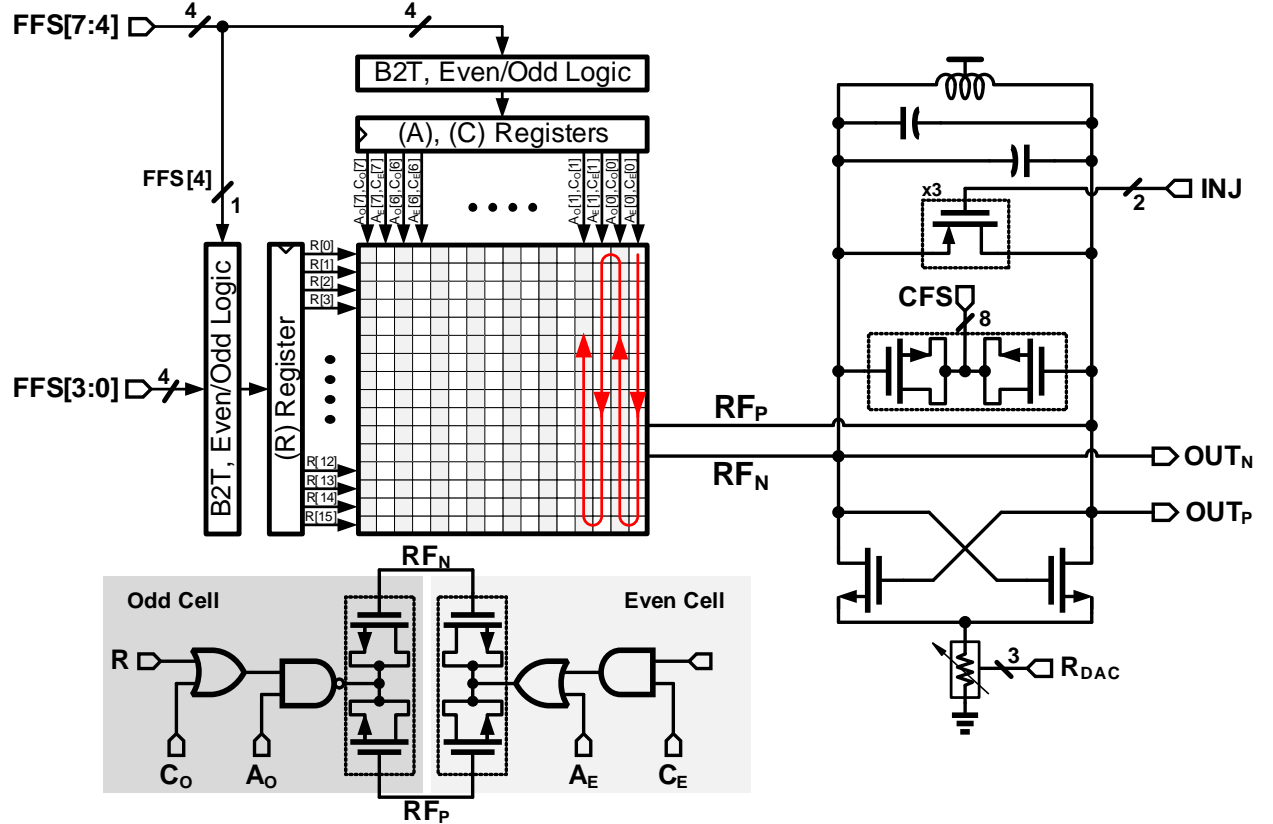
Figure 5.11: LC-based DCO implementation.

The DCO core is optimized to minimize power consumption, as the required phase noise performance is relaxed by injection locking. The DCO core consumes about 2mA from a 1V supply at 6.8GHz. Figure 5.12 shows measured and simulated results of the DCO at 6.8GHz when it is free-running and when it is injection locked (N=64) using two different widths for injection transistor. The measured free-running DCO phase noise is around -120dBc/Hz at 1MHz offset, which translates to a FoM_{VCO} of -193.6dB. We notice that injection locking increases phase noise by almost 3 dB at higher offset frequencies as demonstrated by [114].
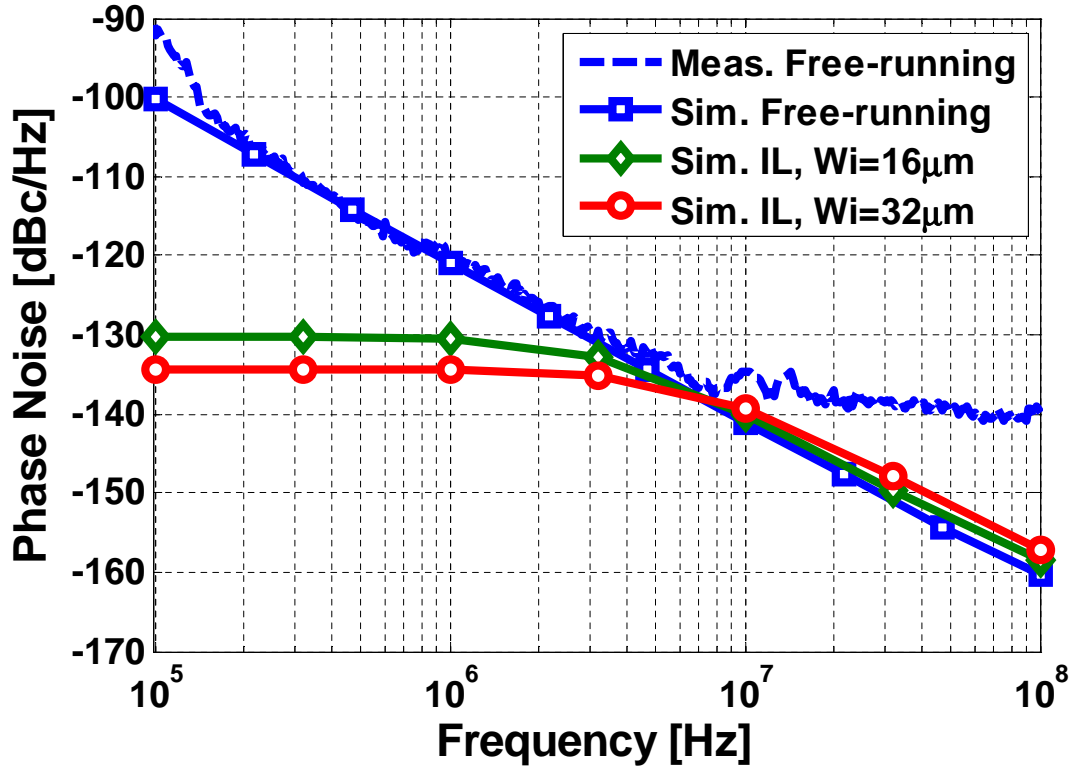
Figure 5.12: Injection locked DCO phase noise measurement and simulation results at 6.8GHz.

5.4.2 Pulse Generator and Other Blocks

The schematic of the pulse generator is shown in Fig. 5.13. It generates a narrow pulse using the positive edge of reference clock (REF) and injects it into the DCO using a 2-bit programmable PMOS switch. The pulse width can be varied from 20ps to 35ps using 4-bit digitally controlled delay cell to control injection strength and filtering bandwidth. A NOR gate implements the injection gating functionality after synchronization with REF negative edge.

The 10-bit digitally controlled delay line (DCDL) is implemented using a cascade of 16 identical delay cells similar to [27]. Each delay stage consists of an inverter loaded with a 6-bit MOS capacitor bank followed by another inverter to restore fast rise and fall times. The DCDL provides about 150ps incremental delay to ensure DLL locking at lowest DCO frequency. The sub-sampling BBPD is implemented using a sense amplifier (SA) based
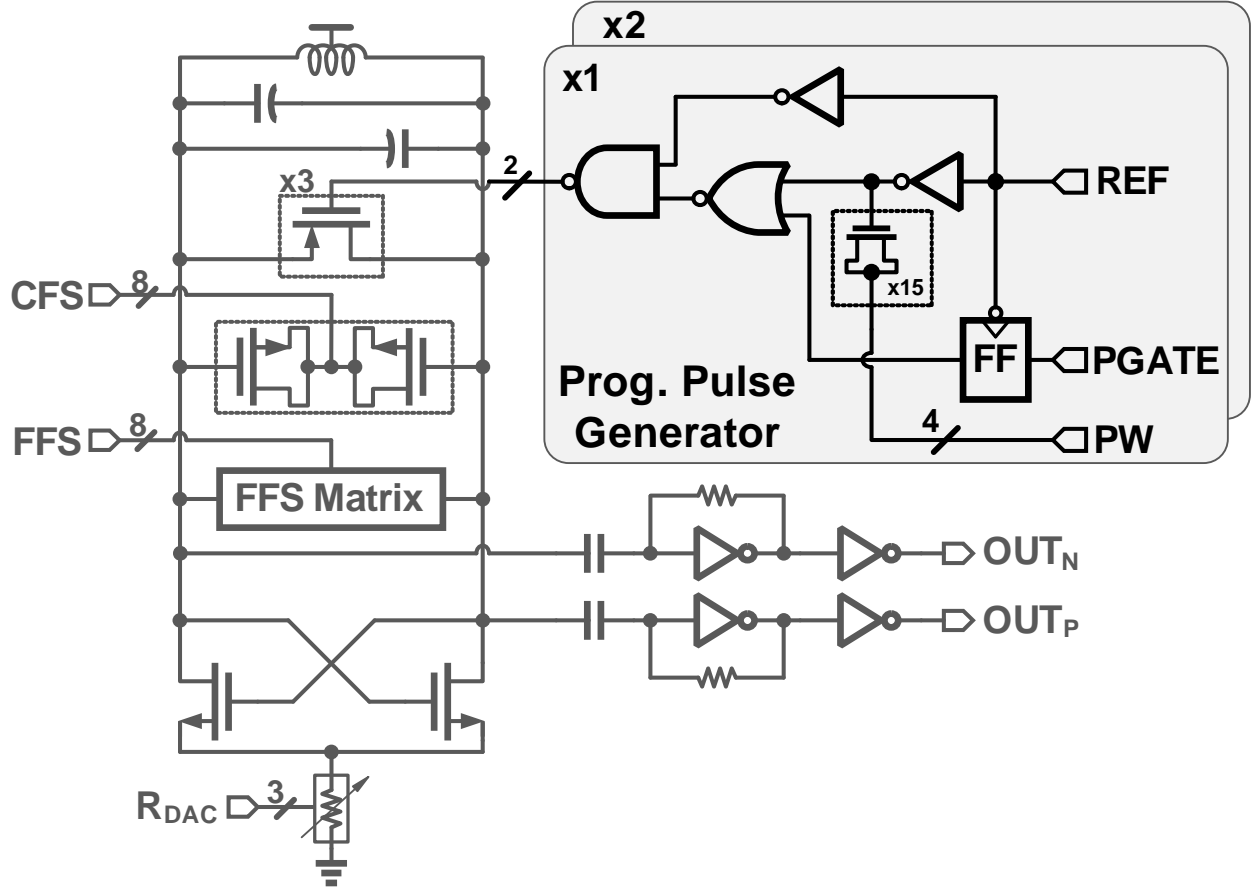
Figure 5.13: Schematic of the programmable pulse generator.

flip-flop followed by a symmetric latch to minimize the hysteresis [117].

5.5 Measurement Results

The proposed injection locked clock multiplier depicted in Fig. 5.7 was fabricated in 65nm CMOS process and its die photograph is shown in Fig. 5.14. It occupies 0.25mm^2 active area. The total power consumption is less than 2.25mW at a supply voltage of 0.9V, of which the DCO and its buffer consume less than 1.8mW. The chip is characterized using Agilent N9000A spectrum analyzer (SA) and Agilent E5052B signal source analyzer (SSA). The measured coarse tuning curve of the DCO is shown in Fig. 5.15(a). The output frequency is tuned from 6.75GHz to 8.25GHz by steps of 6MHz by controlling the 8-bit coarse capacitor bank. A small coarse step is employed to guarantee at least 200% overlap between

coarse and fine tuning curves. The fine tuning characteristics is measured at 6.8GHz, where the approximate frequency resolution (1LSB) is 115kHz (17ppm). The measured differential non-linearity (DNL) and integral non-linearity (INL) of the fine tuning are shown in Fig. 5.15(b). The effectiveness of the proposed zigzag switching order is validated by the excellent DNL/INL performance. The DNL measurement also includes error due to the free-running DCO noise. The sensitivity of the DCO to voltage and temperature variations is measured and the results are shown in Fig. 5.16. When the supply voltage is varied from 0.85 to 1.15V, the frequency only changes by less than $\pm0.25\%$ when the output frequency is 6.75GHz. This variation is largely due to change in the DCO amplitude with the supply due to the resistive bias network. The variation across temperature is less than $\pm0.20\%$ at 8.25GHz and improves as the tank capacitance increases to less than $\pm0.125\%$ at 6.75GHz.
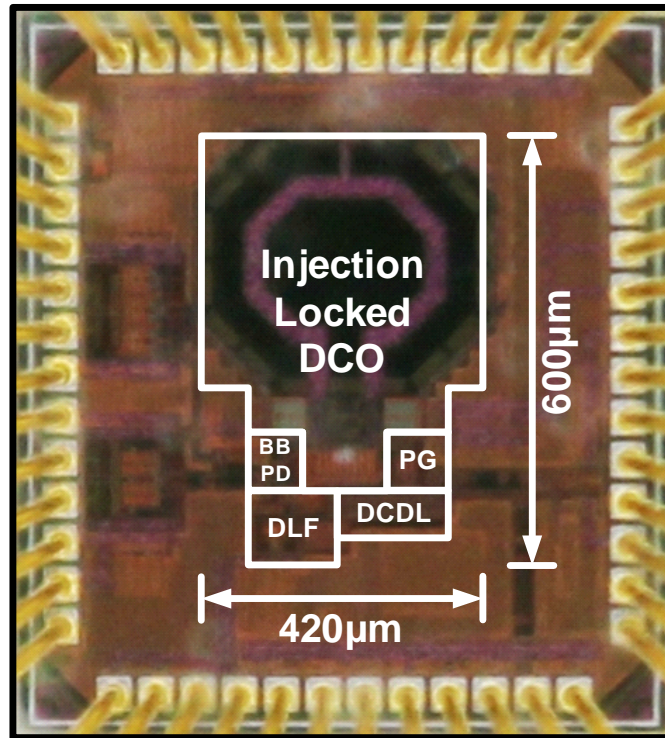
Figure 5.14: Die photograph.

The performance of the ILCM is characterized using an external 106.25MHz reference clock that has about $0.36\text{ps}_{\text{rms}}$ measured integrated jitter from 10kHz to 40MHz and a noise floor of -150dBc/Hz as shown in Fig. 5.17. The measured phase noise of the open loop ILCM without FTL at 6.8GHz is depicted in Fig. 5.17. In case of a zero F_{ERR} and 64

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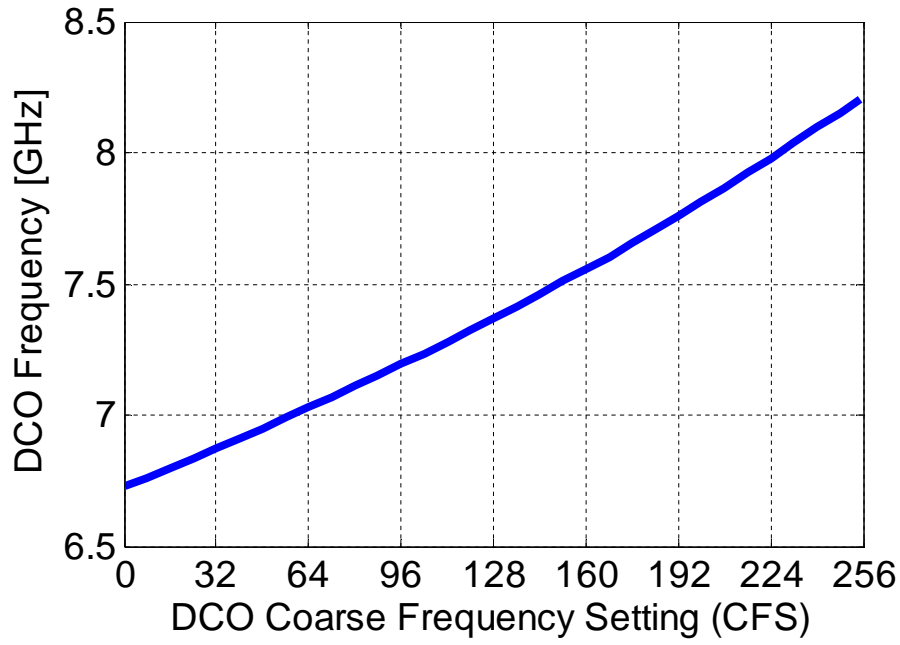
(a)
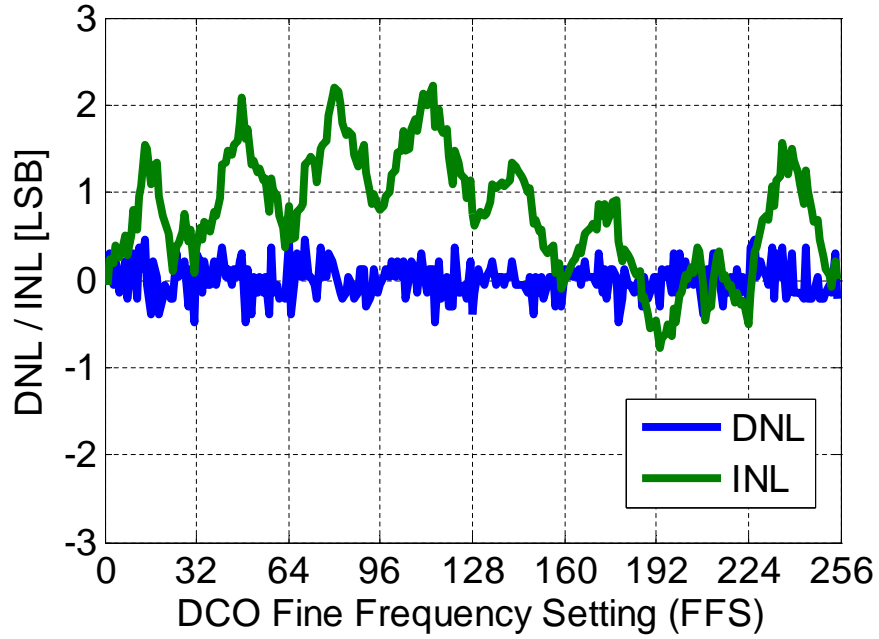
(b)

Figure 5.15: Measured DCO tuning characteristics: (a) coarse tuning, (b) fine tuning DNL/INL.

multiplication factor, an excellent jitter of 173fs$_{rms}$, integrated from 10kHz to 100MHz, is

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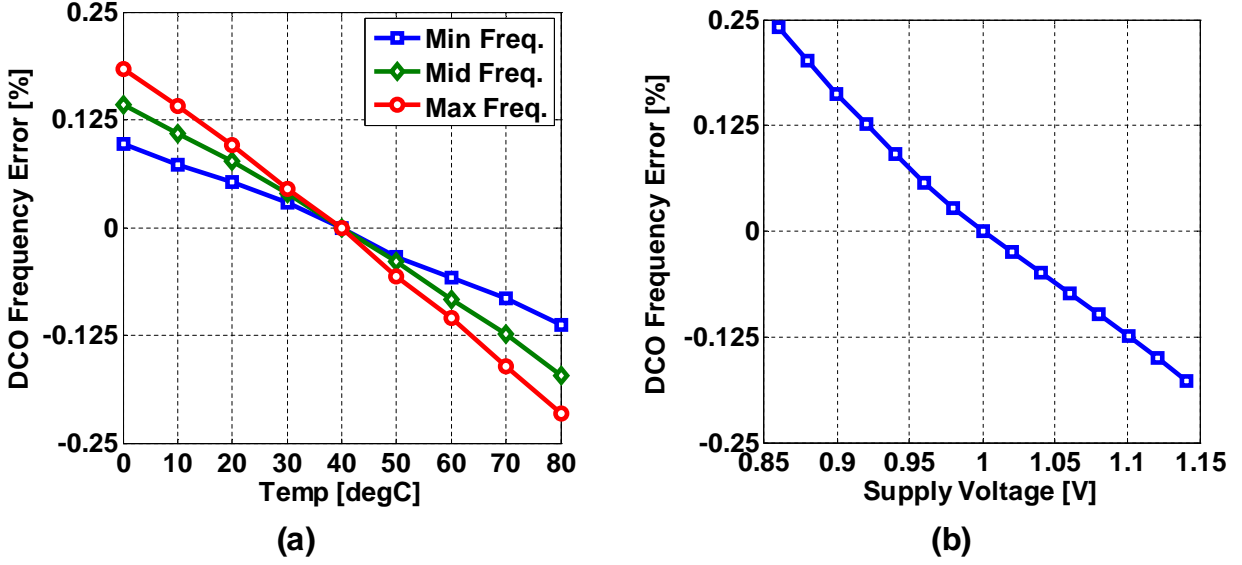
Figure 5.16: Measured DCO free-running frequency across (a) temperature, and (b) supply.

achieved, which is limited only by the reference clock noise. However, in the presence of a frequency error F_{ERR}, the performance of the open loop oscillator degrades considerably as depicted in Fig. 5.18(a). The integrated jitter increases from $173fs_{rms}$ to about $314fs_{rms}$ when $F_{ERR}=360ppm$. When the frequency tracking loop is enabled using a pulse gating rate of $1/8$, F_{ERR} is corrected and the excellent jitter performance is recovered. The integrated jitter is about $184fs_{rms}$, independent of F_{ERR}. This indicates that FTL adds less than $50fs_{rms}$ of noise to the ILCM. Similar jitter performance is achieved across the entire frequency range. Figure 5.18(b) shows the measured phase noise plots at 8GHz with FTL and without FTL ($F_{ERR} = 0$). We also observe that pulse gating ($= 1/4$) causes slight reduction in the noise filtering bandwidth.

The measured output spectrum of ILCM with FTL at 6.8GHz is shown in Fig. 5.19, where the measured reference spur is around -42dBc. The effectiveness of the proposed frequency tracking loop (FTL) to desensitize the performance across voltage variations is demonstrated by measuring reference spur and integrated jitter across supply voltages ranging from 0.88V to 1.08V (see Fig. 5.20). The measured DCO free-running frequency varied by 20MHz in this range, which is about $8\times$ the lock-in range. The conventional ILCM loses lock beyond 25mV supply variation, while the proposed FTL maintains lock with an integrated jitter
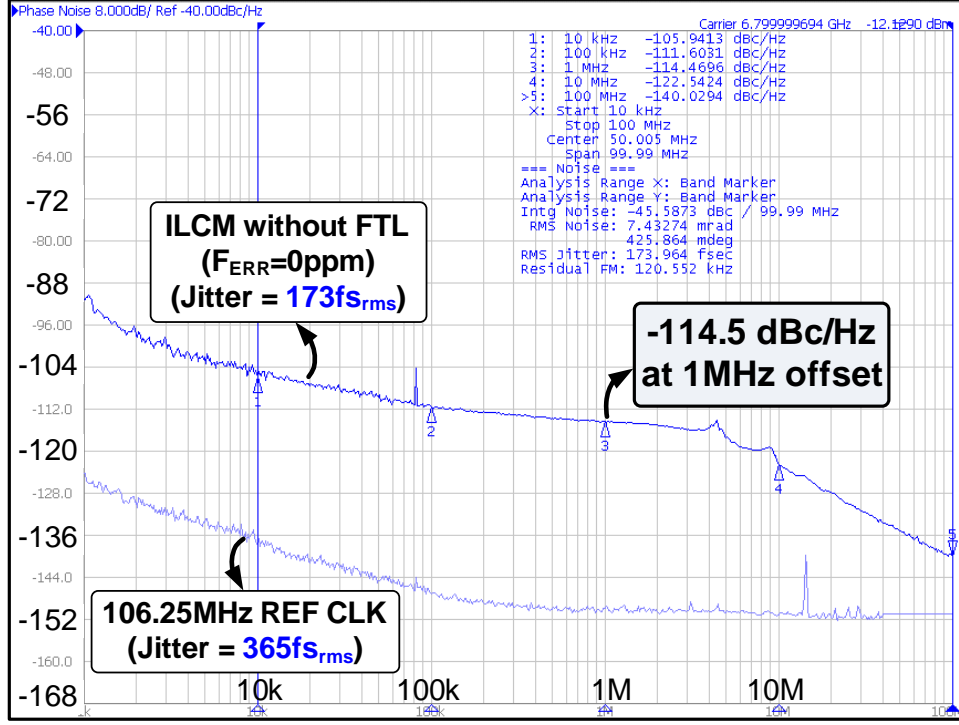
Figure 5.17: Measured phase noise of the reference clock and ILCM output without FTL in case of $F_{ERR} = 0$ at 6.8GHz.

ranging from 180fs$_{rms}$ to 215fs$_{rms}$. The measured reference spur is around -40dBc across the entire supply range.

The performance summary and comparison with state-of-the-art ILCMs are shown in Table 5.1. The proposed architecture achieves excellent jitter and spurious performance even with a large multiplication factor of 64. Compared to prior art, which either relies on a complex power hungry architecture [99] or sensitive analog approaches [100, 101], the proposed frequency tracking loop is based on a simple and accurate digital pulse gating technique that ensures robust operation across PVT variations. The proposed architecture achieves the best power efficiency of 0.33mW/GHz and the best-reported FoM$_J$ of -251dB. This FoM$_J$ is defined by [38] to reflect the jitter power trade-off in clock multipliers as plotted in Fig. 5.21(a) for state-of-the-art integer-N clock multipliers. However, in practice, achieving excellent FoM$_J$ is more challenging at higher frequencies especially as the multiplication factor (N) increases. To clarify this, Fig. 5.21(b) plots the FoM$_J$ and the output frequency of state-of-the-art integer-N clock multipliers. This work achieves at least 3dB improvement

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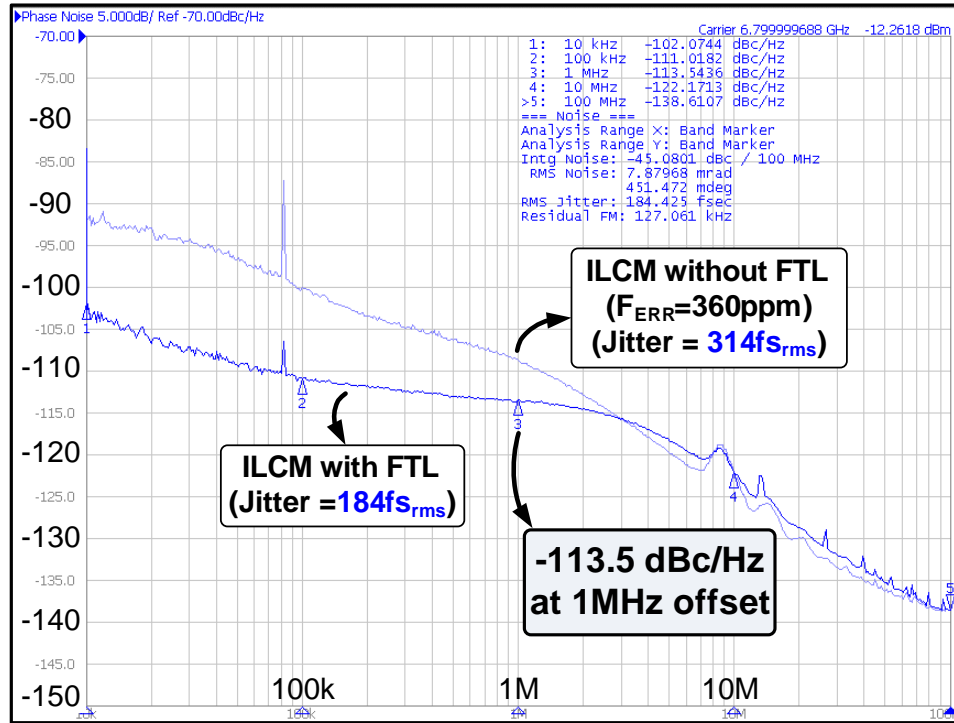
(a)
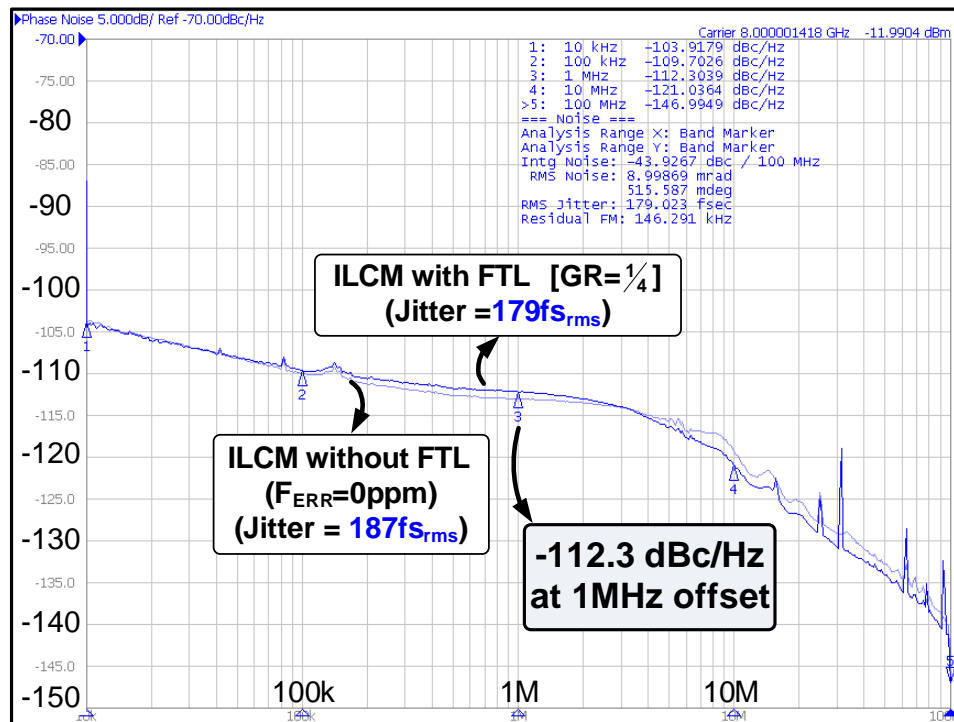
(b)

Figure 5.18: Measured ILCM phase noise with FTL at (a) 6.8GHz, and (b) 8GHz.
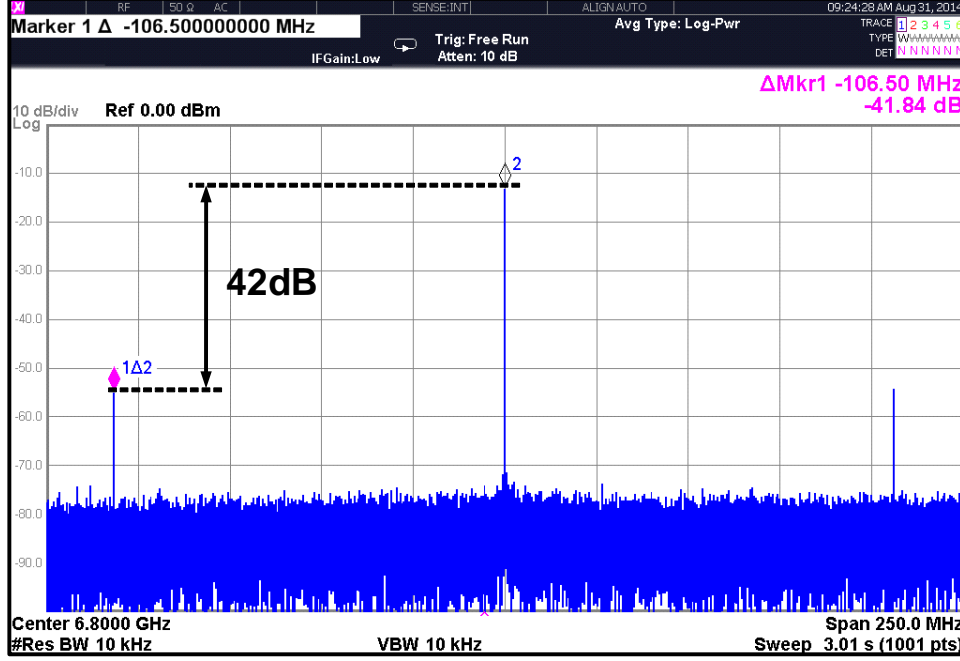
Figure 5.19: Measured output spectrum of the proposed ILCM with FTL (at 6.8GHz, N=64).

in state-of-the-art FoM_J even while using a large multiplication factor of 64.

5.6   Conclusion

Sub-harmonically injection locked clock multipliers (ILCMs) provide a simple means to achieve superior jitter performance. While ILCMs offer many advantages in terms of phase noise, power, and area compared to classical PLLs, they suffer from a narrow lock-in range especially at a large multiplication factor (N). Because of the variations in the oscillator free-running frequency, in practice the performance of ILCMs is vulnerable against process, voltage, and temperature (PVT). In this work, a low phase noise 6.75-8.25GHz injection locked clock multiplier is presented. It employs an all-digital continuous frequency tracking loop (FTL) to ensure robust operation across PVT variations even with a narrow lock-in range. This enables achieving low power operation and large multiplication factor of 64. The measured jitter is only $190fs_{rms}$ integrated from 10 kHz to 100 MHz. The power consumption is less than 2.25mW from 0.9V supply voltage for an output frequency range of

Table 5.1: ILCM Performance Summary

	Helal [99] JSSC'09	Huang [100] JSSC'13	Lee [101] ISSCC'13	Musa [97] JSSC'14	Chien [98] ISSCC'14	This Work
Architecture	LC-ILCM	LC-ILPLL	LC-ILPLL	Ring-ILCM	Ring-ILCM	LC-ILCM
Technology [nm]	130	180	65	65	20	65
Supply [V]	1.2	1.8	1.2	1.0	1.25/1.0	0.9
Output Freq. [GHz]	3.2	2.4	2.4	0.5-1.6	15	6.75-8.25
Ref. Freq. [MHz]	50	150	150	125-400	1875	105-129
Mult. Factor (N)	64	16	16	4	8	64
Ref. Spur [dBc]	-63.9	-40	-48.8	-57	-48	-40
In-band PN [dBc/Hz]*	-127	-126.5	-123.5	NA	NA	-119.2
Ref. Integrated Jitter [fs_rms]	80 1k-20MHz	75 1k-40MHz	75 1k-40MHz	NA	366 100k-1GHz	365 10k-40MHz
Output Integrated Jitter [fs_rms]	130 100-40MHz	145 1k-40MHz	188 1k-40MHz	700 10k-40MHz	268 100k-1GHz	190 10k-100MHz
Power [mW]	28.6	12.6	5.2	0.97	46.2	2.25
Power Eff. [mW/GHz]	**8.94**	**5.25**	**2.17**	**0.8**	**3.08**	**0.33**
FoM_J [dB]**	**-243**	**-246**	**-247**	**-243**	**-235**	**-251**
Continuous Frequency Tracking	Digital (GRO-TDC)	Analog PLL	Analog SSPLL	Digital (VCO Replica)	No	Digital (Pulse Gating)
Area [mm²]	0.4†	0.64	0.25	0.022	0.044	0.25

*Normalized IBPN to 3.2GHz, ** $\mathrm{FoM_J} = 10\log\left[\left(\frac{\sigma_{\mathrm{rms}}}{1\mathrm{sec}}\right)^2 \frac{P}{1\mathrm{mW}}\right]$, † Use external loop filter,
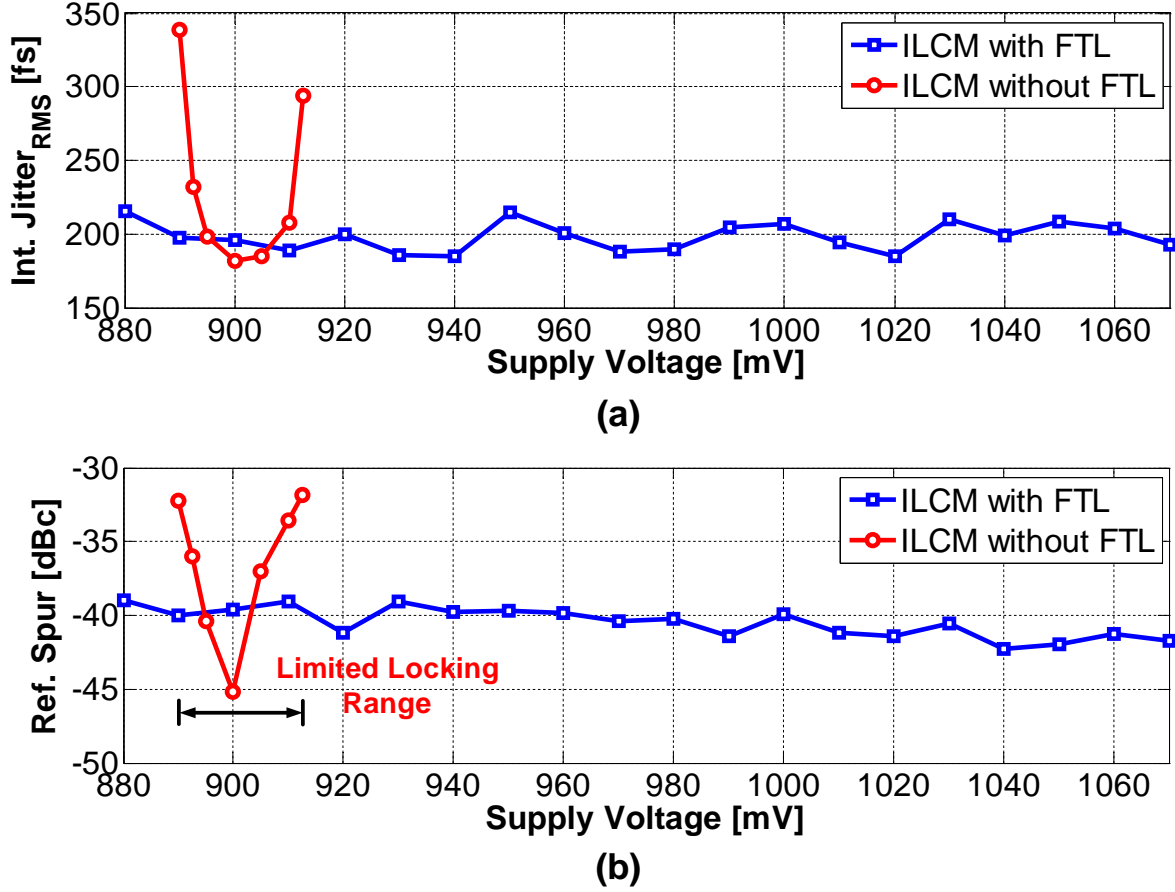
Figure 5.20: (a) Measured integrated jitter, and (b) measured reference spur versus supply voltage with and without FTL.

6.75-8.25GHz. This translates to an excellent figure-of-merit (FoM$_J$) of -251dB. This chapter also introduced an accurate theoretical analysis for phase domain response (PDR) of injection locked oscillators. Compared to ISF-based models, the proposed PDR analysis captures the large-signal behavior of pulse injection, provides accurate analytical prediction of asymmetric lock-in range, injection strength, tracking bandwidth, locking time, and phase noise performance of ILCMs.
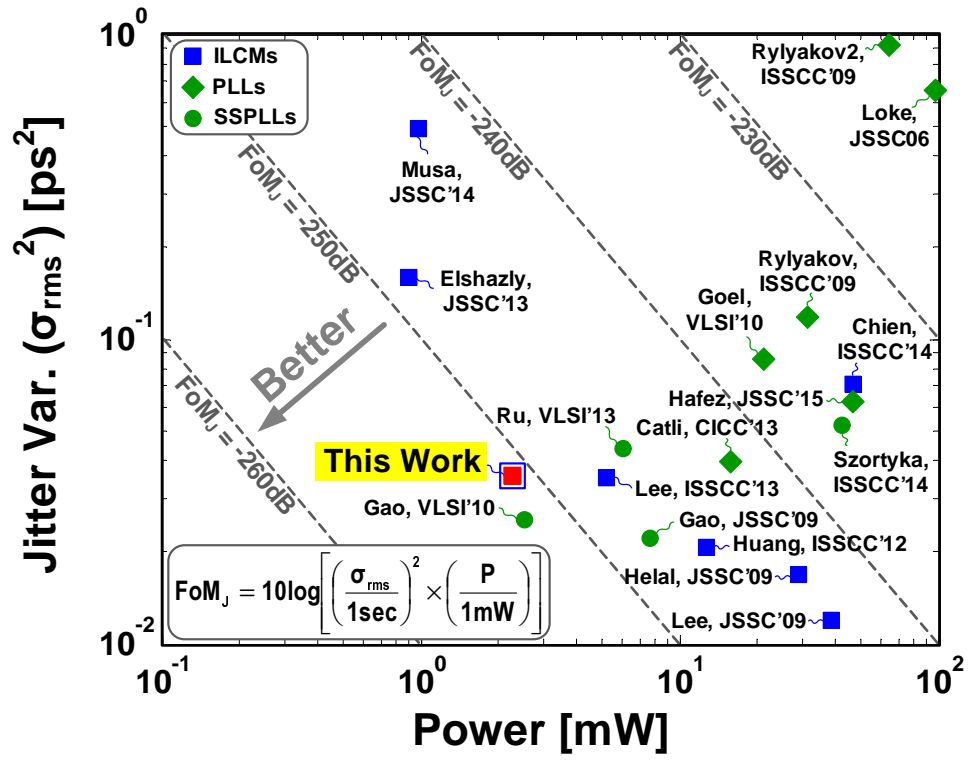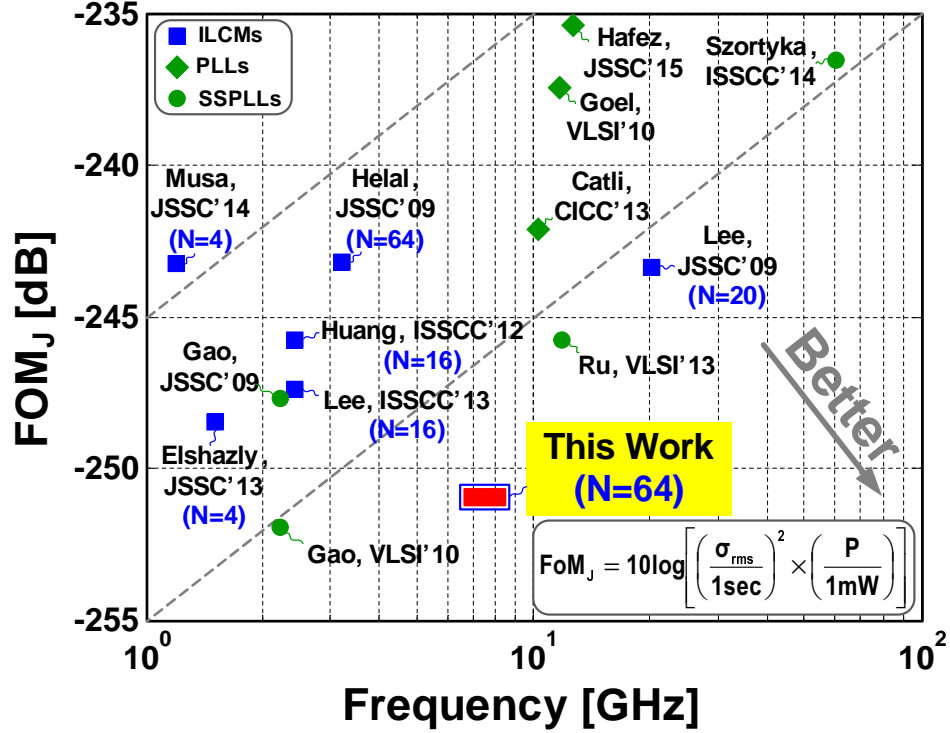
Figure 5.21: FoM comparison. (a) Jitter and power comparison and (b) FoM$_J$ as a function of output frequency.

CHAPTER 6

RAPID ON/OFF FRACTIONAL-N INJECTION-LOCKED CLOCK MULTIPLIERS

6.1 Introduction

With the continuous increase in data rates of wireline and wireless communication systems, there is a growing demand for high frequency frequency synthesizers with stringent performance requirements. Fractional-N frequency synthesizers offer full frequency planning flexibility with very fine granularity ($\sim$100Hz) using a low-frequency reference clock (F_{REF}) provided by a single crystal oscillator. However, their phase noise performance is usually compromised by the quantization noise of the fractional-N operation. In conventional phase-locked loops (PLLs), fractional divider quantization noise can be suppressed by lowering the PLL bandwidth or using quantization noise cancellation (QNC) techniques [5, 13]. But further improvement of conventional PLL phase noise performance, to achieve superior jitter performance ($<$200fs$_{rms}$), always comes with a large power consumption penalty (tens of mWs) [57, 88, 89]. This is due to the fundamental coupled noise bandwidth tradeoff between high-pass filtering of oscillator noise and low-pass filtering of noise from the other loop components such as the charge pump and divider. This imposes stringent noise requirements on the oscillator and/or loop components, thus resulting in a considerable increase in power and area. This design challenge limits the efficiency of conventional fractional-N PLLs, which is quantified by the jitter-power figure-of-merit (FoM_J) introduced in [38].

As a promising architecture to alleviate this tradeoff, sub-harmonic injection locking was proposed for low-noise clock generation [99, 102]. By directly injecting a train of narrow pulses periodically at reference frequency F_{REF} into a free-running oscillator, the oscillator

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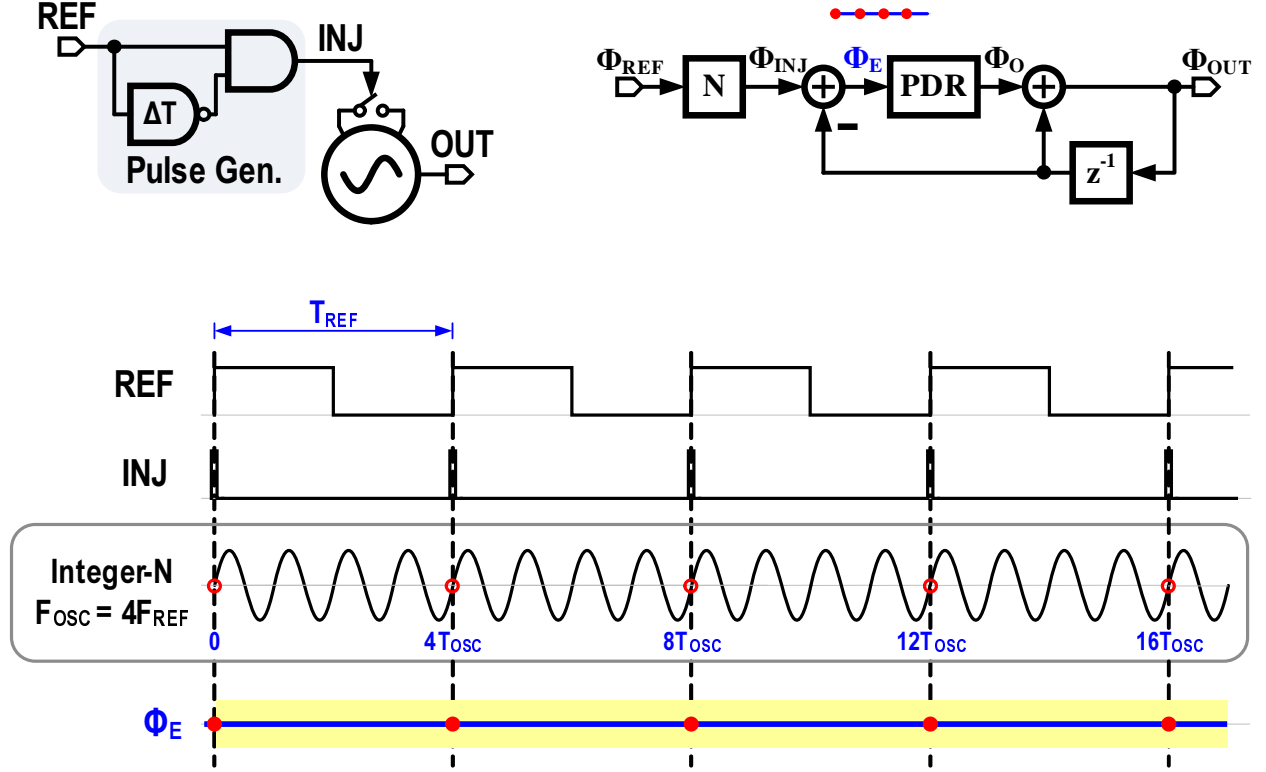
Figure 6.1: Classical ILCM for integer-N multiplication (N = 4): schematic, discrete-time model, and timing diagram.

can be locked to the Nth harmonic such that $F_{OUT} = N\,F_{REF}$ as illustrated by the timing diagram in Fig. 6.1 for N = 4. In the locked state, the oscillator tracks the reference clock and the oscillator close-in phase noise is greatly suppressed. As a result superior jitter performance that is only limited by the reference clock noise can be achieved. However, in practice the spurious and jitter performance of injection-locked clock multipliers (ILCMs) is sensitive to any frequency error between the oscillator free-running frequency F_{FR} and the target frequency $N\,F_{REF}$. Robust performance can be achieved by employing a frequency-tracking loop (FTL) to continuously tune F_{FR} to be very close to $N\,F_{REF}$. Hence an excellent jitter performance ($<200fs_{rms}$) is achieved in a power and area efficient manner, independent of process, voltage, and temperature (PVT) variations [99, 118].

Unfortunately, ILCMs have been fundamentally limited to only integer-N operation and cannot be used for fractional-N frequency synthesis. A coarse fractional-N ILCM operation is realized by rotating the injection across ring oscillator delay stages [85], but the jitter

performance is limited ($>4\text{ps}_{\text{rms}}$) due to the mismatch between the ring delay stages. In this work, we propose a solution to this major challenge in order to leverage the merits of injection locking to achieve robust low jitter fractional-N ILCM operation at a low power consumption. We employ digital-to-time converter (DTC)-based quantization noise cancellation (QNC) techniques in order to align injected pulses to the oscillator's zero crossings. A 10-bit DTC with a very fine time resolution ($\sim$300fs) is implemented using a multi-stage digitally controlled delay line (DCDL). By proper control of DCDL, injection pulse always occurs ideally at the zero crossing of oscillator output, which enables it to pull the oscillator toward phase lock, thus realizing a fractional-N ILCM.

A prototype 20-bit fractional-N ILCM that consumes 3.25mW power is fabricated in 65nm CMOS process [119]. The prototype achieves the best-reported FoM$_\text{J}$ in both integer-(-255dB) and fractional-N (-252dB) modes. The proposed fractional-N clock multiplier also features the first-reported rapid on/off capability, where the absolute jitter is bounded below 4ps after less than 4ns, illustrating almost instantaneous settling. Leveraging this rapid on/off capability, tremendous energy can be saved by turning on the clock multiplier only when needed. Energy proportional links seek to leverage idle times during the link operation to save power at the system-level [120, 121]. By minimizing the synchronization time to nanoseconds range, reliable and efficient energy-proportional links can be realized.

The rest of the chapter is organized as follows. Section 6.2 explains the basic concept of operation of the proposed fractional-N ILCM. Section 6.3 focuses on the fast settling aspects of the proposed ILCMs and demonstrates its rapid on/off capability. The circuit implementation of critical building blocks is presented in section 6.4. The measured results from the test chip are shown in section 6.5. Finally, the key contributions of this work are summarized in section 6.6.

6.2 Fractional-N Operation of ILCM

6.2.1 Basic Operation

Injecting a narrow pulse into an oscillator perturbs its phase. The oscillator phase, defined by its zero crossing, will be pulled towards the injection pulse. The oscillator output phase perturbations (Φ_O) due to pulse injection persist indefinitely. This phase shift Φ_O depends on the position of the pulse with respect to the oscillator phase, which is defined as the input phase error (Φ_E). In case of an early pulse ($\Phi_E > 0$), the oscillator phase is advanced by a positive phase shift, while a late pulse ($\Phi_E < 0$) delays the oscillator phase by a negative phase shift. The relationship between the input phase error Φ_E and output phase shift Φ_O is defined by the pulse injection phase domain response (PDR) [118]. The PDR acts as an implicit phase detector for injection locked clock multipliers (ILCMs). The PDR is inherently a non-linear transfer function, which depends on the oscillator and injection pulse waveforms, similar to a sub-sampling phase detector. The detailed analysis of PDR can be found in [118]. Ideally, when there is no frequency error, both input phase error Φ_E and output phase shift Φ_O reaches zero.

Sub-harmonic ILCM can be modeled using a first order model as shown in Fig. 6.1. As pulse injection process occurs at reference rate, the model is a discrete time model. Unlike classical PLLs, injection locked clock multiplication is a divider-less sub-sampling operation. Therefore, the reference phase Φ_{REF} is scaled by the multiplication factor N, then the oscillator phase is subtracted to attain the input phase error Φ_E. The output phase shift Φ_O due to PDR is added to the oscillator phase to attain the new oscillator phase Φ_{OUT}. The timing diagram in Fig. 6.1 illustrates the integer-N injection locked clock multiplication process for N = 4. Assuming there is no frequency error, Φ_E equals to zero in steady state and the oscillator phase tracks the reference and its phase noise is greatly suppressed.

However, the operation of ILCM fails when it is used for fractional-N clock synthesis. In the example shown in Fig. 6.2, N equals to 4 and the fractional part α equals to 1/3. Assuming there is no frequency error, the oscillator accumulates an additional phase of $T_{OSC}/3$ every reference cycle, and the injection pulse is not anymore aligned with oscillator

Figure 6.2: Classical ILCM for fractional-N multiplication ($N = 4$ and $\alpha = 1/3$): schematic, discrete-time model, and timing diagram.

zero crossings. This additional phase appears as an input phase error Φ_E as shown in the timing diagram. Φ_E rolls over every 3 reference cycles from 0 to 2π, where it goes beyond the valid operating region of the PDR. As a result, the oscillator cannot be injection locked and it operates in an unlocked state with poor frequency stability and phase noise performance.

Noting that the oscillator accumulates an additional phase of T_{OSC}/α every reference cycle, Φ_E can be made zero by adding the same amount of phase shift to the reference clock as well. To this end, a digitally controlled delay line (DCDL) is introduced in the injection path as shown in Fig. 6.3. Ideally, the DCDL ensures the pulse injection always occurs at the oscillator zero crossing. As a result, the input phase error Φ_E reaches zero and the oscillator can be pulled by the injection pulse towards phase lock, thus realizing a fractional-N ILCM where the output frequency $F_{OUT} = (N + \alpha)\, F_{REF}$. This is illustrated by an example for $N = 4$ and $\alpha = 1/3$. We can see, in the model shown in Fig. 6.4, that
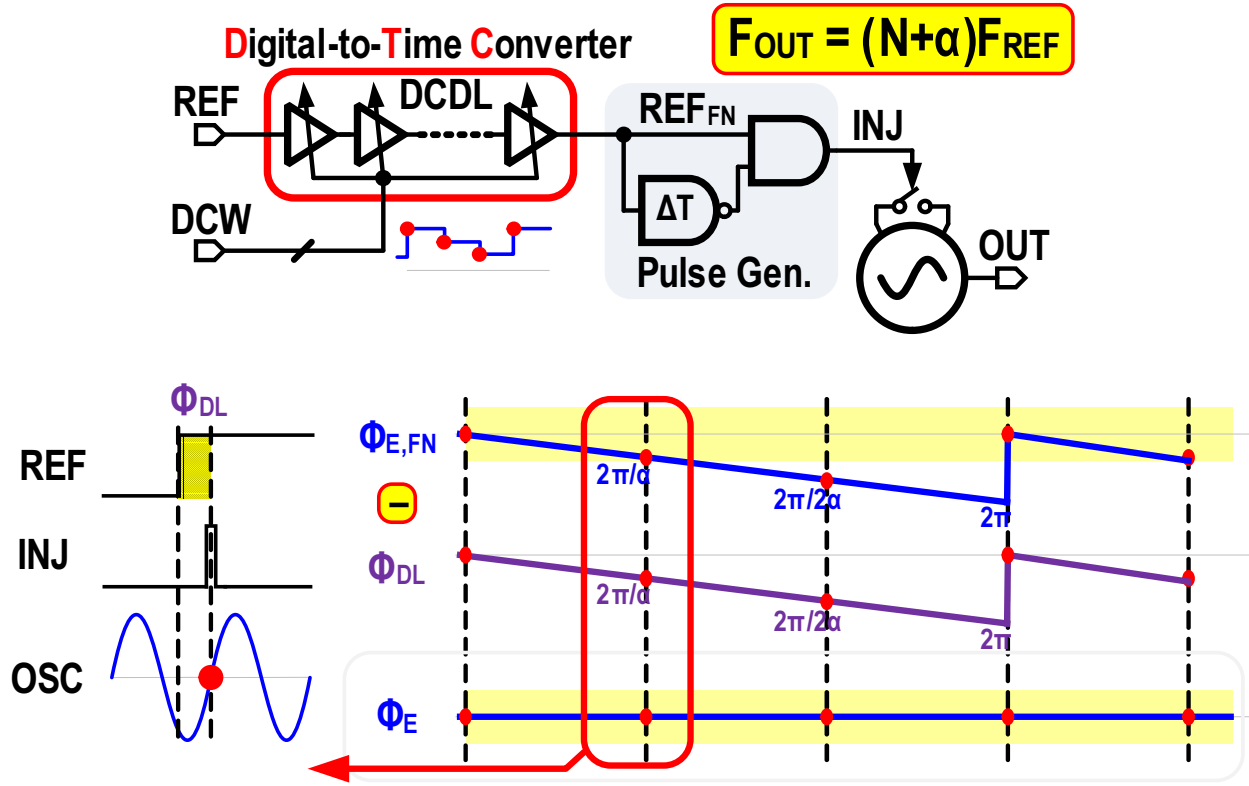
Figure 6.3: Fractional-N ILCM operation concept using delay modulation of the injection pulse.

the added phase shift by the DCDL ideally cancels the accumulated phase shift T_{OSC}/α due to the fractional operation. The DCDL delay control word (DCW) is chosen such that the added delay is equal to T_{OSC}, $2T_{OSC}/3$, $T_{OSC}/3$ in 3 consecutive reference clock cycles. Note that adding a delay of T_{OSC} in the fourth reference cycle results in having 5 oscillator cycles in between third and fourth injection pulses. This behavior is analogous to cycle swallowing present in classical multi-modulus divider-based fractional-N synthesis. The periodic nature of the PDR obviates the need for infinite phase shifting capability of the DCDL. Under this condition, injection pulse occurs ideally at the oscillator zero crossing, and phase locking condition is realized. As shown in the timing diagram in Fig. 6.4, within 3 reference cycles, there are 13 oscillator cycles, thus F_{OUT} equals to $(4+1/3)\,F_{REF}$. Another example is shown in Fig. 6.5, where the fractional part $\alpha = 2/3$. The DCW is chosen such that the added delay is equal to T_{OSC}, $T_{OSC}/3$, $2T_{OSC}/3$ in 3 consecutive reference clock cycles. Two oscillator cycles are swallowed between the second and third injection pulses and between the third
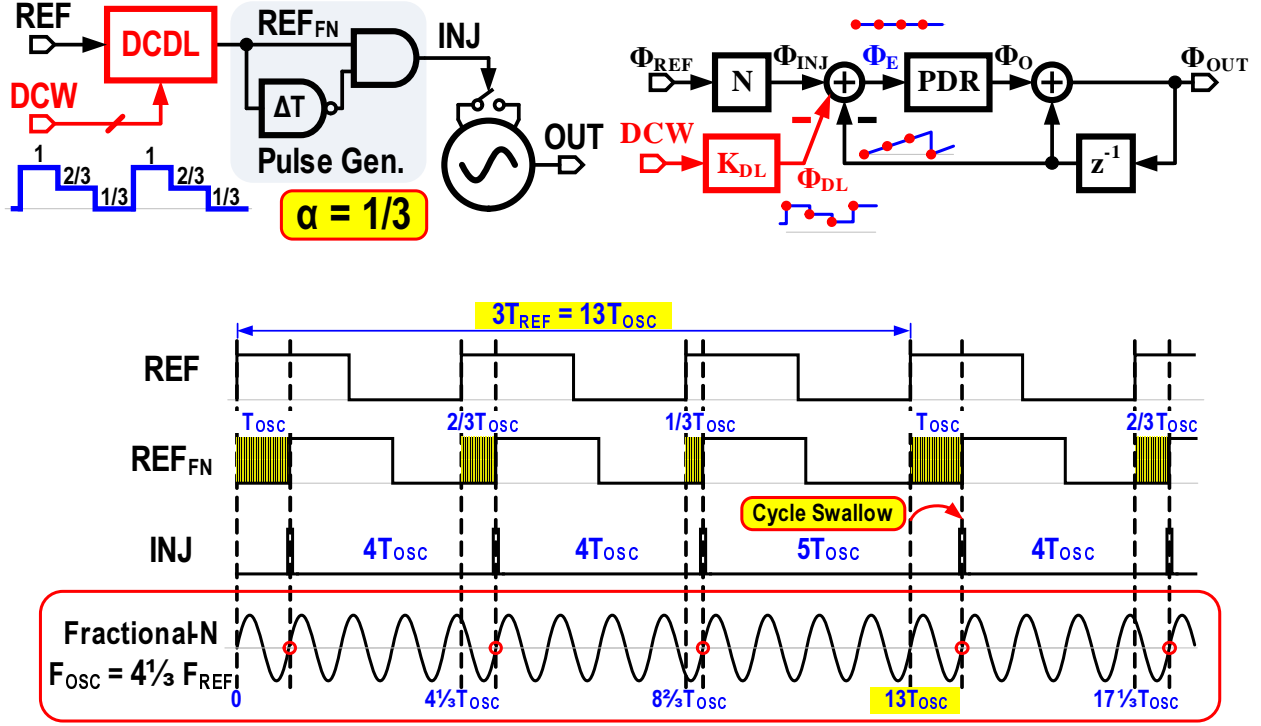
Figure 6.4: Proposed ILCM for fractional-N multiplication ($N = 4$ and $\alpha = 1/3$): schematic, discrete-time model, and timing diagram.

and fourth injection pulses. As a result, there are 14 oscillator cycles with every 3 reference cycles, thus F_{OUT} equals to $(4 + 2/3)\, F_{REF}$.

Generally, within M reference cycles, there are S cycles swallowed as illustrated in Fig. 6.6. This means in steady state:

$$M\, T_{REF} = M\, (N + \alpha)\, T_{OSC} = (M - S) \times N\, T_{OSC} + S \times (N + 1)\, T_{OSC} \qquad (6.1)$$

Therefore, the fractional part $\alpha = S/M$. This clearly illustrates that the output frequency is defined deterministically by the cycle swallowing process, which is similar to the standard multi-modulus divider-based fractional-N synthesis. Based on this concept, a higher order delta sigma ($\Delta\Sigma$) modulator can be used to generate the DCW sequence of the DCDL as depicted in Fig. 6.7. Delay modulation using the DCDL resembles a time-domain QNC technique to ensure the input phase error Φ_E does not go beyond its valid operating region in the PDR. Using a second order $\Delta\Sigma$ modulator, the quantization noise is shaped and
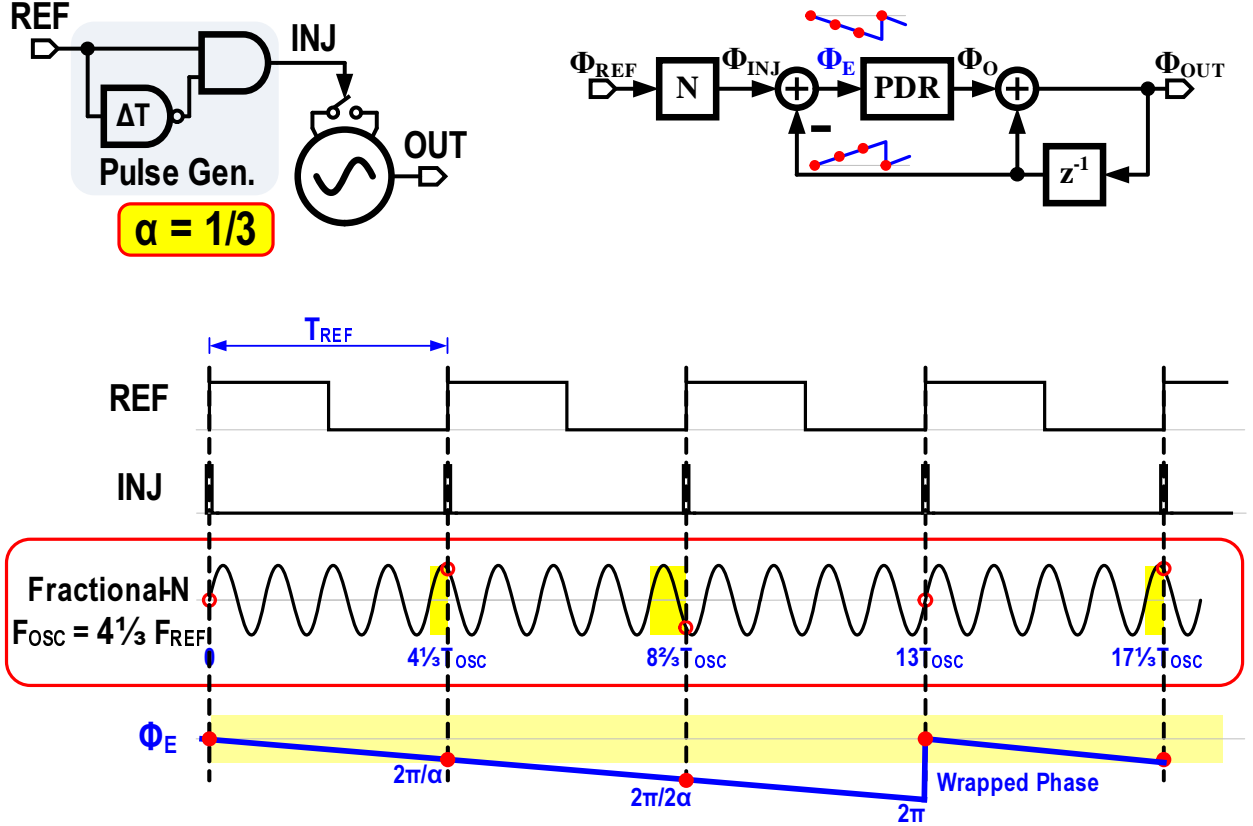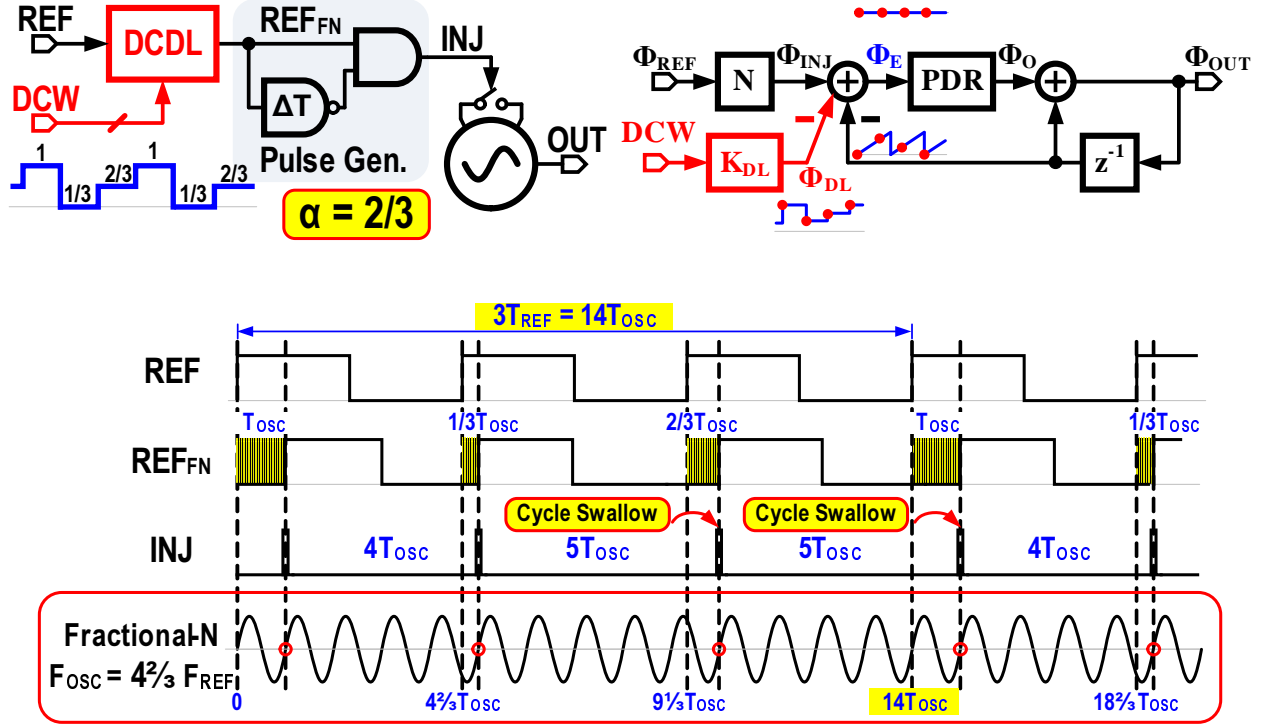
Figure 6.5: Proposed ILCM for fractional-N multiplication ($N = 4$ and $\alpha = 2/3$): schematic, discrete-time model, and timing diagram.
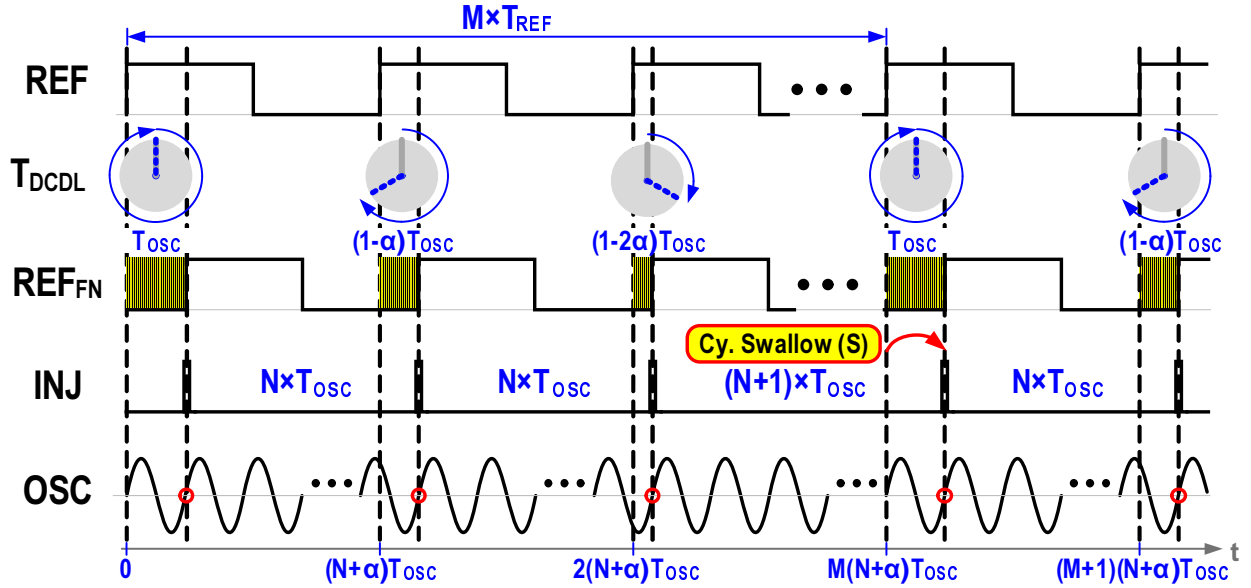
Figure 6.6: Timing diagram of the proposed FN-ILCM.

spread more in time, so the DCDL must span a range of $2T_{OSC}$ to cancel it. However, this cancellation process is susceptible to errors in the DCDL characteristics and to be addressed

by a background calibration scheme.
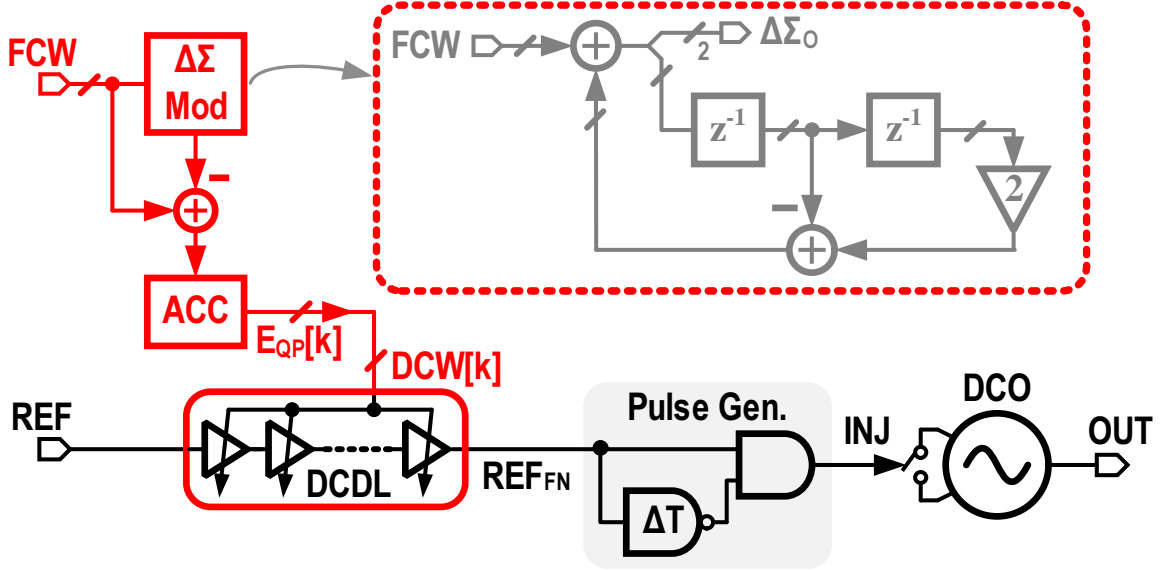
Figure 6.7: Block diagram of the fractional-N ILCM using a second order $\Delta\Sigma$ modulator.

6.2.2 DCDL Background Calibration

A DCDL gain error leads to imperfect quantization noise cancellation (QNC). As a result, the $\Delta\Sigma$ quantization noise leaks to output and the phase noise performance is degraded considerably. Time-domain behavioral simulation is used to evaluate this degradation using F_{REF}=125MHz, $N = 64$, $\alpha = 1/256$. The simulated output phase noise, shown in Fig. 6.8, exhibits a significant performance degradation with larger DCDL gain error. In order to mitigate this phase noise degradation, the DCDL gain (K_{DCDL}) has to be calibrated for a complete QNC. K_{DCDL} is scaled by multiplying digitally the DCDL digital phase control E_{QP} by K_{CAL} to match the pT_{OSC}, where p is the order of the $\Delta\Sigma$ modulator as shown in Fig 6.9. The DCDL gain calibration factor K_{CAL} is estimated in a background manner using a least-mean square (LMS) correlation algorithm, similar to LMS schemes in digital PLLs [9,53]. The LMS correlates the phase control E_{QP} with an error signal that captures the residual phase error due the DCDL gain error.

As the phase detection process is implicit in the PDR of the injection locked oscillator, a dedicated phase detector is required. A sub-sampling bang-bang phase detector (BBPD)
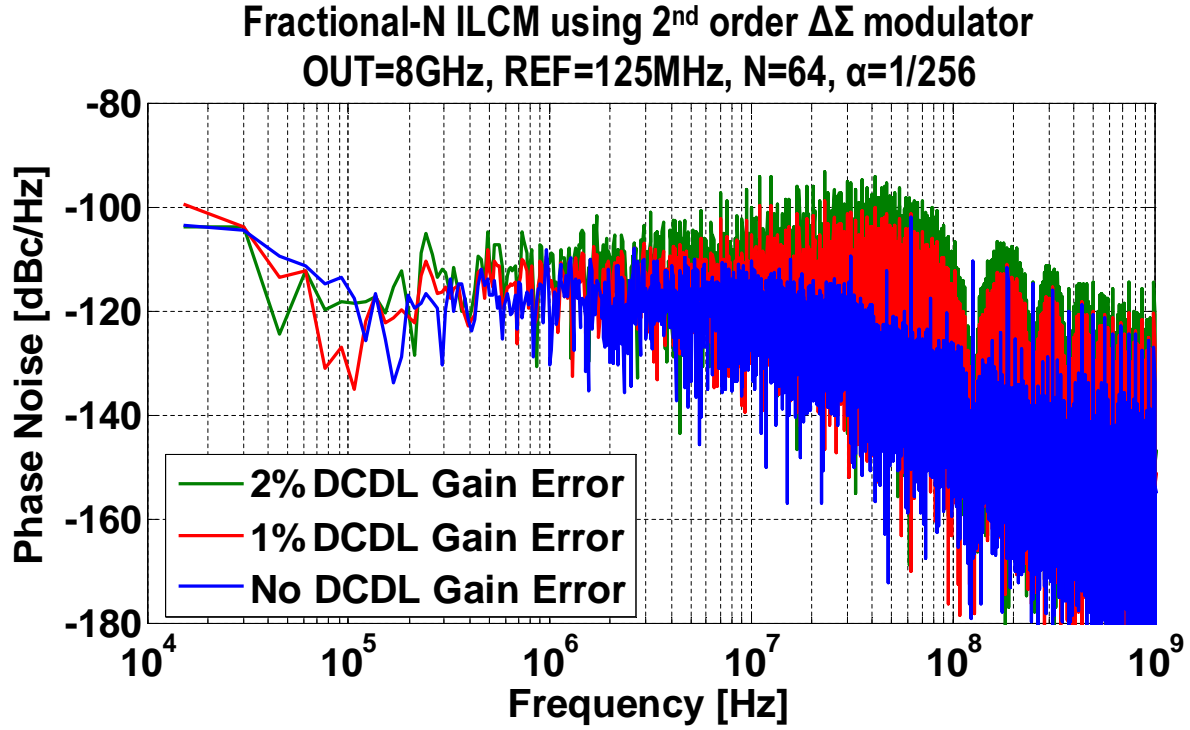
Figure 6.8: Simulated output phase-noise spectrum, 8.0005 GHz output using 125 MHz reference (N = 64 and $\alpha = 1/256$), with 0, 1%, and 2% DCDL gain error.
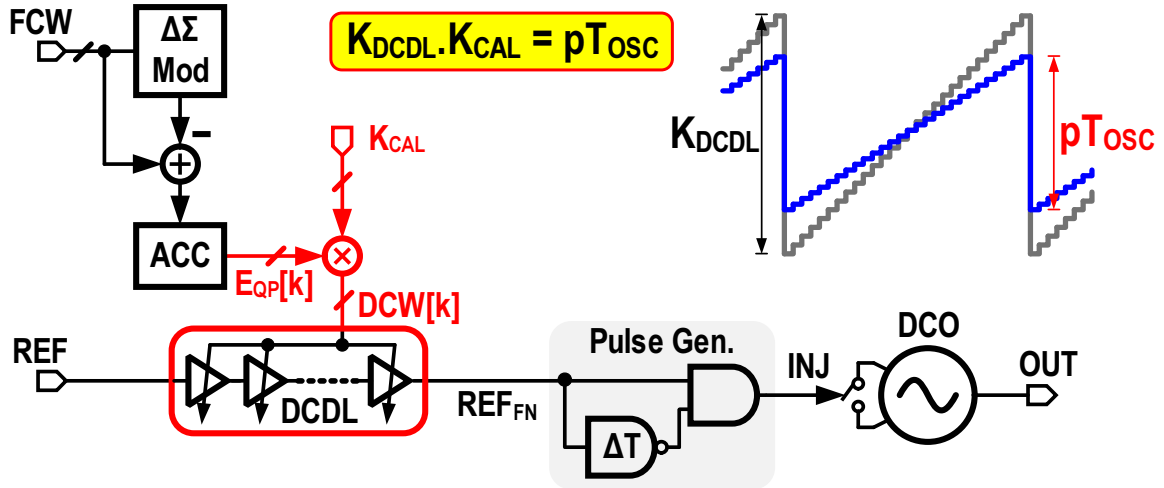
Figure 6.9: Fractional-N ILCM with a calibrated DCDL gain.

generates the error signal Err[k] for a sign-based LMS algorithm as depicted in Fig. 6.10. Because of the delay in the pulse generator and DCO buffer, there is no pre-defined phase relationship between the DCO output and the modulated REF. This time offset may cause the BBPD output to be stuck at continuous $+1$ or continuous -1. To mitigate this, a DLL

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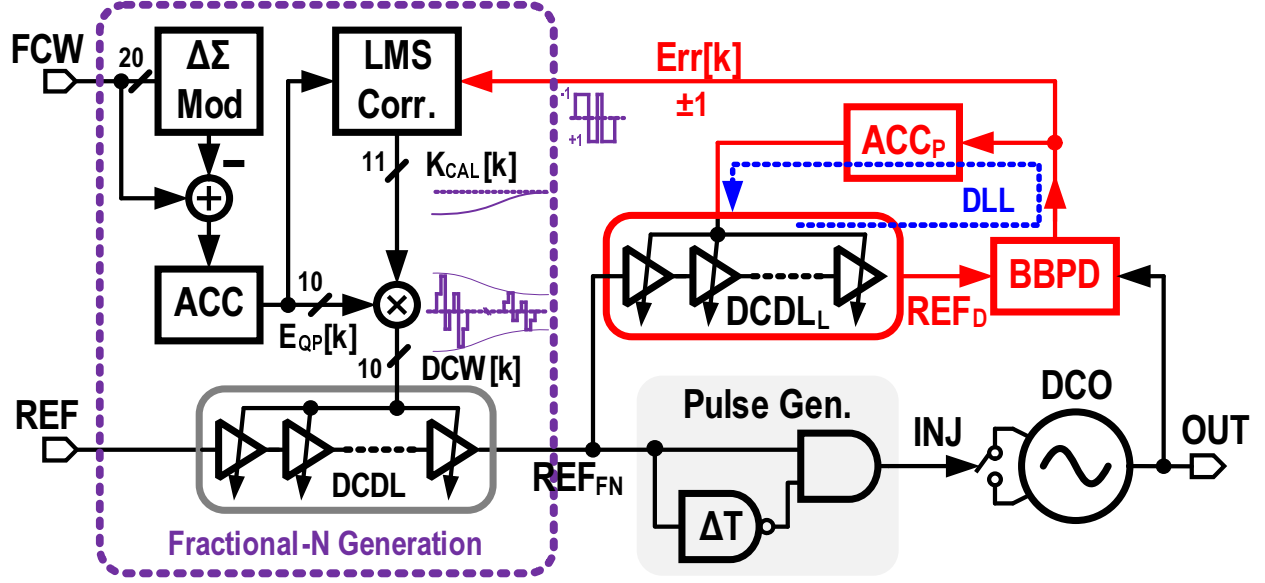
Figure 6.10: Background LMS calibration scheme for scaling DTC gain in fractional-N ILCM.

consisting of the BBPD and accumulator ACC_P tunes the delay of another $DCDL_L$ such that BBPD inputs are aligned on average. As a result, the error signal captures the residual phase error due the DCDL gain error. Consequently, the LMS calibration converges properly.

6.2.3   Frequency Tracking Loop

Besides DCDL gain error, the superior performance of ILCMs can be degraded by the frequency drift of the oscillator. In practice any frequency error F_{ERR} between the oscillator free-running frequency F_{FR} and the target output frequency $F_{OUT} = (N + \alpha)F_{REF}$ will degrade the random and deterministic jitter performance of the clock multiplier. If F_{ERR} is larger than the lock-in range ΔF_L, the oscillator cannot be locked and operation fails. In case F_{ERR} is smaller than ΔF_L, the injection pulses compensate for the accumulated phase error for (N-1) cycles due to F_{ERR} by having a non-zero output phase shift in steady state $\Phi_{O,ss} = -2\pi N\alpha_E$, where $\alpha_E = F_{ERR}/F_{OUT}$ is the relative frequency error. As $\Phi_{O,ss}$ deviates from zero, the effective injection strength (β), the PDR slope in steady state, is reduced and consequently filtering bandwidth is reduced. As a result, the phase noise performance degrades considerably as illustrated in Fig. 6.11. Furthermore, this peri-

odic correction appears as a deterministic jitter, which translates to a large reference spur ($\text{Spur}_{\text{dBc}} \approx 20 \log(\alpha_E N)$) [99].
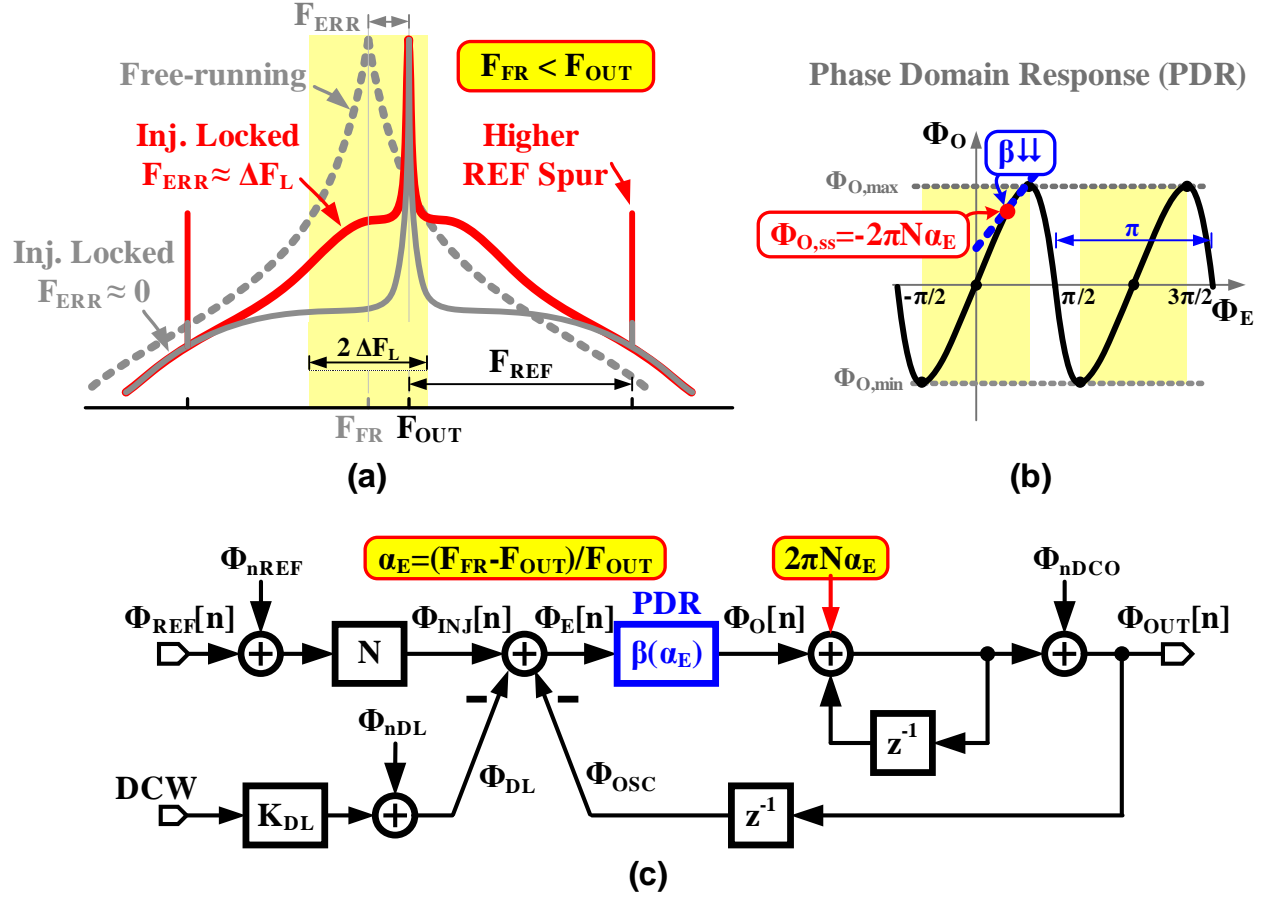
Figure 6.11: The impact of frequency error: (a) output spectrum of ILCM, (b) phase domain response, and (c) phase-domain noise model.

Using a pulse-gating technique, an all-digital continuous frequency tracking loop (FTL) for integer-N ILCMs is introduced in [105]. By disabling or gating some injection pulses, the accumulated phase error in N cycles due to F_{ERR} can be measured using the sub-sampling BBPD. The measured error is integrated using a digital accumulator whose output updates the frequency of the injection-locked DCO incrementally at every pulse gating event. Injection gating resolves the race condition present in injection locked-PLLs, as it decouples the FTL from the injection path. As a result, the phase-locking condition is now only determined by the injection path. This ensures robust operation across supply and temperature variations with excellent jitter and spurious performance. A similar pulse-gating-based FTL

is used in the work for fractional-N synthesis, except for the addition of a second order $\Delta\Sigma$ modulator in the integral path as demonstrated in Fig. 6.12. As the integral path accumulator ACC_I (and hence the DCO) is only updated at every gating pulse, a fractional spur is generated at the gating frequency. The added $\Delta\Sigma$ modulator up-samples ACC_I input from gating frequency to F_{REF} and shapes DCO quantization noise, and hence considerably suppresses this spur.
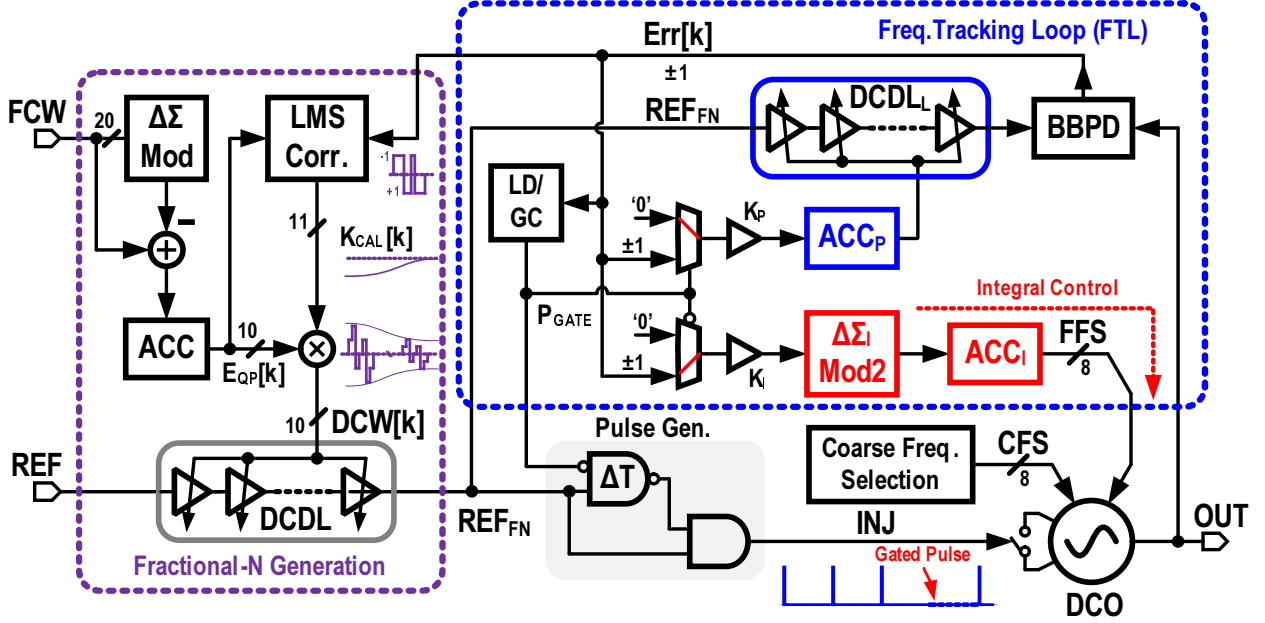
Figure 6.12: Schematic of the proposed fractional-N ILCM with FTL.

6.3 Rapid On/Off ILCM

In energy-constrained applications, the clock generator can be turned off to save power when idle and powered back up only when needed. This power cycling technique is commonly used to realize burst-mode operation in both wireline and wireless communication systems, and it is usually constrained by the settling time of classical PLLs. Therefore rapid on/off clock generators with a minimum power-on time and minimum off-state power are highly desirable. While it is possible to reduce PLL settling time by increasing its bandwidth, the reference frequency sets an upper bound for the bandwidth about $F_{REF}/10$ [122]. Therefore, with 10-100MHz F_{REF} the PLL settling time is in the order of several μs.
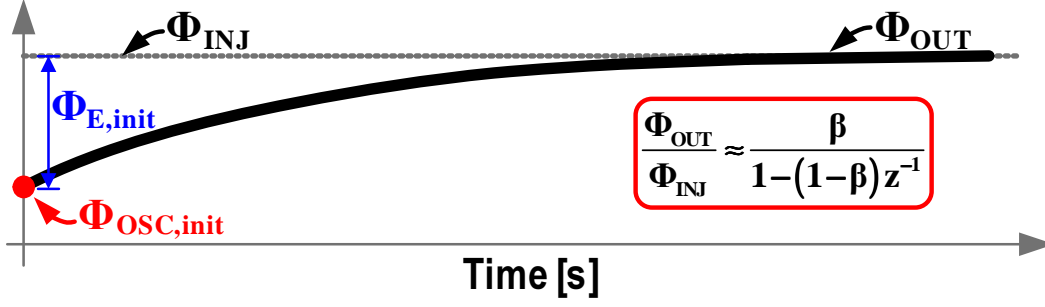
Figure 6.13: Phase settling behavior of ILCM.

Using the proposed digital architecture, the DCO digital control word is stored during the off state and restored at power-on for instantaneous frequency locking. Any residual frequency error caused by supply or temperature variations during the off state is corrected as long it is within the ILCM lock-in range. To ensure that, the time duration of the sleep state is limited to 1ms. Thus, the power-on time is limited by the phase settling behavior. ILCM inherently has a faster phase transient response compared to PLLs, because of it subsampling phase detection characteristics. The phase settling time strongly depends on the injection strength (β) and the initial phase error ($\Phi_{E,init}$). $\Phi_{E,init}$ depends on the unknown oscillator phase Φ_{OSC} on start-up, thus it can take any value from π to $+\pi$. As result, the power-on time is limited to several reference cycles as illustrated in Fig. 6.13.

To overcome this limitation, our goal is to turn-on the ILCM with almost zero initial phase error $\Phi_{E,init}$. This can be achieved by kick-starting the oscillator by a controlled start pulse. A conventional LC-tank builds up oscillations by amplifying thermal noise voltage, where its output phase is random and its start-up time takes several nanoseconds. Using the start pulse kick as a fixed initial condition for every power-on event [120], the output phase trajectory of an oscillator will be deterministic. By controlling the phase of the synchronized start signal using a DCDL$_S$, we can ensure almost zero initial phase error $\Phi_{E,init}$ as shown in the timing diagram in Fig. 6.14. As a result, a very rapid turn-on time, in the order of 2-4ns, is achieved, that is only limited by the oscillator amplitude settling behavior. DCDL$_S$ is calibrated in background using a DLL$_S$ to track voltage and temperature variations during long power-off period. At the beginning of every power on cycle, DCDL$_S$ is adjusted by only 1LSB.
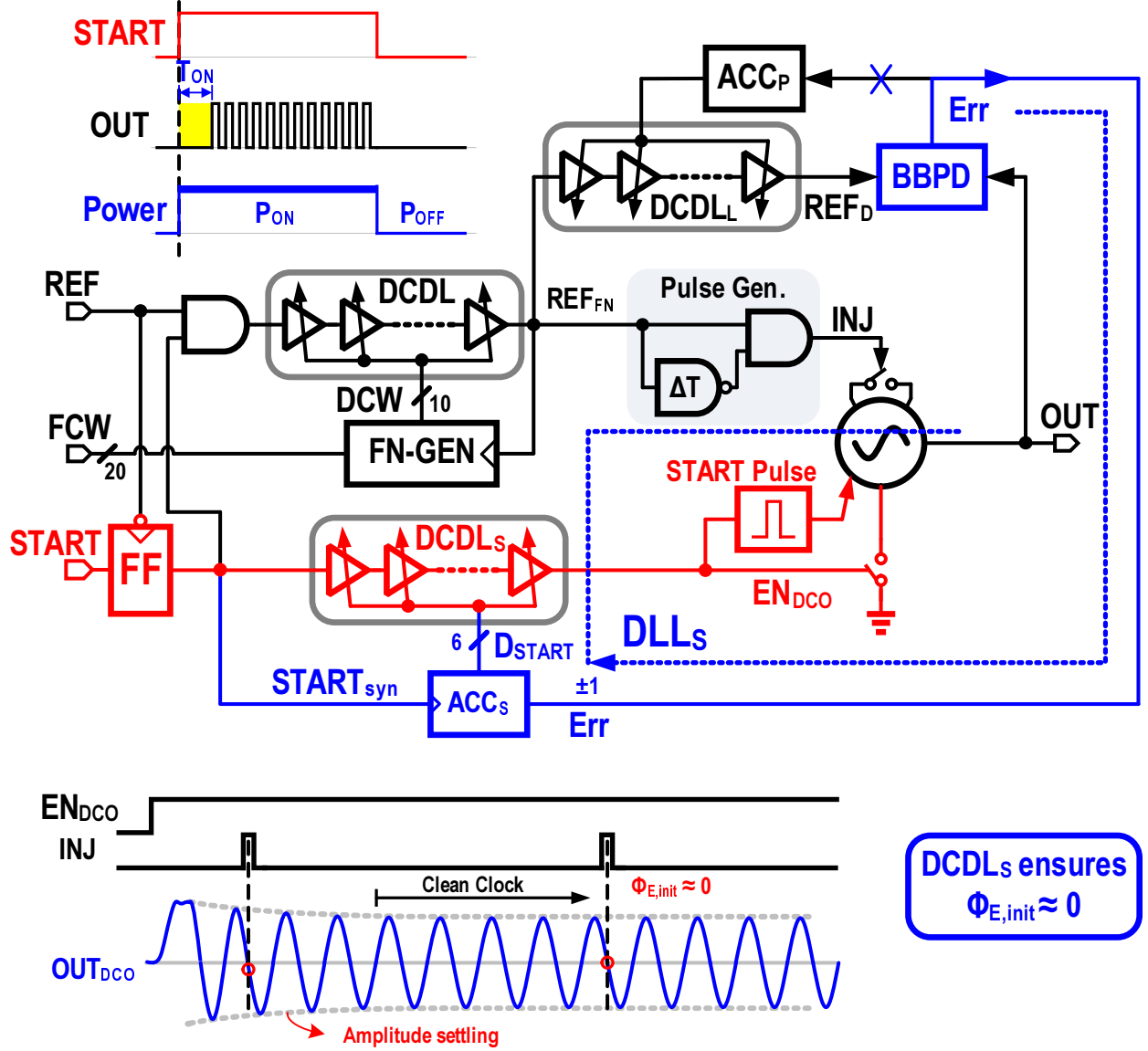
Figure 6.14: Proposed rapid power-on-lock fractional-N ILCM architecture with background calibrated initial phase adjustment.

6.4 Building Blocks

6.4.1 Injection Locked DCO

A 16-bit injection-locked DCO is implemented using NMOS cross-coupled pair and two MOS capacitor banks (8-bit coarse and 8-bit fine) as shown in Fig. 6.15. It is based on the DCO of [118]. The oscillator starts with a deterministic phase using the start pulse as an initial

condition at every power on event. Two additional pull-down NMOS transistors are added at the DCO outputs to provide the initial condition. On power-on, the positive edge of the enable signal generates a narrow pulse to pull down one end of the LC-tank momentarily, to remove the uncertainty in the oscillator phase trajectory, such that the ILCM almost has zero initial phase error for rapid on/off operation in both integer- and fractional-N modes. The pulse generator generates a narrow pulse using the positive edge of the reference clock and injects it into the DCO using a 2bit programmable PMOS switch. The pulse width is controlled from 20ps to 35ps using 4bit digitally controlled delay cell to control the injection strength and filtering bandwidth. A NOR gate implements the injection gating functionality after synchronization with reference clock negative edge.
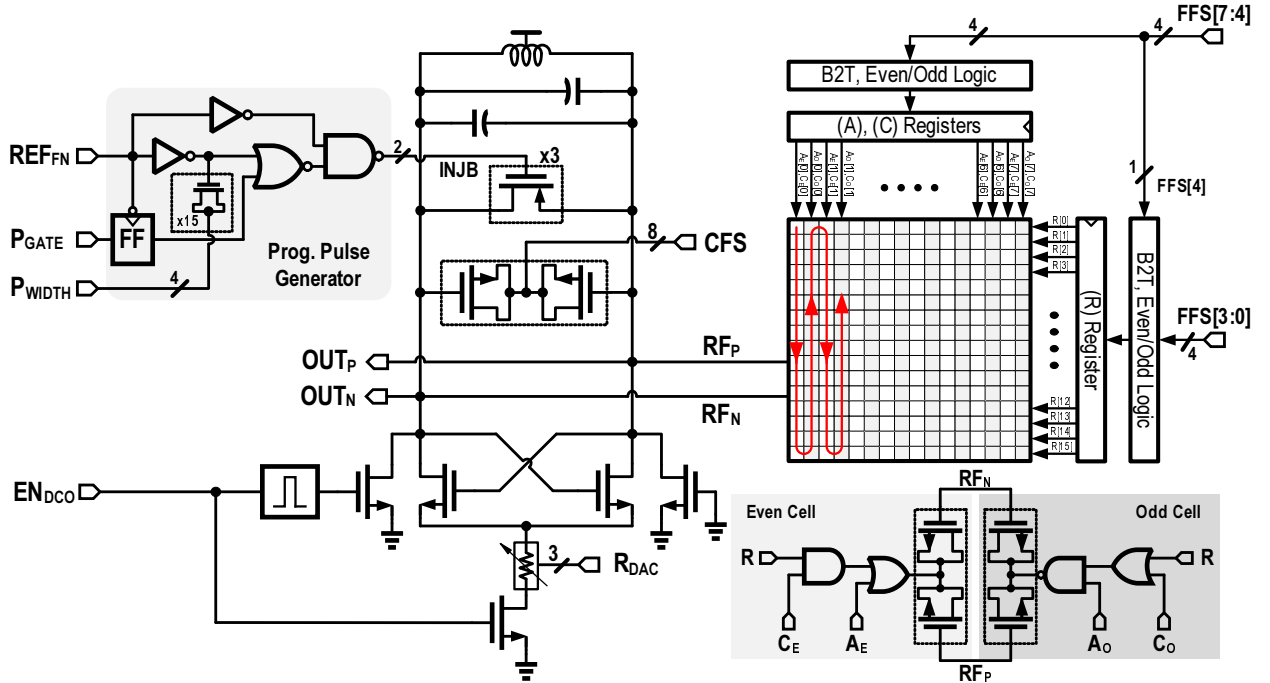
Figure 6.15: LC-based injection locked DCO implementation.

6.4.2 DCDL

A 10-bit digitally controlled delay line (DCDL) is implemented using a cascade of 8 identical digitally controlled delay stages as depicted in Fig. 6.16. It provides about 350ps incremental delay to span at least two oscillator periods over the entire operating range of 6.75 to 8GHz

across PVT variations. The design details are similar to those of the DCDL presented in section 2.4.3. To improve DCDL linearity, we use segmented control to distribute the desired delay equally among all the delays cells. Each delay cell consists of a CMOS buffer loaded with a tunable 128-unit capacitor bank followed by another buffer to restore fast rise and fall times. The unit capacitor cell is implemented using interdigitated MOM capacitor. Post-layout Monte-Carlo simulations show the maximum integral non-linearity of less than 2ps of delay deviation, where the LSB resolution equals to about 0.35ps.
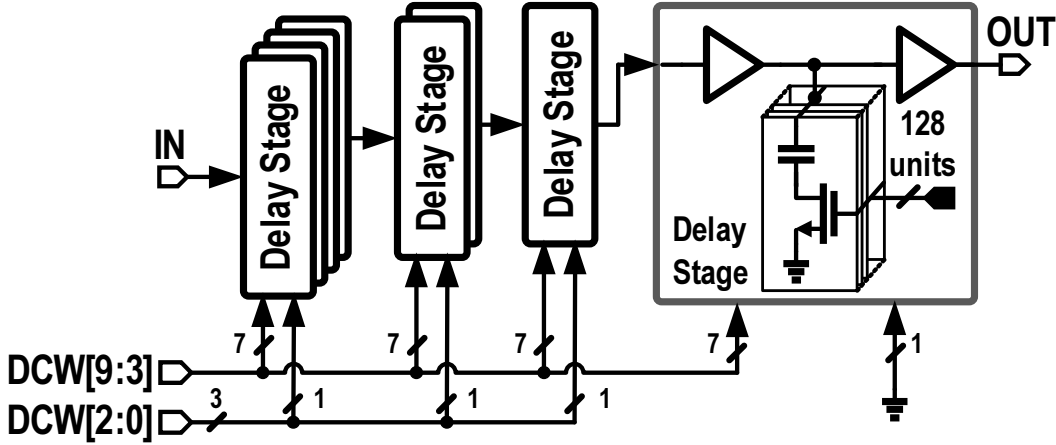
Figure 6.16: Schematic of the DCDL.

6.5 Measurement Results

The proposed fractional-N ILCM shown in Fig. 6.17 was fabricated in 65nm CMOS process and its die photograph is shown in Fig. 6.18. It occupies 0.27mm^2 active area. The prototype is designed to have an output frequency range of 6.75 to 8.25GHz, where a 115MHz reference clock is used in chip testing. Using a 0.9V supply voltage, the chip consumes 2.65mW and 3.25mW in integer- and fractional-N modes respectively. The chip is characterized using Rohde & Schwarz R&SFSUP Signal Source Analyzer (SSA). The measured phase noise of the proposed ILCM in integer-N mode at 7.36GHz is shown in Fig. 6.19. The FTL ensures zero frequency error, and an excellent in-band phase noise of -111.1dBc/Hz at 100kHz offset and -115.7dB/Hz at 1MHz offset is achieved, even when a large multiplication factor of 64
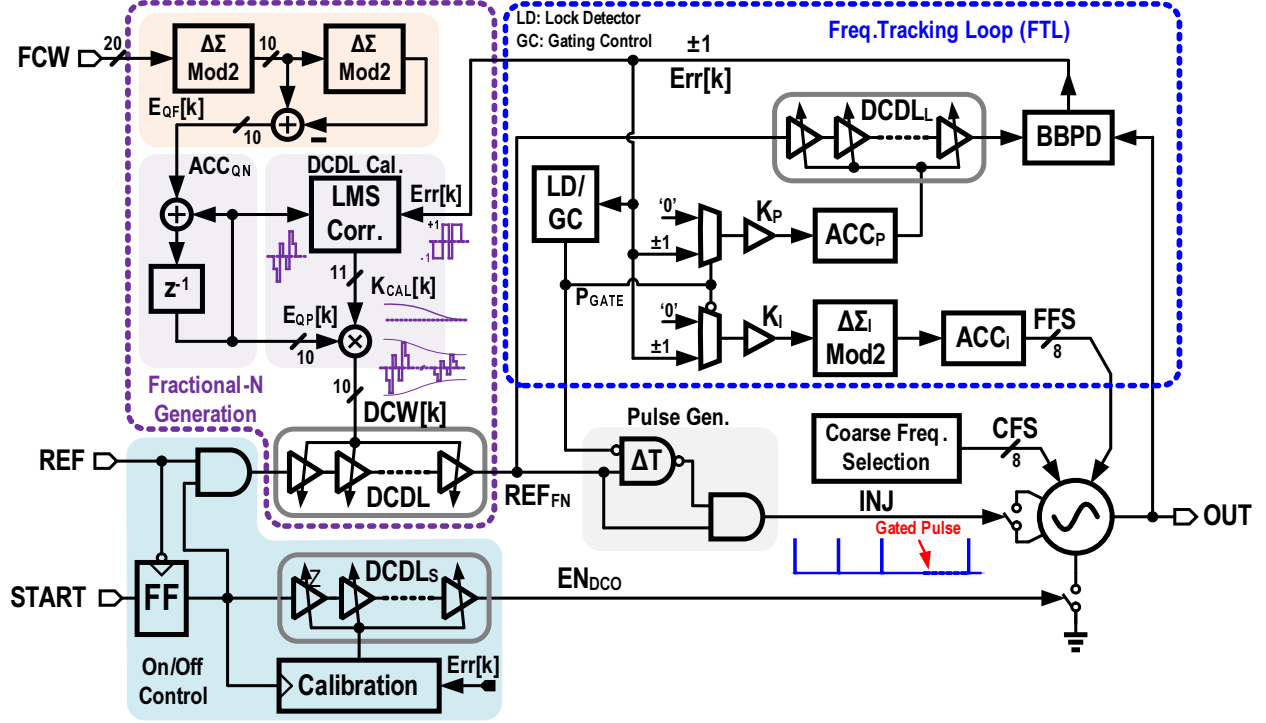
Figure 6.17: Complete architecture of the proposed rapid on/off fractional-N ILCM.

is used. A superior jitter performance of 109fs$_{rms}$ integrated from 10k-30MHz, is achieved, which is limited only by the reference clock jitter which is equal to 190fs$_{rms}$.

The measurement results of the proposed ILCM in fractional-N mode are demonstrated in Fig. 6.20. The in-band phase noise is about -110dBc/Hz at 100kHz offset frequency. The integrated jitter is about 140fs$_{rms}$ and 175fs$_{rms}$ when the fractional spur is out-of-band and in-band, respectively. The degradation in jitter performance in fractional-N mode is attributed to the DCDL non-linearity.

The effectiveness of the proposed frequency tracking loop (FTL) to desensitize the performance across voltage variations is demonstrated by measuring integrated jitter across a supply voltage variation of 0.9V to 1.0V (see Fig. 6.21). The measured DCO free-running frequency varied by 10MHz in this range, which is about 4x the lock-in range. The conventional ILCM loses lock beyond 25mV supply variations, while using the proposed FTL, it remains locked with an integrated jitter less than 110fs$_{rms}$ and 177fs$_{rms}$ in integer- and fractional-N respectively.

The measured output spectrum at 7.36GHz in integer-N mode is shown in Fig. 6.22.
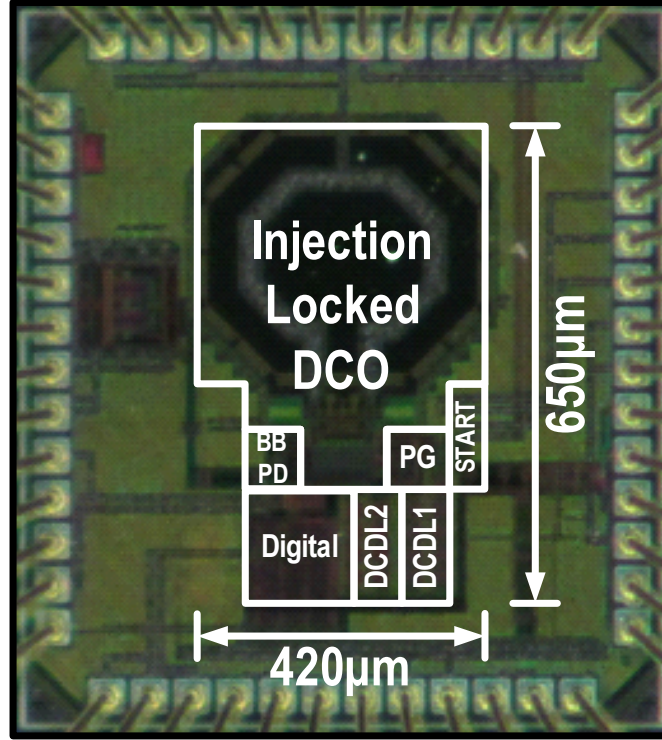
Figure 6.18: Die photograph.

The measured reference spur is around -52dBc even with a large multiplication factor of 64. The measured output spectrum for fractional-N mode with in-band fractional spurs is demonstrated in Fig. 6.23. The worst case fractional spur, for near integer multiplication factor, is less than -42.4dBc at 42.1kHz fractional offset frequency.

The measured power-on transient of the proposed clock multiplier is shown in Fig. 6.24. It demonstrates the absolute jitter settling behavior, captured using an oscilloscope, when the proposed ILCM is powered on and off. The absolute jitter is bounded below 4ps after less than 4ns in both integer- and fractional-N modes, illustrating almost instantaneous settling.

The performance summary and comparison with state-of-the-art integer-N ILCMs are shown in Table 6.1. The proposed architecture achieves superior jitter and spurious performance even with a large multiplication factor of 64. The performance improvement compared to [118] is attributed to the improved phase noise performance of the reference clock and DCO, in addition to shaping DCO quantization noise by $\Delta\Sigma_I$ modulator. This work sets a new record FoM_J of -255dB, with at least 3dB improvement over [91]. This FoM_J is defined by [38] to reflect the jitter power trade-off in clock multipliers as plotted in Fig. 6.25

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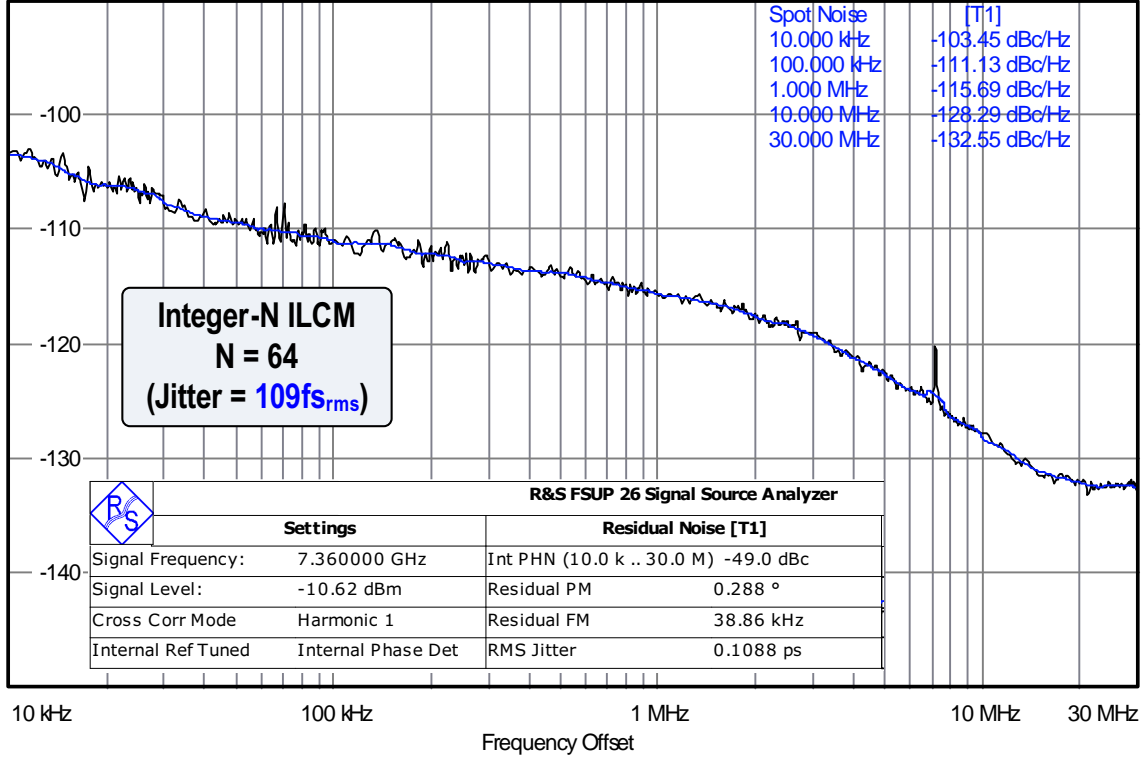
Figure 6.19: Measured phase noise of the ILCM output in integer-N mode at 7.36GHz.

for state-of-the-art integer-N clock multipliers. The performance summary of the proposed fractional-N ILCM and the comparison with state-of-the-art low-jitter fractional-N frequency synthesizers are shown in Table 6.2. The proposed architecture achieves the best power efficiency of 0.44mW/GHz and the best-reported FoM$_J$ of -252dB as demonstrated in Fig. 6.26. This work shows the great potential of leveraging injecting locking in fractional-N frequency synthesis, which brings at least an order of magnitude performance improvement ($\sim$10dB) compared to conventional PLLs. Furthermore, the proposed architecture is the first-reported fractional-N clock multiplier with rapid on/off capability, with less than 4ns wake-up time.

6.6   Conclusion

In conclusion, a new fractional-N injection locked clock multiplier (ILCM) architecture with excellent jitter performance is demonstrated. The delay modulation of injection pulse enables the fractional-N operation. It achieves instantaneous phase locking for rapid On/Off

Table 6.1: Integer-N ILCM Performance Summary

	Helal [99] JSSC'09	Huang [100] JSSC'13	Lee [101] ISSCC'13	Musa [97] JSSC'14	Elkholy [118] JSSC'16	This Work
Architecture	LC-ILCM	LC-ILPLL	LC-ILPLL	Ring-ILCM	LC-ILCM	LC-ILCM
Technology [nm]	130	180	65	65	65	65
Supply [V]	1.2	1.8	1.2	1.0	0.9	0.9
Output Freq. [GHz]	3.2	2.4	2.4	0.5-1.6	6.75-8.25	6.75-8.25
Ref. Freq. [MHz]	50	150	150	125-400	105-129	105-129
Mult. Factor (N)	64	16	16	4	64	64
Ref. Spur [dBc]	-63.9	-40	-48.8	-57	-40	-52
In-band PN [dBc/Hz]*	-127	-126.5	-123.5	NA	-119.2	-123
Ref. Integrated Jitter [fs$_{rms}$]	80 (1k-20MHz)	75 (1k-40MHz)	75 (1k-40MHz)	NA (1k-40MHz)	365 (10k-30MHz)	190 (10k-30MHz)
Output Integrated Jitter [fs$_{rms}$]	130 (100-40MHz)	145 (1k-40MHz)	188 (1k-40MHz)	700 (10k-40MHz)	190 (10k-100MHz)	109 (10k-30MHz)
Power [mW]	28.6	12.6	5.2	0.97	2.25	2.65
Power Eff. [mW/GHz]	**8.94**	**5.25**	**2.17**	**0.8**	**0.30**	**0.36**
FoM$_J$ [dB]**	**-243**	**-246**	**-247**	**-243**	**-251**	**-255**
Continuous Frequency Tracking	Digital (GRO-TDC)	Analog PLL	Analog SSPLL	Digital (VCO Replica)	Digital (Pulse Gating)	Digital (Pulse Gating)
Area [mm^2]	0.4†	0.64	0.25	0.022	0.25	0.27

* Normalized IBPN to 3.2GHz,   † Use external loop filter,   ** FoM$_J$ = $10\log\left[\left(\frac{\sigma_{rms}}{1sec}\right)^2 \frac{P}{1mW}\right]$

Table 6.2: Fractional-N ILCM Performance Summary

	Hsu [5] JSSC'08	Tasca [9] JSSC'11	Elkholy [53] JSSC'15	Raczkowski [123] JSSC'15	Chen [124] ISSCC'15	This Work
Architecture	Digital PLL (TDC)	Digital PLL (DTC)	Digital PLL (DTC+TDC)	Analog SS-PLL (DTC)	Digital SS-PLL (ADC)	Digital ILCM (DTC)
Technology [nm]	130	65	65	28	65	65
Supply [V]	1.5	1.2	1	0.9-1.8	1	0.9
Output Freq. [GHz]	3.6	2.9-4	4.4-5.2	9.2-12.7	2.6-3.9	6.75-8.25
Ref. Freq. [MHz]	50	40	50	40	49.15	115
Power [mW]	39	4.5	3.7	13	11.5	3.25
Ref. Spur [dBc]	-64	-72	-69	-60	-60	-52
In-band Frac. Spur [dBc]	-53	-42	-51.5	-43	-62.3	-42.4
In-band PN [dBc/Hz]*	-107.7	-100.6	-102	-113.9	-109	-120.7
Output Integrated Jitter [ps$_{rms}$] [min|max]]	0.2|0.3 1k-40MHz	0.42|0.56 3k-30MHz	0.42|0.49 10k-20MHz	0.23|0.28 10k-60MHz	0.226|0.24 1k-100MHz	0.14|0.17 10k-30MHz
Power Eff. [mW/GHz]	**10.82**	**1.13**	**0.82**	**1.0**	**2.95**	**0.44**
FoM$_J$ [dB] [min|max]**	**-238|-234.5**	**-241.3|-238.3**	**-241.8|-240.5**	**-241.5|-240**	**-242.3|-241.8**	**-252|-250**
Rapid ON/OFF	**No**	**No**	**No**	**No**	**No**	**Yes (<4ns)**
Area [mm^2]	0.95	0.22	0.22	1.0	0.23	0.27

*Normalized IBPN to 3.2GHz,   ** $\mathrm{FoM_J} = 10\log\left[\left(\frac{\sigma_{rms}}{1\mathrm{sec}}\right)^2 \frac{P}{1\mathrm{mW}}\right]$
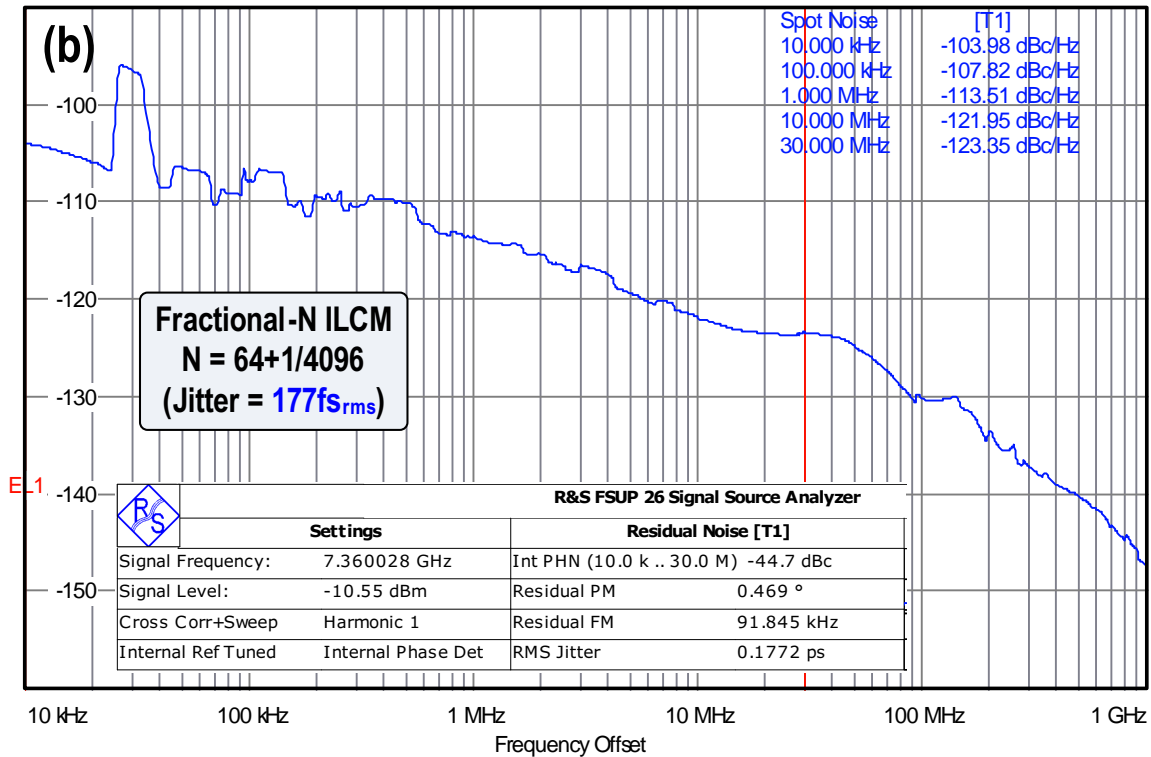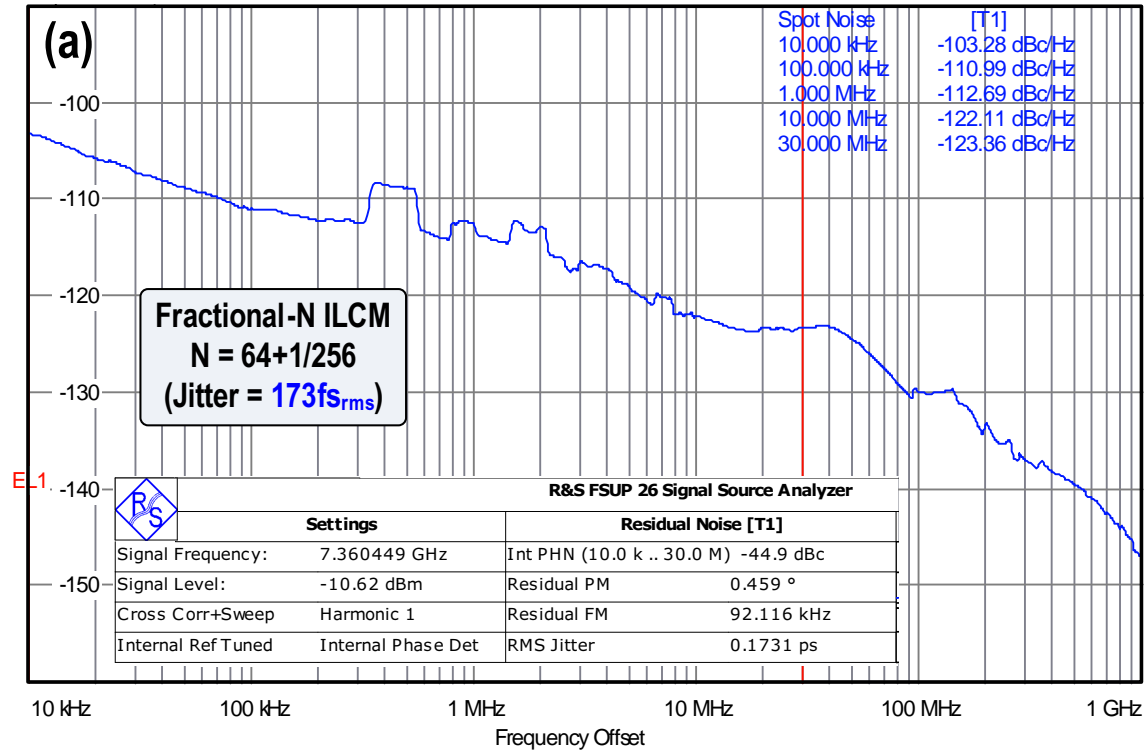
Figure 6.20: Measured phase noise of the ILCM output in fractional-N mode at 7.36GHz when (a) $\alpha = 1/256$ and (b) $\alpha = 1/4096$.
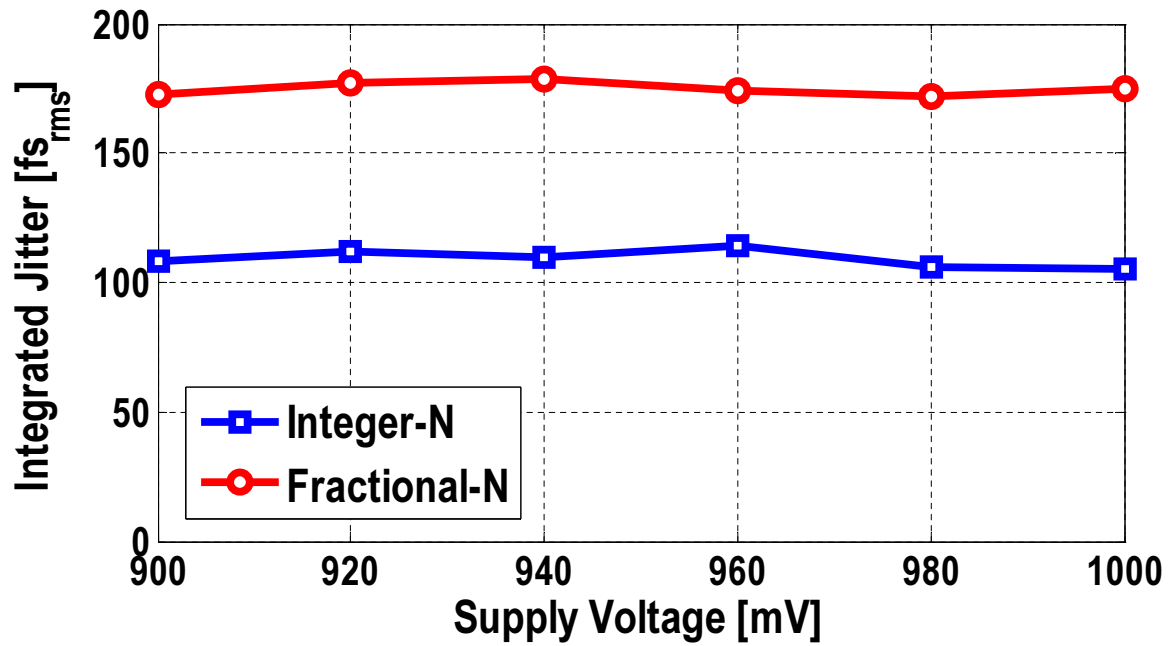
Figure 6.21: Measured integrated jitter versus supply voltage with FTL in integer- and fractional-N modes.
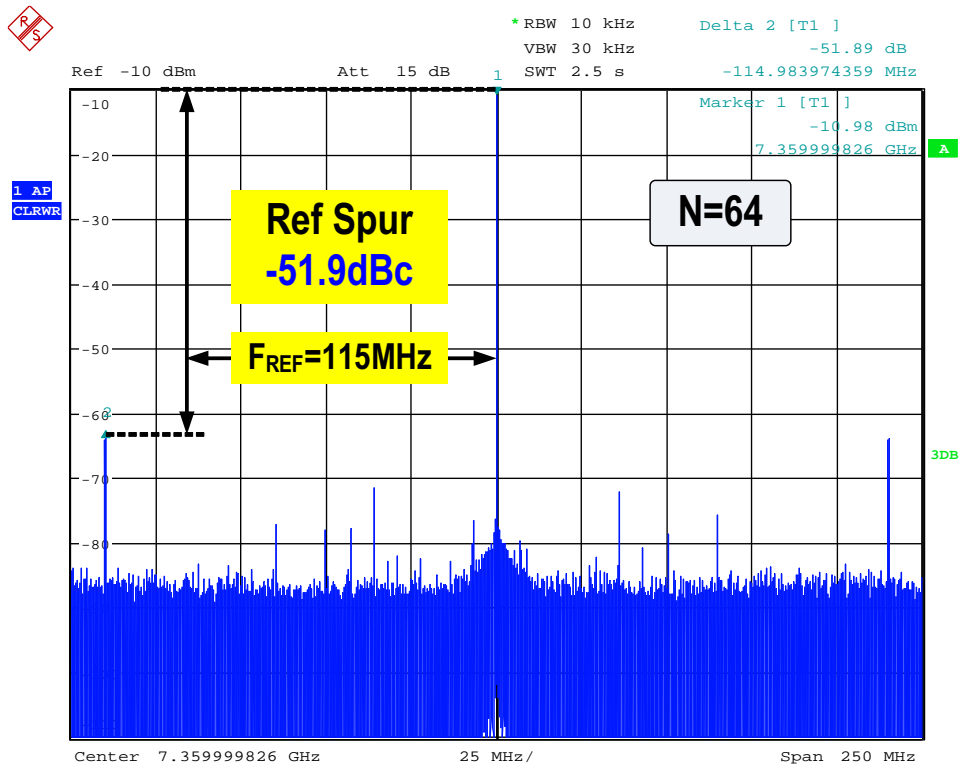
Figure 6.22: Measured output spectrum of integer-N ILCM with FTL (at 7.36GHz, N=64).
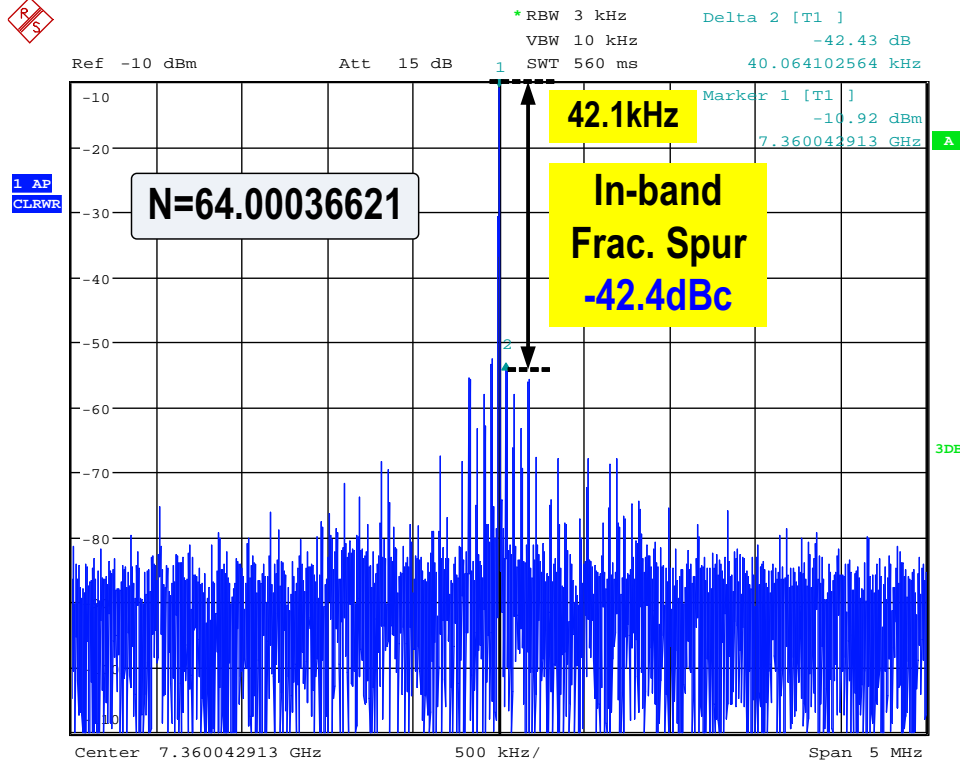
Figure 6.23: Measured output spectrum of fractional-N ILCM with FTL (at 7.36 GHz, N=64, $\alpha = 3/8192$).

operation. It employs an all-digital continuous frequency tracking loop to ensure robust operation across PVT. This enables achieving low power operation and large multiplication factor (N) of 64. The measured jitter is about than $170\text{fs}_{\text{rms}}$ while consuming only 3.25mW at 8GHz output frequency. It achieves the best-reported figure-of-merit (FoM_{J}) of -255dB (integer-N) and -252dB (fractional-N).
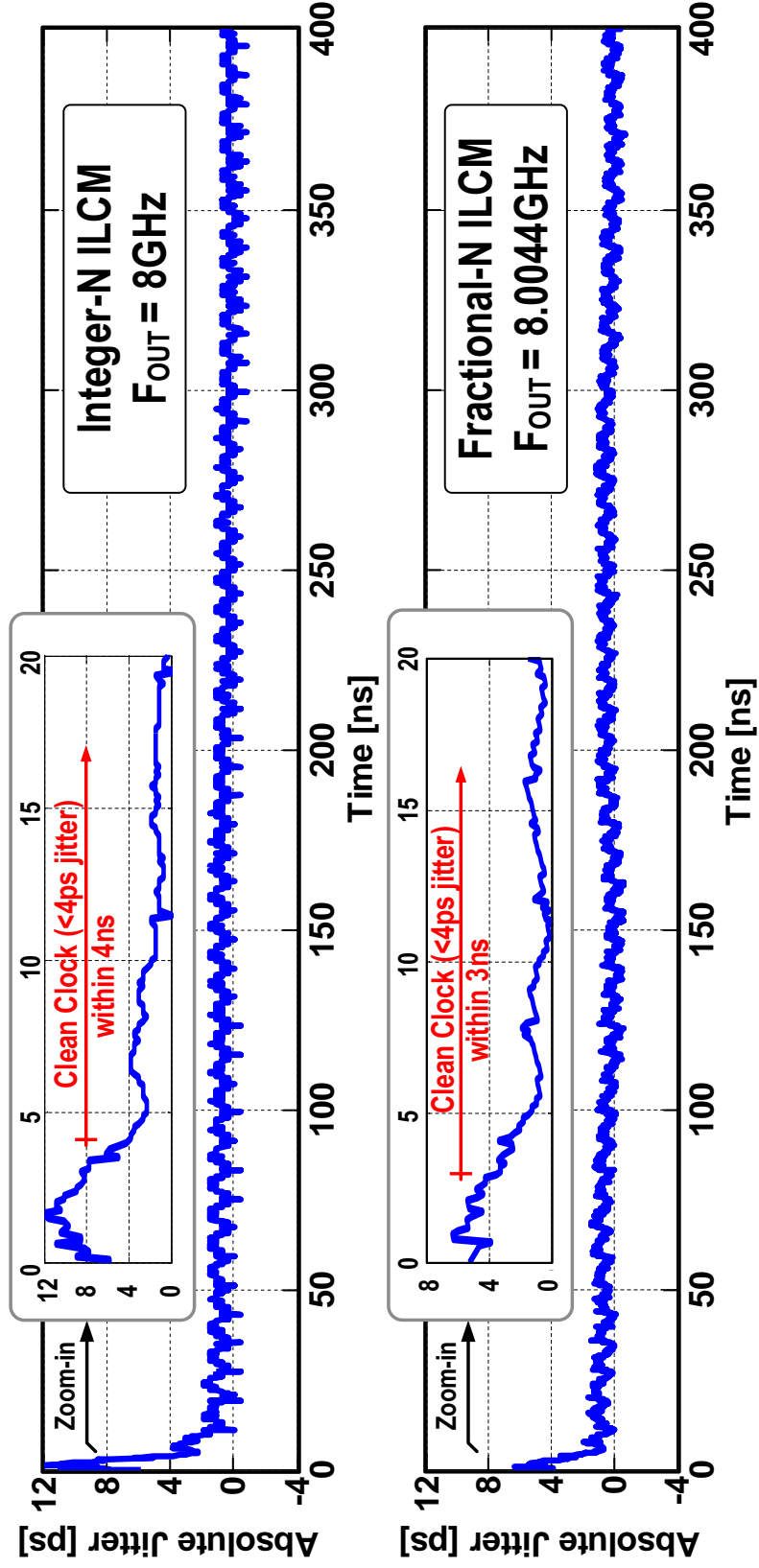
Figure 6.24: Measured ILCM jitter settling behavior during on/off for (a) integer-N and (b) fractional-N modes.
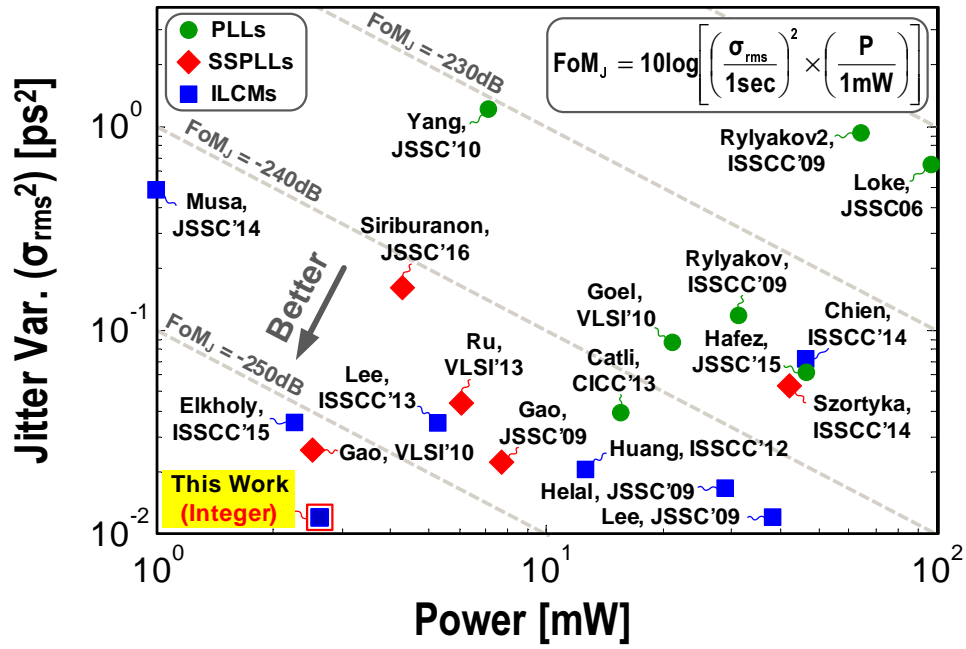
Figure 6.25: Jitter-power FoM$_J$ comparison: integer-N mode.
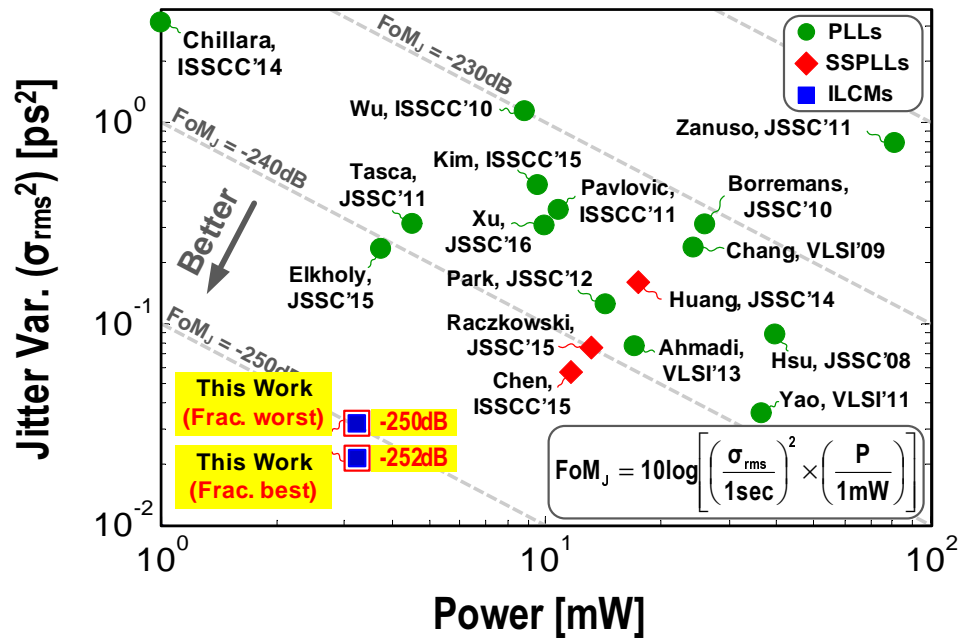
Figure 6.26: Jitter-power FoM$_J$ comparison: fractional-N mode.

CHAPTER 7

CONCLUSION

Low power operation is extremely critical in a wide range of communication applications from data centers to Internet of Things (IoT). Clock and frequency synthesizers play a critical role in both wireless and wireline communication systems. Fractional-N frequency synthesizers are widely used in wireless transceivers to synthesize different channel frequencies from a lower reference frequency. Frequency synthesizers must achieve excellent phase noise and spurious performance in order to meet the overall transceiver system-level requirements. In wireline transceivers, high-performance clocks with low jitter performance are essential to synchronize and recover the transmitted data. Conventionally, clock and frequency synthesizers are implemented using analog charge-pump phase-locked loops (PLLs), where high phase noise performance is typically achieved at the expense of large area and high power consumption. This work focuses on developing energy-efficient techniques by innovating both at the system and circuit levels of fractional-N frequency synthesizers. We also seek to implement highly-scalable, digitally-enhanced realizations of frequency synthesis and clocking modules to leverage the advancement of CMOS technology. My efforts culminate in demonstration of these techniques using experimental results obtained from several custom-designed integrated circuits (ICs) [19, 27, 52, 53, 105, 118, 119, 125].

In the first part of this work, we proposed a low-power LC-based digital fractional-N PLL (FNPLL) for wireline and wireless applications [19, 53]. Conventional digital FNPLLs suffer from conflicting bandwidth requirement to simultaneously suppress oscillator phase noise and quantization errors introduced by the time-to-digital converter (TDC), fractional divider, and DAC. To overcome this trade-off, a quantization noise cancellation (QNC) scheme and a high-resolution TDC were proposed. By performing QNC in time-domain, the wide dynamic range requirement of the TDC is alleviated, and a low power ($<$0.2mW), high

resolution (<1ps), narrow range 4-bit time amplifier (TA)-TDC greatly enhances in-band phase noise. By using TA-TDC in place of a bang-bang (BB) phase detector, the limit cycle behavior that plagues BB-PLLs is greatly suppressed by the TA-TDC, thus permitting wide PLL bandwidth to aggressively suppress the phase noise of a low power oscillator. The proposed architecture is also less susceptible to DTC nonlinearity and has faster settling and tracking behavior compared to a BB-PLL. A prototype was implemented in a 65nm CMOS process using LC-based oscillator. The digital FNPLL achieves better than -106dBc/Hz in-band noise and 3MHz PLL bandwidth at 4.5 GHz output frequency using a 50 MHz reference. The PLL consumes 3.7mW and achieves better than 490fs$_{rms}$ integrated jitter. This translates to a figure-of-merit (FoM$_J$) of -240.5dB, which is the best among the reported FNPLLs.

In the second part of this work, we proposed a low-power ring-based digital FNPLL with multi-phase outputs for wireline applications [52, 125]. Because of the poor phase noise performance and large gain of the ring VCO, a dual-path digital loop filter architecture is proposed to resolve the DAC quantization noise challenge and minimize loop latency for further bandwidth extension up to 6MHz (F$_{REF}$/8). Fabricated in 65nm CMOS process, the proposed FNPLL operates over a wide frequency range of 2.0-5.5GHz using a modified extended range multi-modulus divider with seamless switching. The proposed digital FNPLL achieves -96dBc/Hz in-band phase noise and 1.9ps$_{rms}$ jitter while consuming only 4mW at 5GHz. The FoM$_J$ is -228.5dB, which is at about 20dB better than previously reported ring-based digital FNPLLs.

In the third part of this work, we proposed a multi-output clock generator using open loop fractional dividers for system-on-chip (SoC) platforms [27]. Modern SoCs contain a wide variety of modules with diverse clock requirements. For example, I/O interfaces require low jitter clocks, while core-clocking of a processor may require spread spectrum clocking to reduce electromagnetic interference (EMI) or using dynamic frequency scaling (DFS) for energy efficient operation, which requires clocks with fast frequency switching. A conventional analog PLL-based clock generation unit occupies large area, and has a slow settling and limited SSC modulation capabilities. In view of these drawbacks, a new generic clock generator architecture using open loop fractional dividers was proposed. The prototype fractional

divider was implemented in a 65nm CMOS process, and occupies a compact active area of 0.017mm^2. The measured peak-to-peak jitter is less 27ps over a wide frequency range from 20MHz to 1GHz. The total power consumption is about 3.2mW for 1GHz output frequency. The fractional divider switches the output frequency instantaneously and has unlimited modulation bandwidth that provides excellent SSC performance. The all-digital implementation of the divider occupies the smallest area compared to state-of-the-art designs.

With the ever-increasing requirements for higher data rates serial links, the jitter requirements of clock multipliers pose a real challenge. Conventional PLLs suffer from the coupled noise bandwidth trade-off, thus achieving superior jitter performance ($<200\text{fs}_{\text{rms}}$) mandates stringent noise performance of the oscillator and/or loop components, resulting in high power consumption (tens of mWs). A low-jitter, low-power LC-based injection-locked clock multiplier (ILCM) with a digital frequency-tracking loop (FTL) is presented [105, 118]. The proposed FTL continuously tunes the oscillator's free-running frequency to ensure robust operation across PVT variations. Based on a pulse gating technique, the proposed FTL resolves the race condition existing in injection-locked PLLs by decoupling frequency tuning from the injection path, such that the phase-locking condition is only determined by the injection path. Fabricated in 65 nm CMOS process, a prototype ILCM generates output clock in the range of 6.75-8.25 GHz by multiplying the reference clock by 64. It achieves superior integrated jitter performance of $190\text{fs}_{\text{rms}}$, while consuming 2.25mW power. This translates to an excellent FoM_J of -251dB, which is the best reported high-frequency clock multiplier.

Even though ILCMs achieve superior phase noise compared to conventional PLLs, they have been fundamentally limited to only integer-N operation and cannot be used for fractional-N frequency synthesis. My latest research goal was to overcome this fundamental limitation and extend the benefits of ILCMs to fractional-N. A prototype 20-bit fractional-N ILCM that consumes 3.25mW power is fabricated in a 65nm CMOS process [119]. The prototype achieves the best-reported FoM_J in both integer- (-255dB) and fractional-N (-252dB) modes. The proposed fractional-N clock multiplier also features the first-reported rapid on/off capability, where the absolute jitter is bounded below 4ps after less than 4ns, illustrating almost instantaneous settling. Leveraging this rapid on/off capability, tremendous energy can be

saved by turning on the clock multiplier only when needed. By minimizing the synchronization time to nano-seconds range, reliable and efficient energy-proportional links can be realized. Energy proportional links seek to leverage idle times during the link operation to save power at the system-level [120, 121].

My future work will be focused in the area of advanced wireline systems, particularly the development of energy-proportional links and heterogeneous integration of silicon photonics with electronics for energy efficient short- and medium-range optical links. Energy proportional techniques can maintain excellent energy efficiency across a very wide range of link utilization levels. I believe this technology will help address the important issue of power dissipation in data centers. Fiber-optic technologies are expected to play more critical roles in data center operations in the near future. Optical links can achieve superior performance in terms of power efficiency, data rate, and reach compared to electrical links. We seek to co-design optical devices with electronics to create digitally enhanced photonics and novel system- and circuit-level techniques to provide 10-50 times improvement in cost and power efficiency to meet the future market demands.

REFERENCES

[1] J. Tierno, A. Rylyakov, D. Friedman, A. Chen, A. Ciesla, T. Diemoz, G. English, D. Hui, K. Jenkins, P. Muench, G. Rao, G. Smith, M. Sperling, and K. Stawiasz, "A DPLL-based per core variable frequency clock generator for an eight-core POWER7^{tm} microprocessor," in *IEEE VLSI Circuits Sym. Tech. Papers*, June 2010, pp. 85–86.

[2] R. Best, *Phase Locked Loops 6/e : Design, Simulation, and Applications: Design, Simulation, and Applications*, ser. McGraw-Hill professional engineering. McGraw-Hill, 2007. [Online]. Available: http://books.google.com/books?id=WSB_oAEACAAJ

[3] A. Swaminathan, K. Wang, and I. Galton, "A wide-bandwidth 2.4 GHz ISM band fractional-N PLL with adaptive phase noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2639–2650, Dec 2007.

[4] R. B. Staszewski, J. L. Wallberg, S. Rezeq, C.-M. Hung, O. E. Eliezer, S. K. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2469–2482, Dec. 2005.

[5] C.-M. Hsu, M. Straayer, and M. Perrott, "A low-noise wide-BW 3.6-GHz digital $\Delta\Sigma$ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, Dec. 2008.

[6] E. Temporiti, C. Weltin-Wu, D. Baldi, R. Tonietto, and F. Svelto, "A 3 GHz fractional all-digital PLL with a 1.8 MHz bandwidth implementing spur reduction techniques," *IEEE J. Solid-State Circuits*, vol. 44, pp. 824–834, Mar. 2009.

[7] M. Zanuso, S. Levantino, C. Samori, and A. Lacaita, "A wideband 3.6 GHz digital $\Delta\Sigma$ fractional-N PLL with phase interpolation divider and digital spur cancellation," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 627–638, Mar. 2011.

[8] L. Vercesi, L. Fanori, F. De Bernardinis, A. Liscidini, and R. Castello, "A dither-less all digital PLL for cellular transmitters," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1908–1920, Aug. 2012.

[9] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. Lacaita, "A 2.9-4.0-GHz fractional-N digital PLL with bang-bang phase detector and 560-fs$_{rms}$ integrated

jitter at 4.5-mW power," *IEEE J. Solid-State Circuits*, vol. 46, pp. 2745–2758, Dec. 2011.

[10] E. Temporiti, C. Weltin-Wu, D. Baldi, M. Cusmai, and F. Svelto, "A 3.5 GHz wideband ADPLL with fractional spur suppression through TDC dithering and feedforward compensation," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2723–2736, Dec. 2010.

[11] S. Levantino, G. Marzin, C. Samori, and A. Lacaita, "A wideband fractional-N PLL with suppressed charge-pump noise and automatic loop filter calibration," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2419–2429, Oct. 2013.

[12] S. Pamarti, L. Jansson, and I. Galton, "A wideband 2.4-GHz delta-sigma fractional-N PLL with 1Mb/s in-loop modulation," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 49–62, Jan. 2004.

[13] A. Swaminathan, K. Wang, and I. Galton, "A wide-bandwidth 2.4 GHz ISM band fractional-N PLL with adaptive phase noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, pp. 2639–2650, Dec. 2007.

[14] H. Hedayati, W. Khalil, and B. Bakkaloglu, "A 1 MHz bandwidth, 6 GHz 0.18 μm CMOS type-I $\Delta\Sigma$ fractional-N synthesizer for WiMAX applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3244–3252, Dec. 2009.

[15] M. Ahmadi, D. Pi, B. Catli, U. Singh, B. Zhang, Z. Huang, A. Momtaz, and J. Cao, "A 288fs RMS jitter versatile 8-12.4GHz wide-band fractional-N synthesizer for SONET and SerDes communication standards in 40nm CMOS," in "*IEEE VLSI Circuits Sym. Tech. Papers*", June 2013, pp. C160–C161.

[16] G. Shu, W.-S. Choi, S. Saxena, T. Anand, A. Elshazly, and P. Hanumolu, "A 4-to-10.5Gb/s 2.2mW/Gb/s continuous-rate digital CDR with automatic frequency acquisition in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2014, pp. 150–151.

[17] C.-H. Hsiao, C.-J. Li, F.-K. Wang, T.-S. Horng, and K.-C. Peng, "Analysis and improvement of direct-conversion transmitter pulling effects in constant envelope modulation systems," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 12, pp. 4137–4146, Dec. 2010.

[18] N. Pavlovic and J. Bergervoet, "A 5.3GHz digital-to-time-converter-based fractional-N all-digital PLL," in *ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 54–56.

[19] A. Elkholy, T. Anand, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, "A 3.7mW 3MHz bandwidth 4.5GHz digital fractional-N PLL with -106dBc/Hz in-band noise using time amplifier based TDC," in *IEEE VLSI Circuits Sym. Tech. Papers*, June 2014, pp. 1–2.

[20] M. Gupta and B.-S. Song, "A 1.8-GHz spur-cancelled fractional-N frequency synthesizer with LMS-based DAC gain calibration," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2842–2851, Dec. 2006.

[21] M. Lee, M. Heidari, and A. Abidi, "A low-noise wideband digital phase-locked loop based on a coarse-fine time-to-digital converter with subpicosecond resolution," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2808–2816, Oct. 2009.

[22] K.-S. Kim, W.-S. Yu, and S.-H. Cho, "A 9 bit, 1.12 ps resolution 2.5 b/stage pipelined time-to-digital converter in 65 nm CMOS using time-register," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 1007–1016, Apr. 2014.

[23] A. Elshazly, S. Rao, B. Young, and P. Hanumolu, "A noise-shaping time-to-digital converter using switched-ring oscillators: Analysis, design, and measurement techniques," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1184–1197, May 2014.

[24] R. Nonis, W. Grollitsch, T. Santa, D. Cherniak, and N. Da Dalt, "digPLL-lite: A low-complexity, low-jitter fractional-N digital PLL architecture," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3134–3145, Dec. 2013.

[25] N. Da Dalt, "Linearized analysis of a digital bang-bang PLL and its validity limits applied to jitter transfer and jitter generation," *IEEE Trans. Circuits Syst. I*, vol. 55, pp. 3663–3675, Dec. 2008.

[26] G. Marucci, S. Levantino, P. Maffezzoni, and C. Samori, "Exploiting stochastic resonance to enhance the performance of digital bang-bang PLLs," *IEEE Trans. Circuits Syst. II*, vol. 60, no. 10, pp. 632–636, Oct. 2013.

[27] A. Elkholy, A. Elshazly, S. Saxena, G. Shu, and P. Hanumolu, "A 20-to-1000MHz ±14ps peak-to-peak jitter reconfigurable multi-output all-digital clock generator using open-loop fractional dividers in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 272–273.

[28] S. Haykin, *Adaptive Filter Theory*, 5th ed. Prentice Hall, 2013.

[29] G. Marzin, S. Levantino, C. Samori, and A. Lacaita, "A 20 Mb/s phase modulator based on a 3.6 GHz digital PLL with -36 dB EVM at 5 mW power," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2974–2988, Dec 2012.

[30] M. Perrott, M. Trott, and C. Sodini, "A modeling approach for $\Sigma - \Delta$ fractional-N frequency synthesizers allowing straightforward noise analysis," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1028–1038, Aug 2002.

[31] S.-K. Lee, Y.-H. Seo, H.-J. Park, and J.-Y. Sim, "A 1 GHz ADPLL with a 1.25 ps minimum-resolution sub-exponent TDC in 0.18 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2874–2881, Dec. 2010.

[32] M. Lee and A. Abidi, "A 9 b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769–777, Apr 2008.

[33] L. Vercesi, A. Liscidini, and R. Castello, "Two-dimensions vernier time-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1504–1512, Aug 2010.

[34] K.-S. Kim, Y.-H. Kim, W. Yu, and S.-H. Cho, "A 7 bit, 3.75 ps resolution two-step time-to-digital converter in 65 nm CMOS using pulse-train time amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1009–1017, Apr 2013.

[35] N. Da Dalt, "Theory and implementation of digital bang-bang frequency synthesizers for high speed serial data communications," Ph.D. dissertation, RWTH Aachen University, Aachen, Germany, Feb 2007.

[36] G. Marzin, S. Levantino, C. Samori, and A. Lacaita, "A background calibration technique to control bandwidth in digital PLLs," in *ISSCC Dig. Tech. Papers*, Feb 2014, pp. 54–55.

[37] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1762–1772, Aug. 2014.

[38] X. Gao, E. Klumperink, P. Geraedts, and B. Nauta, "Jitter analysis and a benchmarking figure-of-merit for phase-locked loops," *IEEE Trans. Circuits Syst. II*, vol. 56, no. 2, pp. 117–121, Feb. 2009.

[39] C.-W. Yao, L. Lin, B. Nissim, H. Arora, and T. Cho, "A low spur fractional-N digital PLL for 802.11 a/b/g/n/ac with 0.19 ps_{rms} jitter," in *IEEE VLSI Circuits Sym. Tech. Papers*, June 2011, pp. 110–111.

[40] Y. Li, C. Ornelas, H.-S. Kim, H. Lakdawala, A. Ravi, and K. Soumyanath, "A reconfigurable distributed all-digital clock generator core with SSC and skew correction in 22nm high-k tri-gate LP CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2012, pp. 70–72.

[41] G. Shu, W.-S. Choi, S. Saxena, M. Talegaonkar, T. Anand, A. Elkholy, A. Elshazly, and P. Hanumolu, "A 4-to-10.5 Gb/s continuous-rate digital clock and data recovery with automatic frequency acquisition," *IEEE J. Solid-State Circuits*, vol. PP, no. 99, pp. 1–12, 2016.

[42] J. Kim, A. Balankutty, A. Elshazly, Y.-Y. Huang, H. Song, K. Yu, and F. O'Mahony, "3.5 a 16-to-40Gb/s quarter-rate NRZ/PAM4 dual-mode transmitter in 14nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2015, pp. 1–3.

[43] Y. Frans, D. Carey, M. Erett, H. Amir-Aslanzadeh, W. Fang, D. Turker, A. Jose, A. Bekele, J. Im, P. Upadhyaya, Z. Wu, K. Hsieh, J. Savoj, and K. Chang, "A 0.5-16.3 Gb/s fully adaptive flexible-reach transceiver for FPGA in 20 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1932–1944, Aug 2015.

[44] T. Kawamoto, T. Norimatsu, K. Kogo, F. Yuki, N. Nakajima, M. Tsuge, T. Usugi, T. Hokari, H. Koba, T. Komori, J. Nasu, T. Kawamata, Y. Ito, S. Umai, J. Kumazawa, H. Kurahashi, T. Muto, T. Yamashita, M. Hasegawa, and K. Higeta, "3.2 Multi-standard 185fs_{rms} 0.3-to-28Gb/s 40dB backplane signal conditioner with adaptive pattern-match 36-tap DFE and data-rate-adjustment PLL in 28nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2015, pp. 1–3.

[45] P. Upadhyaya, J. Savoj, F.-T. An, A. Bekele, A. Jose, B. Xu, D. Wu, D. Furker, H. Aslanzadeh, H. Hedayati, J. Im, S.-W. Lim, S. Chen, T. Pham, Y. Frans, and K. Chang, "3.3 A 0.5-to-32.75Gb/s flexible-reach wireline transceiver in 20nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2015, pp. 1–3.

[46] M.-W. Chen, D. Su, and S. Mehta, "A calibration-free 800 MHz fractional-N digital PLL with embedded TDC," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2819–2827, Dec 2010.

[47] W. Grollitsch, R. Nonis, and N. Da Dalt, "A 1.4psrms-period-jitter TDC-less fractional-N digital PLL with digitally controlled ring oscillator in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 478–479.

[48] T.-K. Jang, X. Nan, F. Liu, J. Shin, H. Ryu, J. Kim, T. Kim, J. Park, and H. Park, "A 0.026mm^2 5.3mW 32-to-2000MHz digital fractional-N phase locked-loop using a phase-interpolating phase-to-digital converter," in *ISSCC Dig. Tech. Papers*, Feb 2013, pp. 254–255.

[49] J. Liu, T.-K. Jang, Y. Lee, J. Shin, S. Lee, T. Kim, J. Park, and H. Park, "15.2 A 0.012mm^2 3.1mW bang-bang digital fractional-N PLL with a power-supply-noise cancellation technique and a walking-one-phase-selection fractional frequency divider," in *ISSCC Dig. Tech. Papers*, Feb 2014, pp. 268–269.

[50] K. Takinami, R. Strandberg, P. Liang, G. Le Grand de Mercey, T. Wong, and M. Hassibi, "A distributed oscillator based all-digital PLL with a 32-phase embedded phase-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2650–2660, Nov 2011.

[51] S. Levantino, G. Marucci, G. Marzin, A. Fenaroli, C. Samori, and A. L. Lacaita, "A 1.7 GHz fractional-N frequency synthesizer based on a multiplying delay-locked loop," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2678–2691, Nov 2015.

[52] A. Elkholy, S. Saxena, R. Nandwana, A. Elshazly, and P. Hanumolu, "A 4mW wide bandwidth ring-based fractional-N DPLL with 1.9ps$_{rms}$ integrated-jitter," in *Proc. IEEE Custom Int. Circuits Conf. (CICC)*, Sept 2015, pp. 1–4.

[53] A. Elkholy, T. Anand, W.-S. Choi, A. Elshazly, and P. Hanumolu, "A 3.7 mW low-noise wide-bandwidth 4.5 GHz digital fractional-N PLL using time amplifier-based TDC," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 867–881, April 2015.

[54] C. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, July 2000.

[55] R. Navid, T. Lee, and R. Dutton, "Minimum achievable phase noise of RC oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 630–637, March 2005.

[56] H. Wu, M. Mikhemar, D. Murphy, H. Darabi, and M.-C. Chang, "A blocker-tolerant inductor-less wideband receiver with phase and thermal noise cancellation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2948–2964, Dec 2015.

[57] A. Hafez, M.-S. Chen, and C.-K. Yang, "A 32-48 Gb/s serializing transmitter using multiphase serialization in 65 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 763–775, March 2015.

[58] J. Lin, B. Haroun, T. Foo, J.-S. Wang, B. Helmick, S. Randall, T. Mayhugh, C. Barr, and J. Kirkpatrick, "A PVT tolerant 0.18MHz to 600MHz self-calibrated digital PLL in 90nm CMOS process," in *ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 488–489.

[59] P.-Y. Wang, J.-H. C. Zhan, H.-H. Chang, and H.-M. S. Chang, "A digital intensive fractional-N PLL and all-digital self-calibration schemes," *IEEE J. Solid-State Circuits*, vol. 44, pp. 2182–2192, Aug. 2009.

[60] W. Yin, R. Inti, A. Elshazly, B. Young, and P. Hanumolu, "A 0.7-to-3.5GHz 0.6-to-2.8mW highly digital phase-locked loop with bandwidth tracking," *IEEE J. Solid-State Circuits*, vol. 46, Aug. 2011.

[61] D. Mijuskovic, M. Bayer, T. Chomicz, N. Garg, F. James, P. McEntarfer, and J. Porter, "Cell-based fully integrated CMOS frequency synthesizers," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 271–279, Mar 1994.

[62] I. I. Novof, J. Austin, R. Kelkar, D. Strayer, and S. Wyatt, "Fully integrated CMOS phase-locked loop with 15 to 240 MHz locking range and ±50 ps jitter," *IEEE J. Solid-State Circuits*, vol. 30, no. 11, pp. 1259–1266, Nov 1995.

[63] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723–1732, Nov 1996.

[64] R. Nonis, N. D. Dalt, P. Palestri, and L. Selmi, "Modeling, design and characterization of a new low-jitter analog dual tuning LC-VCO PLL architecture," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1303–1309, June 2005.

[65] M. Ferriss, J. O. Plouchart, A. Natarajan, A. Rylyakov, B. Parker, J. A. Tierno, A. Babakhani, S. Yaldiz, A. Valdes-Garcia, B. Sadhu, and D. J. Friedman, "An integral path self-calibration scheme for a dual-loop PLL," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 996–1008, April 2013.

[66] Y. Akazawa, H. Kikuchi, A. Iwata, T. Matsuura, and T. Takahashi, "Low power 1 GHz frequency synthesizer LSI's," *IEEE J. Solid-State Circuits*, vol. 18, no. 1, pp. 115–121, Feb 1983.

[67] J. Rogers, C. Plett, and F. Dai, *Integrated Circuit Design for High-speed Frequency Synthesis*, ser. Artech House microwave library. Artech House, 2006. [Online]. Available: https://books.google.com/books?id=ZR5TAAAAMAAJ

[68] C. Vaucher and D. Kasperkovitz, "A wide-band tuning system for fully integrated satellite receivers," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 987–997, Jul 1998.

[69] M. Eissa and M. El-Shennawy, "A technique for robust division ratio switching in multi modulus dividers with modulus extension," in *Int. Conf. on Microelectronics (ICM)*, Dec 2010, pp. 84–87.

[70] P. Nuzzo, K. Vengattaramane, M. Ingels, V. Giannini, M. Steyaert, and J. Craninckx, "A 0.1-5GHz dual-VCO software-defined $\Sigma\Delta$ frequency synthesizer in 45nm digital CMOS," in *Proc. of IEEE RFIC Symposium*, June 2009, pp. 321–324.

[71] R. Nandwana, T. Anand, S. Saxena, S.-J. Kim, M. Talegaonkar, A. Elkholy, W.-S. Choi, A. Elshazly, and P. Hanumolu, "A calibration-free fractional-N ring PLL using hybrid phase/current-mode phase interpolation method," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 882–895, April 2015.

[72] T. H. Tsai, M. S. Yuan, C. H. Chang, C. C. Liao, C. C. Li, and R. B. Staszewski, "14.5 a 1.22ps integrated-jitter 0.25-to-4GHz fractional-N ADPLL in 16nm FinFET CM0S," in *ISSCC Dig. Tech. Papers*, Feb 2015, pp. 1–3.

[73] H. Lakdawala, M. Schaecher, C.-T. Fu, R. Limaye, J. Duster, Y. Tan, A. Balankutty, E. Alpman, C. Lee, S. Suzuki, B. Carlton, H.-S. Kim, M. Verhelst, S. Pellerano, T. Kim, D. Srivastava, S. Venkatesan, H.-J. Lee, P. Vandervoorn, J. Rizk, C.-H. Jan, K. Soumyanath, and S. Ramamurthy, "32nm x86 OS-compliant PC on-chip with dual-core atom ® processor and RF WiFi transceiver," in *ISSCC Dig. Tech. Papers*, Feb 2012, pp. 62–64.

[74] G. Magklis, G. Semeraro, D. Albonesi, S. Dropsho, S. Dwarkadas, and M. Scott, "Dynamic frequency and voltage scaling for a multiple-clock-domain microprocessor," *IEEE Micro*, vol. 23, no. 6, pp. 62–68, Nov 2003.

[75] A. Allen, J. Desai, F. Verdico, F. Anderson, D. Mulvihill, and D. Krueger, "Dynamic frequency-switching clock system on a quad-core itanium® processor," in *ISSCC Dig. Tech. Papers*, Feb 2009, pp. 62–63,63a.

[76] D. De Caro, F. Tessitore, G. Vai, N. Imperato, N. Petra, E. Napoli, C. Parrella, and A. Strollo, "A 3.3 GHz spread-spectrum clock generator supporting discontinuous frequency modulations in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 2074–2089, Sept 2015.

[77] H.-R. Lee, O. Kim, G. Ahn, and D.-K. Jeong, "A low-jitter 5000ppm spread spectrum clock generator for multi-channel SATA transceiver in 0.18 μm CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2005, pp. 162–590 Vol. 1.

[78] K. Hardin, J. Fessler, and D. Bush, "Spread spectrum clock generation for the reduction of radiated emissions," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Aug 1994, pp. 227–231.

[79] H. Mair and L. Xiu, "An architecture of high-performance frequency and phase synthesis," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 835–846, June 2000.

[80] Y.-H. Liu and T.-H. Lin, "An energy-efficient 1.5-Mbps wireless FSK transmitter with a $\Sigma\Delta$-modulated phase rotator," in *Proc. European Solid-State Circuits Conf. (ESS-CIRC)*, Sept 2007, pp. 488–491.

[81] ——, "A wideband PLL-based G/FSK transmitter in 0.18 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2452–2462, Sept 2009.

[82] P.-E. Su and S. Pamarti, "A 2.4 GHz wideband open-loop GFSK transmitter with phase quantization noise cancellation," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 615–626, March 2011.

[83] T. Anand, M. Talegaonkar, A. Elshazly, B. Young, and P. Hanumolu, "A 2.5GHz 2.2mW/25μW on/off-state power 2psrms-long-term-jitter digital clock multiplier with 3-reference-cycles power-on time," in *ISSCC Dig. Tech. Papers*, Feb 2013, pp. 256–257.

[84] Y. Li, C. Ornelas, H. S. Kim, H. Lakdawala, A. Ravi, and K. Soumyanath, "A reconfigurable distributed all-digital clock generator core with SSC and skew correction in 22nm high-k tri-gate LP CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2012, pp. 70–72.

[85] P. Park, J. Park, H. Park, and S. Cho, "An all-digital clock generator using a fractionally injection-locked oscillator in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2012, pp. 336–337.

[86] S. Damphousse, K. Ouici, A. Rizki, and M. Mallinson, "All digital spread spectrum clock generator for EMI reduction," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 145–150, Jan 2007.

[87] D. De Caro, C. Romani, N. Petra, A. Strollo, and C. Parrella, "A 1.27 GHz, all-digital spread spectrum clock generator/synthesizer in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1048–1060, May 2010.

[88] J. Kim, J.-K. Kim, B.-J. Lee, N. Kim, D.-K. Jeong, and W. Kim, "A 20-GHz phase-locked loop for 40-Gb/s serializing transmitter in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 899–908, April 2006.

[89] B. Catli, A. Nazemi, T. Ali, S. Fallahi, Y. Liu, J. Kim, M. Abdul-Latif, M. Ahmadi, H. Maarefi, A. Momtaz, and N. Kocaman, "A sub-200 fs RMS jitter capacitor multiplier loop filter-based PLL in 28 nm CMOS for high-speed serial communication applications," in *Proc. IEEE Custom Int. Circuits Conf. (CICC)*, Sept 2013, pp. 1–4.

[90] X. Gao, E. Klumperink, M. Bohsali, and B. Nauta, "A low noise sub-sampling PLL in which divider noise is eliminated and PD/CP noise is not multiplied by N^2," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3253–3263, Dec 2009.

[91] X. Gao, E. Klumperink, G. Socci, M. Bohsali, and B. Nauta, "A 2.2GHz sub-sampling PLL with 0.16ps$_{rms}$ jitter and -125dBc/Hz in-band phase noise at 700μw loop-components power," in *IEEE VLSI Circuits Sym. Tech. Papers*, June 2010, pp. 139–140.

[92] S. Ye, L. Jansson, and I. Galton, "A multiple-crystal interface PLL with VCO re-alignment to reduce phase noise," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, Dec 2002.

[93] R. Farjad-Rad, W. Dally, H.-T. Ng, R. Senthinathan, M.-J. Lee, R. Rathi, and J. Poulton, "A low-power multiplying DLL for low-jitter multigigahertz clock generation in highly integrated digital chips," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1804–1812, Dec 2002.

[94] A. Elshazly, R. Inti, B. Young, and P. Hanumolu, "Clock multiplication techniques using digital multiplying delay-locked loops," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1416–1428, June 2013.

[95] G. Marucci, A. Fenaroli, G. Marzin, S. Levantino, C. Samori, and A. Lacaita, "A 1.7GHz MDLL-based fractional-N frequency synthesizer with 1.4ps RMS integrated jitter and 3mW power using a 1b TDC," in *ISSCC Dig. Tech. Papers*, Feb 2014, pp. 360–361.

[96] C.-F. Liang and K.-J. Hsiao, "An injection-locked ring PLL with self-aligned injection window," in *ISSCC Dig. Tech. Papers*, Feb 2011, pp. 90–92.

[97] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A compact, low-power and low-jitter dual-loop injection locked PLL using all-digital PVT calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 50–60, Jan 2014.

[98] J.-C. Chien, P. Upadhyaya, H. Jung, S. Chen, W. Fang, A. Niknejad, J. Savoj, and K. Chang, "A pulse-position-modulation phase-noise-reduction technique for a 2-to-16 GHz injection-locked ring oscillator in 20nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2014, pp. 52–53.

[99] B. Helal, C.-M. Hsu, K. Johnson, and M. Perrott, "A low jitter programmable clock multiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391–1400, May 2009.

[100] Y.-C. Huang and S.-I. Liu, "A 2.4-GHz subharmonically injection-locked PLL with self-calibrated injection timing," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 417–428, Feb 2013.

[101] I.-T. Lee, Y.-J. Chen, S.-I. Liu, C.-P. Jou, F.-L. Hsueh, and H.-H. Hsieh, "A divider-less sub-harmonically injection-locked PLL with self-adjusted injection timing," in *ISSCC Dig. Tech. Papers*, Feb 2013, pp. 414–415.

[102] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

[103] M. Elbadry, B. Sadhu, J. Qiu, and R. Harjani, "Dual-channel injection-locked quadrature LO generation for a 4-GHz instantaneous bandwidth receiver at 21-GHz center frequency," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 3, pp. 1186–1199, March 2013.

[104] H.-Y. Chang, Y.-L. Yeh, Y.-C. Liu, M.-H. Li, and K. Chen, "A low-jitter low-phase-noise 10-GHz sub-harmonically injection-locked PLL with self-aligned DLL in 65-nm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 3, pp. 543–555, March 2014.

[105] A. Elkholy, M. Talegaonkar, T. Anand, and P. Hanumolu, "A 6.75-to-8.25GHz 2.25mW 190fs$_{rms}$ integrated-jitter PVT-insensitive injection-locked clock multiplier using all-digital continuous frequency-tracking loop in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2015, pp. 1–3.

[106] A. Mazzanti, P. Uggetti, and F. Svelto, "Analysis and design of injection-locked LC dividers for quadrature generation," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1425–1433, Sept 2004.

[107] F. O'Mahony, S. Shekhar, M. Mansuri, G. Balamurugan, J. Jaussi, J. Kennedy, B. Casper, D. Allstot, and R. Mooney, "A 27Gb/s forwarded-clock I/O receiver using an injection-locked LC-DCO in 45nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2008, pp. 452–627.

[108] P. Kinget, R. Melville, D. Long, and V. Gopinathan, "An injection-locking scheme for precision quadrature generation," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 845–851, Jul 2002.

[109] J. Lee and M. Liu, "A 20-Gb/s burst-mode clock and data recovery circuit using injection-locking technique," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 619–630, March 2008.

[110] T. Lee and J. Bulzacchelli, "A 155-MHz clock recovery delay- and phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1736–1746, Dec 1992.

[111] A. Hajimiri and T. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb 1998.

[112] P. Maffezzoni, "Analysis of oscillator injection locking through phase-domain impulse-response," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 5, pp. 1297–1305, June 2008.

[113] D. Dunwell and A. Carusone, "Modeling oscillator injection locking using the phase domain response," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 11, pp. 2823–2833, Nov 2013.

[114] P. Maffezzoni and S. Levantino, "Phase noise of pulse injection-locked oscillators," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 10, pp. 2912–2919, Oct 2014.

[115] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sept 2004.

[116] N. Da Dalt, C. Kropf, M. Burian, T. Hartig, and H. Eul, "A 10b 10GHz digitlly controlled LC oscillator in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb 2006, pp. 669–678.

[117] B. Nikolić, V. G. Oklobdžija, V. Stojanović, W. Jia, J. K.-S. Chiu, and M. Leung, "Improved sense-amplifier-based flip-flop: design and measurements," *IEEE J. Solid-State Circuits*, vol. 35, pp. 876–884, Jun. 2000.

[118] A. Elkholy, M. Talegaonkar, T. Anand, and P. K. Hanumolu, "Design and analysis of low-power high-frequency robust sub-harmonic injection-locked clock multipliers," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3160–3174, Dec 2015.

[119] A. Elkholy, A. Elmallah, M. Elzeftawi, K. Chang, and P. K. Hanumolu, "A 6.75-to-8.25GHz, 250fsrms-integrated-jitter 3.25mW rapid on/off PVT-insensitive fractional-N injection-locked clock multiplier in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Jan 2016, pp. 192–193.

[120] T. Anand, M. Talegaonkar, A. Elkholy, S. Saxena, A. Elshazly, and P. K. Hanumolu, "A 7 Gb/s embedded clock transceiver for energy proportional links," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3101–3119, Dec 2015.

[121] G. Shu, W.-S. Choi, S. Saxena, S.-J. Kim, M. Talegaonkar, R. Nandwana, A. Elkholy, D. Wei, T. Nandi, and P. K. Hanumolu, "A 16Mb/s-to-8Gb/s 14.1-to-5.9pJ/b source synchronous transceiver using DVFS and rapid on/off in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Jan 2016, pp. 398–399.

[122] P. K. Hanumolu, M. Brownlee, K. Mayaram, and U.-K. Moon, "Analysis of charge-pump phase-locked loops," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 9, pp. 1665–1674, Sept 2004.

[123] K. Raczkowski, N. Markulic, B. Hershberg, and J. Craninckx, "A 9.2-12.7 GHz wide-band fractional-N subsampling PLL in 28 nm CMOS with 280 fs RMS jitter," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1203–1213, May 2015.

[124] Z. Z. Chen, Y. H. Wang, J. Shin, Y. Zhao, S. A. Mirhaj, Y. C. Kuan, H. N. Chen, C. P. Jou, M. H. Tsai, F. L. Hsueh, and M. C. F. Chang, "Sub-sampling all-digital fractional-N frequency synthesizer with -111dBc/Hz in-band phase noise and an FOM of -242db," in *ISSCC Dig. Tech. Papers*, Feb 2015, pp. 1–3.

[125] A. Elkholy, S. Saxena, R. K. Nandwana, A. Elshazly, and P. K. Hanumolu, "A 2.0-5.5 GHz wide bandwidth ring-based digital fractional-N PLL with extended range multi-modulus divider," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1771–1784, Aug 2016.