TIME-BASED CONTROL TECHNIQUES FOR INTEGRATED DC-DC CONVERSION

BY

SEONG JOONG KIM

DISSERTATION

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Doctoral Committee:

Associate Professor Pavan Kumar Hanumolu, Chair
Research Professor Philip T. Krein
Professor Naresh R. Shanbhag
Assistant Professor Robert Pilawa-Podgurski

ABSTRACT

Time-based control techniques for the design of high switching frequency buck converters are presented. Using time as the processing variable, the proposed controller operates with CMOS-level digital-like signals but without adding any quantization error. A ring oscillator is used as an integrator in place of conventional opamp-RC or G_m-C integrators while a delay line is used to perform voltage-to-time conversion and to sum time signals. A simple flip-flop generates a pulse-width modulated signal from the time-based output of the controller. Hence time-based control eliminates the need for a wide bandwidth error amplifier, pulse-width modulator (PWM) in analog controllers or high-resolution analog-to-digital converter (ADC) and digital PWM in digital controllers. As a result, it can be implemented in a small area and with minimal power.

First, a time-based single-phase buck converter is proposed and fabricated in a 180nm CMOS process, the prototype buck converter occupies an active area of $0.24mm^2$, of which the controller occupies only $0.0375mm^2$. It operates over a wide range of switching frequencies (10-25 MHz) and regulates output to any desired voltage in the range of 0.6V to 1.5V with 1.8V input voltage. With a 500mA step in the load current, the settling time is less than $3.5\mu s$ and the measured reference tracking bandwidth is about 1MHz. Better than 94% peak efficiency is achieved while consuming a quiescent current of only $2\mu A/MHz$.

Second, the techiniques are extended to a high switching frequency multi-phase buck converter. Efficiency degradation due to mismatch between the phases is mitigated by generating precisely matched duty-cycles by combining a time-based multi-phase generator (MPG) with a time-based PID compensator (T-PID). The proposed approach obviates the need for a complex current sensing and calibration circuitry needed to implement active current sharing in an analog controller. It also eliminates the need for a high-resolution analog-to-digital

converter and digital pulse width modulator needed for implementing passive current sharing in a digital controller. Fabricated in a 65nm CMOS process, the prototype multi-phase buck converter occupies an active area of 0.32mm^2, of which the controller occupies only 0.04mm^2. The converter operates over a wide range of switching frequencies (30-70 MHz) and regulates output to any desired voltage in the range of 0.6V to 1.5V from 1.8V input voltage. With a 400mA step in the load current, the settling time is less than 0.6μs and the measured duty-cycle mismatch is less than 0.48%. Better than 87% peak efficiency is achieved while consuming a quiescent current of only 3μA/MHz.

Finally, light load operation is discussed.The light load efficiency of a time-based buck converter is improved by adding proposed PFM control. At the same time, the proposed seamless transition techniques provide a freedom to change the control mode between PFM and PWM without deteriorating output voltage which allows for a system to manage its power efficiently. Fabricated in a 65nm CMOS, the prototype achieves 90% peak efficiency and $>$ 80% efficiency over an I_{LOAD} range of 2mA to 800mA. V_O changes by less than 40mV during PWM to PFM transitions.

To my family, for their love and support.

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CHAPTER 1

INTRODUCTION

1.1 High Switching Frequency (F_{SW}) DC-DC Converters

Switching DC-DC power converters are essential components in almost all electronic systems in general and portable and hand-held devices in particular. Buck converters are omnipresent in battery powered devices where they are used to generate supply voltages for analog, digital, and radio-frequency ICs. The growing demand to miniaturize portable devices and increase their battery life while at the same time integrating more functionality into them has resulted in an exponential increase in the power density requirement that should be met without compromising power efficiency. Along with high efficiency, converters must also be capable of operating across a wide range of load current and input/output voltages. These features are needed to support techniques such as dynamic voltage scaling for improving power efficiency, especially of digital ICs. Switching buck converters can be implemented using either hysteretic controllers or pulse width modulation (PWM) based controllers. Hysteretic control is simple to implement, achieves good efficiency as well as fast transient response and can be fully integrated in a small area [1]. However, its non-linear behavior leads to large output ripple, unpredictable loop dynamics, and wide variation in switching frequency, which are undesirable in many noise-sensitive portable applications. Recently, various control techniques have been proposed to achieve fixed switching frequency operation in a hysteretic converter [2–5]. As a result, PWM controllers are almost exclusively used in noise-sensitive portable applications as they operate with constant switching frequency and achieve excellent efficiency. However, PWM controllers often require large capacitors that are either impossible to integrate on-die or incur a prohibitively large area penalty. Using external components takes away premium board space and increases system

cost. Even if the controller and the power switches are fully integrated on a single chip, the form factor of the power converter is usually dominated by the size of LC filter. In particular, an inductor whose value is typically in the range of few μH occupies a large area on the board. Techniques that can reduce the size of L and C without compromising efficiency are therefore highly desirable.

Dynamic voltage scaling (DVS) and aggressive use of low power states are shown to be very effective in improving the energy efficiency of complex digital systems such as processors [6]. However, such dynamic power management techniques put additional requirements on the buck converter that provides the supply voltage. For instance, DVS mandates that the converter support a wide range of output voltages and closely tracks the reference voltage. Entering/exiting low power states introduces large load transients that must be supported by the converter without compromising output voltage accuracy. In other words, fast tracking response and good load regulation are also essential features of a buck converter.

In view of these requirements, the most viable approach to achieve both the small form factor and fast tracking response is increasing the switching frequency, F_{SW}, because values of L and C scale inversely proportional to F_{SW} and the tracking bandwidth can be increased proportionally with F_{SW}.

1.2 Multi-Phase DC-DC Buck Convertors

Maintaining high efficiency across a wide range of load currents in a single-phase DC-DC converter is difficult. Power switches designed to reduce conduction loss at large load currents incur large switching loss, which severely degrades efficiency under light load conditions. Multi-phase converters are used to overcome this trade-off by controlling the number of operating phases in proportion to the load current [7–9]. They also provide additional benefit of output current ripple cancellation as illustrated in Fig. 1.1 [10]. The smaller current ripple enables a smaller input/output capacitor and power inductor, which helps to not only achieve a small form factor but also improves the transient response [7, 8]. However, implementation of high-efficiency multi-phase converters also has some difficulties. First, mismatch between the power-trains generates uneven current flow across individual power-

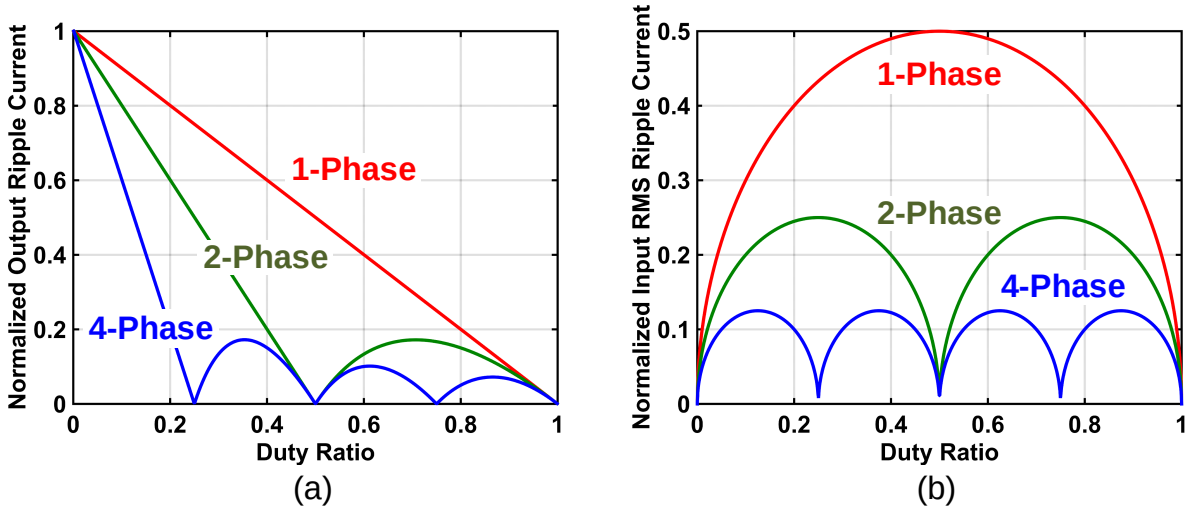


Figure 1.1: Ripple cancellation in multi-phase converters: (a) output current and (b) input current.

trains and significantly degrades converter efficiency [11]. Furthermore, excessive current in one of the power-trains may saturate the inductor, decrease lifetime or cause permanent damage to the inductor [11–13]. There are two commonly used solutions to overcome these issues. The first approach, referred to as active current sharing, is based on matching currents in all power-trains [7]. However, this technique requires high-precision current sensing circuitry along with complex calibration and control schemes to force currents in all the power-trains to be the same. The second approach, referred to as passive current sharing, is based on duty-cycle matching [12]. As explained later (see Section 3.1), matching only duty-cycles (as opposed to matching currents) also ensures high efficiency. However, generating precisely matched duty-cycles using classical analog pulse width modulators is difficult due to their susceptibility to component mismatch. Instead, a digital PWM generator can produce matched duty-cycles [11, 12, 14]. The digital implementation also features small controller area and robustness to noise in addition to precise duty-cycle matching. However, digitally controlled DC-DC converters exhibit undesirable limit cycling behavior due to the inevitable quantization error introduced in the digital controller [15]. Furthermore, highly accurate DC-DC converters operating at high F_{SW} require a high-resolution and high-speed digital PWM generator and an analog-to-digital converter (ADC), both of which consume significant power and area [12, 16].

1.3 Time-Based PID Controller for Light Load

Even though the dynamic power management techniques supported by a high tracking bandwidth (BW) DC-DC converter (i.e. high F_{SW} DC-DC converter) in energy-aware hand-held devices can manage the power consumption of a system efficiently, the light load efficiency in a PWM controlled converter itself is limited by the switching loss which becomes a severe problem especially in a high F_{SW} converters. In order to solve this problem, pulse frequency modulation (PFM) control is commonly used. PFM control manipulates the switching frequency proportional to the load magnitude which also reduces the switching loss accordingly, thereby achieving high efficiency. However, PFM control has some drawbacks compared to PWM control. Power conversion efficiency is not better than PWM mode especially for medium and heavy load because the conduction loss is larger due to the higher peak inductor current than PWM operation. It generally exhibits a larger output voltage ripple which may not be allowed during noise-sensitive circuit operations. Moreover, the variation of the switching frequency along with load magnitude change can introduce a considerable amount of in-band noise for RF application. Consequently, operating in both PWM mode and PFM mode is desirable and the capability to seamlessly change the operation modes is inevitable for power efficient system management.

In this research, time-based design techniques are elaborated to provide effective solutions for a high F_{SW} buck converters. In Chapter 2, a time-based controller that overcomes the aforementioned issues associated with both analog and digital controllers with high F_{SW} is introduced. By using time as the processing variable, we eliminate the need for wide bandwidth amplifiers, PWM block, high-resolution ADCs and digital pulse width modulator (DPWM), while still operating with CMOS-level digital-like signals [17]. In other words, the time-based approach combines the advantages of both analog and digital controllers. Fabricated in a 180nm CMOS process, measured results are shown to prove the efficacy of the proposed controller. In Chapter 3, a time-based multi-phase controller architecture is proposed which efficiently implements passive current sharing without area and power penalty while operating at high F_{SW} for heavy load condition [18]. By generating multiple inherently matched PWM signals, the architecture maximizes efficiency, eliminates the need

for active current sharing, and achieves excellent regulation accuracy and fast load transient response across a wide range of output voltages. Also fabricated in a 65nm CMOS process, the proposed controller demonstrates promising results. In Chapter 4, light load efficiency of a time-based PWM controller is improved by combining time-based PWM control with on-time controlled PFM. In addition, a seamless transition between PWM and PFM modes is achieved by proposed time-domain presetting techniques.

CHAPTER 2

TIME-BASED DESIGN TECHNIQUES

2.1 Trade-Offs in Buck Converter Design

2.1.1 Buck Converter with Voltage-Mode PID Compensator

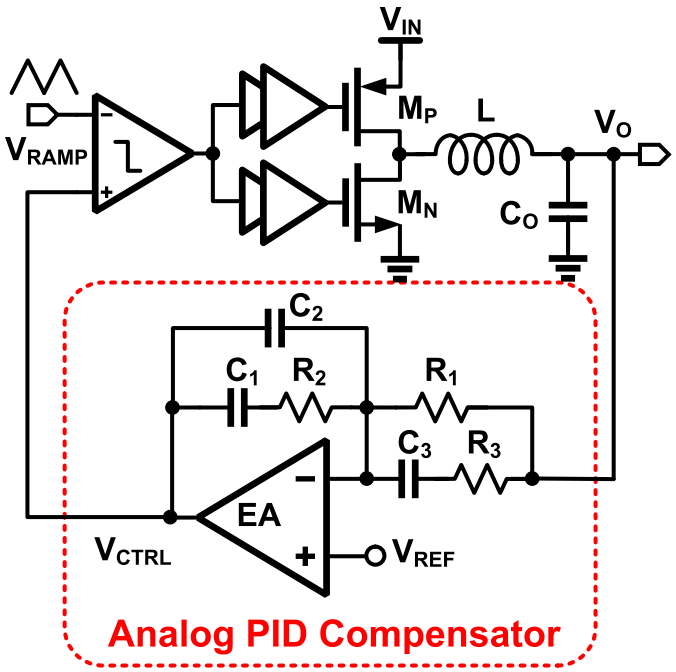


Figure 2.1: Voltage-mode PID buck converter.

The schematic of a buck converter with voltage-mode PID compensator is shown in Fig. 2.1 [19]. Compared to current-mode control, this architecture is more commonly used as it is simple and can achieve high efficiency as well as a fast tracking response. However, it requires large capacitors, high performance error amplifier, and a high-speed comparator with small delay. To quantify the impact of these requirements on area and power of the

controller, consider the design of a buck converter with F_{SW} = 10MHz. Assuming a 220nH power inductor, 4.7μF output capacitor and 20kΩ resistance for R_1, a total capacitance ($C_{tot} = C_1 + C_2 + C_3$) of 130pF is needed for the compensator [19], which occupies more than 385μm $\times$ 385μm of the silicon area, assuming 0.8fF/μm^2 capacitor density. This issue of large silicon area is further exacerbated at lower F_{SW}. High F_{SW} also mandates a very large gain bandwidth product (GBW) for the error amplifier. Assuming a DC gain of 60dB is needed for accurate regulation with a loop bandwidth of 1MHz, the GBW of the error amplifier needs to be as high as 10GHz assuming the required bandwidth of the error amplifier has to be 10 times higher than the loop bandwidth. Such a high error amplifire GBW can be achieved only by dissipating large power. Another limiting factor in high-speed converters is finite comparator delay and ON/OFF time of power switches M_P and M_N. For example, in

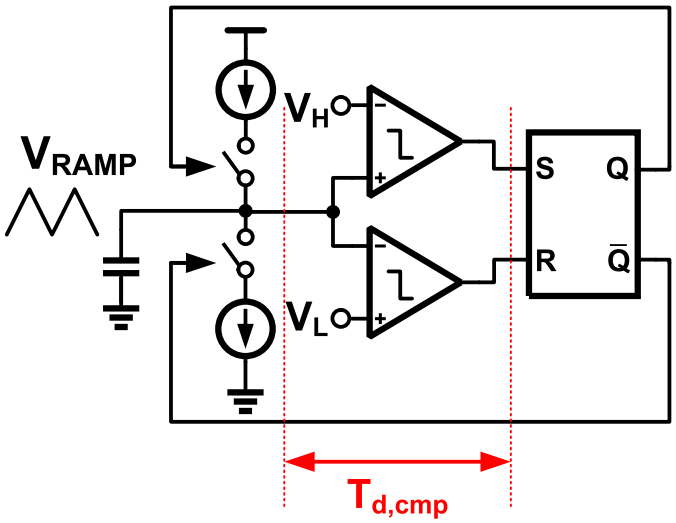


Figure 2.2: Schematic of a conventional ramp generator.

the case of a conventional ramp generator shown in Fig. 2.2, duty-cycle range is limited by the delay of comparators ($T_{d,cmp}$), as illustrated in Fig. 2.3 and expressed mathematically as:

$$D_{min} = \frac{2 \times T_{d,cmp}}{T_{SW}} \quad \text{and} \quad D_{max} = 1 - \frac{2 \times T_{d,cmp}}{T_{SW}} \tag{2.1}$$

where $T_{SW} = 1/F_{SW}$ and D_{min} and D_{max} are the minimum and maximum limits of the duty-cycle, respectively. In order to operate at F_{SW} = 10MHz with a duty-cycle range of 10% $-$ 90%, the required delay should be less than 5ns, which is quite difficult to achieve

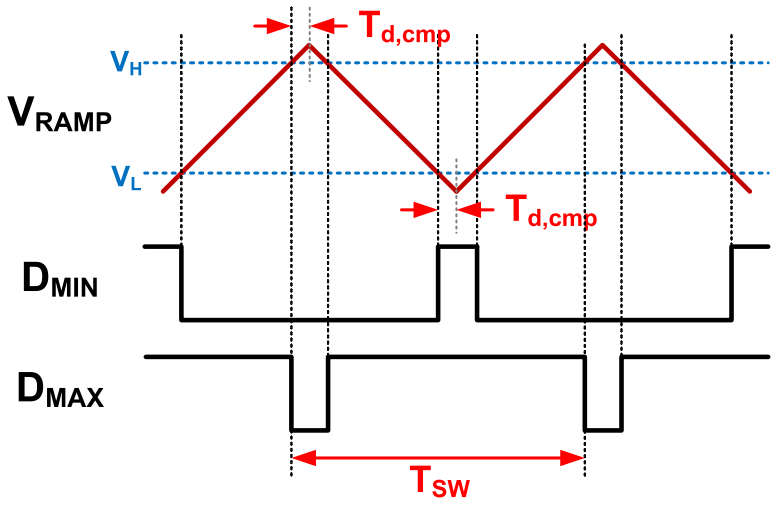


Figure 2.3: Illustration of the impact of comparator delay on duty-cycle range.

with low power consumption. A larger comparator delay limits the duty-cycle range, which not only affects the transient response but also limits the input/output operating voltage range.

2.1.2 Buck Converter with Digital PID Compensator

A digitally controlled converter shown in Fig. 2.4 obviates the need for capacitors and helps to achieve a lower controller area. The error voltage, v_e, is digitized using a analog-to-digital converter (ADC), whose output is processed by a digital PID compensator, wherein the proportional, integral, and derivative control portions are implemented by a gain scaler (performed by bit shifting), digital accumulator and differentiator, respectively. The digital compensator output is fed to a DPWM block, which performs digital-to-time (D-T) conversion and generates the desired duty-cycle. Because of the quantization error introduced by the ADC and DPWM, the converter behavior is non-linear and its steady-state is a bounded limit cycle, which manifests as output voltage ripple [20]. Reducing the ripple requires high-precision ADC and DPWM, both of which consume significant power and increase design complexity. In view of these drawbacks, we present a time-based compensator that combines the positive attributes of both the analog voltage-mode and digital PID compensators.

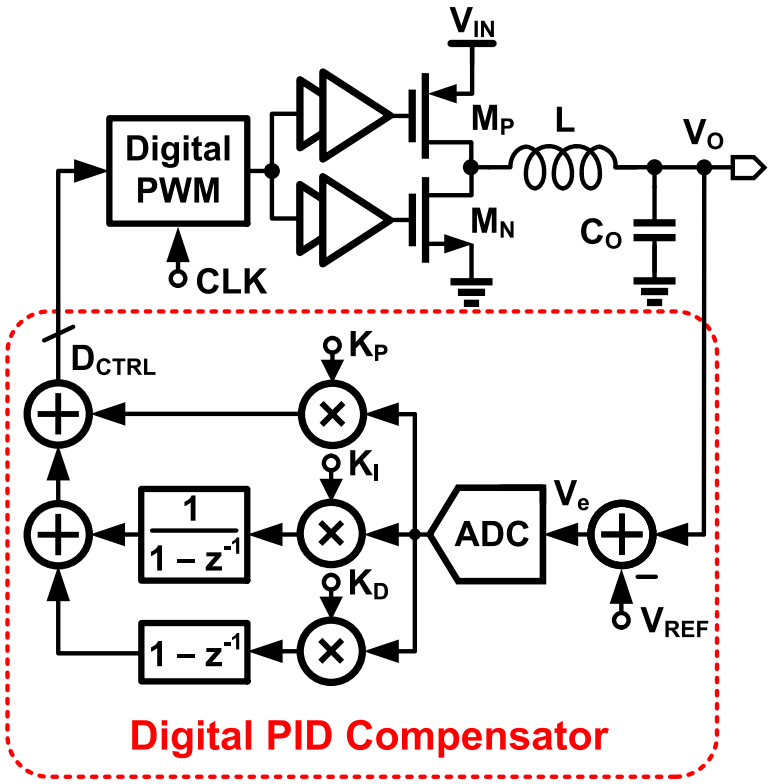


Figure 2.4: Digitally controlled PID buck converter.

2.2 Simplified Buck Converter Using Time-Based Control

A conceptual block diagram of a buck converter using the proposed time-based controller is shown in Fig. 2.5. It consists of a voltage-to-time converter that converts error voltage into a time signal and feeds it to the time-based compensator. The compensator performs time-based signal processing functions on its input to implement PID compensation and generates a time output in the form of a pulse-width modulated signal, V_{PWM}. Similar to a conventional buck converter, the V_{PWM} signal is filtered by external L and C to generate the desired output voltage, V_O. The proposed time-based control offers three main advantages. First, the compensator operates with rail-to-rail CMOS levels much like a digital controller. Because there is no quantization error, the converter behaves like a linear system in steady-state and achieves small ripple voltage similar to an analog voltage-mode PID buck converter. Second, the need for an explicit PWM generator is obviated because, as discussed later in Section 2.2.1, PWM generation is implicit in the proposed time-based processing, i.e. the output of the compensator itself is a PWM signal. Finally, it does not require any large

capacitor, high BW error amplifier, high-speed comparator, or an ADC. As a result, the proposed controller is extremely power and area efficient. These characteristics are elucidated in the context of a simple type-I converter in the following section.

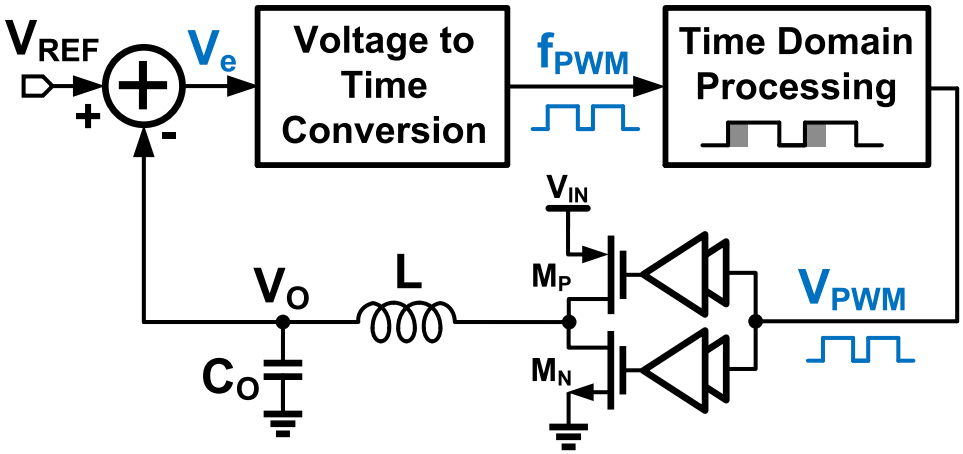


Figure 2.5: Conceptual block diagram of the buck converter using the proposed time-based compensator.

2.2.1 Type-I Buck Converter

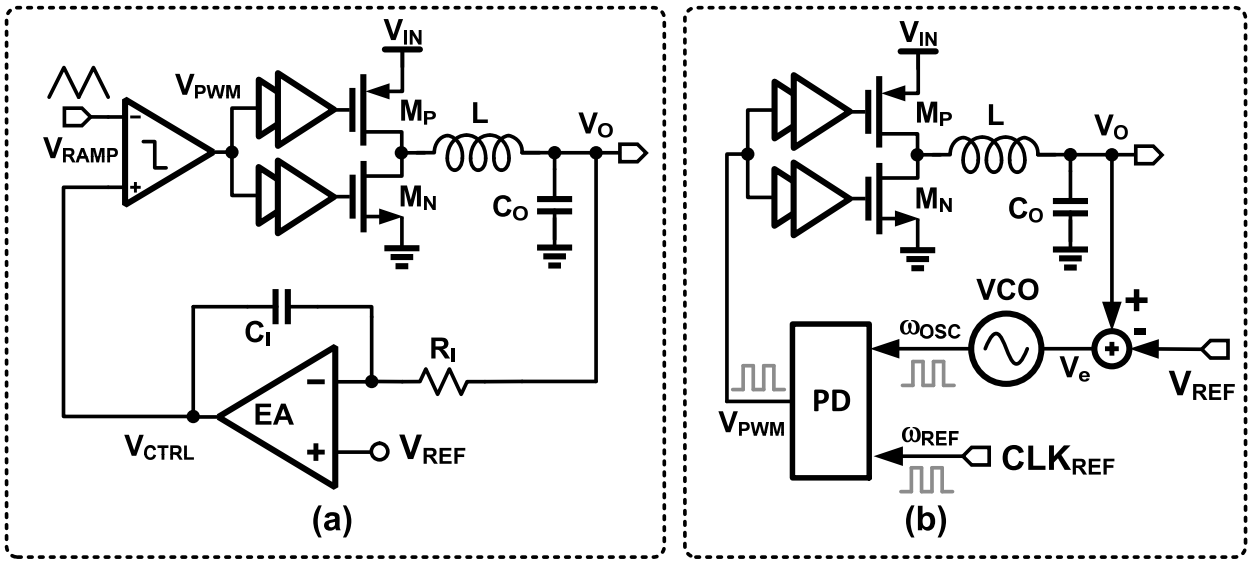


Figure 2.6: Simplified block diagram of: (a) voltage-mode type-I converter and (b) time-based type-I converter.

The simplified block diagrams of the conventional voltage-mode and proposed time-based

type-I buck converters are shown in Fig. 2.6. The voltage-mode integrator realized using an opamp-RC architecture is replaced by a time-based integrator implemented using a voltage-controlled ring oscillator (VCO) [21,22]. VCO converts error voltage, v_e, into frequency, ω_e, such that its oscillation frequency, ω_{OSC}, is equal to:

$$\omega_{\mathrm{OSC}} = \omega_{\mathrm{fr}} + \omega_e = \omega_{\mathrm{fr}} + \mathrm{K_{VCO}} v_e \tag{2.2}$$

where ω_{fr} is VCO's free running frequency expressed in rad/s and $\mathrm{K_{VCO}}$ is its gain expressed in units of rad/s/V. Because phase is the integral of frequency, VCO acts as a voltage-to-phase integrator with a transfer function, $\mathrm{H_{\Phi I}(s)}$, that can be expressed as follows:

$$\Phi_e(t) = \int_0^t \omega_e(\tau) d\tau \implies \mathrm{H_{\Phi I}(s)} = \frac{\Phi_e(s)}{v_e(s)} = \frac{\mathrm{K_{VCO}}}{s} \tag{2.3}$$

Hence, VCO provides both voltage-to-time conversion and loss-less integration functions. Another important advantage offered by the VCO integrator is that it provides infinite DC gain independent of transistor imperfections, supply voltage, and device technology as long as it oscillates. Because VCO is an integrator with voltage input and phase output, its output cannot be directly used to drive the power stage. However, the PWM signal needed to drive the power stage can be easily generated by comparing the VCO output phase with that of a reference clock using a phase detector (PD). In contrast to analog and digital PWM generators, PD, implemented using a simple SR-latch, generates the PWM control signal in the time-based compensator. The output of the PD, denoted by $\mathrm{V_{PWM}}$, is *set* to logic high by the positive edge of the reference clock and is *reset* to logic low by the subsequent positive edge of the VCO output. Similar to a voltage-mode converter, $\mathrm{V_{PWM}}$ drives the power switches, $\mathrm{M_P}$ and $\mathrm{M_N}$, with a duty-cycle D and the resulting output is filtered by the LC filter to generate the output voltage, $\mathrm{V_O}$. Redrawing the time-based type-I buck converter as shown in Fig. 2.7, reveals that it can be viewed as a type-I phase-locked loop (PLL). Therefore, assuming the reference clock frequency is within pull-in range, the feedback loop forces the VCO frequency, ω_{OSC}, to be equal to the reference clock frequency, ω_{REF}. Hence,

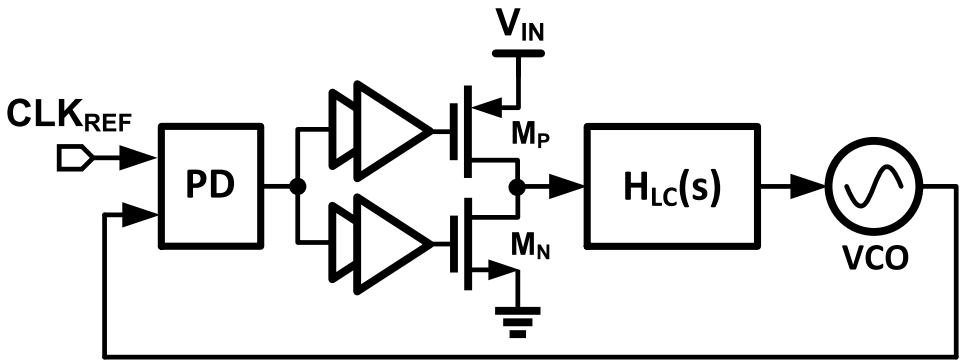


Figure 2.7: Type-I phase-locked loop view of the time-based type-I buck converter.

in steady-state,

$$\omega_{\mathrm{OSC}} = \omega_{\mathrm{REF}} \implies \omega_{\mathrm{fr}} + (\mathrm{V_{OUT}} - \mathrm{V_{REF}})\,\mathrm{K_{VCO}} = \omega_{\mathrm{REF}} \tag{2.4}$$

$$\mathrm{V_{OUT}} = \frac{(\omega_{\mathrm{REF}} - \omega_{\mathrm{fr}})}{\mathrm{K_{VCO}}} + \mathrm{V_{REF}} = \frac{\Delta\omega}{\mathrm{K_{VCO}}} + \mathrm{V_{REF}} \tag{2.5}$$

where ω_{fr} denotes the free running frequency of VCO and $\Delta\omega = \omega_{\mathrm{REF}} - \omega_{\mathrm{fr}}$. From Eq. (2.5), if $\Delta\omega = 0$ then $\mathrm{V_{OUT}} = \mathrm{V_{REF}}$, as desired. Under this condition, because $\mathrm{V_{OUT}} = \mathrm{DV_{IN}}$, duty ratio D (which is a function of the phase difference between ω_{REF} and ω_{OSC}). is forced to be equal to $\dfrac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}}$ and $\mathrm{V_{PWM}}$ becomes a PWM signal at switching frequency, $\mathrm{F_{SW}} = \omega_{\mathrm{REF}}/2\pi$. Note that if $\Delta\omega \neq 0$, then $\mathrm{V_{OUT}}$ settles with an offset voltage equal to $\dfrac{\Delta\omega}{\mathrm{K_{VCO}}}$. In practice, it is difficult to achieve $\omega_{\mathrm{fr}} = \omega_{\mathrm{REF}}$ (or $\Delta\omega = 0$) under all process, voltage, and temperature conditions. As a result, $\Delta\omega \neq 0$ and output regulation accuracy is inevitably compromised.

To minimize output voltage inaccuracy caused by $\Delta\omega \neq 0$, we propose to use a replica VCO to generate the reference clock as shown in Fig. 2.8. Assuming the two VCOs are

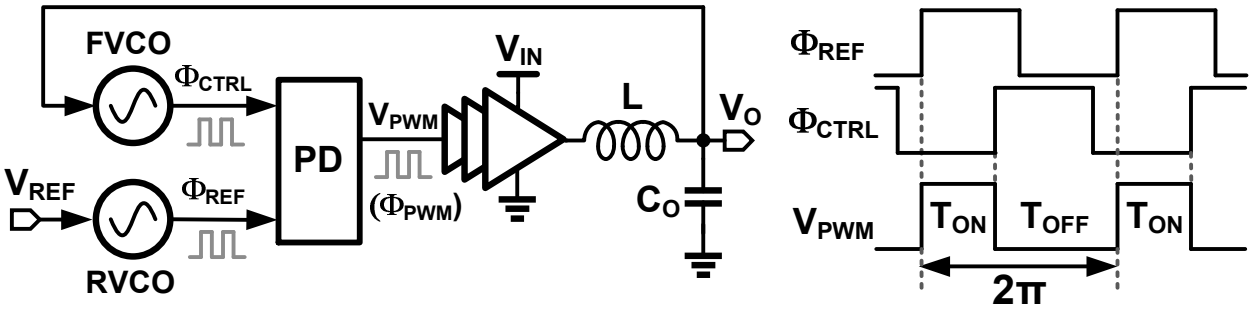


Figure 2.8: An external reference clock-less time-based type-I buck converter.

matched and have same K_{VCO}, their phase outputs can be represented as:

$$\Phi_{CTRL}(t) = \int_0^t \omega_{FVCO}(\tau)d\tau = K_{VCO}\int_0^t V_{OUT}d\tau \tag{2.6}$$

and

$$\Phi_{REF}(t) = \int_0^t \omega_{RVCO}(\tau)d\tau = K_{VCO}\int_0^t V_{REF}d\tau \tag{2.7}$$

where ω_{FVCO} and ω_{RVCO} are the frequencies of FVCO and RVCO, respectively. The output of the phase detector is given by:

$$\Phi_{PWM}(t) = \Phi_{REF}(t) - \Phi_{CTRL}(t) = K_{VCO}\int_0^t (V_{REF}(\tau) - V_O(\tau))d\tau \tag{2.8}$$

Equation (2.8) indicates that any error voltage between V_{REF} and V_O is integrated just like any other integrator, but its output is in terms of phase instead of voltage. Upon closing the converter loop around the integrator, feedback action forces the phase difference between Φ_{REF} and Φ_{CTRL} such that the two VCOs are frequency locked, which is only possible if $V_{REF} = V_O$. This phase difference, Φ_{PWM}, when translated into time-domain, is equal to the ON time of the PWM signal, V_{PWM}, and is given by:

$$T_{ON} = \left(\frac{\Phi_{PWM}}{2\pi}\right)(T_{ON} + T_{OFF}) \tag{2.9}$$

implying that the duty-cycle, $D = \dfrac{T_{ON}}{T_{ON} + T_{OFF}}$ will be

$$D = \frac{\Phi_{PWM}}{2\pi} = \frac{V_O}{V_{IN}} \tag{2.10}$$

Note that the relationship between the phase and duty-cycle is perfectly linear and the V_{PWM} signal is generated without using an explicit pulse width modulator. The steady-state phase domain block diagram of the type-I buck converter is shown in Fig. 2.9. The transfer functions of the VCO-based integral compensator and LC filter (from duty-cycle input to output voltage V_O) are represented by $H_{\Phi I}(s)$ and $H_{LC}(s)$, respectively. The phase detector is represented by its gain, K_{PD}, which is equal to $1/2\pi$ [1/rad] for an SR-latch-based

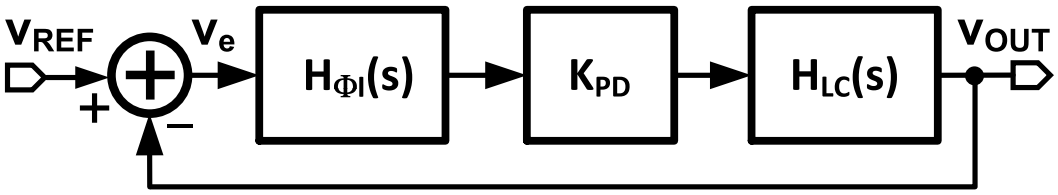


Figure 2.9: Steady-state phase domain block diagram of the time-based type-I buck converter.

PD. Loop gain, LG(s), of the type-I converter is equal to:

$$\mathrm{LG(s)} = \mathrm{H_{\Phi I}(s)} \cdot \mathrm{K_{PD}} \cdot \mathrm{H_{LC}(s)} \tag{2.11}$$

Stability can be guaranteed by making loop gain crossover frequency, ω_{ugf}, to be much smaller than the real part of complex conjugate poles of $\mathrm{H_{LC}(s)}$ in which case $\omega_{\mathrm{ugf}} = \mathrm{K_{VCO}} \cdot \mathrm{K_{PD}}$. Having introduced the concept of time-based control in the context of a simple type-I buck converter, we now extend these ideas to the implementation of a PID compensator.

2.3 Time-Based PID Compensator

We derive the topology and requirements of a time-based PID compensator from its voltage-mode counterpart shown in Fig. 2.1. The transfer function of a voltage-mode PID compensator is given by [23]:

$$\mathrm{H_{PID}(s)} = \frac{v_{\mathrm{ctrl}}(\mathrm{s})}{v_{\mathrm{o}}(\mathrm{s})} = \mathrm{K}\frac{\left(1+\frac{\omega_{\mathrm{z1}}}{\mathrm{s}}\right)\left(1+\frac{\mathrm{s}}{\omega_{\mathrm{z2}}}\right)}{\left(1+\frac{\mathrm{s}}{\omega_{\mathrm{p1}}}\right)\left(1+\frac{\mathrm{s}}{\omega_{\mathrm{p2}}}\right)} \tag{2.12}$$

if we neglect the two high-frequency poles $(\omega_{\mathrm{p1}}, \omega_{\mathrm{p2}})$ in the denominator which are located above the crossover frequency, the equation can be simplified to:

$$\mathrm{H_{PID}(s)} = \mathrm{K}\left(1+\frac{\omega_{\mathrm{z1}}}{\omega_{\mathrm{z2}}}\right) + \frac{\mathrm{K}\omega_{\mathrm{z1}}}{\mathrm{s}} + \frac{\mathrm{K}}{\omega_{\mathrm{z2}}}\mathrm{s} \tag{2.13}$$

where K is equal to $\frac{1}{G_{ugf}}\sqrt{\frac{\omega_{z2}}{\omega_{p1}}}$ and G_{ugf} is the gain of $H_{LC}(s)$ at the crossover frequency. By comparing them to Eq. (2.13) to a canonical PID transfer function, $H_{PID}(s) = K_P + \frac{K_I}{s} + K_D s$, we obtain the proportional, integral and derivative gains, K_P, K_I and K_D, respectively, to be:

$$K_P = K\left(1 + \frac{\omega_{z1}}{\omega_{z2}}\right); \quad K_I = K\omega_{z1}; \quad K_D = \frac{K}{\omega_{z2}} \tag{2.14}$$

Hence, time-based equivalent of the transfer function in Eq. (2.12) can be implemented by using four time-based building blocks: (1) voltage-to-time converter with controllable gain to realize proportional control, (2) an integrator, (3) a differentiator, and (4) a summing block for adding all the individual control parts. Note that the two high-frequency poles (ω_{p1}, ω_{p2}) in Eq. (2.12) which are required to suppress the gain above the crossover frequency [23] will be discussed later in this section. Voltage-to-time conversion can be implemented with a

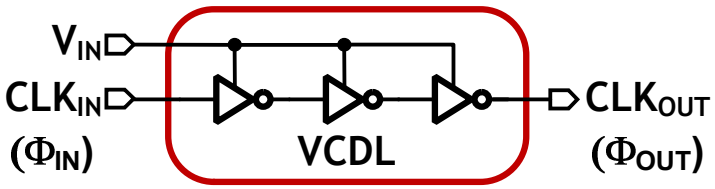


Figure 2.10: Schematic of a VCDL used as time-based proportional control.

voltage controlled delay line (VCDL) as shown in Fig. 2.10. A VCDL, implemented using a chain of tunable delay cells, shifts the phase of input clock, Φ_{IN}, in proportion to the input voltage, V_{IN} with a gain of K_{VCDL}, measured in units of rad/V. The output phase, Φ_{OUT}, of the VCDL can be mathematically expressed as:

$$\Phi_{OUT} = \Phi_{IN} + K_{VCDL} \cdot V_{IN} \tag{2.15}$$

This illustrates that VCDL performs a summing function in addition to the voltage-to-time conversion, making it suitable for implementing time-based proportional control. The input voltage to output phase transfer function of the VCDL (when Φ_{IN} is held constant), $H_{\Phi P}(s)$, is equal to:

$$H_{\Phi P}(s) = \frac{\Phi_{OUT}(s)}{v_{IN}(s)} = K_{VCDL} \tag{2.16}$$

A true time-based differentiator is difficult to implement. Hence, it is implemented using

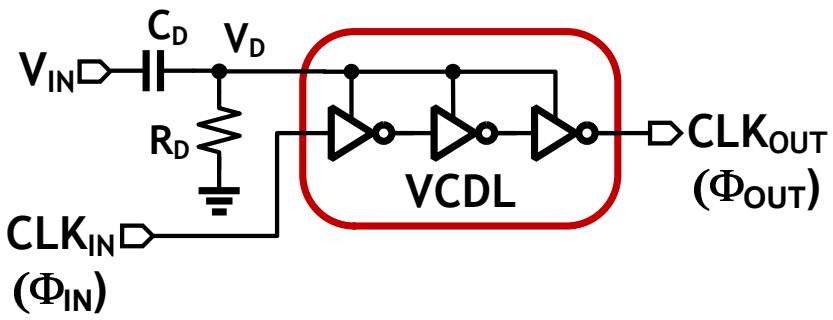


Figure 2.11: Implementation of a time-based differentiator using a cascade of high-pass RC filter and a VCDL.

a voltage/time hybrid approach wherein input voltage, v_{IN}, is passed through a first-order high-pass RC filter before feeding it to the VCDL (see Fig. 2.11). The high-pass filter implements the differentiator function while the VCDL performs voltage-to-time conversion. The transfer function of the filter is given by:

$$\frac{v_{\mathrm{D}}(\mathrm{s})}{v_{\mathrm{IN}}(\mathrm{s})} = \frac{\mathrm{R_D C_D s}}{1 + \mathrm{R_D C_D s}} \approx \mathrm{R_D C_D s} \quad \text{if} \quad \mathrm{R_D C_D} \ll 1 \tag{2.17}$$

Combining this equation with Eq. (2.16), leads to the time-based differentiator transfer function, $\mathrm{H_{\Phi D}(s)}$, equal to:

$$\mathrm{H_{\Phi D}(s)} = \frac{\Phi_{\mathrm{OUT}}(\mathrm{s})}{v_{\mathrm{IN}}(\mathrm{s})} = \mathrm{R_D C_D K_{VCDL} s} \tag{2.18}$$

The three building blocks, namely, the VCDL, VCO, and differentiator can be combined

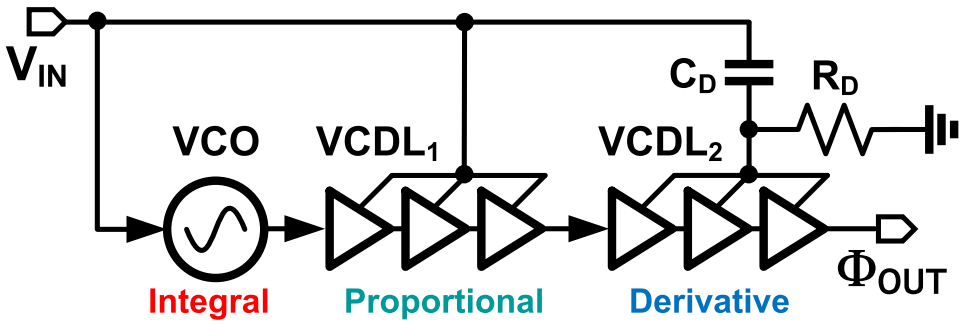


Figure 2.12: Block diagram of a time-based PID compensator.

as shown in Fig. 2.12, to implement the time-based PID compensator. Notably, delays (or equivalently phases) are added when they are cascaded. Therefore, the summation

of integral, proportional and differentiator transfer functions is achieved inherently in the proposed compensator. The voltage to phase transfer function of the compensator, $H_{\Phi PID}(s)$, is equal to:

$$\frac{\Phi_{OUT}(s)}{v_{IN}(s)} = H_{\Phi PID}(s) = K_{VCDL1} + \frac{K_{VCO}}{s} + K_{VCDL2}R_D C_D s \tag{2.19}$$

The coefficients of the time-based PID compensator can be determined by comparing with K_P, K_I and K_D of the voltage domain PID compensator (see Eq. (2.14)), and the results are:

$$K_{VCO} = K\omega_{z1}; \quad K_{VCDL1} = K\left(1 + \frac{\omega_{z1}}{\omega_{z2}}\right); \quad K_{VCDL2}R_D C_D = \frac{K}{\omega_{z2}} \tag{2.20}$$

Note that the coefficient values found in Eq. (2.20) need to be scaled according to the gain difference between the PWM modulator in the voltage domain controller and phase detector in the time-based controller. The two high-frequency poles, $\omega_{p1}$and ω_{p2}, in Eq. (2.12) are provided inherently by the intrinsic pole in a VCDL (thereby designing the BW of VCDL accordingly) and the pole due to the high-pass filter of the differentiator as shown in Eq. (2.17), respectively. Considering the target specifications of the prototype buck

Table 2.1: Prototype buck converter target specifications.

V_{IN}	V_{OUT}	F_{SW}	L	C	BW	Φ_M
1.8V	0.6-1.5V	10MHz	220nH	4.7μF	$\approx$ 1MHz	60°

Table 2.2: Prototype PID compensator parameters.

K	ω_{z1}	ω_{z2}	ω_p
10.6	$2\pi \cdot 80$krad/s	$2\pi \cdot 268$krad/s	$2\pi \cdot 3.73$Mrad/s

converter shown in Table 2.1, the PID compensator parameters can be calculated following the procedure outlined in [23] and the results are tabulated in Table 2.2. Using Table 2.2 and Eq. (2.20), the time-based PID compensator parameters are calculated to be the following:

$$\begin{aligned} &K_{VCO} = 19.2\text{Mrad/s}; \quad K_{VCDL1} = 49.6\text{rad/V}; \quad K_{VCDL2} = 567\text{rad/V} \\ &C_D = 2\text{pF}, \text{ assuming } R_D = 20\text{k}\Omega \end{aligned} \tag{2.21}$$

At $F_{SW} = 10MHz$, $K_{VCDL1} = 49.6rad/V$ is equivalent to $\frac{K_{VCDL1}}{2\pi F_{SW}} = 789ns/V$ and $K_{VCDL2} = 567rad/V$ is equivalent to $\frac{K_{VCDL2}}{2\pi F_{SW}} = 9.02\mu s/V$. The loop gain and phase responses of the converter with the above parameters for varying output voltages are shown in Fig. 2.13. The phase margin is around 60° at nominal output voltage of 1V and is always greater than 45° across an output voltage range of 0.6-1.4V even in the presence PVT variations. In this design, the opposite sensitivity of K_{VCO} and K_{VCDL} also helps to to partially compensate for some of the loop dynamics variation. This is because $K_{VCO} \propto \mu(V_{CTRL} - V_t)$ whereas $K_{VCDL} \propto (\mu(V_{CTRL} - V_t))^{-1}$ for inverter-based VCO/VCDL implementation [22]. The mobility and the threshold voltage of MOS devices are denoted by μ and V_t, respectively. V_{CTRL} denotes the input control voltage.

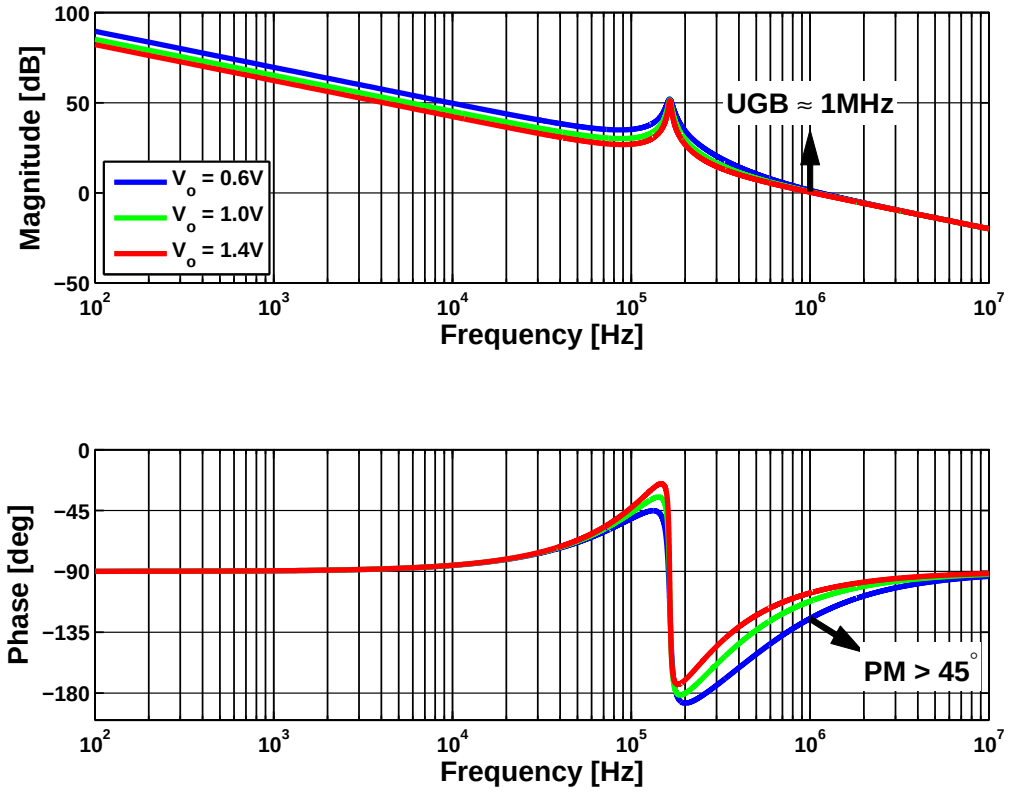


Figure 2.13: Loop gain magnitude and phase response of PID buck converter at $V_O = 0.6V$, 1.0V and 1.4V.

2.4 Time-Based PID Buck Converter

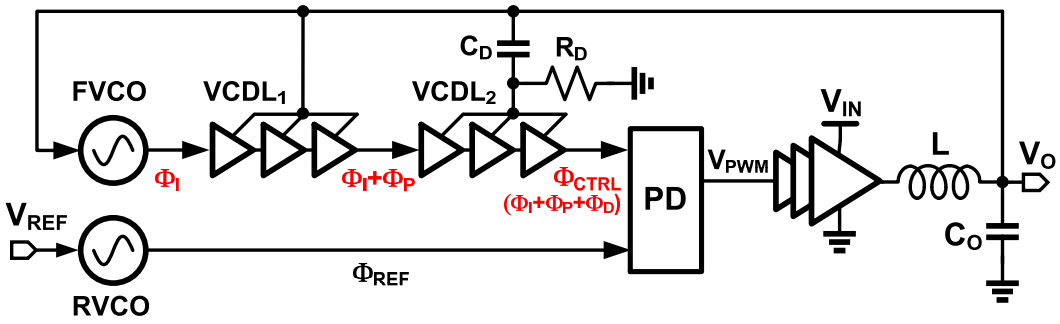


Figure 2.14: Block diagram of the proposed time-based PID buck converter.

A simplified block diagram of a PID buck converter employing a time-based compensator is shown in Fig. 2.14. As in the case of a type-I converter described previously in Section 2.2, RVCO generates the reference clock, compensator outputs a phase control signal, Φ_{CTRL} and the phase detector generates a PWM signal by comparing Φ_{CTRL} with reference phase, Φ_{REF}. RVCO must be designed such that its free-running frequency is equal to the desired converter switching frequency, F_{SW}, when the output voltage, V_O, is equal to the desired voltage, V_{REF}. Under this condition, the negative feedback loop locks the frequency of feedback VCO (FVCO) to that of RVCO, thereby regulating V_O to be equal to V_{REF}. Note that, because VCO acts as an integrator, $F_{FVCO} = F_{RVCO}$ guarantees $V_O = V_{REF}$, independent of the phase difference between the two VCO outputs. As a result, V_O, can be regulated to be equal to V_{REF} by varying the phase difference, or equivalently the duty-cycle without altering the condition $F_{FVCO} = F_{RVCO}$. However, a drawback of this approach is that F_{SW} becomes a function of the output voltage, which is undesirable in many applications. We propose to use a differential architecture as shown in Fig. 2.15, to decouple F_{SW} from the output voltage. In other words, F_{SW} is held constant, independent of the reference and output voltages as explained next. The three differential transconductors, G_{mI}, G_{mP}, and G_{mD}, convert the voltage difference between V_{FB} (or V_D) and V_{REF} into output currents, i_I, i_P, and i_D, which are used to implement integral, proportional, and differential control, respectively. Current-controlled ring oscillators (CCOs), RCCO and FCCO, are used as active loads in transconductor G_{mI}. The tail current of G_{mI} (i_I) is adjusted such that the

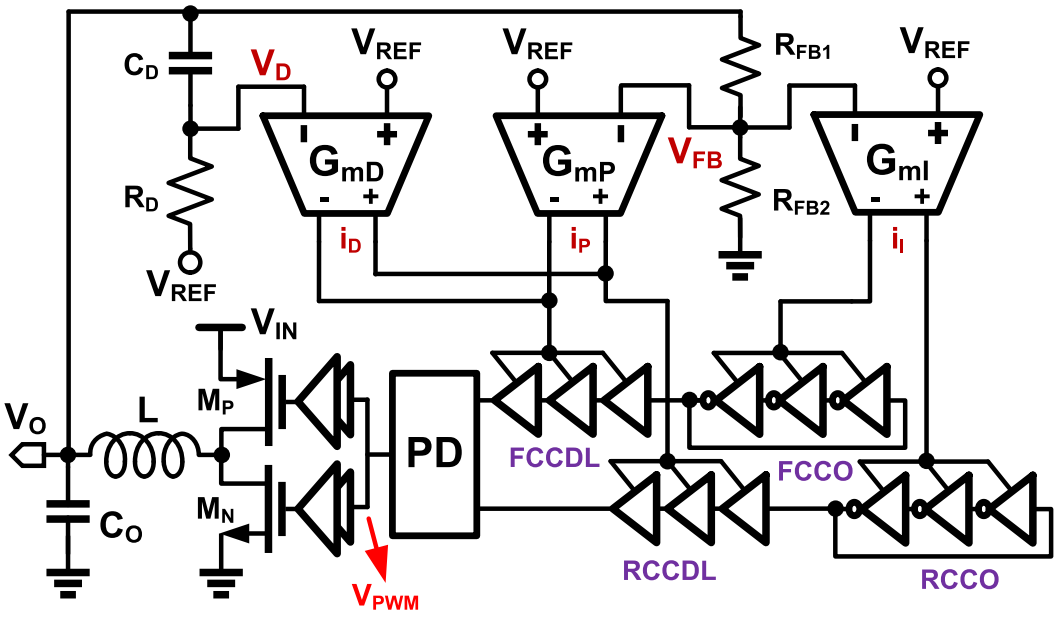


Figure 2.15: Differential implementation of the proposed time-based PID buck converter.

free-running frequency of RCCO and FCCO is equal to the desired switching frequency when input differential voltage is equal to zero, i.e, when $V_{FB} = V_{REF}$. Hence, F_{SW} is nominally constant across the entire output voltage range. Proportional and derivative control paths are implemented using differential transconductors (G_{mP} and G_{mD}) loaded with current-controlled delay lines (CCDLs). By summing the proportional and derivative controls in current domain, simply by shorting the outputs of G_{mP} and G_{mD}, one delay line is eliminated. This not only helps to reduce power consumption but more importantly lowers loop delay and improves the phase margin. The differential implementation also helps to bias the CCDL in the middle of its range when $V_{FB} = V_{REF}$, so that the useful linear range of the CCDL is maximized. This prevents saturation of the CCDL for both positive and negative load/line transients, which improves the converter's transient response. A side benefit of using a differential CCDL output is that it automatically results in dual edge pulse width modulation at the PD output, which has been shown to provide 2x faster response compared to single edge modulation [24].

2.5 Building Blocks

2.5.1 VCO

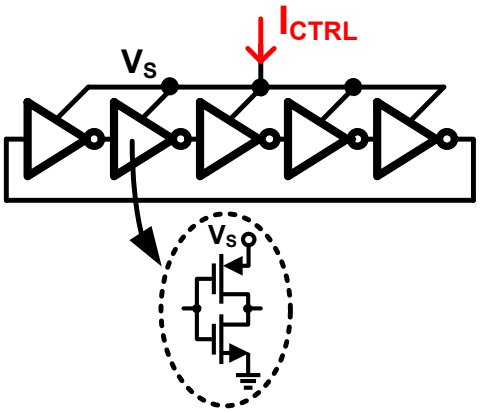


Figure 2.16: Schematic of current controlled oscillator.

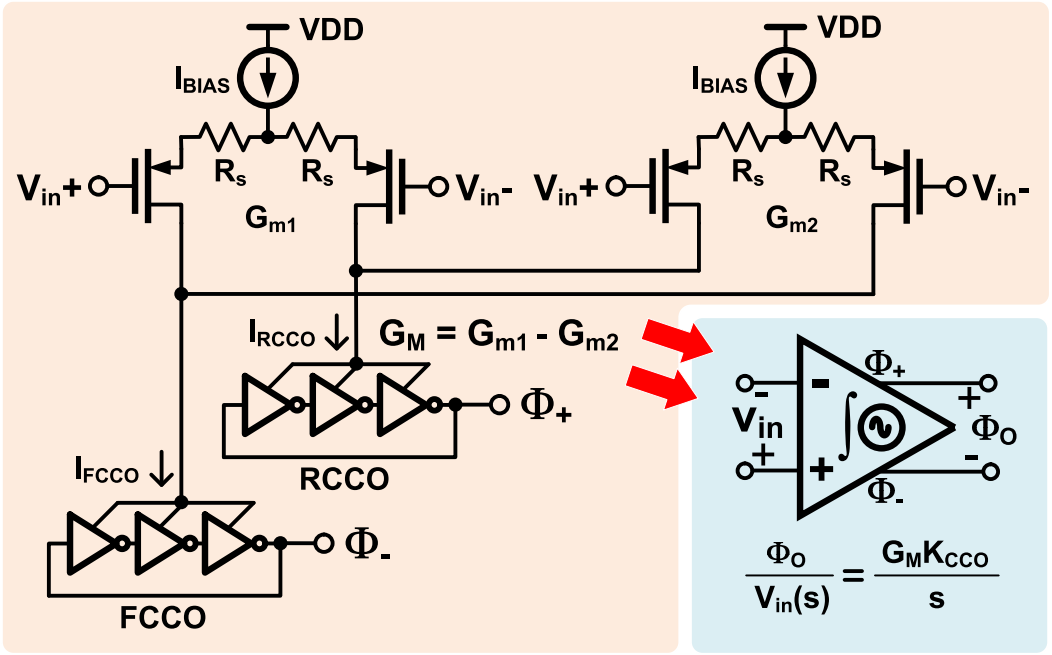


Figure 2.17: Schematic of low gain VCO.

The schematic of the CCO is shown in Fig. 2.16. It is composed of five single-ended CMOS inverter-based delay stages, whose delay is tuned by varying the supply current, I_{CTRL}. The simulated tuning range of the CCO designed in a standard 180nm CMOS process is 10-30 MHz when I_{CTRL} is varied from 4-10 μA and the CCO gain, K_{CCO}, is approximately

4.6MHz/μA at an oscillation frequency of 10MHz. A VCO can be constructed from a CCO by converting input voltage to current by using a transconductor and feeding its output current into the CCO as shown in Fig. 2.17. This results in a VCO gain of:

$$K_{VCO} = G_M K_{CCO} \tag{2.22}$$

where G_M is the gain of the trasnconductor and it is equal to the transconductance of the transconductor G_{mI} in Fig. 2.15. To achieve a 1MHz tracking bandwidth at a converter switching frequency of 10MHz, the needed K_{VCO} was calculated to be about 844KHz/V. From Eq. (2.22) and simulated K_{CCO} = 4.6MHz/μA, G_M should be equal to 0.18μA/V. Assuming an overdrive voltage of 200mV, the bias current needs to be as low as 18nA to achieve the desired G_M. To avoid such low bias currents, two G_M reduction techniques were employed in the proposed VCO. First, resistor degeneration is used to reduce G_M to 4μA/V. Second, weak positive feedback has been implemented using a second differential pair to reduce the effective $G_M = G_{m1} - G_{m2}$ further to about 0.18μA/V.

2.5.2 VCDL

A voltage controlled delay line implemented as a combination of transconductor and CCDL is used for proportional and derivative (PD) control. As shown in Fig. 2.15, two separate transconductors, G_{mP} and G_{mD}, are used to vary the supply current and consequently the delay of CCDLs. The input of G_{mD} is fed with the high-pass filtered V_O to achieve derivative control whereas G_{mP} is used to achieve proportional control. The CCDLs are implemented using a 10-stage cascade of CMOS inverters.

2.5.3 Phase Detector

The phase detector is simply an RS latch with pulse generators at its inputs as shown in Fig. 2.18. The pulse generators generate narrow pulses on every positive edge transition of their inputs, resulting in RS flip-flop-like behavior for the phase detector. The duty-cycle of the pulse width modulated signal, V_{PWM}, is set at every positive edge of the reference

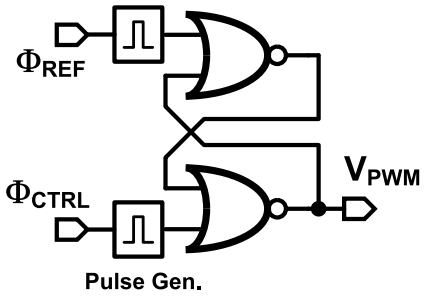


Figure 2.18: Block diagram of phase detector (PD).

phase, Φ_{REF}, and reset at every positive edge of the control phase, Φ_{CTRL}. Consequently, the duty-cycle of V_{PWM} waveform is proportional to the difference of two control phases. As mentioned before, this implementation of the phase detector avoids use of an explicit PWM as the output of the phase detector is a digital waveform with CMOS levels carrying the necessary duty-cycle information provided by control input phases.

2.6 Experimental Results

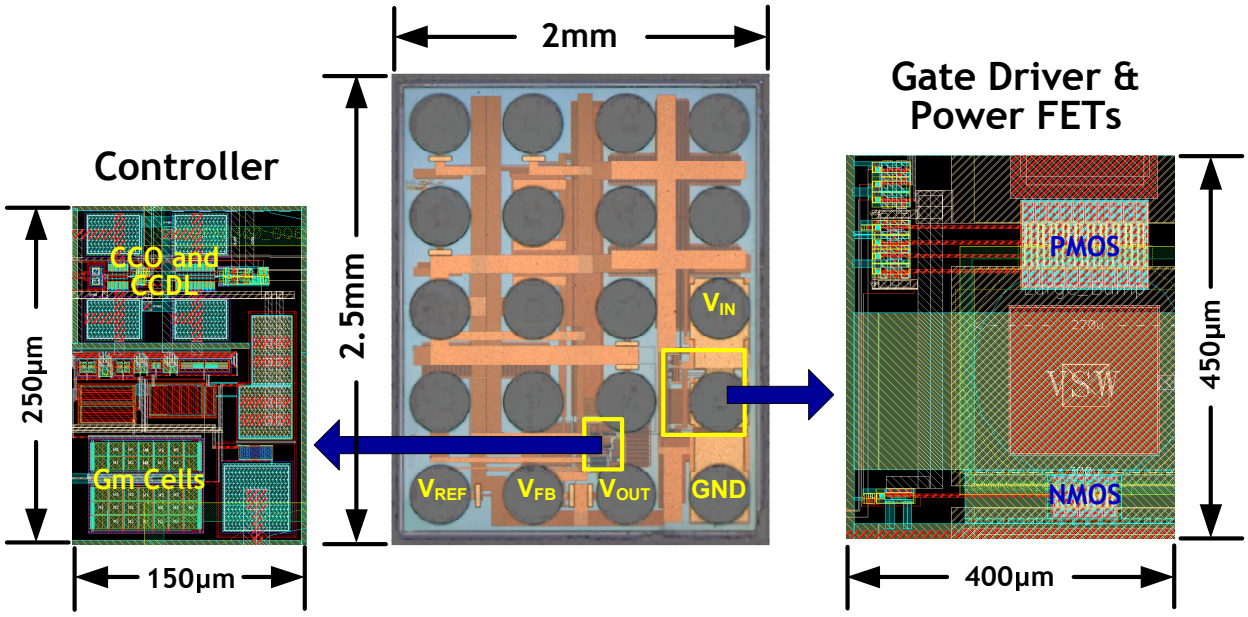


Figure 2.19: Die photograph and layouts of controller and driver.

The proposed buck converter was implemented in 180nm CMOS process and the die photo is shown in Fig. 2.19. The total die area is bump-limited and is equal to $5\mathrm{mm}^2$. The

active die area is 0.24mm^2 of which the controller occupies only 0.0375mm^2. Power supply decoupling capacitors are placed between the bumps, which occupy an additional active area of about 0.7mm^2. Operating with an input voltage of 1.8V, L = 220nH (Q $\approx$ 60 at 10MHz, air core inductor), and C_O = 4.7μF (ceramic, 0603, X7R), the converter regulates its output to any desired voltage in the range of 0.6V to 1.5V. Measured output spectra of the two oscillators (RCCO and FCCO in Fig. 2.15) in free-running and closed-loop modes are shown in Fig. 2.20. As expected, the spectra of free-running oscillator outputs do not show a clear spectral peak due to the poor frequency stability of ring oscillators. However, when the feedback loop is closed, the PID control loop locks the two oscillators to the mean of their free-running frequencies as indicated by clear spectral peaks in their outputs (see Fig. 2.20). This frequency locking behavior proves that the feedback voltage (V_{FB}) is stable and equals the reference voltage (V_{REF}) as desired. Steady-state waveforms of the

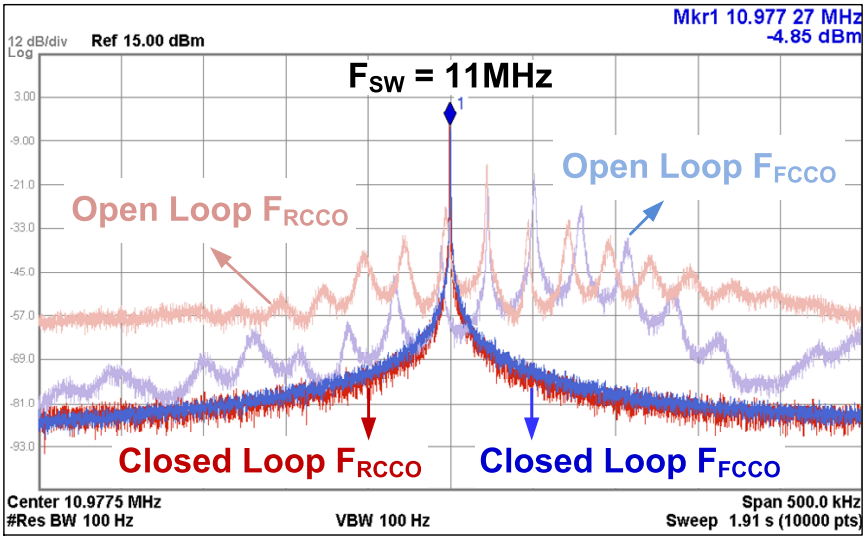


Figure 2.20: Measured output voltage spectra of two CCOs.

two oscillator outputs (V_{RCCO}, V_{FCCO}), PWM signal (V_{PWM}), and the output voltage are shown in Fig. 2.21. The duty-cycle of V_{PWM} generated from V_{RCCO} and V_{FCCO} by the PD is constant and is equal to about 58% when V_O is regulated to 1V with V_{IN} = 1.8V and load current, I_{LOAD}=200mA. This indicates that the control loop also phase locks the two oscillators with a static phase offset needed to regulate the output voltage to the desired level. The transient response of the converter measured under different load current step conditions is shown in Fig. 2.22. Zoomed-in waveforms are depicted in Figs. 2.23 and 2.24.

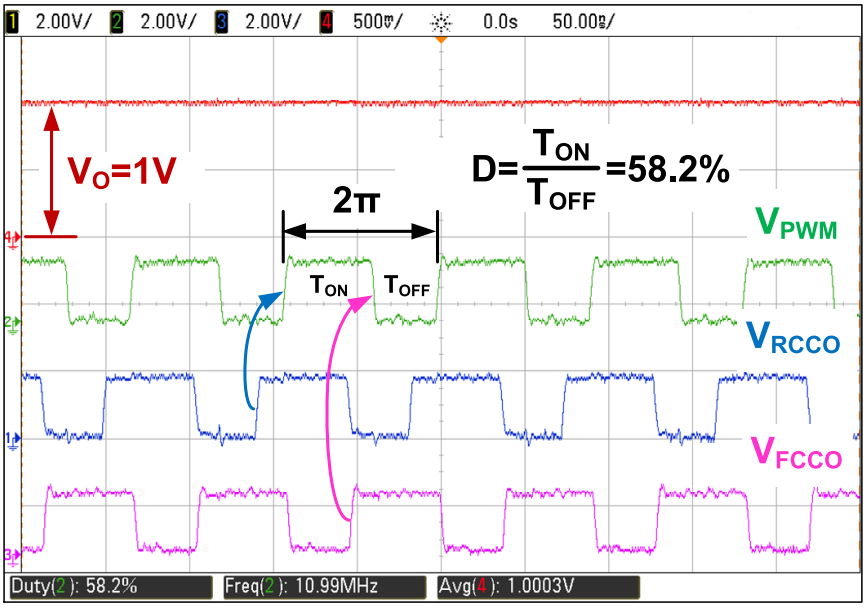


Figure 2.21: Measured steady-state waveforms.

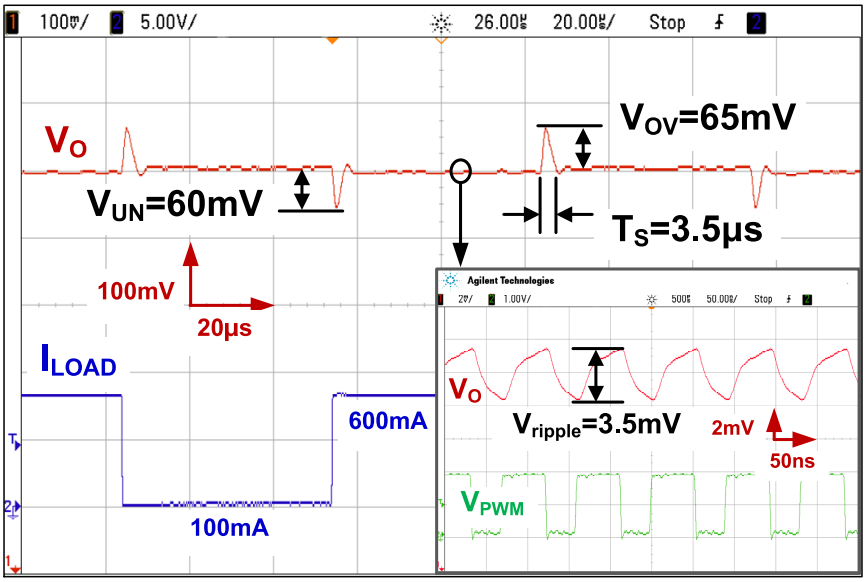


Figure 2.22: Measured transient response.

The measured undershoot/overshoot is 60mV/65mV and the settling time is less than 3.5μs. Steady-state output ripple voltage is about 3.5mV as illustrated in the inset of Fig. 2.22. The initial start-up transient shown in Fig. 2.25 indicates a start-up time of 17.5μs. Measured efficiency of the converter at V_O=1V is plotted as a function of load current for different F_{SW} in the range of 11MHz to 25MHz in Fig. 2.26. Peak efficiency of 94% is achieved at F_{SW}=11MHz with about 100mA output current. For load currents ranging from 20-600 mA,

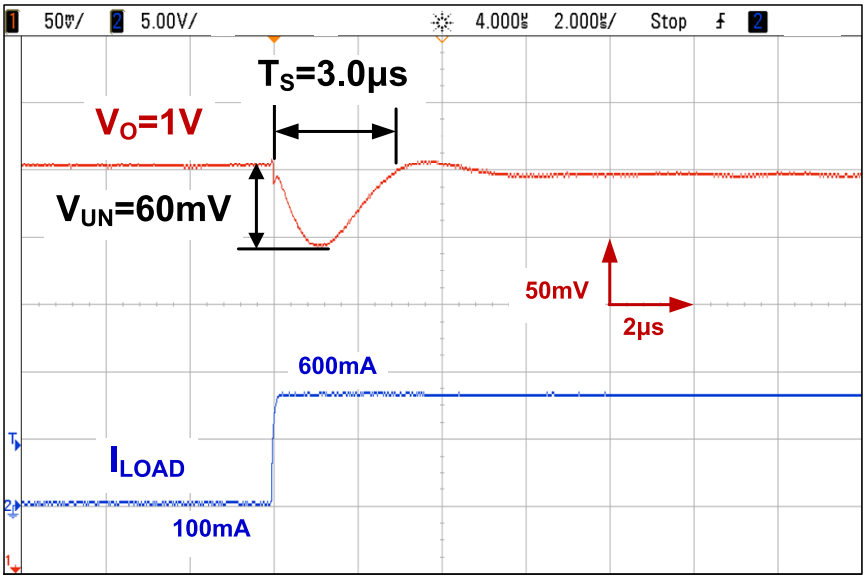


Figure 2.23: Zoomed-in transient response for 100mA to 600mA load step.

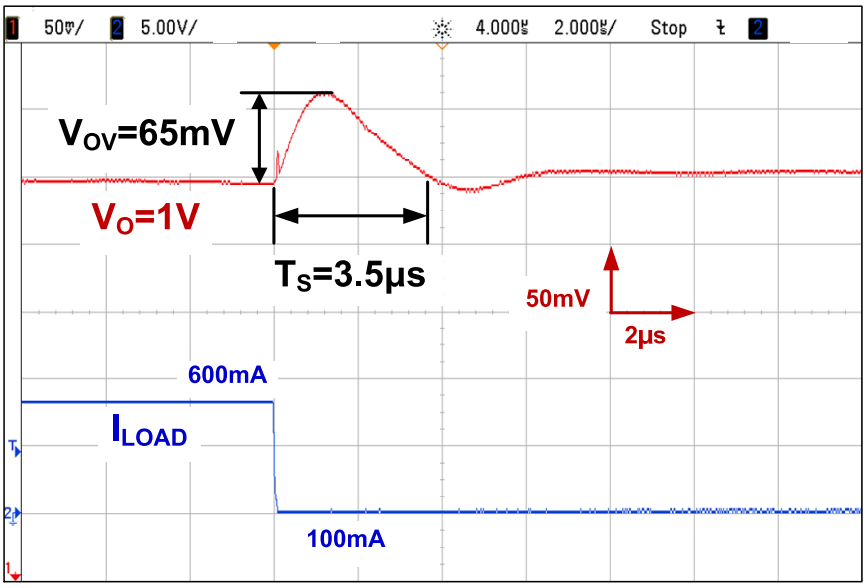


Figure 2.24: Zoomed-in transient response for 600mA to 100mA load step.

efficiency is higher than 78% across all switching frequencies. This illustrates the time-based controller's ability to operate across a wide range of switching frequencies. Efficiency plots at V_O=0.6V and V_O = 1.4V, also shown in Fig. 2.26, illustrate the proposed converter's ability to simultaneously operate at high F_{SW} and regulate V_O across a wide range of voltages.

The reference tracking ability of the converter is quantified by measuring the bandwidth of reference voltage to output voltage transfer function, $H_{REF}(s)$ for V_O = 1V. To this end, the

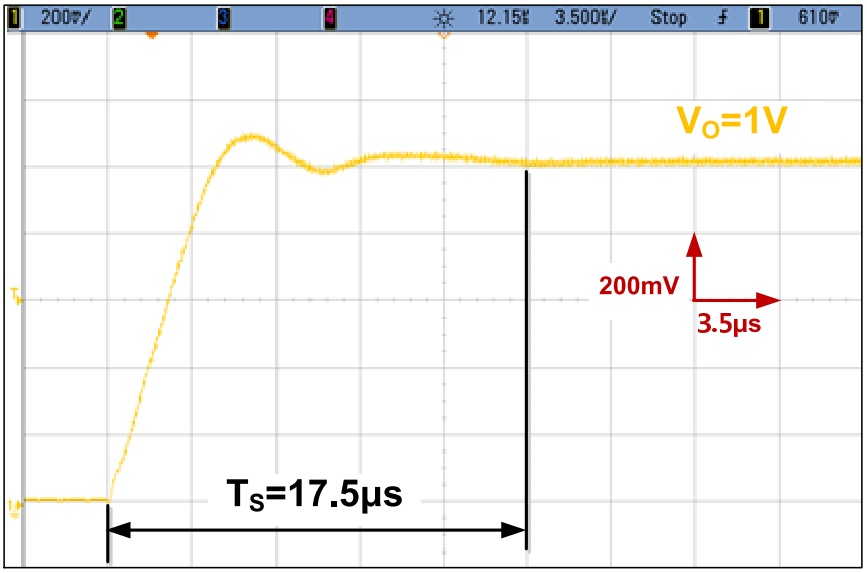


Figure 2.25: Measured initial start-up transient response.

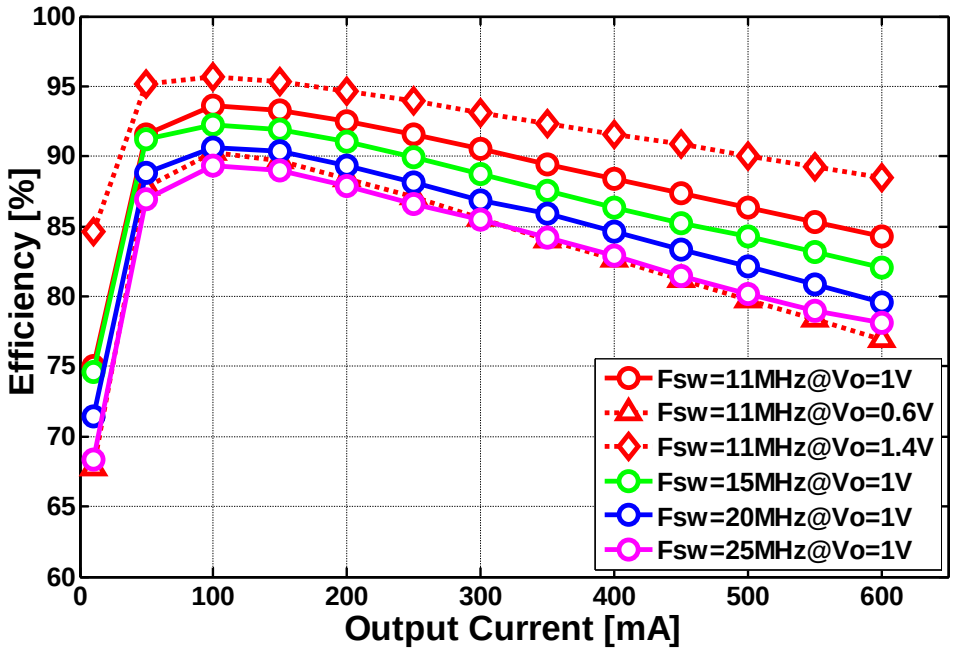


Figure 2.26: Measured efficiency as a function of switching frequency.

magnitude response of $H_{REF}(s)$ is measured by applying a sinusoidal tone on the reference voltage and measuring converter's response to it at the output. By sweeping the frequency of sinusoidal tone, the complete magnitude response is obtained and is plotted in Fig. 2.27. The -3dB bandwidth is approximately 1MHz, which is about $1/10^{th}$ of the switching frequency. Hence, time-based control can also achieve a very high reference tracking bandwidth.

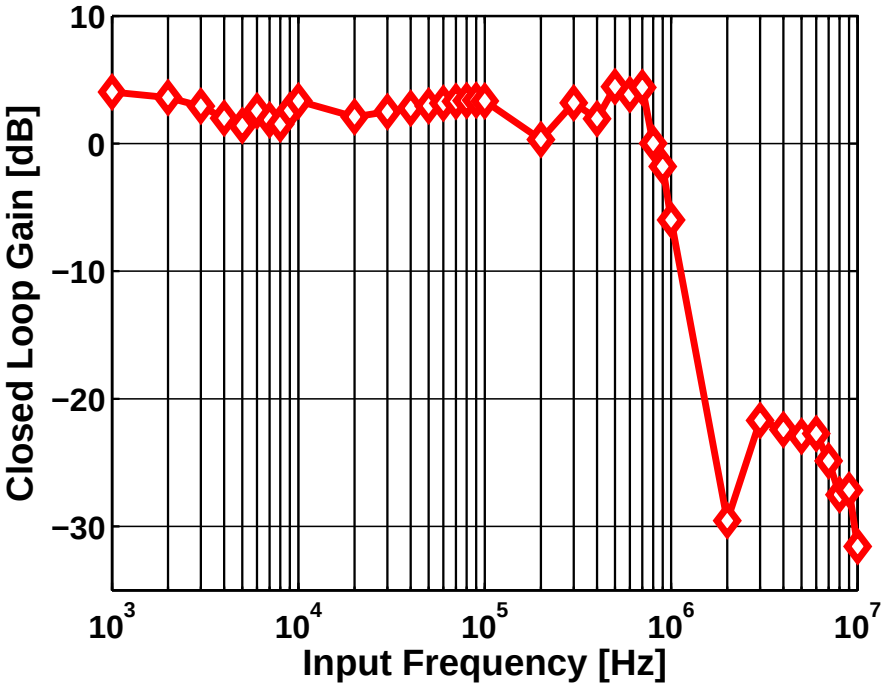


Figure 2.27: Measured magnitude response of $H_{REF}(s)$ as a function of frequency.

The measured quiescent current at $F_{SW} = 11$MHz is 23μA, which translates to a current efficiency of about 2μA/MHz. The VCOs and the VCDLs together consume about 52% of the current while other intermediate blocks (logic buffers and phase detector) consume 48%. The low quiescent current makes time-based control very attractive for low-power applications and in systems that spend the vast majority of their time in the idle state. A performance summary and comparison of the buck converter using proposed time-based control techniques with the state-of-the-art buck converters are shown in Table 2.3.

Table 2.3: Performance of the proposed buck converter and its comparison with the state-of-the-art.

Publication	This Work	[25] ISSCC '14	[26] ISSCC '10
Control Loop	Time-based PID	Voltage mode PID	Digital PID
Process	180nm CMOS	130nm CMOS	180nm CMOS
Supply Voltage [V]	1.8	3.3	3.3
Output Voltage [V]	0.6-1.5	0.45-2.4	1.8
F_{SW} [MHz]	11-25	10	0.5
L [nH]	220	330	1880
C [μF]	4.7	3.3	22
Max. Load Current [A]	0.6	N/A	1
Settling Time [μs]	3.5	4.44	100
Output Ripple [mV]	3.5	N/A	18
Controller Current [μA]	23	N/A	590
Peak Efficiency [%]	94	91.8	94
Area [mm^2]	0.24	N/A	2.25

CHAPTER 3

TIME-BASED MULTI-PHASE BUCK CONVERTER

3.1 Impact of Phase Mismatch on the Efficiency of Multi-Phase Converters

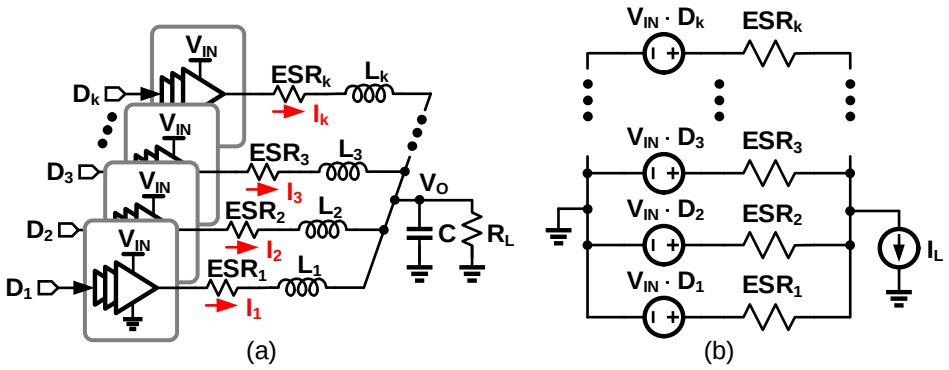


Figure 3.1: (a) Conceptual multi-phase buck converter and (b) its model used for analysis.

An important performance metric of a power converter is efficiency. In addition to conduction and switching losses, mismatch between the power-trains in a multi-phase converter also degrades efficiency. Figure 3.1 (a) shows the basic architecture of a multi-phase converter. As illustrated in Fig. 3.1 (a), there are three possible sources of mismatch, namely duty-cycle mismatch ($D_i \neq D_j$ for $i \neq j$), parasitic series resistance mismatch ($ESR_i \neq ESR_j$ for $i \neq j$) and inductance mismatch ($L_i \neq L_j$ for $i \neq j$). These mismatches cause uneven current distribution among the power-trains and/or degrade converter efficiency. To analyze these effects, consider the k-phase buck converter model shown in Fig. 3.1 (b) [11]. The inductance mismatch only affects AC current and has negligible impact on efficiency. For instance, with 1A of load current, equivalent series resistance (ESR) of 150mohm, an inductance of 30nH and F_{SW} of 30MHz, the efficiency change due to 10%

inductance variation is less than 0.05% including skin-effect of the inductor. Hence inductors are not included in the model. In order to estimate the contribution of duty-cycle mismatch and ESR mismatch separately, we begin by assuming that all the duty-cycles are matched and that only the resistance of i^{th} power-train is different by ΔESR from the resistances of the other power-trains, which are all equal to ESR. Then the current variation, ΔI_i, of i^{th} power-train with respect to the ideal current, I_i, when both the duty-cycles and the ESRs are matched is derived as [11]:

$$\left(\frac{\Delta I_i}{I_i}\right)_{ESR} = -\frac{k-1}{k} \cdot \frac{\Delta ESR}{ESR} \tag{3.1}$$

where ESR includes all the series resistances in the current path of each power-train and is equal to $ESR = R_{SW}+R_L+R_{others}$ and $R_{SW} = D\cdot R_{PMOS}+(1-D)\cdot R_{NMOS}$ is the resistance of switching transistors, R_L is the ESR of the power inductor, and R_{others} represents all other series resistances in the power-train. For a more fair comparison, the sum of the ESRs of all power-trains is kept constant regardless of the mismatch, i.e. $(ESR' + \Delta ESR) + (k - 1) \cdot (ESR' - \Delta ESR/(k - 1)) = k \cdot ESR'$, where ESR' is the average resistance of all power-trains and ΔESR is the resistance mismatch. This also ensures that the output voltage remains constant regardless of the mismatch. The first term, $(ESR' + \Delta ESR)$, represents the resistance of i^{th} power-train and the second term, $(ESR' - \Delta ESR/(k - 1))$, represents resistance of other power-trains. From the converter model shown in Fig. 3.1 (b), the currents of the power-trains are given by:

$$I_{i,\Delta ESR} = \frac{\left(ESR' - \frac{\Delta ESR}{k-1}\right)}{(k-1)(ESR' + \Delta ESR) + \left(ESR' - \frac{\Delta ESR}{k-1}\right)} \cdot I_L \tag{3.2}$$

$$I_{others,\Delta ESR} = \frac{1}{k-1}(I_L - I_i) \tag{3.3}$$

and the conduction loss and the efficiency are given by:

$$P_{loss,\Delta ESR} = I_i^2(ESR' + \Delta ESR) + (k-1)I_{others}^2\left(ESR' - \frac{\Delta ESR}{k-1}\right) \tag{3.4}$$

$$\eta_{\Delta ESR} = \frac{V_O I_O}{V_O I_O + P_{loss,\Delta R}} \tag{3.5}$$

Figure 3.2 (a) shows that with 10% variation of ESR, current in the power-train and converter efficiency vary by 3.6% and 0.014%, respectively.

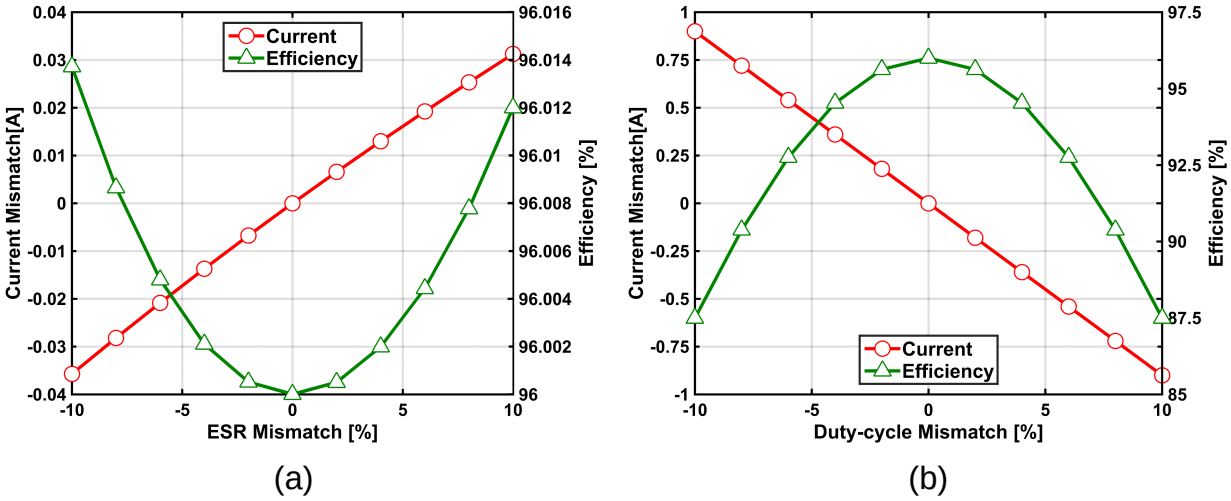


Figure 3.2: (a) Effect of ESR mismatch and, (b) effect of duty-cycle mismatch ($V_{IN} = 1.8V$, $V_O = 0.9V$ and $I_L = 1A$).

Next, assuming that all the ESRs are matched and that only the duty-cycle of the i^{th} power-train is different by ΔD from the other duty-cycles, which are equal to D, then the current variation, ΔI_i, of the i^{th} power-train with respect to the ideal current, I_i, when both the duty-cycles and the ESRs are matched is derived as [11]:

$$\left(\frac{\Delta I_i}{I_i}\right)_D = \frac{k-1}{k} \cdot \frac{V_{IN}\Delta D}{ESR} \tag{3.6}$$

For a more fair comparison, we also assume that the duty-cycle mismatch, ΔD, between the i^{th} power-train and the other power-trains is distributed to maintain the same output voltage. In other words, we can express ΔD_i as:

$$\Delta D_i = -(k-1)\Delta D_{others} \tag{3.7}$$

where $\Delta D = \Delta D_i - \Delta D_{others}$. From the converter model shown in Fig. 3.1 (b), the current

in each of the power-train is given by:

$$I_{i,\Delta D} = \frac{I_L}{k} + \frac{V_{IN}\Delta D_i}{ESR} \tag{3.8}$$

$$I_{others,\Delta D} = \frac{I_L}{k} - \frac{V_{IN}\Delta D_{others}}{ESR} = \frac{1}{k-1}(I_L - I_i) \tag{3.9}$$

and the conduction loss and efficiency are given by:

$$P_{loss,\Delta D} = I_i^2 ESR + (k-1) I_{others}^2 ESR \tag{3.10}$$

$$\eta_{\Delta D} = \frac{V_O I_O}{V_O I_O + P_{loss,\Delta D}} \tag{3.11}$$

Plotting the current mismatch and the efficiency as shown in Fig. 3.2 (b) indicates that with 10% of duty-cycle variation, the current and efficiency vary by 90% and 8.5%, respectively. The main reason behind this large efficiency degradation is the large unbalanced current distribution caused by the duty-cycle mismatch as predicted by Eq. (3.12) [12].

$$\left(\frac{\Delta I_i}{I_i}\right)_D = \frac{k-1}{k} \cdot \frac{1}{1-\eta} \cdot \left(\frac{\Delta D}{D}\right) \tag{3.12}$$

For example, assuming 95% efficiency (η=0.95), Eq. (3.12) shows that the mismatch of the power-train current ($\Delta I_i/I_i$) is amplified by about 20 times with respect to the duty-cycle variation. From the above analysis, we note that significant current mismatch comes mostly from the duty-cycle mismatch rather than ESR or inductance mismatches.

3.2 Tackling Phase Mismatch: Prior Art

There are two approaches to mitigate efficiency degradation caused by duty-cycle mismatch [11]. The first approach is based on matching the duty-cycle in all the phases, also referred to as passive current sharing. The second approach is based on matching the currents in all the phases and this method is also referred to as active current sharing [7]. In passive current sharing, the load current is divided according to the ESRs of power-trains while active current sharing ensures that the load current is split equally among all the power-

trains. As shown in Fig. 3.3, both the approaches offer similar efficiency improvement but implementing them, in practice, is challenging, particularly at high F_{SW} as discussed next.

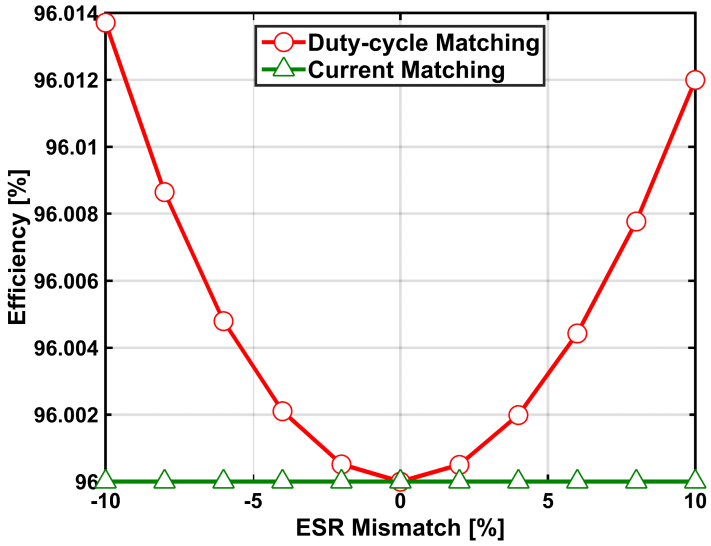


Figure 3.3: Efficiency vs. ESR mismatch with duty-cycle and, current matching.

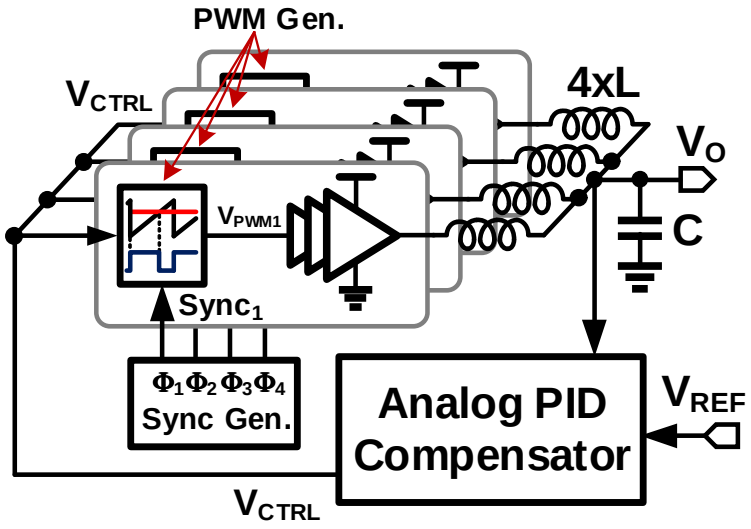


Figure 3.4: Multi-phase buck converter with analog PID compensator.

Consider the classical voltage mode PID multi-phase converter shown in Fig. 3.4. This architecture has many advantageous features such as high efficiency, accurate output voltage regulation, small output voltage ripple and good tracking response. However, a generation of precisely matched duty-cycles at high F_{SW} is difficult due to comparator offsets and

mismatch in ramp slopes. V-to-PWM conversion is performed by comparing the control voltage signal (V_{CTRL}) with a triangular-shaped ramp voltage signal using comparators. All the power-trains share the control voltage while the ramp voltages are generated separately so as to interleave the phases of the power-trains by $2\pi/k$. Figure 3.5 shows the conventional architecture for the PWM generator. Input voltage offset of comparators and mismatch between ramp generators directly appears as duty-cycle mismatch. The mismatches between current sources ($I_{Ri} \neq I_{Rj}$ for $i \neq j$) and ramp capacitors ($C_{Ri} \neq C_{Rj}$ for $i \neq j$) appear as a ramp slope difference and causes duty-cycle mismatch. Current sensing, calibration

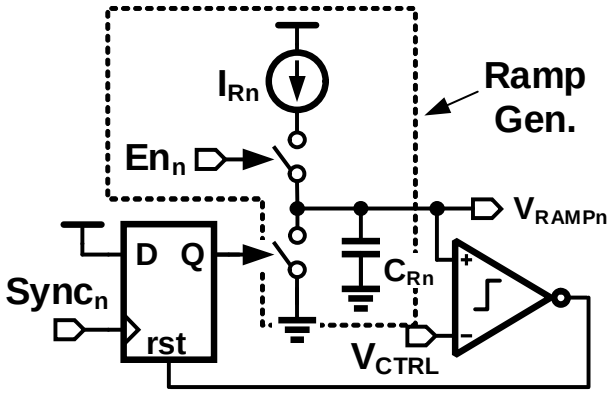


Figure 3.5: Schematic of analog PWM generator.

and feedback circuits are typically employed to make all the power-train currents to be the same, that is to achieve active current sharing [7]. However, even with the added complexity, precisely matched power-train currents are still difficult to achieve due to device mismatches in the current sensing circuit itself. For example, a conventional current sensing circuit based on the matching between the power transistor in the driver and the replica transistor in the current sensor suffers from the mismatch between the two transistors and it directly appears as a current mismatch [27]. As an alternative, precisely matched duty-cycle can be achieved by using digital PWM generator [11, 12]. However, DC-DC converters with high switching frequency and accuracy require high-resolution and high-speed digital PWM, which is power and area hungry to implement. In view of these drawbacks, we propose a high F_{SW} time-based multi-phase controller that achieves high efficiency by implementing passive current sharing in an area and power efficient manner.

3.3 Proposed Multi-Phase Buck Converter with Time-Based Controller

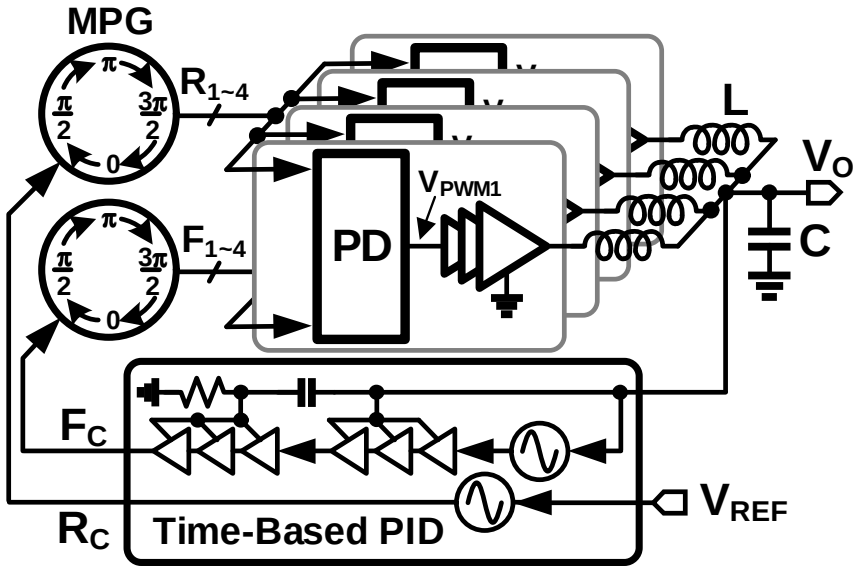


Figure 3.6: Proposed multi-phase buck converter architecture.

A simplified block diagram of the proposed multi-phase buck converter is shown in Fig. 3.6 [18]. It consists of a time-based proportional-integral-derivative (T-PID) compensator, time-based multi-phase generator (MPG) that generates precisely matched duty-cycles, and power switches in each of the phases driven by a switch driver. Though the compensator and MPG are implemented using mostly digital circuits and operate with full CMOS levels, they do not add quantization error. This is because time-based controller building blocks such as the VCO, VCDL, and PD have infinite resolution similar to the building blocks of conventional voltage-mode analog controller. As a result, the buck converter does not exhibit an undesirable limit cycle behavior that plagues digital controllers. Each of the building blocks of the proposed buck converter is described in detail next.

3.3.1 Time-Based PID Compensator (T-PID)

A time-based compensator that combines the good attributes of both analog and digital compensators was recently introduced [28]. It possesses high regulation accuracy and low

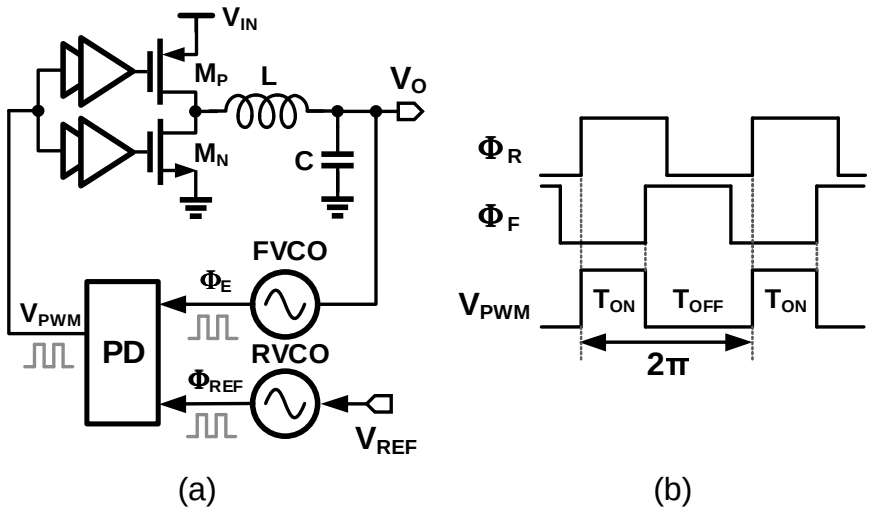


Figure 3.7: Buck converter with time-based Type-I compensator.

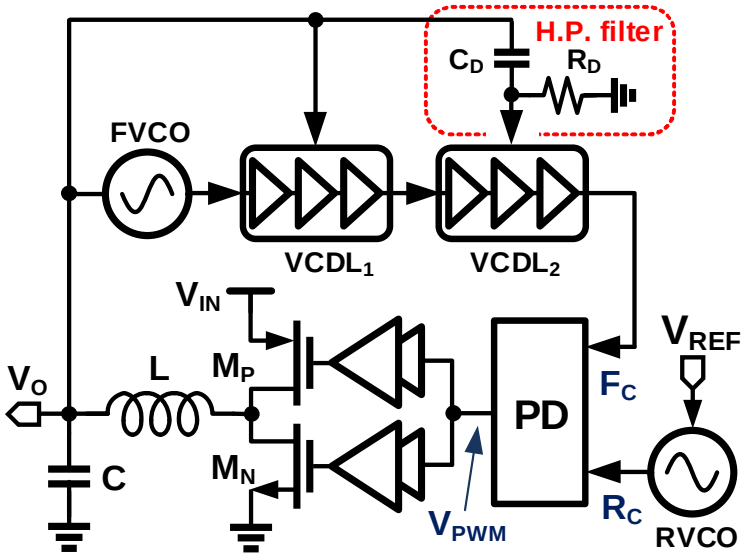


Figure 3.8: Buck converter with time-based PID compensator.

ripple attributes of an analog compensator and robustness to noise and small area of a digital compensator. We briefly describe its basic operation using a simplified buck converter shown in Fig. 3.7. It employs a time-based Type-I compensator implemented using voltage-controlled oscillators (RVCO and FVCO) and an S-R latch-based phase detector (PD). The error voltage ($V_{REF} - V_O$) is integrated and converted into phase, Φ_E, by the FVCO. The PD measures the phase difference between Φ_E and reference phase Φ_{REF} and produces the desired PWM signal. If V_O is lower than V_{REF}, FVCO frequency increases, which increases

the duty-cycle and pushes V_O closer to V_{REF} such that V_O is equal to D times V_{IN} and FVCO frequency is equal to RVCO frequency, in steady-state (see Fig. 3.7(b)). Thus, the entire buck converter can also be viewed as a frequency locked loop (FLL). The Type-I compensator can be extended to implement a PID compensator as shown in Fig. 3.8. Voltage controlled delay, $VCDL_1$ implements proportional control while $VCDL_2$ along with the high-pass filter implements derivative control.

3.3.2 Multi-Phase PWM Generator

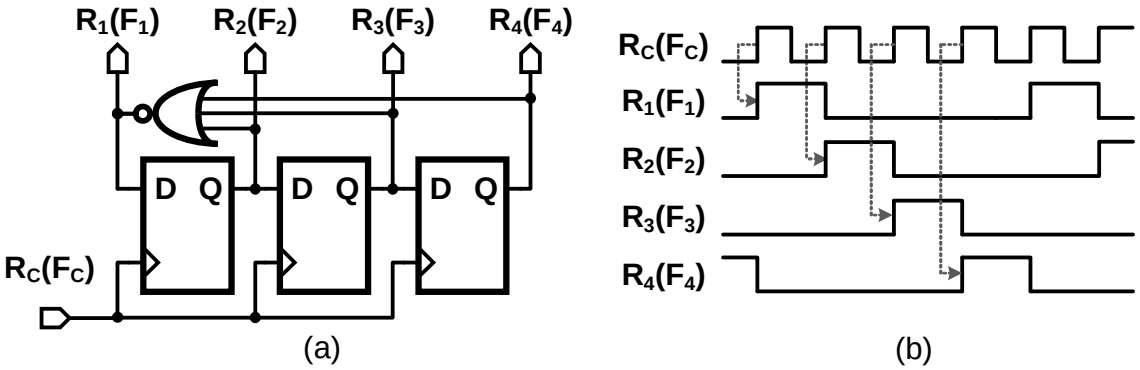


Figure 3.9: Schematic of multi-phase generator (MPG).

Four PWM signals to control each of the four phases with precisely matched duty-cycles are generated from the phase outputs (Φ_{R_C} and Φ_{F_C}) of the compensator. The four-phase duty-cycle generation is performed in two stages. First, a multi-phase generator (MPG) produces four uniformly spaced phase signals from R_C and R_F, which are then used by a set of phase detectors to generate four PWM signals with precisely matched duty-cycles. The architecture of the MPG is depicted in Fig. 3.9 (a). It consists of three D-flip-flops connected in a feedback shift register configuration in which the NORed output of the three D-flip-flops in the chain is fed back to the input of the first D flip-flop. All the D-flip flops are clocked by the input clock (either R_C or F_C) and Q output of D flip-flops serve as four phase outputs ($R_{1\sim4}$ or $F_{1\sim4}$). The operation of the MPG can be best described using the timing diagram shown in Fig. 3.9 (b). On the first positive edge of R_C (F_C), R_1 (F_1) signal becomes logic high and remains high until the next positive edge. On the second positive edge, R_1

(F_1) goes low and R_2 (F_2) becomes logic high and remains high until the arrival time of the third positive edge. Similarly, R_3 (F_3) and R_4 (F_4) signals are generated subsequently. This process repeats itself after R_4 (F_4) goes low. Note that the MPG behavior is analogous to a divide-by-four frequency divider and as a result, the frequency of the output phases is one-fourth the frequency of the input clock frequency.

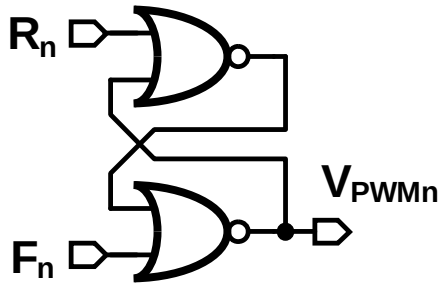


Figure 3.10: Phase detector (PD).

The four PWM signals, $V_{PWM1\sim4}$, that drive the power FETs in each of the four phases are generated from $R_{1\sim4}$ and $F_{1\sim4}$, using an S-R latch-based phase detector shown in Fig. 3.10. Each phase detector PD_n measures the phase difference between R_n and F_n signals and generates the corresponding V_{PWMn} with the desired duty-cycle (see Fig. 3.11). Because the frequencies of RVCO and FVCO are locked in steady-state, the frequency of all the V_{PWM} signals is equal to $1/(4T_{VCO})$, where T_{VCO} is the time period of R(F)VCO. Further V_{PWM} signals are separated exactly by one VCO period, T_{VCO}, which translates to a precise $\pi/2$ phase spacing when normalized by the period of the V_{PWM} signals ($4T_{VCO} = 2\pi$). The duty-cycle of all the V_{PWM} signals are also precisely matched because they are generated from the same input (R_C/F_C) and using well-matched circuit elements such as D-flip flops. The duty-cycle of the V_{PWM} signals is equal to:

$$D_{1\sim4} = \frac{T_{R_n-F_n}}{4 \cdot T_{R(F)VCO}} = \frac{\Phi_{R_n-F_n}}{2\pi} = \frac{V_O}{V_{IN}} \tag{3.13}$$

where $T_{R_n-F_n}$ is the time period between the positive edges of R_n and F_n and $\Phi_{R_n-F_n}$ is the phase difference between R_n and F_n.

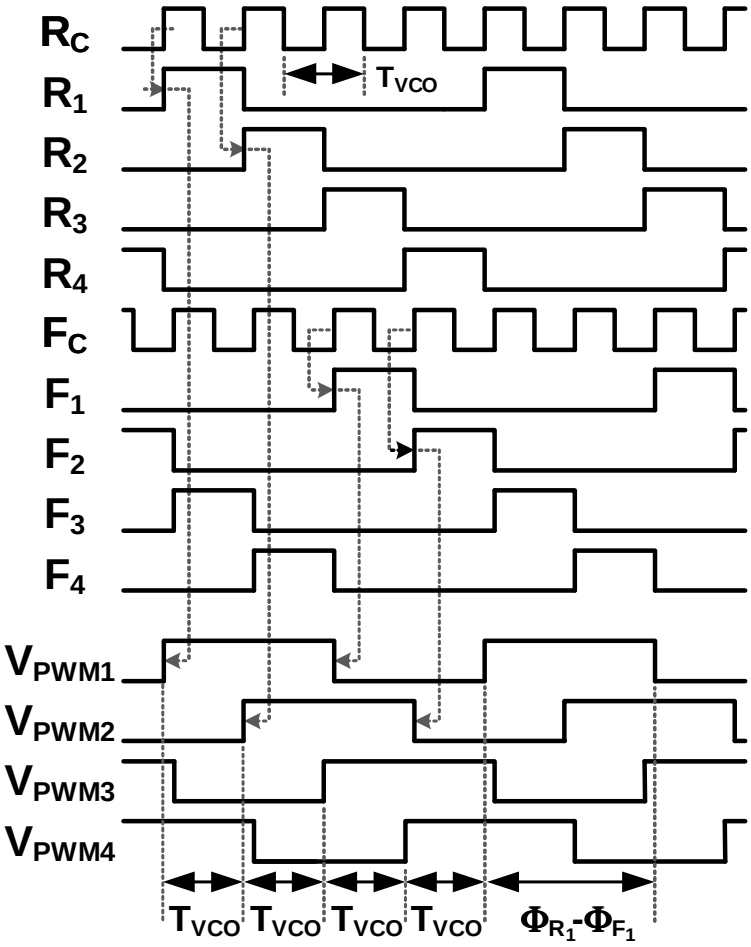


Figure 3.11: Waveforms in the proposed controller.

3.4 Time-Based Controller Implementation Issues

3.4.1 Output Voltage Offset

The output voltage offset defined as the deviation of the output voltage from the reference voltage is dictated by two error sources. Considering the implementation of the two VCOs (RVCO and FVCO) shown in Fig. 3.12, the two sources are: (a) threshold voltage and current gain mismatch (ΔV_{TH} and $\Delta\beta$) between the input differential pair transistors and (b) mismatch between the free-running frequencies ($\Delta\omega_{free}$) of two current-controlled oscillators (FCCO and RCCO). The expression for the output voltage offset (ΔV_O) can be derived as:

$$\Delta V_O = \Delta V_{TH} + \frac{V_{OV}\Delta\beta}{2\beta} + \frac{\Delta\omega_{free}}{G_M \cdot K_{CCO}} \tag{3.14}$$

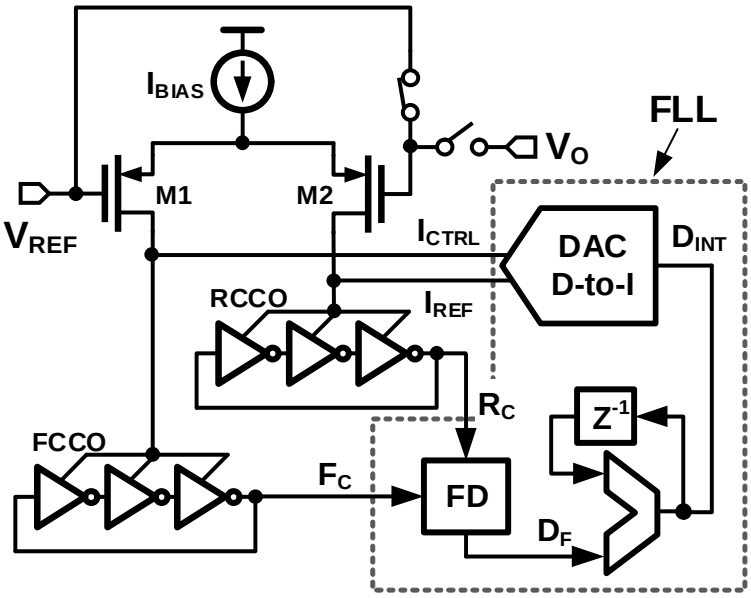


Figure 3.12: Pseudo differential VCO along with FLL to match free-running frequencies of RCCO and FCCO.

where V_{OV} is the overdrive voltage (V_{GS}-V_{TH}), β is equal to $\frac{W\mu C_{OX}}{L}$, G_M is the average transconductance of M1 and M2, and K_{CCO} is the average frequency gain of the two CCOs in rad/sec/A. We note increasing the device area and choosing large overdrive voltage can easily mitigate the offset caused by input pair mismatch. On the other hand, mitigating the offset voltage caused by free-running frequency mismatch is not as straightforward. For example, in this design, the standard deviation of the frequency mismatch of the two VCOs was 6MHz, which translates into 200mV of output voltage offset ($K_{VCO} \approx 30$MHz/V). We propose to suppress this voltage offset by using a digital frequency locked loop (FLL) shown in Fig. 3.12. The FLL measures the difference between the free-running frequencies of the two CCOs and tunes the frequency of FCCO to be equal to that of the RCCO. The residual offset after the FLL achieves frequency lock is determined by the frequency resolution of FLL ($F_{FLL,LSB}$) and is equal to:

$$V_{O,offset} = \frac{F_{FLL,LSB}}{K_{VCO}} \tag{3.15}$$

where the K_{VCO} is equivalent to $G_M \cdot K_{CCO}$. In order to achieve less than 5mV of output voltage offset with a coverage of 3-sigma value of the frequency mismatch, FLL resolution in our design is approximately 150kHz. A conventional counter-based frequency detector (FD)

measures the frequency error in the form of a digital word, D_F, by finding the difference between the number of RCCO and FCCO periods in a given interval [29]. A digital loop filter composed of a digital accumulator integrates D_F and tunes the FCCO frequency through a thermometer-coded current mode digital to analog converter (DAC). FLL monotonically increases/decreases the FCCO frequency such that frequency error is close to zero in steady-state. Due to the limited resolution of DAC, the steady-state is a bounded limit cycle, which manifests itself as dithering of the FD output between ± 1 codes. To prevent this dithering, the accumulator output is frozen after the FLL is locked. As a result, the residual frequency error in steady-state is dictated by the LSB of DAC ($I_{DAC,LSB}$) and CCO gain (K_{CCO}) and is equal to $I_{DAC,LSB} \cdot K_{CCO}$.

3.4.2 Cycle-Slipping

Time-based compensator is susceptible to cycle-slipping behavior [30], which can severely limit the output voltage range of the converter. Consider the waveforms shown in Fig. 3.13 which depict the response of voltage- and time-based controllers. A load step from light load to heavy load causes a voltage droop in the output voltage. In response to this, the feedback loop increases the control voltage (V_{CTRL}) in voltage mode controller and the phase difference between R_n and Fn in time-based controller so as to increase the duty-cycle in both cases. A major difference between the behavior of voltage- and time-mode controllers is in the way they respond when the duty-cycle reaches either 100% or 0% during the transient. In the case of a voltage mode controller, the duty-cycle saturates to 100% and remains at 100% even if the control voltage becomes higher than the maximum ramp voltage as shown in Fig. 3.13 (a). However, in case of time-based controller, when the phase difference reaches 2π, it rolls-over to zero due to the inherent modulo-2π behavior of the phase detector shown in Fig. 3.14. This large sudden jump in phase introduces a large transient in the output voltage and severely degrades the transient response of the converter. Similarly, a rapid change of output load current from heavy load to light load may result in the sudden change of duty-cycle from 0% to 100%.

In an attempt to mitigate cycle slipping, we first note that cycle-slip causes two successive

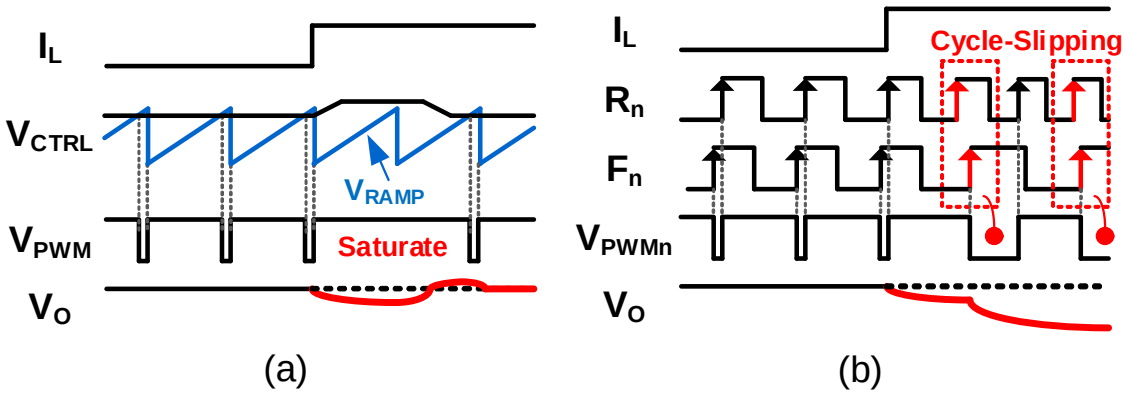


Figure 3.13: Saturation and cycle-slip behaviors.

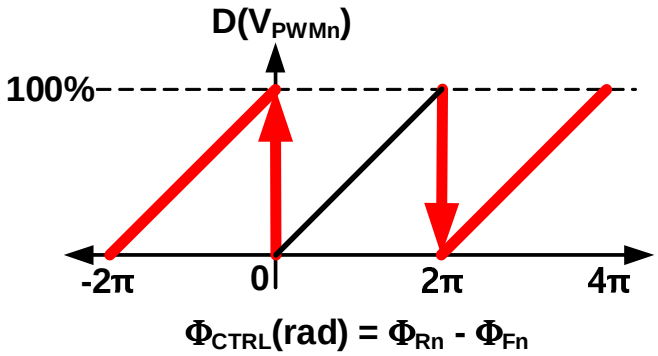


Figure 3.14: Duty-cycle vs. phase of control signal.

positive edges on R_n or F_n without an intervening positive edge on F_n or R_n as shown in Fig. 3.13 (b). Based on this, a Cycle-Slip Detector (CSD) along with the modified phase detector (see Fig. 3.15 (a)) detects when two successive positive edges occur on R_n (or F_n) and sets signal SH (or SL) to logic high. The detailed state-machine for CSD control implementation is depicted in Fig. 3.15 (b). As a result, signals SH (or SL) saturate the duty-cycle to 100% (or 0%) through a simple logic operation in the phase detector. Accordingly, the large output droop caused by the cycle-slip is prevented as illustrated in Fig. 3.16.

3.5 Prototype Buck Converter

The block diagram of the implemented prototype four-phase buck converter is shown in Fig. 3.17. Other than the four inductors, L_{1-4} (90nH each), and the output capacitor, C

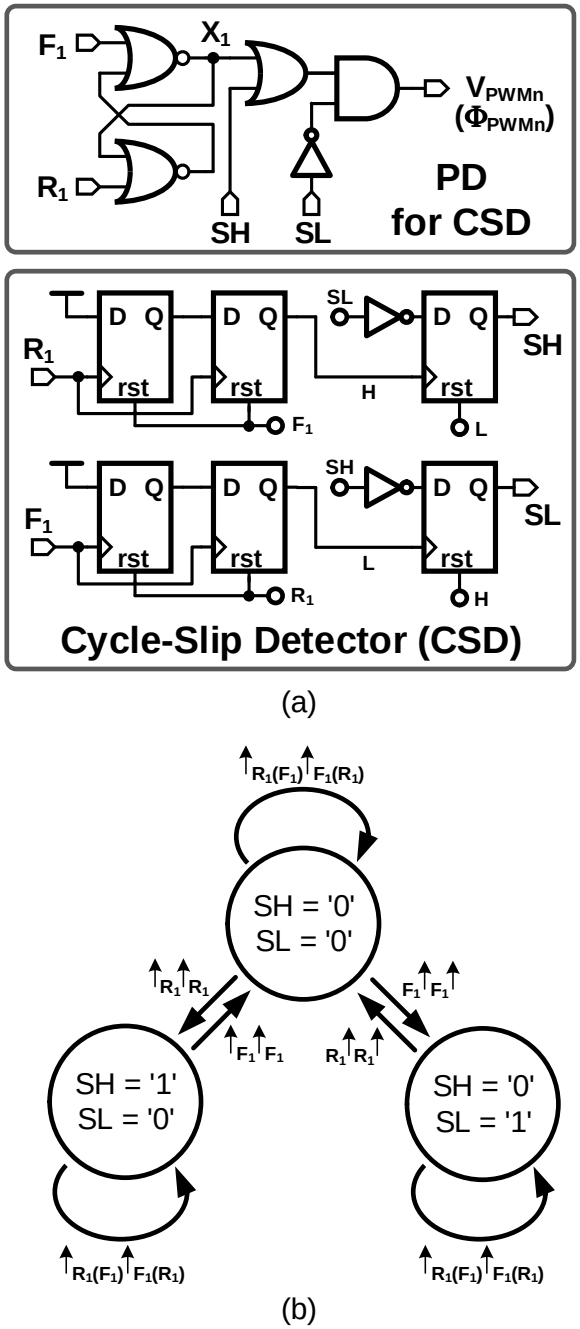


Figure 3.15: (a) Proposed PD with CSD and, (b) its state-machine representation.

(480nF), all other components are integrated on chip. The prototype converter was designed to operate with higher than 30MHz switching frequency and generate output voltages in the range of 0.6-1.5V from a 1.8V input voltage with target specifications shown in Table 3.1.

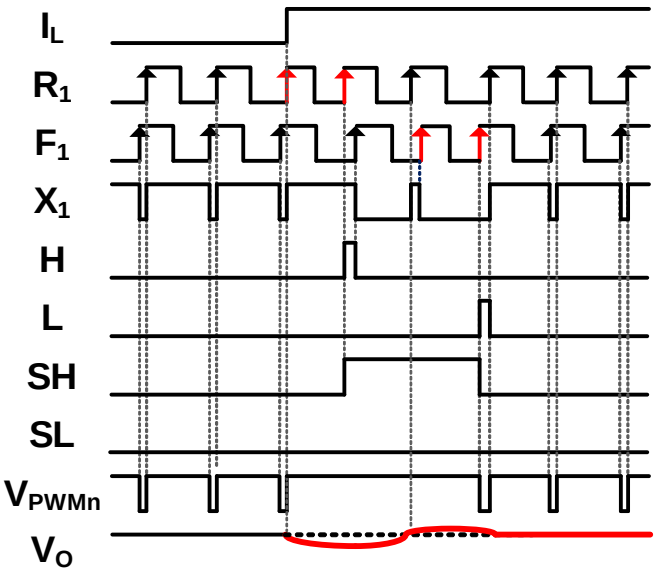


Figure 3.16: Operation of cycle-slip detector (CSD).

Table 3.1: Prototype buck converter target specifications.

V_{IN}	V_{OUT}	Phases	F_{SW}	L	C	BW	Φ_M
1.8V	0.6-1.5V	4	30MHz	90nH	470nF	$\approx$ 5MHz@1-phase	50°

3.5.1 Compensator Design

The T-PID compensator was implemented in pseudo-differential architecture and the two VCDLs for the proportional and the derivative control shown in Fig. 3.8 are combined using one CCDL. The CCDL is implemented using a cascade of 11 single-ended inverters. This not only helps to reduce power consumption but also improves phase margin by lowering loop delay [28]. The loop parameters are calculated using the transfer function of the time-based PID compensator shown in Eq.(3.16):

$$H_{T-PID}(s) = \frac{1}{k}\left(K_{VCDL_1} + \frac{K_{VCO}}{s} + K_{VCDL_2} R_D C_D s\right) \tag{3.16}$$

where k is the number of phases and is equal to 4 in our design, and $K_{VCDL1,2}$ and K_{VCO} are gain of the VCDLs and VCO, respectively. The open-loop transfer function $H_{Multi-buck}(s)$ of

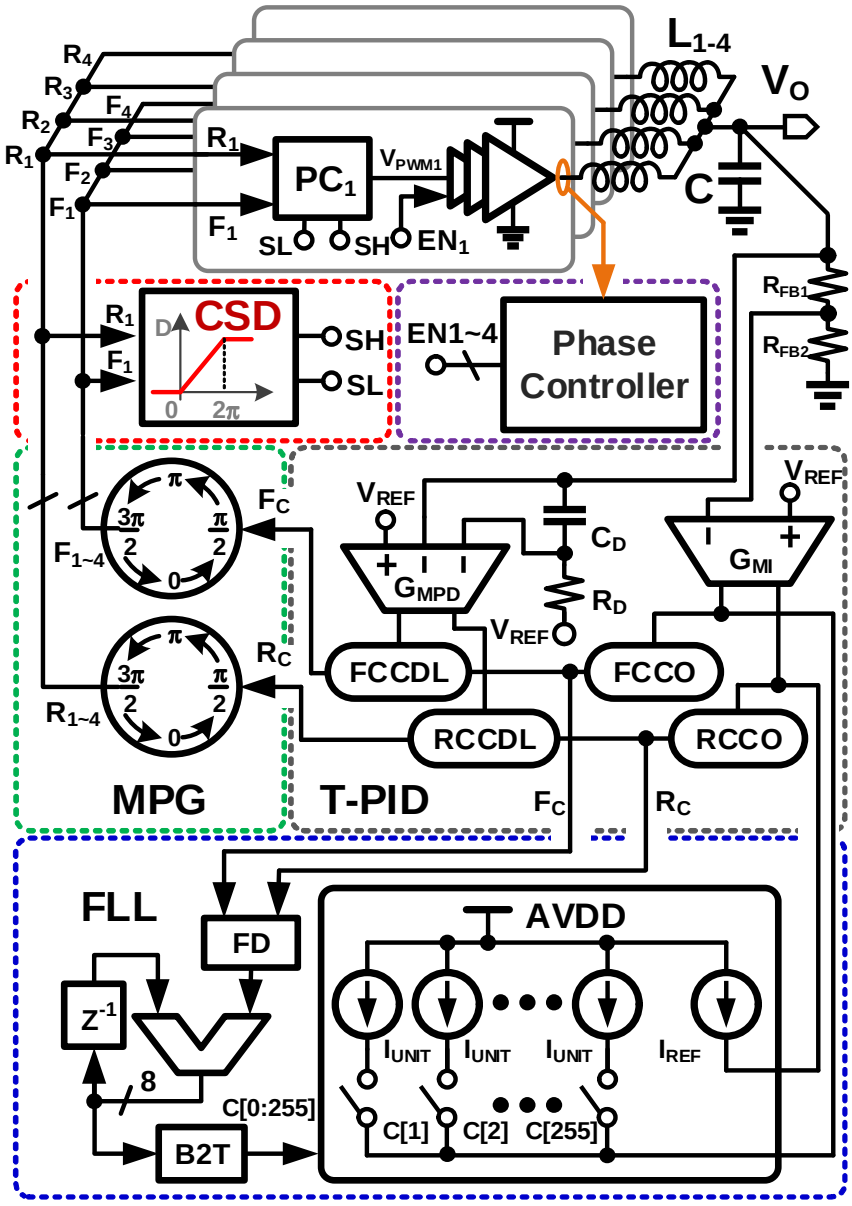


Figure 3.17: Complete block diagram of the prototype multi-phase buck converter.

the converter is equal to:

$$H_{Multi-buck}(s) = H_{BUCK}(s) \cdot H_{T-PID}(s) \cdot H_{PD}(s) \tag{3.17}$$

where H_{BUCK} and H_{PD} are the transfer function of buck converter and phase detector, respectively. L is equal to sum of all inductances connected in parallel according to the number of operating phases. The values of compensator parameters such as K_{VCO}, K_{VCDL1}, K_{VCDL2}

and R_DC_D are calculated using the design process described in [28] and the result is shown in Table 3.2. These parameters are chosen to achieve a GBW of 9.85MHz, 8.64MHz, and 4.84MHz and phase margin of 55 degrees, 68 degrees, and 54 degrees for a 4-, 2-, and 1-phase operation, respectively. The phase margin is greater than 45 degrees even in the presence of PVT variations [3]. A bode plot of the open-loop transfer function $H_{Multi-buck}(s)$ using the calculated parameters is shown in Fig. 3.18.

Table 3.2: Parameters for time-based circuit components.

K_{VCO}	K_{VCDL1}	K_{VCDL2}	R_DC_D
43.11MHz/V	0.2146μs/V	2.146μs/V	1.566ns

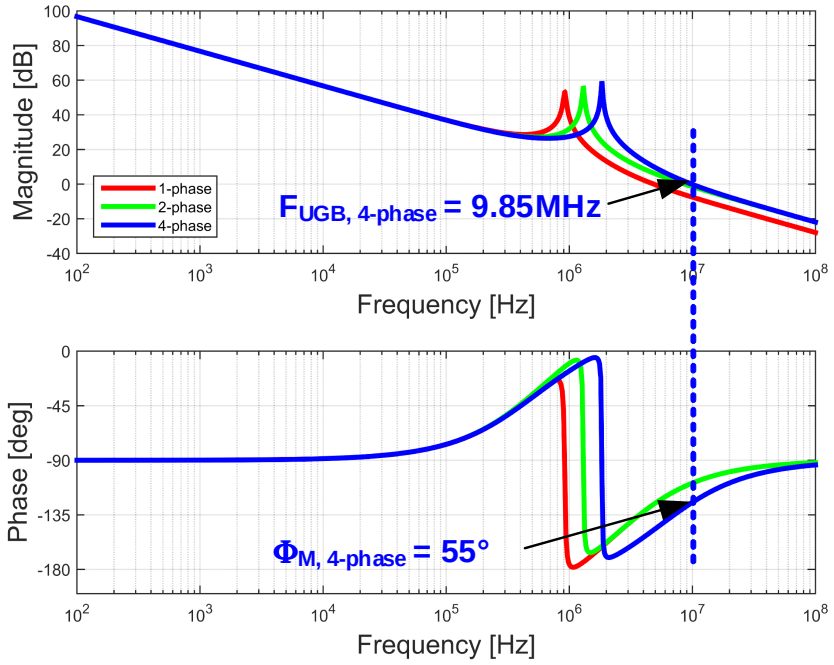


Figure 3.18: Bode plot of the converter.

3.5.2 Output Driver Architecture

The schematic of the cascoded output driver capable of operating with 1.8V input voltage is shown in Fig. 3.19 [31]. Using cascoded 1V devices instead of 1.8V devices results in smaller area and lower power. In 65nm CMOS logic process, the cascoded output driver occupies

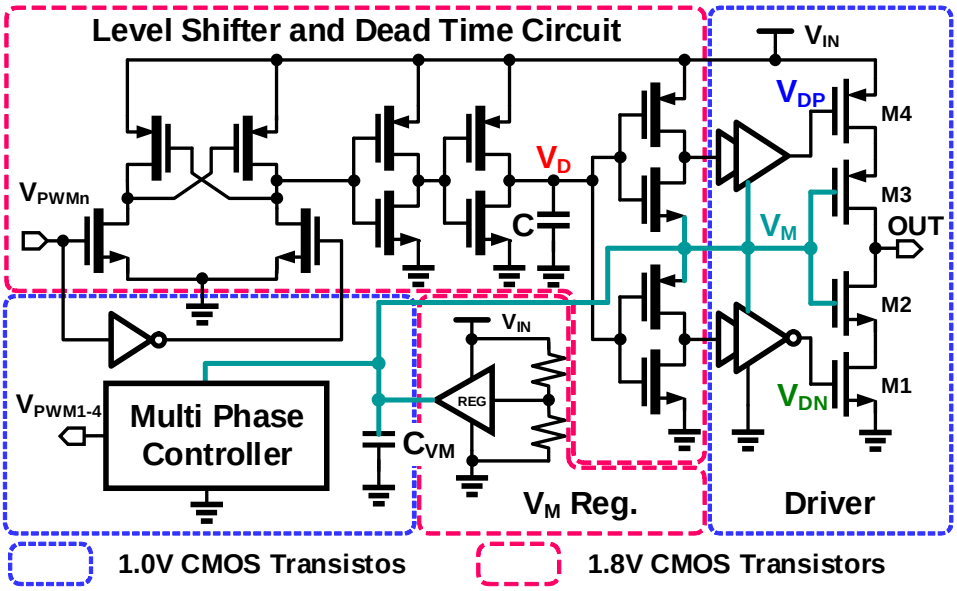


Figure 3.19: Cascoded output driver.

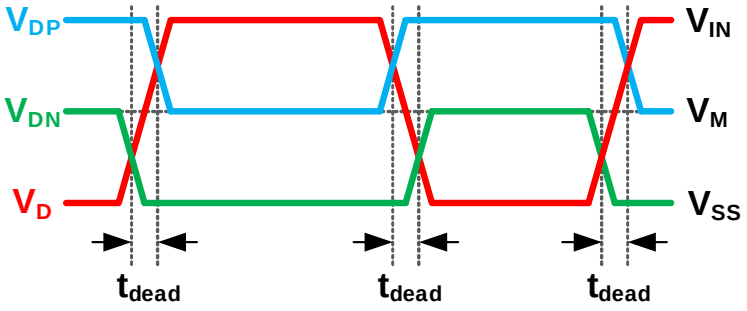


Figure 3.20: Dead time generation.

60% smaller die area and has 55% lower gate switching power consumption compared to an output driver using 1.8V devices for the same on-resistance. The gates of cascode transistors M3 and M2 are biased with voltage V_M equal to $V_{IN}/2$ (=0.9V). As a result, transistors M1 and M4 are driven within the power rails of V_M-VSS and V_{IN}-V_M both of which are equal to 0.9V. High side switching charge is recycled and utilized to power the controller. When the high-side driver pulls down the gate voltage of M4 from V_{IN} to V_M, the current (charge) is saved into V_M capacitor (C_{VM}). Next, saved charge in the V_M capacitor is reused when the low-side driver pulls up the gate voltage of M1 from VSS to V_M. Because the gate capacitance of the high-side switch (M4) is 3.4 times larger than the low-side switch (M1) in our design, the amount of recycled charge (approximately 2.74mA/power-train) is more

than sufficient to supply power to both low-side switching (approximately 0.8mA/power-train) and the controller (approximately 0.1mA). Regulator (V_M Reg.) generates voltage V_M during start-up and regulates it during normal operation. Dead-time is generated by using the slope of intermediate voltage V_D as shown in Fig. 3.20. As V_D rises from VSS to V_{IN}, low-side front-end inverter composed of thick oxide transistors (1.8V) turns on first and the high-side front-end inverter turns on subsequently. The delay between these two on-times was utilized to generate dead time for the cascoded output driver. The duty-cycle mismatch of output drivers due to device mismatches is negligible ($<$ 100ps) compared to the converter switching period (33.3ns@F_{SW} = 30MHz). As a result, device mismatches only contribute to a maximum efficiency degradation of about 0.01%. The effect of driver delay (from V_{PWMn} to $V_{DP/DN}$) can also be neglected in our design because the delay ($\approx$ 1.5ns) is much smaller than the time constant associated with the BW of converter (τ_{BW} = 16ns).

3.6 Experimental Results

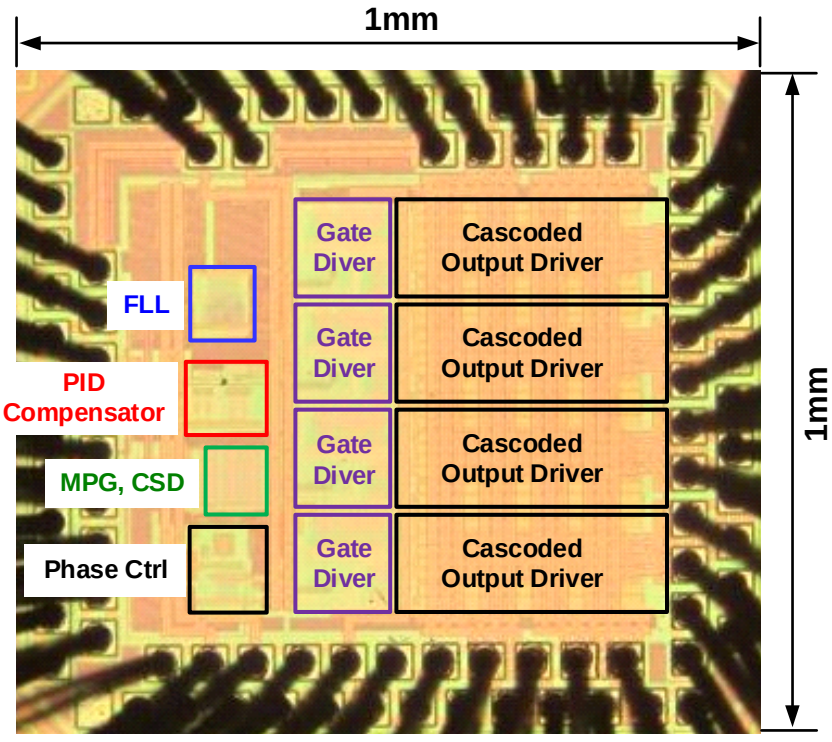


Figure 3.21: Die photo.

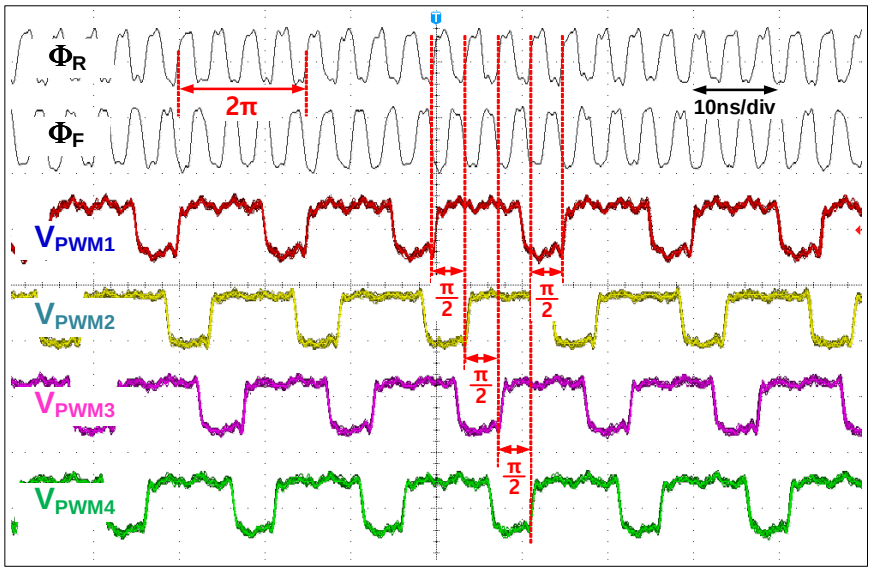


Figure 3.22: Measured steady-state waveforms (V_O=1V).

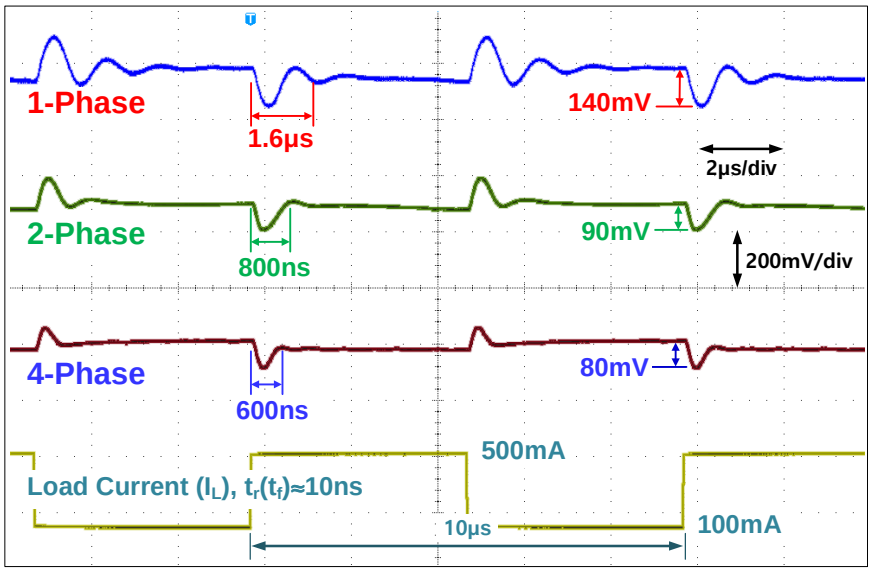


Figure 3.23: Measured load transient response (V_O=1V).

The proposed buck converter is implemented in 65nm CMOS process. The die photo is shown in Fig. 3.21. The total die size is 1mm^2 of which the active area is 0.32mm^2. The measured steady-state waveforms of the compensator outputs and PWM signals are shown in Fig. 3.22. The duty-cycle mismatch among the PWM signals is less than 0.48% at 30MHz switching frequency, which contributes to only 3.24% of current mismatch and 0.022% of efficiency degradation. Figure 3.23 shows the converter transient response when a 400mA load current step is applied. The measured undershoot/overshoot is 140mV, 90mV

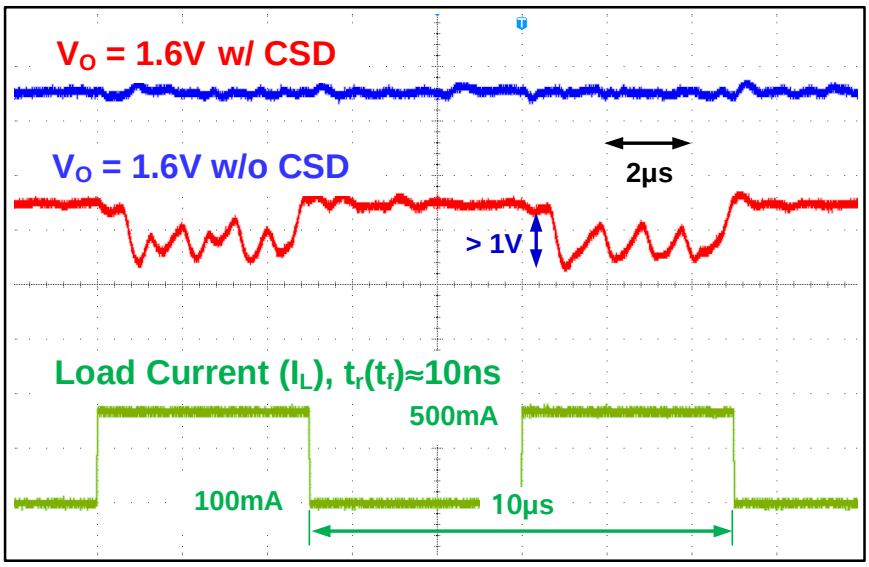
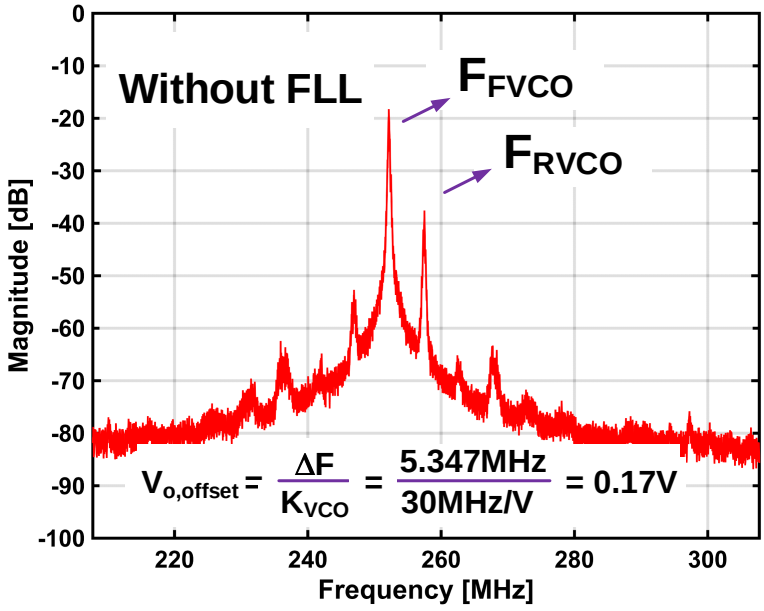
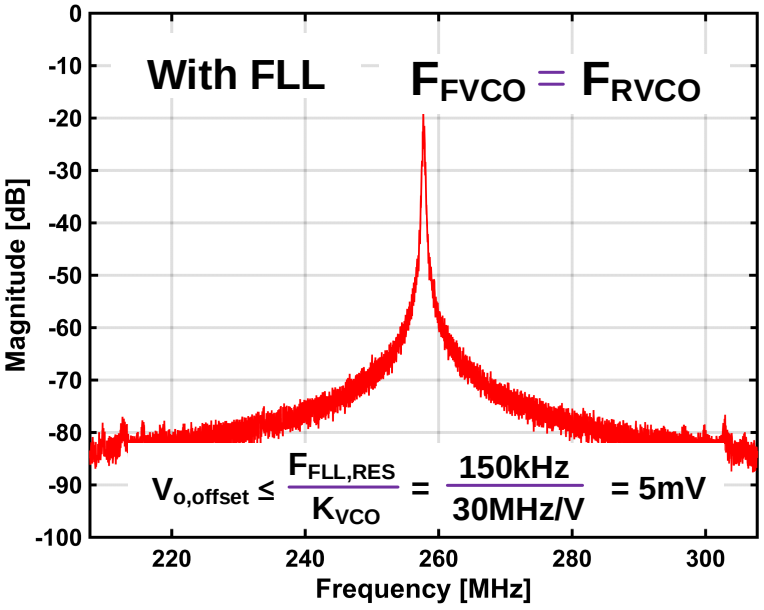


Figure 3.24: Measured output voltage waveform with CSD and, without CSD.

and 65mV and settling time is less than 1.6μs, 0.8μs, and 0.6μs when operating with one, two, and four phases, respectively. Figure 3.24 shows measured output voltage waveforms when the cycle slipping detector is enabled/disabled and 400mA load step is applied at an output voltage of 1.6V. It is clear that the cycle-slip detector prevents the transient response degradation, as desired. Figure 3.25 shows the measured output spectra of the two VCOs. When the FLL is turned off (Fig. 3.25 (a)), mismatch between the free-running frequencies of the two VCOs is measured to be about 5.35MHz, which translates to an output voltage offset of 0.17V. When the FLL is turned on (Fig. 3.25 (b)), the frequency error and the output voltage offset reduces to less than 0.15MHz and about 5mV, respectively. The measured efficiency curves of the converter at V_O=1V plotted as a function of load current for two different F_{SW} of 30MHz and 70MHz are depicted in Fig. 3.26. Peak efficiency of 87% is achieved at F_{SW}=30MHz at a load current of 150mA. For load currents ranging from 70-700mA, the efficiency is higher than 80%. Efficiency curves at F_{SW}=70MHz illustrate the proposed converters ability to operate at a high F_{SW}. Performance summary and comparison with state-of-the-art multi-phase converters is shown in Table 3.3. The proposed time-based multi-phase buck converter achieves 87% peak efficiency and power density of 2.5W/mm^2 while consuming 90μA of controller current at F_{SW} of 30MHz, which compare very favorably with state-of-the-art converters.



(a)



(b)

Figure 3.25: Measured frequency spectra of the two VCOs (a) without FLL and, (b) with FLL (V_O=1V).

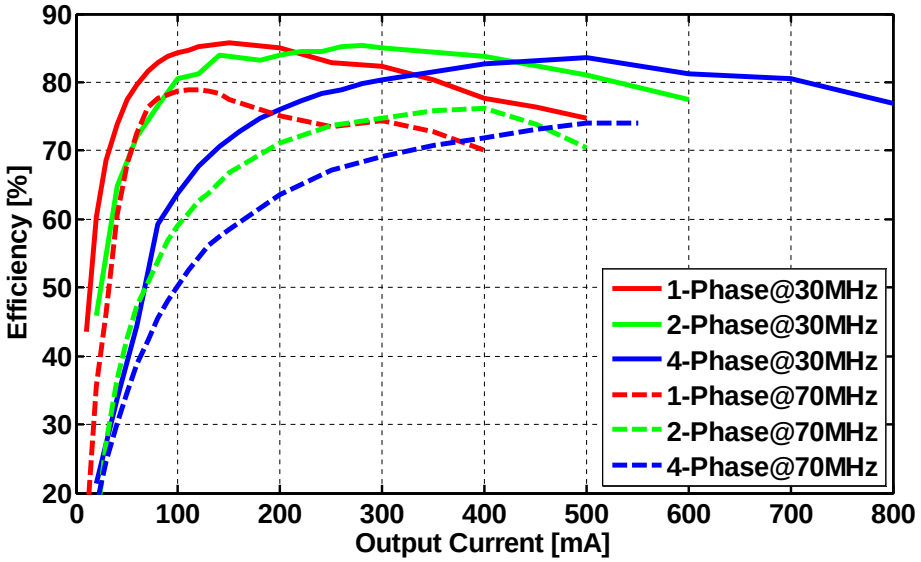


Figure 3.26: Measured efficiency plots (V_O=1V).

Table 3.3: Performance of the proposed buck converter and its comparison with the state-of-the-art.

Publication	This Work	JSSC '05 [32]	JSSC '09 [33]
Process	65nm CMOS	90nm CMOS	0.5μm CMOS
Control	T-PID PWM	Hysteretic	Hysteretic
Sync.	MPG	Injection	DLL
Input Supply [V]	1.8	1.2/1.4	4-5
Output Voltage [V]	0.6-1.5	0.9/1.1	0.86-3.93
F_{SW} [MHz]	30-70	233	25-70
L [nH]	90	2.5	110-220
C [nF]	470	6.8	6-190
$I_{LOAD,MAX}$ [A]	0.8	0.3/0.4	1
$I_{Q,Controller}$ [μA]	90@30MHz	N/A	N/A
Peak Effi. [%]	87@V_O = 1V	83.2/84.5	83@V_O = 3.3V
Pwr. Den. [W/mm^2]	2.5	1.93/3.14	1.2

CHAPTER 4

TIME-BASED CONTROLLER WITH LIGHT LOAD

4.1 Light Load Efficiency

Aggressive use of dynamic power management techniques in energy-aware hand-held devices requires buck converters to have: (i) fast reference tracking to support DVS, (ii) an ability to quickly switch from light load to heavy load to support deep power states, (iii) high efficiency across a very wide range of loads, and (iv) small form factor. Various high FSW switching DC-DC converters with PWM control have been introduced highlighting some advantages, i.e., small form factor, fast load transient response, and the ability of integration [7, 32, 34]. However, its high switching loss and high static power consumption makes it more difficult to maintain high efficiency in a light load condition which has the significant inpact on the overall battery lifetime of a mobile device. Accordingly, additional control loop such as PFM has to be added so as to decrease the switching frequency proportional to a load condition which can greatly improve the light load efficiency [31,35]. By having the two control loops, the light load efficiency can be improved by PFM control while PWM control can provide low output voltage ripple, constant F_{SW}, and high efficiency especially for non-light load current.

4.1.1 Pulse Frequency Modulation Control

Figure 4.1 shows the individual power loss components of the fixed switching frequency (i.e. PWM control). It can be seen that the power efficiency degrades at low load output current due to the fixed amount of the switching loss regardless of the magnitude of the load current. In the comparison to the fixed frequency case, Fig. 4.2 shows the PFM case

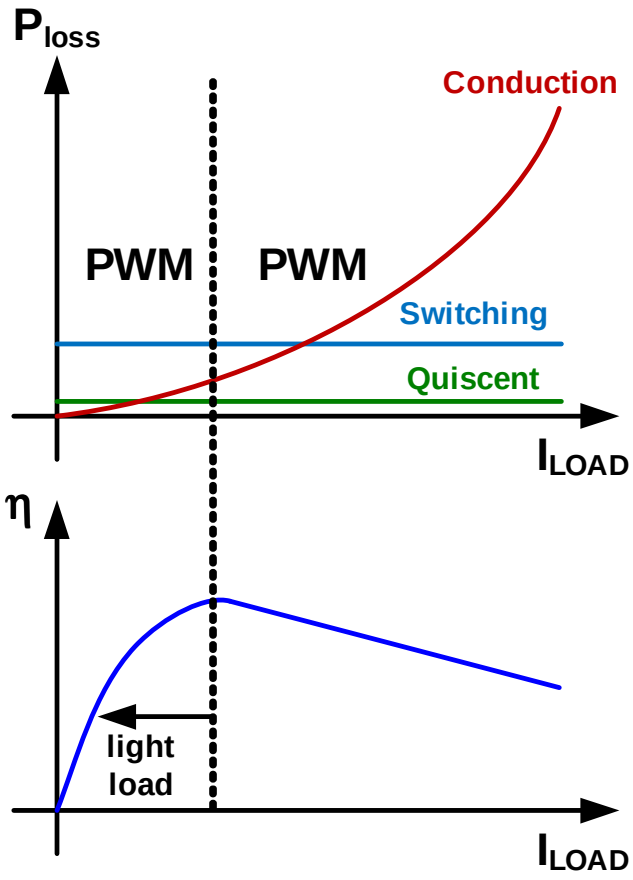


Figure 4.1: Power loss vs. load current in PWM.

where the switching frequency varies proportional to the magnitude of the load current. The efficiency for light load is improved because both the switching loss and the conduction loss decrease with load current. For the PFM operation, the control variable to regulate output voltage is the switching frequency with a fixed inductor peak current ($I_{L,pk}$). Figure 4.3 shows the inductor current waveforms in the PFM operation. For each PFM pulse, the total amount of charge (Q_{PFM}) which is transferred to the output can be calculated as:

$$Q_{PFM} = \frac{1}{2} \times I_{L,pk} \times (t_r + t_f) \tag{4.1}$$

where t_r and t_f are:

$$t_r = \frac{L \times I_{L,pk}}{(V_{IN} - V_O)} \text{ and } t_f = \frac{L \times I_{L,pk}}{V_O} \tag{4.2}$$

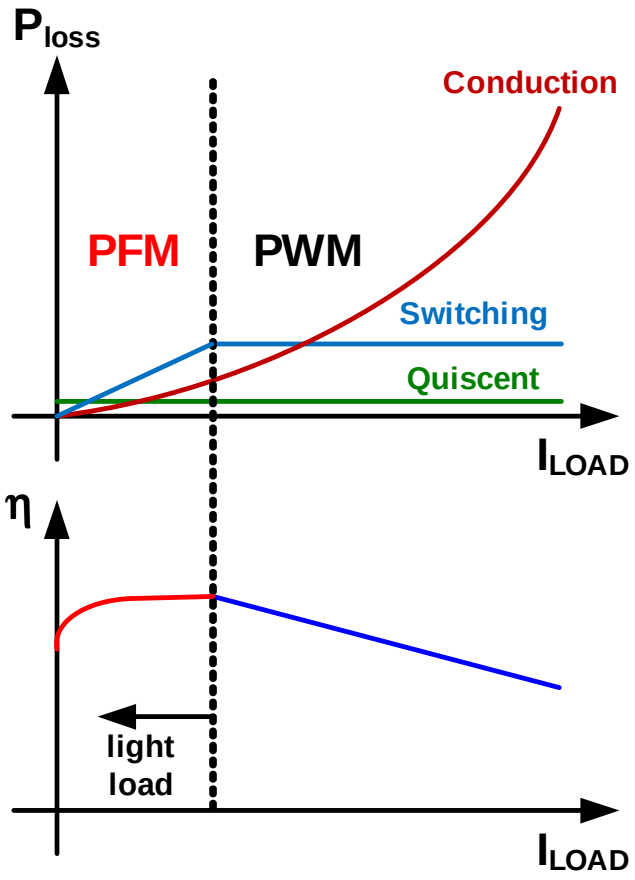


Figure 4.2: Power loss vs. load current in PFM control for light load.

Accordingly, the switching frequency will be set where the total amount of the transferred charge per second to the output is equal to the load current (I_{LOAD}) and then it can be written as:

$$F_{SW,PFM} = \frac{I_{LOAD}}{Q_{PFM}} = \frac{2 \times I_{LOAD}}{I_{L,pk} \times (t_r + t_f)} \tag{4.3}$$

As shown in Eq. (4.3), the switching frequency varies proportional to the amount the load current (I_{LOAD}) which results in the reduction of both the switching and conduction losses. The optimal efficiency in the PFM operation can be found by investigating the loss components of the PFM operation. Referring to the Fig. 4.3, the conduction loss ($P_{cond,PFM}$) and

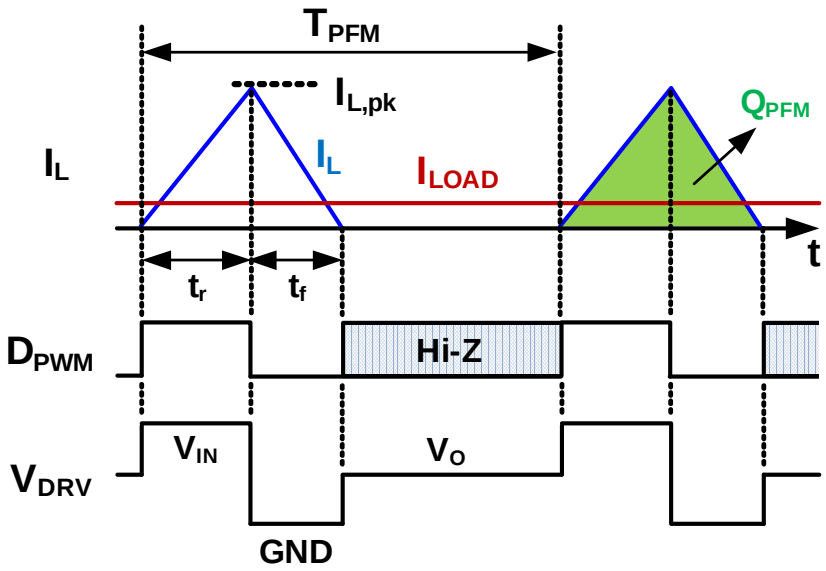


Figure 4.3: Inductor current waveform in PFM.

the swiching loss ($P_{sw,PFM}$) of the PFM operation can be obtained by:

$$\begin{aligned} P_{cond,PFM} &= \frac{1}{T}\int_0^T (I_L(t))^2 \times ESR_{tot} dt = I_{L,rms}^2 \times ESR_{tot} \\ &= I_{L,pk}^2 \times \frac{(t_r + t_f) \times ESR_{tot}}{3} \times F_{SW,PFM} \end{aligned} \tag{4.4}$$

$$P_{sw,PFM} = C_{tot} \times V_{IN}^2 \times F_{SW,PFM} \tag{4.5}$$

where the ESR_{tot} is the total series resitance in the current path (inductor, power transistors, etc.) and the C_{tot} is the total summed capacitance of the gate driver. From Eq. (4.3), Eq. (4.4) and Eq. (4.5), the total power loss of PFM operation can be estimated to:

$$P_{loss,PFM} = I_{L,pk} \times \frac{2 \times I_{LOAD} \times ESR_{tot}}{3} + C_{tot} \times V_{IN} V_O (V_{IN} - V_O) \times \frac{2 \times I_{LOAD}}{L \times I_{L,pk}^2} \tag{4.6}$$

Then the efficiency of PFM operation will be:

$$\begin{aligned} \eta_{PFM} &= \frac{P_O}{P_O + P_{loss,PFM}} \\ &= \frac{V_O}{V_O + I_{L,pk} \times \frac{2 \times ESR_{tot}}{3} + C_{tot} \times V_{IN} V_O (V_{IN} - V_O) \times \frac{2}{L \times I_{L,pk}^2}} \end{aligned} \tag{4.7}$$

Note that the efficiency of the PFM operation is now independent of the output load current (I_{LOAD}). In reality, the existence of static power consumption such as quiescent current and leackage current degrades the efficiency if the output power ($P_O = V_O \times I_{LOAD}$) decreases to a value where it is comparable to the static power. The $I_{L,pk}$ value for maximum efficiency can be found by minimizing the denominator in Eq. (4.7) by derivating it with respect to $I_{L,pk}$ and setting it equal to 0. The result is:

$$I_{L,pk}@\eta_{max} = \left\{ \frac{6 \times C_{tot} \times V_{IN} V_O (V_{IN} - V_O)}{ESR_{tot} \times L} \right\}^{\frac{1}{3}} \tag{4.8}$$

$$I_{L,pk} = \frac{V_{IN} - V_O}{L} \times T_{ON,PFM} = \frac{V_{IN} - V_O}{L} \times t_r \tag{4.9}$$

By inspecting the Eq. (4.8), the maximum efficiency can be obtained by having an appropriate peak inductor current ($I_{L,pk}$) which can be controlled by the on-time ($T_{ON,PFM}$) as shown in Eq. (4.9) which is identical to t_r in Eq. (4.2). However, Eq. (4.8) also shows that the maximum efficiency is not only the function of $I_{L,pk}$ but also a function of input and output voltages (V_{IN} and V_O). Therefore, the on-time ($T_{ON,PFM}$) needs to be adjusted according to Eq. (4.8) with respect to input and output voltages. Figure 4.4 and Fig. 4.5 show examples

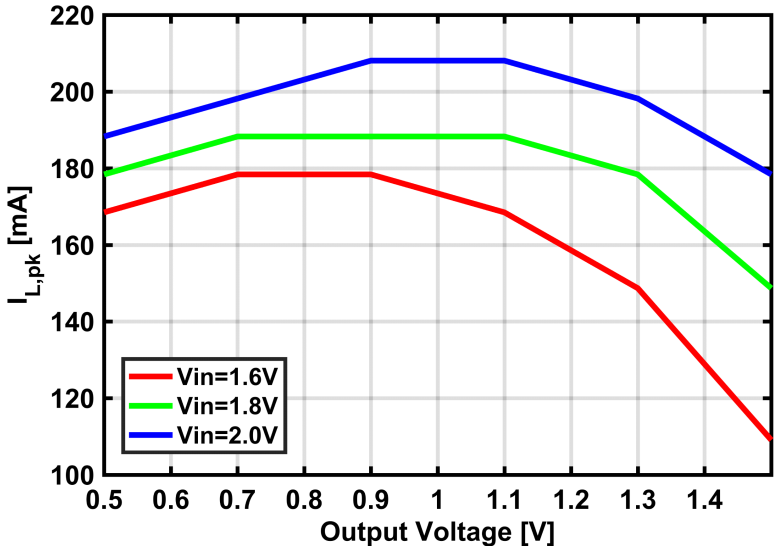


Figure 4.4: Optimal $I_{L,pk}$ for various input and output voltages.

of the optimum $I_{L,PK}$ and the associated on-time ($T_{ON,PFM}$) for several different input and

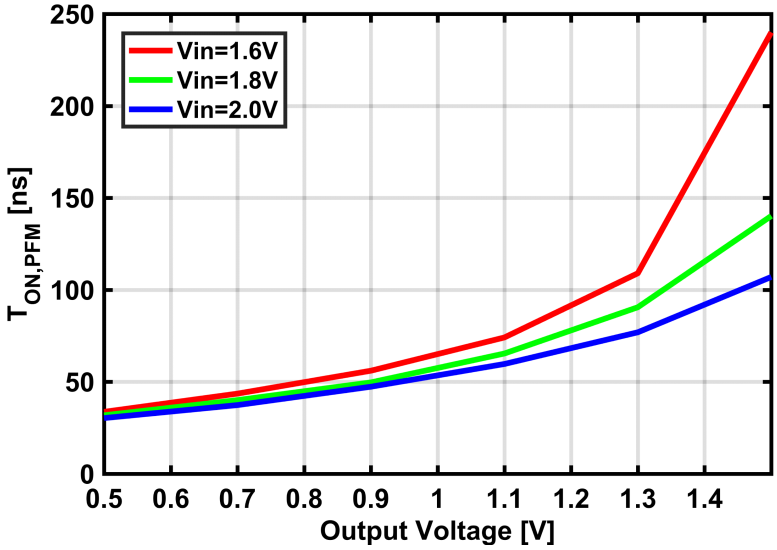


Figure 4.5: Optimal $T_{ON,PFM}$ various input and output voltages.

output voltages. Note that if it is assumed that the on-time for the best efficiency shown in Fig. 4.5 is used, then the maximum suppliable load current will be the half the associated $I_{L,pk}$ value in Fig. 4.4. This is depicted in the Fig. 4.6. The efficiency and the output voltage

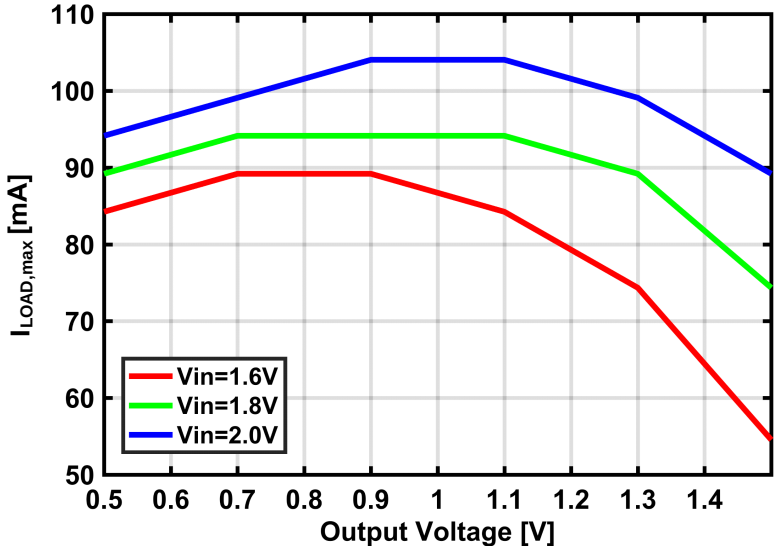


Figure 4.6: Maximum output load current with optimal $T_{ON,PFM}$.

ripple associated with the on-time in Fig. 4.5 are shown in Fig. 4.7 and Fig. 4.8.

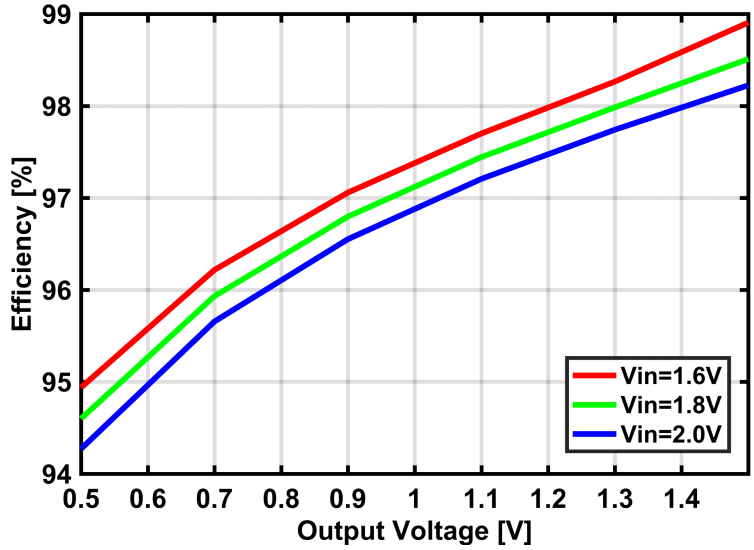


Figure 4.7: Efficiency with optimal $T_{ON,PFM}$.

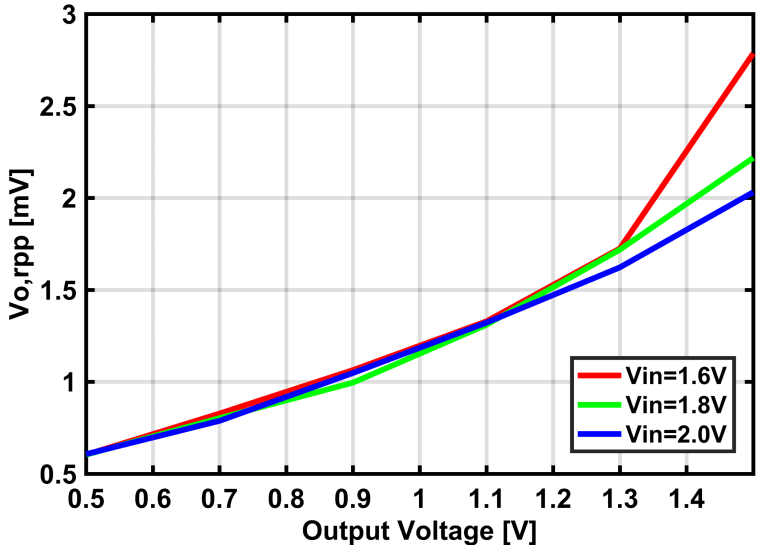


Figure 4.8: Output voltage ripple with optimal $T_{ON,PFM}$.

4.2 Proposed PFM Operation

Figure 4.9 shows the block diagram of the proposed PFM controller. It is composed of a comparator, zero crossing detector (ZCD), LUT, and finite state machine (FSM). The comparator compares the output voltage with the reference voltage and generates EN_{DRV} = high if the output voltage is lower than the reference voltage and generates EN_{DRV} = low unless otherwise. The ZCD detects when the inductor current becomes negative and forces

the driving node (V_{DRV}) of the output power stage to be high impedance. Finally, the FSM operated by a high-speed clock (CLK_{HS}) generates control signals for the output power stage to regulate output voltage. The state machine for the FSM is shown in Fig. 4.10. When

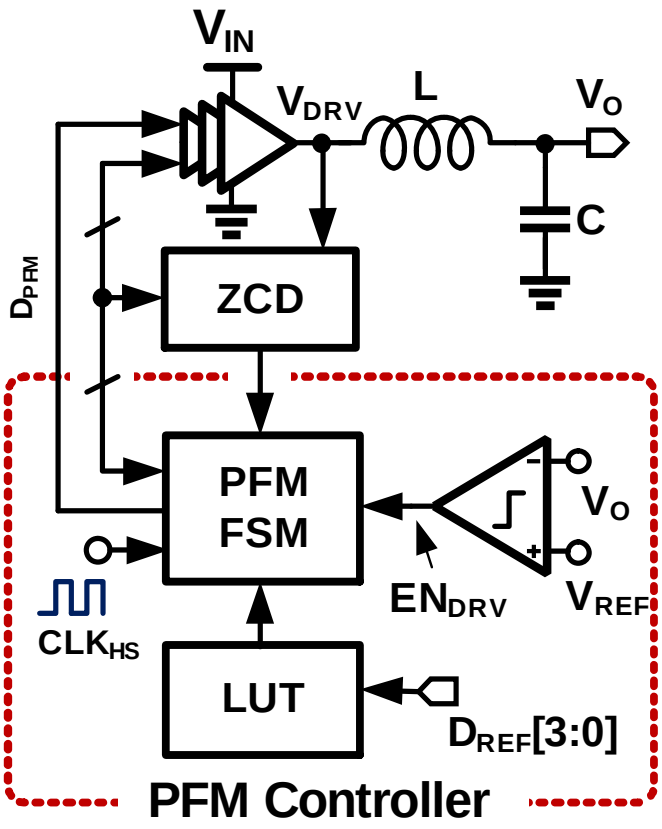


Figure 4.9: Proposed PFM controller.

the comparator generates EN_{DRV} = high, the FSM sets the output power stage high (D_{PFM} = high) for a given time period, $T_{ON,PFM}$, which is measured by counting the high-speed clock (CLK_{HS}). The optimal counting value (CNT_{OPT}), i.e., optimal on-time, for the best power conversion efficiency is provided by LUT assuming a system provides the information (D_{REF}) to the LUT, accounting for the input and the output voltages of the system. Once the counted value (CNT_{PFM}) reaches at CNT_{OPT}, the state machine checks again whether the output voltage is lower than reference voltage or not. If it is still lower (EN_{DRV} = high), the on-time is extended until the output voltage rises above the reference voltage (EN_{DRV} = low) to maintain the voltage regulation as depicted in Fig. 4.11. The extension of the on-time happens when the load current is higher than the maximum current that the given on-time

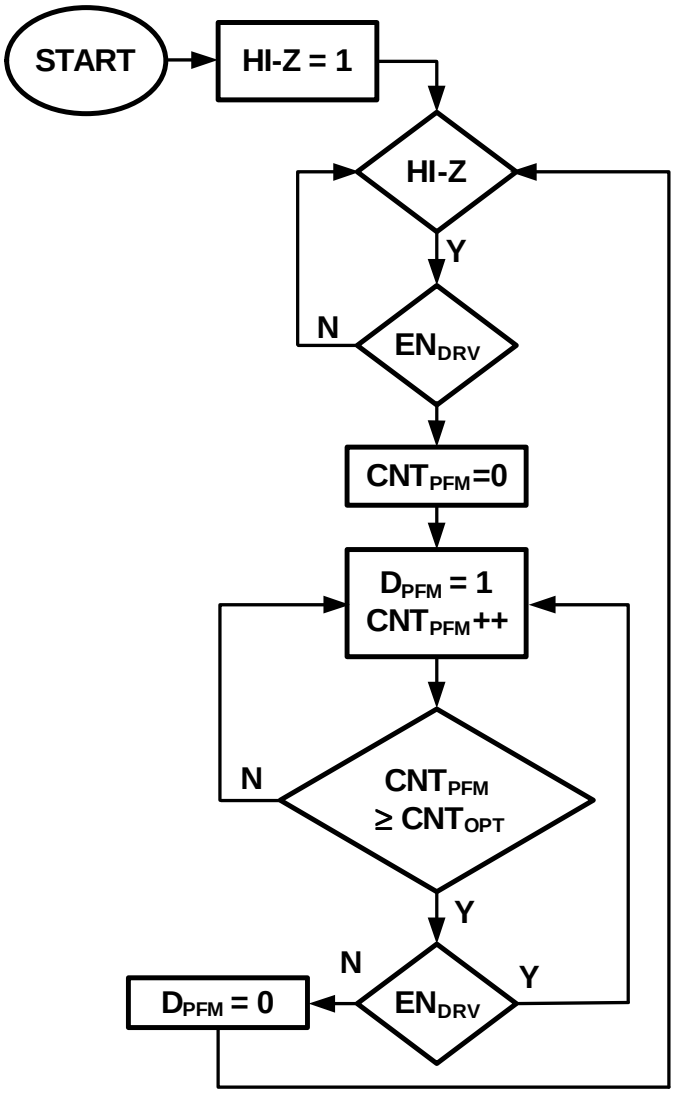


Figure 4.10: Finite state machine (FSM) for PFM control.

can supply as shown in Fig. 4.4. Compared to linear control of the switching frequency shown in [35], the proposed architecture provides the faster transient response because of the non-linear on/off operation of the control loop and the simpler circuit architectures at the expense of added digital FSM and high-speed clocks. Accordingly, this architecture can be more beneficial for the finer silicon processes where the power and the die area of the digital FSM can be scaled down proportionally.

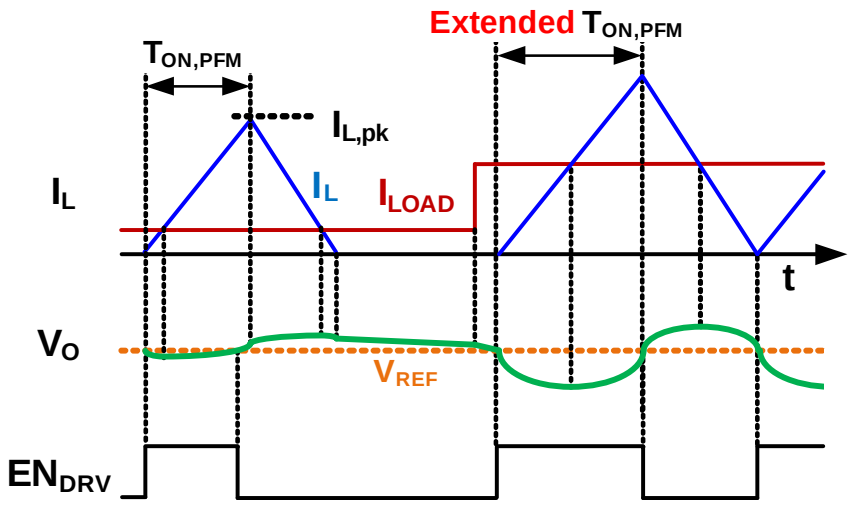


Figure 4.11: On-time extension in PFM mode.

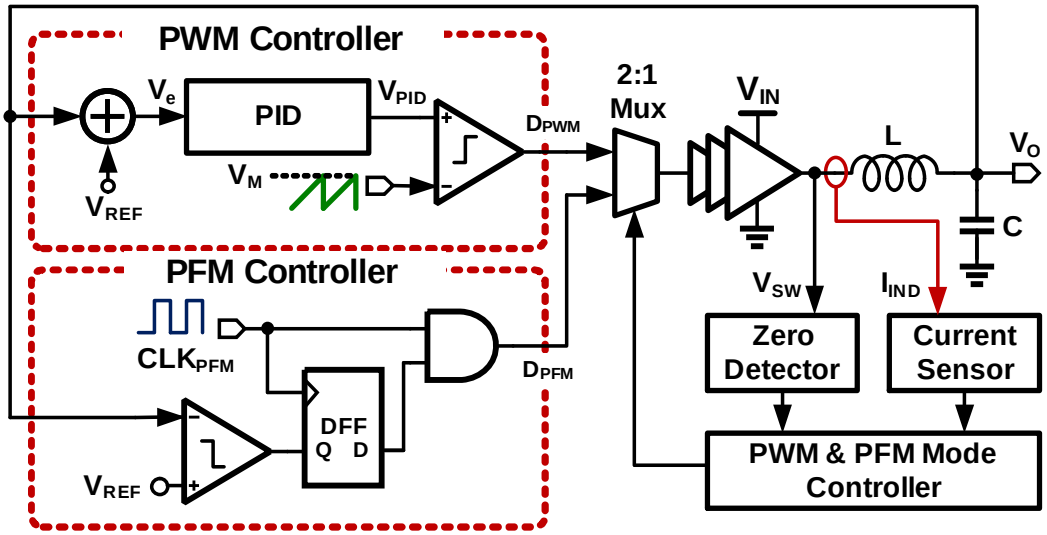


Figure 4.12: Combination of conventional PWM and PFM controllers.

4.3 Considerations on Transitions between PFM and PWM

Figure 4.12 shows the block diagrams of the combination of both voltage mode PWM and PFM controllers and Fig. 4.13 shows the voltage mode PID compensator in detail. First, PFM to PWM transition sequence is considered as shown in Fig. 4.14. Initially, the PWM controller (voltage mode PID compensator) is in off-state to save the static power of the controller while the output voltage is being regulated by PFM controller. When the output load (I_{LOAD}) rises to a value higher than a predetermined threshold value (I_{TH}) the transition

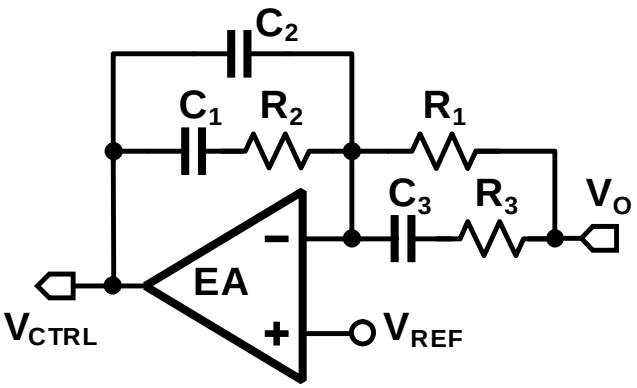


Figure 4.13: Conventional voltage mode PID compensator.

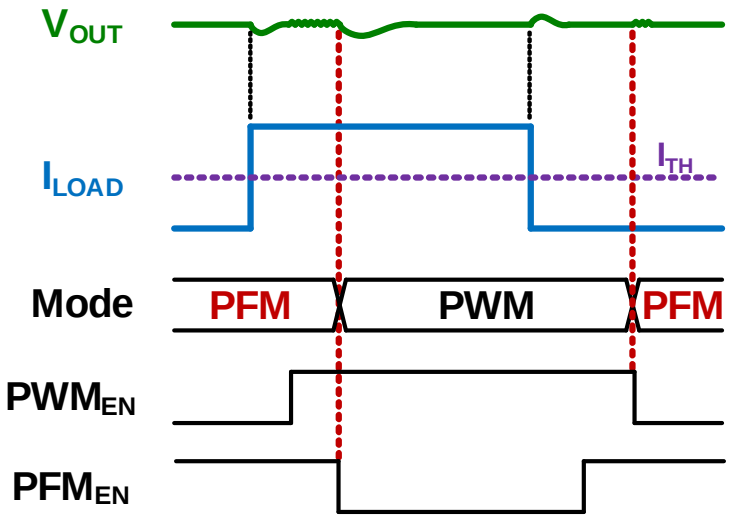


Figure 4.14: Transition sequence.

sequence from PWM to PFM is initiated. The PWM controller is turned on and then the mux control signal is toggled so that the output voltage begins to be regulated by the PWM controller. At the instance of the toggling the PID compensator in the PWM controller starts from an undefined status (i.e. V_{CTRL} node voltage). Accordingly, the duty-cycle (D_{PWM}) can be largely different from its steady-state value at the moment of the transition and it may take a significant amount of time to reach steady-state. This transition from PFM to PWM can deteriorate output voltage significantly, which severely restricts the ability to enter deep power saving states at the system level. Figure 4.15 shows the simulated results of the transition. In this simulation, V_{IN} is used for PWM modulation voltage (V_M). Accordingly, the steady-state V_{CTRL} value will be close to the target output voltage,

$V_{CTRL} = V_M \times D = V_{IN} \times \frac{V_O}{V_{IN}} = V_O$. The larger dfference between the initial value of the V_{CTRL} node voltage (V_{init}) and the steady-state value (1V) results in the larger output voltage error from its target value.

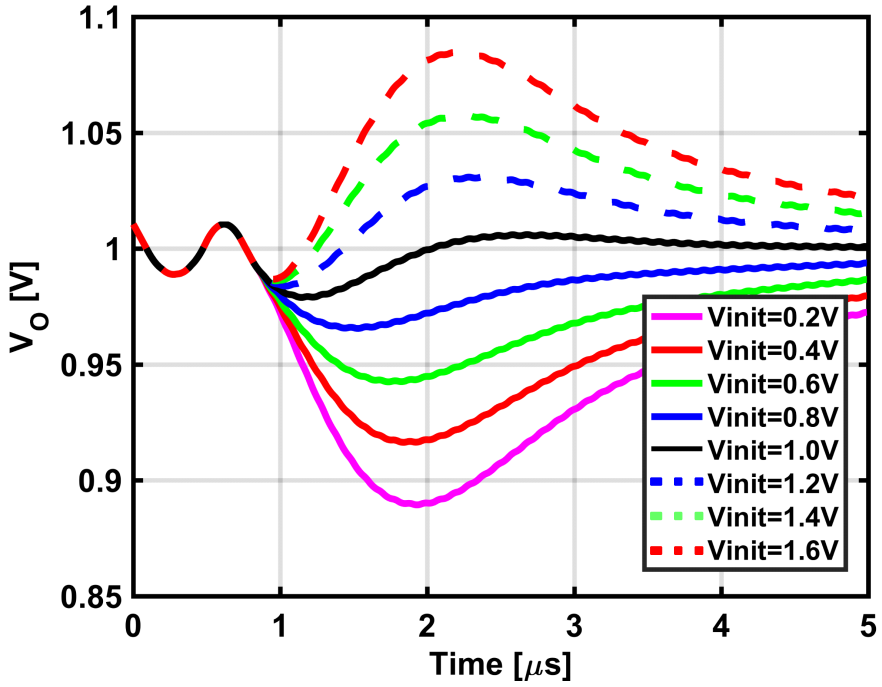


Figure 4.15: Transition simulation in conventional architecture.

The output voltage error can be minimized by presetting the state of the PWM controller close to its steady-state before making the mode transition as shown in the case of $V_{init} = 1V$ in Fig. 4.15. To do the presetting, the voltage mode PID controller in Fig. 4.12 needs to be modified to the architecture in Fig. 4.16. The modified PID controller has presetting switches so that the V_{CTRL} node voltage can be preset toV_{PRE} node voltage before the mode changes from PFM to PWM as shown in Fig. 4.17. Accordingly, output voltage error can be minimized by setting $V_{PRE} = V_M \times \frac{V_O}{V_{IN}}$.

While initializing the PWM control voltage in a voltage-mode controller can perform the presetting in the above manner, however, lack of an explicit signal that controls the duty-cycle makes it challenging to do the same in time-based controllers.

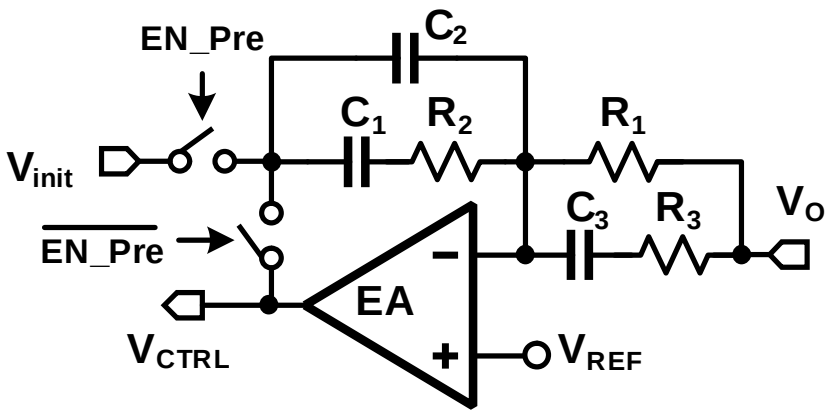


Figure 4.16: Modified voltage-mode PID compensator.

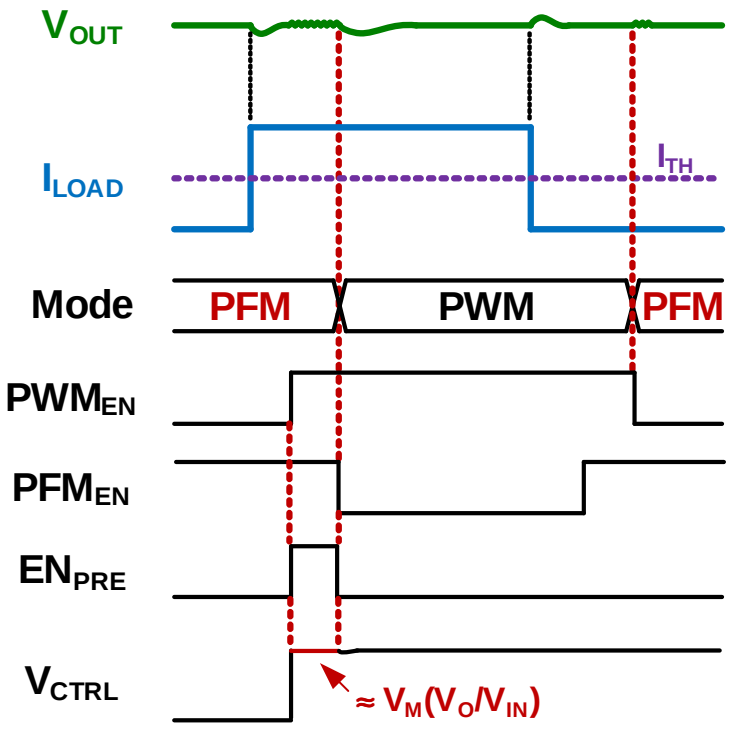


Figure 4.17: Timing diagram of presetting operation.

4.4 Proposed Transition Control in Time-Based PID Controller

Figure 4.18 shows block diagram of the proposed buck converter. It is composed of buck stage, time-based PWM and PFM controllers, and circuitry that performs seamless transition between PWM and PFM in accordance with I_{LOAD}. The converter operates in PWM for I_{LOAD} higher than user-specified threshold, I_{TH}, and in PFM when $I_{LOAD} < I_{TH}$. In

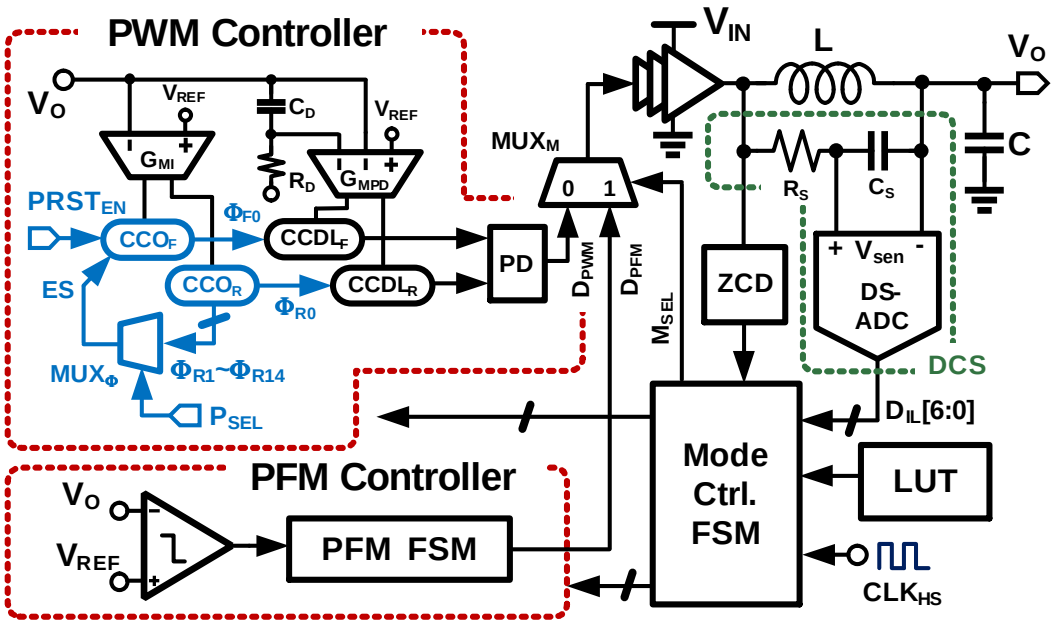


Figure 4.18: Proposed architecture.

the PWM mode, current controlled oscillators CCO_F and CCO_R provide integral control while the current controlled delay lines, $CCDL_F$ and $CCDL_R$, in conjunction with the CR (C_DR_D) filter, implement proportional + derivative control as explained in Chapter 2. A phase detector (PD) compares phase of $CCDL_F$ and $CCDL_R$ outputs and generates duty-cycle, D_{PWM}. In the PFM mode, a comparator and an inductor current zero crossing detector (ZCD) along with digital PFM logic modulate F_{SW} and the on-time of PFM pulse, D_{PFM}. The mode switching circuitry consists of digital current sensor (DCS) and mode control FSM that makes use of DCS outputs (D_{IL}) and generates PWM/PFM enable signals, PWM_{EN}/PFM_{EN}, along with the mode select signal M_{SEL}. PWM controller is completely turned off when the converter operates in PFM and vice versa to save power. DCS is implemented using a RC (R_SC_S) filter-based inductor current emulator followed by a low-power dual-slope analog to digital converter.

4.4.1 Steady-State Condition in Time-Based PID Compensator

The proposed mode switching technique is based on the observation that, in steady-state, feedback forces the frequency of two CCOs and the delay of two CCDLs to be equal, F_{CCO_F}

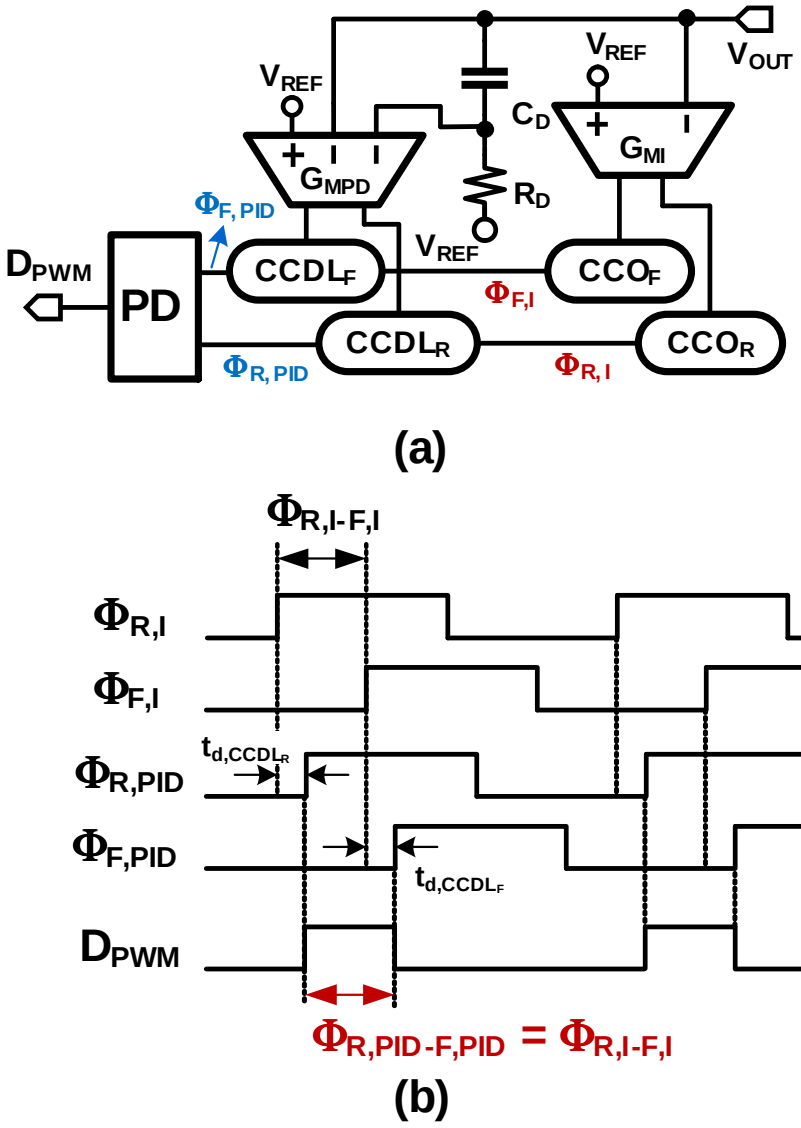


Figure 4.19: Steady-state condition of T-PID compensator.

$= F_{CCO_R}$ and $t_{d,CCDL_F} = t_{d,CCDL_R}$ as depicted in Fig. 4.19. Consequently, D_{PWM} is solely dictated by the phase difference ($\Delta\Phi = \Phi_{R,I} - \Phi_{F,I}$) between the two CCO outputs, namely, $D_{PWM} = \Delta\Phi/2\pi$. Hence, seamless switching from PFM to PWM can be accomplished by presetting $\Delta\Phi = D_{PWM} \times 2\pi$.

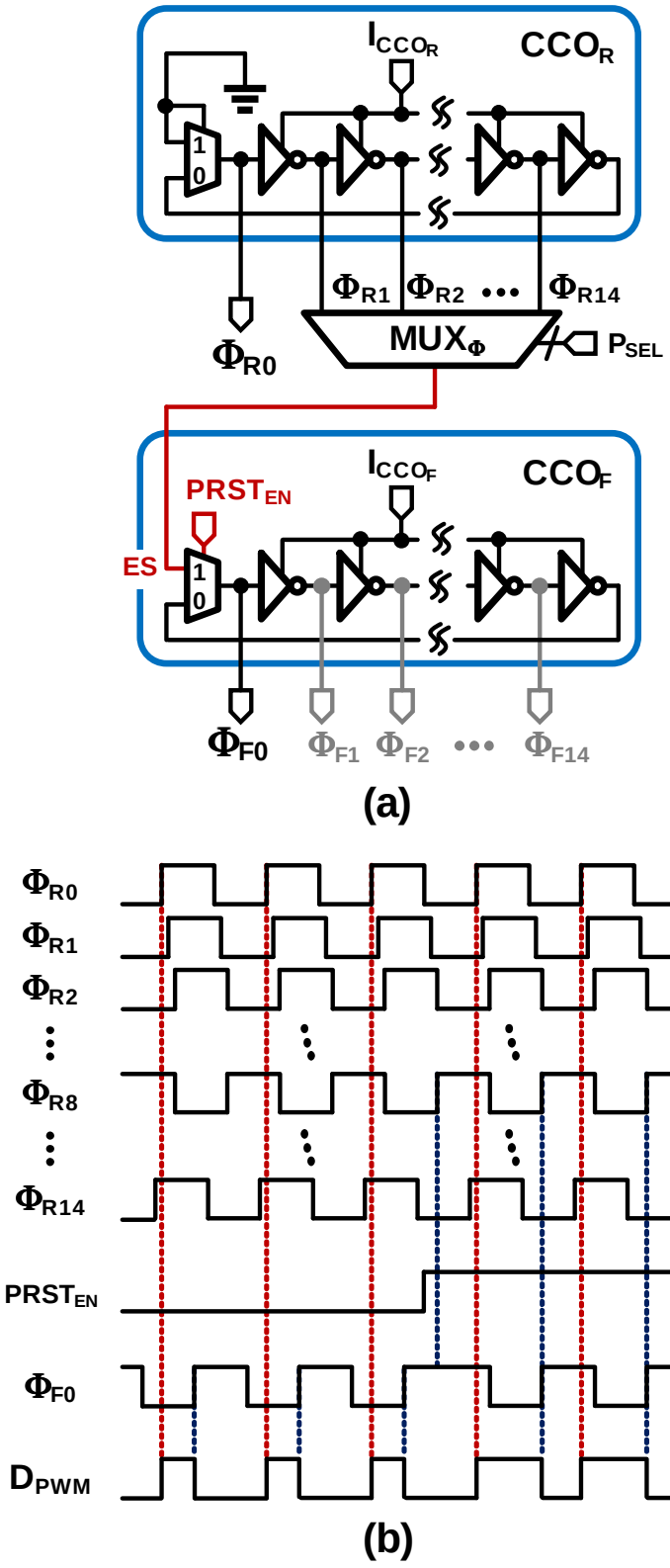


Figure 4.20: Proposed presetting operation of T-PID compensator.

4.4.2 Phase Presetting between Two VCOs

Figure 4.20 illustrates the proposed duty-cycle presetting technique for time-based controllers. Both CCO_R and CCO_F ring oscillators are converted to gated ring oscillators by adding a mux that selects between an external signal and feedback signal of the oscillator. When the external signal is selected, oscillator is open and its output phase is dictated by the external signal. Therefore, using one of the 15 phases ($\Phi_{R0} - \Phi_{R14}$) of CCO_R as the external signal input of CCO_F mux, CCO_F output phase, Φ_{F0}, can be set to the desired phase with a resolution of $2\pi/15$. For instance, when CCO_F phase is set by Φ_{R8} ($P_{SEL} = 8$) $\Delta\Phi$ equals π, which presets D_{PWM} close to 50%. Note that CCO_R always operates in the closed-loop oscillator mode because its mux control input is grounded.

Additionally, the reqiured resoultion of the phase outputs can be estimated by referring to Fig. 4.15. The sensitivity between output voltage error (ΔV_O) and preset voltage error ($\Delta V_{init} = |V_{init} - V_{REF}|$) can be approximated to:

$$S_{\Delta V_O/\Delta V_{init}} = \frac{\Delta V_O}{\Delta V_{init}} = \frac{\Delta V_O}{|V_{init} - V_{REF}|} \approx 0.155 \tag{4.10}$$

Assuming a constraint on output voltage error of 30mV during mode change, the required resolution (N_Φ) will be:

$$N_\Phi = V_M \times \frac{S_{\Delta V_O/\Delta V_{init}}}{0.03} \approx 9.5 \tag{4.11}$$

where V_M is the modulation voltage (see Fig. 4.12) and is equal to V_{IN} (1.8V) in the simulation shown in Fig. 4.15.

4.4.3 Transition Control between PFM and PFM

The mode switching control proceeds in the following sequence (see Fig. 4.21). Using the DCS output, mode control FSM detects when the I_{LOAD} crosses I_{TH}, and asserts PWW_{EN} and preset enable, $PRST_EN$, signals. While the converter continues to operate in the PFM, PWM_{EN} turns on the PWM controller and $PRST_{EN}$ initiates presetting of the phase difference between the two CCOs to nominally $\Delta\Phi_1 = D_1 \times 2\pi$, where D_1 is the desired duty-cycle in PWM. While presetting $D_{PWM} = D_1$ is necessary, it does not guarantee

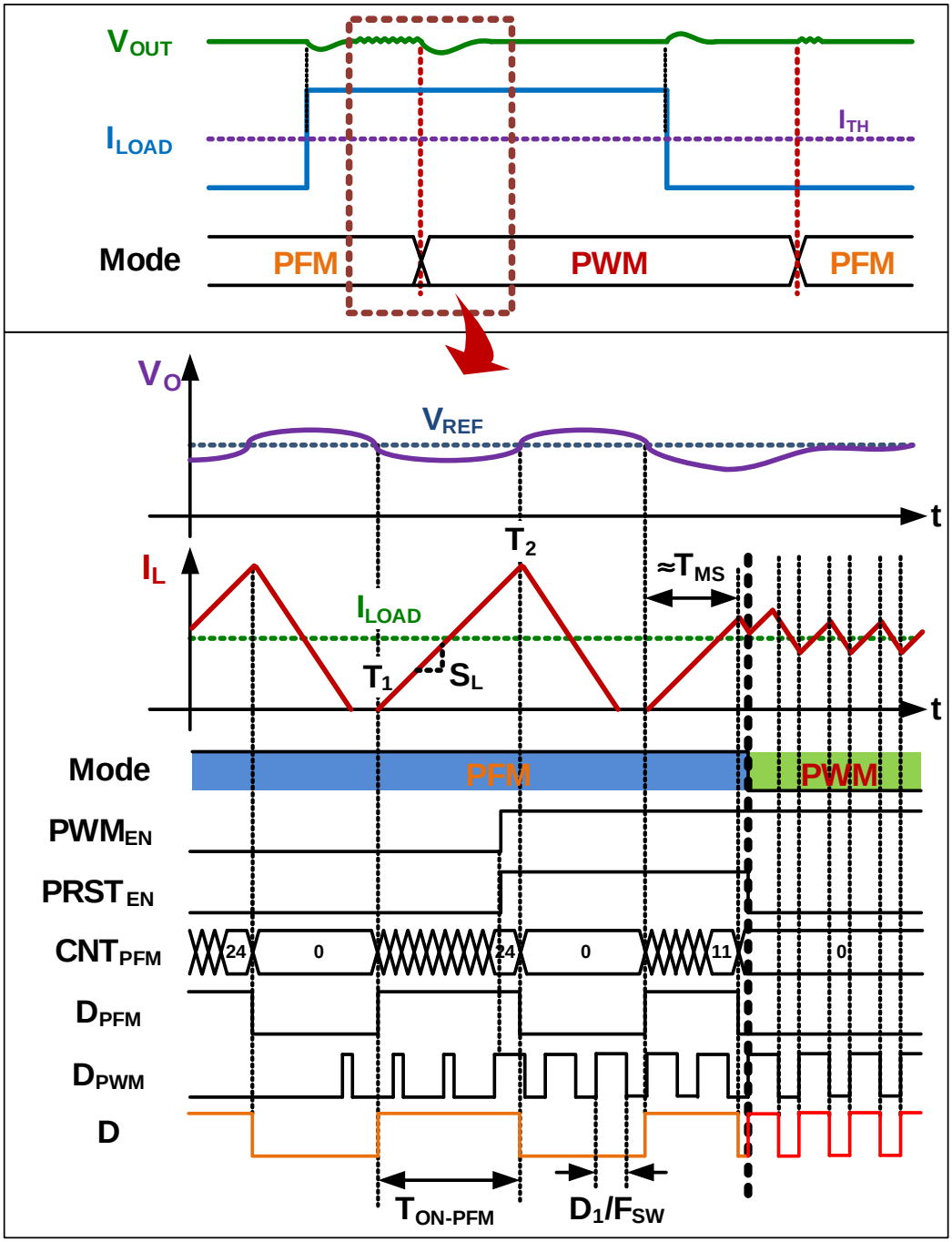


Figure 4.21: Transition sequence of proposed converter.

minimum perturbation of output voltage during the mode transition. For instance, as depicted in Fig. 4.21, if the mode switching takes place at t = T_1(or T_2) when I_L is farthest away from the I_{LOAD}, the output voltage will exhibit larger undershoot (or overshoot). To minimize this, converter has to be switched to PWM when I_L is in the vicinity of I_{LOAD}.

Because I_L always starts from zero at the beginning of every on-pulse in the PFM, its slope, $S_L = \Delta I_L/\Delta T = (V_{IN} - V_O)/L$, can be tabulated and stored in a look-up table (LUT) for various values of V_{IN}, V_O, and L. Using this, the instance at which $I_L \approx I_{LOAD}$ can be estimated to be $T_{MS} = I_{LOAD}/S_L$. In the prototype, the estimated T_{MS} is applied to the on-time of PFM pulse by a counter (CNT_{PFM}) that begins to count the number of clock cycles from the start of on-time until it reaches the target count of $[T_{MS}/T_{CK}]$, where T_{CK} is the period of the counter clock. For example, with V_{IN}=1.8, V_O=1V, L=220nH, T_{CK} = 10ns, and I_L = 400mA, the mode control FSM asserts $M_{SEL} = 1$ (see Fig. 4.18) and triggers transition to PWM when the counter reaches 11. At this point, the mode transition is complete and the PWM controller corrects any residual output voltage error and continues to operate in PWM mode until the I_{LOAD} falls below I_{TH}. Note that PWM to PFM transition occurs rapidly because PFM comparator turns on in a few μs and PFM controller regulates V_O by instantly providing PFM on-pulse if V_O is lower than V_{REF}.

4.5 Experimental Results

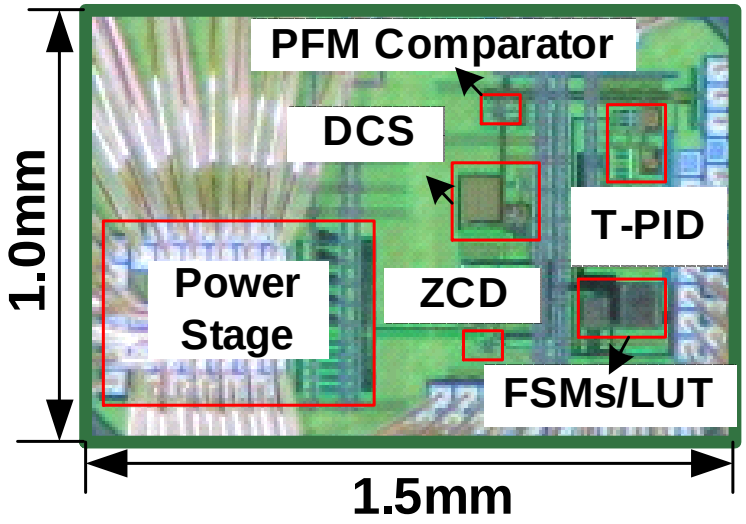


Figure 4.22: Die photo.

The proposed PWM/PFM buck converter implemented in a 65nm CMOS process occupies an active area of 0.14mm^2 as shown in Fig. 4.22 and is packaged in 60-pin QFN package.

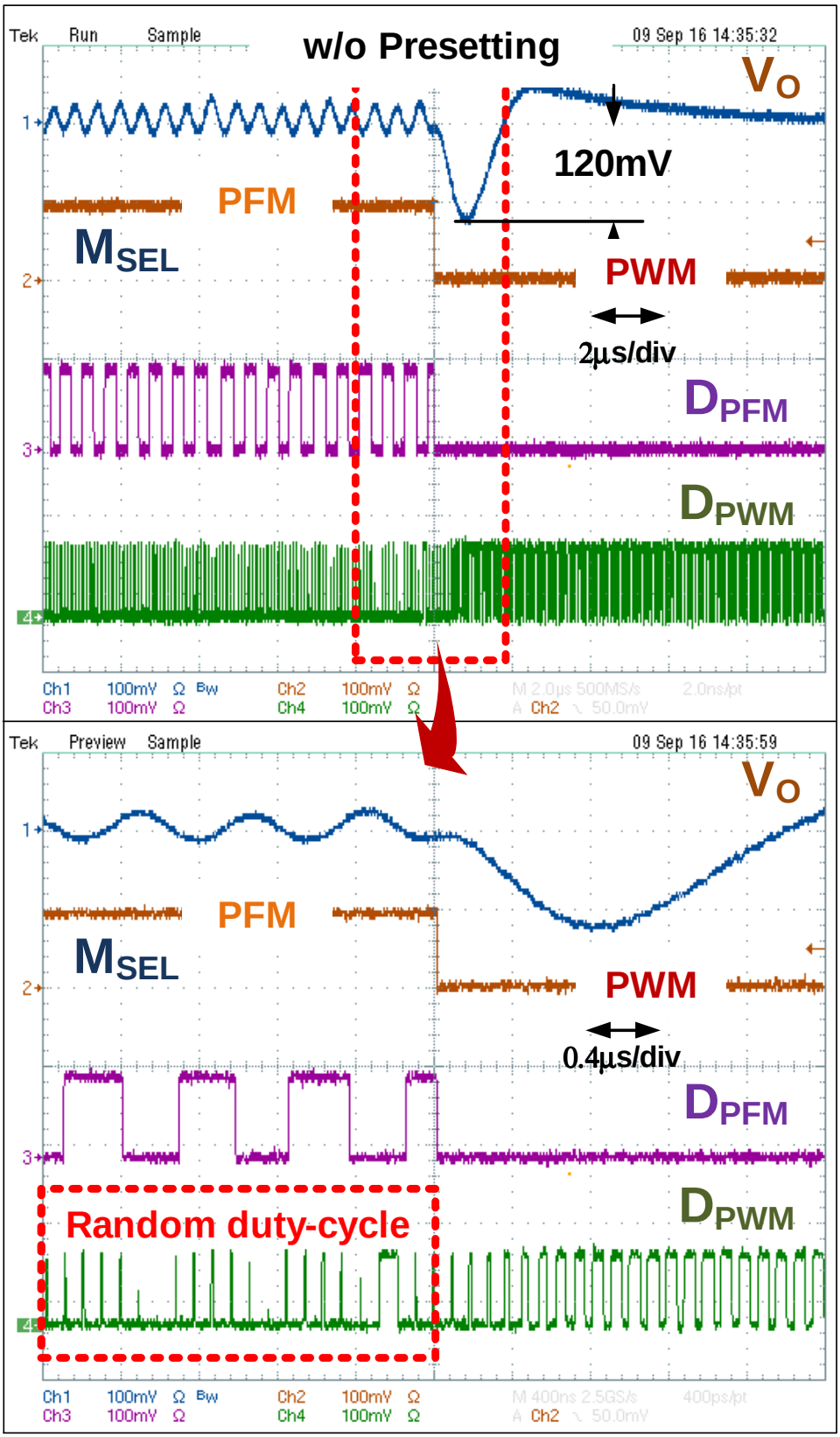


Figure 4.23: Transition without presetting operation.

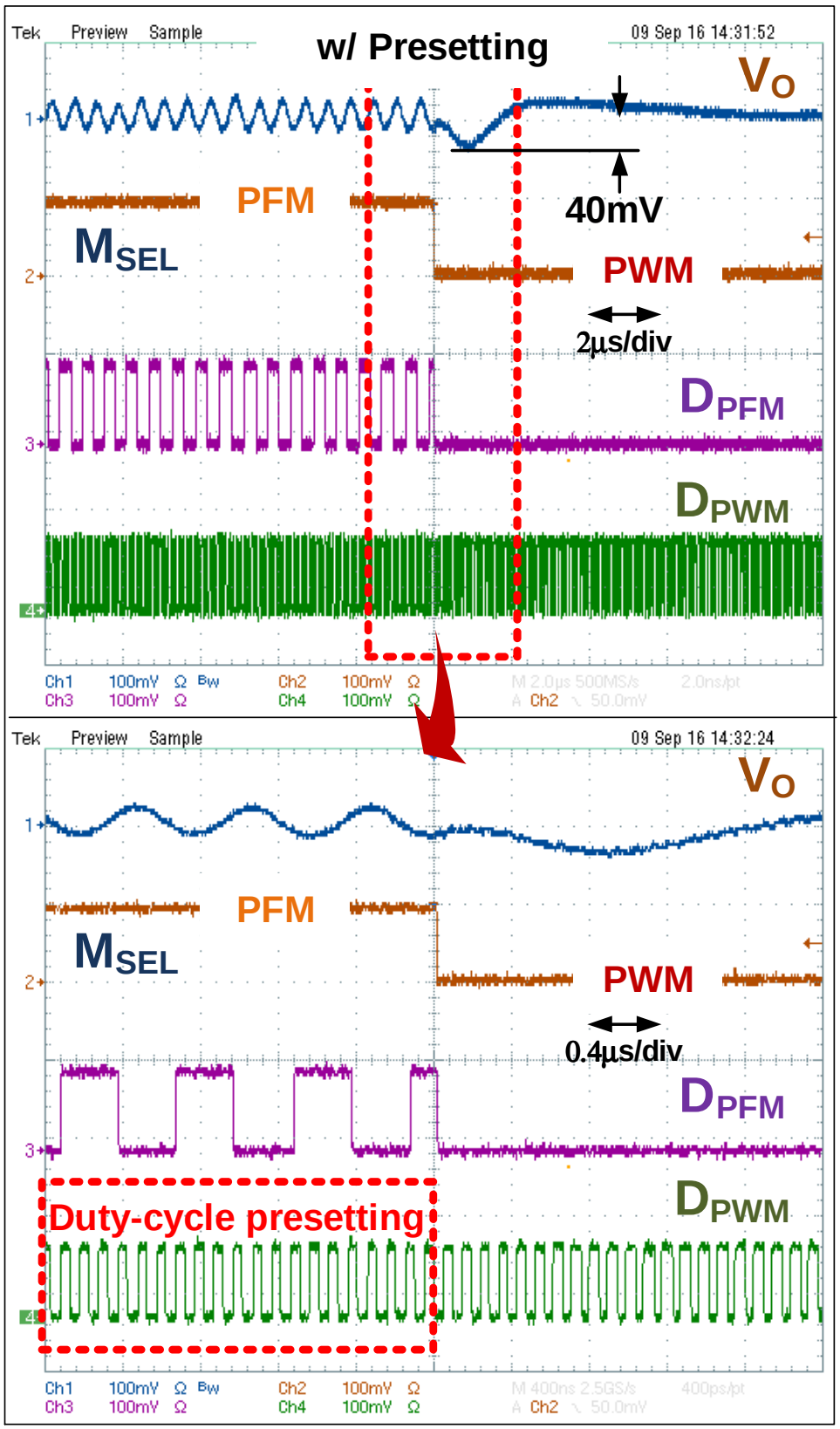


Figure 4.24: Transition with presetting operation.

The converter regulates output from 0.5-1.5V from an input voltage of 1.8V while consuming about 45μA quiescent current at F_{SW} = 10MHz in PWM and about 75μA quiescent current in PFM. Figure 4.23 and Fig. 4.24 show the measured waveforms during PFM to PWM transition with and without the proposed automatic presetting, respectively. Presetting decreases output error voltage from 120mV to 40mV. The measured PWM/PFM waveforms (D_{PWM}/D_{PFM}) also clearly demonstrate the presetting behaviors. Figure 4.25 shows

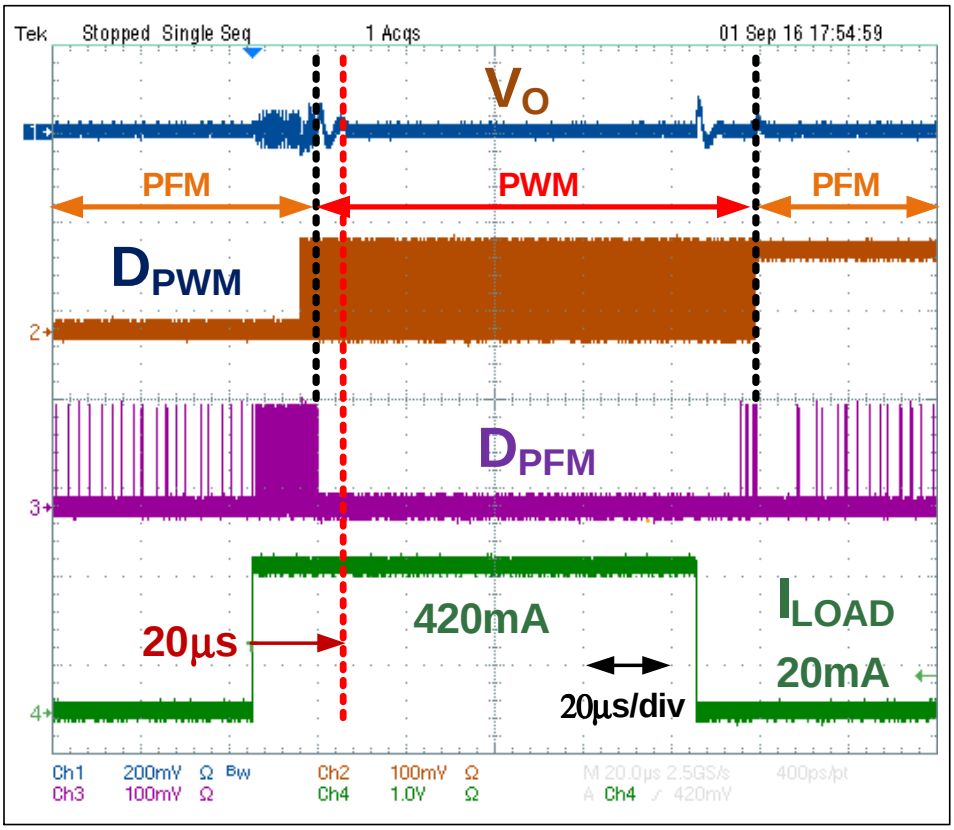


Figure 4.25: Transition operation of the prototype converter.

the converters mode transition operation when the load changes from 20mA to 420mA and vice versa. The mode transition is accomplished within about 20μs. The measured peak efficiency is 90% and the efficiency is above 80% over 2mA to 800mA I_{LOAD} range as shown in Fig. 4.26.

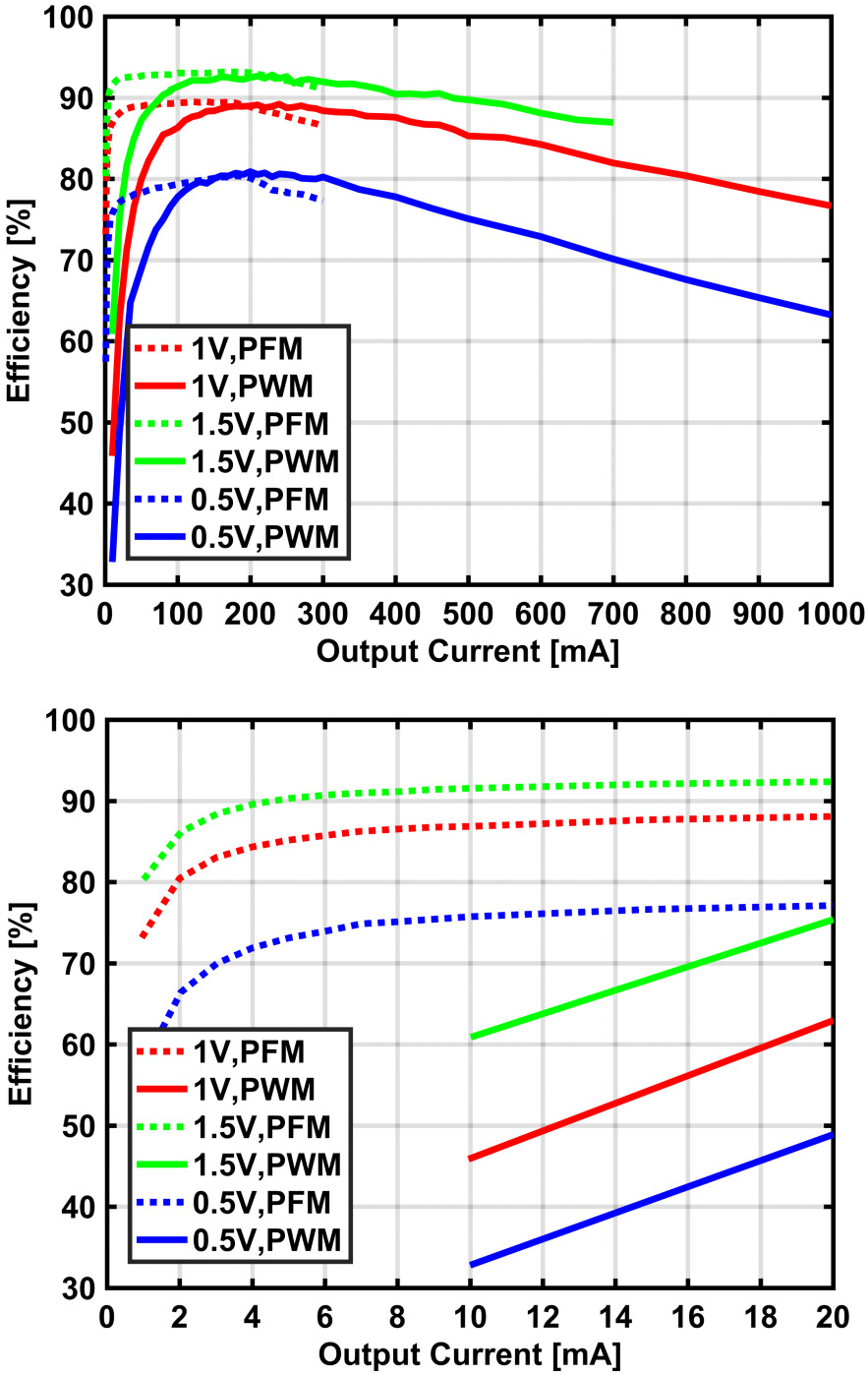


Figure 4.26: Measured efficiency.

CHAPTER 5

CONCLUSION

Using time as the processing variable, the proposed time-based control techniques for DC-DC converters combine the advantages of conventional analog and digital controllers. It operates with CMOS-level digital-like signals but without adding any quantization error. Using simple circuits such as ring oscillators, delay lines, and flip-flops, a time-based controller eliminates the need for wide bandwidth error amplifier, PWM block in analog controllers or high-resolution ADC and digital PWM block in digital controllers. As a result, it can be implemented in small area and with minimal power consumption. The time-based single-phase buck converter was fabricated in a 180nm CMOS process, the prototype buck converter occupies an active area of 0.24mm^2, of which the controller occupies only 0.0375mm^2. Its operation is verified over a wide range of switching frequencies (10-25 MHz) while providing output voltages between 0.6V and 1.5V from 1.8V input voltage. With a 500mA step in the load current, the output settles within 3.5μs and the reference tracking bandwidth is measured to be about 1MHz. The prototype converter consumes a quiescent current of only 2μA/MHz and achieves better than 94% peak efficiency. A high F_{SW} time-based multi-phase buck converter was also proposed for higher output power. By combining a highly digital multi-phase generator (MPG) with a time-based PID compensator (T-PID) that operates with CMOS-level digital-like signals, the proposed multi-phase converter provides accurately matched duty-cycles without adding any quantization error. The simple generation of highly matched duty-cycles enables achieving high efficiency by eliminating the need for complex current sensing and calibration circuit for active current sharing or high-resolution analog-to-digital converter (ADC) and digital PWM for passive current sharing. As a result, it can be implemented in small area and with minimal power consumption while operating at high F_{SW}. Additionally, FLL and CSD were proposed so as to mitigate VCO free-running

frequency mismatch induced output voltage offset and to increase the operating range of the output voltage. Experimental results obtained from the prototype four-phase converter indicate peak efficiency of 87% while consuming only 90μA at 30MHz switching frequency. Finally, a 10MHz buck converter with enhanced light load efficiency was presented by combining time-based PWM control with PFM. It also achieves seamless transition between PWM and PFM which provides the freedom of exchanging the control mode between PFM and PWM which greatly facilitates system power management. Fabricated in a 65nm CMOS, the prototype achieves 90% peak efficiency and $>$ 80% efficiency over I_{LOAD} range of 2mA to 800mA. V_O changes by less than 40mV during PWM to PFM transitions.

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