COMPARATIVE ANALYSIS OF ANALOG LDO DESIGN

BY

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THESIS

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ABSTRACT

The presented research analyses different topologies of low dropout (LDO) regulator, mostly focusing on different frequency compensation schemes and power supply rejection analysis. This thesis discusses different analog LDO topologies and analyzes how they achieve stability using small signal analysis and related equations. The power supply rejection (PSR) of a different error amplifier and pass device has been analyzed and concluded that a Type-B amplifier with n-channel metal oxide semiconductor field effect transistor (MOSFET) output stage or a Type-A amplifier with p-channel MOSFET (PMOS) output stage yields the best PSR. Digital LDO regulator topologies have also been discussed. The digital LDO regulator is intriguing due to its low power and synthesizability, but it suffers from coarse voltage regulation and poor PSR compared to the analog LDO regulator.

ACKNOWLEDGMENTS

I would like to thank my advisor, Professor Pavan K. Hanumolu, for providing great support throughout my academic research career. He has been guiding me with exceptional insight and passion. I would like to thank my fellow graduate students in the same research group. Thanks to Tejasvi Anand, Seong-Joong Kim, Daniel Coombs, and Braedon Salz for the help in coursework and research projects.

Finally, I would like to thank my family and my girlfriend. Thank you for the support and care.

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CHAPTER 1: INTRODUCTION

Power management has become an important issue in modern circuit design. While switched mode power converters are used between power-rail supply (110 V) and on-chip supply (1-5 V), linear regulators are used to reduce the noise further and generate the desired voltage level for different blocks. LDO regulator falls into a class of linear voltage regulator that operates at a relative low voltage across the pass transistor.

The presented research analyses different topologies of LDO regulator, mostly focusing on different frequency compensation schemes and power supply rejection analysis. Pole locations are calculated using small signal analysis. Conventional LDO regulator requires a large output capacitor that allows for good stability with reasonable power supply rejection. Large external capacitors increase the number of pin counts and take up valuable board space. Thus, recent research focuses on capacitor less LDO regulators which are more suitable for SoC applications.

Digital LDO regulator topologies have also been discussed. Digital LDO regulator is intriguing due to its low power and synthesizability but suffers

from coarse voltage regulation and poor power supply rejection (PSR) compared to the analog LDO regulator.

CHAPTER 2: LDO REGULATOR METRICS

Linear voltage regulators can be categorized into two different topologies: conventional linear voltage regulators and LDO regulators. The main difference between these two types is in the pass transistor and the dropout voltage. An LDO regulator uses common source configuration for the pass transistor while the linear voltage regulator uses a source follower or Darlington pair. This allows the dropout voltage of the LDO regulator to be as low as 0.1 without pushing the pass element into saturation.

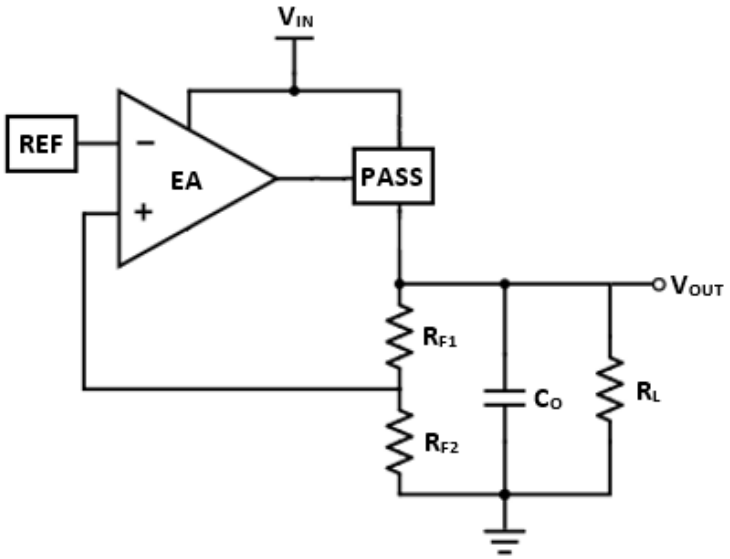

Figure 2.1: LDO block diagram

The block diagram in Figure 2.1 shows how the LDO regulator regulates the output voltage. A simple LDO regulator consists of a bandgap circuit, an error amplifier, a pass transistor, and feedback resistors. V_{OUT} refers to the

output voltage of the regulator and V_{REF} is the reference voltage from the bandgap circuit. The feedback adjusts the impedance of a pass transistor such that V_{OUT} is equal to V_{REF}. This allows the feedback to regulate the output voltage regardless of load current. More specifically, the output voltage is sensed through the feedback resistors and compared with a fixed reference voltage that is generated by the bandgap circuit. An error amplifier then feeds an error signal to the pass device so that the impedance of the pass device changes. The negative feedback loop causes the impedance of the pass device to change until the scaled V_{OUT} is equal to V_{REF}. For the case of a metal–oxide–semiconductor field-effect transistor (MOSFET) as a pass device, an error signal is the gate voltage of a MOSFET and it needs to stay in the linear/saturation region to regulate the output voltage.

Ideally LDO regulators provide constant output voltage regardless of the supply voltage noise or the load current variations. Performance metrics of LDO regulators can be categorized into steady-state, dynamic-state, and high-frequency specifications.

The dropout voltage is the minimum voltage across the pass device to

maintain regulation. The dropout voltage depends on pass device parameters, minimum supply voltage, and the maximum load current. The dropout voltage typically ranges from 0.1 to 0.5 V.

$$V_{DROPOUT} = V_{DSAT} = \sqrt{\frac{2I_{MAX}}{\mu_P C_{OX} W/L}} \tag{2.1}$$

An approximate value of the dropout voltage for a MOSFET is given in Equation (2.1). This equation can be used to get approximate transistor sizes when the maximum load current and the dropout voltage are specified.

The static parameter also includes line regulation and load regulation. General equations for line regulation and load regulation are derived from the transfer functions of a MOSFET-based LDO regulator. Transfer functions are found using Mason's gain rule.

$$H = \frac{\sum_j M_j \Delta_j}{\Delta} \tag{2.2}$$

$H =$ transfer function of the system

$j =$ index number of a forward path from input to output

$M_j =$ gain of forward path j from input to output

$\Delta = 1 - \sum$ (all loop gains)

$+ \sum$ (nontouching loop gains multiplied two at t time)

$- \sum$ (nontouching loop gains multiplied three at t time)

$+ \sum$ (nontouching loop gains multiplied four at t time) …

$\Delta_j = \Delta$ calculated after excluding all feedback loops that intersect with forward path *j*

Using the Mason's gain rule, transfer function for V_{OUT} due to V_{IN} can be calculated as follows. Figure 2.2 shows the signal flow for an LDO regulator.

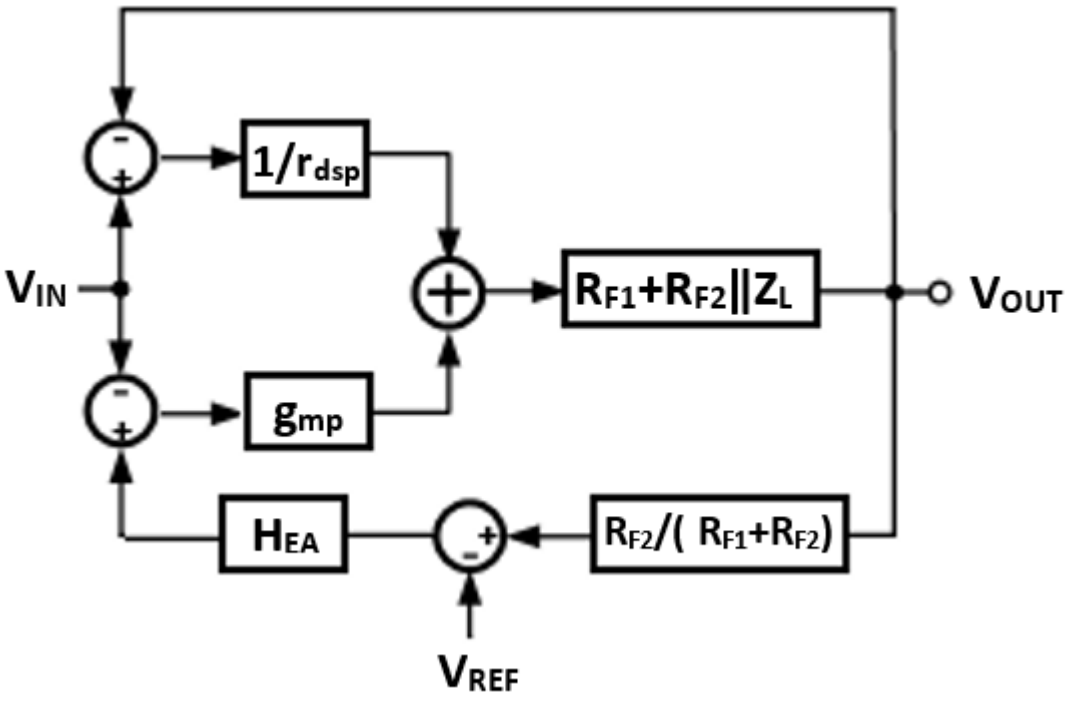

Figure 2.2: LDO regulator signal flow

$$\frac{V_{OUT}}{V_{IN}} = \frac{1 + g_{mp} r_{dsp}}{1 + \left(A_{EA0} \cdot g_{mp} \cdot r_{dsp} \cdot \beta + \frac{r_{dsp}}{R_{FL}} \right)} \tag{2.3}$$

g_{mp} is the pass transistor transconductance, r_{dsp} is on-resistance of the MOSFET, A_{EA0} is error amplifier gain, and β is the feedback factor.

Line regulation measures the ability to maintain desired output voltage with varying input voltage. This reflects the deviation at steady-state. An ideal voltage regulator maintains constant output voltage with changing input voltage. Figure 2.3 shows ideal behavior of an LDO regulator.

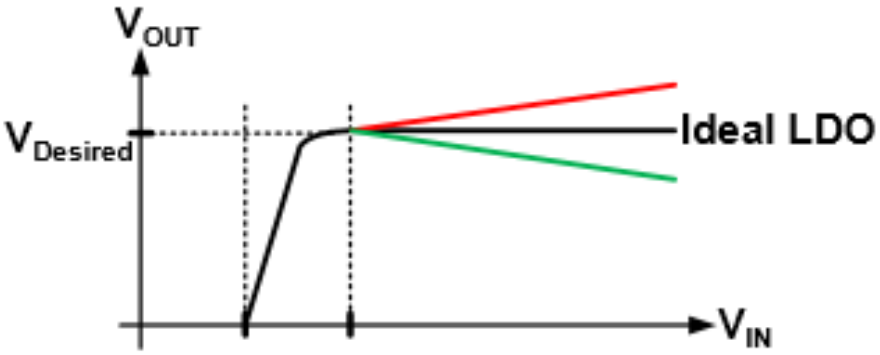

Figure 2.3: Line regulation

Line regulation is approximated to be L_R in Equation (2.4), which is directly taken from Equation (2.3).

$$L_R = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{1 + g_{mp} r_{dsp}}{1 + \left(A_{EA0} \cdot g_{mp} \cdot r_{dsp} \cdot \beta\right)}$$
$$\Rightarrow L_R \approx \frac{1}{\beta A_{EA0}} \tag{2.4}$$

Since an ideal voltage regulator should have a line regulation of 0, error amplifier gain has to be sufficiently large to suppress the output change due to input voltage.

Load regulation measures LDO regulator's ability to maintain a desired output voltage with a varying output load current. This also reflects the deviation at steady-state.

$$LR_{load} = \frac{\Delta V_O}{\Delta I_O} = \frac{r_{op}}{1 + A\beta} \tag{2.5}$$

The output impedance of the pass transistor is r_{op} and $A\beta$ is the loop gain. The load regulation can be improved by decreasing the output resistance or increasing the loop gain.

Dynamic state specifications of LDO regulators define the maximum allowable output variation during load and line transience. An LDO regulator must specify its transient response time to show its regulation

capability. Line transient and load transient responses are both dynamic metrics unlike load regulation or line regulation. Line transient response is a measure of an LDO regulator's ability to maintain output voltage with varying input voltage. Load transient response is a measure of an LDO regulator's ability to maintain output voltage with a varying output load current. The load transient response is a function of the maximum load current, the output capacitance, and the bandwidth of the LDO regulator. It can be improved by having a higher value of output capacitance and a higher bandwidth.

Power supply rejection (PSR) shows the LDO regulator's ability to reject the output voltage variation due to the input voltage change. This is similar to line regulation but the whole frequency domain is considered. Most LDO regulator designs specify PSR due to its importance in practical uses. The type of an error amplifier and type of a pass device tend to be the largest contributors of PSR, which will be discussed later in Chapter 4. Large output capacitance also improves PSR.

Power efficiency of an LDO regulator is mainly affected by the quiescent current, load current, output voltage, and input voltage.

$$\text{Power efficiency: } \eta = \frac{I_{OUT}V_{OUT}}{(I_{OUT} + I_Q)V_{IN}} \tag{2.6}$$

The quiescent current is mainly caused from the bias current in the reference generator, error amplifier, and feedback resistors. Unless the load current and quiescent current have comparable values, power efficiency becomes only dependent on the output voltage and the input voltage. This can only be improved by having a large pass transistor, but it would cause slewing due to large gate capacitance.

CHAPTER 3: ANALOG LDO COMPENSATION SCHEME

The conventional linear regulator has high dropout voltage but it is inherently stable due to its low output impedance. The dominant pole is generated from the output node of an error amplifier, while the second pole is pushed to much higher frequency due to low output impedance. However, the LDO regulator has a higher output impedance due to common source configuration. There has to be a compensation measure to guarantee stability in the form of pole splitting or pole-zero cancellation. Many publications have found different ways of maintaining the stability [1]. This thesis analyzes and evaluates each compensation schematics.

A typical uncompensated LDO regulator is shown in Figure 3.1. Approximate pole zero locations for a typical LDO regulator that has not been compensated are shown in Figure 3.2 along with the equations for each pole and zero in Equation (3.1), Equation (3.2), and Equation (3.3).

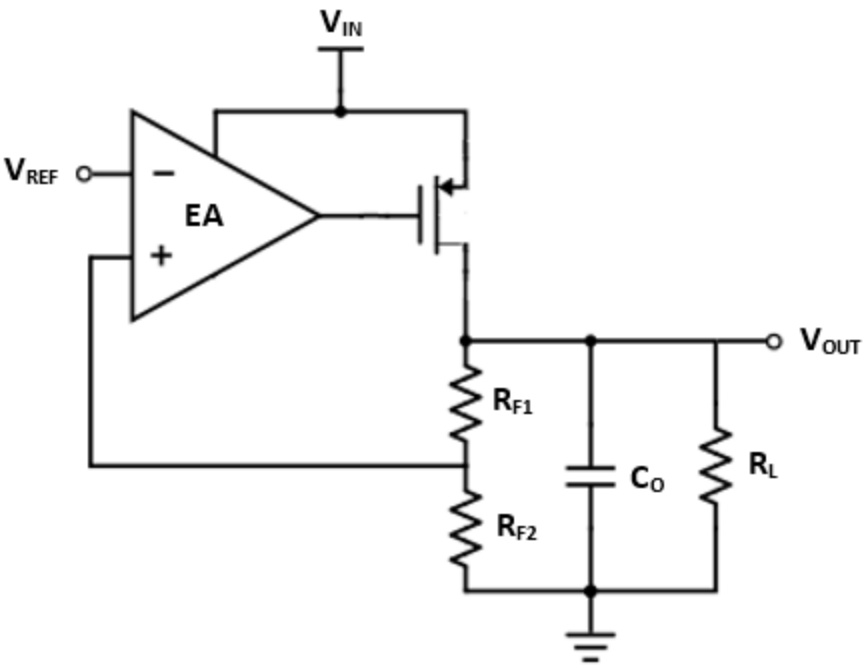

Figure 3.1: Uncompensated conventional LDO

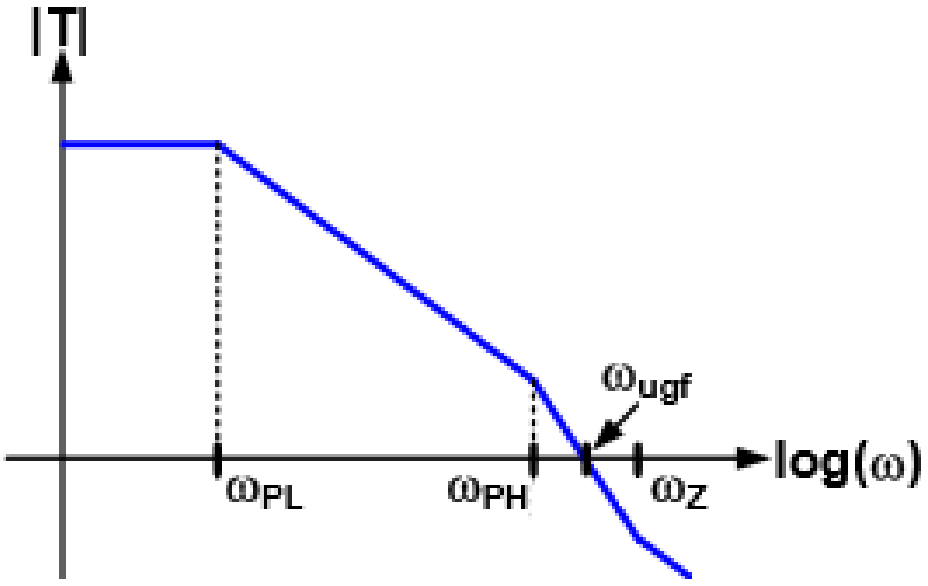

Figure 3.2: Approximate pole-zero locations for uncompensated LDO

$$\omega_{PL} \approx \frac{1}{R_{OUT} C_O} \tag{3.1}$$

$$\omega_{PH} \approx \frac{1}{R_{OEA} \cdot [C_1 + g_{mp} \cdot R_{OUT} \cdot C_{gdp}]} \tag{3.2}$$

$$\omega_Z \approx \frac{g_{mp}}{C_{gdp}} \tag{3.3}$$

The dominant pole ω_{PL} is generated from the output node of the LDO regulator. The second dominant pole ω_{PH} is located close to the dominant pole and stability cannot be guaranteed. A conventional LDO regulator uses equivalent series resistance (ESR) of the output capacitor to produce zero and maintain stability. Figure 3.3 shows how ESR is implemented. However, ESR also creates another pole and its location heavily depends on the ESR value. Decrease in ESR causes zero to move to the right causing the phase margin to decrease, and increase in ESR causes the new pole to

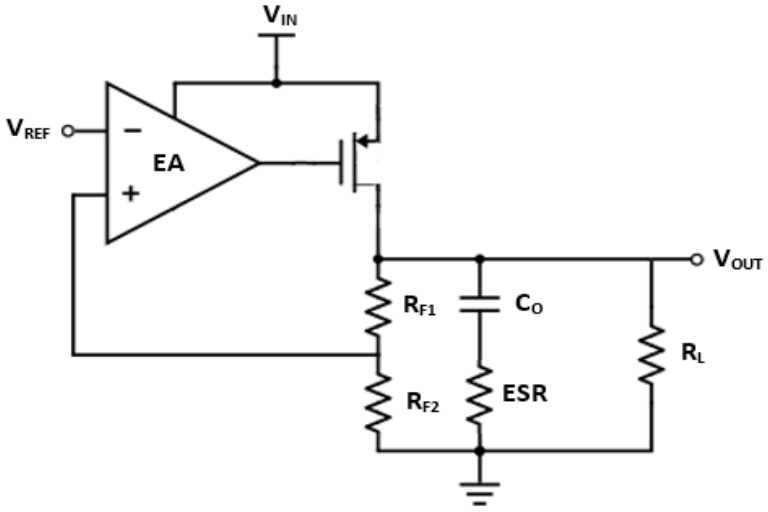

Figure 3.3: Conventional LDO with ESR attached

move to the left causing instability. Thus, researchers have strived to find different ways of introducing zero without using ESR.

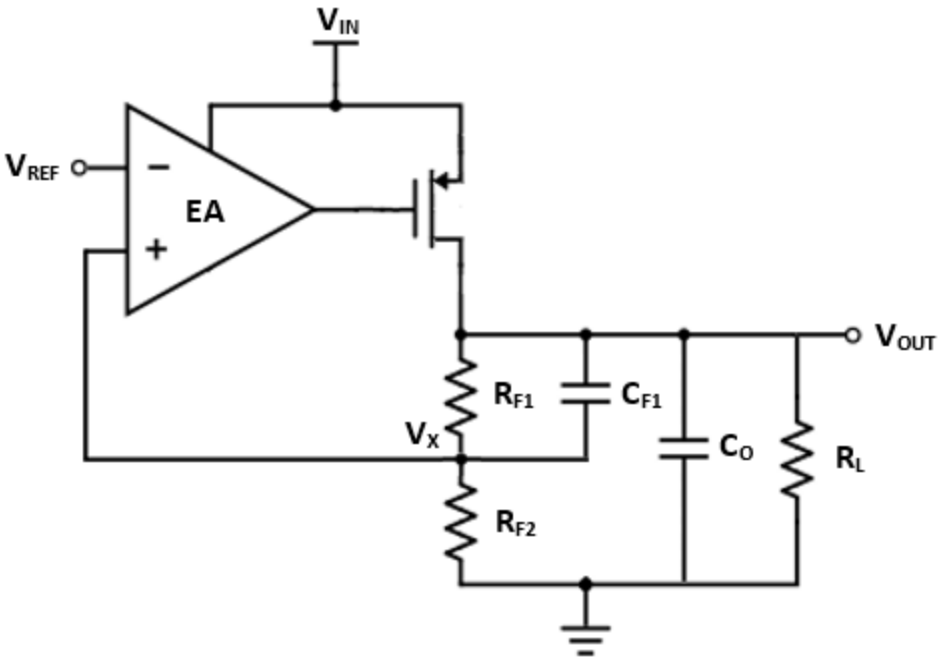

Figure 3.4: Conventional LDO with a feed-forward capacitor

Chava and Silva-Martinez report a frequency compensation scheme that uses a feed-forward capacitor to produce a zero to guarantee stability [1]. This scheme generates a zero internally instead of using ESR to generate a zero. A capacitor is added between the output node and V_X, as shown in Figure 3.4, to provide a bypass path for the loop gain.

$$\omega_{ZF} = \frac{1}{R_{F1}C_{F1}} \tag{3.4}$$

$$\omega_{PF} = \frac{1}{(R_{F1} \parallel R_{F2})C_{F1}} \tag{3.5}$$

This produces a pole-zero pair in Equation (3.4) and Equation (3.5). Although the zero is generated as required, the pole ω_{PF} is not far from the zero and needs to be removed. Figure 3.5 shows how a feed-forward capacitor is implemented in the circuit.

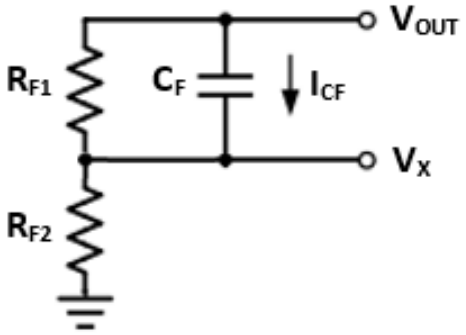

Figure 3.5: Feed-forward capacitor

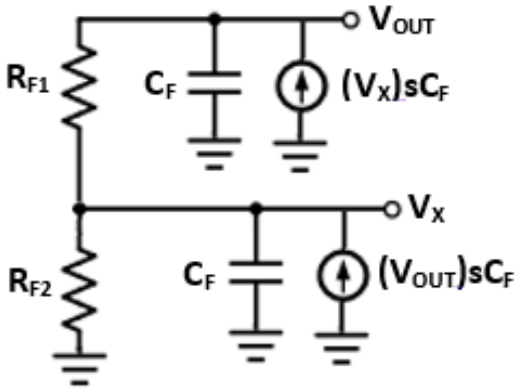

Figure 3.6: Ground capacitor and VCCS equivalent to feed-forward capacitor

Figure 3.6 shows how C_F in Figure 3.5 can be realized as two frequency-dependent voltage controlled current source (VCCS) with ground capacitors.

$$V_{OUT}\left(sC_F + {}^{1}/_{R_{F1}}\right) = V_X({}^{1}/_{R_{F1}} + {}^{1}/_{R_{F2}} + sC_F) \quad (3.6)$$

Kirchhoff's current law (KCL) equation based on Figure 3.5 is derived in Equation (3.6). The $V_X(sC_F)$ term in Equation (3.6) contributes to the generated pole and it can be removed by removing the capacitor C_F connected to V_X and VCCS at the output node in Figure 3.6. It should also be noted that C_F at the output node does not significantly affect the node voltage since C_F is much smaller than Co at the output node. The resulting configuration is shown in Figure 3.7. This becomes a two-pole and one-zero system. The zero remains unchanged and the dominant pole is given in Equation (3.7). The dominant pole location slightly changes but it is still mostly dependent on the output capacitor.

$$\omega_{PL} = \frac{1}{R_{OUT}(C_O - \frac{C_F}{\beta})} \quad (3.7)$$

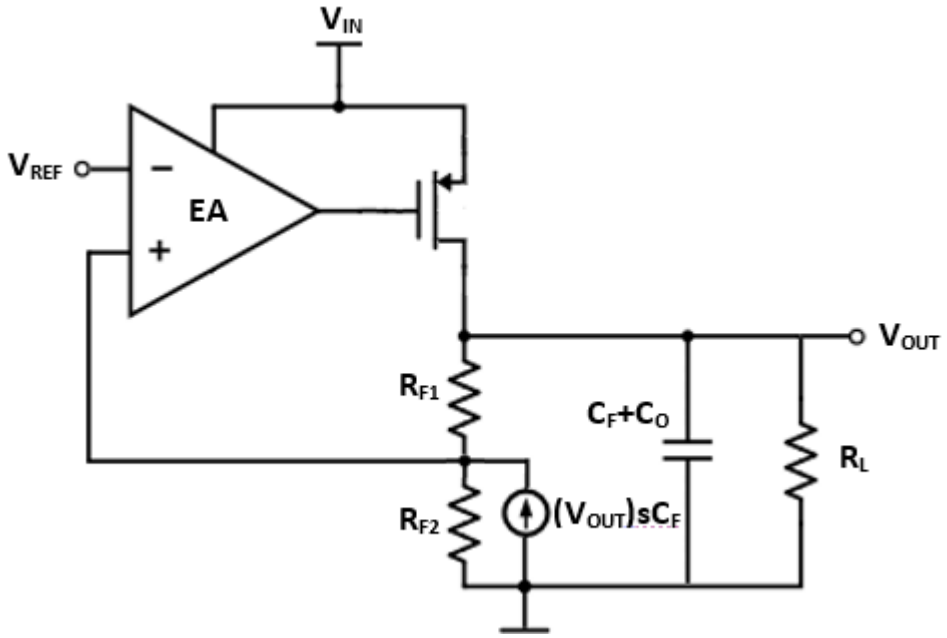

Figure 3.7: Implementation of a feed-forward capacitor after removing the extra pole

Al-Shyoukh et al. uses an impedance attenuated buffer to push the second dominant pole at the gate of the pass transistor to high frequencies [2]. As shown in Equation (3.2), the second dominant pole is a function of error amplifier output impedance and capacitance at the node. However, the capacitance C_1 is difficult to reduce since it is set by the load current and V_{DSAT} of the pass transistor. Reducing the error amplifier output impedance is also difficult since it affects load/line regulation. In order to move the pole location without changing C_1 or V_{DSAT}, a buffer is employed, as shown in Figure 3.8. A source follower can be adopted as a buffer to shield C_1 from loading the error amplifier. Small input capacitance and

lower output impedance allow the second dominant pole to be pushed to high frequencies as shown in Equation (3.8) and Equation (3.9) compared to the second dominant pole in Equation (3.2).

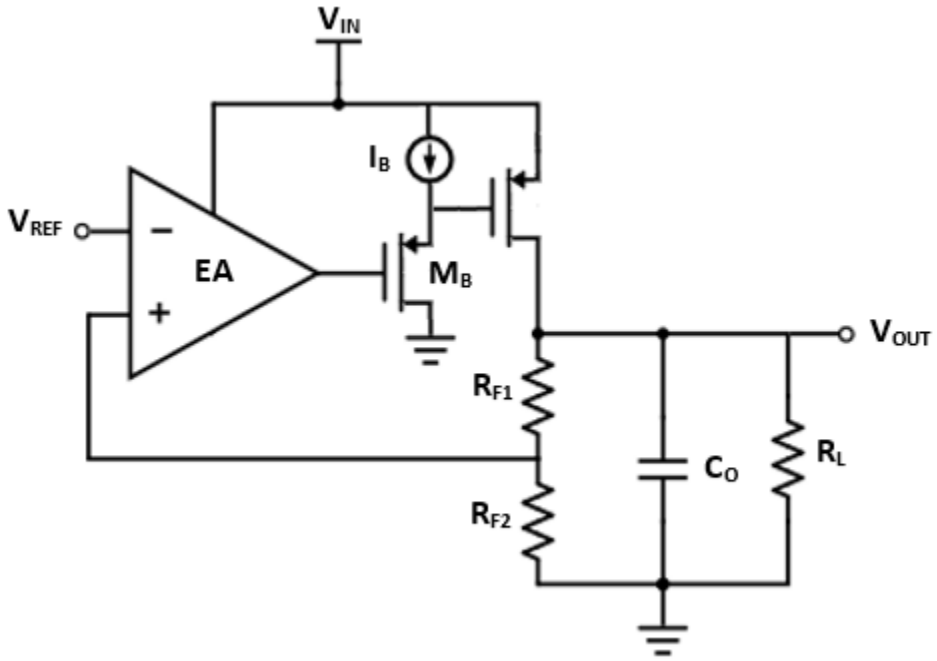

Figure 3.8: Conventional LDO with buffer

$$\omega_{PB} = \frac{1}{R_B C_1} \tag{3.8}$$

$$R_B \approx 1/g_{mB} \propto \frac{1}{(W/L)I_B} \tag{3.9}$$

However, large load current requires a larger pass device and increases the gate capacitance. This requires the current through the source follower to be greatly increased to lower the output impedance further. Instead of dissipating more power through the source follower to reduce the output

impedance, Al-Shyoukh et al. use shunt feedback to reduce the output impedance as shown in Figure 3.9 [2]. The improved buffer has an output impedance of R_B in Equation (3.10) where R_X is resistance at the gate of transistor M_S in Figure 3.9. Thus, this scheme maintains stability without using the ESR and achieves low power.

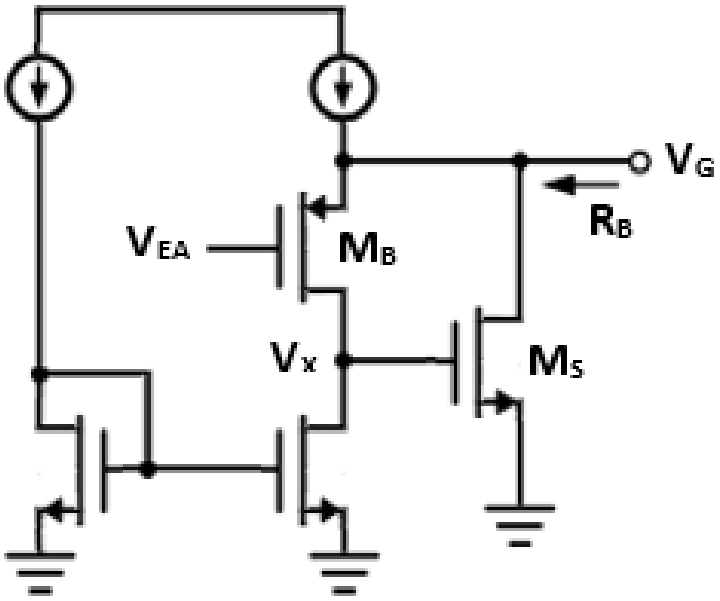

Figure 3.9: Improved buffer that uses shunt feedback

$$R_B \approx \frac{1}{(g_{mB} \cdot R_x) g_{mS}} \tag{3.10}$$

Unlike the conventional LDO regulator that relies on large output capacitors for regulation and stability, the capacitor-less LDO regulator

has an output capacitance less than a few hundred pF. Thus, the uncompensated capacitor-less LDO regulator has a dominant pole at the gate of the pass transistor and a second dominant pole at the output of the pass transistor. Equations (3.11), (3.12), and (3.13) show pole and zero locations of the capacitor-less LDO regulator. The compensation schemes used in conventional LDO regulators cannot be used. Rather, the Miller compensation, cascade compensation, or cascaded compensation can be used depending on the applications.

$$\omega_{PL} = \frac{1}{R_{OEA}(C_1 + g_{mp} \cdot R_{OUT} \cdot C_{gdp})} \tag{3.11}$$

$$\omega_{PH} = \frac{1}{R_{OUT} C_O} \tag{3.12}$$

$$\omega_Z = \frac{g_{mp}}{C_{gdp}} \tag{3.13}$$

Figure 3.10 shows how a compensation capacitor can be inserted between the gate and drain of the pass transistor. This causes the separation between the two poles in Equations (3.11) and (3.12). However, a large compensation capacitor is required to ensure stability, and stability can be compromised with load current variation. This also shows poor PSR at high frequency.

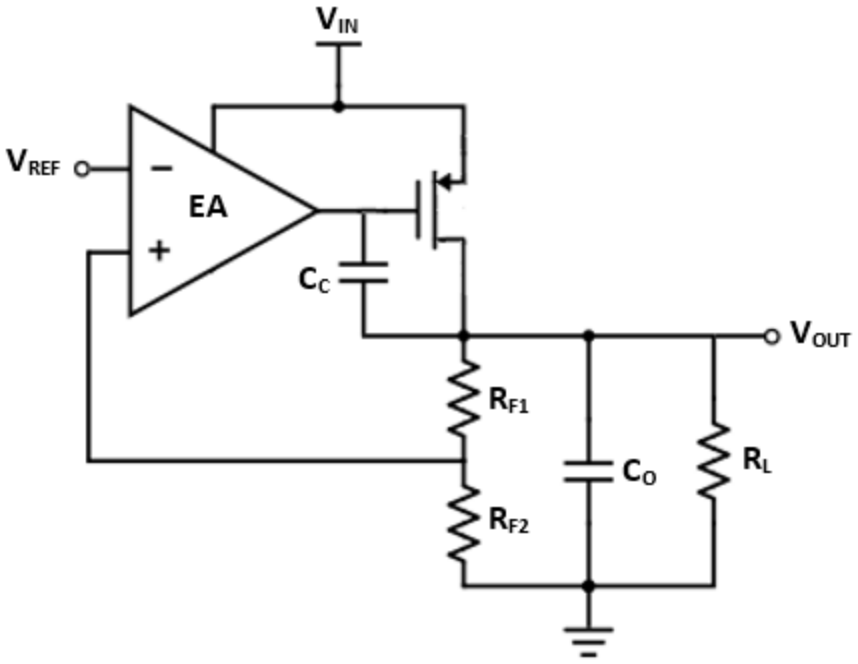

Figure 3.10: Capacitor-less LDO with miller compensation

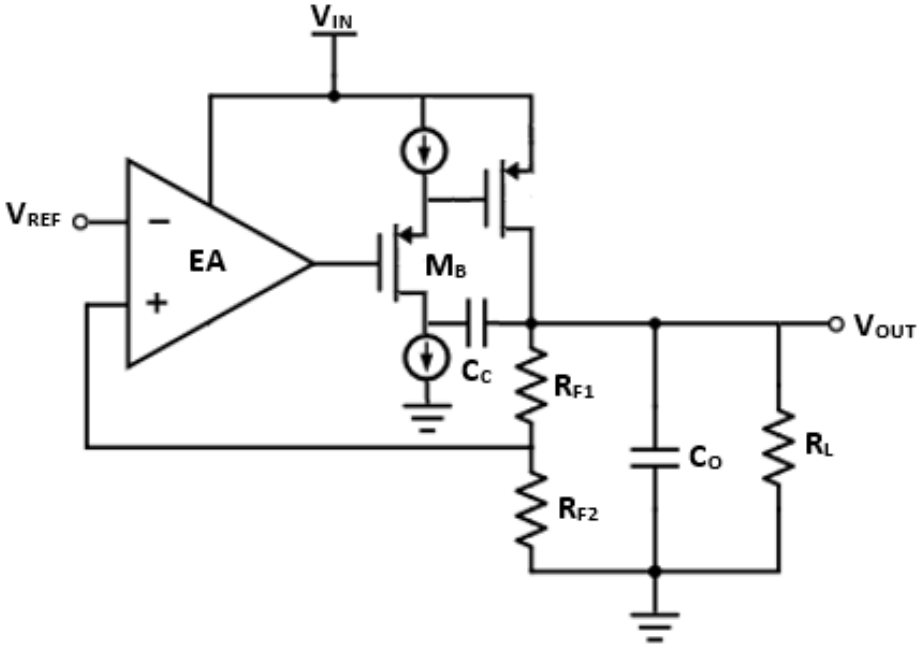

Figure 3.11: Capacitor-less LDO with cascode compensation

Cascode compensation improves the capacitive load capability and power supply rejection [3]. The LDO regulator with typical cascode

compensation is shown in Figure 3.11. It suppresses the feed-forward path that comes from the compensation capacitor while keeping the Miller effect of C_C. The right-half plane zero from the feed-forward path essentially works like the left-half plane pole and needs to be removed for stability. Equations (3.14) and (3.15) show two poles associated with the cascode compensated LDO regulator.

$$P_1 \approx \frac{1}{R_{OEA}C_1 + R_{OUT}(C_C + C_O) + g_{mp} \cdot R_{OEA} \cdot R_{OUT} \cdot C_C} \tag{3.14}$$

$$P_2 \approx \frac{R_{OEA}C_1 + R_{OUT}(C_C + C_O) + g_{mp} \cdot R_{OEA} \cdot R_{OUT} \cdot C_C}{R_{OEA} \cdot R_{OUT} \cdot C_1(C_C + C_O)} \tag{3.15}$$

Pole locations can be simplified to Equations (3.16) and (3.17) for small C_O, the capacitance at the output; Equations (3.18) and (3.19) for large C_O.

$$P_1 \approx \frac{1}{g_{mp} \cdot R_{OEA} \cdot R_{OUT} \cdot C_C} \tag{3.16}$$

$$P_2 \approx \frac{g_{mp}C_C}{C_1(C_C + C_O)} \tag{3.17}$$

$$P_1 \approx \frac{1}{R_{OUT}(C_C + C_O)} \tag{3.18}$$

$$P_2 \approx \frac{1}{R_{OEA}C_1} \tag{3.19}$$

CHAPTER 4: ANALOG LDO PSR ANALYSIS

Power supply rejection defines the LDO regulator's ability to reject the output voltage variation due to input voltage change. Any path from the input to the output can contribute to degrading PSR. It includes the path through the reference generator, error amplifier, and pass device.

The output stage of the regulator can be either a PMOS or an n-channel MOSFET (NMOS) device. Since an NMOS device requires large voltage headroom, it can be used as a pass device when low dropout voltage is not needed. It behaves as a source follower and conducts all the noise present at the input to the output. Thus, it is important to have as low a ripple as possible at the gate to minimize the ripple at the output [4].

On the other hand, a PMOS device is used for most of the recent research due to its low dropout voltage. Due to its higher output impedance, the compensation of the regulator is more difficult than for the regulator with the NMOS device. Due to the pass transistor orientation, the gain from the source to the drain is equal in magnitude to the gain from the gate to the drain. Since these two gains are out of phase, supply ripple can be fed to

the gate of the PMOS to cancel out the ripple from the source [4].

Gupta et al. categorizes error amplifier to two different types to evaluate PSR for each type [4]. The Type-A error amplifier is shown in Figure 4.1 and its small signal model is shown in Figure 4.2. It consists of an NMOS input pair and a PMOS current-mirror.

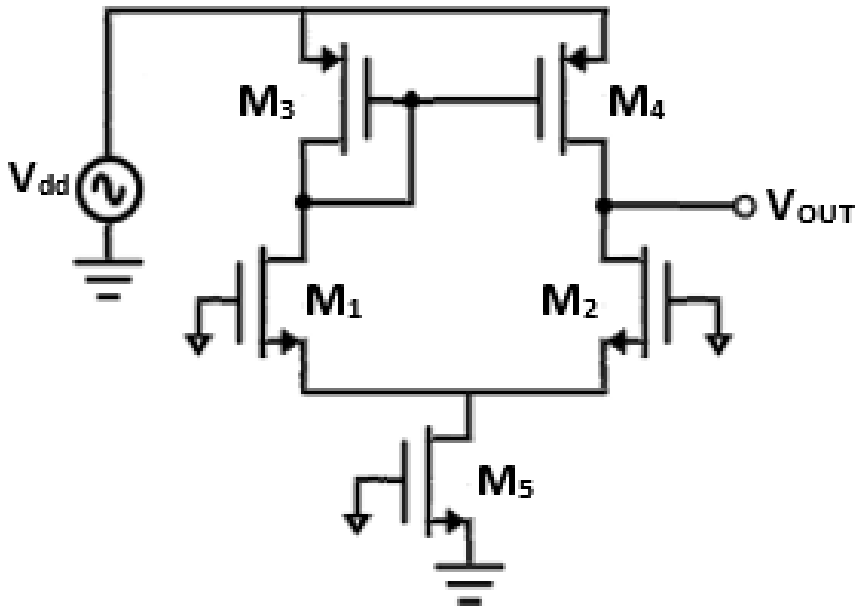

Figure 4.1: Type-A error amplifier

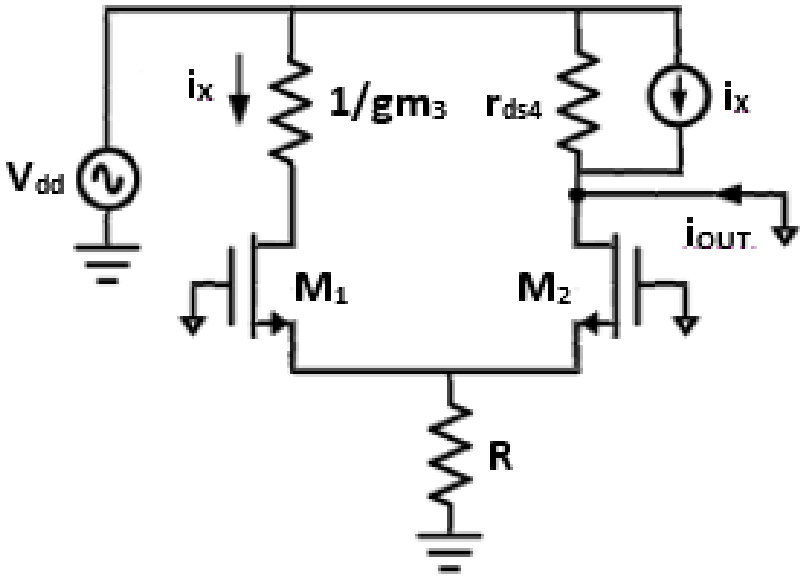

Figure 4.2: Type-A error amplifier small signal model

$$\frac{v_{out}}{v_{dd}} = -G_M R_{out} \tag{4.1}$$

$$R_{out} = (r_{ds2} \parallel r_{ds4}) \tag{4.2}$$

$$i_{out} = 2i_x + \frac{v_{dd}}{r_{ds4}} \tag{4.3}$$

$$i_x = \frac{v_{dd}}{1/g_{m3} + 2r_{ds1}} \tag{4.4}$$

$$G_M = r_{ds1} \parallel r_{ds4} \tag{4.5}$$

$$\frac{v_{out}}{v_{dd}} \approx 1 \tag{4.6}$$

PSR is calculated to be 1 from the small signal model analysis. G_M is calculated by grounding the output node and calculating i_{out} in terms of v_{dd}. The analysis shows that all the noise at the supply appears at the

output for the Type-A error amplifier. The Type-A error amplifier can provide the supply noise to the gate of the PMOS output stage to cancel out the feedthrough. Thus, the PMOS output stage can be used with the Type-A error amplifier to maximize PSR.

The Type-B error amplifier is shown in Figure 4.3 and it consists of a PMOS differential pair and an NMOS current-mirror [4]. Small signal analysis reveals that none of the supply noise appears at the output. The Type-B error amplifier is suitable for the NMOS output stage, which requires a small gate ripple to minimize the output noise.

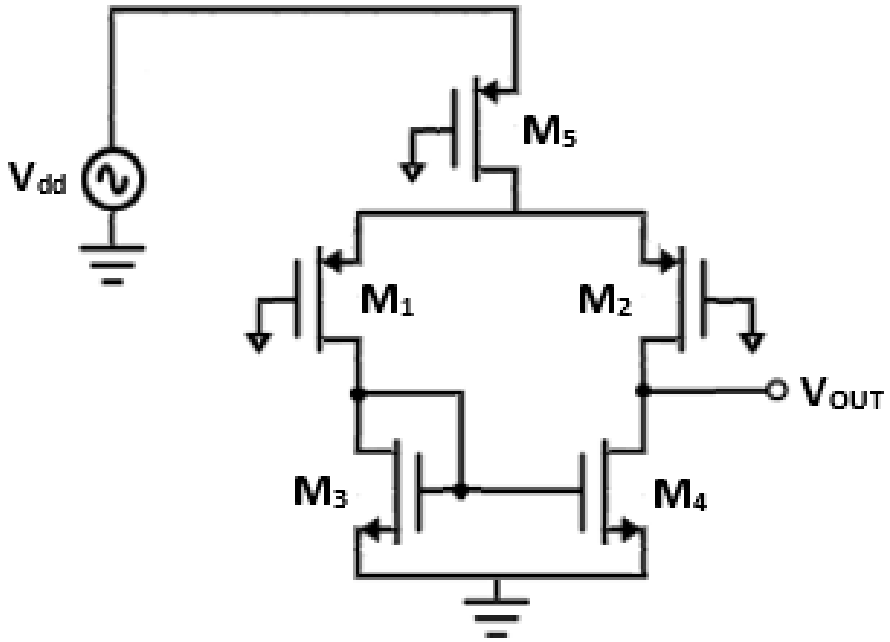

Figure 4.3: Type-B error amplifer

It can be concluded that the Type-B amplifier with an NMOS output stage or the Type-A amplifier with a PMOS output stage yields the best PSR. This can be further improved by cascading regulators at the cost of dropout voltage.

CHAPTER 5: DIGITAL LDO REGULATOR

The difficulty of designing a high gain amplifier for an analog LDO regulator and lowered supply voltage gave rise to the digital LDO regulator in recent years. The digital LDO regulator broadly comes in two different categories: designs that use a comparator with a digital controller and designs that convert the voltage difference into other information.

Raychowdhury et al. present a fully digital LDO regulator based on a phase locked loop (PLL) [5]. This design converts the difference between the output voltage and reference voltage to the phase difference and directly use it for regulation. The design consists of two voltage-controlled oscillators (VCOs), each run by a reference voltage and the output voltage. The VCO outputs are used as clock signals for the 32-bit Johnson Counter with PMOS devices and latches inside each stage [5]. At steady state, the phase difference comes to a constant value and the amount of current from the turned-on devices matches the load current. A simulated Bode plot shows a high phase margin, more than 80 degrees at light load [5]. This configuration is capable of fine voltage regulation based on PLL, but it consumes high power compared to the comparator-based LDO regulator

and suffers from PVT dependency.

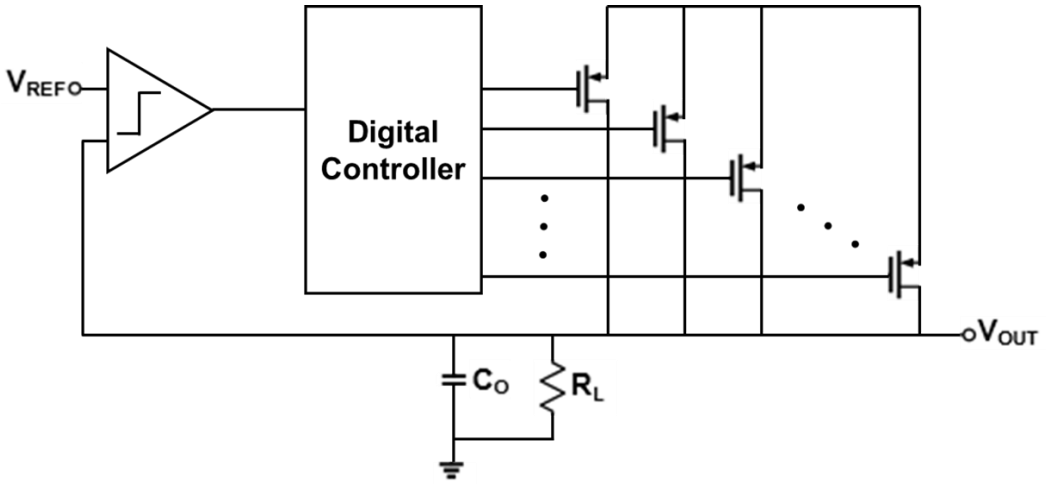

Figure 5.1: Basic comparator-based digital LDO

The comparator-based digital LDO regulator in Figure 5.1 uses a comparator to detect the difference between the reference voltage and the output voltage that needs to be regulated. Then, an error signal from the comparator is fed into the digital controller which usually comes in the form of a shift register. The digital controller is connected to an array of PMOS and continuously switches them until the output voltage is close to the reference voltage. The design in [6] implements the digital controller with a bi-directional shift register. This design can be fully expressed in hardware description language and synthesized from commercially available standard libraries. It also consumes little power due to its simplicity. However, the voltage regulation is limited by the clock

connected to the shift register which deteriorates the transient response and causes voltage ripple at steady-state.

More recent designs focus on enhancing the transient response of the comparator-based digital LDO regulator. Nasir et al. [7] present a digital LDO regulator using a programmable barrel shifter that can access several PMOSs at a time to enhance the transient response. The most recent architecture from [8] separates the coarse loop from the fine loop so that the coarse loop responds to a large load change while the fine loop is used to maintain the steady-state output. These measures definitely enhance the transient response, but the output ripple still remains as a problem. Unless a huge number of power transistors are used, most of the designs fail to keep low output voltage ripple for various load current [9].

CHAPTER 6: CONCLUSION

This thesis discusses different analog LDO topologies and analyzes how they achieve stability using small signal analysis and related equations. The conventional analog LDO regulator uses a feed-forward capacitor and/or adds a buffer to ensure stability. The capacitor-less LDO regulator uses cascode compensation to keep the Miller effect and remove the RHP zero. The PSR of different error amplifier and pass devices has been analyzed. The conclusion is that the Type-B amplifier with an NMOS output stage or Type-A amplifier with a PMOS output stage yields the best PSR. Digital LDO topologies have also been discussed. The digital LDO regulator is intriguing due to its low power and synthesizability but suffers from coarse voltage regulation and poor PSRR compared to the analog LDO regulator.

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