MULTIGATE MOSFETS FOR DIGITAL PERFORMANCE AND HIGH LINEARITY, AND THEIR FABRICATION TECHNIQUES

BY

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DISSERTATION

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ABSTRACT

The aggressive downscaling of complementary metal–oxide–semiconductor (CMOS) technology is facing great challenges to overcome severe short-channel effects. Multigate MOSFETs are one of the most promising candidates for scaling beyond Si CMOS, due to better electrostatic control as compared to conventional planar MOSFETs.

Conventional dry etching-induced surface damage is one of the main sources of performance degradation for multigate transistors, especially for III-V high mobility materials. It is also challenging to increase the fin aspect ratio by dry etching because of the non-ideal anisotropic etching profile. Here, we report a novel method, inverse metal-assisted chemical etching (i-MacEtch), in lieu of conventional RIE etching, for 3D fin channel formation. InP junctionless FinFETs with record high-aspect-ratio (~ 50:1) fins are demonstrated by this method for the first time. The i-MacEtch process flow eliminates dry-etching-induced plasma damage, high energy ion implantation damage, and high temperature annealing, allowing for the fabrication of InP fin channels with atomically smooth sidewalls. The sidewall features resulting from this unique and simplified process ensure high interface quality between high-k dielectric layer and InP fin channel. Experimental and theoretical analyses show that high-aspect-ratio FinFETs, which could deliver more current per area under much relaxed horizontal geometry requirements, are promising in pushing the technology node ahead where conventional scaling has met its physical limits.

The performance of the FinFET was further investigated through numerical simulation. A new kind of FinFET with asymmetric gate and source/drain contacts has been proposed and simulated. By benchmarking with conventional symmetric FinFET, better short-channel behavior with much higher current density is confirmed. The design guidelines are provided. The

overall circuit delay can be minimized by optimizing gate lengths according to different local parasites among circuits in interconnection-delay-dominated SoC applications.

Continued transistor scaling requires even stronger gate electrostatic control over the channel. The ultimate scaling structure would be gate-all-around nanowire MOSFETs. We demonstrate III-V junctionless gate-all-around (GAA) nanowire (NW) MOSFETs for the first time. For the first time, source/drain (S/D) resistance and thermal budget are minimized by regrowth using metalorganic chemical vapor deposition (MOCVD) in III-V MOSFETs. The fabricated short-channel (L_g=80 nm) GaAs GAA NWFETs with extremely narrow nanowire width (W_{NW}= 9 nm) show excellent transconductance (g_m) linearity at biases (300 mV), characterized by the high third intercept point (2.6 dBm). The high linearity is especially important for low power applications because it is insensitive to bias conditions.

To my mother and father

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CHAPTER 1 – INTRODUCTION

The integrated circuit (IC) industry has benefited from driving Moore's law for decades. Primarily by dimensional downscaling of the channel length, we can obtain higher performance, lower power consumption and more complex functionality per area, faster switching speeds, and reduced cost per transistor. As MOSFET feature dimensions shrink down to sub-20nm range, nanoscale processing encounters tremendous difficulties, for instance, severe short-channel effects, degraded driving ability, high-field effect, direct gate tunnelling current, high series resistance and nanopatterning issues, etc. Continuing Moore's law encounters unprecedented difficulties. Tremendous technical innovations are required to develop CMOS devices beyond the 10 nm technology node. Enormous efforts have been made in developing new materials, processes, and architectures for the next generation of transistors with shorter channel length [1].

1.1 Challenges for the down-scaling of metal-oxide-semiconductor field-effect transistors

As the feature size of MOSFETs continues shrinking according to Moore's law, CMOS technology faces tremendous challenges, primarily due to severe short-channel effects (SCE). Figure 1.1 depicts the major challenges associated with scaling of channel length, and Table 1.1 summarizes the targets for scaling proposed by ITRS. The major innovations are based on the introduction of new high-k/metal gate stacks, advanced S/D technologies, mobility enhancement technologies and advanced multigate structures. In this thesis, the main focus will be developing advanced multigate transistor structures, both by device simulation design and new fabrication technologies.

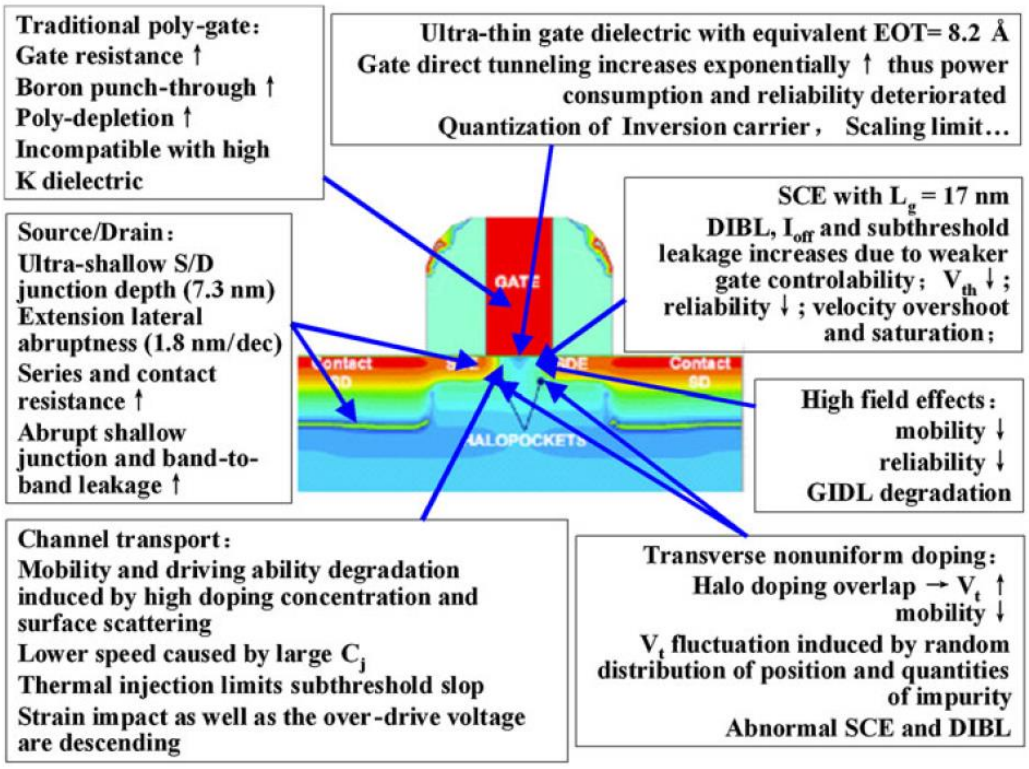

Figure 1.1: Difficult challenges for the scaling of CMOS device. Reprinted with permission from [1].

Table 1.1: Summary of technology trend targets proposed by ITRS 2013 [2]

year	Node name (nm)	Logic half pitch (nm)	Fin half pitch (nm)	Fin width (nm)	6-t SRAM size (μm^2)	V_{dd} (V)	1/CV/I (1/psec)
2017	7	25	19	6.8	0.038	0.8	1.75
2021	3.5	16	12	6.1	0.015	0.74	2.10
2025	1.8	10	7.5	5.4	0.006	0.68	2.52

1.2 Multigate MOSFETs

Novel device structures (e.g. nonplanar MOSFETs such as double-gate or tri-gated/Ω-gated FinFET, and ultimately, gate-all-around FET) are indispensable for the continuous scaling of CMOS devices due to the effective suppression of short-channel effects. The device structures evolve from single-gated planar FET to fully gate-all-around MOSFET. The increased number of

gates enhances electrostatic control of the gate electrode over the charge carriers flowing from source to drain in the channel, and therefore reduces the short-channel effects.

1.2.1 Double-gate FinFETs

The scaling of planar MOSFETs is limited by severe transverse short-channel effects and longitudinal gate dielectric tunneling; moreover, the controllability of single-gate MOSFETs is much weaker than multigate MOSFETs (FinFETs or tri-gate transistor). FinFETs are promising candidates for nanoscale devices with 10-30nm gate length due to quasi-planar architecture and simplicity of fabrication process that is compatible with traditional CMOS process [3, 4]. FinFETs do not require dopant concentration as high as planar transistors and thus could suppress short-channel effects more effectively. The gate is self-aligned with S/D, and it is better for controlling electrostatic between S/D which results in near-ideal subthreshold gradient and excellent DIBL behavior.

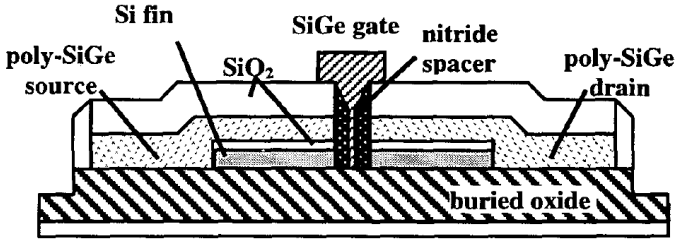

Figure 1.2: The early proposed self-aligned double-gate FinFETs on SOI substrate. Reprinted with permission from [5].

The first proposed self-aligned double-gate FinFET with gate-length of 45nm by quasi-planar process is shown in Figure 1.2 [5]. The deposited SiO_2 and SiN serve as hard mask, and then the fin structure is exposed by electron beam lithography. After the deposition of gate SiO_2 and in situ doped poly-silicon stack, the silicon S/D is etched with the fin protected by hard mask. Then a GeSi layer is deposited to form the raised S/D, and silicidation completes the process. The gate-last process is compatible with low-temperature high-k/metal gate integration. The ultra-

thin fin body significantly suppresses short-channel effects and the poly-SiGe raised S/D lowers the contact resistance. The fabricated devices show good performance characteristics with high on-current of 820 μA/μm at V_{dd}=1.2V.

As for UTB SOI double-gate MOSFETs using SiO_2-based dielectrics, it is found that there exists a stringent confinement for scaling the thickness of the silicon body to reach the specifications of the ITRS in terms of drain and gate leakage current. Meanwhile, moderate gate-S/D underlap not only benefits the suppression of gate-induced drain leakage (GIDL) [6], but also could control the effective gate length by different bias, thus relaxing the requirement for ultra-narrow fin width.

Combing strain technologies such as compressive and tensile contact-etch-stop liners could improve the drive-current enhancement by a factor of 2 in both n- and p-FinFETs [7], and allow V_{dd} scaling and trade enhanced carrier velocity for reduced inversion charge [8].

Metal-gate with tunable work-function is required to avoid applying high channel doping to achieve ideal V_{th}. In addition, integration of metal gate with SOI FinFETs could induce strain to the Si(110) channel [9]. The adjusting requirement of gate work function for double FinFETs is relaxed compared with planar MOSFETs. The performance of nMOS and pMOS could be optimized simultaneously by adjusting gate work functions, achieving symmetrical V_{th} and high I_{on}.

The device structure is shown in Figure 1.3. The fin structure is etched with nitride hard mask. Annealing in H_2 atmosphere is performed to reduce surface roughness. 3nm HfSiO and 3-20nm TiN are deposited using atomic layer deposition. The S/D implantation and Ni silicidation are performed after the nitride spacer formation. The poly-silicon is deposited at the end.

TiN layer with different thickness and deposition methods would induce different strain into the channel. Thin TiN and Ti-rich TiN corresponds to high tensile stress, while thick TiN deposited by atomiclayer or chemical vapor deposition corresponds to compressive stress. The discrepancy between different crystal orientations diminishes with the decrease of channel length; therefore, high performance of CMOS device with identical crystal orientation is promising.

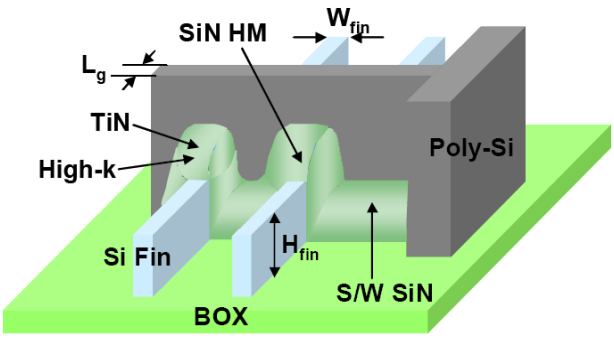

Figure 1.3: FinFET integration with TiN metal gate-induced stress on SOI substrate. Reprinted with permission from [9].

FinFET is preferable for storage application because it could increase density due to its 3D nature. Recently, highly scaled FinFET SRAM cells, of area down to $0.128\mu m^2$, were fabricated using high-κ dielectric and a single metal gate [10]. It is demonstrated that the un-doped FinFET SRAM cell has a significant advantage in read/write margin over a planar-FET SRAM cell, which would have higher σV_{th} mainly caused by heavy doping into the channel region, further substantiating the superior scaling capability of FinFETs.

There are severe challenges such as the simplicity of the integration technology, high reliability and reproducibility, and ultra-high parasitic S/D resistance due to greatly suppressed effective contact area in multigate device (as well as UTB-SOI in the previous section). The complicated fabrication process also may induce severe parasitic parameters. The sub-20nm gate length device is greatly influenced by quantum confinement effects and has high sensitivity to

process variations [11]. Simulation results show that device performance has high sensitivity to the fin width variation [12] and gate work function variation [13] in sub-20nm regime. Great efforts are still required for the practicality of double-gate MOSFETs.

1.2.2 Tri-gate and Pi-gate MOSFETs

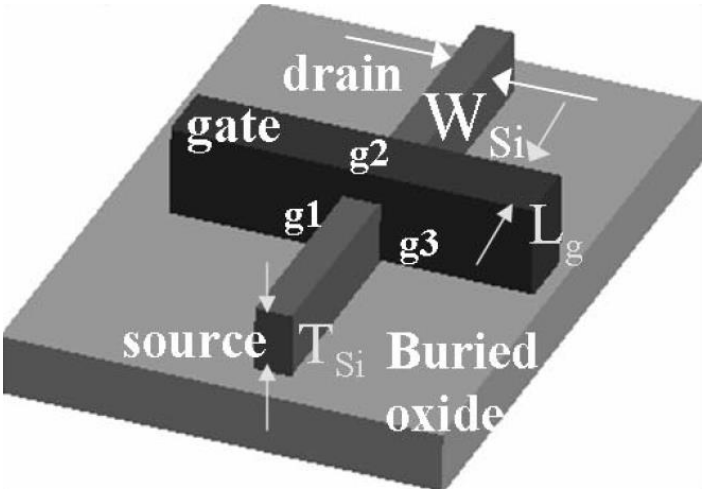

Figure 1.4: Illustration of the device structure of tri-gate MOSFETs. Reprinted with permission from [14].

The tri-gate MOSFET which has a top and two side gates on an insulating layer is superior to double-gate FinFET for further suppressing short-channel effects due to enhanced gate electrostatic control. Fully-depleted (FD) tri-gate CMOS transistors with 60nm physical gate lengths have been successfully fabricated on SOI substrates [14]. Figure 1.4 shows a schematic of the device structure of a tri-gate MOSFET. The transistors show near-ideal subthreshold gradient, excellent DIBL behavior and high drive current. The most significant aspect for tri-gate MOSFETs is the much-relaxed silicon body dimensions requirement for full depletion conditions, thus achieving excellent short-channel performance without tightening the lithography requirements.

The mobility enhancement technologies are important for boosting tri-gate device performance. Novel schematic integration strategies are needed due to the complex three-

dimensional structures of tri-gate devices. Studies have shown that <1 1 0> current (or strain) direction is the best for strained tri-gate nMOS since 2.0×mobility enhancement in uniaxially strained silicon-on-insulator (SOI) tri-gate nMOS with (1 1 0) sidewall channels is obtained due to uniaxial strain inducing the repopulation of electrons from fourfold valleys to twofold valleys [15]. Figure 1.5 shows the ideal integration of different strain technology for tri-gate CMOS.

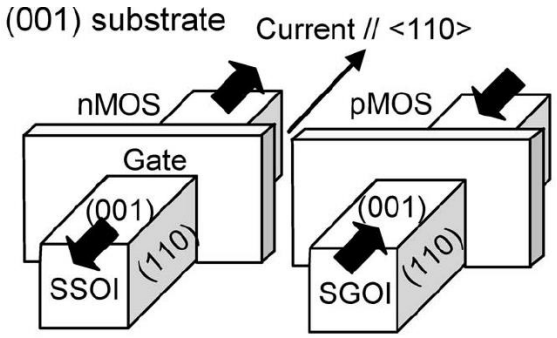

Figure 1.5: Proposed tri-gate CMOS structures, utilizing a SSOI nMOS and SGOI (GOI) pMOS with optimized uniaxial tensile and compressive stress and current flow direction. Reprinted with permission from [15].

As a result, a novel multigate device structure having a high uniaxial mobility channel by appropriately merging globally strained substrates with a local strain technique called lateral strain relaxation is developed [16]. The additive integration of channel materials, strain configuration and current flow direction is attractive for boosting tri-gate transistors. SiGe or Ge channels, (110) surface orientation/<110> channel direction and uniaxial compressive strain along <110> direction are used as pMOS boosters with additional advantages of low contact and S/D sheet resistances of p^+-SiGe layers. The local Ge condensation technique is utilized to form local SGOI regions for pMOS on SSOI substrates [17]. The uniaxial stress could be formed on the SiGe channel by applying a lateral strain relaxation process. Strained Si directly on insulator (SSOI) substrates [18], where biaxial or uniaxial tensile strain is along the <100> current flow direction, could be used as nMOS boosters.

$Si_{0.99}C_{0.01}$ S/D and tensile stress SiN etch-stop layer (ESL) could be combined as the stressor for boosting 25nm gate length n-FinFET performance by introducing large strain to channel as shown in Figure 1.6 [19]. The key of the fabrication process is selective epitaxy raised after $Si_{0.99}C_{0.01}$ S/D and spacer formation, then LPCVD high stress SiN ESL deposition after S/D implantation and activation. This combination results in an encouraging 56% I_{Dsat} enhancement over the control non-strained FinFETs.

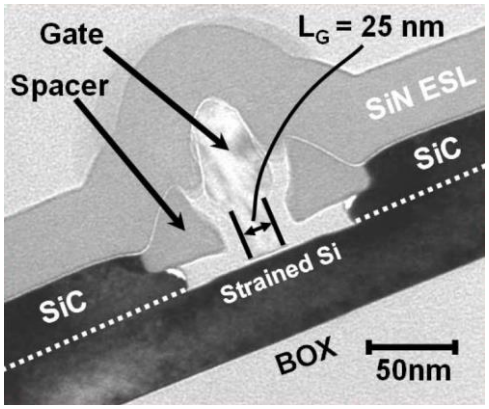

Figure 1.6: TEM micrograph of tri-gate device featuring 25 nm poly-Si gate with a raised $Si_{0.99}C_{0.01}$ S/D combined tensile stress SiN etch-stop layer. Reprinted with permission from [19].

The surface roughness and the shape of the sidewalls are found to be important for improving the performance of the strained-NW MOSFETs. A kind of anisotropic thermal etching technique in H_2 atmosphere is developed in order to fabricate strained Si and SiGe tri-gate nanowire (NW) MOSFETs with reduced line-edge roughness and smooth direction [20]. Mobility enhancement due to strain is observed for the reduced surface roughness scattering.

The contact resistance between the S/D silicide and Si-fin dominates the parasitic S/D resistance of multiple-gate FETs, which is a great barrier for scaling. Simply applying the selective epitaxial growth of Si on S/D regions is not enough to meet the semiconductor roadmap target for parasitic S/D resistance for aggressively scaled tri-gate CMOS [21]. Therefore, in order to reduce the S/D parasitic resistance in SiGe source/drain tri-gate devices, metal

germanosilicide is considered as the natural solution. Nickel germanosilicide (NiSiGe) is not suitable with morphological instability due to agglomeration and germanium (Ge) out-diffusion [22], while an appropriate concentration of Pt (about 10 at.%) could provide superior morphological stability and reduced Schottky barrier height for holes with an acceptable sheet resistivity. In consequence, this gives rise to an overall 18% enhancement in drive current performance compared with NiSiGe contact technology [23].

Fabrication of tri-gate MOSFETs on bulk substrate [24, 25] could combine the advantages of both a tri-gate device (reduced variability in performance and improved scalability) and planar bulk device (low substrate cost and capability for dynamic threshold-voltage control). The design considerations for tri-gate bulk MOSFETs are investigated through 3D numerical simulations [26]. The combination of retrograde channel doping with a multigate structure provides for superior electrostatic integrity, and the requirement of stringent aspect-ratio control is greatly relaxed. The tri-gate bulk MOSFET also provides reduced variability due to suppression of random dopant fluctuations and the flexibility of dynamic threshold-voltage control for further yield improvement and versatility.

The accumulation of the carrier density in the corners of highly doped channels may significantly influence the behavior of long-channel devices leading to “corner effects” [27], which are found to dominate the tri-gate device behavior in the subthreshold regime by 2D and 3D simulations [28]. The parasitic corner conduction could be efficiently suppressed in lightly doped short devices with narrow and high fins, rounded corners, and ultra-thin gate oxides.

The Pi-gate or Ω-shape gate devices are intermediate between tri-gate and gate-all-around MOSFETs by extending the sidewalls into the buried oxide. They could offer electrical characteristics like gate-all-around MOSFET but without too much process complication.

Simulations show that Pi-gate gives rise to a virtual back gate which effectively enhances current drive and shields the back of the channel region from electric field lines from the drain [29].

An analytical model is derived to investigate body effects in tri-gate or Pi-gate devices based on the representation of capacitive coupling effects between the front- and back-gate and the channels [30]. The results show that the body factor is much smaller than in regular single-gate SOI devices because of the enhanced coupling between gate and channel**,** and because the lateral gates shield the device from the electrostatic field from the back gate. The extreme case is the gate-all-around transistor in which the channel is completely isolated from the substrate and thus has no body effects.

The corner effects in Pi-gate MOSFETs are investigated by directly solving the 2-D self-consistent Schrödinger-Poisson equation [31]. The results obtained are quite similar to a tri-gate device showing that low doped channel, thin gate oxide, and rounded corners in an aggressively scaled device are beneficial for suppressing corner effects. The critical point is to reduce the potential variations along the Si-SiO_2 interface, and the transition between fully and partial depletion is not an indicator for the elimination of corner effects.

The Ω-shape gate device is superior to SNWFETs in terms of lower manufacturing complexity, and it has been clarified that the difference between the electrical characteristics of the surrounding-gate and the Ω-shape gate nanowire MOSFETs with 70% coverage is insignificant [32]. Therefore, choosing the Ω-shape gate device as the substitution for SNWFETs will also be an alternative solution [33].

The gate-all-around nanowire channel MOSFETs are classified as the quasi-ballistic transport channel that will be discussed in the next chapter.

1.2.3 Gate-all-around MOSFETs

As the device channel length scales, the enhanced injection from the source and the reduced scattering of quasi-ballistic transport of carriers is needed for fully-depleted low doped MOSFETs. Some advanced quasi-ballistic channel devices such as silicon nanowire MOSFETs, tunneling transistors and carbon nanotubes, will possibly be utilized in the later stages of the roadmap.

Silicon nanowire gate-all-around MOSFETs which feature a quasi-ballistic transport mechanism are considered to be one of the most promising candidates for the end of the semiconductor roadmap for they have the best gate control, excellent current conduction and suppression of short-channel effects. Many critical technical difficulties, such as the definition of the under gate and the compatibility with traditional CMOS fabrication flow, have been demonstrated in the fabrication of SNWFETs both on SOI and bulk substrate.

Fabrication of nanowire GAA MOSFET on SOI substrate is easier due to the naturally existing sacrificed buried oxide, and the mainstream of fabricating SNWFETs on SOI substrate is based on the stress limited oxidation mechanism [34]. N. Singh et al. fabricated the silicon nanowire GAA CMOS device and the corresponding inverter with diameter of less than 5nm by traditional top-down CMOS process as shown in Figure 1.7 [35, 36]. The active area region and silicon fin are defined by KrF phase-shift mask lithography and dry etch. 140nm length nanowire is formed during dry oxidation. The gate electrode is defined wider than the nanowire to form low source/drain series resistance and facilitate the definition of the under-gate. The nanowire CMOS device featuring 180 nm long nanowire and 5nm diameter shows high I_{on}/I_{off} (10^6). The on-current could be further improved by reducing the channel length and gate dielectric thickness. The excellent short-channel effects demonstrate the superior gate controllability and

thus could relax the urgent requirement of thin gate oxide. There is no sharp corner because of no kink curves in the output characteristics. The substrate bias effects are eliminated due to the shielding effects of poly-silicon to the body.

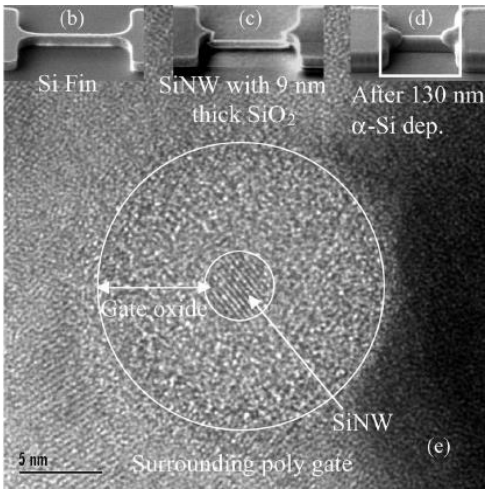

Figure 1.7: Silicon nanowire GAA MOSFETs fabricated by stress-limited oxidation method on SOI substrate. Reprinted with permission from [35].

A serious problem with SNWFETs on SOI substrate is the enormous source/drain series resistance caused by ultra-thin silicon body. This could be settled by the integration of a Schottky barrier source/drain structure [37]. The silicide/nanowire junction is similar to an ohmic contact in silicon nanowire transistors at high gate bias due to improved source/drain injection. Potential barrier as low as 215 meV for the hole and 665 meV for the electron could be achieved by aluminum inter-diffusion process [38]. A NiSi silicide Schottky barrier source/drain CMOS device has been fabricated using dopant segregation technology. The device shows high $I_{on}/I_{off}(10^5)$, near ideal DIBL (10m V/V) and Ss (60 mV/dec). The Schottky barrier nanowire nMOS with erbium silicided source/drain has also been demonstrated utilizing the low barrier between Er and n-type Si [39]. Another possible solution is the optimization of the doping profiles of source/drain extension and silicidation process [40]. The absolute value of the driving current of SNWFETs is always small due to finite conduction area. Therefore, the enhancement

of driving current by strain technology is quite necessary. The integration of high-level uniaxial tensile strain into SNWFETs was achieved on SOI substrate [41]. An average of 2× enhancement in current drive and intrinsic transconductance has been demonstrated for NW widths from 50nm down to 8nm, indicating the promise of this approach for deeply scaled SNWFETs.

Innovative breakthroughs also have been made in recent years on bulk fabrication process due to no self-heating effects or floating-body effects, lower cost, and compatibility with the-state-of-art bulk silicon planar process. A Damascene dummy gate process which features a unique epitaxial SiGe serving as a factitious sacrificial layer on bulk substrate has been proposed by Suk et al. [42, 43], and a method of direct etch silicon to produce the under-gate has been put forward by Tian et al. [44]. Later, Pott et al. proposed a local oxidation method to realize local SOI structure facilitate for producing nanowire on bulk substrate [45].

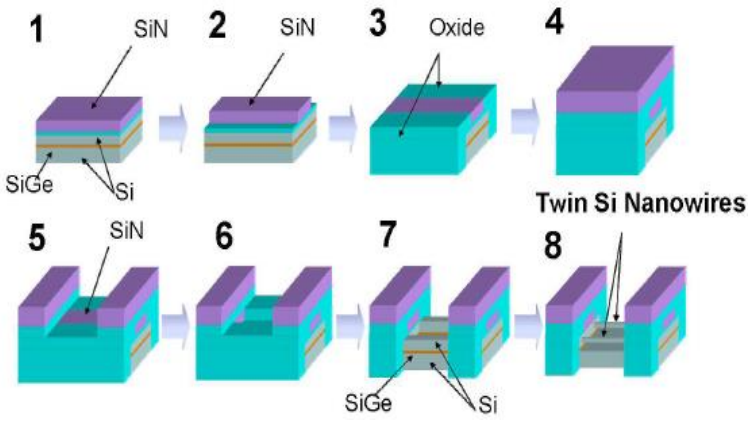

Figure 1.8: Process flow schematic diagram for twin Si nanowire FET(TSNWFET) fabrication using Damascus dummy gate technology and SiGe as the sacrificed layer. Reprinted with permission from [42] .

Figure 1.8 shows a typical process flow schematic diagram for twin Si nanowire FET fabrication using Damascus dummy gate technology. SiGe/Si layers are epitaxially grown followed by SiN hard-mask deposition and trimming. High density plasma (HDP) oxide fills in the trench region to form the STI isolation and another SiN layer is deposited. After Damascene-

gate photo process, the dummy gate layer between photo resist layers and trimmed hard-mask SiN layer is removed. The exposed Si area is trenched by using the oxide dummy layer as a hard mask. Finally, the field oxide is recessed and the subsequent exposed SiGe layer is removed with high selectivity to Si. An optional H_2 annealing is applied to smooth the cross-sectional shape of nanowires.

In order to further scale the gate length of SNWFET, a precisely controlled isotropic etching process is utilized to shrink the bottom part of the surrounding TiN gate into the sub-10nm regime, the same as the top part, as shown in Figure 1.9. The fabricated sub-10nm SNWFETs on bulk Si substrate with 13-nm-diameter silicon nanowire channel show on-state currents of 1494/1054 μA/μm and off leakage currents of 102/6.44 nA/μm for N/PMOS, respectively [43].

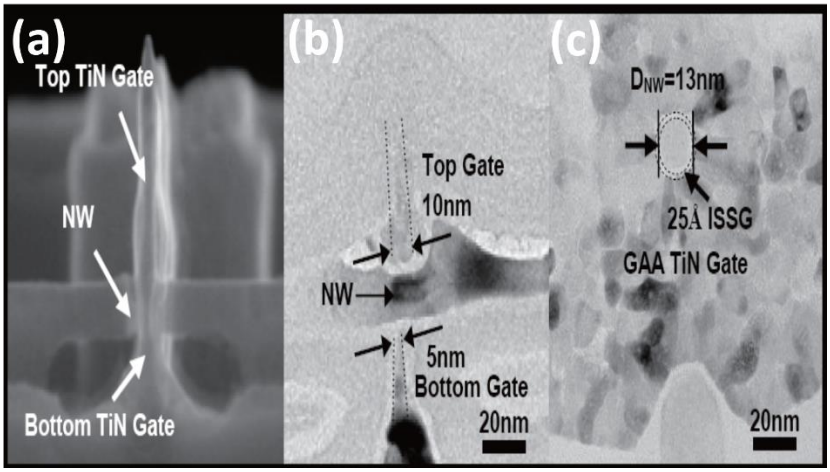

Figure 1.9: VSEM image of SA GAA structure (a), TEM images of 10nm top gate/5nm bottom gate (b) and 13-nm-diameter silicon nanowire as well as 25Å ISSG gate oxide (c). Reprinted with permission from [43].

The V_{th} increases with the reduction of nanowire diameter (DNW) due to the surface potential boosting and the quantum-confinement-induced band-gap broadening [46]. The short-channel effects improve with the decrease of DNW because of enhanced electrostatic integrity (EI) of the nanowire channel. The area-normalized current density inversely increases proportionally to

DNW reduction, which shows that the volume inversion becomes more dominant as DNW decreases [47].

Admittedly, S/D parasitic resistance (R_{SD}) becomes extremely severe in this structure due to the ultra-thin nanowire S/D extension. The effective channel length (L_{eff}) of SNWFET, which is greater than the physical L_g as the result of the injection point moving out of the gate edge in highly resistive nanowire S/D, causes not only performance degradation but also mobility underestimation. DIBL improves with the reduction of gate oxide thickness (T_{ox}) because thinner T_{ox} can more effectively reduce the fringing field so as to suppress drain field penetration into the channel. The on-current becomes saturated as T_{ox} is below about 30 Å. Therefore, T_{ox} remains relatively thick to keep high performance as well as to suppress gate leakage current for the SNWFET.

The main issue of fabricating nanowire GAA MOSFETs on bulk substrate is the formation of the sacrificial layer. Moreover, growing a uniform thin oxide around the nanowire is difficult due to the oxidation rate dependence on crystalline orientation. Very sharp silicon corners with thin grown gate oxides can be a reliability concern because of very high electric fields when the transistor is turned on. Minimizing the parasitic parameters with continuing shrinking of the gate length, and placing more nanowires within a certain width to boost its on-current, are intractable problems.

The industry has demonstrated that the multigate transistor indeed brought significant benefits for transistor scaling. Using multigate structure to scale transistors into the sub-10 nm era is quite promising.

1.2.4 Junctionless mode multigate MOSFETs

Conventional inversion mode transistors have met significant challenges associated with the source/drain (S/D) region, which is one of the key elements for improving SCE immunity and preventing punch-through [48]. Abrupt and ultrashallow junctions are required and the gradient needs to be as high as possible. The S/D parasitic resistance becomes high when the junction depth scales down below 10 nm. The thermal budget required by source/drain dopant activation is also a severe problem when integrated with high-k gate dielectric. Very complicated methods have been developed to achieve ultrashallow junction for S/D formation [49], regardless of the potential of greatly increased sophistication and cost. Therefore, people are considering eliminating the PN junction in transistor operation.

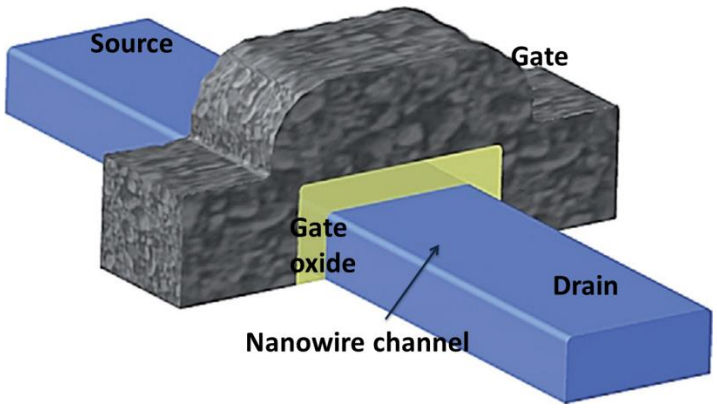

Figure 1.10: Schematic of an n-channel nanowire transistor. Reprinted with permission from [50].

The first principle of the JL MOSFET was proposed in [51] by simulation. Figure 1.10 shows the basic schematic of nanowire multigate JL MOSFETs. The name of the transistor can be simplified as a "gated resistor". When the device is turned on, the entire channel region can be regarded as neutral when considering the simplest situation that V_{ds} is low and in flat band condition. The transistor is just behaving like a highly doped resistor. The carriers are conducted in the bulk region instead of the surface as compared with the traditional inversion mode junction

based transistors. Admittedly, the mobility is lowered in the highly doped region due to increased dopant scattering. However, when considering scaling the gate length of MOSFETs into the sub-100 nm region, the inversion mobility is comparable to the bulk mobility in the highly doped region.

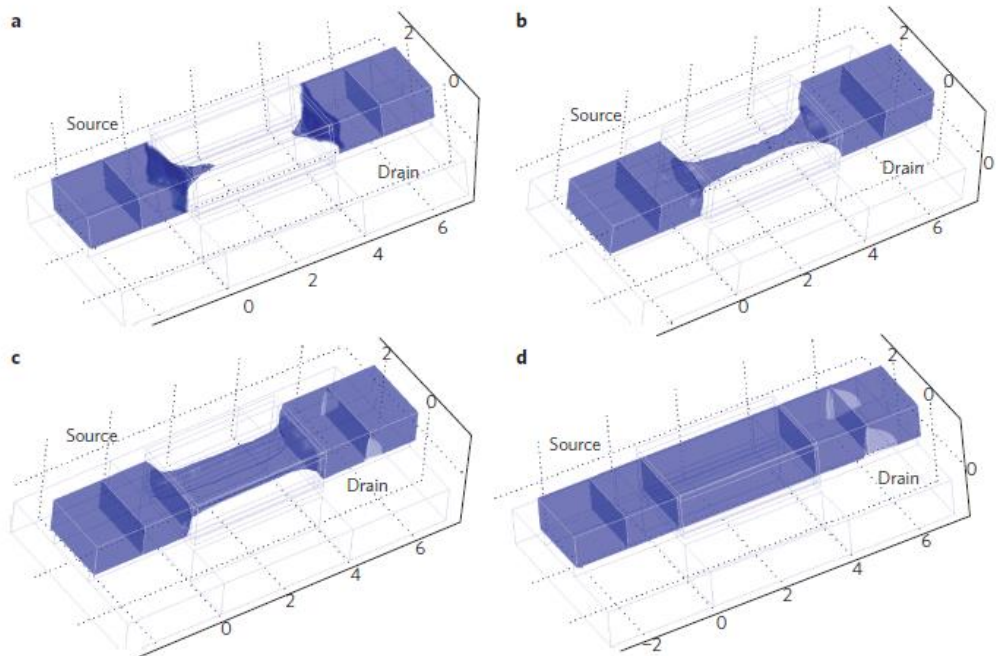

Figure 1.11: Electron concentration contour plots in an n-type junctionless gated resistor. (a) below V_{th}, (b), slightly above V_{th}, (c) higher V_g, (d) flat band. Reprinted with permission from [50].

Figure 1.11 shows the electron concentration contour plot for an n-type JL MOSFET. It can be clearly observed that the conduction path is located near the center of the nanowire. It significantly reduces the surface scattering compared with the regular transistor. When increasing the gate bias over the flat-band voltage, the channel becomes accumulated such that the on-current would be further increased upon the increase of V_{GS}. When reducing the gate bias below the flat band voltage, the channel is partially depleted so that the conducting width (neutral area) becomes narrower. When the gate bias reaches threshold voltage, the neutral channel looks like a string-shape connecting source and drain. When the gate bias is below the

threshold voltage, the device is turned off and the whole channel region becomes fully depleted. The leakage current is mainly due to trap-assisted gate tunneling instead of gate-induced drain leakage effects (GIBL) [52].

There are many unique properties regarding the JL MOSFETs. First, the transconductance degrades much more slowly when gate voltage is increased due to bulk conduction mechanism. Actually, this is good for exploring the devices with high linearity as will be discussed in Chapter 4; second, the degradation of mobility with temperature is much lower than in the inversion mode transistor. This is because the mobility in JL MOSFETs is limited by impurity scattering while mobility in lightly doped inversion mode MOSFETs is limited by photon scattering. The impurity scattering has much less dependence on temperature than photon scattering. Third, the intrinsic delay time for traditional inversion mode transistor is:

$$\tau = \frac{CV}{I} \approx \frac{C_{ox} W_{si} L V_{DD}}{\mu C_{ox} (W_{si} / L)(V_{DD} - V_{th})^2} \approx \frac{L^2}{\mu V_{DD}} \tag{1.1}$$

while the intrinsic delay for JL MOSFET is

$$\tau = \frac{CV}{I} \approx \frac{C_{ox} W_{si} L V_{DD}}{q \mu N_D (\mathrm{T}_{si} W_{si} / L) V_{DD}} \approx \frac{C_{ox} L^2}{q \mu N_D T_{si}} \tag{1.2}$$

where W_{si} is the width of the device, L the gate length, V_{DD} the supply voltage and C_{ox} the gate oxide capacitance, T_{si} is the thickness of the silicon and N_D the doping concentration. As shown in (1.2), we could find that the intrinsic delay decrease as EOT reduces in JL MOSFET. This is a merit indicating that we do not have to aggressively scale EOT to increase switching speed. The JL MOSFET is more immune to short-channel effects because the gate controlled depletion region extends into the SDE which provides a longer effective channel length. Simply increasing the doping concentration can bring about significant performance boost. There is indeed an imperfection in JL MOSFETs. The variability of the threshold voltage is greater than that in the

conventional ultrathin body SOI transistor. This is because the conduction channel is the entire body instead of just the surface. The change of thickness of the body directly reflects the change of conduction current. The surface conduction device has less dependence on channel thickness (body region) variation. However, this problem could be solved by precise epitaxy/etching technology to achieve thin films with variation less than 0.2 nm. It can also be alleviated by adopting some other technology as discussed later.

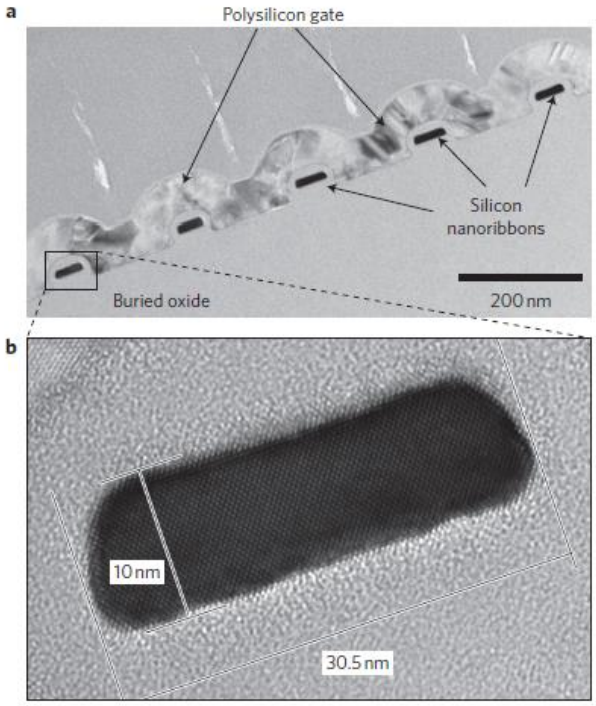

Figure 1.12: TEM of cross-section of silicon JL FETs. (a) Five parallel devices with a common polysilicon gate electrode. (b) Magnification of a single nanowire. Reprinted with permission from [50].

An example of silicon-on-insulator technology for the fabrication of JL MOSFETs is shown in Figure 1.12. The fabrication starts with commercial SOI wafers, and silicon nanowires are defined by e-beam lithography with thickness of 10 nm and tens of nanometers width. Ion implantation is employed to achieve uniform high doping within the nanowires after gate oxide growth. The high doping is required to ensure a high driving current and low source/drain

resistance. In order to fully deplete the channel during off-state, the geometries need to be extremely small. The gate electrode was formed by LPCVD deposition of amorphous silicon. After gate doping, the samples were annealed in N_2 ambient for 30 mins. The gate was patterned by RIE etching. The SiO_2 protective layer was patterned and Ti/W-Al metallization process was used for contact.

One difference from the inversion mode transistor is that we have to use P+ poly-silicon for NMOS but N+ poly silicon for PMOS in order to obtain appropriate V_{th}. The aspect ratio is less than one in this particular case, which is not area efficient. In this way, we developed a new semiconductor etching technology to achieve much higher aspect ratio as will be discussed in Chapter 2.

1.2.5 Comparison between inversion mode and junctionless mode multigate MOSFETs

Table 1.2 summarizes the merits and drawbacks for both inversion mode and junctionless mode MOSFET. Clearly, there are many advantages of Junctionless mode MOSFET over the inversion mode MOSFET. First, it has lower thermal budget because there is no implantation and high temperature annealing in the fabrication process flow of the junctionless MOSFET. The majority carriers are in the center of the channel instead of the surface, where the electric fields are weaker compared with the surface region. Therefore, mobility is less degraded with the increase of surface electric field in the junctionless mode MOSFET. This is the origin of higher linearity in junctionless mode transistors compared with inversion mode transistors which will be discussed in Chapter 4. Since the scattering is photon-determined scattering rather than surface scattering, mobility is less degraded with the increase of temperature in junctionless mode MOSFETs. The delay is dependent on C_{ox}, which relaxes the urgent requirement of increasing

C_{ox} when scaling. The major drawback of the junctionless mode MOSFET is its larger V_{th} fluctuation due to fin width variation, which is due to the factor that it is a bulk conduction transistor that is sensitive to the fin width.

Table 1.2 Comparison between junctionless mode and inversion mode MOSFET

	Junctionless mode MOSFET	Inversion mode MOSFET
SCE control	Controversial	Controversial
Cost/Thermal Budget	Low	High
Mobility vs Electron field degradation	Less	More
Mobility vs Temperature degradation	Less	More
Intrinsic delay	Dependent on C_{ox}	Independent on C_{ox}
V_{th} fluctuation	More	Less

The most controversial debate is whether immunity to SCEs is improved in junctionless mode MOSFET. Collinge et al. [53] claim that SCE are less serious in the junctionless mode transistor because in off-state, the depletion region controlled by the gate fringing fields can be extended laterally to the source/drain extension region. This results in a longer effective channel length in off-state, which effectively blocks the leakage paths. The subthreshold slope as well as gate electrostatic control over the channel is better than in a conventional inversion mode transistor. However, Rios et al. [54] discovered a contradictory conclusion that inversion mode transistor should be better in terms of SCE control. They claimed SCE are worse due to the larger effective EOT in junctionless mode MOSFET since the majority carriers are travelling away from the surface. The gate electrostatic potential control losses are due to the larger EOT. They fabricated short-channel (26 nm) junctionless mode and inversion mode FinFET and compared the DC characteristics, confirming theory. The conclusion from Intel Corporation might sound good, but the junctionless mode MOSFET should have its own market in some

specific areas, such as ultra-high-aspect-ratio FinFET where uniform S/D doping is not easy and high linearity, high temperature stability applications due to its unique operating principle.

CHAPTER 2 – METAL-ASSISTED CHEMICAL ETCHING FOR III-V MULTIGATE MOSFET FABRICATION

Nanostructure formation is the key process factor for multigate MOSFET fabrication. For transistor applications, nanostructures with smooth interfaces and extremely narrow feature sizes are critical for high performance improvement. Traditional dry etching by reactive ion implantation is a mainstream way to generate nanostructures, but has many shortcomings and is getting harder to scale down. Wet chemical etching usually provides good interface for nanostructures, but it can only deal with large dimensions. A new etching method that combines the merits of dry and wet etching is highly demanded.

2.1 Problems with conventional dry etching for fin formation

Shrinking the transistor size horizontally is only one side of the coin. We might be able to obtain higher on-state current per unit area by fully utilizing the bulk substrate conductivity as the channel, that is, exploring performance enhancement in the longitudinal direction instead of horizontal direction. One key point is that we must keep the lateral dimension narrow enough to maintain sufficient gate electrostatic control. Therefore, FinFETs with high-aspect-ratio (AR) fins might be one of the ideal device structures to satisfy the requirements.

The conventional well-known etching method, neither dry etch nor wet etch, can readily produce high AR fins with ideal vertical sidewall due to the non-ideal anisotropic etching profile. The tapered sidewall is due to the difficulty of making the reaction flow contact the surface and the fact that the reaction product evaporates as etching proceeds deeper. Figure 2.1 shows the cross section of state-of-the-art fins dry etched showing the non-vertical sidewalls. Due to the non-ideal anisotropic profile, there is a large leakage path at the wider bottom side such that the highest aspect ratio of the fins is less than 10:1.

What is worse, the plasma-based reactive ion dry etching causes irreversible damage to the sidewalls when fabricating FinFETs, particularly for III-V channels [55, 56], where such damage is difficult to repair compared to Si-based channels in CMOS technology. Sidewall damage induces a disordered interface between the high-k gate dielectric and semiconductor channel, which impedes the carrier surface mobility and degrades device sub-threshold characteristics [57]. Moreover, sophisticated techniques [58] are required to improve the selectivity over different materials by dry etching. Dry etching needs to be performed in an expensive high vacuum system. For the above reasons, dry etching hinders progress toward aggressively scaled FinFETs. On the other hand, pure wet chemical etching usually does not degrade the crystallographic integrity and has high selectivity, but it is only suitable for large features (>1 μm).

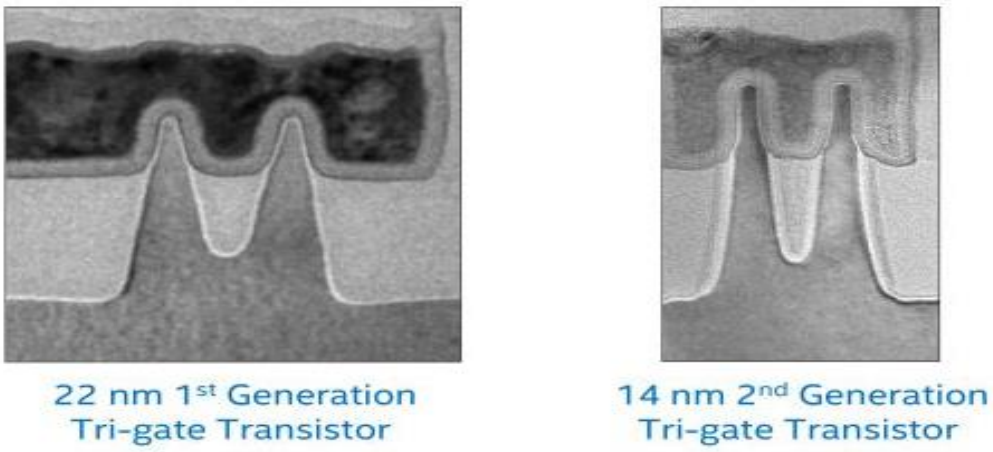

Figure 2.1: Cross section TEM images of commercial FinFETs at 22nm and 14 nm by Intel. Reprinted from Intel website http://www.intel.com.

2.2 Principle of metal-assisted chemical etching

MacEtch was first proposed in [59]. Metal serves as a hard mask as well as a catalyst that initiates the chemical etching by injecting holes to the substrate. There is a Schottky barrier

between metal and substrate which behaves like a barrier for hole injection. Different metals have different barrier heights with a certain material, thus the etching behaves much differently. It is worth noting that there is no etching without metals. Figure 2.2 illustrates the chemical reaction at the metal/substrate interface.

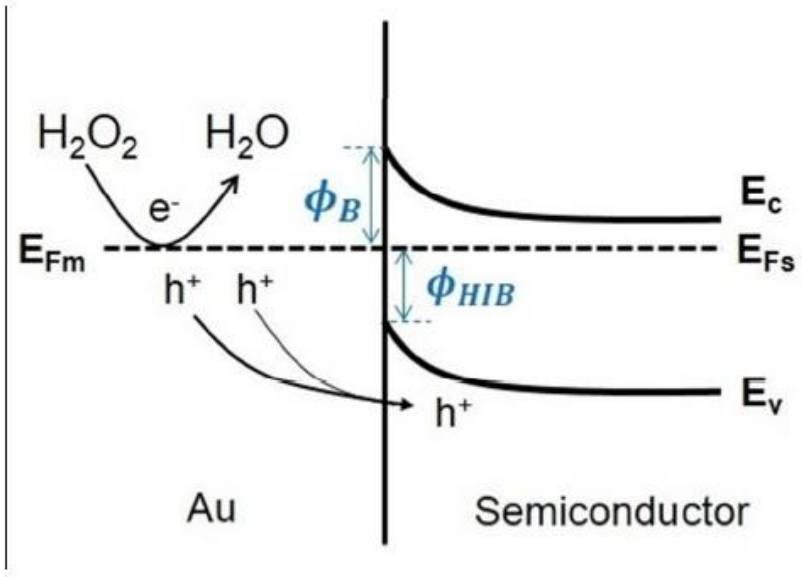

Figure 2.2: Schematic of Au/semiconductor interface for the mechanism of MacEtch. Reprinted with the permission from [60].

MacEtch comprises two steps: a charge transfer process and a mass-transfer process. In the charge transfer process, the metal (Au) catalyst and semiconductor (InP) can be considered as a cathode and anode, respectively. The metal catalyst provides electrons which react with the oxidant H_2O_2 at the cathode as:

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+$$

The appropriate work function of metal is the key to achieve the charge transfer process.

Holes are generated in this step and further react with InP and H_2O at the anode (InP): [61]

$$\text{(i) } InP + 4H_2O + 8h^+ \rightarrow InPO_4 + 8H^+, \text{ or}$$

$$\text{(ii) } InP + 0.55H_2O + 8h^+ \rightarrow 0.5In_2O_3 + H_3PO_4 + 8H^+$$

In the mass-transfer process, the generated In- and InP based oxides are dissolved in H_2SO_4.

There is a significant difference between the inverse MacEtch presented here and the traditional MacEtch. In our structure, there is thick P-rich oxide layer right beneath the metal catalyst which prevents further oxidation. Au catalyst is responsible for the formation of an interfacial, P-based oxide layer that cannot be dissolved in H_2SO_4 during MacEtch. Therefore, the following etching preceded by the hole diffusion into the InP substrate. The thin In-rich oxide layer along the sidewalls can be dissolved by H_2SO_4, and MacEtch is proceeding.

From the crystallographic dependence study, we found the Au patterns oriented at 45° relative to the primary <110> flat on (100) surface, which is good to form perfectly anisotropic etching profile. This is because the facets with the low index {010} planes instead of high-index planes are most exposed to the etching solutions. The concentrations of H_2SO_4 and H_2O_2 were optimized to obtain the best controllable etch rate and vertical etching profiles. The top P-rich oxide layer collapsed onto the sidewall after MacEtch and was removed by dilute HF solution. Figure 2.3 shows the InP nanostructures with different patterns. The structures include highly ordered arrays of nanopillars from ~1.1 μm^2 Pt square pads (Figure 2.3(a); note that the InP pillars are directly beneath the Pt pads), arrays of nanoscale fins after Au removal (Figure 2.3(b)), microscale mesas forming the letters UIUC (Figure 2.3(c); inset shows a high-magnification view of squared area from the letter 'I' where the InP block sits directly beneath the Au pad), and circular InP microstructures from concentric Au rings (Figure 2.3(d)). These images demonstrate that the i-MacEtch process can be implemented to fabricate three-dimensional (3D) InP micro and nanostructures from various metal patterns, whether the pattern is linear, circular, discrete, or continuous. The comparison of two noble metals widely used for MacEtch, Pt and Au, is studied first. The Pt and Au layers were patterned by SL on the InP

substrates in Figure 2.4(a) and 2.4(b), respectively. The Pt serves as a strong catalyst to assist chemical etching which is highly anisotropic with vertical sidewalls. Au has a higher barrier with InP such that fewer holes are generated, thus it is more dominated by chemical etching. Therefore, vertical sidewall is only obtained for a certain orientation (45º relative to the primary <110> flat) where etching is fastest in the lowest atomicdensity plan. We also have a control etching shown in Figure 2.4(c) that uses a photoresist SU8 as hard mask. There is no etching at all using the same etching solution as the ones with metal catalyst, which verifies that metals do serve as important catalysts to initiate the etching and direct the etching behaviors.

Figure 2.5 shows SEM images (after Au removal) obtained at plan-view (a,d), low-magnification 45° tilted-view (b,e) and high-magnification 45° tilted-view (c,f) of InP nanostructures formed by i-MacEtch using the two distinct pattern orientations indicated. Note that the pattern orientations shown in Figure 2.4 are the same as in Figure 2.5(d). It can be seen that vertical sidewalls on all four sides are achieved (Figure 2.4(c)), where the Au patterns are oriented at 45° relative to the wafer flat edge, so that the low-index {010} planes are the facets most exposed to the etching solutions. Conversely, when the Au patterns are oriented at 90° relative to the primary (110) flat edge (Figure 2.5f), in addition to the perpendicular {010} planes, as in the case of purely masked wet etching [62], sloped facets that are presumably the slow etch (211)A facets are also produced. Thus, only the 45° orientation of the metal patterns is suitable for the formation of perfectly vertical nanostructures having (100) sidewall facets, while a 90° oriented metal pattern leads to the formation of features having multifaceted geometries with high-index sidewall facets. Asoh et al. also noted crystal orientation-dependent anisotropic etching in their study of Pt-assisted InP etching [63].

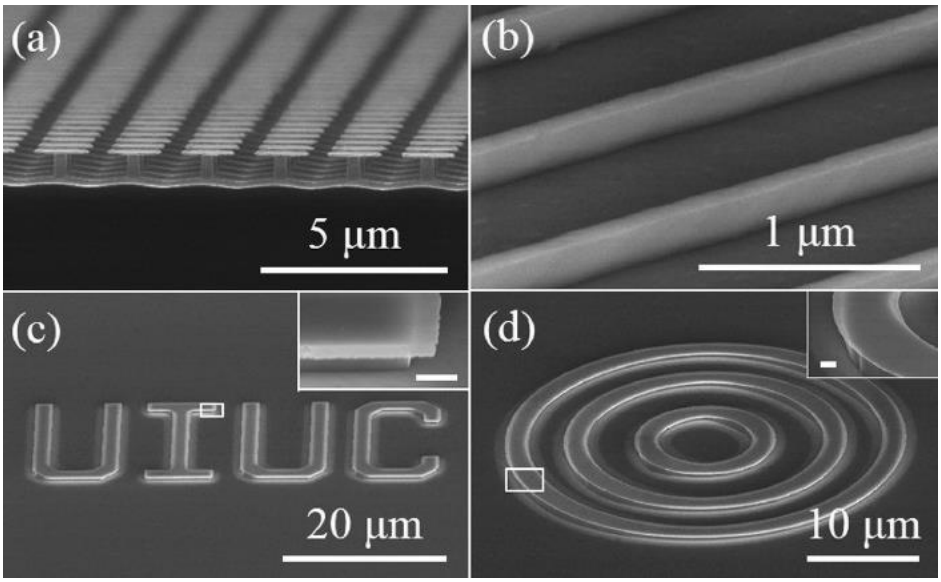

Figure 2.3: InP nanostructures generated from i-MacEtch: (a) arrays of nanopillars generated from Pt square pads, (b) arrays of nanoscale fins from Au lines after Au removal, (c) the letters "UIUC" from Au pads with inset showing a high-magnification view of the outlined region (white box) corresponding to the letter "I", and (d) concentric InP microstructures generated from a set of Au rings, with inset showing the high-magnification view of the outlined region. The inset scale bars are 500 nm and metal catalyst layers were patterned by SL (a) and EBL (b−d). Reprinted with permission from [60].

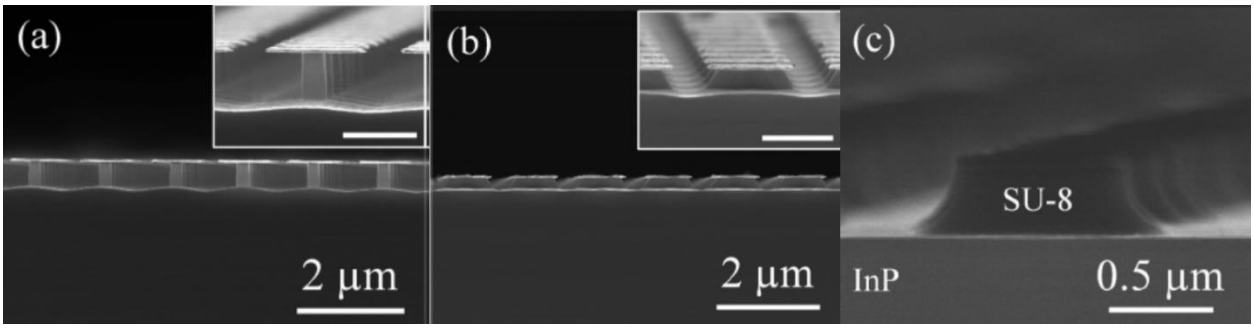

Figure 2.4: Cross-sectional SEM images of InP pillar arrays formed by i-MacEtch with metal catalyst patterns (sitting on top) made of (a) 30 nm thick Pt and (b) 30 nm thick Au disks. (c) i-MacEtch control experiment: SEM shows no etching with SU-8 as a mask. Inset scale bars represent 1 μm. Reprinted with permission from [60].

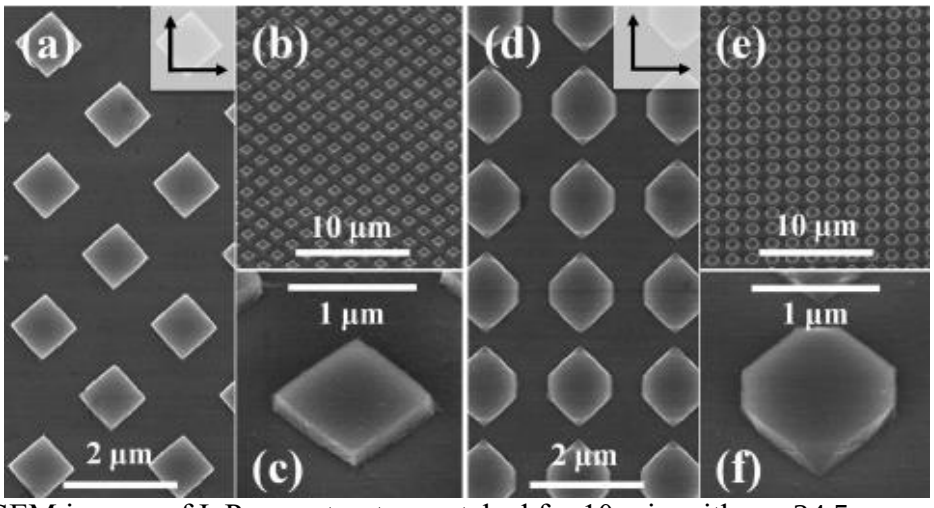

Figure 2.5: SEM images of InP nanostructures etched for 10 min with γ = 24.5 at room temperature, where the square Au catalyst patterns (removed before SEM) were aligned at (a–c) 45° and (d–f) 90° relative to the (110) wafer flat edge (the two arrows in the top-view images indicate equivalent ⟨110⟩ directions). (a,d) panels show plan-view images, while (b,c,e,f) were obtained at a 45° tilted angle. Reprinted with permission from [60].

2.3 Fabrication of high-aspect-ratio InP FinFET by MacEtch

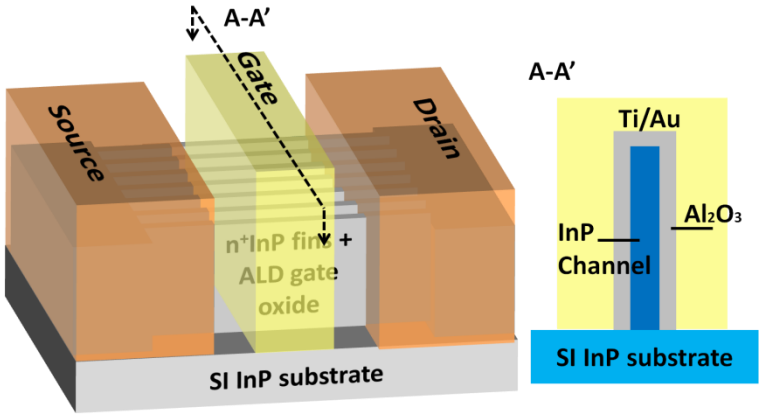

Figure 2.6: Schematic representation of the final device structure. The cross-sectional view of the InP JL-MOSFET is shown along the A-A' plane in the right-hand-side panel. Reprinted with reference [64].

Figure 2.6 shows a schematic representation of the fabricated InP multigate JL-MOSFET structure. Figure 2.7 depicts the key fabrication steps. The InP FinFET channels were first defined by e-beam patterning on a 600 nm thick MOCVD grown Si-doped (8×10^{17} cm^{-3}) InP epitaxial layer on a semi-insulating InP substrate. After native oxide removal by diluted HF, the

samples were loaded for Au evaporation (30 nm). This was followed by the newly developed inverse MacEtch (i-MacEtch) process, where Au serves as a catalyst to induce local electrochemical etching in a solution of H_2O_2 and H_2SO_4 at room temperature. After the desired aspect ratio was reached, Au was removed in commercially available Au etchant. Figure 2.8 (a)-(b) shows an array of InP fins that are ~20 nm wide and ~700 nm tall. Unique to i-MacEtch, the sidewall etching profile is remarkably smooth, independent of metal pattern edge roughness, and free of ion-induced damage. Figure 2.8 (c) shows a bright-field TEM image of the fin sidewall, which confirms its atomically smooth surface.

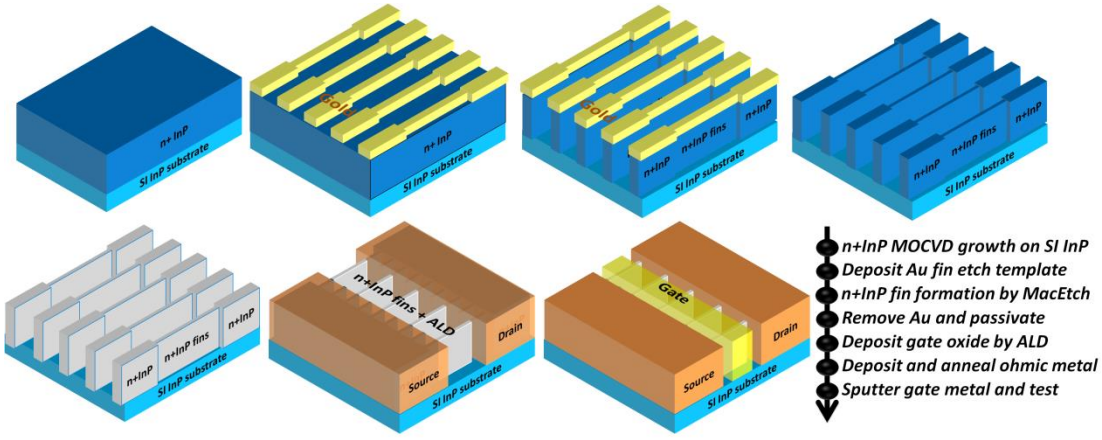

Figure 2.7: Schematic diagram and corresponding description of the process flow for the fabrication of an InP JL-MOSFET by i-MacEtch. The maximum annealing temperature is maintained below 500 °C throughout the whole process. Reprinted with permission from [65].

To fully isolate the fin channels, 700 nm tall fins were formed by intentionally overetching the 600 nm thick doped epi-layer. The samples were dipped into diluted HF 10:1 for 40s to remove the collapsed oxide generated by MacEtch. Then the samples were immersed into diluted 1:1 $(NH_4)_2S$: DI H_2O for 10 min for surface passivation. Al_2O_3 (~10 nm) was immediately deposited by ALD as the gate dielectric, followed by a 30 s RTA at 500 °C. In order to fully wrap the metal contacts over the high AR InP fins, tilted sputtering of Ge/Au/Ni/Au was employed for source/drain (S/D) pads and Ti/Au (10 nm/100 nm) for the gate metal. S/D

contacts were annealed by RTA in N_2 at 400 °C for 30 s. Figure 2.8 (d) shows the cross-section of a single fin conformably covered by the gate stack. Fins with widths as narrow as 15 nm and AR > 50:1 were achieved. Figure 2.9 (a) and (b) show the top and tilted view of the fabricated device.

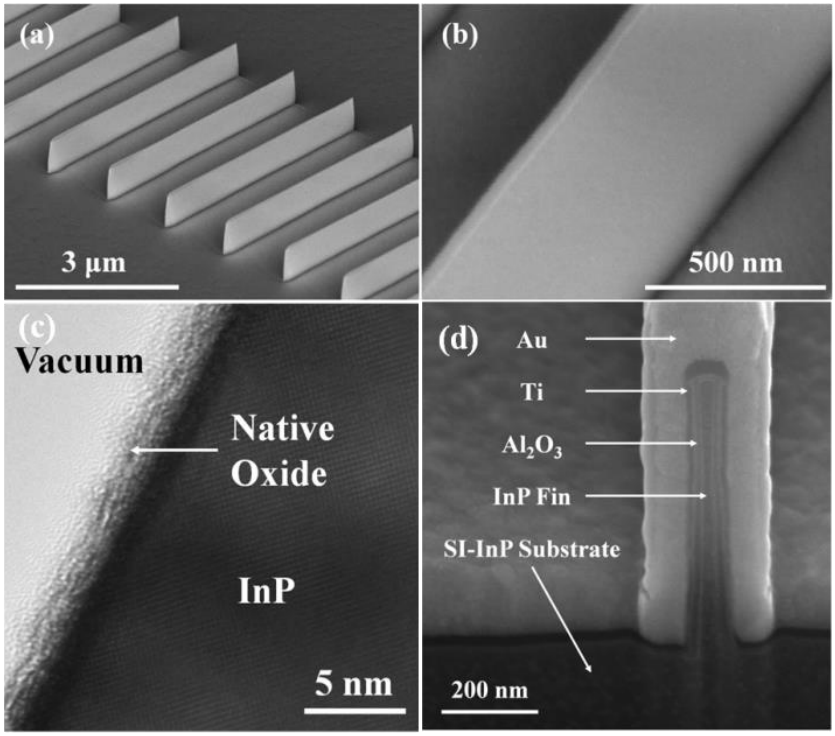

Figure 2.8: 60° tilted-view SEM images of (a) an array of InP fin nanostructures fabricated by i-MacEtch and (b) high-magnification view of the central region of a single fin. (c) HR-TEM image showing the sidewall of a single InP after i-MacEtch; (d) 52° tilted-view SEM image showing the cross-section at the center of a single metal-coated 14 nm wide InP fin with aspect ratio ~50:1. Reprinted with permission from [65].

Note that the on-state performance, including transconductance g_m and drive current I_{on}, is reasonable for a long channel device with un-optimized parasitics (similar to a long channel Si junctionless transistor in [50]). We would also like to point out that the unprecedently high-aspect-ratio (50:1) fins used in this work for device farbication greatly raised the difficulty in processing. We indeed attempted to scale down the channel length. However, due to the extremely tall fins, the topological uneveness was so huge that it was difficult to do sub-100 nm

feature patterning in a university lab. We first spun thin e-beam resist PMMA (200 nm) on top of the fins for source/drain patterning. Disconituity of PMMA coverage of the fin sidewalls could easily occur due to the poor conformality of spin coating for these deep trenches. Therefore, after S/D metal sputtering and lift-off, metals could still be connected as shown in Figure 2.10 because there was no PMMA coating along the fin sidewall between source and drain where it should have been. For this reason, we had to significantly increase the thickness of PMMA to ~600 nm and raise the corresbonding dose and energy during e-beam lithography. The minimal feature size that can be written has been greatly increased due to the imposed extreme lithography condition. It is almost impossible to pattern sub-100 nm features using a 600 nm thick resist.

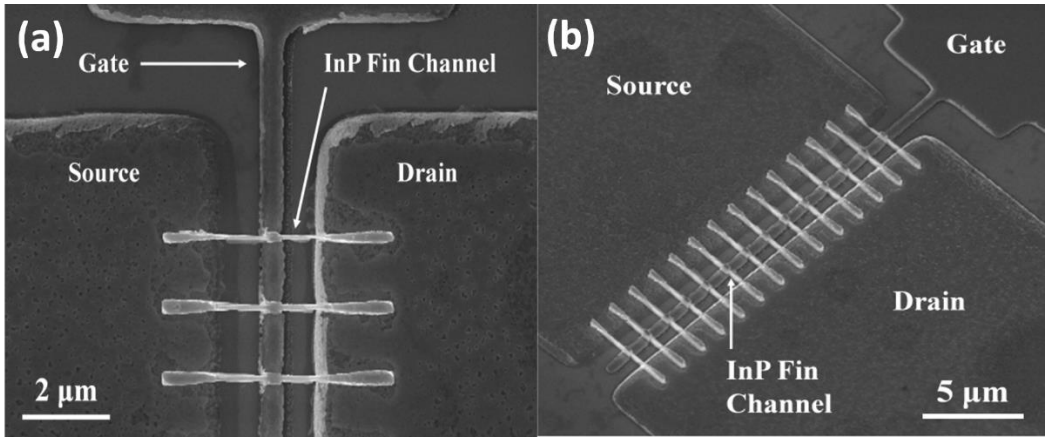

Figure 2.9: (a) Top-view and (b) tilted view SEM image showing the final JL-MOSFET structure. As shown, the gate is centrally aligned between the source and drain.

We do expect much better performance as long as a shorter channel length device can be fabricated by developing advaced 3D process technology, such as resist reflow [66], disperse coating [67], spray and electrodeposition [68], or directed self-assembly nanolithography [69]. The optimization could be achieved by many other ways, like lithography innovation (may be incorporated with CMP and other plannarize methods) and/or S/D regrowth to minimize the offset resistance. Those technology optimizations need to be explored extensively, but they are beyond the scope of this work. We emphasze that we have fabricated a FinFET with 50:1 aspect

ratio here, which definitely imposes a great barrier in 3D processing. On the other hand, FinFETs may not require such a high-aspect-ratio in the near future. Lower aspect ratio (e.g. 10 – 20 to 1) FinFETs, which can be controllably produced by our etching method, may not pose severe processing difficulty. We chose an ultra-high-aspect-ratio (50:1) structure in this work so that the ultimate potential of this method can be demonstrated. We sincerely hope that the significance of this demonstration still holds despite the processing challenge and resulting performance compromise.

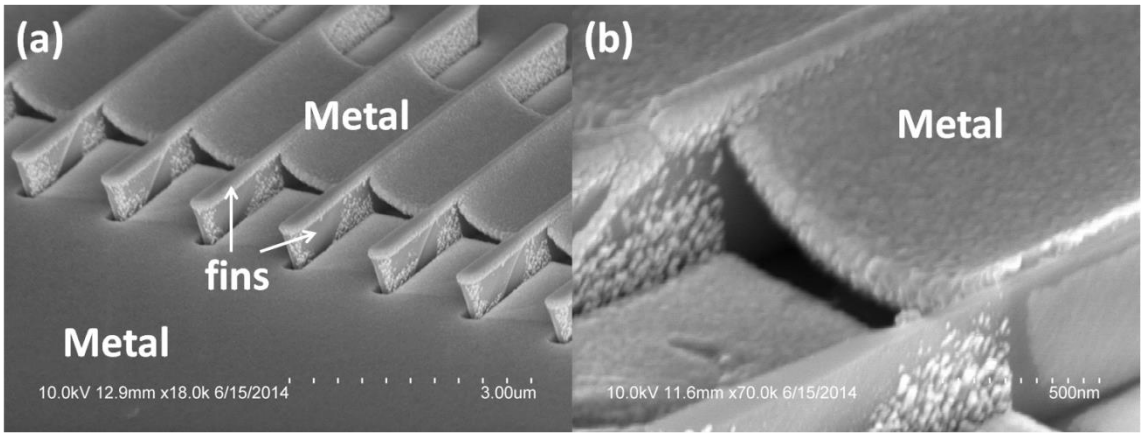

Figure 2.10: Failure example showing metal lift-off above the tall fins patterned using a 200 nm thin e-beam resist. (a) SEM image after source/drain metal desposition and lift off using a thin PMMA layer (200 nm), when the original fin height is 700 nm, (b) zoomed view of the non-removed metals on top of gate region due to poor conformal PMMA coverage on the tall fin sidewalls.

2.4 Device characterization and discussion

To reveal the superiority of MacEtch for device application, we have done the device characterization on Agilent4200. Figure 2.11 shows the electrical performance of a device with an array of 14 fins with gate length L_g = 560 nm, fin width W_{fin} = 20(32) nm, and height H_{fin} = 600 nm. The sub-threshold slope (SS) extracted from the transfer curves (Figure 2.11 (a), (b)) is ~ 70/80 mV/dec, respectively. The device is sharply turning on/off, which is due to the enhanced gate electrostatic control over the extremely narrow fins with low interface states density [70]

fabricated by MacEtch. The on/off ratio reaches as high as 5×10^5, which is comparable with the state-of-the-art techniques [71]. There was no hysteresis when sweeping V_{gs} in opposite directions. These are direct indications of high interface quality with minimum mobile charges or traps between the etched fin surface and high-k dielectric. The high negative V_{th} is attributed to the low gate work function and fixed oxide charges, which was extracted by TCAD simulation to be on the order of 7×10^{12} cm^{-2}. The drive current reaches 52(160) μA/μm at $V_{ds} = 1$ V for the $W_{fin} = 20/32$ nm devices, respectively.

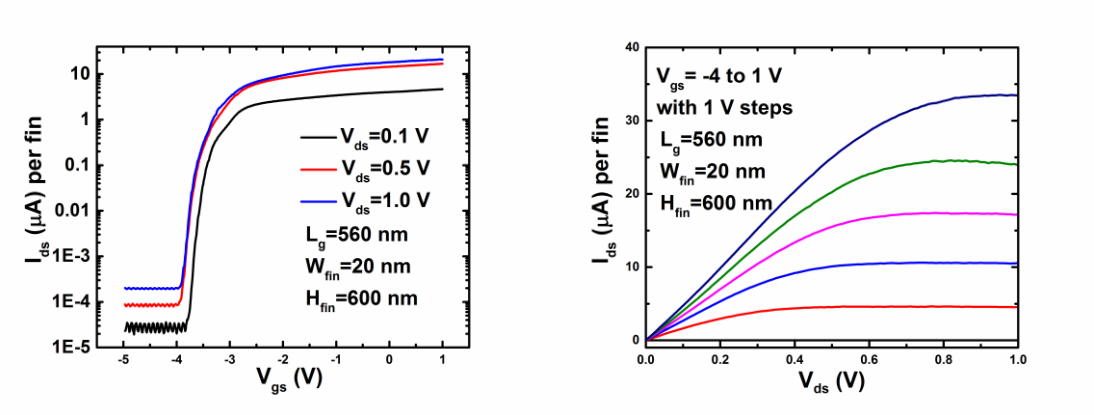

Figure 2.11: (a) I_{ds}-V_{gs} semi-log curves and (b) I_{ds}-V_{ds} curves of representative devices with W_{fin} = 20 nm, showing abrupt turn on in the subthreshold region. Reprinted with permission from [65].

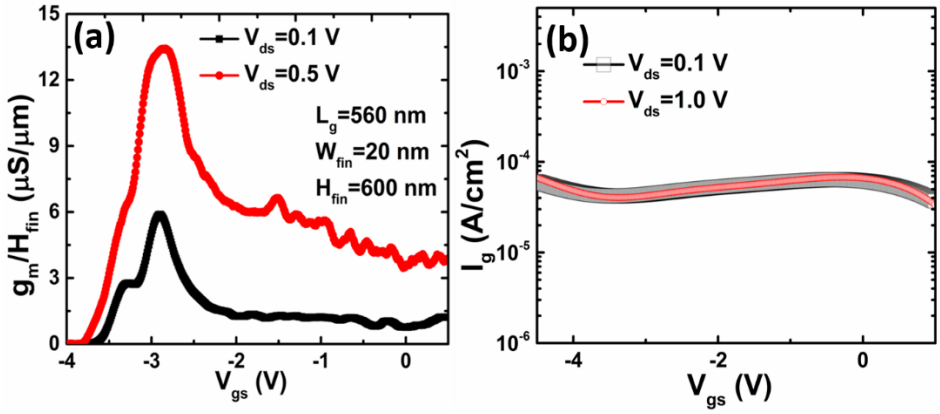

Figure 2.12: (a) normalized g_m-V_{gs} curves and (b) I_{gate}-V_{gs} curves of representative devices with W_{fin} = 20 nm.

Note that the current is normalized by the fin height (not width). If we increase the aspect ratio of fins further, the current conducted by each fin will increase accordingly. The aspect ratio cannot be infinitely increased since it introduces difficulty in 3D nano-patterning process. The plots of the two terminal I-V curves prior to the gate metal deposition show total resistance of 0.8 kΩ and 2.8 kΩ respectively. We intentionally widen the S/D terminals by forming a dumbbell-shaped metal catalyst pattern (Figure 2.9) to reduce the contact resistance. However, the contact separation is still large (2 μm). Figure 2.12(a) shows the normalized transconductance g_m vs. V_{gs}. The relatively small g_m is due to the large parasitic source/drain resistance. One of the key concerns is to reduce the source/drain contact distance to further improve the transistor performance by reducing the parasitic resistance. Much higher I_{on} can be expected if the S/D region is optimized, either by employing advanced patterning methods to shrink the contact distance, epitaxial regrowth in S/D extension area, and/or increasing the channel doping concentration. Figure 2.12(b) shows the normalized gate leakage current at V_{ds} = 0.1 and 1 V, which is extremely low ($4e10^{-5}$ A/cm^2), results from good isolation of the gate from S/D. Therefore, the gate leakage is not contributing to the device leakage I_{off} in this case. Since I_{off} for devices with different W_{fin} are nearly identical, the major device leakage conduction should come from the substrate instead of the device channels, as measured from the substrate. The gate stack can effectively turn off the narrow fin channel so that almost no leakage current flows through the fins. Substrate engineering is the only way to further reduce the on-current [72]. V_{th} and the I_{on}/I_{off} ratio change gradually with W_{fin}. Smaller W_{fin} (below 30 nm) is beneficial for reducing V_{th} while maintaining relatively large I_{on}/I_{off} ratio. Figure 2.13 (b) plots SS as a function of W_{fin}. Due to the strong gate electrostatic control enabled by the high AR structure, even the widest fin width (W_{fin} = 60 nm) device shows a low SS (120 mV/dec) and DIBL (110 mV/V).

The extracted low field effective electron mobility approaches the bulk value as W_{fin} increases (Figure 2.13 (a)).

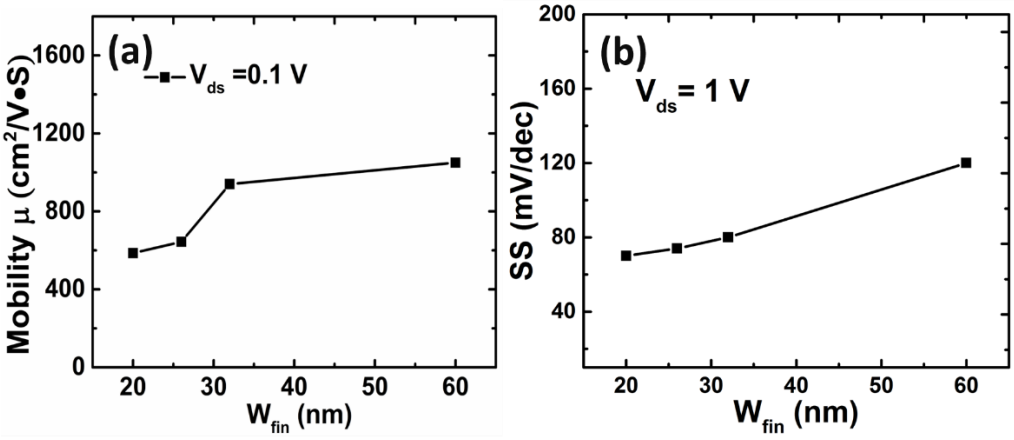

Figure 2.13 (a) The extracted low-field electron mobility μ vs. W_{fin}. (b) Subthreshold slop Ss vs. W_{fin} for InP FinFETs with L_g=560 nm, EOT= 3.9 nm and active fin height H_{fin} = 600 nm. Reprinted with permission from [65].

Although it is not easy to do an absolutely fair performance benchmarking since the on-state performance can be easily traded with other device metrics, such as much larger parasitic capacitance and/or worse off-state performance (Ss, I_{off} etc.), we provide Table 2.1 for comparison of different FinFET structures including stacked nanowires for the same purpose of high current per unit surface area. Channel length L_c is defined as the distance between metallurgical junction of S/D and channel in inversion mode transistor, while L_c simply represents the S/D contact distance in a junctionless transistor. From Table 2.1, we can conclude that the absolute value of I_{on} that a single fin can conduct in a low-aspect-ratio FinFET remains low [50], even if the channel length is aggressively scaled [73]. The stacked channel device either suffers from severe parasitic problem that leads to a low I_{on} [74], or non-uniformity issue due to 3D process challenge that results in unacceptable leakage and Ss [75]. Our prototype ultra-high-aspect-ratio FinFET demonstrated here shows reasonably high current per fin due to the increased conducting volume and low off-state leakage. It does not suffer non-uniformity due

to the excellent etching control. Therefore, our method represents a big step towards super-high current density electronics.

Table 2.1: Comparison of figures of merit of different technologies

Ref	L_g	L_c	EOT	V_{DD}	I_{on} per fin/stack	Perimeter per stack	I_{off} per fin/stack	Ss	Type
[50]	1 μm	N/A	10 nm	1 V	0.25 μA	70 nm	2 pA	63 mV/dec	FinFET
[74]	250 nm	N/A	4.3 nm	1 V	20 μA	113 nm	1 pA	62 mV/dec	Stacked channel
[73]	14 nm	N/A	N/A	0.8 V	33.7 μA	100 nm	4.2 nA	67 mV/dec	FinFET
[75]	1 μm	200 nm	4.5 nm	1 V	480 μA	480 nm	N/A	94 mV/dec	Stacked channel
This work	560 nm	1.8 μm	4.3 nm	1 V	7.2 μA	1200 nm	0.1 nA	63 mV/dec	FinFET

A novel technique, i-MacEtch, has been developed for sculpting III-V materials with highly anisotropic, high-aspect-ratio profiles to replace the traditional dry etching method in the semiconductor device fabrication process. We implement it into the fabrication of InP JL-FETs with ultra-high ARs, without the need for dry etching, ion implantation, or high temperature annealing, which is the revolution to redefine the traditional FinFET fabrication. These are all crucial to maintain the quality of high-k/III-V material surfaces and interfaces. The fabricated devices with narrow fin widths exhibit excellent on-state performance and near-ideal SS. Because of the simplicity, scalability, and high compatibility, we believe the III-V i-MacEtch can be incorporated into III-V transistor fabrication for future III-V based circuit manufacturing.

2.5 Theoretical investigation of the scaling behavior of high AR on JL FinFETs

The recently reported JL FinFETs showed very low on-state current (~0.03 μA per fin at 1 V overdrive) [50], presumably due to the fairly low AR (<1/3 with W_{fin} = 30 nm and H_{fin} = ~ 10 nm) in addition to the low electron mobility of silicon. In comparison, the on-state current

measured from the high AR (> 30 for the active fin) InP FinFET is much higher, and it can be further increased if we continue to increase the fin AR by further etching. Preliminary simulation studies were carried out by TCAD simulation to investigate the ultimate scaling behavior and design rules for this type of high AR FinFETs using experimental, carefully calibrated TCAD model parameters.

2.5.1 Device operating principle and optimization process

$$I_{on,\,flatband} = q\mu N \frac{H_{fin} W_{fin}}{L_c} V_{dd} \tag{2.1}$$

At flat-band condition, the drain current of JL FinFETs can be expressed as (2.1), where μ is the mobility, N is the carrier concentration, L_c is the channel length, V_{DD} is the supply voltage, W_{fin} is the fin width and H_{fin} is the fin height. $I_{on,\,flat\,band}$ can be simply increased by increasing N, W_{fin} or H_{fin} and reducing L_c. However, due to the limited bias swing of power supply, I_{on} usually cannot reach the flat band condition even at the highest bias V_{dd}. I_{on} can be simply denoted as:

$$I_{on} = \alpha\,(N, W_{fin}, C_{ox}) \times I_{on,\,flat\,band} \tag{2.2}$$

where $\alpha\,(N, W_{fin}, C_{ox})$ is the function of N, W_{fin} and C_{ox} for a specific technology node with known L_c and V_{dd}. It is expected that $0 < \alpha < 1$ in a low power supply system. Larger C_{ox}, smaller N and smaller W_{fin} would increase α because of the suppressed SCE. Therefore, both increased available conduction carriers and suppressed SCE are indispensable to maximizing the on-state current.

Traditional channel length L_c scaling requires increasing doping concentration and reducing W_{fin}, which is quite difficult to scale technically. Incredibly high N helps deliver more current. However, W_{fin} has to be aggressively scaled correspondingly (W_{fin}<5 nm when N is greater than 1×10^{20} cm^{-3} [76]) for maintaining good electrostatic control. Such extreme values are impractical

to achieve in experimental processing. There is unacceptable performance fluctuation among different devices. Therefore, channel doping concentration N and fin width W_{fin} have to be considered comprehensively in order to get the highest performance at a particular channel length L_c. As shown in Figure 2.14 (a), at a fixed L_c=100 nm and N=1×10^{18} cm^{-3}, the maximum I_{on} first increases with the increase of W_{fin} because of the increased conduction area. After reaching a maximum point, the I_{on} reduces due to the worse Ss results from a weaker gate electrostatic control. As shown in Figure 2.14 (b), for a fixed N (i.e. W_{DM}) and L_c, there is also an optimal W_{fin} for the highest I_{on}. I_{on} increases with the reduction of W_{fin} because of stronger electrostatic control. After reaching a maximum point, it reduces with further reduction of W_{fin} because of the reduced current conduction volume where gate electrostatic control is already strong enough to yield a low Ss.

We plot the maximum I_{on} for each technology node for three different doping concentration levels as shown in Figure 2.14 (c). All devices simulated here have the same total area (500 nm × 500 nm), which means a shorter L_c has a larger S/D thus lower S/D resistance. Increasing N can improve I_{on} as expected for all L_c. Interestingly, for a fixed doping level, I_{on} has a non-monotonic relationship with L_c. I_{on} first increases with the reducing of L_c due to reduced S/D distance. After reaching a peak point, it decreases with further reducing L_c because of severe short-channel effects. The transition points move lower as N increases. When N is higher than 8e18 cm^{-3}, the optimal W_{fin} requires below 10 nm which can be considered infeasible experimentally. Correspondently, we also plot the scaling behavior of L_c vs. I_{on} for three different W_{fin} as shown in Figure 2.14 (d). A similar phenomenon is observed that I_{on} first increases with the reduction of L_c. However, the slope of I_{on}-L_c is small because higher N is chosen for longer L_c devices, which counteracts the effects of larger S/D resistance due to smaller S/D area. After reaching a

maximum point, I_{on} reduces due to more severe short-channel effects. Unlike ultra-thin body layer or low AR fins, the maximum allowable W_{fin} doubles theoretically in the high AR double-gate FinFETs, thus doubling the available conduction carriers per fin.

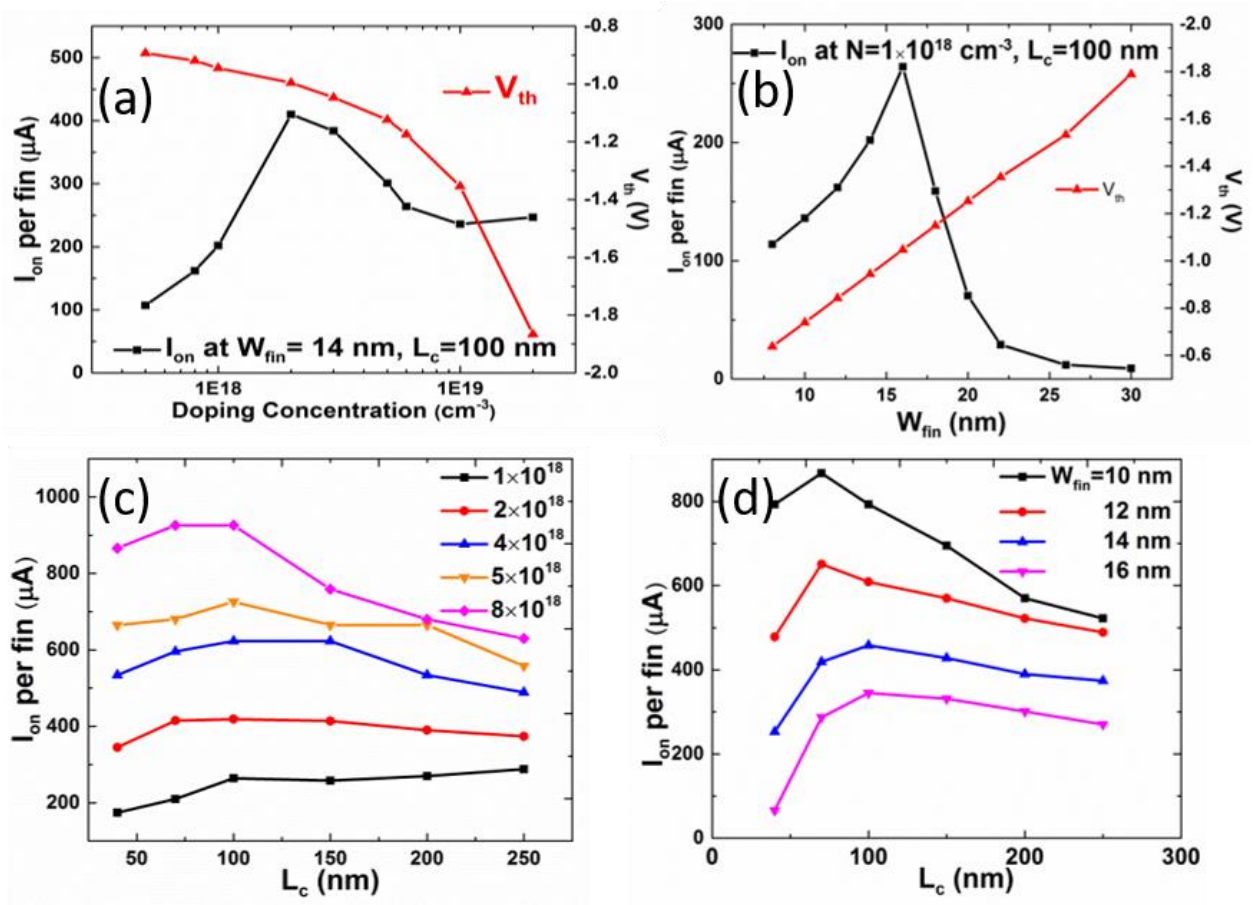

Figure 2.14: Simulated device performance. (a) I_{on} vs. doping concentration (N) for L_c=100 nm, H_{fin}=700 nm, W_{fin} =14 nm; (b) I_{on} vs. W_{fin} for L_g=100 nm, H_{fin}=700 nm and N=1×10^{18} cm^{-3}; (c) the maximum I_{on} vs. L_g for different channel N from 1×10^{18} to 8×10^{18} cm^{-3} and H_{fin}=700 nm; (d) the maximum I_{on} vs. L_g for different fin width W_{fin} from 10 to 18 nm and H_{fin}=700 nm; I_{on} were extracted at $V_{gs}=V_{off,\ state}+V_{dd}$, $V_{ds}=V_{dd}$=0.8 V, and $V_{off,\ state}=V_{gs\ at\ Ids=100\ nA}$. EOT =1 nm for all simulated devices.

2.5.2 Projections for the ultimate scaling performance

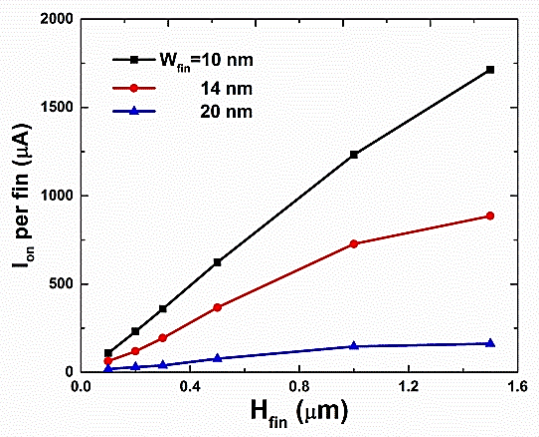

Figure 2.15: Modeled I_{on} vs. H_{fin} for a fixed L_c=100 nm, W_{fin} =10, 14 and 20 nm, EOT =1 nm and N is optimized for each W_{fin} and L_c; I_{on} were extracted at $V_{gs}=V_{off,\ state}+V_{dd}$, $V_{ds}=V_{dd}$=0.8V, and $V_{off,\ state}=V_{gs\ at\ Ids=100\ nA}$. All simulated devices have identical total area (500 nm × 500 nm).

Considering the scaling limitations, we found the highest theoretical value for I_{on} can reach 0.6 mA per fin, corresponding to L_c=150 nm for W_{fin}=12 nm, H_{fin}=700 nm and $N=4\times10^{18}$ cm^{-3}. Further increasing N or reducing W_{fin} reduces carrier mobility significantly due to the ionized dopants scattering and surface roughness scattering. It also causes unacceptable threshold fluctuation due to device parameter variation by process. In terms of lateral transistor scaling, the bottleneck set by the structural limitation and the increasing cost to reduce L_c, i.e. severe short-channel effects and expensive patterning costs, is impossible to solve. The conventional horizontal L_c scaling law fails at this point if W_{fin} and N reach their physical limitation. The only remaining option is H_{fin}, where Figure 2.15 shows nearly linear dependence of I_{on} with H_{fin}. The relation deviates from linear after H_{fin} surpasses 1 μm because the carriers at the bottom channel have to travel a long distance to the surface contact. Through the optimization from Figure 2.14 (a) to (d), it is possible to achieve I_{on} as high as 1 mA/μm at I_{off} = 100 nA/μm even in a relatively long channel device (L_c=100 nm, EOT=1 nm, W_{fin}=12 nm and $N=4\times10^{18}$ cm^{-3}) as shown in Figure 2.15. Such a high on-current rivals the proposed targets for state-of-the-art 14 nm

technology node FinFETs in the International Technology Roadmap for Semiconductors (ITRS) [2] which still has no known solution.

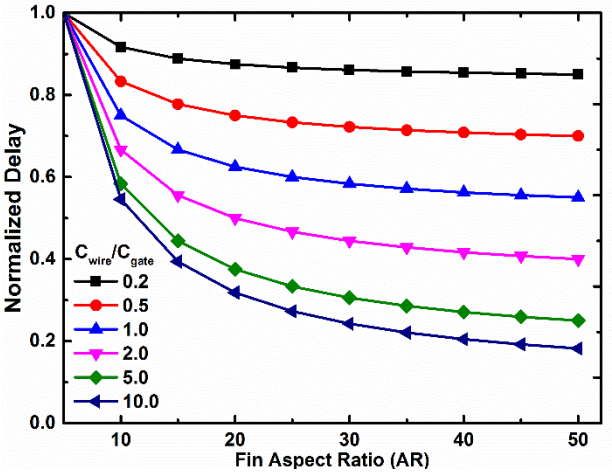

Figure 2.16: Calculated gate delay ($\tau=C_{total}V_{DD}/I_{on}$ and $C_{total}=C_{wire}+C_{gate}$) as a function of fin AR for: C_{wire} per logic gate = 0.2, 0.5, 1.0, 2.0, 5.0 and 10.0 of C_{gate}. The delay values are normalized to the intrinsic delay of FinFET with AR of 5:1.

I_{on} increases at the expense of increased gate capacitance. However, increasing fin aspect ratio would improve gate delay if accounting for the interconnect delays. Like stacking nanowire channels in the vertical direction, increasing fin AR results in much larger active device width in the vertical direction. By itself, higher aspect ratio does not improve intrinsic individual transistor delay ($C_{gate}\times V_{DD}/I_{on}$), but it does improve the total gate delay if C incorporates the external parasitic interconnection capacitance C_{wire} $C_{total}=C_{gate}$ + C_{wire}, where C_{wire} is assumed constant for a certain area [77] that consistent with AR as well as C_{gate}.

The higher AR, the larger C_{gate}; therefore, the relative weight of C_{wire} is sharply reduced. The resulting performance should be significantly improved, which is plotted in Figure 2.16. The equivalent gate delay drops rapidly with increasing of fin aspect ratio, especially at the beginning. The slope is sharper for devices with larger parasitic interconnection capacitance since I_{on} is dominating the delay behavior.

In summary, despite the long channel prototype performance, we demonstrated two major advancements on the state-of-the-art of FinFET technology by using ultra-high-aspect-ratio fin channels:

- We eliminated RIE dry etching and high energy implantation/annealing in III-V FinFET fabrication, which is essential for minimizing ion-induced surface damage and interface states density between the III-V channel and the high-k gate dielectric. As a result, the quality of the InP/Al_2O_3 inteface is significantly improved, which is manifested in the subthreshold characteritics reported: SS close to 60 mV/dec and $I_{on/off}$ is > 10^5.
- We achieved unprecedentedly high-aspect-ratio FinFET. The motivation for raising the fin height is to increase current output per chip surface area, similar to the purpose of stacking channels in the vertical direction. Although this change does not affect the intrinsic transistor switching performance (τ=CV/I) much since the I_{on} increase is canceled by the capacitance C_{gate} increase, it does help to reduce extrinsic delay τ because I_{on} increases faster than C_{total} (which includes both C_{gate} and $C_{interconnect}$) as fin aspect ratio increases. This benefit would be more pronounced for aggresively scaled circuits where transistors are so densely packaged that $C_{interconnect}$ plays a more and more important role.

CHAPTER 3 – DEVICE STRUCTURE DESIGN FOR ULTIMATE SCALING OF MULTIGATE MOSFETS

Down-scaling of FinFETs into sub-10 nm has met tremendous challenges. The feature sizes such as EOT and fin width are physically limited to atomic level, thus it is getting harder and harder to scale. Abrupt ultra-shallow source/drain junctions are difficult to control below 10 nm technology node. It is hard to make the compromise between on-state current and off-state leakage via doping profile optimization. Therefore, structural innovation would be useful to extend Moore's law by using multigate MOSFETs.

3.1 Challenges with the scaling of FinFETs

The main driveing force for downscaling FinFETs is to reduce intrinsic delay $\tau = \frac{CV}{I}$ and device footprint. Figure 3.1 shows the generalized schematic of a FinFET composed of fin arrays. To maintain excellent gate electrostatic control, there is a minimal requirement for fin width W_{fin}, namely, that the ratio $W_{fin}/L_g<0.7$. Therefore, the minimal feature size is different from the conventional FinFET dimension. When L_g scales down below 10 nm, it is extremely challenging to fabricate fin width below 7 nm. It is a difficult technical problem to pattern such thin fins. It also causes significant fin width variations that result in threshold voltage fluctuations. The extremely narrow fins degrade carrier mobility due to surface roughness scattering and quantum confinement. Scaling fin pitches or fin aspect ratio can reduce device footprint but do not help to improve the intrinsic performance since C and I are assumed to increase proportionally. Another key factor for scaling is the equivalent oxide thickness (EOT) which is also hard to scale beyond 0.7 nm. To push the technology node beyond 10 nm and even 5 nm, innovations in FinFET architecture are highly demanded.

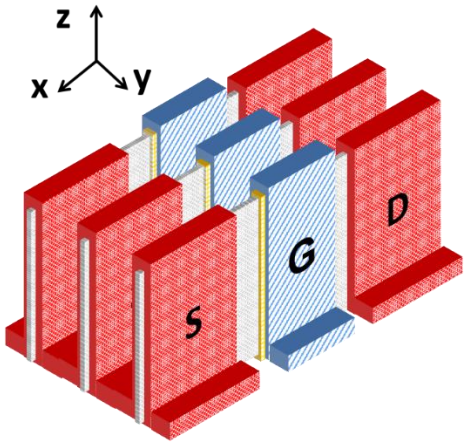

Figure 3.1: 3D schematic of fin array based FinFETs.

Recently, Angada et al. [78], [79] investigated using high-k dielectric spacer to replace conventional low-k spacer in underlap doped FinFET both by TCAD simulations and experimental demonstration. The principle theory is based on the design of underlapped doped FinFET structure to make a compromise between on-state current and off-state leakage. For extremely scaled gate length, the gate fields need to extend to source/drain extension (SDE) to control off-state leakage. Therefore, the doping concentration at SDE should be low. This compromises the on-state current by introducing a large parasitic resistance due to SDE. Figure 3.2 shows the schematic of FinFET with high-k spacer. The high-k spacer has a lower equivalent SiO_2 thickness. Therefore, the gate fringing fields can penetrate the high-k spacer to control the potential of SDE. At off-state, the additional gate field helps to deplete SDE and turn off the transistor so that the off-state leakage can be reduced. At on-state, the fringing gate field helps to accumulate/invert SDE region to boost the carrier concentration. Therefore, a higher drive current I_{on} is expected. The comparison of I-V curves for FinFETs with spacers of different dielectrics confirms the TCAD simulation that a much higher I_{on}/I_{off} ratio is achieved by using high-k dielectric spacers. An inevitable side effect of using high-k spacer is the increased parasitic capacitances C_{gs} and C_{gd}, which add to the total device capacitances. Note that the delay

due to interconnection capacitance is dominating beyond 45 nm technology node. Therefore, the increase of sidewall capacitance does not degrade the overall circuit delay since the current is increasing more compared to the total capacitance. Therefore, there is still a net benefit. Note that the fringing field is not as strong as the planar field which requires a large compensation sidewall capacitance. Another drawback is that the designer cannot choose the permittivity flexibly. On a system level, there are different circuits with different interconnection densities. To optimize the entire system for the minimal delay of each part, one might prefer to choose different high-k spacers for different circuits. However, it is impossible to dynamically change high-k-spacer for different parts of circuits. Therefore, another kind of device structure innovation is required to solve the problems.

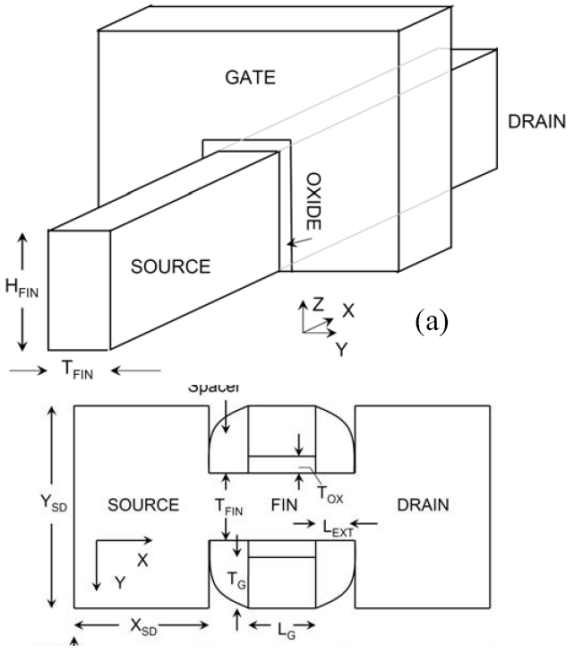

Figure 3.2: Schematic for 3D structure FinFET and cross section showing the high-k dielectric spacer. Reprinted with permission from [78].

3.2 One-sided source/drain extension contact FinFET for low power applications

3.2.1 Background of conventional symmetric SDE FinFET

FinFETs have become the mainstream device architecture beyond 14 nm technology node due to their strong gate electrostatic potential control [1-4]. The distance between S/D contacts has to scale simultaneously with gate length in order to shrink the device size as well as to stimulate ballistic transport [5]. Since the channel would be intentionally left undoped, the heavily doped source/drain (S/D) region would diffuse a considerable amount of carriers towards the channel at on-state at the N^+ (or P^+)/intrinsic junction. Due to the proximity of S/D contacts for aggressively scaled devices, the equilibrium carrier density in the channel will be so high from diffusion and S/D direct tunneling that it will be harder and harder to turn off. Narrowing the fin width below 5 nm [6] to help turn the transistors off is impractical due to demanding fabrication processes, unwanted width fluctuation and severe degraded carrier mobility resulting from quantum confinement and surface scattering. The electrical gate dielectric thickness is hard to scale to meet the low leakage requirement for lower power products [7]. New materials such as III-V compounds [8], new working principles such as tunneling FET (TFET) [9] or new architectures such as nanowire FETs [10], have their own problems such as low on-state current and/or new processing flows that require extensive efforts.

Here, we propose and simulate the performance of a FinFET structure with asymmetric S/D extension (SDE) contact for low power applications. Scaling performances of one-sided and double-sided SDE contact FinFETs are compared and analyzed in detail. By removing SDE contact from one side of the fin, the carriers diffused to the channel would be reduced while retaining the minimal S/D contact separation. We find that a one-sided SDE contact FinFET has much better scaling behavior. The optimized on-state current, I_{on}=0.16 mA/μm at I_{off}=50 nA/μm

and V_{DD}=0.4 V for L_G=10 nm, is higher than the conventional double-sided SDE contact FinFETs and the Si TFET counterpart [11], and even approaches the theoretical value of III-V heterojunction TFETs [12].

3.2.2 Concept of one-sided SDE contact FinFETs

The top-view schematic for a conventional FinFET with gate to S/D underlap [13] is shown in Figure 3.3 (a). The channel is left undoped to improve carrier mobility and avoid random dopant fluctuation. The SDE region is also left undoped to extend gate electrostatic control. To shrink the effective S/D contact separation $L_{S/D}$, one can deposit a highly doped film as shown in Figure 3.3(b), which partially covers the fin SDE.

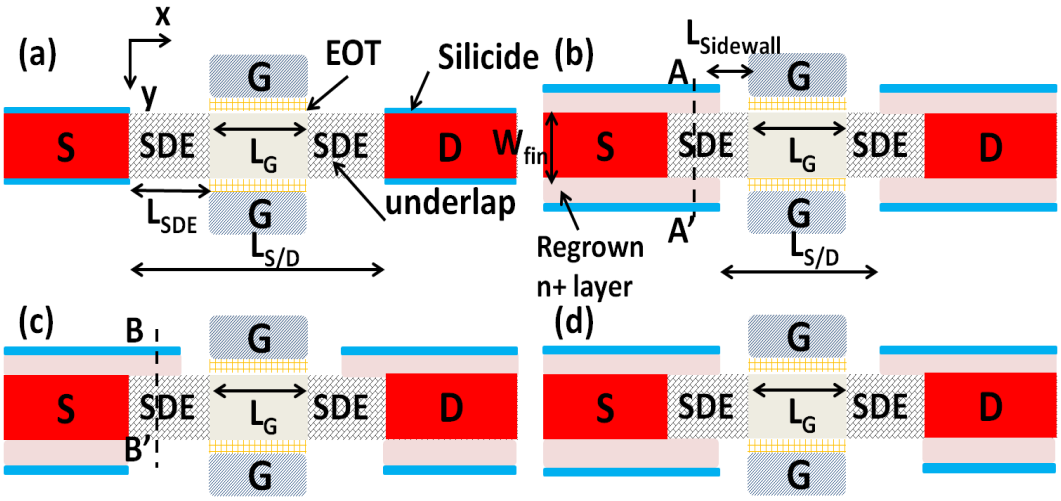

Figure 3.3: Top-view schematic diagrams of (a) double-gate FinFET with gate to S/D underlap: separated by SDE; (b) double-gate FinFET with gate underlap plus regrown highly doped S/D contacting layer; (c) double-gate FinFET with one-sided SDE contact for S/D; (d) double-gate FinFET with drain-only one-sided SDE contact; the fin height is denoted as H_{fin} in the vertical direction.

The basic analysis for FinFET in Figure 3.4 is based on solving Poisson's equation for an ideally abrupt one-sided N^+ or P^+, $(1\times10^{20}\ cm^{-3})$/i (intrinsic, $1.45\times10^{10}\ cm^{-3}$) junction. Carriers diffuse from N^+ (or P^+) to the intrinsic side. Poisson's equation inside the intrinsic layer is expressed as:

$$\frac{d^2\Phi(x)}{dx^2} = \frac{qn_i}{\varepsilon_{si}} e^{q\Phi(x)/kT} \tag{3.1}$$

where $\Phi(x)$ is the potential distribution if we define $\Phi(0) = 0$ at the edge of N^+ side and $\Phi(\infty) = E_g/2$ (where E_g is the band gap) at the neutral intrinsic side. One can solve (3.1) by numerical simulation. The results show that carrier concentration exponentially decreases from 1×10^{20} cm^{-3} (N^+) to 1.45×10^{10} cm^{-3} (intrinsic) over a distance of around 60 nm. If the distance between heavily doped source and drain is less than 120 nm, it cannot return to the intrinsic value n_i. Numerical simulations show the equilibrium carrier concentration reaches over 1×10^{18} cm^{-3} when channel length scales down to 10 nm, which means the transistor is fully turned on even without gate bias. Either a negative gate bias or a midgap metal gate work function is required to turn off by bringing the carrier concentration back to n_i. Similar to a junctionless mode transistor [14, 15], either a lower carrier concentration or a narrower fin width is imperative for better on/off characteristics [16].

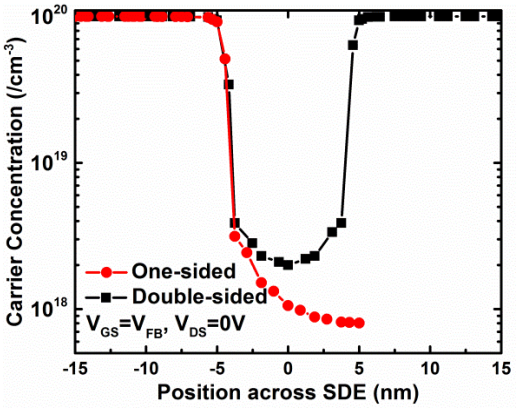

Figure 3.4: Comparison of equilibrium carrier concentration n_{SDE} in the x-axis center of SDE region along y direction between double-sided (along A-A' dashed line in Figure 3.3(b)) and one-sided SDE FinFETs (along B-B' dashed line in Figure 3.3(c)), where [-5 5] is the SDE region.

It is difficult to scale L_G and the S/D contact separation $L_{S/D}$ by lateral doping engineering [17]. This is because the band bend diagram in the intrinsic channel side is insensitive to the

heavily doped S/D side in the N+/i junction, due to the fact that the built-in potential is nearly constant ($E_g/2$) and the intrinsic channel length is short. The lateral doping engineering also increases the effective separation between degenerately doped S/D ohmic contacts, thus increasing parasitic resistance [18].

We now consider removing one side of the SDE contacts (see Figure 3.3(c) for illustration) so that the equilibrium carrier concentration in the SDE region (n_{SDE}) can be reduced, as shown in Figure 3.4. Channel potential can be more flexibly modulated by gate bias because fewer carriers are diffused from SDE region to channel. The gate electrostatic control, and thus the SCE immunity, can be expected to improve, compared with double-sided SDE contact FinFET with identical device geometries.

Carrier concentration at the source side should be higher than the drain side due to current continuity. The drain side is more critical to determine SCE since it competes with the gate to take control over channel potential. Therefore, we consider one-sided drain extension contact only, while keeping the source as double-sided SDE contacts as illustrated in Figure 3.3(d), which should benefit of both I_{on} and SCE.

Device performance was simulated using the 3-D device simulator [19]. Drift-diffusion model with field dependent mobility was adopted. The band-gap narrowing model, band-to-band tunneling model, Shockley-Read-Hall recombination model and density-gradient quantum correction were used. Table 3.1 summarizes the device parameters used in the simulation, including the symbols defined in Figure 3.3. As a validation to the simulation model, Poisson's equation in the n^+ drain side was solved analytically by space charge approximation. The analytical results of $\Phi(x)$ perfectly match with the numerical solutions.

Table 3.1 Design parameters for the simulation of silicon one-sided/double-sided SDE contact FinFETs

Doing Concentration (cm^{-3})	Gate Oxide (nm)	Gate Work Function (eV)	$L_{sidewall}$ (nm)	W_{fin}/H_{fin} (nm)	L_{SDE} (nm)	L_G (nm)
1×10^{20}(S/D)/ 1.45×10^{10} (channel)	0.5	4.5	4	7/50	10	7-20

3.2.3 Performance analysis of one-sided SDE contact FinFETs

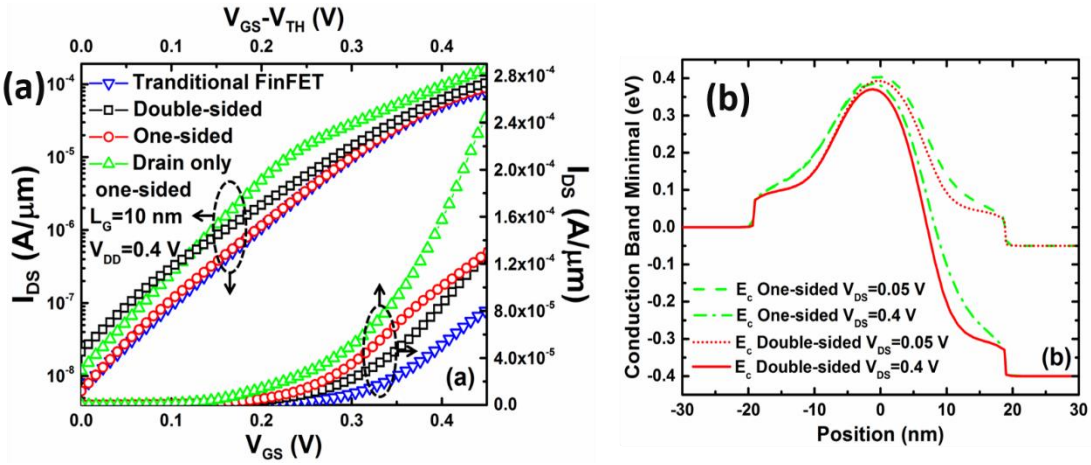

Figure 3.5: (a) The transfer characteristics of double-sided ($L_{S/D}$=18 nm), one-sided SDE contact ($L_{S/D,top}$ =18 nm and $L_{S/D,bottom}$=30 nm), Drain-only one-sided SDE and conventional FinFET with $L_{S/D}$=30 nm and iso-I_{off} leakage; (b) conduction energy band minimal along source to drain for one-sided and double-sided SDE contact FET at off-state V_{GS}=0.0 V when V_{DS}=0.05 V and V_{DS}=0.4 V, respectively.

Figure 3.5 (a) shows the logarithmic and linear plots of transfer curves for the four device architectures illustrated in Figure 3.3 for L_G=10 nm and V_{DS}=0.4 V. From the logarithmic plot, it can be seen that the leakage current I_{off} at V_{GS}=0 V in the one-sided SDE contact structure is ~50 nA/μm, which is lower than that with double-sided SDE contact, while drain-only one-sided FET sits between these two. Note that for the traditional FinFET structure without regrown SDE, although the same I_{off} (50 nA/μm) as with one-sided SDE FinFET at V_{GS}=0 V is achieved, a

much larger source to drain separation (30 nm vs 18 nm) is required, which suffers a significant I_{on} reduction (as will be discussed later). The above observation confirms that a lower equilibrium carrier population in SDE is critical to reduce off-state leakage since the channel is easier to deplete.

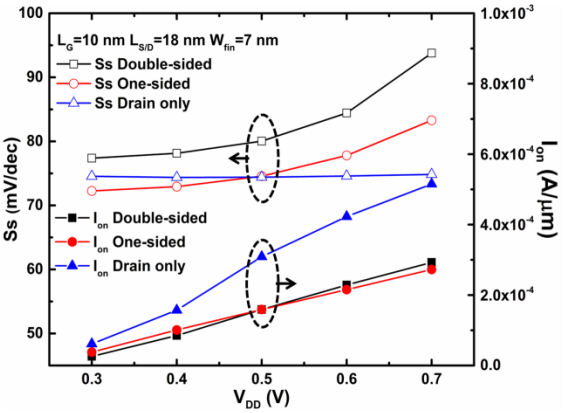

Figure 3.6: The bias dependence of Ss (left y-axis) and I_{on} (right y-axis) for one-sided, double-sided and drain-only one-sided SDE contact FinFETs, respectively.

The underlying physical interpretation is further analyzed by the conduction energy band minimum E_c along the channel at off-state for V_{DS}=0.4 V and 0.05 V respectively, as shown in Figure 3.5(b). In double-sided SDE contact FinFET, the potential barrier height is lowered with the increase of V_{DS} due to its strong drain biasing effect. The effective energy barrier width is also narrowed, leading to worse SCE. In contrast, the lowering and narrowing of potential barrier in the one-sided SDE contact FinFET are significantly attenuated. This wider and taller potential barrier effectively prevents leakage at off-state, and improves the gate electrostatic modulation. The corresponding E_c plot for the drain-only one-sided device sits between the above two, which is not plotted here for legibility. From the linear plot in Figure 3.5(a), it is clear that the conventional FinFET has the lowest I_{on} at the same overdrive voltage (V_{GS}-V_{TH}) and iso-I_{off} condition. I_{on} in the one-sided structure is higher than the double-sided counterpart for V_{GS} below 0.5 V. Remarkably, the drain-only one-sided SDE FinFET has the highest I_{on} (0.16 mA/μm),

which is more than 3x higher than the conventional FinFET (0.05 mA/μm) and 2x higher than the double-sided SDE FinFET (0.08 mA/μm), at iso-I_{off} and V_{DD}=0.4 V.

Figure 3.6 shows the bias dependence of the minimal subthreshold slope (Ss) and I_{on}, when V_{DS}=V_{DD}. As expected, Ss is lower in the one-sided SDE contact FinFET than in its double-sided counterpart for all biases due to better gate electrostatic control. As V_{DD} increases, both Ss are deteriorated due to a larger transverse electric field. Ss in the drain-only one- sided contact FinFET shows a weak dependence on V_{DD}, with values smaller than one-sided counterpart when V_{DD}>0.5 V. This is because of its asymmetric S/D nature, despite its higher equilibrium carrier concentration than its one-sided counterpart. In contrast to the conventional asymmetric S/D MOSFETs, either using asymmetric S/D doping profile [20] or different spacers [21], the drain-only one-sided SDE contact FinFET has asymmetric SDE contact structure with minimal source to drain contact distance $L_{S/D}$ unaffected. As V_{DD} increases, the portion of V_{DD} drops on the drain resistance R_D is larger compared to source resistance R_S since R_D>R_S. On one hand, the effective V_{DS}'≈V_{DS}-I_{DS}×R_D across the channel is reduced due to a larger R_D such that Ss is less degraded with V_{DD}. On the other hand, a smaller R_S results in a larger effective V_{GS}'=V_{GS}-I_{DS}×R_S which is closer to the external V_{GS}, so that Ss is also less degraded with the increase of V_{DD} and I_{DS}.

I_{on} is higher in one-sided SDE FinFET as long as V_{DD}<0.5 V because of a steeper Ss [16]. At low biases, n_{SDE} at the source extension side can follow the increase of inversion carriers in channel, satisfying the following expression:

$$n_{SDE} \geq C_{ox}(V_{GS} - V_{TH}) / (q \times 2H_{fin}) \tag{3.2}$$

where C_{ox} is the gate capacitance and q is the basic charge. When V_{DD} is higher than the crossover (0.5 V), n_{SDE} in the one-sided SDE contact FinFET becomes a bottleneck such that it becomes insufficient to support the increase of inversion carriers in channel $n_{channel}$=C_{ox}×(V_{DD}-

V_{TH}). Therefore, its on-state current falls below that of the conventional double-sided SDE contact FinFET, thus it is better suited for low power applications. The drain-only one-sided SDE FinFET has the largest I_{on} due to both the steep Ss and a small R_S.

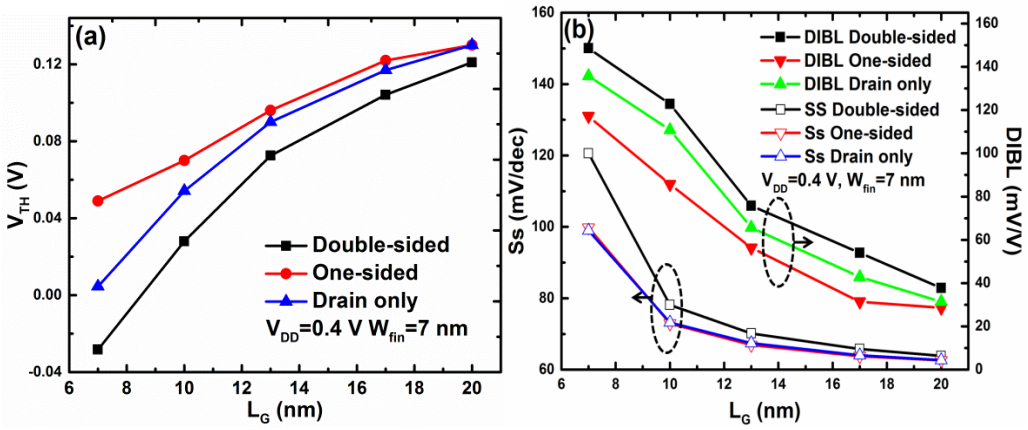

Figure 3.7: (a) V_{TH} roll-off as the scaling of gate length; (b) the rise of subthreshold slope (left) and DIBL (right) at V_{DS}=0.4 V in one-sided, double-side, and drain-only one-sided SDE contact FinFETs.

Figure 3.7 (a) and (b) show V_{TH} roll-off and Ss/DIBL versus physical gate lengths for different SDE contact architectures, respectively. It can be seen that V_{TH} roll-off is suppressed, and Ss and DIBL are reduced in the one-sided SDE contact structure for gate lengths down to 7 nm. The double-sided SDE FinFET exhibits larger Ss and DIBL as expected due to severe SCE for all L_G, but the difference is much bigger when the gate length scales down below 10 nm. The values of V_{TH} and DIBL of the drain-only one-sided SDE contact FinFET sit between the other two due to its medium level of carrier concentration in SDE, but its Ss is similar to that of the one-sided SDE FinFET when V_{DD}=0.4 V. The smaller R_S and higher carrier concentration in the channel counteract their effects on Ss in the drain-only one-sided SDE FinFET. The comparison indicates that the one-sided SDE contact FinFET has the best scalability with the same physical dimensions.

The equilibrium carrier concentration in a FinFET channel becomes incredibly high due to the extreme proximity of S/D contacts with aggressive scaling. We designed a FinFET structure that has double gates but one-sided SDE contact, enabling low power operation with high on-state current (0.16 mA/μm at L_G=10 nm and V_{DD}=0.4 V). By lowering the carrier concentration at the SDE region, the one-sided asymmetric SDE design provides better gate-to-channel electrostatic control and SCE immunity and offers a better design option for sub-10 nm gate length FinFETs.

3.3 Asymmetric gate FinFET for high performance system-on-chip (SoC) applications

3.3.1 Underlapped gate to SDE doping and spacer design

FinFETs have become the mainstream device architecture beyond 14 nm technology nodes due to their strong gate electrostatic potential control [73, 80]. In the off-state, the effective channel length (L_{eff}) needs to be extended by the undoped underlapped source/drain extension (SDE), in order to suppress short-channel effects (SCE) [81]. In the on-state, the carrier concentration in SDE needs to increase so as to minimize parasitic resistance. Down-scaling through conventional lateral doping engineering makes it hard to compromise between SCE and parasitic resistance because it increases the effective separation between degenerately doped S/D ohmic contacts [82]. One can introduce fringing electric field from the sidewalls of the gate to enhance gate electrostatic modulation over SDE [78, 79]. However, the permittivity of high-k spacer needs to be high since the gate fringing electric field is not as strong as perpendicular fields. The permittivity cannot be flexibly chosen according to interconnection density among different system-on-chip (SoC) circuits. Therefore, it significantly compromises the benefits of higher conduction current.

Here, we present a novel FinFET design, which features asymmetric gate lengths along fin sidewalls, through 3-D technology computer-aided design device simulation using Sentaurus Device [83]. Unlike the historically proposed asymmetric gate FinFET [84], a shorter gate is used to shrink the shortest source to drain separation while a longer gate helps modulate channel potential. SCEs are mitigated with fin width (7 nm) even wider than the minimal gate length (5 nm), and conduction-current (as high as 0.75 mA/μm (NMOS), 0.4 mA/μm (PMOS) at V_{DD}=0.7 V) is significantly increased. The overall circuit delay can be minimized by optimizing gate lengths according to different local parasites among circuits in the interconnection delay dominated SoC applications.

3.3.2 Design of asymmetric gate FinFETs

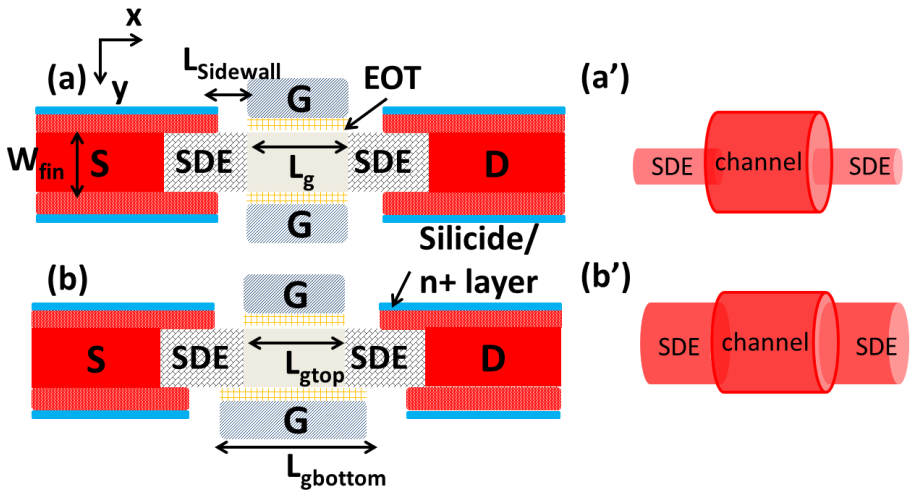

Figure 3.8: Cross sectional schematic top view of (a) conventional symmetric double-gate FinFET and (a') is the pipeline model for carrier populations, showing SDE region is the bottleneck for conduction-current flow; (b) asymmetric gate FinFET, showing top and bottom gates with two different gate lengths L_{gtop} and L_{gbotom}, (b') is the pipeline model showing the bottleneck of SDE region has been removed.

Figure 3.8 illustrates the cross-section across the fin channel region from source to drain, for conventional symmetric gate (a) and asymmetric gate FinFET (aFinFET, b). Channel region as well as SDE are left undoped to ensure high carrier mobility and minimized SCE in both

cases. The heavily doped S/D contacting layers are assumed to be epitaxially regrown on top of fin S/D region and in-situ doped with $2\times10^{20}cm^{-3}$.

At on-state, the carrier concentration in gate overlapped channel region $n_{channel}$ is modulated by gate bias $Q_n \approx C_{ox}\times(V_{gs}-V_{th})$. In conventional FinFET, the carrier concentration in SDE region n_{SDE} is low such that it becomes a bottleneck for current conduction as shown in the schematic in Figure 3.8 (a, right). In aFinFET, it can still be effectively modulated by n_{SDE} due to the gate-to-SDE overlap such that the bottleneck is eliminated (Figure 3.8b, right). At off-state, the channel is more difficult to turn off for conventional FinFET due to the small gate capacitance. In aFinFET, the longer gate assists the short gate to enhance gate to channel electrostatic coupling by additional fringing electric field, which effectively improves SCE and reduces leakage. This kind of aFinFET is experimentally feasible by CMOS compatible fabrication process [85].

Table 3.2 Design parameters for the conventional symmetric and asymmetric gate FinFETs

Doing Concentration	Gate Oxide	Gate Work function	$d_{Sidewall}$ Thickness	H_{fin}	W_{fin}	L_{gtop}
2×10^{20}(S/D)/ 1.5×10^{10}(channel) cm^{-3}	0.7 nm	4.5(NMOS)/4.75 eV (PMOS)	3 nm	50/ 100 nm	7 nm	5 nm

Device performance was simulated using the 3-D device simulator [83]. Drift-diffusion model with field-dependent mobility was adopted. The band-gap narrowing model, band-to-band tunneling model, Shockley-Read-Hall recombination model and density-gradient quantum correction were used. Table 3.2 summarizes the device parameters used in the simulation, including the symbols defined in Figure 3.8.

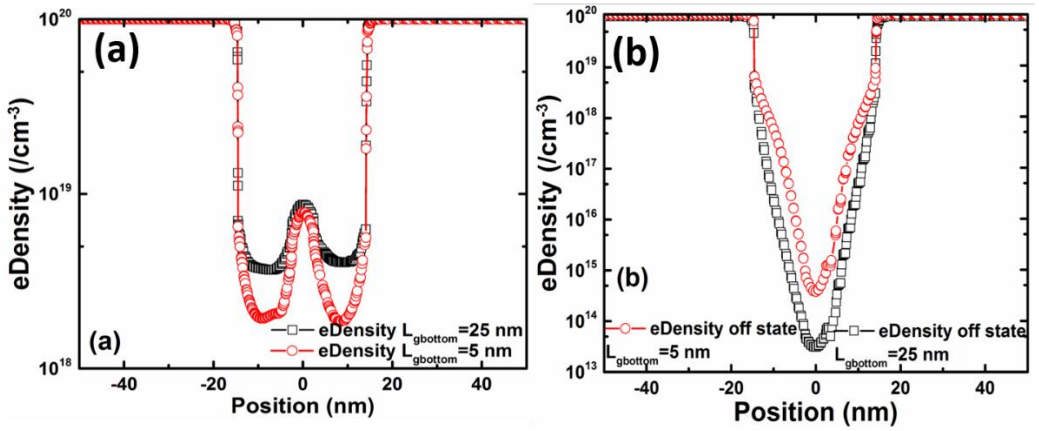

Figure 3.9: Comparison of carrier concentration along channel direction for (a) on-state when V_{GS}=0.7 V, V_{DS}=0.05 V and (b) off-state when V_{GS}=0 V and V_{DS}=0.05 V, where x-axis=0 is the center point of channel. In detail, [-5, 5] is channel, [-15, -5] is the source extension and [5, 15] is the drain extension, beyond which is source/drain region respectively.

Figure 3.9 (a) and (b) show the comparison of equilibrium carrier concentration across channel region between symmetric and asymmetric gate FinFETs at on/off-states respectively. As expected, at on-states, n_{SDE} is increased that approaches $n_{channel}$ in aFinFET compared with conventional FinFET. At off-state, $n_{channel}$ in aFinFET is more than an order of magnitude lower than in a conventional FinFET which results from stronger electrostatic coupling by the extended gate to SDE overlap.

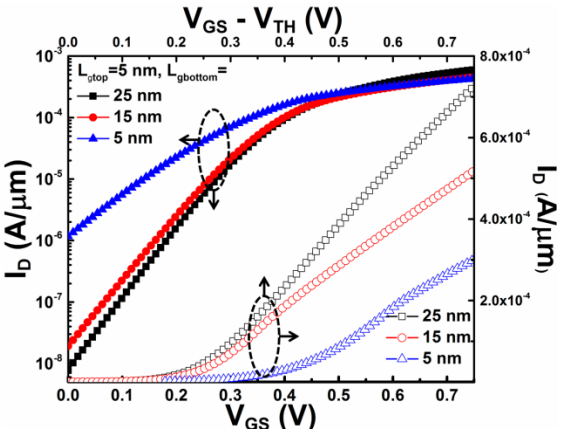

Figure 3.10: Logarithmic and linear plots of transfer curves for the designed FinFET with L_{gtop}=5 nm and three different $L_{gbottom}$=5, 15 and 25 nm respectively. V_{DS}= V_{GS}=0.7 V. All EOT are 0.7 nm, W_{fin}=7 nm, channel is left undoped and S/D is highly doped n-type with $N_{S/D}$=1×10^{20} cm^{-3}. I_{on} was extracted at iso-I_{off}=100 nA/μm.

Figure 3.10 shows the comparison of the logarithmic and linear plots of transfer curves with three different $L_{gbottom}$=5, 15 and 25 nm for NMOS and PMOS respectively, with L_{gtop}=5 nm, $L_{sidewall}$=3 nm and V_{DD}=0.7 V. For symmetric gate FinFET $L_{gbottom}$= L_{gtop}=5 nm, the device can barely be turned off with the lowest on/off ratio (10^2). As $L_{gbottom}$ increases, I_{on} increases due to the increased n_{SDE} and I_{off} reduces due to the reduced $n_{channel}$ as shown in Figure 3.9. The on/off ratio reaches 10^5, which is around three orders of magnitude higher than the conventional FinFET. The highest I_{on} extracted reaches 0.75 mA/μm, which is around 3× higher than conventional FinFET at iso-I_{off}=100 nA/μm and V_{DD}=0.7 V. Note that the excellent device switching performance is achieved with an aggressively scaled source to drain distance of 11 nm. This is an incentive for ballistic transport [86] due to a small footprint.

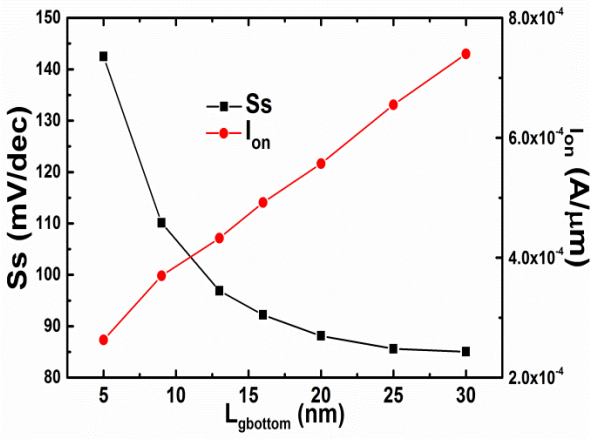

Figure 3.11: Extracted minimal subthreshold slope (SS, left axis) and I_{on} (right axis) vs. different $L_{gbottom}$. SS and I_{on} improve with increasing $L_{gbottom}$, confirming the role of extended fringing gate electric fields that help to improve SCE and increase I_{on}.

Figure 3.11 compares the trend of the minimal subthreshold slope (Ss) and DIBL varied with $L_{gbottom}$ at a fixed L_{gtop}=5 nm. DIBL is extracted as the V_{th} difference between V_{DS}=0.05 V and 0.7 V. As $L_{gbottom}$ increases, Ss reduces from 143 mV/dec to 83 mV/dec and DIBL reduces from to mV/V. The electric fields from the gate extension overlapped with SDE effectively modulate the channel potential. The excellent short-channel behavior is obtained at a fin width of 7 nm,

which is smaller than the minimal gate length (5 nm). The relaxation on fin width is helpful to extend FinFET scaling since the minimal feature relies on gate length rather than conventional fin width. A wider fin should be beneficial for higher carrier mobility and better manufacturability.

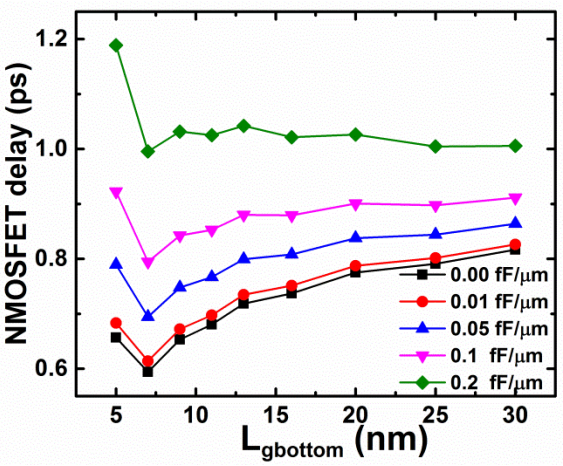

Figure 3.12: Simulated CMOS invertor delay τ vs. $L_{gbottom}$ with different C_{load}. The electrical width for PMOS is twice that of NMOS. The dual-gate work function has been carefully chosen to achieve identical off-state current for both NMOS and PMOS.

One of the main concerns for aFinFET is the increased gate intrinsic capacitance C_{ox}. At a constant V_{DD}, on-current I_{on} increases at the expense of increased gate capacitance C_{ox}. The equivalent circuit delay ($\tau=C_{load}\times V_{DD}/I_{on}$) largely relies on the load capacitance $C_{load}=C_{ox}+C_{INT}$, where C_{INT} is the interconnect capacitance. C_{load} is dominated by C_{INT} at 45 nm node [2, 87]. Beyond 45 nm node, C_{INT} becomes more prevalent due to extremely dense layout and multi-layer interconnections. Therefore, the cost of increased C_{ox} may be trivial when increasing I_{on} in aFinFET where C_{INT} dominates. Figure 3.12 shows the results of simulated total CMOS invertor delay versus $L_{gbottom}$ for different C_{load}. When C_{load} is low, τ largely depends on C_{ox}. At the beginning of increasing $L_{gbottom}$, I_{on} increases faster than C_{ox}, thus τ gradually reduces. When $l_{gbottom}$ increases beyond a certain point, the loss of C_{ox} eventually becomes dominant over I_{on} so that τ degrades. The optimized minimal point shifts to the right side when C_{INT} is high. A larger

$L_{gbottom}$ is preferable so that the nominal current density is increased at the same footprint as long as τ does not degrade. There are different C_{INT} due to interconnection densities among different SoC circuits. Therefore, one can choose different $L_{gbottom}$ according to the local C_{INT} for highest SoC performance.

FinFETs with asymmetric gate configuration show improved SCE immunity and higher current density due to the additional gate extension overlap to SDE. They are promising for future ultimate-scaled high-performance SoC applications since the equivalent circuit delay could be minimized by optimized gate length design.

3.4 Scaling junctionless multigate field-effect transistors by step-doping

3.4.1 Problems with scaling of junctionless transistor

Junctionless multigate field-effect transistors (JL MuGFETs) have been proposed as a potentially better alternative to traditional inversion mode MOSFETs for their scalability and fabrication simplicity [50, 88]. Conventional JL MuGFET design involves a uniformly doped channel at a high level (N_D>10^{19} cm^{-3}) in order to deliver high current per unit width and minimize source/drain resistance (R_{SD}). However, the on-current improvement by increasing N_D reaches a limit because bulk conduction carrier mobility is degraded due to the increased impurity scattering. The device gets more difficult to turn off as N_D increases, because higher gate bias is required to deplete the entire channel. The ultrahigh channel doping concentration will also enhance coupling between drain and channel, which can induce significant drain-induced barrier lowering effects (DIBL) [52].

Shrinking the dimension of the fins would help to alleviate the problems. However, the design rules will be tightened. Both the width and thickness of fins have to be extremely scaled due to the reduced maximum depletion width W_{DW} as N_D increases [89]. For example, the fin

width needs be as small as 5 nm when N_D =8e19 cm^{-3} for better gate electrostatic control [76, 90, 91]. Such a small fin is difficult to fabricate [92] and would deteriorate the conduction-current by introducing large parasitic resistance. It may also lead to the swing of threshold voltage due to the potentially larger process variation for smaller scales [93]. The potential threshold swing issue is even worse for JL compared with the inversion-mode devices since JL devices are more sensitive to fin width variability [94]. Introducing non-uniform dopant distribution profiles in the channel is promising, as reported in planar JT devices using a Gaussian profile [95], which showed improvement of the off-current at the expense of the on-current. More systematic design and analysis is needed, especially for JT MuGFETs.

3.4.2 Illustration for device structure with step-doping and simulation methodology

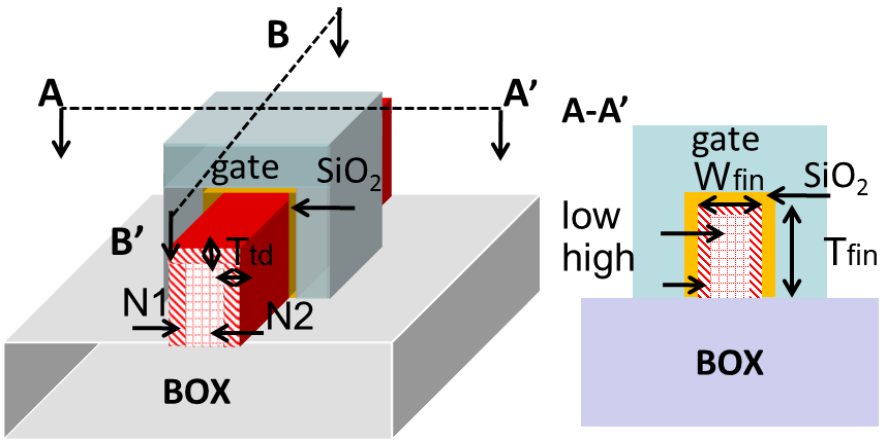

Figure 3.13: Schematic of the structure of a step doped JL MuGFET. The cross sectional view (along A-A') indicates two different doping regions inside the channel. T_{fin} and W_{fin} are the total thickness and width of the fin, respectively, and T_{td} is the transition depth. Reprinted with permission from [96].

Here, we present a design that adopts the step-doping scheme in JL MuGFETs, with higher doping concentration on both the top surface as well as the side walls of fins. Comparison with uniform-doping and retrograde-doping reveals that the high-low step-doping is superior in terms of better threshold voltage control, lower off-state leakage, higher on-current with the same total

number of dopants, and better SCE immunity. We then discuss the underlying mechanism and define a scaling factor metric to quantify its improved scalability. The implementation of step-doping could be useful for the scaling of JL MuGFETs.

Table 3.3 Summary of design parameters for the simulation of JL MuGFETs.

	Uniform	Retrograde-doping	Step-doping
channel doping	2.75e19 cm^{-3}	5e18/5e19 cm^{-3}	5e19/5e18 cm^{-3}
gate oxide	2 nm	2 nm	2 nm
gate work function	5.5 eV	5.5 eV	5.5 eV
transition depth (T_{td})	N/A	2 nm	2 nm
T_{fin}	20 nm	20 nm	20 nm
W_{fin}	9 nm	9 nm	9 nm
L_{gate}	10-170 nm	10-170 nm	10-170 nm
W_{DM}	7.2 nm	5.5 nm	15 nm

A JL MuGFET structure employing step-doping profile is schematically shown in Figure 3.13. The cross sectional view along the A-A' direction shows the two regions with different doping concentrations, high (N_1, near-surface or shell, shaded with hash lines) and low (N_2, subsurface or core, shaded with grids) as indicated. We will call this the step-doping if it is high to low doped from the surface; in contrast, retrograde-doping [97] refers to low to high. For ease of analysis, we assume the high and low doped regions have the same area A, i.e. $(T_{fin}-T_{td})\times(W_{fin}-T_{td})=T_{fin}\times W_{fin}/2$, where T_{fin} and W_{fin} are the total thickness and width of the fin, respectively, and T_{td} is the transition depth. For comparison, we use a control design with the same total number of dopants, but uniformly doped with doping concentration of $(N_1+N_2)/2$. 3D

numerical simulation of the device DC performance was carried out using Synopsis Sentaurus at 300 K. The parameters used for simulation of a Si channel are summarized in Table 3.3. Band-to-band tunneling [98] and mobility degradation due to impurity scattering were taken into account [83]. Quantum mechanical correction was not included to save simulation time and should not affect the analysis on different doping schemes. Note the proposed structure can be readily fabricated either by advanced implantation and annealing technology or by in situ doping during epitaxial growth.

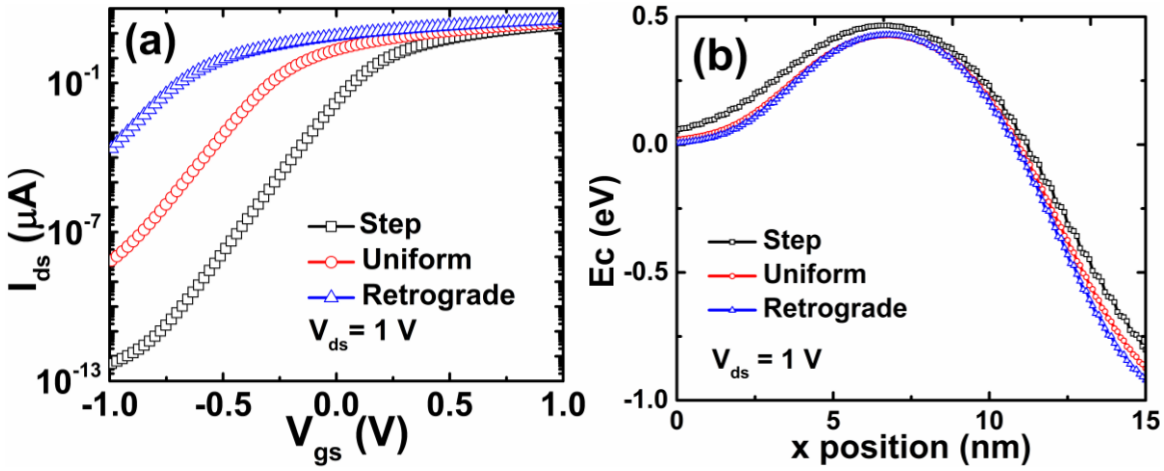

Figure 3.14: (a) Comparison of the transfer I_{ds}-V_{gs} curves for different doping schemes with L_g=15 nm and the detailed parameters adopted from Table 3.3. (b) Comparison of conduction band minimum E_c versus positions in the channel (along B-B' in Figure 3.13) at off-state (V_{gs}=V_{th}-1/3*V_{DD}), for different doping schemes with L_g=15 nm that source at zero and drain at 15 nm in x-axis. The detailed device parameters are adopted from Table 3.3. Reprinted with permission from [96].

3.4.3 Improved scaling performance by step-doping

Shown in Figure 3.14 (a) are the simulated transfer curves I_{ds}-V_{gs} for aforementioned devices (L_g = 15 nm) but with three different doping schemes. The relevant parameters used in the simulation are listed in Table 3.3. At V_{ds}=V_{DD}=1 V and V_{gs}= V_{th}+2/3V_{DD}, I_{on} is found to be 650, 480, 370 μA/μm for step doping, uniform doping and retrograde doping, respectively,

normalized by the fin height. This can be understood because I_{on} can be estimated from Equation (3.3),

$$I_{on} \approx \sum q\mu N \frac{T_{fin} W_{fin}}{L_g} V_{DD} \tag{3.3}$$

where μ is the mobility, N is the carrier concentration, L_g is the gate length, V_{DD} is the supply voltage, and $\sum$ accounts for the summation of the conducting carriers with different μ. Although the total amount of conducting charges in the channels is the same for three designs, the different dopant distribution changes the effective fin width. The gate bias converts the channel from depletion to flat band, then to accumulation mode faster because of a smaller effective fin width for the step-doping case which will be discussed further later. This leads to more carriers for the same amount of gate voltage overdrive. On the other hand, the mobility difference between the highly doped areas (2.75e19 and 5e19 cm^{-3}) is not significant [99], while the mobility in the lower doped area (5e18 cm^{-3}) is much higher which contributes to more current. Therefore a higher on-current in the step doping scheme is expected.

Furthermore, the sub-threshold behaviors show significant improvement. The subthreshold slope (SS) is 88 mV/dec for the step-doping scheme from 98 mV/dec for the uniform doping scheme, with the retrograde-doping scheme being the worst at 107 mV/dec. Correspondingly, the step-doping scheme has the lowest off-state current compared with the other two.

The source barrier, which is the maximum difference of the off-state conduction band minimum E_c in the source/channel region, determines the off-state current. Figure 3.14 (b) plots the off-state $E_c(x)$ at the interface of Si and SiO_2 along the middle of the fin channel (i.e. along B-B' in Figure 3.13). Both the height and the width of source barrier are slightly larger for the step-doping scheme compared with the other two. Although the difference is small, it may still block the tunneling at off-state more effectively, contributing to lower leakage current.

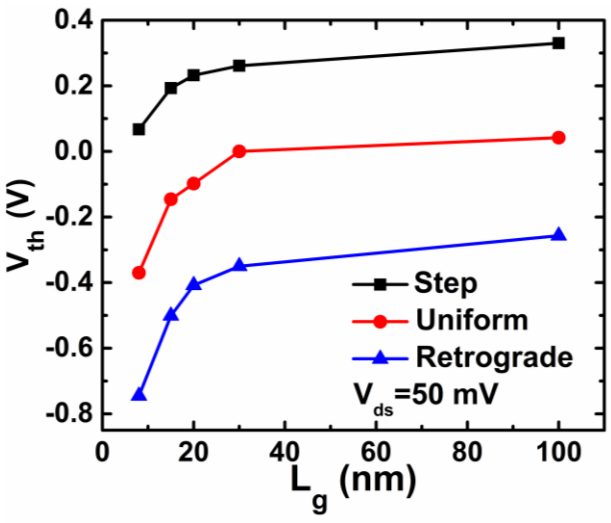

Figure 3.15: Comparison of threshold voltage (V_{th}) roll-off with the scaling of the gate length (L_g) between the three different doping schemes. Reprinted with permission from [96].

In addition, the threshold voltage (V_{th}) becomes more and more negative, from step, uniform, to retrograde-doping structures, as can be seen from Figure 3.14 (a). This could be attributed to the slope of the electric field (dE/dx) in the channel. The lower doped region is located away from the gate metal in the step-doping case, resulting in a reduced dE/dx and thus smaller surface potential φ_s [100] compared with the other two. Therefore, lower V_{th} value can be achieved according to Gauss' law (note the total charge are identical for all cases). This feature is useful for the scalability of junctionless transistors because it can help turn off transistors without the need for excessively high gate work function or scaled fin dimensions.

Figure 3.15 examines the SCE by plotting the V_{th} roll-off as a function of gate length (L_g). The steep decay of V_{th} for small L_g can be seen for all doping schemes, but the decay rate is the slowest one for the step-doping structure. The trends of Ss and DIBL as a function of L_g are also examined and shown in Figure 3.16. The step-doping structure shows the lowest Ss and DIBL across the entire L_g range. Clearly, the step-doping scheme leads to better SCE immunity.

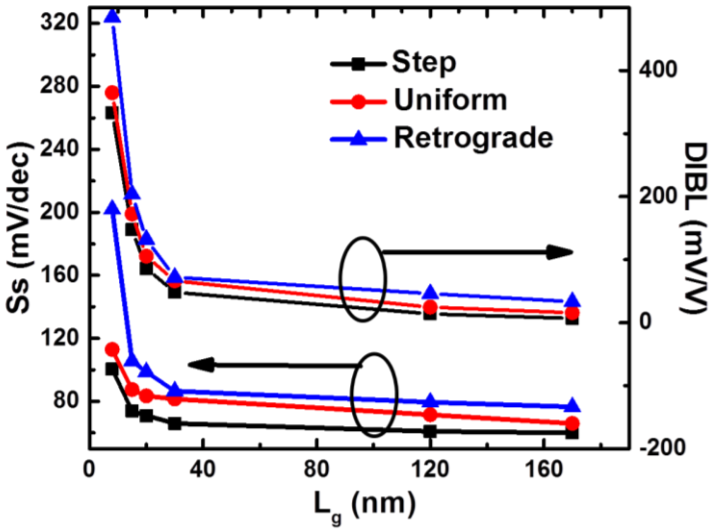

Figure 3.16: Subthreshold slope (Ss) and drain-induced barrier lowering (DIBL) comparison verse gate length using the same parameters in Table 3.3. Reprinted with permission from [96].

We believe the improved SCE immunity results from the smaller effective fin width "seen" by the gate electrode in step-doping and better gate electrostatic control. On one hand, the thicker W_{fin} is, the more current it can deliver per fin. The maximum W_{fin} is, however, limited by the maximum depletion width W_{DM} in order to ensure total depletion at off-state. On the other hand, lower channel doping concentration, i.e. larger W_{DM}, is desired in order to improve SS, DIBL and lower leakage for the same W_{fin} [52]. To evaluate the extent of depletion in the channel, we define an effective fin width scale factor $\alpha = W_{fin}/W_{DM}$. The smaller α, the easier the channel can be turned off by complete depletion, which means stronger gate electrostatic control and better SCE immunity.

We compare α for the three doping schemes: 1) $N_1 > N_2$; 2) $N_1 = N_2$; 3) $N_1 < N_2$, where N_1 and N_2 are the near-surface and subsurface doping concentrations, respectively, as indicated in Figure 3.13. We assume (1) and (3) have the same transition depth T_{td} for comparison and $T_{td}<W_{DM,\ N1}$. By integrating Poison's equation along the normal direction of oxide/Si interface

[89], we can calculate the effective W_{DM} for an arbitrary two-step-doping scheme:

$$W_{DM,non-uniform} = \sqrt{T_{td}^{\ 2} - \frac{N_1}{N_2} T_{td}^{\ 2} + \frac{2\varepsilon_{si}}{qN_2}\varphi_s} \tag{3.4}$$

where $\varphi_s = \frac{kT}{q}(\ln\frac{N_1}{n_i} + \ln\frac{N_2}{n_i})$.

We substituted $N = (N_1+N_2)/2$ in (2) to obtain the value of $W_{DM,\,2}$ for the uniform-doping scheme. We found that $W_{DM,\,1} > W_{DM,\,2} > W_{DM,\,3}$ holds true only when $N_1 > N_2$. The calculated values of W_{DM} are 15, 7.2, and 5.5 nm for step, uniform, and retrograde-doping schemes, respectively, using parameters listed in Table 3.3. Since the physical thicknesses W_{fin} are all identical for these three schemes, we can deduce that $\alpha 1 < \alpha 2 < \alpha 3$. Therefore, the step-doping scheme yields the smallest α thus the best off-state control. This also implies that if the same off-state performance is designed for all three schemes, wider fins for the step-doping scheme can be allowed. As a result, the step-doping scheme leads to better scalability by relaxing device fabrication requirements which also should reduce parasitic resistance.

We presented a step-doping scheme for the scaling of junctionless transistors. Lower $|V_{th}|$, higher I_{on}/I_{off} ratio and better SCE immunity can be achieved with the high-low step-doping in the channel. The standby power consumption is significantly reduced while achieving higher on-state current. The benefits of step-doping are attributed to the reduction of effective fin width. This design methodology relaxes the requirement for fin width scaling in JL MuGFETs, allowing continued scaling of JL transistors.

CHAPTER 4 – GATE-ALL-AROUND NANOWIRE MOSFET FOR HIGH-LINEARITY LOW POWER APPLICATION

4.1 Motivations for improving linearity in MOS transistors

For radio frequency (RF) circuits in modern communication systems, linearity is a crucial consideration for minimizing high order harmonics and inter-modulation, to guarantee less distortion between input and output signals. Transistor transconductance (g_m) contribution is a dominant factor compared to output conductance (g_d) for the non-linearity of RF amplifier and other circuit elements at high frequency, because the internal capacitances and substrate network reduce the optimal impedance for low distortion [101]. Unfortunately, g_m non-linearity is an inherent property of conventional transistors because of the mobility degradation at high field, as well as bias dependent source/drain (S/D) resistance [102] and channel length modulation effect (CLM) [103]. High linearity is even more difficult to achieve at low power supply and room temperature, which are required for portable RF applications.

There are many reports on improving the linearity at the circuit level by integrating and individually addressing discrete devices [104-106]. However, such schemes require more resources and larger footprint. Few efforts have been put into improving linearity at the device level. Kaya and Ma reported the approach of double-gate Si metal-oxide-semiconductor field effective transistors (MOSFETs) [107]. Recently, Razavieh et al. demonstrated that nanowire (NW) gate-all-around (GAA) MOSFET has the potential to achieve good linearity when operating at the quantum capacitance limit [108]. These two approaches showed promising results. However, the improvements demonstrated thus far are limited in their range of operating voltage or temperature, as well as by technical difficulties in realizing the full potential of these mechanisms. It is of great interest to find other ways to achieve high linearity using NW GAA

MOSFETs, not only for their excellent digital performance [109], but also for the potential in superior analog/RF scalability [110].

Here, we first provide physical understanding of linearity in NW GAA MOSFETs. Then we present a device architecture that employs vertically-stacked III-V NWs with tunable size and doping levels as the high mobility channel. Specifically, we use GaAs here to take advantage of its high electron mobility property. Through modeling and 3D numerical simulation, we demonstrate that by properly adjusting the doping and dimension of the stacked NWs individually, significant improvement in linearity, characterized by high IP3 at maximum transconductance point $g_{m,\,max}$, can be achieved, even for low power supply operation at room temperature. Finally, we discuss other metrics for high frequency RF/Analog performance of this device architecture.

4.2 Vertically-stacked individually-tunable nanowire field effect transistors for low power operation with ultrahigh radio frequency linearity

4.2.1 Device structure illustration and simulation methodology

Figure 4.1 schematically depicts the proposed vertically stacked NW GAA MOSFET architecture, but we will analyze the g_m linearity of a single NW channel device. We adopt a charge-based long channel model for g_m analysis [111], which is valid for NW GAA MOSFETs operating at low electric field. As gate bias V_{gs} increases above threshold voltage (V_{th}) and below V_{gs}-V_{th}<V_{ds} (drain bias), the transconductance of the device can be expressed by:

$$g_m = \frac{2\pi\mu_{eff} RC_{ox}(V_{gs} - V_{th})}{L_{eff}} \tag{4.1}$$

and when $V_{ds} = V_{gs} - V_{th}$, g_m reaches its peak value:

$$g_{m,\max} = \frac{2\pi\mu_{eff} RC_{ox} V_{ds}}{L_{eff}} \tag{4.2}$$

where μ_{eff} is the effective mobility, R is the NW radius, L_{eff} is the effective gate length which varies with CLM, C_{ox} is the gate oxide capacitance per unit area, and V_{ds} is specified as the drain-to-source bias which excludes the voltage drop across the S/D resistance. When V_{gs}-V_{th} exceeds V_{ds}, both the μ_{eff} and V_{ds} are reduced due to high field related mobility degradation and the impact of S/D resistance, respectively. Therefore g_m, which has the same format as (2), is significantly reduced at V_{gs} beyond $g_{m,max}$.

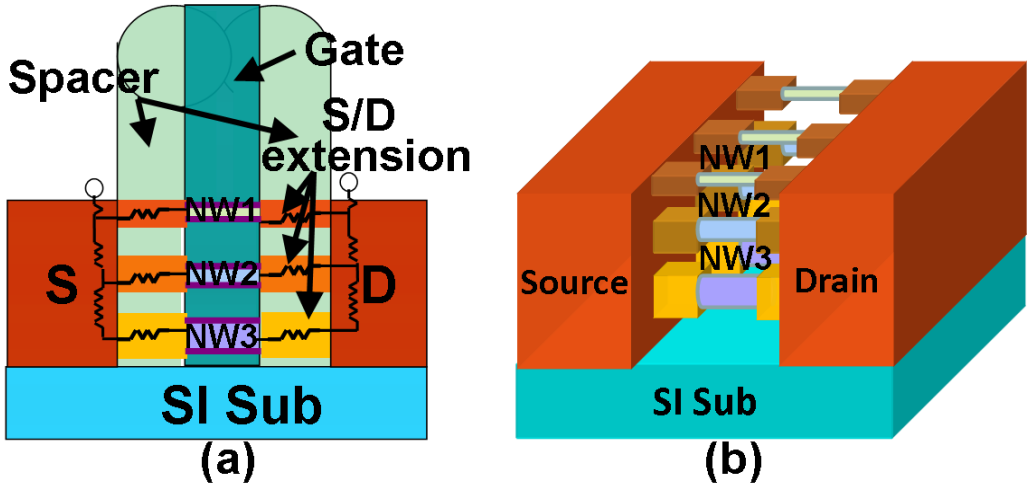

Figure 4.1: Schematic illustrations of vertically stacked NW GAA MOSFET design on a semi-insulating substrate (SI Sub): (a) Cross-sectional view with gate stack, S/D, and SiN spacer; (b) three-dimensional view of the stacked NWs without the gate stack. Reprinted after permission from [112].

3D numerical simulation is performed by the device simulation package Synopsys TCAD SENTAURUS, employing the hydrodynamic model to incorporate the non-stationary transport effects [113]. A density-gradient equation is adopted to account for the first order quantum mechanical correction [114]. We assume the channel and S/D region material in this design is GaAs. As an example, we assume that the NW is uniformly p-doped at low level (5e14 cm^{-3}) with a relatively large diameter (D_{nw} = 30 nm). The doping level in the S/D regions is high (n^+,

1e19 cm^{-3}) and the S/D extension is lower (n, 2e18 cm^{-3}). The intrinsic doping-related S/D resistance is assumed to be 2 kΩ. The NW is surrounded by 10 nm Al_2O_3 as the high–k gate dielectric and a gate metal with mid-gap work function of 4.5 eV (e.g. WN). A moderate value of interface charge density 5e11 $eV^{-1}•cm^{-2}$ is assumed at the GaAs/Al_2O_3 interface based on published experimental data [115]. All parameters and conditions used for the simulations are for room temperature operation.

4.2.2 Device design for improving linearity by stacking nanowire channels

Figure 4.2 (a) and (b) show the simulated g_m vs. V_{gs} curves as a function of nominal gate length L_g and drain bias V_{ds}, respectively. As L_g scales down, the g_m linearity becomes worse (Figure 4.2 (a)). This can be attributed to larger contribution of S/D resistance as well as more severe mobility degradation for devices of smaller L_g. In Figure 4.2 (b), it is shown that the linearity improves for higher V_{ds}. This can be attributed to the counteraction between L_{eff}, μ_{eff}, and V_{gs}-V_{th}. An incremental g_m is expected when V_{gs}-V_{th}<V_{ds} because g_m should increase with V_{gs} as seen in (4.1). However, L_{eff} increases more significantly due to CLM and μ_{eff} drops as V_{ds} increases. As a result, higher V_{ds} corresponds to a flatter g_m vs. V_{gs} curve. However, as can be seen from Figure 4.2, it is much more challenging for a NW GAA MOSFET with a short-channel to achieve good linearity at low V_{ds}.

Based on the analysis of single NW channel in Figure 4.2, if several NW channels with different g_m vs. V_{gs} profiles, either descending or ascending within a certain range of V_{gs} bias, can be superimposed, it is possible to obtain a near constant total g_m of the NW group, thus overall better linearity. The profile of the g_m vs. V_{gs} curve can be tuned by changing the NW diameter and doping concentration. Hence, we propose a vertically stacked NW GAA MOSFET structure similar to that of [116] except that the stacked NW 1, 2, and 3 possess different

diameters and doping concentrations, as illustrated in Figure 4.1(a) and (b). The structure can be realized experimentally by growing the epitaxially stacked lattice-matched (e.g. GaAs/AlGaAs) or strained (e.g. InGaAs/AlGaAs) layers with different thickness and doping concentrations on top of a semi-insulating substrate, either by metalorganic vapor phase deposition (MOCVD) or molecular beam epitaxy (MBE), followed by selective etching of the sacrificial (e.g. AlGaAs) layers to form GAA structure as in reference [117].

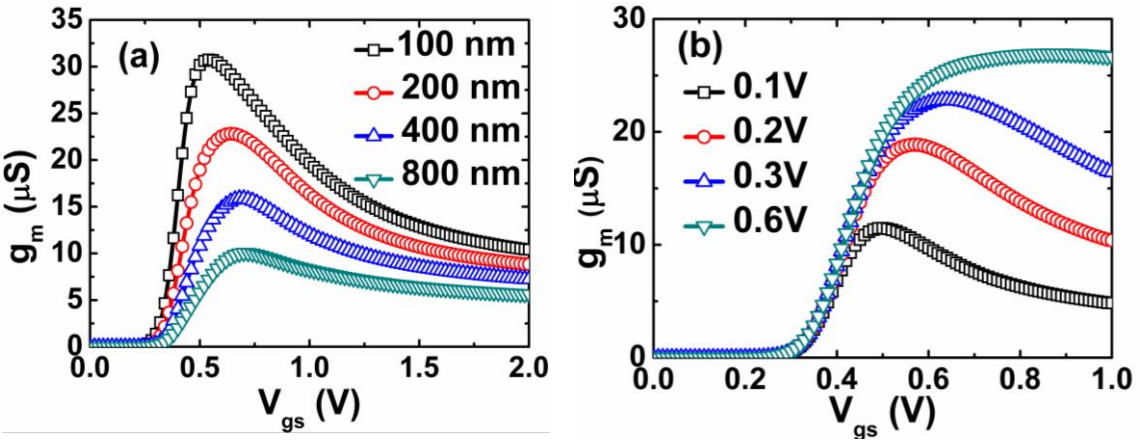

Figure 4.2: Transconductance g_m as a function of gate bias V_{gs} for a single NW GAA MOSFET, NW radius = 14 nm with p type doping concentration 5e15 cm^{-3}. (a) Different L_g at V_{ds}=0.3 V. (b) Different V_{ds} for L_g =200 nm. Reprinted after permission from [112].

From eq. (4.1), the rising slope of g_m vs. V_{gs} at saturation region is $2\pi\mu RC_{ox}/L_{eff}$. V_{th} determines the position of $g_{m,max}$, and can be readily tuned by the NW doping concentration N (cm^{-3}), while it only decreases slightly with the increase of NW radius R.

We choose NW3 to be the NW with a large radius and low p-type doping concentration. Thus the NW3 channel has the lowest V_{th} and largest $g_{m,max}$ and it dominates the device performance when V_{gs} is low. Then on top of the NW3 we stack NW1 and NW2 with smaller radii and heavier p-type doping concentration N_1 and N_2. Therefore, these two NW channels should have relatively higher V_{th} and smaller $g_{m,max}$. The ideal situation is that the descending

profile of $g_{m,R3}$ exactly compensates the rising slope of $g_{m,R1}$ and $g_{m,R2}$ throughout a wide range of V_{gs}.

Through numerical iterations, a 3-stack NW structure with N_3 (p-type, 5e15) < N_2 (p-type, 3.2e18) < N_1 (p-type, 5.8e18) and R_3 (20 nm) > R_2 (15 nm) > R_1 (8 nm) has been chosen to illustrate the methodology of the design. This representative set of parameters can keep g_m of NW1 and NW2 rise at the right V_{gs} range to compensate the descending g_m of NW_3.

Table 4.1 Summary of design parameters and simulated electrical properties of individual and stacked NW devices at V_{ds}=0.3V.

	Radius (nm)	Doping conc. (cm^{-3})	V_{th} (V)	$g_{m,max}$ (μS)	V_{gs} @ $g_{m,max}$ (V)	IP3 @ $g_{m,max}$ (dBm)
NW1	7	p-type, 5e18	0.352	7.17	0.8	-7.50
NW2	15	p-type, 3e18	0.345	13.57	0.8	-9.59
NW3	20	p-type, 5e15	0.077	45.84	0.43	-8.86
Total	stack		0.098	47.96	0.58	-1.50

However, the rising slope of the g_m - V_{gs} curve is tied to the magnitude of $g_{m,max}$ as shown in eq. (4.2). The magnitude of $g_{m,max}$ for smaller NWs needs to be further increased in order to effectively increase the overall g_m flatness. The local potential V_{ds} near the top surface is larger because of less voltage drop across S/D resistance, so NW1, NW2 and NW3 have to be placed from top to bottom in sequence. A spacing of 40 nm between the adjacent NWs is used for the simulation. We further adopt different S/D extension doping concentration (N_{ext1} (n-type, 1e18)

> N_{ext2} (n-type, 8e17) > N_{ext3} (n-type, 5e17)) in the stack. These two design considerations lead to a larger effective V_{ds} for NW channels of smaller diameters thus result in larger $g_{m,\ maxR1}$ and $g_{m,\ max\ R2}$. Table 4.1 summarizes one set of design parameters for the vertically stacked GaAs NW FET. Note that the design parameters are a function of material related data, i.e. high-field dependent mobility degradation and S/D parasitic resistance. Other device parameters are the same as mentioned previously. These carefully designed parameters give rise to significantly improved linearity; i.e., g_m is nearly independent of V_{gs} over the range of 0.4 – 0.8 V, as shown in Figure 4.3.

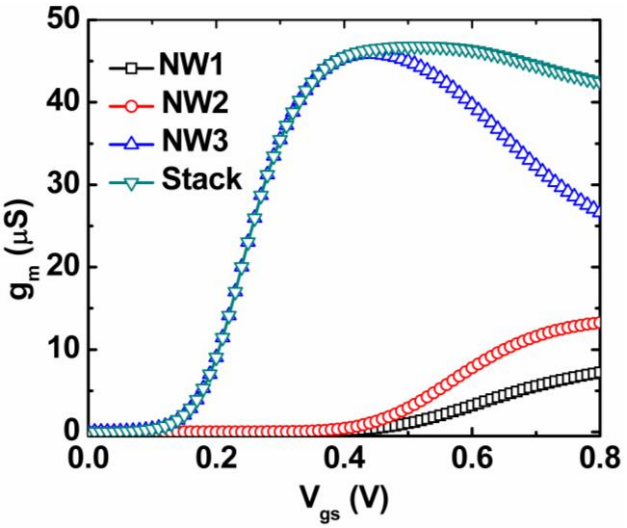

Figure 4.3: Transconductance g_m verse gate bias V_{gs} plot for NW1, NW2, NW3 and the vertically stacked NWs with L_g=200 nm. Reprinted after permission from [112].

The significant improvement in linearity is also supported by the figure of merit for linearity, the third order intercept point (IP3), which is defined as follows [104]:

$$IP3 = \frac{2g_{m1}}{3g_{m3}R_s} = \frac{4\dfrac{\partial I_D}{\partial V_{gs}}}{R_s\dfrac{\partial^3 I_D}{\partial V_{gs}^{\ 3}}} \tag{4.3}$$

where R_s is the source resistance, g_{m1} is the transconductance and g_{m3} is its 2nd derivative. Figure 4.4 shows the calculated IP3 of the optimized vertically-stacked NW GAA MOSFETs compared

with the individual NW cases. To reduce differentiation noise we used cubic-spline interpolation and performed polynomial regression at 7th–9th degree. This approach generally produces smoother IP3 curves as a function of gate bias. It can be seen that IP3 is improved from -8.86 dBm (the best single wire, NW3) to -1.5 dBm (stack) at the corresponding $g_{m,max}$, which is an improvement of ~ 7.36 dBm. This result represents significant advancement compared with previous efforts for device level linearity improvements both in magnitude and operating voltage range [107, 108].

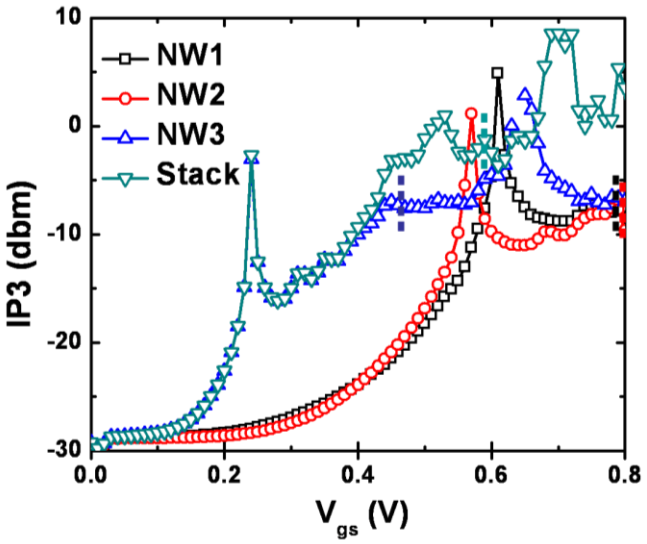

Figure 4.4: Third-order intercept point IP3 (dBm) versus gate bias V_{gs} plot for NW1, NW2, NW3 and stacked NW design at V_{ds}=0.3V; the dashed vertical lines indicate the $g_{m.max}$ position. Reprinted after permission from [112].

It is worth noting that the improvement in linearity is bias dependent, as is the case for the single stack device. One set of specific device design parameters (diameter and doping) corresponds to an optimized linearity for one specific bias range. Since the worst linearity problem is at low bias condition, our example for linearity improvement was optimized for low power application at V_{ds} of 0.3 V. Furthermore, as can be seen from the transfer curves shown in Figure 4.5 for different gate lengths (100 – 600 nm), the channel length dependence of g_m

linearity for stacked design is much weaker, compared to the single NW case (Figure 4.2(a)). This indicates that the superposition effect of multistacked NWs is valid no matter how large S/D resistance is relative to channel resistance.

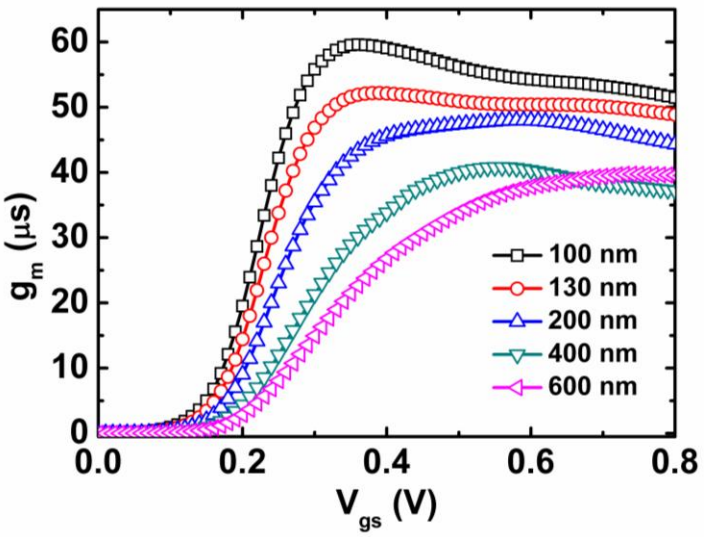

Figure 4.5: Transconductance g_m as a function of gate bias V_{gs} for the stacked NW design with specified gate lengths at V_{ds} = 0.3 V. Reprinted after permission from [112].

For digital circuits, this stacked NW design is expected to have excellent digital performance because of the GAA structure and much higher driving current density due to the stacked integration [116]. For analog circuits, there are two important metrics: one is the intrinsic gain g_m/g_d and the other is power efficiency g_m/I_d, in which g_d is the conductance of the transistor and I_d is the drain current. Figure 4.6a and 4.6b show the comparison of g_d and g_m/g_d, and I_d and g_m/I_d, respectively, as a function of V_{gs} for the stacked design and individual nanowire (NW3). We can see that both g_m/g_d and g_m/I_d of NW3 and stack design are at the same highest value when V_{gs} is low. However, as V_{gs} increases, g_m/g_d and g_m/I_d of the stacked case become larger than the NW3 case, even though g_d and I_d also increase. Thus the vertically stacked design improves driving current without a penalty in intrinsic gain and power efficiency, which is beneficial for analog circuits.

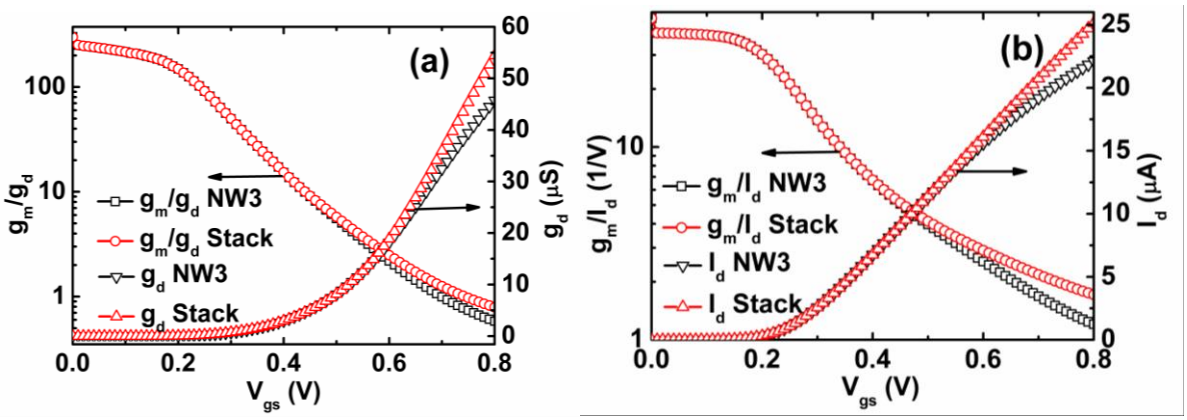

Figure 4.6: (a) Self-gain g_m/g_d, and (b) power efficiency g_m/I_d as a function of V_{gs} at V_{ds}=0.3 V, as well as the corresponding (a) conductance g_d and (b) drive current I_d plotted on the respective right vertical axis's. Reprinted after permission from [112].

In addition, we have compared the high frequency RF performance of the NW stack vs. individual NWs, using a two-port network configuration with parasitic capacitances and intrinsic resistances included in the simulation. The cut-off frequency f_T was extracted by unity current gain ($|Y_{21}/Y_{11}|$ = 1 in Y-parameter matrix). The maximum oscillation frequency f_{max} was extracted by the unity Mason's unilateral gain [118]. The simulation results reveal that the high frequency metrics are dominated by the largest diameter NW3 as expected because it has the largest g_m, and the stack only shows slight improvement. f_T and f_{max} start to increase sharply after V_{gs} exceeds 0.2 V. f_T of 11 GHZ and f_{max} of 140 GHZ are achieved at a low supply voltage V_{dd} of 0.3 V. All of these results indicate that the vertically-stacked NW GAA MOSFET design yields a good compromise between intrinsic gain g_m/g_d, power efficiency g_m/I_d and bandwidth f_T for low power consumption.

In summary, we have analyzed the linearity issues in NW GAA MOSFETs and presented a design of vertically stacked NW GAA MOSFETs that can achieve excellent linearity at low bias. For a representative design, IP3 at $g_{m,max}$ reaches as high as -1.5 dBm at room temperature, with excellent high frequency RF/analog performance. Our design offers a good solution for ultrahigh RF linearity performance and ultra-low power consumption portable system-on-chip

applications. The design is experimentally feasible. The methodology can be universally applied to all multi-stack NW GAA MOSFETs with different materials choice.

4.3 Improving linearity by junctionless gate-all-around nanowire transistors

For short-channel devices, g_m linearity is especially degraded because of the mobility degradation and the severe source/drain (S/D) resistance [102, 112]. Junctionless (JL) FETs [50], which exploit bulk conduction, can minimize mobility degradation caused by surface roughness-related scattering or high-k surface phonon scattering [119]. The lower electric field in the channels [120] also leads to less field mobility degradation, when compared to traditional junction-based transistors. Ultra-thin and narrow nanowires (NWs) surrounded by a multiple gates, such as using the gate-all-around (GAA) structure [117], is a critical design guideline for JL nanowire MOSFETs (NWFETs) [93]. However, scaled NWs may impose large S/D resistance, which can be reduced by taking advantage of the high electron mobility and versatile bandgap and doping engineering of III-V materials [121]. Thus it is quite interesting to explore the potential for improving the linearity using III-V JL nanowire MOSFETs (NWFETs).

III-V JL GAA NWFETs are fabricated with an implantation-free technology through S/D regrowth by metalorganic chemical vapor deposition (MOCVD). The fabricated short-channel devices (L_g=80 nm) show excellent g_m linearity at low bias conditions (V_{dd}= 300 mV), characterized by the high third intercept point (2.6 dBm).

4.3.1 Experimental process flow for junctionless gate-all-around nanowire transistor

A new process flow for fabrication of nanowire gate-all-around MOSFETs has been designed and executed. The schematic illustration is shown in Figure 4.7. Semi-insulating (SI) GaAs substrate with (100) orientated surface is used as the starting material. Two stacks of lattice matched undoped AlGaAs (100 nm) and GaAs (100 nm) with n-type Si doped 2e17cm-3 are

grown in sequence in a horizontal-flow Aixtron metal organic chemical vapor deposition (MOCVD) reactor under atmospheric pressure. This thin GaAs layer serves as the future channel region and the AlGaAs serves as the sacrificial layer. Figure 4.8 shows the cross section of as-grown stacked AlGaAs/GaAs.

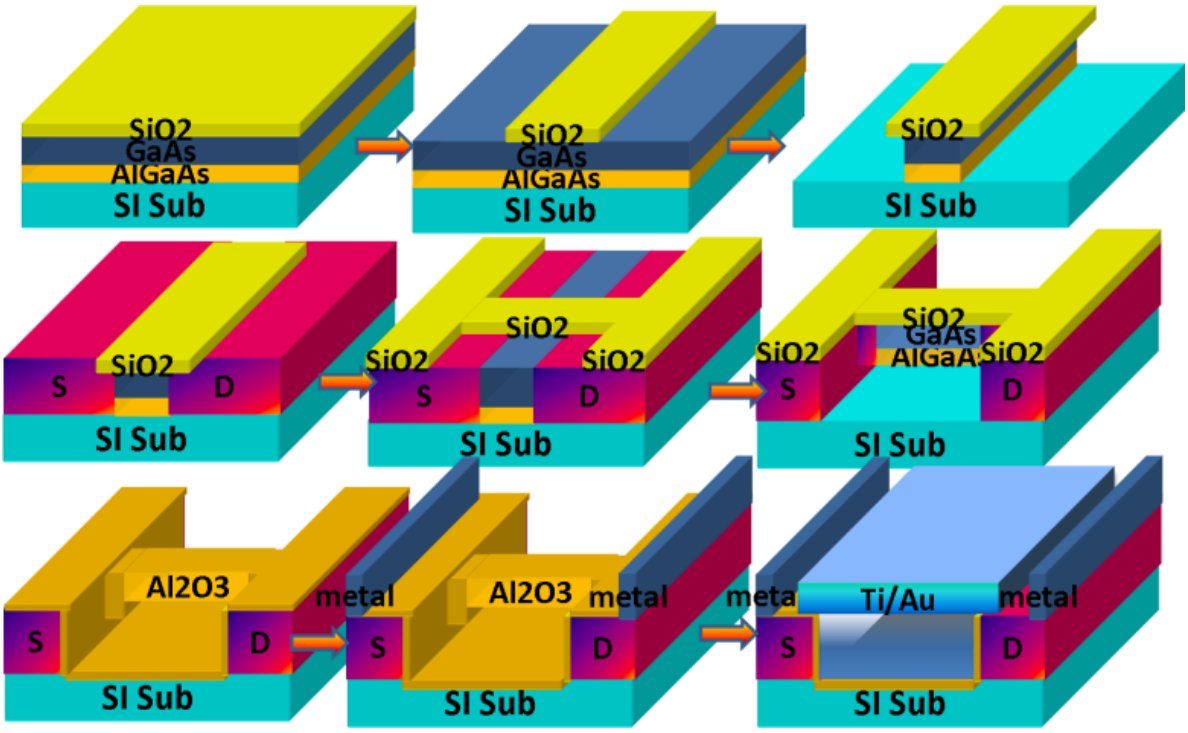

Figure 4.7: Schematic process flow for regrowth S/D nanowire gate-all-around MOSFETs. Reprint after reference [88].

In order to minimize S/D resistance and shrink gate length [2], as well as avoid traditional implantation-induced damage and high temperature annealing, we adopt S/D regrowth technology [122]. 120 nm SiO_2 is deposited by LPCVD as the hard-mask layer for regrowth. The first e-beam lithography is performed to open the regrowth area on eLine Raith system using Polymethyl methacrylate (PMMA) positive e-beam resist. After development, the hard mask is etched in a plasma Freon reactive ion etching (RIE) system. Then the PMMA is removed by PG remover. After standard cleaning, a wet etching in H_2SO_4: H_2O_2: ionized water=1:8:80 for 1 min is performed to etch away S/D area, aiming to prevent dry etch-induced damage [123]. The inset

in Figure 4.8 (left) shows the cross-sectional view of isotropic wet etching. The wafer is immediately transferred to a MOCVD chamber to regrow the 200 nm S/D region with 5e18 cm^{-3} Si doping concentration. Various gate lengths as short as 200 nm are determined by the separation between S/D at this step. Figure 4.8 (right) shows the cross sectional view of S/D and channel area after regrowth.

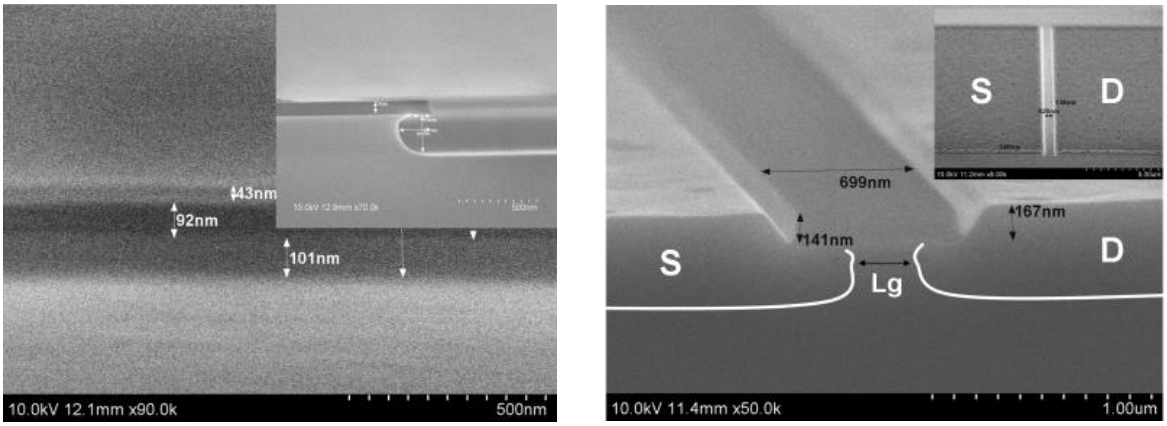

Figure 4.8: (left) Stacked AlGaAs/GaAs material grown by MOCVD. The inset shows wet etching performed prior to regrow. (right) Cross sectional view of regrowth S/D area using SiO_2 as hard mask; the inset shows the top view.

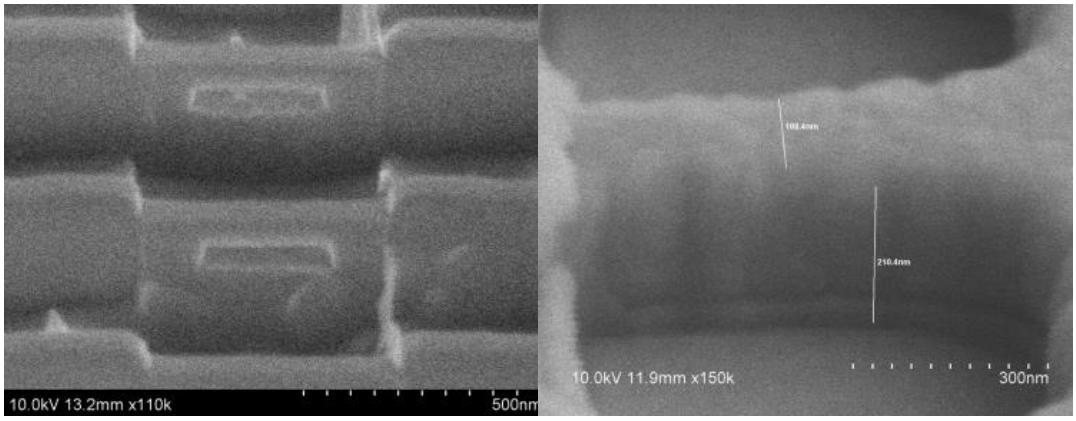

Figure 4.9: Suspended nanowires between S/D (left) and nanowires covered by gate stack after two step sputtering metals (right).

The SiO_2 hard mask for regrown GaAs is removed in BOE. Afterwards another SiO2 layer with 100 nm thickness is deposited by LPCVD. The second e-beam lithography is performed to pattern the fins between the S/D. The SiO_2 hard mask is etched by RIE etching. The

GaAs/AlGaAs fins with 200 nm height are etched by inductively coupled plasma (ICP) RIE after the removal of PMMA. A wet etching in 25% HF is performed to selectively remove the exposed AlGaAs sacrificed layer to suspend GaAs nanowires. An overetch in BOE is allowable because the S/D region is protected by the regrown GaAs, which facilitates the process control. SEM pictures are taken by a Hitachi 4800 microscope. Figure 4.9 (left) shows the suspended nanowires after BOE etching.

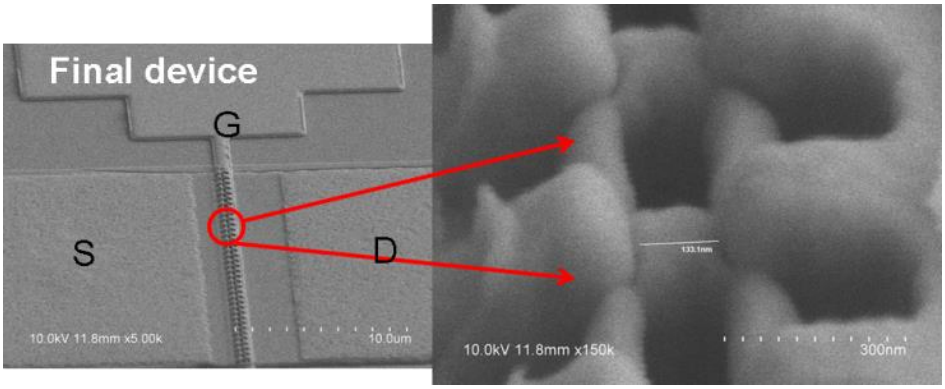

Figure 4.10: The finalized device SEM image and zoomed in picture showing the fin channels covered by gate stack.

The sample was put in 10% $(NH_4)_2S$ solution for 10 min to passivate the surface before loading into atomic layer deposition (ALD) chamber to deposit 10 nm Al2O3 as the gate dielectric. The S/D contact area is exposed in another e-beam lithography. Ge/Au/Ni/Au (20 nm/50 nm/30 nm/50 nm) was deposited by e-beam evaporation in sequence. A rapid temperature annealing (RTA) at 350 C for 90s is performed for the source/drain ohmic contact formation. Finally the Ti/Au (10 nm/100 nm) stack was patterned by e-beam lithography and lift-off as the gate stack. Figure 4.9 (right) shows the SEM picture of the suspended nanowires covered by gate stacked (Al_2O_3/Ti/Au). The device ended with acetone/methanol/IPA standard cleaning process. Figure 4.10 shows the completed device and zoomed-in view of the raised regrowth S/D and short GAA channels.

4.3.2 Device characterization and discussion

The electrical characterization was carried out using a Keithley 4200 semiconductor characterization system. Figure 4.11 shows the transfer characteristic at V_{ds}=0.1 V, 0.5V and 0.1 V and the output curve at different Vgs for the fabricated device with the gate length L_g=200 nm and nanowire width D_{NW}= 200 nm, respectively. From this curve, we could extract Ss and DIBL are 210 mV/dec and 332 mV/V respectively. The good SCE performance is due to the better gate-all-around electrostatic integrity. The threshold voltage Vth =-0.147 V, which is obtained by the linear extrapolation of Id-Vg curve at Vds =50 nm. Figure 4.11 clearly shows that there are two different subthreshold slopes (Ss). This is due to the corner effects [124], which indicate the electric-field in the corner is higher than the central bulk area. The non-uniform electric field distribution leads to two sub-channels, i.e. surface and bulk channel, and turns on at different bias, which leads to two different Ss.

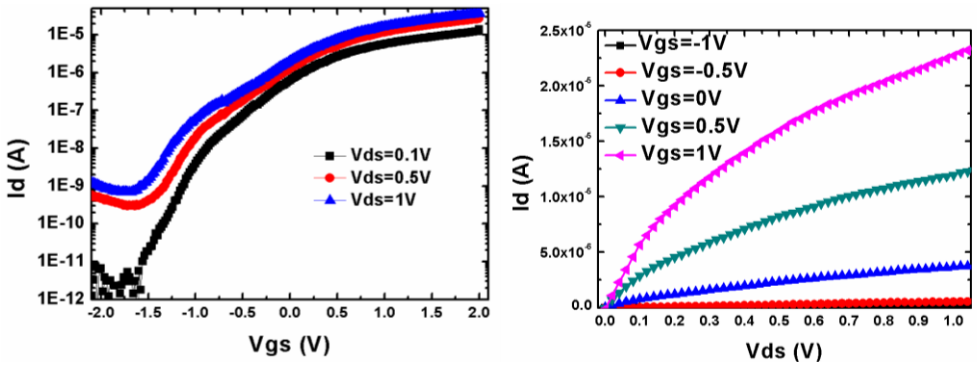

Figure 4.11: (left) Transfer characteristic of the fabricated GaAs NW GAA MOSFET with gate length L_g=200nm, nanowire diameter D_{nw}=200 nm. (right) Output characteristic of the same device. Reprinted with permission from [88].

Figure 4.12 shows the extracted transconductance vs. different V_{gs}. The transconductance is almost constant when the device is turned on. Thus high linearity is achieved for large bias range (>1.0V). Two factors may help to explain the phenomenon. The transistor is junctionless, which is named “gated-resistor”. The conduction carrier is majority rather than minority carriers. The

electric field is smaller than the traditional NPN junction MOSFETs [120], which leads to more slight mobility degradation. The second reason is that we use extremely small nanowires as the channel. The absolute channel resistance is much larger than the regrown highly doped S/D region. Therefore, the effects of S/D resistance might be small enough relative to channel resistance such that the linearity improves. We can obtain flat g_m curves even at biases as low as 0.1 V as shown in Figure 4.12. This is an improvement over previously published data.

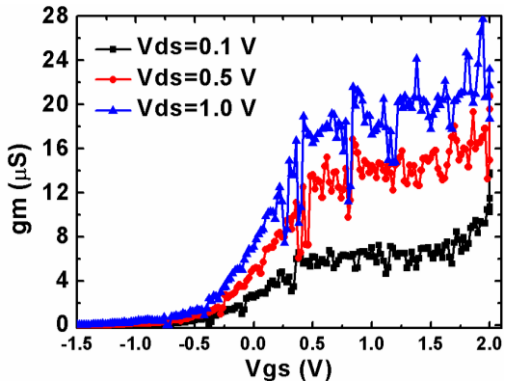

Figure 4.12: Extracted transconductance vs. different V_{gs} for V_{ds}= 0.1V, 0.5 V and 1.0 V respectively.

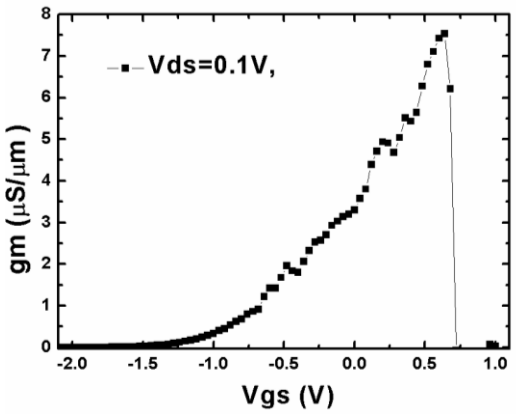

Figure 4.13: g_m vs. V_{gs} for the control planar GaAs MOSFET, L_g= 250 nm. T_{Al2O3}=9 nm.

The control planar bulk GaAs MOSFETs are fabricated in parallel. Figure 4.13 shows the g_m vs. V_{gs} of the fabricated device with L_g=250 nm. Significantly larger gate leakage is observed for

high V_{gd}. The linearity is not as good as NW GAA MOSFETs because the relative weight of S/D resistance is larger and the gate leakage is larger, which contributes to non-linearity, in this case.

There are two important metrics to evaluate the device RF performance. One is intrinsic gain g_m/g_d, and the other is power efficiency g_m/I_d. These values vs. different V_{gs} are plotted in Figure 4.14 respectively. The intrinsic gain drops continuously as V_{gs} increases and reaches almost unity when $V_{gs}=V_{th}$. The power efficiency also decreases with the increase of V_{gs} and reaches 5 at V_{th}. It can be easily understood from the g_m curve in Figure 4.13 that the obtained linear g_m has relatively small value which sacrifices other RF metrics.

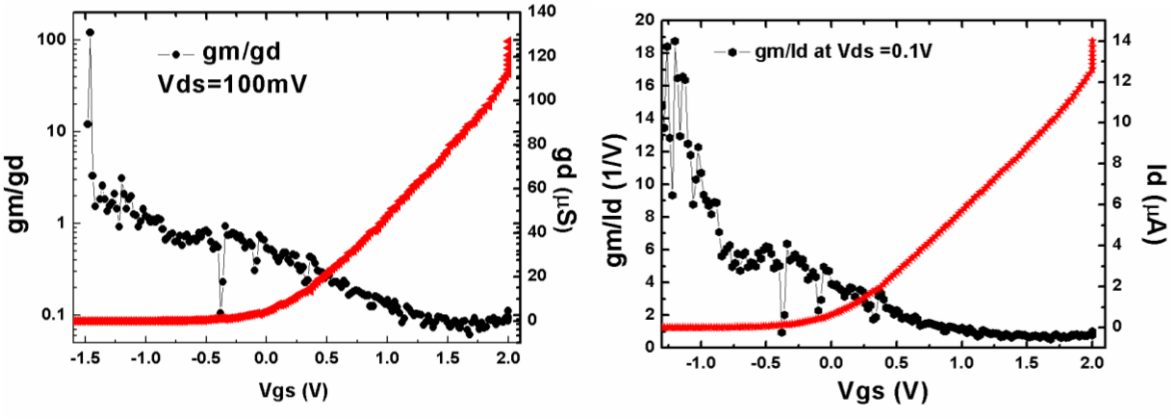

Figure 4.14: (left) Intrinsic gain g_m/g_d vs. different V_{gs} at V_{DS} =100 mV. (right) Power efficiency vs different V_{gs} at V_{DS}= 100 mV.

CHAPTER 5 – FUTURE WORK

5.1 Developing improved high-aspect-ratio FinFETs

The ultimate on-state current, I_{on}, is limited by the thermal consideration at a fixed value of off-state leakage, I_{off}, and overdrive voltage V_{DD}, and the gate delay (CV_{DD}/I_{on}) can then be reduced only at the expense of increased V_{DD} resulting in increased power consumption ($CV_{DD}^2/2$). Tunnel transistors [125] offer subthreshold characteristics steeper than the thermodynamic limit 60mV/decade at room temperature, but achieving high I_{on} at low I_{off} and low V_{DD} is challenging. Subthreshold logic [126] operates at low V_{DD}, but is slow because of low I_{on}. Obviously, the volume of active devices is only a very small portion (several hundreds of nm) of the whole wafer, while the majority of the wafer (160-300 μm in thickness) is simply used as mechanical support. If we can increase the current conduction in the depth direction, the on-current for a given surface area can be boosted readily. In addition, the source/drain region is much deeper than that of planar FETs or low AR FinFETs, which guarantees improved S/D resistance.

The key to fabricate high AR FinFETs is the formation of a high AR fin channel. Conventional etching methods, dry etch or wet etch, cannot readily produce high AR fins with ideal vertical sidewall due to the non-ideal anisotropic etching profile. The tapered sidewall is due to the difficulty of making the reaction gas flow contact the surface and the fact that the reaction product evaporates when etching proceeds deeper. Worse is that plasma-based reactive ion dry etching causes irreversible damage to the sidewalls when fabricating FinFETs, particularly for III-V channels [55, 56], where such damage is difficult to repair compared to Si-based channels in CMOS technology. Sidewall damage induces a disordered interface between the high-k gate dielectric and semiconductor channel, which impedes the carrier surface mobility

and degrades device sub-threshold characteristics [57]. Moreover, sophisticated techniques [58] are required to improve the selectivity over different materials by dry etching. For the above reasons, dry etching hinders progress toward aggressively scaled FinFETs. On the other hand, pure wet chemical etching usually does not degrade the crystallographic integrity and has high selectivity, but it is only suitable for large features (>1 μm).

We propose to use a novel etching method - metal-assisted chemical etching (MacEtch) [59] - for fabricating nanoscale structures. Li [127] developed MacEtch conditions for various materials, like GaAs [128], Si [129] and InP [60], to produce nanostructures with arbitrary patterns such as pillars, holes, fins, letters, characters, and flowers. MacEtch is a wet but directional semiconductor (e.g. Si, SiGe, GaAs, InP, GaN, etc.) etching technique which uses a chemically stable thin layer of noble metal acting as a catalyst to guide the etch process in a solution that usually consists of an oxidant (to generate holes) and an acid (to remove the oxidized species). The oxidant in the solution oxidizes the semiconductor surface and the acids remove the oxides to precede etching. Under controlled etch conditions, only the semiconductor material directly underneath the catalyst metal is removed. This results in the catalyst metal being “engraved” or “buried” into the semiconductor, leaving behind a 3D semiconductor pattern that is complementary to the metal pattern, as illustrated in Figure 5.1 (a-b), and the corresponding MacEtch-produced structures are shown in Figure 5.1 (c). The sidewall roughness of MacEtch-produced semiconductor structures is largely determined by the catalyst metal pattern edge roughness. The sidewall verticality or anisotropy is affected by competing etching processes when mass transport of the oxidized species is limited. MacEtch is size specific, under open circuits, at room temperature, without high energy ions and related damage, and with practically no infrastructure needed. The AR that MacEtch can produce is essentially unlimited

as long as the metal-semiconductor interface can be kept intimate as etching proceeds. Extremely tall pillars, fins, and deep holes can be fabricated by MacEtch [127] with AR far exceeding 100:1 [129], as shown in Figure 5.1 (d). The demonstrated results are highly scalable in dimension and with high throughout.

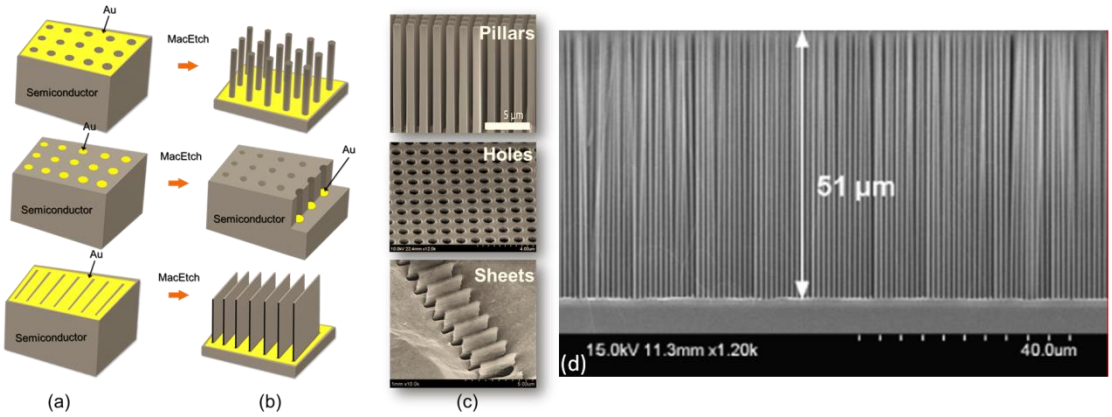

Figure 5.1: Nano-structure formation by MacEtch, (a)-(c) Schematic and corresponding SEM images of nanopillars, holes and fins fabricated by MacEtch. (d) Silicon pillars with AR higher than 100:1. Reprinted with permission from [129].

On the other hand, the metal catalyst can function as a catalyst mask, where etching takes place inversely compared to conventional forward MacEtch. Thus, the i-MacEtch mechanism causes the semiconductor regions not interfaced with the catalyst layer (i.e., between the metal covered areas) to be preferentially etched. In addition, the areas directly underneath the catalytic metal mask can be etched (laterally) simultaneously at a fixed ratio relative to the vertical etch rate determined by the i-MacEtch condition. This feature can result in high AR nanostructures that are much narrower than the metal pattern, relaxing patterning requirements. Most of all, the sidewall smoothness is no longer limited by the metal catalyst pattern edge roughness and by nature, atomically smooth sidewalls can be produced. Record high AR (~ 50:1) InP fins with fin width as narrow as 12 nm were demonstrated by this method (ref). In contrast, pure wet etching such as H_3PO_4:HCl {110} selective facet etch produced vertical fins that were 200 nm in height.

However, it is strongly crystallographically dependent and impossible to scale the fin pitch since the lateral etching versus vertical etching rate cannot be tuned individually. In contrast, the etching behavior of MacEtch can be well controlled by the metal catalyst. To achieve the targeted etching profile and desired rate, the metal redox potential, oxidant, and acid ratio can be tuned [59, 127, 130].

5.2 Developing MacEtch for other materials, like Ge, InAs, $In_{0.53}Ga_{0.47}As$ and GaP

We have developed MacEtch for various materials systems, including Si, GaAs and InP, with lateral dimensions as small as sub-10 nm scale and AR as large as hundreds [60, 127, 128]. For this program, we will focus on Si, Ge, InP, and $In_{0.53}Ga_{0.47}As$, all of which are available in bulk or thick epitaxial layer form and well positioned for high speed or low power applications. Through these activities, we aim to study the mechanism of MacEtch of these materials for the required pattern size and pitch at the atomic level and manage the etching process to produce ultra-high AR fins with smooth sidewalls.

5.2.1 Achieving atomically smooth sidewalls with minimized interface states

All of these structures produced by MacEtch or i-MacEtch are free from high energy ion damage by nature. However, damage-free does not guarantee smoothness, which is also critical to high quality interface for FinFETs. For forward MacEtch where the non-stationary metal catalyst descends into the semiconductor, the sidewall is literally “engraved” by the Au pattern edge and ends up with exactly the complimentary pattern of the metal edge, as can be seen clearly in the example shown in Figure 5.2. The roughness produced this way can be improved by (1) the metal edge roughness; (2) inverse MacEtch (i-MacEtch) to allow etching underneath the metal, where the sidewall roughness is completely independent of metal edge roughness [60]; or (3) post-MacEtch chemical smoothing. All three approaches can be explored.

In the example shown before, atomically smooth high AR (50:1) InP fin array was achieved by i-MacEtch. The i-MacEtch process in that case was enabled by the insoluble thick layer of complex oxide underneath the catalyst metal (Au) [60]. Through this program, we will explore the mechanism of i-MacEtch by first fully characterizing the composition and formation process of the insoluble oxide, which may provide insights on enabling forward MacEtch for this material and i-MacEtch for other materials.

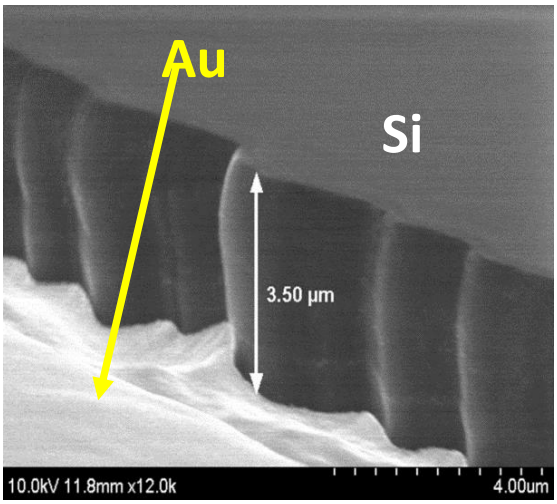

Figure 5.2: MacEtched sidewall roughness (SEM). The groove pattern on the Si sidewall follows exactly the Au metal edge roughness (lighter contrast), which was produced during the Au patterning in this exaggerated example.

To evaluate the etch roughness at the atomic level, TEM and atomic force microscope (AFM) [131] will be used by removing the fins and laterally placed onto a mechanical support. Simple MOS capacitors can be fabricated for C-V measurements [132] in order to characterize the interface states density D_{it} in order to evaluate the MacEtched surface quality.

The focus of this task is the development of the MacEtch process for producing ultra-high ARs fins of various materials with controlled fin width/height. To continue pushing the AR limit, several critical aspects of the MacEtch processes need to be understood and managed.

For forward MacEtch, maintaining an intimate interface between the constantly-moving catalyst metal layer and the semiconductor throughout the entire etching process becomes more challenging when the lateral dimension is reduced, which gives the metal layer more mobility. Understanding and controlling the etch rate determining step (e.g. carrier generation vs. mass transport) in each material and pattern size and pitch, under different acid/oxidant ratios and metal redox potentials, will require full-scale systematic efforts. In addition, if necessary, magnetic-field guided *h*-MacEtch [133] can also be used to force the metal layer to stay in place and enhance etching rate and reduce porosity.

We have already got some preliminary results for MacEtch on InAs/InGaAs, using the mixture of DI water, $KMnO_4$ and HF. The MacEtched results for InAs and InGaAs are promising but still need to be optimized. Due to the strong oxidation rate in MacEtched process, porous layers appear at the outermost pillars, resulting from excess holes generated that diffused to the substrate. The ways to solve this problem are to use a weaker oxidant or use digital etching [134, 135] to remove the porous area by further oxidation/acid removal.

For i-MacEtch, because it is not anisotropic like forward MacEtch, the goal and challenge are to enhance vertical vs. lateral etch rate, thus achieveing denser fin pitch. Note that i-MacEtch is different from pure wet chemical etching with a non-catalytic mask, because the catalytic etching in a solution that does not cause etching without the catalyst weakens the crystal orientation dependence and allows more control in etching anisotropy.

5.2.2 Searching for CMOS compatible MacEtch catalyst

The elephant in the room for MacEtch is the use of Au as the catalyst, which can be detrimental to CMOS, even though Au does not get consumed and the MacEtch process takes place at room temperature and thus there is no possible diffusion into Si. Efforts will be

dedicated to explore CMOS-compatible metal, e.g. W, Ni, graphene, etc., for this purpose. Through this study, the effect of metal work function, redox potential, size, and thickness on MacEtch will be explored.

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APPENDIX A - MODELING OF ONE-SIDED S/D CONTACT DOUBLE-GATE FINFET

In order to solve Poisson's equation, we need to apply a 3D box along the channel direction as shown in Figure A.1. Unlike the conventional definition, this 3D box is located at the drain side. Using the fully depletion approximation, we have equation (A.1):

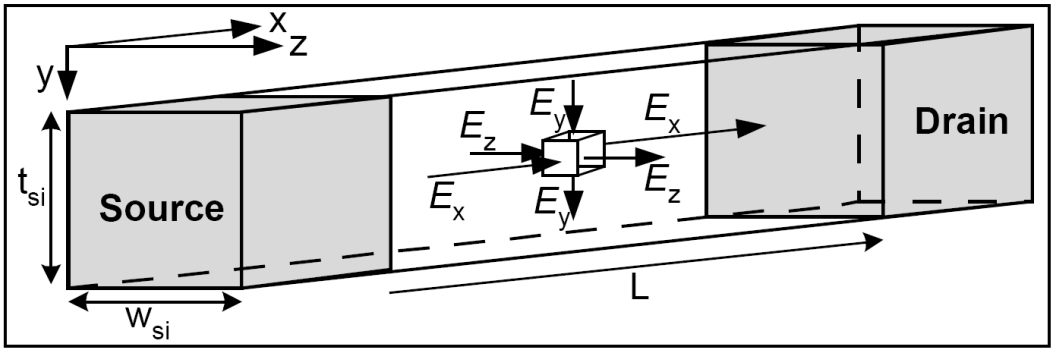

Figure A.1 Coordinate system and electric field components in a multiple-gate device. Reprinted with permission from chapter 1 of J.-P. Colinge, *FinFETs and Other Multigate Transistors*, (Springer, 2008).

$$\frac{d^2\Phi(x,y,z)}{dx^2}+\frac{d^2\Phi(x,y,z)}{dy^2}+\frac{d^2\Phi(x,y,z)}{dz^2}=\frac{qN_D}{\varepsilon_{si}} \tag{A.1}$$

Assuming ideal double gate, there is no variation in the z direction, then:

$$\frac{d\Phi(x,y,z)}{dz}=0 \tag{A.2}$$

We can simplify the Poisson's equation as:

$$\frac{d^2\Phi(x,y)}{dx^2}+\frac{d^2\Phi(x,y)}{dy^2}=\frac{qN_D}{\varepsilon_{si}} \tag{A.3}$$

where $\Phi(x,y)$ is the two-dimensional potential along the x-y plane, N_D is the carrier doping concentration at drain, q is the basic electron and $\varepsilon_{si}$is the permittivity of silicon.

The purpose is to find out the x component of potential distribution $\Phi(x,y)$, so we can know the relative lateral influence of the drain electric field on the channel potential. The universal solution of (A.1) can be written as

$$\Phi(x, y) = c_0(x) + c_1(x)y + c_2(x)y^2 \tag{A.4}$$

The boundary conditions for a double-sided S/D FinFET are

1. When t=0, $\Phi(x,0) = c_0(x)$, which is the surface potential.

2. When t=0, the electric field at the M-S junction interface is

$$c_1(x) = \frac{d\ \Phi(x, y)}{dy}|_{y=0} = E_M \quad \text{where } E_M = \frac{qN_D}{\varepsilon_{si}} \times W_{si} \tag{A.5}$$

3. When $t=W_{fin}$, the electric field at the M-S junction is just the opposite direction of the other fin side, so:

$$\frac{d\ \Phi(x, y)}{dy}|_{y=tsi} = -E_M \text{ and } c_2(x) = -\frac{E_M}{W_{fin}} \tag{A.6}$$

Substituting the boundary conditions into (A.1), we could obtain $\frac{d^2\Phi(x, y)}{dx^2} \propto 3qN_D$ for conventional FinFET. The boundary condition for a one-sided S/D contact FinFET is the same except that when $t=W_{fin}$, the electric field at the M-S junction is approximately zero. Therefore, from similar deduction, we can obtain $\frac{d^2\Phi(x, y)}{dx^2} \propto 2qN_D$.

The coefficient for the x-component of $\Phi(x,y)$ is 50% smaller for a one-sided S/D contact FinFET, which means a weaker lateral expansion of drain electric field. The device should suffer less from SCE because of a stronger gate electrostatic control. It is interesting to note that the reduction of the coefficient by structural innovation is equivalent with reducing drain doping concentration N_D, which is well known historically for mitigating charge sharing effects as lateral channel doping engineering.

The results are verified by 3D numerical simulation. We have investigated the conduction energy potential barrier E_c vs. position along the channel direction. It can be found that the E_c profile for 50% lower $N_{S/D}$ doping concentration for double-sided SDE contact FinFET exactly

matches with the one with 50% higher $N_{S/D}$ doping concentration for the one-sided SDE contact FinFET, just as reducing $N_{S/D}$ is the same as reducing SDE contacts. SCE is improved because of weaker drain electric field penetration.

APPENDIX B - DETAILS OF PROCESS FLOW E-BEAM LITHOGRAPHY

All e-beam lithography is performed in a nanoengineering workstation (eLine RAITH) in the Materials Research Lab at the University of Illinois. The standard process flow for electron beam lithography is listed as follows:

1 Standard solvent clean using acetone, methanol, isopropanol.

2 Pre-bake in hot plate for 80s at 180˚C.

3 Spin on e-beam resist (PMMA A4) for a certain thickness.

4 Post-bake in hot plate for 2 min at 200˚C.

5 E-beam exposure at various doses and energies.

6 Develop in MIBK:IPA for 50s.

7 Rinse in IPA for 30s and blow using N_2 gun.

8 Optional: O_2 plasma RIE etch at 150W for 10s.

For different patterning, fins, S/D or gate, there are different requirements for the parameters of each step. For small patterns, we spin 200 nm PMMA at 2500 rpm for 60s in step 3. Since the fins are high, we need to significantly increase the thickness of PMMA to conformally cover the entire fins. We spin twice: spin 300 nm PMMA at 1500 rpm for 60s and repeat step 3 and 4 to spin 200 nm PMMA at 2500 rpm for 60s, aiming to get a total thickness of 500-600 nm PMMA.

For fin patterns with 200 nm PMMA A4, the energy selected is 10 kV and the dose is around (0.9-1.3)×100 $\mu C/cm^2$ of the basis dose. For patterning S/D and gate on top of the high-

aspect-ratio fins, we still use 10 kV accelerating voltage while using a high dose of (2.1-2.4) $\mu C/cm^2$ of the basis dose.

APPENDIX C - MACETCH OF INP SUSPENDED NANOWIRES

Different etching conditions are explored for InP MacEtch. By increasing oxidant concentration H_2O_2 and choosing a certain alignment orientation, we can produce suspended nanowires by MacEtch.

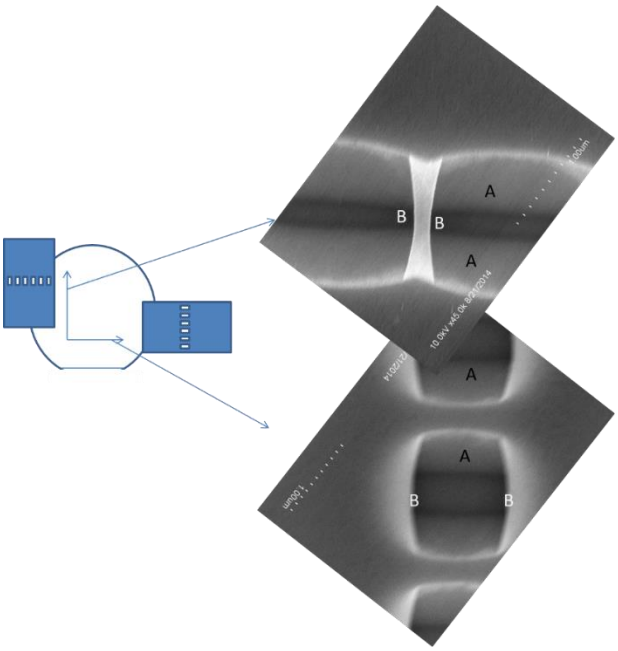

Figure C.1: Schematic of layout and the corresponding SEM images for the etched structures for two different angles, respectively.

Figure C.1 shows the layout and etching results of InP for 0˚ and 90˚ along the wafer flat edge. Etching along sidewall A has an acute angle α, while etching along sidewall B has an angle of negative β. If the fins are aligned with 0˚ associated with the wafer flat edge, there is a significant undercut of fins. As the undercut goes, the underneath area may be completely removed such that suspended nanowires are formed.

Figure C.2 shows the optimized etching results showing the minimal fin size of 12 nm. To the best of our knowledge, there is no way to fabricate suspended nanowires without sacrificial layers. It is much simplified compared to the selective RIE etching, without attacking the surface

which should have great potential for the application of III-V nanowire gate-all-around transistors.

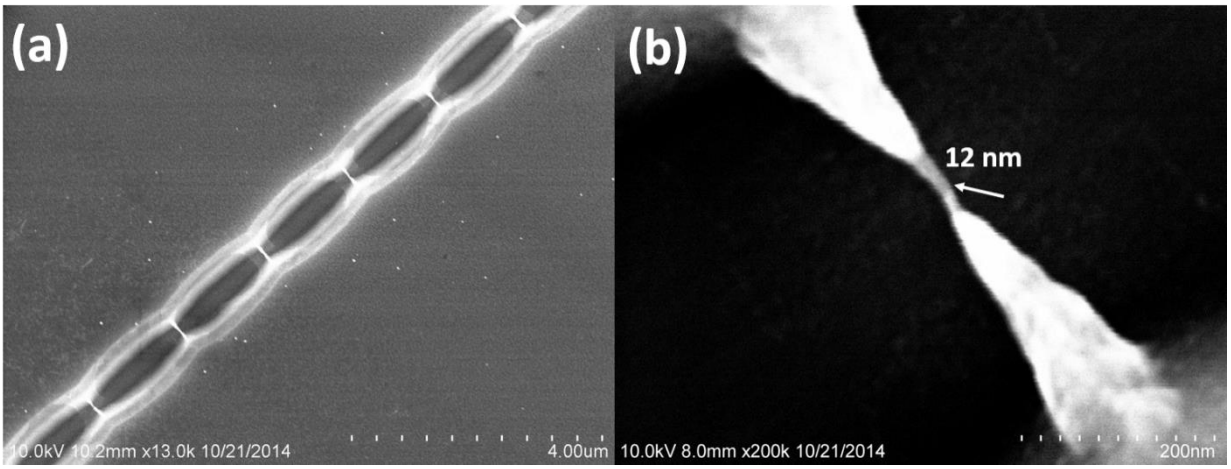

Figure C.2: Suspended nanowires fabricated by MacEtch. (a) SEM images for the fin arrays; (b) zoomed-in picture for one nanowire with minimal width of 12 nm.

APPENDIX D - LIST OF PUBLICATIONS AND PATENTS

Journal Publications

[1] Yi Song, Parsian K. Mohseni, Seung Hyun Kim, Jae Cheol Shin, Ilesanmi Adesida, and Xiuling Li, “Ultra-high-aspect-ratio InP junctionless FinFETs by metal-assisted chemical etching for extreme scaling,” *IEEE Electron Device Lett.,* vol. 37, issue 8, pp. 970, 2016.

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Pending Publications

[1] Yi Song, Wenjuan Zhu, Ilesanmi Adesida and Xiuling Li, “Nanoscale FinFETs design with one-sided source/drain extension contacts for low power applications,” In preparation for submission, 2016.

[2] Yi Song, and Xiuling Li, “Nanoscale FinFETs with asymmetric gate-source/drain overlap,” In preparation for submission, 2016.

Conference proceedings:

[1] Yi Song, Parsian K. Mohseni, Seung Hyun Kim, Jae Cheol Shin, Chen Zhang, Kelson Chabak, and Xiuling Li, "Metal-Assisted Chemical Etching: A New Nanomanufacturing Method for III-V Junctionless 3D MOSFETs with Damage-free, High-Aspect-Ratio Fins," *73th Device Research Conference,* Columbus, OH, June, 2015.

[2] Yi Song, Huajie Zhou, Qiuxia Xu, Jun Luo, Chao Zhao and Qingqing Liang, " High Performance N- and P-Type gate-all-around Nanowire MOSFETs Fabricated on Bulk Si by CMOS-Compatible Process," in *69th Device Research Conference*, Santa Barbara, CA, June, 2011.

Patents

[1] US Patent TF12047-US, "Field Effect Transistor Structure Comprising A Stack of Vertically Separated Channel Nanowires", with Yi Song and Xiuling Li, Application No. 13/896,537.

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[5]CN Patent Accept No. 200910242770.6, "A novel method for fabricating ultra-short gate length gate-all-around nanowire MOSFETs on bulk substrate," with Yi Song, Qiuxia Xu and Huajie Zhou.

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[7] CN Patent Accept No. 201010578678.X, "A new method for fabricating gate-all-around metal-oxide- semiconductor field effective transistor," with Huajie Zhou, Yi Song and Qiuxia Xu.