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# THREE-DIMENSIONAL FIELD-EFFECT TRANSISTORS WITH TOP-DOWN AND BOTTOM-UP NANOWIRE-ARRAY CHANNELS

BY

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DISSERTATION

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# ABSTRACT

This dissertation research effort explores new transistor topologies using three-dimensional nanowire (NW)-array channels formed by both bottom-up and top-down synthesis. The bottom-up NW research centers on the Au-catalyzed planar GaAs NW assembly discovered at the University of Illinois Urbana-Champaign (UIUC). The top-down NW research approach involves plasma etching of an emerging wide-bandgap material, Gallium Oxide ($Ga_2O_3$), to make arrays of NW channels (or fins) for high-power electronics.

Bottom-up AlGaAs/GaAs heterostructure core-shell planar NWs are demonstrated on a wafer scale with excellent yield. Their placement is determined by lithographically patterning an array of Au seeds on semi-insulating GaAs substrate. The GaAs NWs assemble by lateral epitaxy via a vapor-liquid-solid mechanism and align in parallel arrays as a result of the (100) GaAs crystal plane orientation; then, a thin-film AlGaAs layer conforms to the GaAs NWs to form AlGaAs/GaAs NW high-electron mobility channels. Radio frequency (RF) transistors are fabricated and show excellent dc and high-frequency performance. An $f_{max}$ > 75 GHz with < 2 V supply voltage and $I_{ON}/I_{OFF} > 10^4$ is measured which is superior compared to carbon-based nanoelectronics and "spin-on III-V NWs". A comprehensive small-signal model is used to extract the contributing and limiting factors to the RF performance of AlGaAs/GaAs NW-array transistors and predict future performance. Finally, a process is developed to show that III-V NWs on sacrificial epitaxial templates can be transferred to arbitrary substrates.

Top-down NWs were formed from Sn-doped $Ga_2O_3$ homoepitaxially grown on semi-insulating beta-phase $Ga_2O_3$ substrates by metal-organic vapor phase epitaxy. First,

conventional planar transistors were fabricated from a sample set to characterize and understand the electrical performance as a function of Sn-doping and epitaxial channel thickness. Second, the high-critical field strength was evaluated to highlight the benefit of using $Ga_2O_3$ as a disruptive technology to GaN and SiC. Lastly, the planar transistor results feed into a design for a top-down NW-array transistor. The $Ga_2O_3$ NW-arrays were formed by $BCl_3$ plasma etching. A new wrap-gate transistor demonstrates normally-off (enhancement-mode) operation with a high breakdown voltage exceeding 600 V which is superior to any transistor using a 3D channel.

*To my best friend and wife, Amber, and my two precious kids, Kenleigh and Maverick.*
*My success is because of all of your sacrifice and support.*

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## TABLE OF CONTENTS

**1. INTRODUCTON TO NANOWIRE ELECTRONICS ........................................ 1**

1.1 Toward 3D Transistor Channels ........................................ 1

1.2 Bottom-Up versus Top-Down Nanoelectronics ........................................ 5

1.3 NW Transistors for RF ........................................ 7

1.4 NW Transistors for Power ........................................ 8

1.5 Organization of Dissertation ........................................ 9

1.6 Figures and Table ........................................ 11

**2. LITERATURE REVIEW ........................................ 14**

2.1 High-Speed Nanoscale Transistors ........................................ 14

2.2 High-Power NW Transistors ........................................ 23

2.3 Figures ........................................ 25

**3. BOTTOM-UP NW-ARRAY AlGaAs/GaAs HEMT ........................................ 29**

3.1 Growth of AlGaAs/GaAs NW HEMTs ........................................ 29

3.2 Wafer-Scale NW HEMTs in Dense Lateral Arrays ........................................ 31

3.3 NW-HEMT Device Fabrication ........................................ 33

3.4 NW-HEMT DC Electrical Characterization ........................................ 35

3.5 Figures ........................................ 37

**4. TRANSFER PRINTING OF GaAs NWS TO ARBITRARY SUBSTRATES ... 44**

4.1 Engineered NW Sacrificial Epitaxy ........................................ 44

4.2 Transfer-Last Process Development ........................................ 45

4.3 Transfer-First Process Development ........................................ 47

4.4 Figures and Table ........................................ 50

**5. RF CHARACTERIZATION AND MODELING OF AlGaAs/GaAs NW-ARRAY TRANSISTORS ........................................ 56**

5.1 Introduction ........................................ 56

5.2 Equivalent Circuit Model and RF Setup ........................................ 57

5.3 NW-HEMT RF Characterization Results ........................................ 60

5.4 NW-HEMT Equivalent Circuit Extraction Procedure ........................................ 62

5.5 NW-HEMT RF Performance versus Bias and $L_G$ ........................................ 65

5.6 Figures and Tables ..................70

**6. TOWARD TOP-DOWN NW $Ga_2O_3$ MOSFETS ..................84**

6.1 Device Development of $Ga_2O_3$ MOSFETs ..................85

6.2 $Ga_2O_3$ Doping and Thickness Study ..................86

6.3 Critical Field Strength Potential of $Ga_2O_3$ MOSFETs ..................90

6.4 Top-Down NW $Ga_2O_3$ MOSFET ..................92

6.5 Figures and Tables ..................100

**7. CONCLUSIONS AND FUTURE WORK ..................112**

7.1 Research Achievements ..................112

7.2 Future Work ..................113

**REFERENCES ..................116**

**APPENDIX A. NANOSCALE RF TRANSISTOR TABLES ..................127**

**APPENDIX B. SMALL-SIGNAL MODEL EXTRACTION CODE ..................133**

# 1. INTRODUCTON TO NANOWIRE ELECTRONICS

In electronics, a textbook nanowire (NW) is a path of discrete solid semiconductor constrained in two dimensions such that carriers are quantum confined in one dimension along the length of the NW. The degree of quantization depends on the dimensions of the constrained planes and the electronic structure of the semiconductor material—specifically the electron effective mass. For example, InAs quantum NWs, with among the lightest effective masses of common semiconductors, can be realistically fabricated with nanoscale lithography and quantized conduction has been observed [1]. NWs in this sense could have interesting applications for very low-power logic, ballistic transport, and a variety of opto-electronics (nanoscale LEDs, lasers, etc.). Though, for field-effect transistor (FET) amplifiers, implementing quantum NWs may be challenging due to the one-dimensional density of states available. For a traditional power amplifier, a high density of states is desired to maintain adequate current and benefit other significant transistor metrics such as transconductance and speed. In this research, a proposal for a NW width relaxed to sub-micron dimensions will have quasi-one-dimensional properties while its “bulk-like” three-dimensional (3D) cross section remains advantageous for enhanced electrostatic channel control.

## 1.1 Toward 3D Transistor Channels

The fabrication of electronic devices has traditionally relied on bulk, or planar, semiconductor processing technologies. A bulk semiconductor device is a two-dimensional (2D) planar technology where epitaxial layers are grown on a polished

semiconductor wafer surface (say in the *x-y* plane). Electrical isolation between numerous devices on a wafer is achieved by top-down etching of the bulk semiconductor leaving multiple 2D "mesas" on the wafer surface. In an FET, the gate voltage potential modulates carriers injected into the source which flow through the active layers on the "mesas" and collect at the drain. Close proximity of the gate with an adequate footprint (width, $W_G$, and length, $L_G$) to the carriers flowing from source to drain gives better static transistor characteristics since the electrostatic coupling is stronger. It should be noted that a good static transistor is, generally, a prerequisite for a good RF transistor which will be discussed in Section 1.3. FET dc performance is dependent on device and gate geometry and is represented by a parallel plate capacitor with a dielectric thickness ($t$) and electrical permittivity ($\varepsilon$) spatially separating two different electrical potentials. The capacitance, $C_G$, is expressed as

$$C_G = \frac{\varepsilon \cdot W_G \cdot L_G}{t} \quad \text{(F)} \tag{1}$$

It is clear that high permittivity and small dielectric thickness are desired to maintain high capacitive coupling between the channel and gate contact. Reducing the lateral dimension from source-to-drain ($L_{SD}$) is also necessary to reduce channel resistance. However, at some point, $C_G$ can become insufficient for device operation if $t$ becomes too large or, more commonly, $L_G$ and/or $L_{SD}$ is too small. The latter is the case with aggressive modern day technology scaling—the device dimensions are 14 nm and still shrinking [2]. In this case, the channel modulation is equally or more dependent on the lateral electrical field (instead of vertical gate-channel electric field) coming from the drain terminal—an effect known as drain induced barrier lowering (DIBL). In a similar scenario, when the gate length ($L_G$) becomes too small the vertical gate-channel electric

field is weak with poor channel modulation. Both anomalies are types of short-channel effects (SCE).

Now suppose 2D mesas are cut into dense parallel arrays of aggressively scaled "nano-channels" as illustrated in Figure 1. The "nano-channels" are commonly referred in literature as fins, nano-ribbons, nano-belts, and "NWs". Here, "NWs" is put in quotes because, generally, NWs are defined as quasi-one-dimensional (1D) structures synthesized using bottom-up metal-catalyzed growth processes [3]. Regardless of the name, these 3D channels have a unique three-dimensional (3D) geometry which allows the gate terminal to wrap along the sides, top, and—in a suspended channel—the bottom facet as well. The "multi-gate" or "wrap-gate" configuration significantly strengthens the gate-channel electrostatics. In other words, *the same $L_G$ wrapping around arrays of NWs will mitigate SCE over the same $L_G$ on a 2D planar mesa*. It is for this reason that Intel has experienced resounding success with the tri-gated silicon complementary metal-oxide-semiconductor (CMOS) transistor [2, 4, 5]. The static performance advantage of 3D channels is defined as the voltage gain, or intrinsic gain, expressed as

$$G_o = \frac{G_M}{G_{DS}} \quad \text{(unitless)} \tag{2}$$

where GM is the dc transconductance ($dI_{DS} / dV_{GS}$) and $G_{DS}$ is the dc output conductance ($dI_{DS} / dV_{DS}$) and are both measured from the FET current-voltage ($I$-$V$) curves. Figure 2 (a) illustrates the improvement of $G_o$ using a 3D silicon fin-FET over conventional planar Si FETs which can be implied for other semiconductors as well [6]. The $G_o$ is significantly better via $G_{DS}$ reduction while the $G_M$ is basically the same for planar and 3D channels per unit width ($W$). $W$ is the sum of sides and top facet lengths in contact

with the gate. A general trend is the $C_G$ rises linearly with $G_M$. In fact, equation (1) can be alternatively expressed as

$$\frac{C_G}{L_G} = \frac{G_M}{v_{eff}} \qquad \text{(F/cm)} \tag{3}$$

where $v_{eff}$ is the effective velocity of carriers (electrons and holes) in the transistor channel. If we assume carrier transport remains unchanged by reducing a mesa to *high-density* "nano-channels" then we can conclude the delay factor, $G_M / C_G$, essentially remains unchanged. The cutoff frequency ($f_T$), defined as the theoretical speed which electrons transport can be switched on and off under the intrinsic gated region, is strictly dependent on the delay factor and expressed as

$$f_T = \frac{1}{2\pi}\left(\frac{1}{\tau}\right) = \frac{1}{2\pi}\left(\frac{v_{eff}}{L_G}\right) = \frac{1}{2\pi}\left(\frac{G_M}{C_G}\right) \qquad \text{(Hz)} \tag{4}$$

In Figure 2(b), the effect of $f_T$ has been characterized for silicon fin-based FET versus conventional planar FET and confirms the marginal improvement of switching speed for by transforming the channel from 2D to 3D for digital electronics. This device was fabricated by top-down lithography with tight control over the fin spacing which is important to preserve RF performance.

The motivation behind 3D transistors overwhelmingly favors static over analog performance. In fact, very little is reported about the high-speed performance of 3D transistors because, frankly, based on speed alone there is no justification to outperform state-of-the-art planar devices. For example, III-V and silicon FETs have achieved $f_T$ of 688 and 485 GHz, respectively [7, 8]. Still, however, some researchers are actively pursuing the analog performance of 3D transistors for RF applications mainly to understand the drawbacks related to the spacing and geometry of fins [9, 10]. For

example, while the fin geometry improves dc performance, the unused space between adjacent fins forms a parasitic capacitance between the gate, source and drain terminals. Essentially, the $G_M$ and $C_G$ in equation (4) are normalized by different $W_G$; the $G_M$ is normalized by a smaller $W_G$ since the transistor $G_M$ occurs only on the 3D fins; however, the $C_G$ builds up mostly on the fins, but also in the gaps with an overall larger $W_G$ so $f_T$ usually is reduced. ***Reducing the gaps between 3D channels is critical for RF nanoelectronic devices.***

Suppose the gaps between nano-channels can be engineered to have a small parasitic capacitance effect. The $f_T$ would approach a planar FET, but for RF applications, the maximum frequency of oscillation ($f_{max}$) is generally accepted as the figure of merit (FoM) which incorporates device layout such as ohmic and gate resistance to amplify RF signals with higher output power [11]. The expression for $f_{max}$ is

$$f_{\max} = \frac{f_T}{2\sqrt{G_{DS}\left(R_G + R_i + R_S\right) + 2\pi f_T R_G C_{gd}}} \propto \frac{G_M}{\sqrt{G_{DS} + G_M}} \qquad \text{(Hz)} \qquad (5)$$

and is not only dependent on $f_T$ but also the three terminal resistances ($R_G$, $R_S$, $R_D$), channel charging resistance ($R_i$), and feedback capacitance ($C_{gd}$). Most importantly, it should be noted that embedded in equation (5) is a similar expression to $G_o$ in equation (2). Apparently, by engineering 3D nano-channels with negligible spacing between fin channels, excellent dc and RF performance may be obtained.

## 1.2 Bottom-Up versus Top-Down Nanoelectronics

The debate on how to build semiconductor devices as the dimensions begin to approach sub-micrometer dimensions is ongoing—bottom-up or top-down processing?

There is no doubt the "safe" answer is "top-down" because the planar processing techniques are incredibly well-understood and cost-effective. As can be seen by modern day CMOS, the nanoscale channels are becoming 3D to gain back the electrostatic control which is otherwise lost with a planar channel. However, the 3D channels must be etched from bulk material in top-down processing, and the sidewalls become rough and rich with defects. Surface channel FETs such as silicon MOSFETs in inversion-mode and high-electron mobility sheet channels can be particularly sensitive to surface roughness. Junctionless MOSFETs, on the other hand, do not invert their channels; instead, these use the entire channel bulk and have been considered to be possibly less sensitive to surface roughness [12]. At some point; these sidewalls will become so close together that the active channel width diminishes and is dominated by surface depletion from a non-ideal interface rich with traps and defects. These defects create trapping centers and degrade device performance. Additional processing techniques to reduce sidewall damage have been considered such as light wet-etching and high-temperature annealing.

Conversely, NWs grown by bottom-up self-assembly are molecularly constructed from a super-saturated metal catalyst—a process known as vapor-liquid-solid (VLS) epitaxy. In essence, VLS NWs are assembled *in-situ* with a diameter and length dictated by the size of the metal seed nanodots and growth time, respectively [13]. Further, the growth mechanism can be switched from VLS epitaxy to conventional thin-film epitaxy to make III-V NW heterojunctions such as NW-based HEMTs [14]. III-V NWs can also be grown by selective area epitaxy (SAE), but this method uses aggressively scaled "top-down" EBL line patterning which can cause roughened NWs [15]. Further, core-shell

NW heterojunctions can be challenging for SAE NWs. The main disadvantages for NWs grown by VLS are the linear packing density and lack of mature unidirectional growth technology. A summary of advantages and disadvantages of nanowire channel synthesis is shown in Figure 3.

## 1.3 NW Transistors for RF

The big question surrounding 3D III-V NWs is "why choose a NW FET over today's mature planar technology?" This is an excellent question, and it can be answered by assessing relevant state-of-the-art III-V NW electronic devices—*"what are research groups around the world trying to achieve that cannot be done with planar III-V FETs?"* ***One clear answer is heterogeneous integration toward multiple semiconductor materials in-plane without complex chip bonding.*** Due to the non-discrete channels of conventional FETs, transfer printing of planar mesas is difficult and only reported for silicon and III-V "nano-membranes" with limited success (i.e., much lower $f_{max}$ than predicted by $L_G$ and $v_{eff}$) [16-18]. In industry, heterogeneous integration of high-mobility III-V semiconductors onto silicon substrates has garnered extreme attention for system-on-chip (SoC) applications with multi-function sensing. For example, the III-V layer can provide low noise and high gain for RF sensing while driven by modern day complementary metal-oxide-semiconductor (CMOS) devices on the silicon layer. Or, perhaps there will be a push for light-weight conformal (flexible) wireless electronics for wearable commercial and/or unmanned military flight vehicles. Impressive III-V/Si heterogeneous integration has been demonstrated with Si CMOS wafers with either

mismatched III-V epitaxy on silicon or complex chip assembly [19-23]. However, all methods are complex and require stacking silicon or III-V "chiplets" which are still tens of microns out of plane from other layers. Using VLS NW epitaxy, transfer printing NW devices is a distinct advantage over planar FETs. VLS NWs can easily transfer to any non-native substrates and remain *in-plane* for easy interconnecting [13, 24].

## 1.4 NW Transistors for Power

The previous sections discussed NWs as they pertain to applications for low-power switching and RF because of the small bandgap of III-V and silicon. Conversely, high-power transistors require wide bandgap (WBG) semiconductors for high breakdown voltage ($V_{BK}$) applications. The $V_{BK}$ is related to the bandgap of the semiconductor ($E_G$) by $V_{BK} \sim E_G^{1.5}$ [25]. A comparison of common WBG semiconductors is shown in Table 1. Clearly, GaN, SiC, diamond, and, most recently, gallium oxide ($Ga_2O_3$) are of high interest. GaN and SiC are the most mature WBG semiconductors but have been plagued by high-cost substrate synthesis. GaN is grown heteroepitaxially on Si and SiC with high performance but has more defects due to the lattice mismatch. Conversely, $Ga_2O_3$ has a native substrate grown by melt-growth and should become very affordable after device demonstrations emerge showing high-performance and thermal solutions.

Power electronics applications usually require a normally-off operation for high-voltage safety and ultra-low gate leakage and power dissipation. A wrap-gate device can deplete the channel as result of a built-in potential penetrating in the NW channel from the top and sides while the access regions remain undepleted. Not only does this reduce

SCE as discussed above, it can also lead to high breakdown operation. The same NW challenge for RF applies here—a high density of NW channels is necessary for high drive current in the on-state. The FoMs for power electronics are the Johnson FoM (addressing high-frequency power) and Baliga FoM (addressing conduction losses). Overall, $Ga_2O_3$ is among the leading candidates since it has a wider bandgap than GaN and SiC, can be readily doped, and can be grown homoepitaxially.

## 1.5 Organization of Dissertation

A "big-picture" overview of integrating NWs as a transistor channel has been highlighted in this chapter. In the following dissertation research, both bottom-up and top-down NW synthesis will be explored to make novel FETs. Two main efforts were explored in this dissertation: (1) bottom-up NWs using parallel arrays of GaAs NWs grown by selective lateral epitaxy are investigated on semi-insulating GaAs substrates toward a high-speed, low-power technology transferrable to other substrates; (2) access to an emerging ultra-wide bandgap (UWB) semiconductor, $Ga_2O_3$, became available during this research as a revolutionary power electronics material. $Ga_2O_3$ MOSFETs have only been demonstrated once on (010) surface orientation before this research. During this research, we collaborated with growth on (100) surface orientation; thus, significant planar $Ga_2O_3$ MOSFET process development was first investigated followed by design and fabrication toward a desired normally-off MOSFET operation using top-down NW synthesis. A chapter breakdown is as follows:

Chapter 2 discusses background of low- and high-power transistors using nanotechnology.

Chapter 3 discusses fabrication and dc characterization of novel AlGaAs/GaAs NW array HEMTs by bottom-up synthesis.

Chapter 4 discusses process development toward a transferrable III-V NW technology on a sacrificial epitaxial template.

Chapter 5 discusses the theory, measurement, and modeling of the RF characteristics of the fabricated AlGaAs/GaAs NW array HEMTs.

Chapter 6 discusses the fabrication and characterization of planar $Ga_2O_3$ devices which culminate in a top-down NW $Ga_2O_3$ MOSFET with normally-off operation.

Chapter 7 addresses the conclusions of this dissertation and comments on the challenges and next steps for continuing research in NW transistors.

## 1.6 Figures and Table

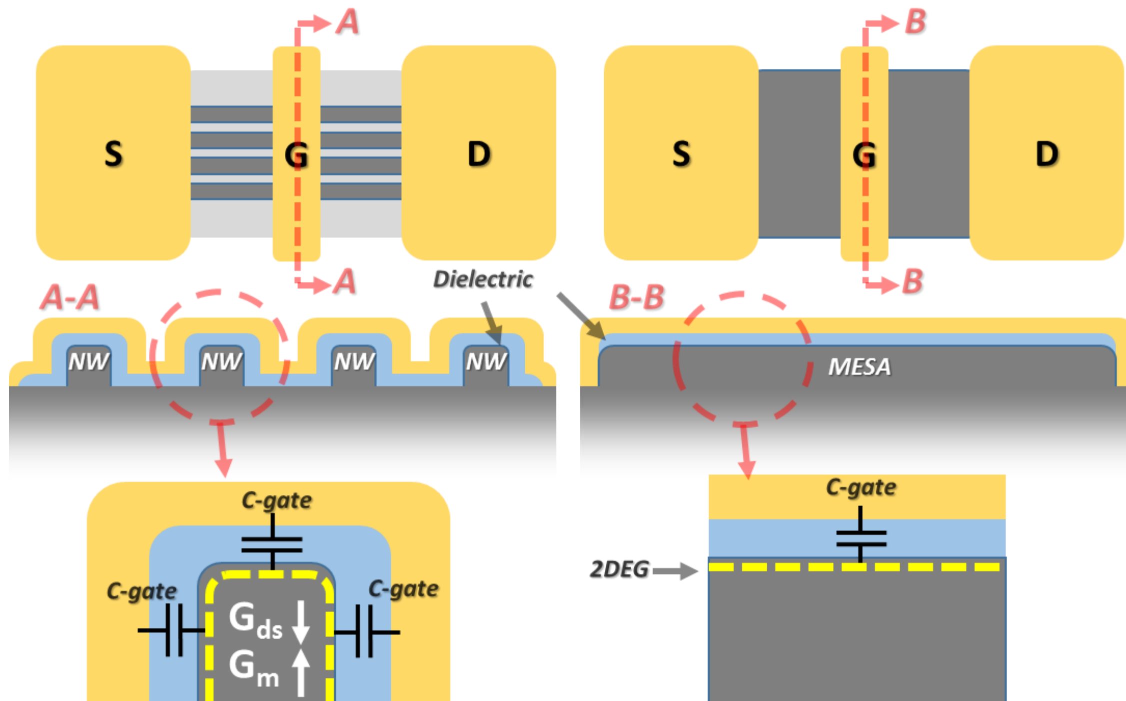


**Figure 1**: (left) 2D channel fins to form wrap-gated transistors with high voltage gain, and (right) conventional planar transistor structure with simple parallel-plate capacitor.

(a) (b)

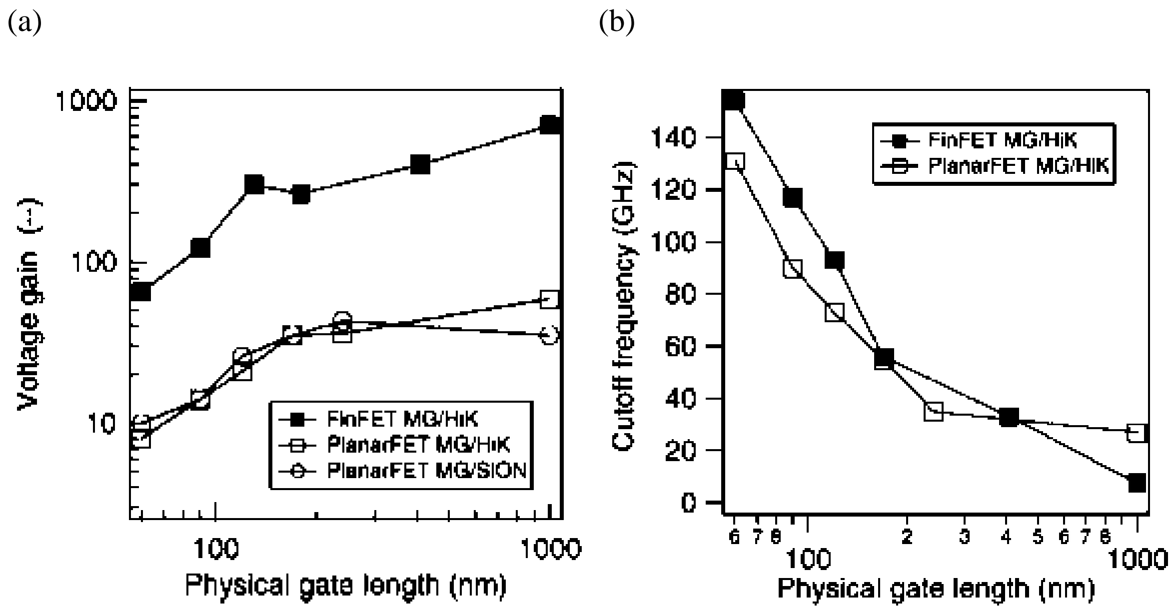


**Figure 2**: Comparison of a planar FET and 3D (finFET) evaluated by the (a) voltage gain and (b) cutoff frequency versus gate length. The finFET has significantly improved voltage gain and marginally better cutoff frequency. The study used silicon CMOS devices employing a multiple-gate (MG) contact with high-κ (HiK) gate dielectric (reprinted with permission from ref. [6] ©Copyright [2006] IEEE ).

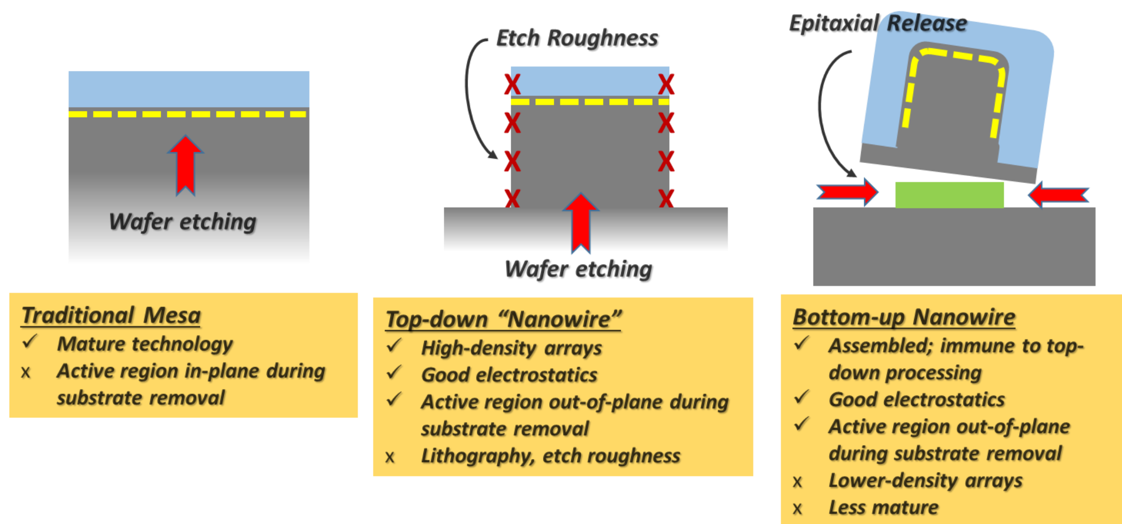


**Figure 3**: Channel evolution from (left) traditional mesa-based FET to (middle) 3D top-down "NWs" or fins to (right) bottom-up assembly of NWs.

**Table 1**: Comparison of Figures of Merit for Common Power Semiconductors (credit: Drs. Gregg Jessen and Stefan Badescu, AFRL)

| | Si | GaAs | 4H-SiC | GaN | Diamond | β-$Ga_2O_3$ |
|---|---|---|---|---|---|---|
| $E_G$ (eV) | 1.1 | 1.4 | 3.3 | 3.4 | 5.5 | 4.9 |
| μ ($cm^2$/V·s) | 1400 | 8000 | 1000 | 1200 | 2000 | 300 |
| $E_C$ (MV/cm) | 0.3 | 0.4 | 2.5 | 3.3 | 10 | 8 |
| $\varepsilon_{REL}$ | 11.8 | 12.9 | 9.7 | 9 | 5.5 | 10 |
| $v_{SAT}$ ($10^7$ cm/s) | 1.0 | 1.2 | 2.0 | 2.5 | 1.0 | 1.1 |
| λ (W/m·K) | 150 | 50 | 370 | 130 | 2000 | 10, 30 |
| BFOM ($\mu\varepsilon E_C^3$) | 1 | 15 | 340 | 870 | 24661 | 3444 |
| JFOM ($v_{SAT}E_C$) | 1 | 2 | 17 | 28 | 33 | 29 |

# 2. LITERATURE REVIEW

This chapter presents background information on nanoscale channel transistors to set the stage for the design, fabrication, characterization and the integration of bottom-up and top-down NW transistors presented in the following chapters. NWs and nanotubes (NTs) became technologically feasible after certain milestone demonstrations first appeared in the early 2000s; a summary of relevant studies will be given. In parallel, 2D materials have been heavily proposed as next-generation devices competing with NW/NT solutions. The vast majority of literature provides examples for low-power, high speed performance. Still, however, nanotechnology lacks behind conventional planar technology, but can be quite superior in terms of ease of heterogeneous integration. In contrast, NWs for WBG semiconductors are far more compelling for high-power MOSFETs and normally-off high-voltage applications; though, very few are reported in literature. In any case, nanotechnology remains in its infancy stages with significant room for future materials and device development.

## 2.1 High-Speed Nanoscale Transistors

RF electronics for wireless commercial and military applications rely heavily on high mobility, low noise III-V semiconductors. Over the last 35 years, since the invention of the high-electron mobility transistor (HEMT), there has been an endless push for ultra-high-speed transistors. Much of the increase is demanded by the commercial wireless market and, more recently, by high-power military applications. RF transistors are fundamentally different than, for example, logic transistors, because the

input signal oscillates with a particular frequency and amplitude superimposed on the dc voltage. The signal is amplified by the RF transistor depending on its gain-frequency characteristics. The maximum frequency an RF transistor can amplify the input with unity gain is referred to as the $f_{max}$. For most RF applications, the $f_{max}$ is the FoM to evaluate RF devices since wireless signals need to be amplified with a power gain [11]. With $f_{max} > f_T$, an RF transistor can amplify signals higher than its $f_T$ value but lower than the $f_{max}$ since a small current gain less than 1 is compensated by a larger voltage gain (net power gain > 1) [26]. Therefore, design tradeoffs making the $f_{max} > f_T$ are common.

The most pivotal point in the development of RF devices was the formation of a high-electron mobility two-dimensional electron gas (2DEG) in III-V heterostructures. The first to exploit this, Mimura proposed the n-AlGaAs/GaAs-based HEMT in 1980 [27]. The basic operational theory of HEMTs is a wider-bandgap semiconductor with a supply of donor electrons (i.e., n-doped AlGaAs), or net polarization charge (i.e., undoped wurtzite AlGaN) against an intrinsic channel (i.e., GaAs, GaN in these two examples) forms a quantum well (QW) two-dimensional electron gas (2DEG) as a result of band-bending to align their Fermi levels ($E_F$). The QW 2DEG can be modulated like a switch with an applied gate voltage. An AlGaAs/GaAs HEMT band diagram schematic is shown in Figure 4 which is normally-on (depletion-mode) at equilibrium.

Since 1980, frequency performance has been unprecedented: GaN HEMT with $f_T/f_{max}$ = 450/440 GHz [28]; InAs/InP pseudomorphic HEMT (pHEMT) with $f_T/f_{max}$ = 644/681 GHz [29]; InGaAs/GaAs metamorphic HEMT with $f_T/f_{max}$ = 688/800 GHz [8]; and InGaAs/InAlAs/InP HEMT with $f_T/f_{max}$ = 0.38/1.1 THz have been reported [30, 31].

To date, III-V HEMTs offer the best combination of $f_T/f_{max}$ and noise performance of any device.

### 2.1.1 Nanosheet RF Transistors

The most widely cited solution is to replace the traditional transistor mesa with an atomically precise nanosheet with high mobility. Currently, graphene is the most popular choice because it has been shown theoretically its room-temperature (RT) electron and hole mobility is 2-3 orders of magnitude higher than III-V semiconductors [32]. For this reason, graphene has an impressive record $f_T > 300$ GHz [33]. However, the record $f_{max} =$ 70 GHz and $I_{ON}/I_{OFF} < 100$ is much lower than predicted [34]. The culprit for low $f_{max}$ is the zero-bandgap electronic structure which causes high output conductance in saturation. This type of RF performance is more typical of logic transistors requiring high $f_T$, though the bandgap issue is also critical for digital electronics. Therefore, so far, graphene for use in logic and RF electronics has been disappointing. The most appealing aspect of graphene is it can be synthesized by chemical-vapor deposition on semi-insulating SiC or transferred to any substrate. A de-embedded $f_{max}$ has been experimentally measured as 70 GHz [34], 29 GHz [33] and 2-4 GHz [35, 36] on SiC, glass and flexible polymer substrates, respectively.

More nanosheets have been discovered such as transition metal dichalcogenides (TMDs) with the presence of a bandgap but at the expense of RT mobility about an order of magnitude lower than III-V semiconductors. Among the most researched is molybdenum disulfide ($MoS_2$) with a direct bandgap of ~1.8 eV and bulk mobility in the

range of 200-500 $cm^2/Vs$ [37]. Few layer $MoS_2$ mobility measurements were reported around 200 $cm^2/Vs$ [37, 38]. $MoS_2$, so far, is superior to graphene as it can be heterogeneously integrated with better RF gain and $I_{ON}/I_{OFF}$ operation for a variety of applications. $MoS_2$ RF devices were first reported and integrated on silicon by H. Wang et al. in 2012 with $f_{max}$ = 1 GHz for $L_G$ = 300 nm and $I_{ON}/I_{OFF}$ ~ $10^9$ showing far more promise than graphene [39]. In 2014, an $f_{max}$ = 50 GHz was reported with $MoS_2$ integrated with silicon and $f_{max}$ = 10.5 GHz with $MoS_2$ integrated on flexible substrates [38]. Another interesting TMD nanosheet is black phosphorus (BP) with hole and electron mobilities exceeding 1000 $cm^2/Vs$ [40]. BP RF devices were first reported by H. Wang et al. in 2014 with $f_T/f_{max}$ = 12/20 GHz for $L_G$ = 300 nm and $I_{ON}/I_{OFF}$ ~ 2000 [41]. $WSe_2$ is also gaining interest with p-type operation and mobility in the range of ~250 $cm^2/Vs$ [42], but RF performance has not been yet reported.

### 2.1.2 Nanotube RF Transistors

If the nanosheet is rolled into a nanotube, the electronic properties can become more favorable. For example, rolling graphene into carbon nanotubes (CNTs) induces an electronic bandgap, but the bandgap energy is ultra-sensitive to CNT diameter [43]. Just fractions of Angstroms can be the difference between a metallic and semiconducting CNT. For this reason, parasitic metallic CNT channels reduce the theoretical device performance predicted by an all-semiconducting CNT transistor. The state-of-the-art performance of CNTs is similar to graphene—high $f_T$ but low $f_{max}$ which is mainly limited by the high leakage in the off-state leading to lower output resistance.

CNTs, however, may be more promising than nanosheets because the metallic CNTs can be removed. Highly cited techniques for obtaining high-performance all-semiconducting CNTs include selective chemistry, selective etching, selective destruction, electrophoretic separation, chromatography, ultracentrifugation, and selective growth—all of which are reviewed adequately in [44].

Just as challenging is aligning them in parallel arrays for higher current and high intrinsic capacitance to suppress parasitic components and improve input-output matching for RF applications. CNTs can be catalytically grown in dense arrays on quartz substrate, and the metallic CNTs are destroyed by applying a bias to cause electrical breakdown; the semiconducting CNTs survive the breakdown process due to their finite bandgap. Rogers et al. in 2007 demonstrated high-performance logic transistors using this technique with state-of-the-art $I_{ON}/I_{OFF} \sim 10^4$, but the RF performance was not included [45]. The only significant reports of high-speed CNTs have reached near or above 100 GHz, but the $f_{max}$ is limited to due to the unoptimized alignment and presence of metallic CNTs [46-48]. Recently, a report of $f_T/f_{max} > 70$ GHz was reported using high-density polyfluorene-sorted semiconducting carbon nanotubes [49]. However, largely, most CNT devices reporting high-speed have an average $I_{ON}/I_{OFF}$ around 1-100—far below modern day devices, but have an advantage of aligning them on virtually any substrate.

### 2.1.3 Bottom-Up Vertical NW RF Transistors

Bottom-up III-V NWs are typically grown in a metal-catalyzed VLS mechanism as illustrated in Figure 5. The growth process is categorized into three phases—metal alloying, crystal nucleation, and axial growth. The process begins by depositing a metal catalyst to initially form a liquid alloy phase with the substrate; then a vapor phase at high temperature; the resultant alloy possesses a relatively lower freezing temperature; the continuing vapor phase prefers to settle in the liquid alloy until it becomes supersaturated; the result is solid, single-crystal semiconductor growth propagating away from the substrate-droplet interface in the thermodynamically favorable direction [3]. The (111) and (111)B facets have been found to have the lowest surface free energy for group IV elemental and III-V compound semiconductors, respectively [50, 51]. The preferred NW growth directions are <111> for diamond IV NWs [3], <111>B for zinc-blende (ZB) III-V NWs [52, 53] and <0001> for wurtzite (WZ) III-V NWs [54-57]. Figure 5 illustrates VLS NW growth of vertical silicon NWs on (111) silicon substrate using a gold catalyst forming a Au-Si liquid alloy.

Because the (111)B crystal facet has the lowest surface free energy, <111>B vertical III-V NWs are readily available if grown on (111)B substrates [52]. Vertical III-V NWs require either complicated processes for making vertical transistors or undesirable post-growth alignment techniques for making planar transistors. Tomioka et al. reported the first vertical III-V NW HEMT array topology using $In_xGa_{1-x}As$ based quantum-confined core multi-shell gate-all-around (GAA) NWs on silicon substrate with high $I_{ON}/I_{OFF}$ [58]. Presumably, the vertical configuration is challenging for making RF devices because high-speed performance is rarely reported in this configuration. The

lone report of a high-speed vertical array NW transistor was reported by Lund University researchers demonstrating $f_T/f_{max}$ = 103/155 GHz from n-type InAs NW-MOS transistors on silicon substrate with ~32 nm diameter [59]. Despite the wrap-gate structure, an $I_{ON}/I_{OFF}$ ~ 100 was reported because of the complicated vertical fabrication.

### 2.1.4 Bottom-Up Planar NW RF Transistors

A planar NW array layout is more conducive for high-speed but detaching and aligning vertical NWs in parallel on a foreign substrate has been challenging. In order to make planar NW FETs, many post-growth alignment methods have been developed to align the as-grown vertical III-V NWs in-plane with the substrates such as contact printing [60], field-assisted [61], blown bubble [62], combing [63], sliding [64], Langmuir–Blodgett [65], microfluidics [66, 67] or dielectrophoresis [68, 69]. Aside from the additional processing complexity involved in these alignment processes, none of them have the precise NW positioning capability required for making large-scale ICs. So far, the only reported planar NW array transistor is a n-type InAs NW MOSFET fabricated by aligning randomly spun-on NWs on flexible substrate but with $f_T/f_{max}$ < 2 GHz [70]. RF measurements have also been made on single NW planar FETs comprised of InAs [71], AlGaN/GaN [72] and $SnO_2$ [73]. Growing from top-down patterned Au seeds, VLS planar ZnO NW arrays on R-plane sapphire substrates were achieved [74]; however, due to the non-ideal NW quality, the performance of the FETs made from the ZnO NW arrays is far below what are needed for post-Si ICs. Similar work using ZnO VLS NW arrays on c-plane GaN and GaN on (0001) sapphire was also demonstrated

with more than two crystallographic directions, which makes parallel arrays challenging [75, 76].

Planar VLS NW arrays grown *in-situ* without relying on breaking and randomly spinning NWs on substrates was first reported and patented by Professor Li's research group at UIUC [13]. The planar NW growth mechanism relies on overcoming the thermodynamically-favored forces with one that is kinetically favored. While planar VLS NW growth kinetics remains under investigation, it is clear the wetting of the liquid metal droplet surface forming an alloy with the underlying semiconductor plays an important role. Chen et al. recently investigated planar GaAs NW growth in detail and observed this phenomena with various microscopy inspections [77]. With a (100) SI GaAs substrate, the <111>B planes form a symmetric acute angle with the substrate plane. Therefore, VLS epitaxy of GaAs NWs propagate bi-directionally with equal probability in the parallel [0-11] and [01-1] directions. Uni-directional NW growth is possible with (110) GaAs substrate since the <111>B plane is asymmetric [78]. Figure 6 illustrates planar GaAs NW growth direction for (100) and (110) GaAs substrate orientations.

After the GaAs NWs are grown, the MOCVD growth conditions can be configured for conventional thin-film epitaxy without removing the sample and exposing it to ambient air. Using this technique, undoped planar GaAs NWs can be grown on the SI GaAs substrate and a thin-film n-type $Al_xGa_{1-x}As$ wide bandgap carrier supply layer can be deposited *in-situ* to form arrays of 3D NW-HEMT channels. In this dissertation research, we have demonstrated an $f_{max}$ > 75 GHz with AlGaAs/GaAs planar NW-HEMT

channels which is the highest reported for planar VLS epitaxy and superior to any carbon nanoelectronics reported thus far [79].

### 2.1.5 Selective Area Regrowth NW RF Transistors

A competing technology for high-speed nanoelectronics is selective area regrowth (SAR) of III-V epitaxy to make NW channels. The SAR process allows for growth of nanoscale 3D III-V channels in dense arrays positioned and patterned on a wafer scale by top-down lithography. The key advantage is high-speed performance with bulk-like performance and fabrication. For example, an $f_T/f_{max}$ was recently reported around 200/300 GHz for InGaAs SAR NW arrays. In contrast to planar VLS NWs, however, that SAR is a top-down NW process which is subject to aggressive lithographic scaling as with conventional top-down devices. Regardless, the SAR process is certainly promising as a high-speed logic solution to replace silicon.

### 2.1.6 Summary of RF Nanoelectronics

Figure 7 plots the RF figure of merit, $f_{max}$, as a function of inverted gate length. A complete set of tables can be found in Appendix A. It should be noted that $f_{max}$ is a strong function of $f_T$ and also dependent on gate resistance. The results indicate top-down patterning of NWs is still a viable technology for high-speed operation—especially top-down patterning and growing by SAR. Among the bottom-up NW technologies, InAs vertical NW arrays have great potential if vertical transistor fabrication has a

manufacturable path forward. Compatible with planar processing, planar array GaAs NWs reported in the following chapters have the highest $f_{max}$ among VLS NWs and even surpass 2D and nanotube electronics.

## 2.2 High-Power NW Transistors

As mentioned in Chapter 1, NW channels with wrap-gate topology can be especially useful in WBG devices to deplete the gated channel to form a normally-off transistor with high breakdown voltage. Figure 8 illustrates a potential energy barrier forms from interface effects in the ungated regions. Under the gate, additional depletion from the energy barrier is introduced by the gate metal work function. The result is a high-breakdown MOSFET obtained at a desirable 0-V gate bias. Without a wrap-gate structure, a negative gate bias is required to deplete the channel of carriers to obtain high breakdown which leads to off-state power dissipation. While NWs appear beneficial for power electronics, device demonstrations are just recently emerging. Under this research, the first normally-off $Ga_2O_3$ NW-MOSFET was fabricated and characterized.

### 2.2.1 Normally-Off GaN NW FETs

AlGaN/GaN HEMTs have been utilized to obtain low on-resistance in the ungated regions due to a normally-on 2DEG. However, in the gated region, the AlGaN is etched away to remove the 2DEG. Additional electrostatic control is gained by forming NW channels using chlorine-based dry etching. Im et al. reported normally-off GaN

NW-HEMT and NW-MOSFET devices with high dc performance by scaling the width of the NW channels [12]. In this case, 60-80 nm wide fins were sufficient to deplete the gated channel. A $V_{BK}$ up to ~250 V was obtained for a GaN NW-MOSFET. The MOSFETs are junctionless (JL), meaning the entire device is built on the n-doped GaN. The authors suggest a superior SS ~ 68 mV/dec was obtained in the JL GaN NW-MOSFET because the conduction mechanism is in the volume of the bulk channel versus the surface-channel mechanism in the NW-HEMT. This may suggest JL type NW-MOSFETs may be more immune to surface traps. Lu et al. also reported a tri-gate GaN-NW-MOSFET with SS ~ 86 mV/dec and $V_{BK}$ ~ 585 V [80]. Instead of etching GaN NWs in-plane with the substrate, vertical NWs can be configured as well with added fabrication complexity. Yu et al. demonstrated enhancement-mode vertical NW MOSFETs with SS ~ 68 mV/dec and 140 $V_{BK}$ [81].

To summarize, GaN-based NW-MOSFETs have demonstrated very good device performance with high $V_{BK}$, low $SS$ and normally-off operation. These trends provide motivation to continue research of NW-based power electronics in WBG semiconductors such as $Ga_2O_3$. We report in Chapter 6 the first planar and NW-based $Ga_2O_3$ MOSFETs with record performance.

## 2.3 Figures

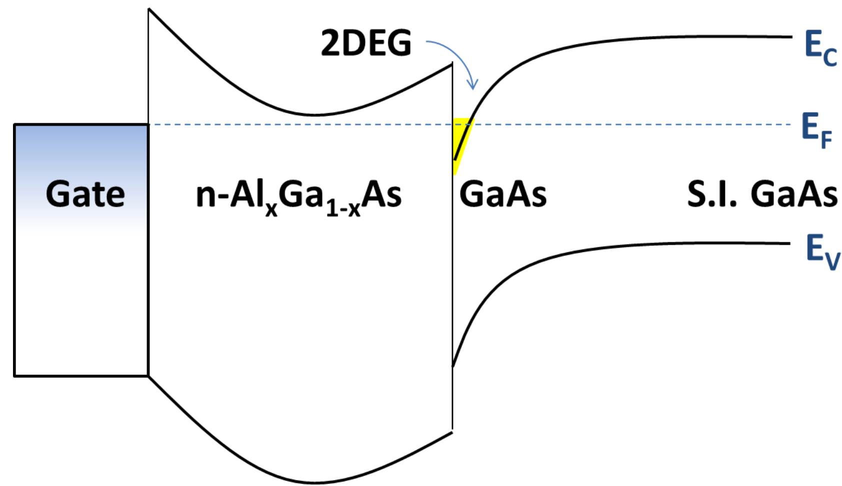


**Figure 4**: Energy band diagram schematic of Schottky gate n-AlGaAs/GaAs HEMT with 2DEG formation at equilibrium.

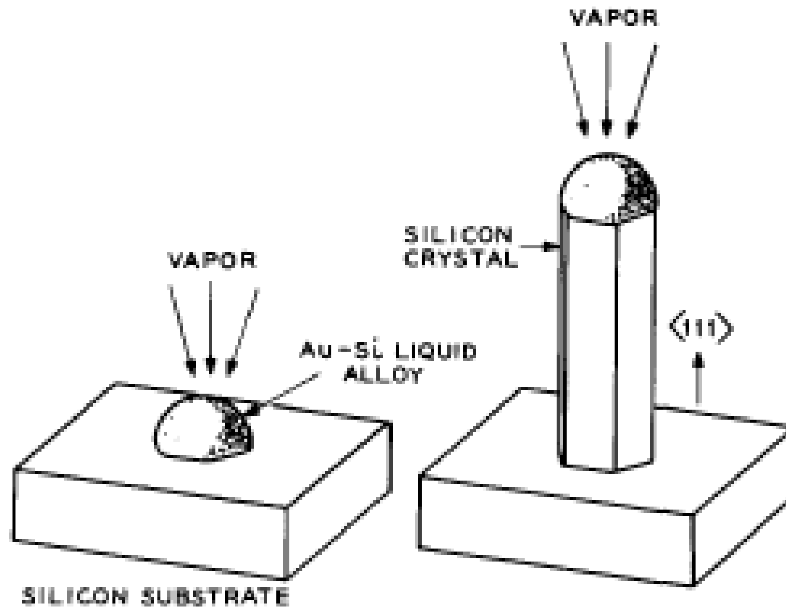


**Figure 5**: VLS growth of a silicon NW propagating vertically on (111) silicon substrate. The catalyst is gold and forms a liquid gold-silicon liquid alloy to promote growth. (Reprinted from [3], with the permission of AIP Publishing.)

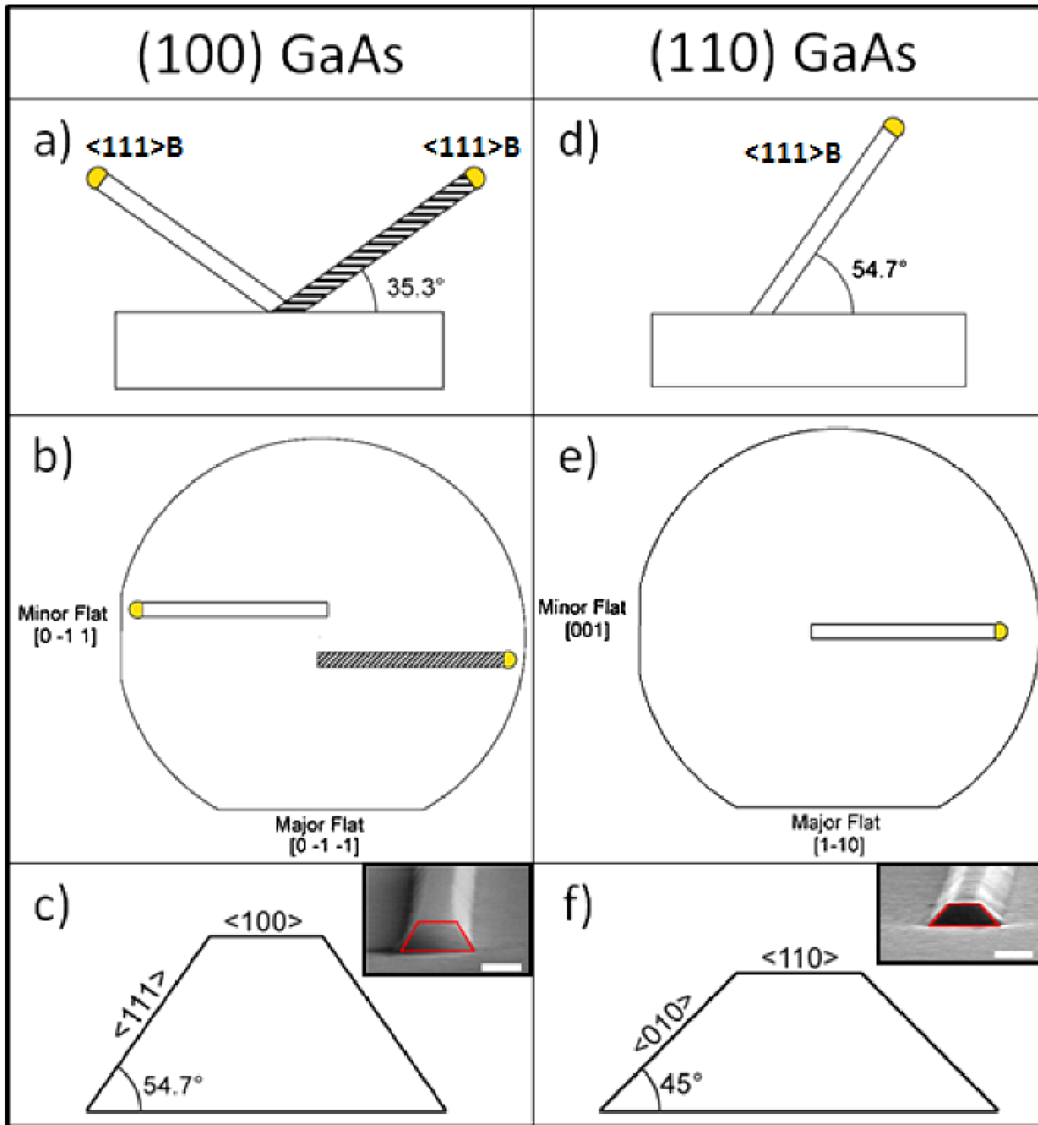


**Figure 6**: Growth properties of GaAs NWs on (left) (100) GaAs substrate and (right) (110) GaAs. The top row illustrates the thermodynamically favored VLS out-of-plane growth. The bottom row illustrates the shape of the GaAs NW when it grows via kinetically favored planar VLS growth (reprinted with permission from ref [82] ©Copyright (2013) Institute of Physics).

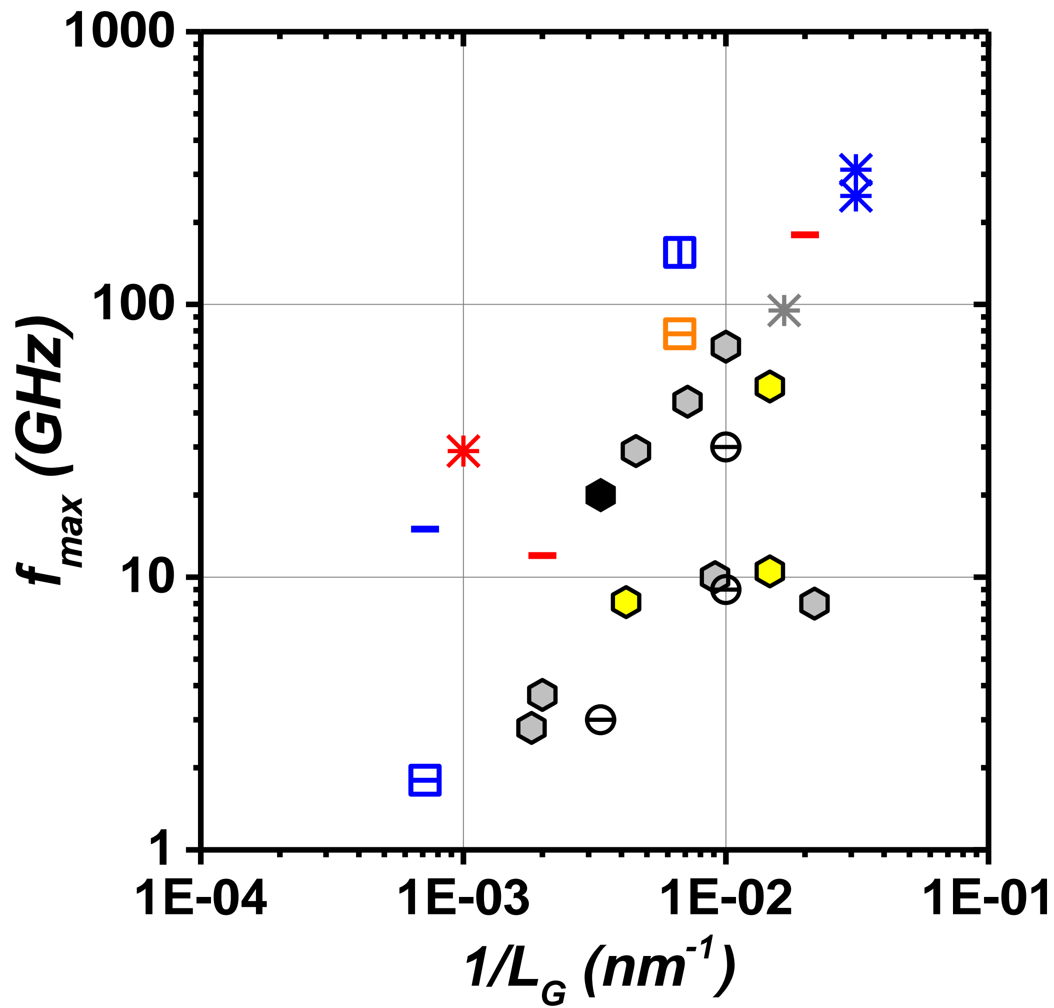


**Figure 7**: $f_{max}$ vs. $1/L_G$ benchmarking for various nanotechnology RF transistors.

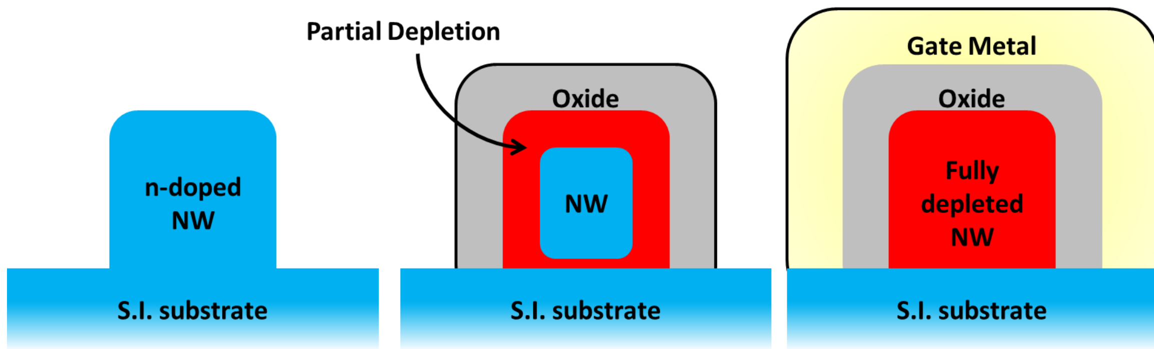


**Figure 8**: (left) n-type NW channel on S.I. substrate with ideal interfaces (no depletion); (center) partial depletion of the NW induced by interface traps and substrate depletion; (right) addition of metal work function potential causing fully depleted NW core.

# 3. BOTTOM-UP NW-ARRAY AlGaAs/GaAs HEMT[1]

This chapter presents details of the growth, fabrication and dc characterization of a NW-HEMT device grown on a SI (100) GaAs substrate (1.5 x 1.5 $cm^2$) with dense parallel arrays of 3D AlGaAs/GaAs core/shell NWs. This is the first nanoelectronic device reported with parallel arrays of NWs based on a heterojunction and shows superior static electrical performance relative to other vertical or dispersed broken vertical NWs on any substrate.

## 3.1 Growth of AlGaAs/GaAs NW HEMTs

The growth of GaAs NWs was accomplished on a cleaved 1.5 x 1.5 $cm^2$ (100) SI GaAs substrate piece supplied by AXT, Inc. in an Aixtron 200/4 metal-organic chemical vapor deposition system (MOCVD). Before NW growth, an array of Au nanodots is patterned by electron beam lithography (EBL) using A6 PMMA resist and wet-developed with MIBK:IPA solution. The volume of the Au nanodots determines the approximate size of the trapezoidal GaAs NW. For the sample in this study, the Au was deposited by electron beam metal evaporation with a thickness of 30 nm and nominal diameter of 100 nm and forming a disk-like shape with 300 nm center-center pitch. The Au nanodots become a liquid alloy spherical colloid during NW growth which determines the cross-

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[1] The content in this chapter is adapted with permission from X. Miao, K. Chabak, C. Zhang, P. K. Mohseni, D. Walker Jr, and X. Li, "High-speed planar GaAs nanowire arrays with $f_{max}$ > 75 GHz by wafer-scale bottom-up growth," *Nano Letters,* vol. 15, pp. 2780-2786, 2014 [79]. Copyright (2015) American Chemical Society

section size of the GaAs NW. For example, the NW width is approximately equal to the diameter of the liquid Au colloid. An SEM of an optimized e-beam lithography process with ~170 nm (target 150 nm) diameter Au dots separated by ~130 nm (target 150 nm) is shown in Figure 9.

Following metal liftoff, a stringent cleaning process of repeating 10 min soaks in PG remover solvent heated to 100 °C was carried out before loading the sample in an Aixtron 200/4 MOCVD reactor. Trimethyl-gallium (TMGa), trimethyl-aluminum (TMAl), $AsH_3$ and $Si_2H_6$ were used as the precursors for Ga, Al, As and Si. Oxide desorption was carried out at 625 °C for 10 min with $AsH_3$ overpressure. The reactor pressure and temperature were then brought to 950 mbar and 450 °C for VLS NW growth. Constant flows of 10-sccm TMGa ($1.16 \times 10^{-4}$ mol/min) and 10-sccm $AsH_3$ ($4.46 \times 10^{-4}$ mol/min) were used in the 200-sec VLS GaAs NW growth. In the NW growth, reactor temperature was initially kept at 450 °C for 20 sec, then dropped linearly to 430 °C in 60 sec and maintained at 430 °C for another 120 sec. With such two-temperature-step VLS growth method, planar GaAs NW arrays with ~100% yield and high crystal quality were achieved.

After the VLS NW growth, the reactor pressure was adjusted to 100 mbar, and the reactor temperature was elevated for epitaxial thin film growth. Approximately 3 nm undoped $Al_{0.33}Ga_{0.67}As$ spacer was grown at 500 °C to stabilize the surface atoms of GaAs NWs and preserve the NWs' original 3D morphology from the following high temperature growth. The 50 nm Si-doped ($3 \times 10^{18}$ $cm^{-3}$) $Al_{0.33}Ga_{0.67}As$ barrier layer and 50 nm $n^+$ ($5 \times 10^{18}$ $cm^{-3}$) GaAs ohmic contact layer were grown at 680 °C for high doping efficiency. This process is illustrated in Figure 10.

As illustrated in Figure 11(a), the operation of a planar NW array-based HEMT relies on the gate's modulation of the two-dimensional electron gas (2DEG) formed at the hetero-interfaces between the AlGaAs barrier and the GaAs NW sidewall and top facets [14]. Therefore, a conformal $Al_{0.33}Ga_{0.67}As$ barrier wrapping over the NWs is critical for good device performance. High background $H_2$ flow was adopted during the barrier growth, which effectively reduced the $Al_{0.33}Ga_{0.67}As$ growth rate and promoted a better barrier coating. Figure 11(b) shows the cross-section of the planar NW heterostructure with two identical GaAs NWs sharing the $Al_{0.33}Ga_{0.67}As$ barrier. Since the growth substrate is semi-insulating, no conduction occurs at the hetero-interfaces between the $Al_{0.33}Ga_{0.67}As$ and the GaAs substrate. This was confirmed by characterizing a control device with no NW in the channel.

## 3.2 Wafer-Scale NW HEMTs in Dense Lateral Arrays

Figure 11(c) shows a tilt-view scanning electron microscope (SEM) image of a representative planar GaAs NW array with 100% planar NW yield. The planar GaAs NWs grow bi-directionally in the anti-parallel [0-11] and [01-1] directions, with respective lengths of ~22 and 28 $\mu$m for the 140-second growth. The origin of the difference in growth rate for the two presumably crystallographically equivalent directions is under further study. Because of the bi-directionality, the grown NWs are no longer equally spaced; wherever there are missing NWs in the array propagating to one side, they can be surely found on the other side. The insets of Figure 11(c), from the left to the right, show the patterned Au seeds, the dividing line between the oppositely

propagated NWs and the near-tip portions of the [01-1] planar NWs. The tiny out-of-plane GaAs whiskers at the dividing line are originated from tiny Au particles split from the patterned Au seeds.

Figure 11(d) is a top-view SEM image of 4 x 6 planar GaAs NW arrays illustrating wafer-scale growth capability. The probabilities of planar GaAs NWs grow in the [0-11] and [01-1] directions are about equal because the [0-11] and [01-1] directions are crystallographically equivalent [82]. The tilt-view SEM image of a cleaved planar GaAs NW array in Figure 11(e) shows that the planar GaAs NWs grown from the patterned seeds have perfectly uniform trapezoidal cross-sections.

Figure 12(a) shows a low-magnification TEM image of a planar GaAs NW removed from the as-grown substrate via FIB. The Au seed particle is clearly visible at the tip of the NW. Prior to TEM lamella preparation, a protective $Al_2O_3$ layer of approximately 30 nm thickness was conformably deposited by atomic layer deposition (ALD) to protect the NW from ion-beam induced damage, followed by in-situ Pt layer deposition. Figure 12(b)-(d) show HR-TEM images of the Au/GaAs NW interface, the substrate, and the NW body, respectively, along locations marked in Figure 12(a). NW growth persists along the equivalent <110> directions of the cubic, zinc-blende crystal. Remarkably, the NW body is entirely free of twin-plane defects and stacking faults. The NW/substrate interface exhibits perfectly atomic lattice registry. As anticipated from a homoepitaxial system, no interfacial dislocations are found. Contrast variation at the NW/substrate interface is simply due to thickness differences, whereas other local contrast differences are attributed to milling artifacts arising from ion-beam exposure. The identical correlation of inverse-space domain symmetry, as shown by the FFT

patterns associated with the NW tip, substrate, and NW body (insets of Figure 12(b)-(d), respectively), indicates monolithic and single-crystalline epitaxial NW growth.

Figure 13 shows high-resolution transmission electron micrograph (HR-TEM) analysis of a representative planar NW liberated from the as-grown sample reveals a purely zinc-blende NW crystal structure, entirely free of twin-defects and stacking faults, with VLS growth along the <110> direction. The inset is the reduced magnification image that highlights the cross-sectional geometry of the Au nanoparticle relative to the NW and substrate.

## 3.3 NW-HEMT Device Fabrication

The device fabrication is fully compatible with the planar processing. The NWs can be aligned to the mask sets with combinations of EBL and optical lithography. Prior to the MOCVD growth, alignment markers were etched into the SI GaAs (100) substrates using a PlasmaTherm 770 Inductively Coupled Plasma (ICP) etching system with an optically defined pattern using SF-11 PMGI photoresist as the etch mask. The ICP etch settings were $BCl_3/Cl_2/Ar$ (32/8/5 sccm) at 300 W for ~15 sec for an etch depth of ~1 $\mu$m. Au seeds with 100 nm diameter, 300 nm center-to-center separation and 30 nm thickness were formed by EBL, Au evaporation and lift-off processes. After growth of the bi-directional planar NW arrays, the relatively longer [01-1] arrays (~35 $\mu$m) were chosen for device processing. Since the [0-11] and [01-1] planar NWs have the same sizes, crystal quality (defect-free) and NW sidewall and top facets, they have the same electrical properties [14].

The long [01-1] planar NW arrays were sufficiently long to make a two-finger T-gated RF pad layout where both gates share the same NWs. The GaAs NWs have a tapering factor (NW length with respect to parasitic sidewall growth) greater than 1000:1 [14, 83]. Ohmic contacts were deposited using an EBL pattern and metal evaporation and lift-off of Ge/Au/Ni/Au (20/50/30/50 nm). The sample was alloyed at 400 °C for 20 sec in hydrogen ambient in a lab-built annealing system. Next, an optically-defined mesa wet-etch step using $H_2SO_4$:$H_2O_2$:$H_2O$ (1:8:80) for 20 sec was achieved to remove the $n^+$ GaAs cap in the extrinsic region of the devices. The pad metal was deposited using optical lithography, metal evaporation and lift-off of Ti/Au. The next step was EBL of the T-gate which consisted of exposing and developing a tri-layer PMMA/MMA/PMMA resist stack using a JEOL3600 FS EBL at the Air Force Research Laboratory (AFRL). Finally, gate recess etching was done in citric acid: $H_2O_2$ (4:1) for 7 sec and followed by metal evaporation and lift-off of Ti/Pt/Au. The devices were left unpassivated. The complete process flow is illustrated in Figure 14.

A representative fully fabricated device with $L_G$ = 150 nm and 30 planar GaAs NWs spanning across both channels is shown in Figure 15(a). Figure 15(b) is a magnification of the channel region showing all three transistor terminals. It should be noted that NWs in the ungated regions in Figure 15(b) appear merged. This is because the shared thick $n^+$ GaAs cap layer buries the original corrugated NWs, as shown in Figure 11(b). However, the actual number of NWs can be specified in the center of the T-gate where the $n^+$ GaAs cap is wet-etched down to the $Al_{0.33}Ga_{0.67}As$ barrier layer. Figure 15(c) shows the fully fabricated device chip with 115 precisely positioned planar NW array-based HEMTs.

## 3.4 NW-HEMT DC Electrical Characterization

The static current-voltage ($I$-$V$) characteristics two-finger planar NW array-based HEMTs with various T-gate $L_G$ from 150 nm to 300 nm in 50 nm increments were characterized. Many of the results are normalized based on the top and two-sidewall NW periphery under the T-gate ($W_{NW}$ = 75 + 75 + 60 = 210 nm). For example, on the device with $L_G$ = 150 nm, there are 30 NWs spanning across both channels, and the total device width is 12.6 $\mu$m (2 x 30 x 0.21 $\mu$m). Figure 16(a) shows the output $I_{DS}$-$V_{DS}$ performance of a representative NW-HEMT with $L_G$ = 150 nm. The output current voltage ($I$-$V$) performance shows excellent saturation at low-bias where a maximum transconductance ($G_{M,peak}$) is achieved. The transconductance of the device is defined as

$$G_M = \left(\frac{dI_{DS}}{dV_{GS}}\right)_{V_{DS}} \quad \text{(S)} \qquad (6)$$

and shown in Figure 16(b) along with additional studied $L_G$ range. The threshold voltage, $V_{TH}$, was extracted using a tangent line to $I_{DS}$ at the $G_{M,peak}$ gate voltage and extrapolating to $I_{DS}$ = 0. Using this technique, a positive $V_{TH}$ = +0.23 V was extracted for all four $L_G$ indicating enhancement-mode operation and excellent SCE. The excellent SCE can be additionally illustrated in Figure 16(c) by the linear behavior of intrinsic gain given by equation (2). Despite good control of SCE, the $I$-$V$ response in Figure 16(a) indicates some lower output resistance evident by the non-ideal slope in the saturation current region. This effect can be explained by viewing the transfer characteristics in log form in Figure 16(d). In the sub-threshold regime, the subthreshold swing (SS) and drain-induced barrier lowering (DIBL) metrics can be used to quantify the NW-HEMT off-to-on properties as well as the short-channel effects. The SS and DIBL are expressed as

$$SS = \left( \frac{d \log(I_{DS})}{dV_{GS}} \right)_{V_{DS}} \qquad \text{(mV/dec)} \qquad (7)$$

$$DIBL = \left( \frac{dV_{GS}}{dV_{DS}} \right)_{I_{DS}} \qquad \text{(mV/V)} \qquad (8)$$

which both are extracted to be 102 mV/dec and 151 mV/V, respectively. The soft-roll off at $I_{ON}$ is likely attributed to the differences in the barrier thickness of the AlGaAs barrier layer as shown in Figure 11(b). In essence, the gate capacitance from the gate to channel separation changes from side to top facets. The sidewalls have thicker barrier which would shift the threshold voltage more negative; then the top facet dominates at more positive bias. Therefore, the shape of the log($I_{DS}$) curve can be explained as the sidewalls turning on well below the extracted device $V_{TH}$; which then is suppressed near 0 V as the dominant top facet begins to turn on near the extracted Vth. The overall on to off ratio is $I_{ON}/I_{OFF}$ ~ $10^4$ which is comparable to planar devices. Figure 16(d) also illustrates the well-documented forward-bias limitation of Schottky barrier GaAs HEMTs which occurs near $V_{GS}$ = +0.7 V. Future iterations of the NW-HEMT could include a thin gate insulator to reduce gate leakage.

## 3.5 Figures

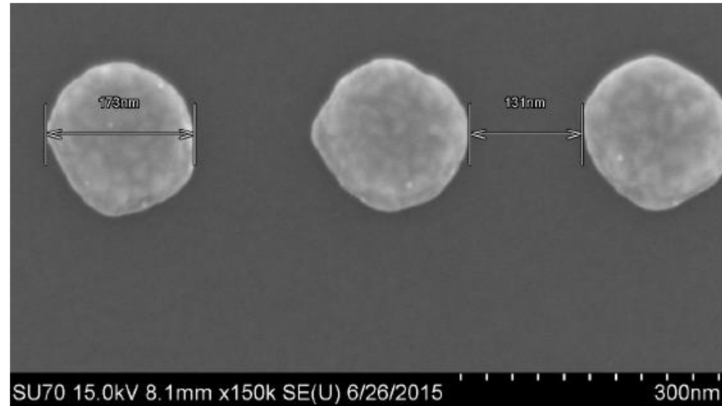



**Figure 9**: SEM micrograph of ~170 nm (target 150 nm) diameter Au dots separated by ~130 nm (target 150 nm) defined electron beam lithography.

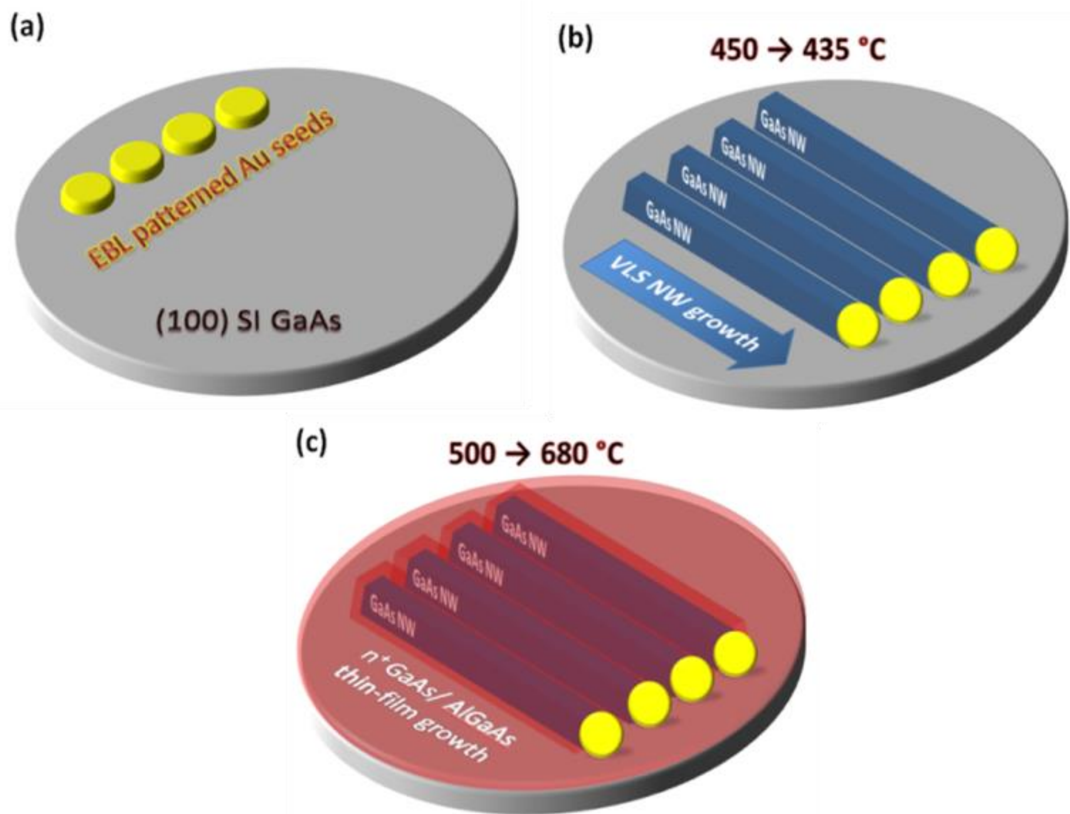



**Figure 10**: (a) EBL-defined Au-seed array deposition; (b) VLS lateral epitaxy of undoped GaAs NWs after eutectic Au-Ga liquid alloy formation of the metal seeds; (c) *in-situ* thin film growth of AlGaAs HEMT barrier at elevated temperature.

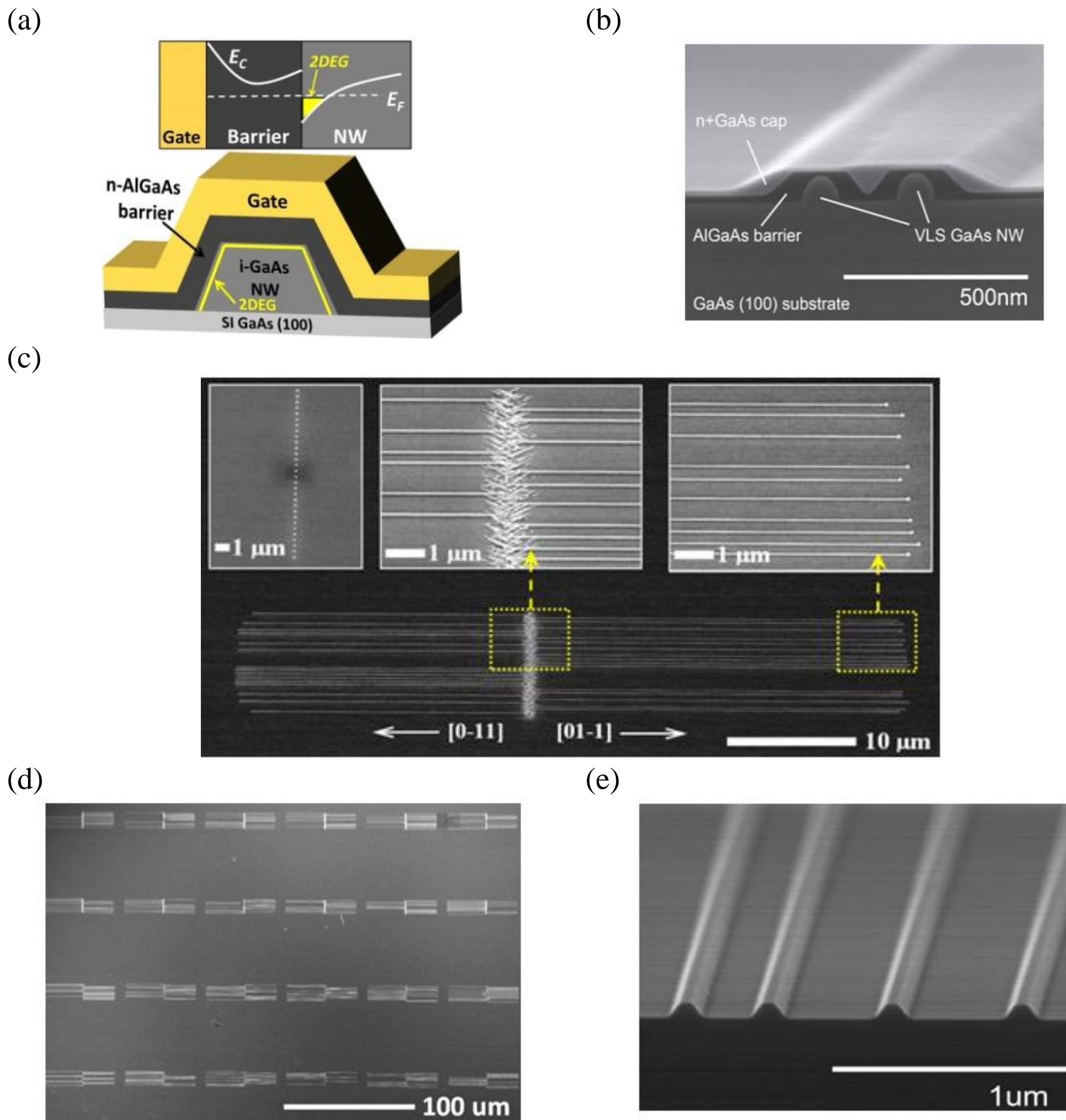



**Figure 11**: (a) Schematic cross-section of a 3D AlGaAs/GaAs NW-HEMT transistor with wrap-gate. The energy band diagram above illustrates the Schottky gate formed by Fermi-level pinning and the 2DEG formation when the device is biased in accumulation. (b) False-colored cross-section SEM of adjacent NW-HEMT channels depicting the conformal AlGaAs barrier and n+GaAs ohmic cap epitaxial layers on the undoped GaAs NW core. (c) Tilt-view SEM image of a representative planar GaAs NW array with 100% planar NW yield. The planar NWs grow bi-directionally in the anti-parallel [0-11] and [01-1] directions. Insets, from the left to the right, show the patterned Au seeds, the dividing line between the oppositely propagated NWs and the near-tip portions of the [01-1] planar NWs. (d) Top-view SEM image of 4 x 6 planar GaAs NW arrays, illustrating the wafer-scale growth capability. (e) Tilt-view SEM image of a cleaved planar GaAs NW array. The planar NWs have perfectly uniform trapezoidal cross-sections.

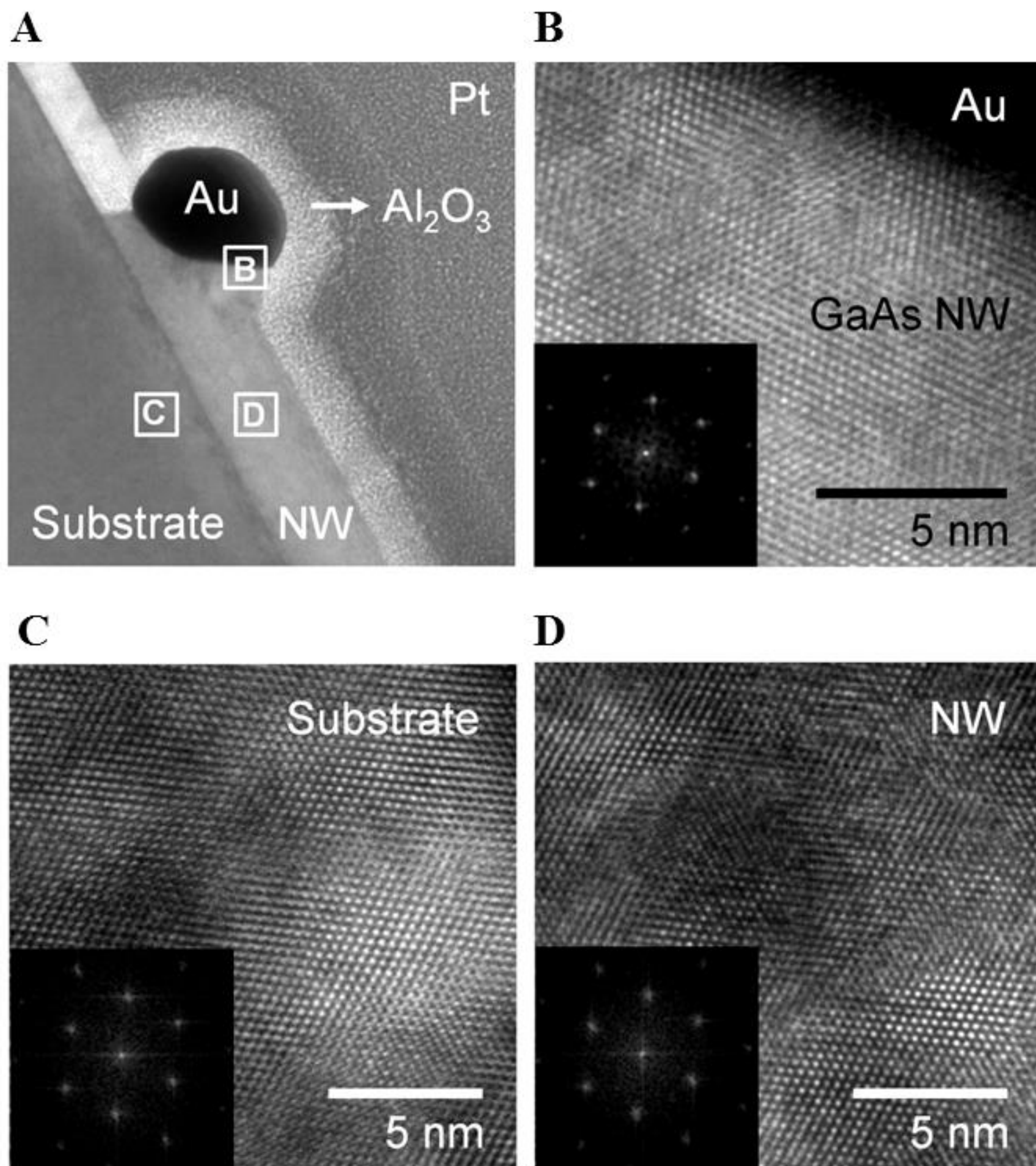



**Figure 12**: TEM characterization of planar NWs. (a) Overview TEM of FIB-prepared foil, showing the Au seed particle and planar NW of interest on the SI GaAs (100) substrate, encapsulated by protective $Al_2O_3$ and Pt layers. The approximate locations of the regions shown in panels (b)-(d) are indicated. (b)-(d) HR-TEM images obtained along the Au/GaAs interfacial plane, substrate, and NW body, respectively, with corresponding FFT patterns shown as their insets.

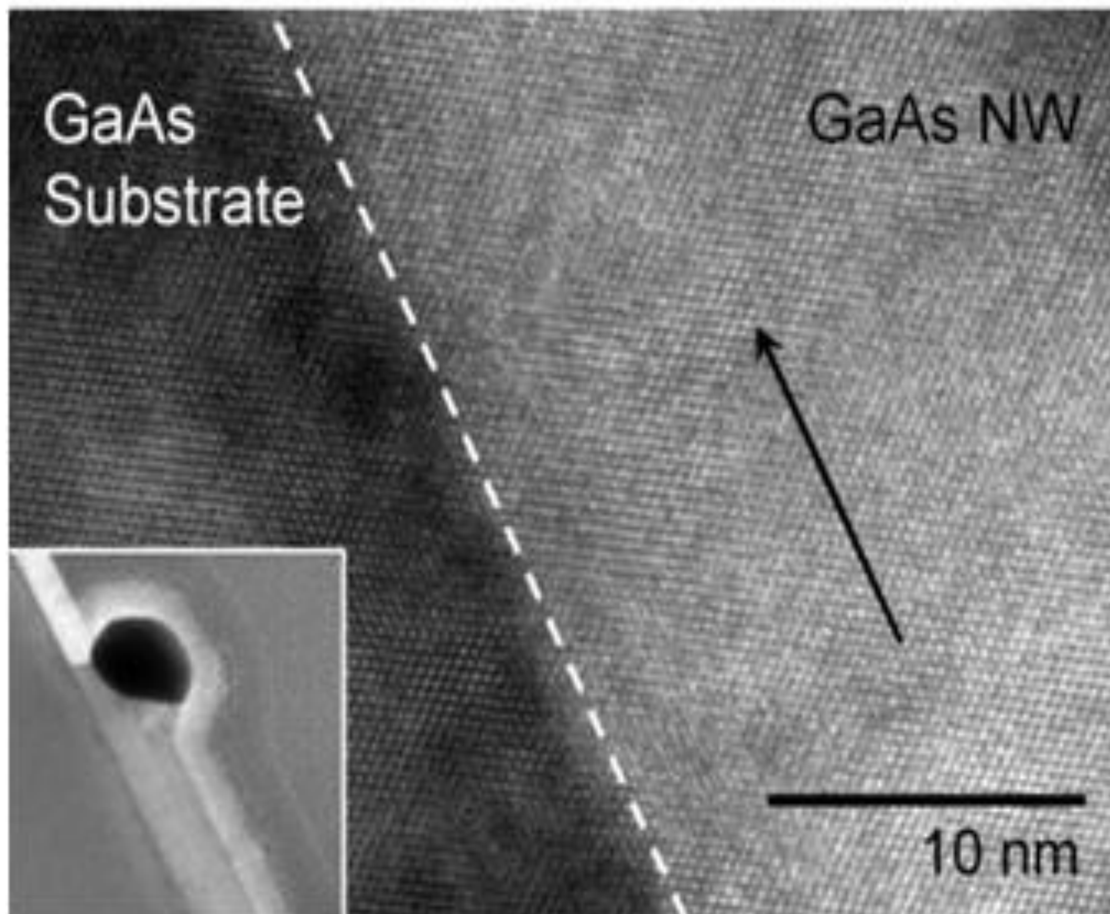
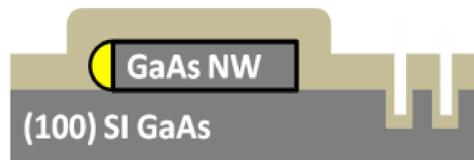



**Figure 13**: HR-TEM image of a representative planar GaAs NW liberated from the as-grown sample (the black arrow indicates the NW growth direction), showing its defect-free and zinc-blende construction. The inset highlights the cross-sectional geometry of the Au nanoparticle relative to the NW and substrate.

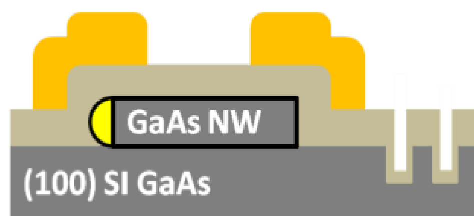
1. Chlorine ICP etch EBL marks

2. Au seed catalyst deposition

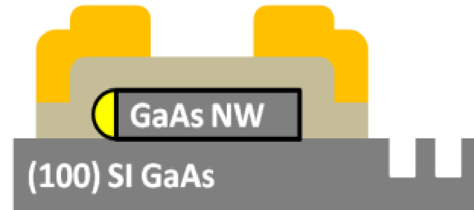
3. MOCVD growth of GaAs NW & epitaxial layers



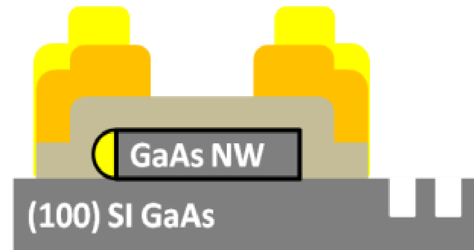

4. Ohmic metal deposition & alloy




5. Acid wet-etch mesa isolation




6. Metal interconnect deposition




7. Gate recess & T-gate deposition

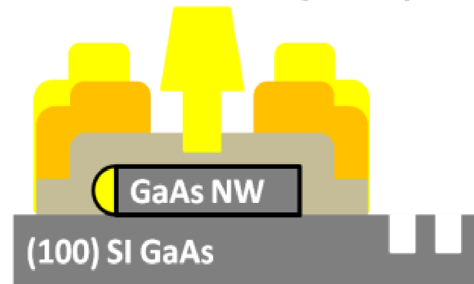



**Figure 14**: Fabrication process flow for a typical NW-HEMT device.

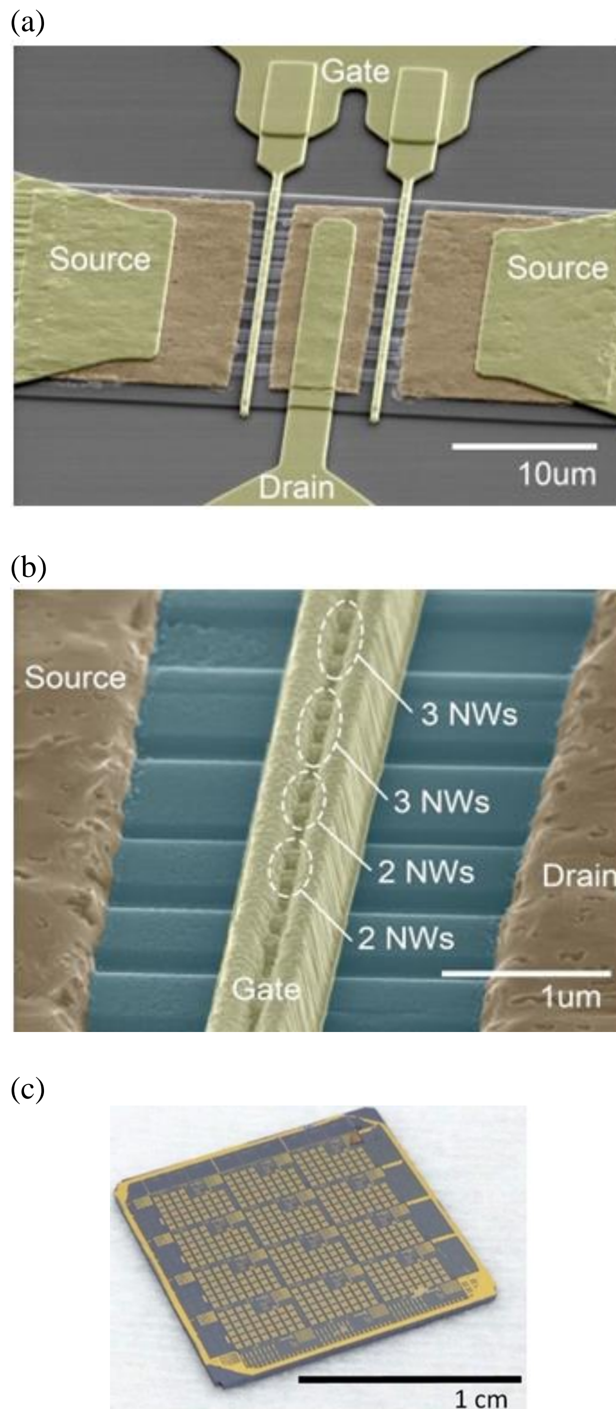



**Figure 15**: (a) Tilt-view false-color SEM image of a representative fully fabricated planar NW array-based HEMT with $L_G$ = 150 nm and 30 planar GaAs NWs spanning across both channels. (b) Magnified, tilt-view false-color SEM image of one channel of a representative fully fabricated planar NW array-based HEMT with $L_G$ = 150 nm and 30 planar GaAs NWs spanning across both channels. (c) Optical image of a fully fabricated 1.5 x 1.5 $cm^2$ device chip with 115 precisely positioned planar NW array-based HEMTs.

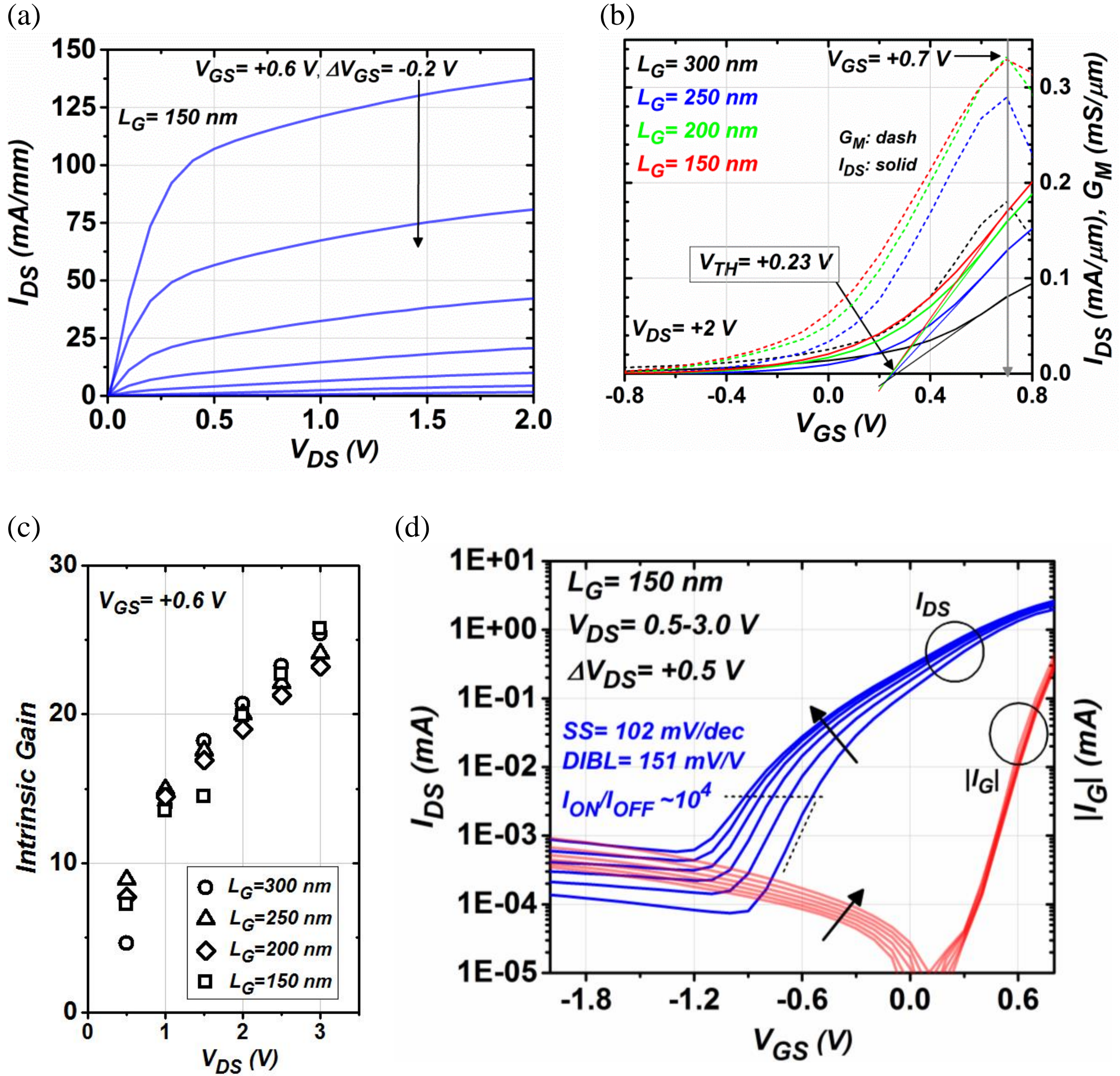



**Figure 16**: (a) Output drain-source current versus drain-source voltage. The top curve indicates $V_{GS}$ = +0.6 V, and the subsequent curves are in increments of -0.2 V. (b) Transfer characteristics of the NW-HEMT for all studied $L_G$. The extracted threshold current is nearly constant over $L_G$ indicating excellent short-channel effects. (c) Intrinsic gain of the NW-HEMT device at $V_{GS}$ = +0.6 V ($G_{M,\text{peak}}$) for various $L_G$ and $V_{DS}$. (d) Log drain-source current (blue) and two-terminal gate diode (red) characteristics as a function of $V_{DS}$ of the NW-HEMT for $L_G$ = 150 nm.

# 4. TRANSFER PRINTING OF GaAs NWS TO ARBITRARY SUBSTRATES

This chapter is presents process development of transferring GaAs-based NWs from the native GaAs substrate onto other substrates. The motivation is to combine inexpensive substrate materials with high-performance III-V semiconductors which are, ultimately, the main drivers for using NWs versus conventional planar epitaxy. By transfer-printing NWs, new heterogeneously integrated devices can be realized. Several approaches are highlighted with their associated challenges and successes for follow-on efforts in this area.

## 4.1 Engineered NW Sacrificial Epitaxy

The planar GaAs NW VLS process has an epitaxial relationship with the GaAs substrate. Therefore, to release the GaAs NWs a sacrificial epitaxial layer must be grown directly beneath a GaAs "cap layer", which is required to facilitate the NW growth. Fortunately, very nice etch selectivity exists in the $Al_xGa_{1-x}As$ compound. For $x > 0.4$, stark contrast in HF-based solutions is observed with binary AlAs etching very quickly while binary GaAs is extremely robust. The growth of GaAs NWs on epitaxial GaAs versus polished GaAs substrate required a design of experiments.

We investigated the quality of GaAs NW assembly on varying thicknesses of $Al_xGa_{1-x}As$/GaAs sacrificial templates grown by MOCVD on (100) GaAs substrates. Table 2 lists the various growths and microscope-based yield inspection results of the GaAs NWs assembled from ~250 nm Au colloids. On imperfect GaAs capping layers,

the NWs grow planar but make peculiar right-angle turns which we suspect is due to surface roughness propagating from growth defects in the epitaxy as depicted in Figure 17. Growing the layers thicker relaxes the strain resulting in increased surface roughness which is correlated with microscope inspection. The optimal results come from the thinnest epitaxial layers where the unrelaxed lattice accommodates strain.

Two main approaches were considered to release GaAs NWs from the GaAs substrate—(1) transfer last (TL) (after complete top-side fabrication) and (2) transfer first (TF). The TL process shields the NWs from chemicals, but the FETs and contacts (especially T-gate) are susceptible to cracking, etc. The TF process slightly etches the NWs, but is most promising for making substrate agnostic NW FETs albeit marginal yield transferring all of the NWs.

## 4.2 Transfer-Last Process Development

The TL process is shown in Figure 18(a). The NWs are self-assembled on the engineered sacrificial epitaxy and front-side FET fabrication is completed. Then, the entire sample is submerged in a two-step wet-etch. Then a box is lithographically patterned around the entire FET to protect it from wet-etching. The first wet-etch is $H_3PO_4$:$H_2O_2$:$H_2O$ (25:3:1) to etch away the GaAs cap layer and reveal the (Al,Ga)As sacrificial layer on the perimeter of the box. The box pattern mask is removed in acetone, and the sample is again lithographically patterned using an interdigitated finger/anchor which physically keeps the FET attached to the substrate while allowing the next wet-etch step to remove the sacrificial layer. The sample is immediately cleaned in $H_2O$ and

submerged in a 2:1 HF:ethanol solution to remove the small amount of AlGaAs sacrificial layer. The ethanol acts as a surfactant to mitigate the “bubbling” which can create a self-seal around the sample preventing HF etching [84]. Finally, a stamp or adhesive was used to pick up the device. Figure 18(b) shows a 4 x 4 array of NW-FET devices on a PDMS stamp after picking up the devices from the GaAs substrate.

Figure 18(c) shows an optical image of transferred devices. An adhesive, a UV-curable polymer, was spun and baked at 110 °C for 20 min on the receiver glass substrate so the adhesion force was enough to release the PDMS stamp after printing the device. The stamp was gently pressed against the adhesive coated glass substrate and slowly lifted back to reduce damage of the NW devices. Each printed device is approximately 400 $\mu$m x 400 $\mu$m. While a few of the devices were transferred neatly, there were several in Figure 18(c) that were damaged. Figure 18(d) shows a close-up optical micrograph of a successfully transferred device without damage; the randomly grown n-GaAs NWs are shown clearly under the contacts.

Before transferring, the devices are built on the sacrificial epitaxy design which proved to be quite leaky compared to the expected current from one or few NWs. The reason is attributed to the larger pad metal in comparison to the contacted NW periphery. In an attempt to reduce the leakage of the sacrificial epitaxy, Figure 19(a) shows a simple experiment with varying UID $Al_xGa_{1-x}As$ (x = 0.7) thickness with constant 100 nm UID GaAs cap with 50 $\mu$m wide transistor devices without NWs. Figure 19(b)-(d) shows the sample variations and transfer *I-V* behavior of each. In the case of NWT-180, there is some leaky n-type conduction which is somewhat suppressed on NWT-181 with an equally thick AlGaAs layer. Interestingly, the conduction type turns to leaky p-type

conduction and is likely due to background carbon doping in the thicker AlGaAs. While the leakage is improved, it is still far above the single $\mu$A range expected from a NW channel. When the AlGaAs is increased to 500 nm (NWT-182), the p-type conduction increases due to the AlGaAs layer becoming less depleted by the top and bottom GaAs layers. The conclusion is that it would be challenging to test a NW-FET before transferring it to another device without an exhaustive optimization study to make the AlGaAs/GaAs epitaxy near semi-insulating. From this limited study, the best scenario occurs when the AlGaAs and GaAs layers are equally thick.

After transferring the devices, the best identified devices did not show transistor *I-V* behavior. It is suspected that the NW/metal interfaces were likely damaged during mechanical peel and transfer. In addition, it is unclear if the UV-adhesive affects device performance. Overall, the TL process is less favorable as it requires time-consuming transistor fabrication before attempting high-risk transferring in addition to adhesives. The process was redesigned to transfer the NWs without adhesives as the first step followed by a low-temperature Pd/Ge/Au ohmic contact process and interconnect metal described in Section 4.3.

## 4.3 Transfer-First Process Development

Section 4.2 highlighted challenges of (1) making devices on leaky sacrificial material and (2) transferring fully fabricated NW-FETs attached to the GaAs membrane without cracking. This motivated investigating a process to transfer the NWs to a foreign substrate first; then proceed with transistor fabrication. For one, this cuts down on

fabrication time as the most difficult process (transfer) is done first. Two, only the NWs are transferred without the membrane, so there is much less material susceptible to cracking.

The TF process is illustrated in Figure 20. Once the NWs are self-assembled on the engineered sacrificial epitaxy, the entire sample is submerged in a two-step wet-etch. The first wet-etch is $H_3PO_4$:$H_2O_2$:$H_2O$ (25:3:1) just long enough to etch away the GaAs cap layer and reveal the $Al_xGa_{1-x}As$ sacrificial layer. Because this etch also etches the GaAs NW, it is prudent that the capping layer is extremely thin. The effects of the brief wet-etch on the NW is shown in Figure 21. Fortunately, Table 2 indicated a thin ~20 nm GaAs cap resulted in the best yield of planar NWs. To reduce surface roughness and potentially allow for pre-transfer testing, an equally thin layer of sacrificial ~20 nm UID $Al_xGa_{1-x}As$ ($x > 0.4$) was grown. After the first etch, the sample is immediately cleaned in $H_2O$ and submerged in diluted HF to remove the thin AlGaAs. It was observed the NWs do not float away; rather, they remain weakly attached; perhaps due to water surface tension adhesion creating a Van der Waal's like bond. An SEM of the NW after the HF etch is shown in Figure 22. Some of the NWs have slight buckled look which is evidence of successful release. After lightly drying the sample, the NWs can be directly pulled off and stamped onto other substrates with low-moderate yield.

The TF process was prototyped on ~250 nm wide $n^+$ GaAs NWs grown from dispersed Au seed colloids on GaAs substrate with 20/20 nm UID GaAs/$Al_xGa_{1-x}As$ ($x = 0.7$). The receiver substrate was chosen as p-type Si with a thermally grown 1 $\mu$m thick oxide. No adhesives were used to allow for a high-temperature annealing. Figure 23 shows two representative GaAs NWs after the TF process. While the PDMS transfer

process was done carefully by hand, it is remarkable the GaAs NWs remain parallel with the Au colloid still attached. The NWs appear to be very uniform and roughly ~200 nm thick after the GaAs cap etch. Occasionally, the NWs were broken but this can be improved by using a mask-aligner for PDMS stamping.

The next step was to overlay an ohmic contact pattern on the randomly transferred NWs on $SiO_2$/Si substrate. Since there were no adhesives involved, the standard 425 °C, 25 sec rapid thermal anneal was attempted with Ge/Au/Ni/Au ohmic contacts. Figure 24(a) shows an SEM inspection of the NW after high-temperature processing. The NW clearly experiences severe tension due to differences in thermal expansion between GaAs and $SiO_2$ and causes breakage near the ohmic contacts. To reduce this effect, a low-temperature Pd/Ge/Au solid diffusion ohmic contact process was implemented and eliminated the NW breakage as shown in Figure 24(b). The Pd/Ge/Au was annealed for 3 hrs in a furnace oven at 175 °C [85]. However, the NW was not conductive after checking with a two-terminal *I-V* test. This could be related to the minimal etching of the NW when the capping layer is removed since a radial doping gradient has been reported to exist in doped NWs where the outer edge is doped higher than the core [86]. Future attempts should utilize NWs grown from densely patterned parallel arrays to increase the total current output.

## 4.4 Figures and Table

**Table 2**: Various Engineered $Al_xGa_{1-x}As$/GaAs Sacrificial Epitaxy and the Observed Quality of Planar GaAs NW Assembly

| *$Al_xGa_{1-x}As$* | | *GaAs cap* | *Planar GaAs NW Quality* |
|---|---|---|---|
| x = 0.7 | 500 nm | 100 nm | Poor |
| x = 0.7 | 500 nm | 50 nm | Marginal |
| x = 0.7 | 100 nm | 100 nm | Poor |
| x = 0.7 | 100 nm | 50 nm | Marginal |
| x = 0.7 | 10 nm | 100 nm | Poor |
| n/a | n/a | substrate | Excellent |
| x = 0.7 | 20 nm | 20 nm | Good |
| x = 0.7 | 20 nm | 10 nm | Good |

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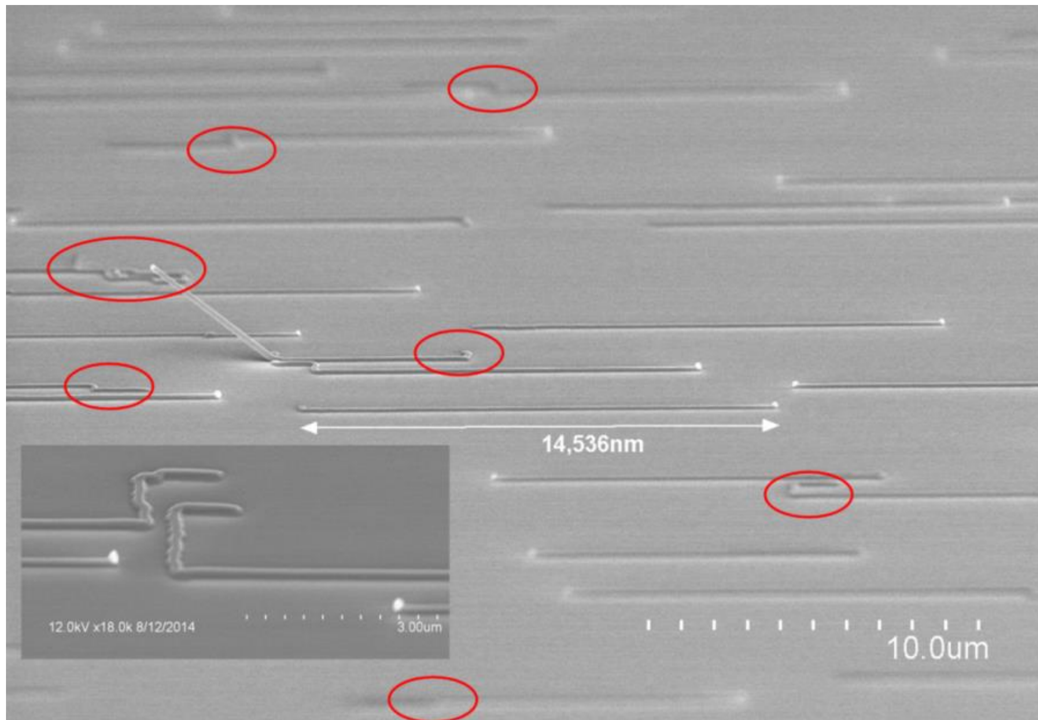
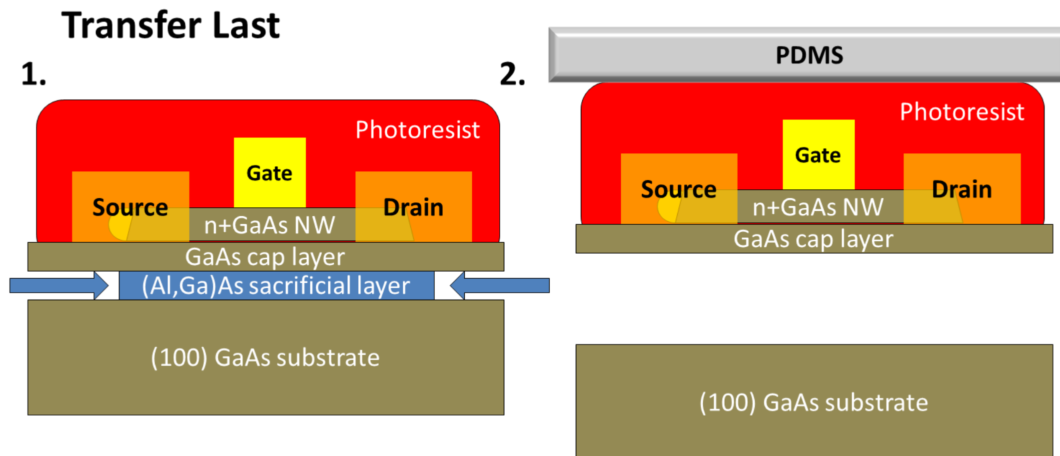
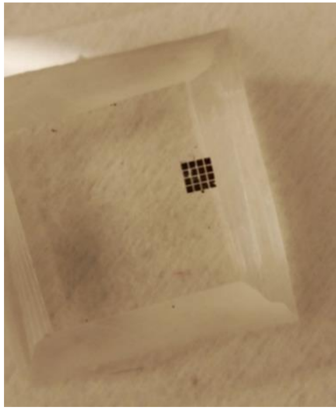



**Figure 17**: SEM of planar of GaAs NWs assembly from ~250 nm Au colloids on 500/100 nm of $Al_xGa_{1-x}As$/GaAs (x = 0.7) engineered epitaxy. Several defects in the NW are shown in red circles. A representative close-in inspection of the turning GaAs NWs is shown in the inset.

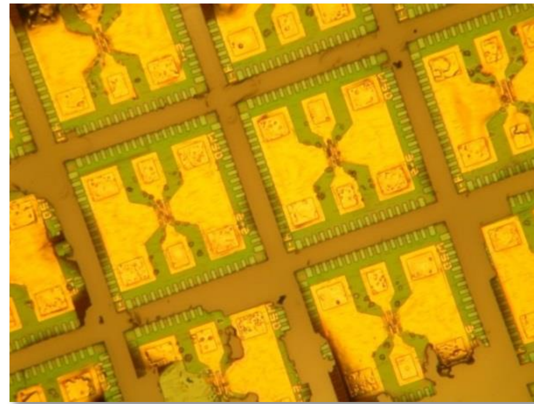
(a)




(b)



(c)



(d)

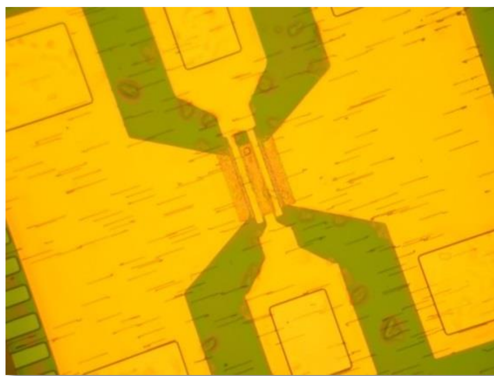


**Figure 18**: (a) Illustration of transfer last process. The NW-FET is fully fabricated on the top side, then covered with photoresist (1). Then, the (Al,Ga)As layer is selectively wet-etched in HF:ethanol (2:1) to release the NW-FET. With the device weakly tethered to the wafer with photoresist, a PDMS stamp is then applied and peeled back to break the resist bond (2). (b) 4 x 4 array of NW-FETs released from the GaAs substrate and picked up using a PDMS stamp. (c) The 4 x 4 array of devices printed and released from the PDMS stamp onto an adhesive-coated glass wafer piece. (d) Zoom-in view of a successfully transferred NW FET device in (b).

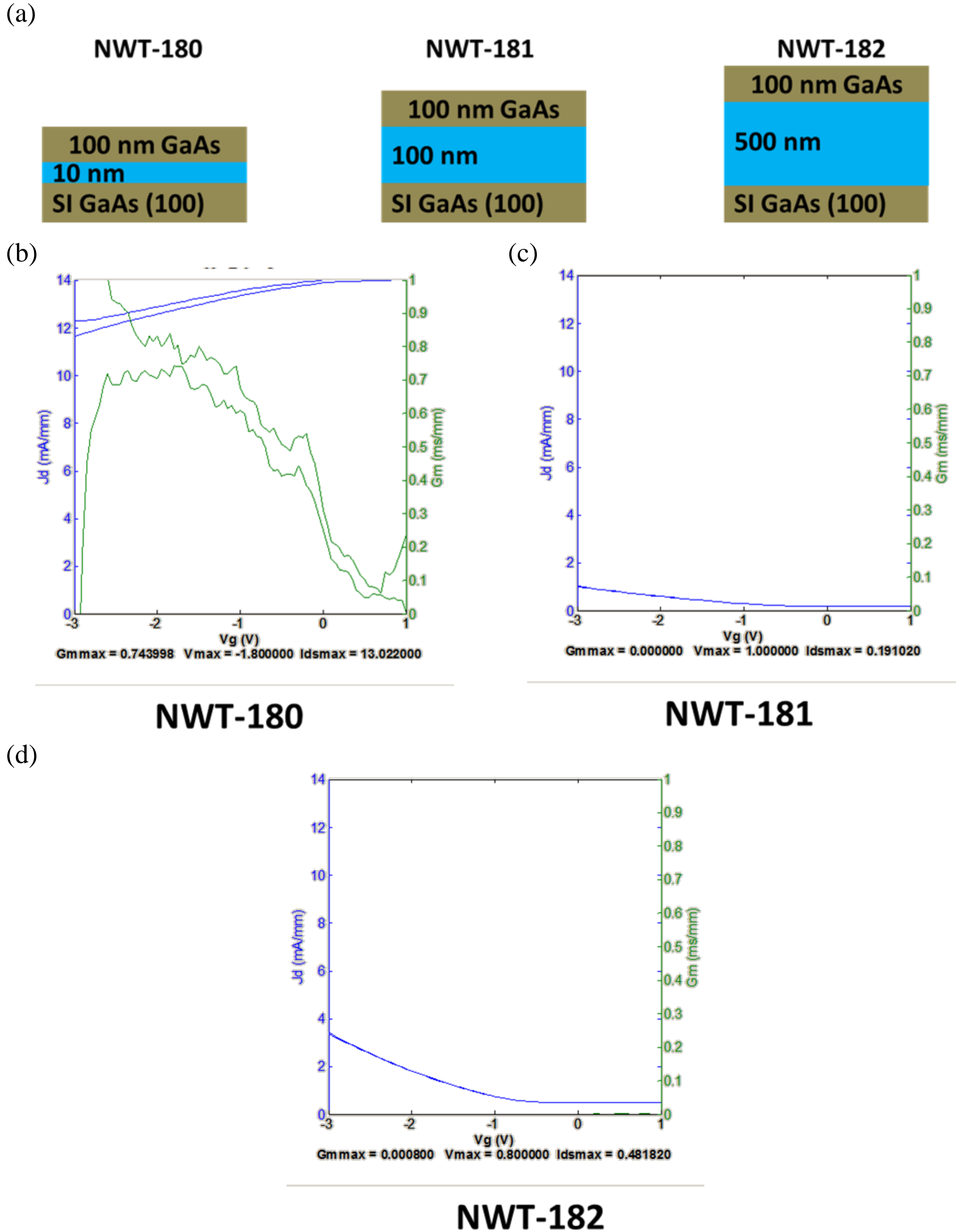



**Figure 19**: (a) Epitaxy structures for parasitic leakage test. Transfer *I-V* behavior of (b) 10 nm, (c) 100 nm and (d) 500 nm UID $Al_xGa_{1-x}As$ (x = 0.7) layers capped with 100 nm UID GaAs. The blue (left), green (right) and black (bottom) labels refer to $I_{DS}$ (mA), $G_M$ (mS) and $V_{GS}$ (V). The scales are 0-14 mA, 0-1 mS and (-3)-(+1) V for $I_{DS}$ (mA), $G_M$ (mS) and $V_{GS}$ (V), respectively. There are two $G_M$ and $I_{DS}$ curves representing forward and reverse sweep.

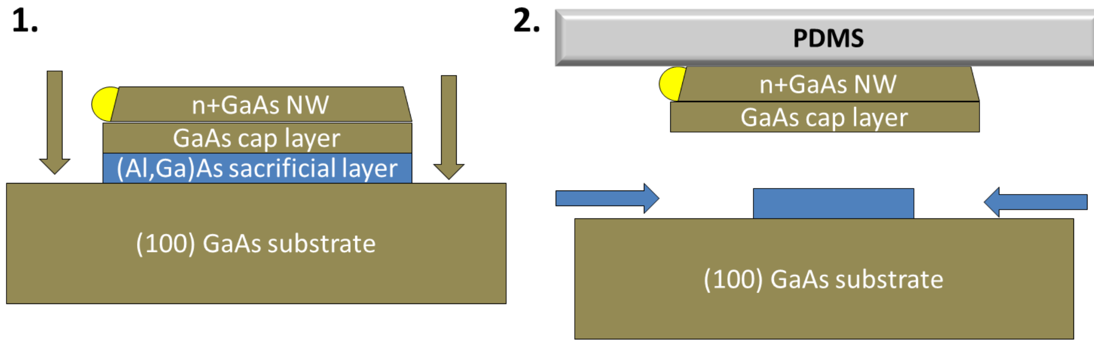



**Figure 20**: Illustration of transfer first process. The NWs are blanket wet-etched without a mask in $H_3PO_4$:$H_2O_2$:$H_2O$ (25:3:1) just long enough to reveal sacrificial layer (1). Then, the $Al_xGa_{1-x}As$ layer is selectively wet-etched in dilute HF to release the NW-FET. The NWs lay weakly bonded on the substrate after the etch, and a PDMS stamp is then applied and peeled back to lift the released NWs (2).

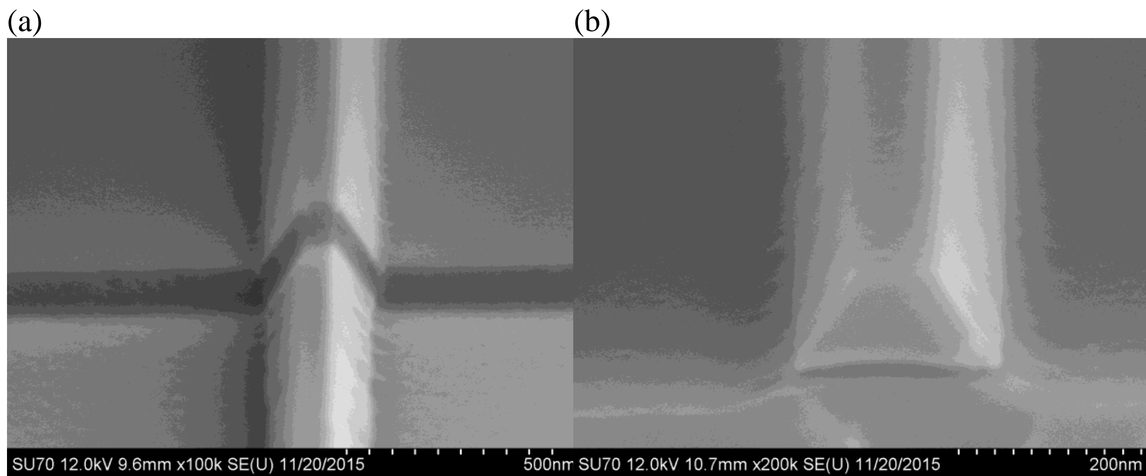



**Figure 21**: (a) SEM image of thin GaAs cap layer etch in $H_3PO_4$:$H_2O_2$:$H_2O$ (25:3:1) with minimal etching of the n-GaAs NW as well. (b) Cross-sectional SEM image of the thin sacrificial AlGaAs layer underneath the n-GaAs NW (darker contrast) exposed from the sides after etching the thin GaAs cap layer away.

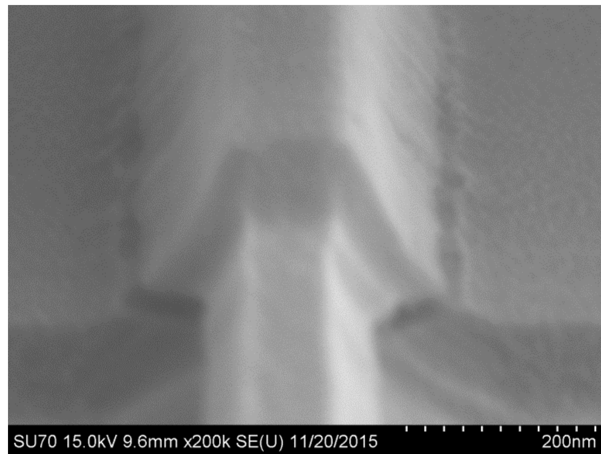



**Figure 22**: (a) SEM image of a NW after both the short $H_3PO_4$:$H_2O_2$:$H_2O$ (25:3:1) etch and 60 min 2:1 Ethanol:HF etch to etch the thin AlGaAs layer. The etched AlGaAs region can be seen by the darker contrast on the sides of the NW. There appears to be some slight roughness from minimal GaAs etching in the long HF release solution.

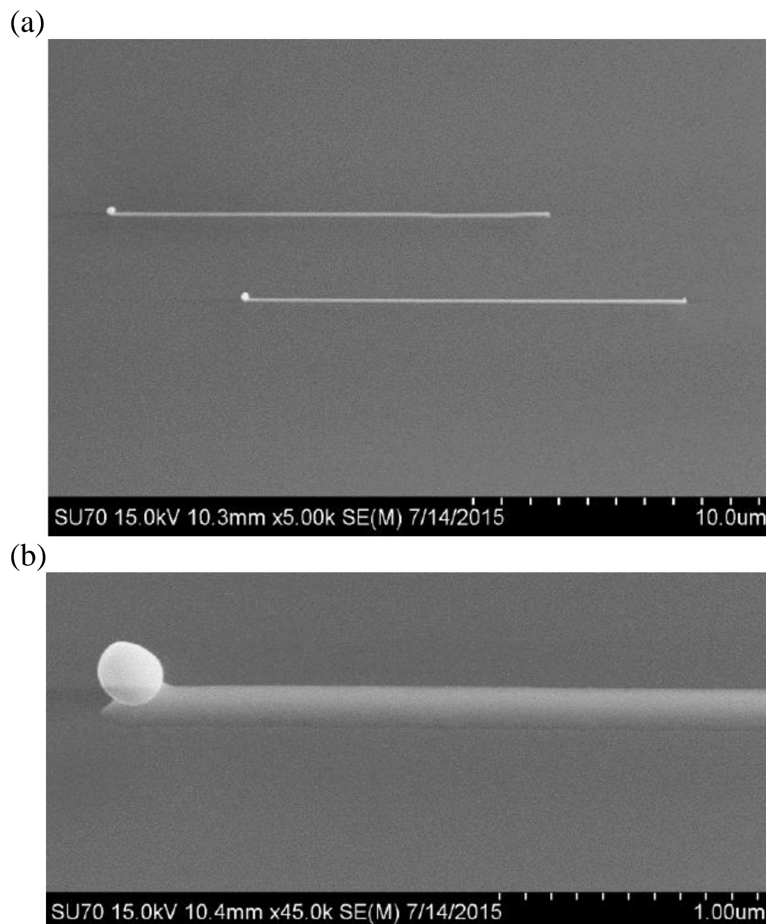



**Figure 23**: (a) Tilted SEM of parallel-aligned GaAs NWs on $SiO_2$/Si substrate. (b) Close-up view on the colloid tip of one of the GaAs NWs.

(a)

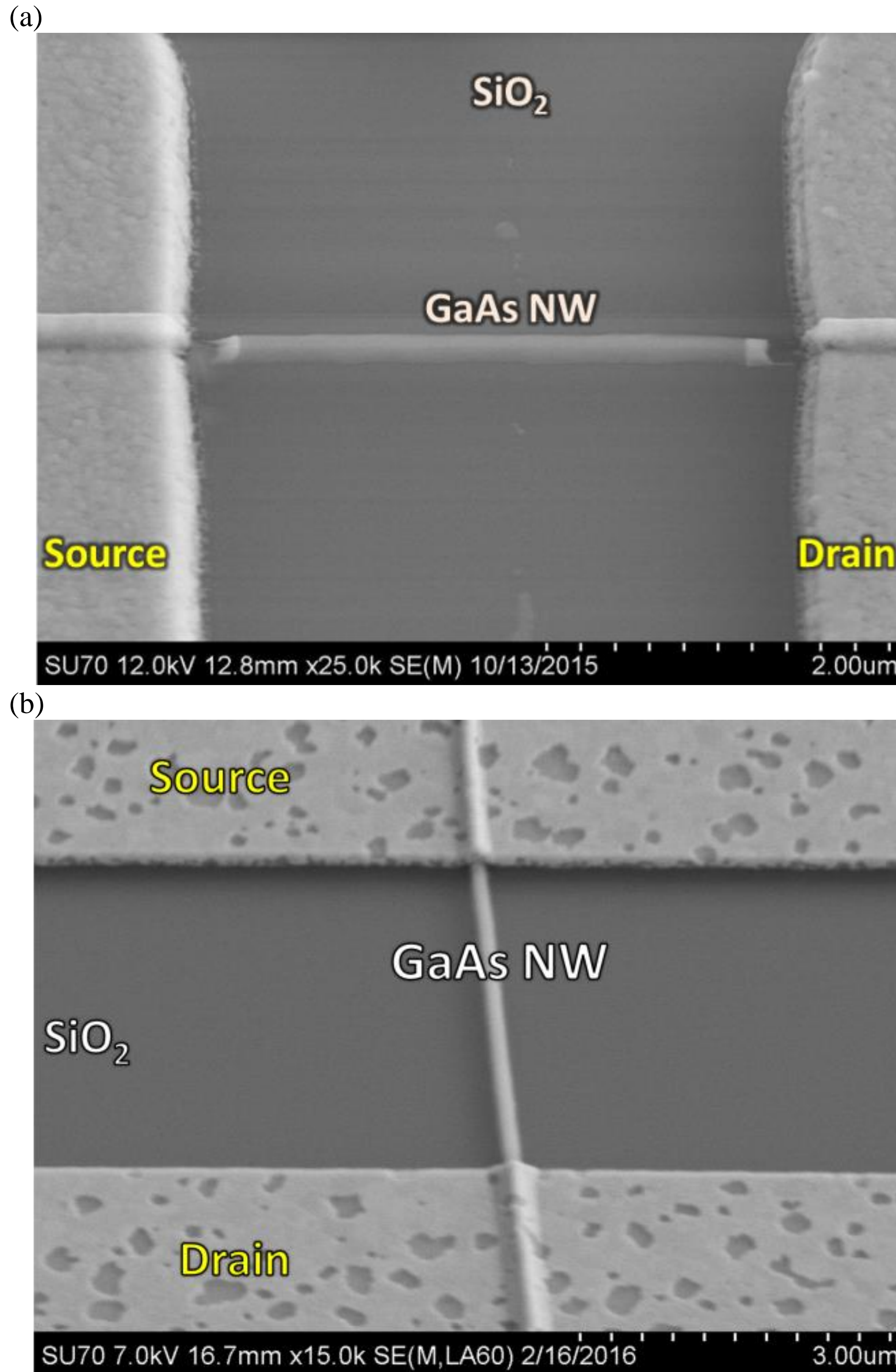



**Figure 24**: (a) Ge/Au/Ni/Au ohmic contacts to n-GaAs NW after rapid thermal anneal for 25 sec at 425 °C resulting in NW damage. (b) Optimized Pd/Ge/Au contact annealed at 175 °C for 3hrs retains NW structural integrity.

# 5. RF CHARACTERIZATION AND MODELING OF AlGaAs/GaAs NW-ARRAY TRANSISTORS[2]

In this chapter, we present an in-depth study of the RF performance of fabricated NW-HEMTs from Section 3.3 and use a conventional small-signal equivalent circuit model (SSM) to investigate the limiting and contributing factors for high $f_{max}$ using planar-array NW-HEMT channels. RF characterization of NW-HEMTs as a function of $L_G$ and bias are discussed in detail [87].

## 5.1 Introduction

III-V NWs for electronic devices are emerging due to their inherent 3D geometry, which can be utilized as a multiple gate, high-mobility channel with enhanced electrostatic gate-channel coupling [88]. Attention has especially been given to NWs grown by metal-catalyzed vapor-liquid-solid (VLS) epitaxy as this eliminates damage from top-down etching. Immediate benefits of III-V NWs, so far, have focused on improved static performance over conventional transistors [14, 24, 58, 59, 89, 90]. Realizing high-speed NW performance requires densely packed arrays of NWs aligned in parallel so that the overall intrinsic gate capacitance ($C_{g,i}$) is large compared to the total parasitic capacitance ($C_{g,p}$) [91]. By doing so, high-speed 3D NW channels with enhanced electrostatics are candidates for future RF nanoelectronics with high maximum

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[2] The content in this chapter is adapted with permission from K. D. Chabak, X. Miao, C. Zhang, D. E. Walker, P. K. Mohseni, and X. Li, "RF performance of planar III–V nanowire-array transistors grown by vapor–liquid–solid epitaxy," *IEEE Electron Device Letters,* vol. 36, pp. 445-447, 2015 [87]. Copyright (2015) IEEE

oscillating frequency ($f_{max}$) [26]. However, the practical challenges of NW assembly have resulted in low $f_{max}$, and the RF behavior of nanoscale channels has been left largely unexplored. For example, the record RF speed for laterally aligned InAs and silicon VLS NWs is 1.8 GHz [24] and 0.34 MHz [92], respectively, while the best carbon nanotube transistor has reached just 30 GHz [47]—all far below their theoretical potential. Major contributing factors for low $f_{max}$ include the fringing fields of the gated regions between NWs which do not conduct in the on-state but still contribute to $C_{g,p}$. One solution is to leave dense arrays of VLS NWs in their preferred out-of-plane growth direction, but this creates high pad capacitance from overlapping transistor terminals [59]. Alternatively, an $f_{max}$ exceeding 300 GHz with 32-nm gate length ($L_G$) has also been achieved with III-V 3D channels aligned in the substrate plane via selective regrowth [93]. In that case, the channel geometry depends on top-down lithography compared to bottom-up NWs grown by VLS method which require patterning only the metal catalyst nanoparticle. Here, we use an SSM to investigate the limiting and contributing factors for high $f_{max}$ using planar-array NW-HEMT channels. RF characterization of NW-HEMTs as a function of $L_G$ and bias are discussed in detail.

## 5.2 Equivalent Circuit Model and RF Setup

The RF performance of a III-V HEMT has been conventionally modeled by a lumped element equivalent circuit model. The lumped elements can be determined by two-port network small-signal scattering (S-) parameters made with a network analyzer equipped and bias tees to configure the transistor in on or off states. Many different

versions of SSMs exist; however, the core of each is based off the gold-standard SSM reported in refs [94, 95]. Figure 25 shows a typical SSM with extrinsic terminal inductances ($L_S$, $L_D$, $L_G$), terminal resistances ($R_S$, $R_D$, $R_G$) and pad layout capacitance ($C_{pg}$,$C_{pd}$). The intrinsic transistor region consists of intrinsic terminal capacitance ($C_{gs}$,$C_{gd}$,$C_{ds}$), current source ($v_{gs} \cdot g_{mi}$ where $g_{mi}$ is the intrinsic transconductance) and output conductance ($g_{ds}$). An added term, $R_i$, is the intrinsic resistance associated with the charging time of the gate capacitance.

The extrinsic pad inductance and capacitance components can be de-embedded by using on-wafer open and short transistor structures to understand the intrinsic device. The intrinsic region of the device physically is the area within the transistor channels containing the electrically isolated mesa. This consists mainly of the ohmic metal, gate and minimal interconnect metal. The open and short structures replace the intrinsic box with nothing (insulating substrate) and metal, respectively. The NW-HEMT transistor and associated open and short layout standards are shown in Figure 26.

For characterizing NW-HEMT RF devices, the expected frequency response is no higher than millimeter range; therefore, a standard short-open-load-thru (SOLT) calibration procedure is sufficient to place the measurement reference plane at the probe tips. The procedure uses short, open, 50 Ω load, and thru structures on an alumina substrate standard provided by Cascade Microtech®. However, the structures in Figure 26 are used to further move the reference plane to the device under test (DUT) intrinsic region. This is done by measuring the S-parameters of the open ($[S]_O$) and short devices ($[S]_S$); then, the S-parameters are transformed to Y- and Z-parameters ($[Y]_S$, $[Y]_O$, $[Z]_S$,

$[Z]_O$). With these parameters, the measured NW-HEMT extrinsic S-parameters ($[S]_E$) can be transformed to intrinsic S-parameters ($[S]_I$) by using the following equations:

$$[S]_{E,S.O} \rightarrow [Y]_{E,S.O} \qquad \text{(S)} \qquad (9)$$

$$[Y_{S-O}] = [Y_S] - [Y_O] \qquad \text{(S)} \qquad (10)$$

$$[Y_{E-O}] = [Y_E] - [Y_O] \qquad \text{(S)} \qquad (11)$$

$$[Y_{S-O}, Y_{E-O}] \rightarrow [Z_{S-O}, Z_{E-O}] \qquad (\Omega) \qquad (12)$$

$$[Z_I] = [Z_{E-O}] - [Z_{S-O}] \qquad (\Omega) \qquad (13)$$

$$[Z_I] = [Z_{E-O}] - [Z_{S-O}] \qquad (\Omega) \qquad (14)$$

$$[Z_I] \rightarrow [S_I] \qquad \text{(UL)} \qquad (15)$$

The RF gains measured are current-gain ($H_{21}$), maximum available gain (MAG) and unilateral gain (U) which are derived from two-port network theory; the corresponding frequencies where gain falls to zero are cutoff frequency ($f_T$), $f_{max}$,MAG and $f_{max}$,U, respectively. The $f_T$ is dependent on material and thickness of the channel and barrier as well as the gate length ($L_G$). When $f_T$ is higher than the measured frequency range, the $H_{21}$ is extrapolated with a -20 dB/dec on a gain versus log frequency plot. The power gains account for resistance drop from input to output and result in more complex expressions. MAG refers to a theoretical condition where the input and output of the two-port transistor are conjugate matched for optimum power while remaining stable. The stability factor, κ, must be greater than 1 to remain unconditionally stable. When $\kappa < 1$, oscillations occur and the device is conditionally stable. The gain in the conditionally stable regime is referred to as Maximum Stable Gain (MSG). Generally, high-frequency transistors are unconditionally stable at low-moderate frequencies and the MSG rolls off

at -3 dB/oct; then, at κ = 1, a “kink” is observed where the transistors enters into an unconditionally stable gain condition where MAG rolls off at approximately -6 dB/oct. However, the MAG roll off must be modeled using an equivalent circuit to precisely understand this behavior. For this reason, U is often used to extract $f_{max}$ since it is a theoretical gain quantity where the feedback is assumed neutralized and free of complications [96]. Typically, U rolls off conveniently at -20 dB/dec for easy $f_{max}$ extraction. However, in many documented cases of high-speed III-V FETs, the U can be noisy as a result of high drain bias making extraction more challenging [29, 30]. The $f_{max}$ is regarded as more relevant for wireless/RF applications because the amplifier is not merely switching on/off, but amplifying incoming signals with a voltage and current gain (hence, their product being a power gain).

## 5.3 NW-HEMT RF Characterization Results

RF performance was characterized with an Agilent E8364B parametric analyzer equipped with bias tees for dc bias. S-parameters for each device were measured at various gate and drain bias in the 0.01-40 GHz range at -27 dBm power. Intrinsic device RF performance is defined as the NW-HEMT with probes and de-embedding performed as outlined in the previous section.

The devices are two-finger AlGaAs/GaAs NW-HEMT devices grown and fabricated on a (100) semi-insulating (SI) GaAs wafer with NW diameter ~160 nm and 300 nm patterned NW center pitch. The number of NWs per device is ~25, each of which spans across both sides of the double channels; and the T-gate $L_G$ varies from 150-

300 nm in 50 nm increments. The T-gates were cross-sectioned in a FEI Dual Focus Ion Beam tool and shown in Figure 27. The devices are the same as fabricated and described in Chapter 2. The NW-HEMT device and layout description are shown in Figure 28.

Representative gain versus frequency RF measurements are shown in Figure 29(a) (left) for $L_G$ = 150 nm and $V_{GS}/V_{DS}$ = +0.6/2.0 V. The $H_{21}$ decreases by -20 dB/dec and falls to 0 dB at $f_T$ = 33 GHz. The MAG and U are both plotted and extracted to $f_{max}$ = 75 GHz using a conventional small-signal circuit model discussed in the next section. As expected, the power gains (MAG, U) were well above $H_{21}$ which is evidence of the excellent electrostatics. In Figure 29(b), the effect of $L_G$ and $V_{DS}$ is shown for a fixed $G_{M,peak}$ gate bias.

Figure 30 and Figure 31 illustrate the effect of de-embedded $f_T$ and $f_{max,\mathrm{UPG}}$ as a function of gate and drain bias for each gate length. The best de-embedded frequency performance, $f_T/f_{max}$ ~ 33/75 GHz, was obtained with $L_G$ = 150 nm measured at $V_{DS}$ = 2 V with 30 NWs spreading along a 20 $\mu$m contact width—a NW density of ~1.5 NWs/$\mu$m. To our knowledge this is the highest reported $f_{max}$ achieved on any nanoscale device with VLS NWs, CNTs, or 2D sheets aligned in-plane with the substrate [24, 34, 46, 47, 97]. The peak $f_T$ occurs at lower drain voltage because it is mostly dependent on gate and channel design and reaches a maximum as soon as the $G_{M,max}$ is achieved which is at low bias in these devices. The tendency for the $f_T$ to degrade slightly with $V_{DS}$ is likely due to the hot-electron effects induced by a higher electric field near the drain region. The peak $f_{max}$ performance shifts slightly toward high $V_{DS}$ because of its higher sensitivity to gate-to-drain capacitance. In addition, $G_M$ from the NW channel remains high once $V_{DS}$ saturates (~ 1 V); therefore, a high $f_T/f_{max}$ ~ 37/67 GHz was measured at $V_{GS}/V_{DS}$ = +0.6/1

V, which is enticing for applications demanding high gain with small power consumption.

## 5.4 NW-HEMT Equivalent Circuit Extraction Procedure

SSM research is an active area with several different versions of models proposed. The main challenge is isolating and extracting each individual term in the circuit. For example, the SSM in Figure 25 has 14 parameters; so, one requires 14+ equations to solve for each of them. The extraction methodology requires simplifying the transistor in depletion and zero-bias mode.

In depletion, the transistor is an open circuit because there is no current flow. In this case, the intrinsic portion of the device is replaced by a depletion capacitance leaving only pad capacitance and inductance. If the circuit is represented by admittance parameters (Y-parameters), the real part contains conductance and the imaginary component represents capacitive ($\sim\omega C$) and weak inductive ($\sim 1 / \omega L$) impedances where $\omega = 2\pi \cdot f$. By taking only the imaginary part and representing the circuit at low-frequency (< 6 GHz), inductance and resistance are negligible and represented in the equivalent circuit in Figure 32. Therefore, using a two-port network S-parameter measurement and converting to Y-parameters, one arrives at four empirical expressions ($Y_{11}$, $Y_{12}$, $Y_{21}$, $Y_{22}$) which can be used to solve for three capacitors—$C_b = C_{b1} = C_{b2} = C_{b3}$ (depletion), $C_{pg}$ (gate pad capacitance), and $C_{pd}$ (drain pad capacitance) shown in equations (16)-(18).

$$\mathrm{Im}(Y_{12}) = -\omega\left(\frac{C_b}{3}\right) \quad \text{(S)} \qquad (16)$$

$$\mathrm{Im}(Y_{11}+Y_{12})=\omega\left(C_{pg}+\frac{C_b}{3}\right) \qquad \text{(S)} \qquad (17)$$

$$\mathrm{Im}(Y_{22}+Y_{12})=\omega\left(C_{pd}+\frac{C_b}{3}\right) \qquad \text{(S)} \qquad (18)$$

Representative measured admittance parameters from 10 MHz to 40 GHz in the form of equations (16) - (18) are shown in Figure 33. These three equations are linear, and the slope corresponds to three variables and three equations. An excellent linear fit was used to calculate and extract $C_b$, $C_{pg}$ and $C_{pd}$. It was found that $C_{pg}$ = $C_{pd}$ = 25 fF which is commensurate with a similar pad layout used in GaN HEMTs [98].

A similar approach is used at zero-bias ($V_{DS}$ = $V_{GS}$ = 0), where the circuit is represented by a T-network of resistance, capacitance, and inductance for each terminal shown in Figure 34. By converting the zero-bias S-parameter measurement to impedance parameters ($Z$-parameters) with de-embedded pad capacitance, equations (19)-(21) can be realized with the real part containing the resistance and the imaginary part contains the capacitive (~1 / $\omega C$) and inductive (~$\omega L$) impedances [99]:

$$Z_{11}=R_g+R_s+j\omega(L_g+L_s)+\frac{\frac{1}{3}R_{ch}}{1+j\omega C_{ds}R_{ch}}+\frac{R_{dy}}{1+j\omega C_g R_{dy}} \qquad (\Omega) \qquad (19)$$

$$Z_{12}=R_s+j\omega L_s+\frac{\frac{1}{2}R_{ch}}{1+j\omega C_{ds}R_{ch}} \qquad (\Omega) \qquad (20)$$

$$Z_{22}=R_d+R_s+j\omega(L_d+L_s)+\frac{R_{ch}}{1+j\omega C_{ds}R_{ch}} \qquad (\Omega) \qquad (21)$$

In many approaches, [$Z$] is multiplied by $\omega$, and each terminal inductance can be extracted from three plots of $\omega$Im[$Z$] versus $\omega^2 L$ where the resistance and capacitance have no influence [100]. However, there is some discrepancy to fitting the inductance

and resistance by linear fit, and it does not accurately capture $C_{ds}$ in the zero-bias condition [99].

An approach defined by Brady et al. [99] uses a convenient non-linear fitting procedure for HEMTs that begins with a best guess parameter, then does polynomial fitting to the frequency dependent Z-parameters. $R_{dy}$ and $R_{ch}$ in equations (19) - (21) refer to the resistance due to the Schottky barrier and drain-source channel, respectively. It should be noted that the two parallel RC networks in the middle of Figure 34 are distributive but are drawn otherwise for simplicity. A summary of the process follows (for details, please refer to [99]):

1. Calculate estimations of the following parameters using some frequency-dependent assumptions: $R_{ch}$, $R_d + R_s$, $C_{ds}$, $L_d + L_s$.
2. Plot real and imaginary parts of equation (21) using a least squares fitting (LSF) function and scanning for minimum error between measured and simulated Z-parameters.
3. Calculate estimations of the following parameters using some frequency-dependent assumptions: $R_s$, $L_s$.
4. Plot real and imaginary parts of equation (20) using a least squares fitting (LSF) function and scanning for minimum error between measured and simulated Z-parameters.
5. Calculate estimations of the following parameters using some frequency-dependent assumptions: $C_g$, $R_{dy}$, $R_g + R_s$, $L_g + L_s$.
6. Plot real and imaginary parts of equation (19) using a least squares fitting function and scanning for minimum error between measured and simulated Z-parameters.

The results of these steps comparing the LSF simulated functions Z-parameters against the measured Z-parameters are shown in Figure 35 ($Z_{11}$), Figure 36 ($Z_{12}$), and Figure 37 ($Z_{22}$).

Finally, with the extrinsic inductance, resistance and capacitance assigned a particular value (bias independent), they can be simply de-embedded from the device S-parameter measurements in the on-state (“hot-FET”). The remaining intrinsic elements can be calculated analytically by transforming the de-embedded S-parameters to Y-parameters and using the well-established analytical equations developed for general FETs to assign bias-dependent values for the intrinsic variables shown in Figure 25 [94, 95]. Table 3 shows the final calculated small-signal parameters. Figure 38 illustrates excellent agreement among the model and measured S-parameters for $L_G$ = 150 nm at a bias of $V_{GS}/V_{DS}$ = +0.6/2.0 V.

## 5.5 NW-HEMT RF Performance versus Bias and $L_G$

Section 5.4 described the extrinsic (bias-independent) and intrinsic (bias dependent) extraction procedure to characterize RF performance at a single bias condition. However, it is necessary to characterize the NW-HEMT RF performance as a function of $V_{GS}$, $V_{DS}$ and $L_G$ to fully understand its operational potential. Further, by scaling the $L_G$, critical information can be obtained about the parasitic capacitance penalty from using NWs.

S-parameters were measured for $V_{GS}$ from +0.3 V to +0.7 V in +0.1 V increments and $V_{DS}$ from +0.5 V to +3.0 V in +0.5 V increments for each of the four $L_G$. The

extraction methodology was used in from Section 5.4 to arrive at the small-signal equivalent circuit parameters. Table 4 shows the results of varying $V_{DS}$ and $L_G$ with $V_{GS}$ = +0.6 V ($G_{M,peak}$). The $f_T/f_{max}$ shown in the table are calculated values based on the simulated circuit values. For example, the measured $f_T$ and simulated $f_{max}$ in Figure 39 was 30 GHz and 75 GHz respectively; the calculated $f_T$ and $f_{max}$ from Table 4 using equations (4) and (5) was 28 GHz and 67 GHz, respectively, giving an error of approximately 7% for $f_T$ and 11% for $f_{max}$. The larger discrepancy in $f_{max}$ can be expected since the experimental value is extrapolated with the model; whereas, the $f_T$ value was measured within the frequency measurement range. Nevertheless, the measured, simulated, and analytically calculated $f_T/f_{max}$ are in good agreement. The agreement is additionally shown in the smith chart plots of Figure 40 for the same device at different drain voltages illustrating excellent agreement in simulated and measured S-parameters versus bias.

Figure 41 illustrates the variation of extracted SSM parameters as a function of $V_{GS}$, $V_{DS}$ and $L_G$, respectively. The gate capacitances, $C_{gs}$ and $C_{gd}$, are greatly affected by both drain and gate bias because of the close proximity of the gate-recessed $n^+$ GaAs cap to the T-gate stem, just tens of nanometers as confirmed by cross-sectional SEM. The source and drain access resistance ($R_S$, $R_D$) was in the range of 25-35 Ω for the studied $L_G$ range. The $R_S$ is excellent considering the extracted intrinsic transconductance, $g_{m,I}$ ~ 3-6 mS, results in $R_S \cdot g_{m,i} << 1$ and the measured transconductance, $g_m = g_{m,i} / (1 + R_S \cdot g_{m,i})$, is not greatly affected. Low Ti/Pt/Au T-gate resistance ($R_G$) increased incrementally from 100-188 Ω·$\mu$m as $L_G$ decreased. The intrinsic resistance ($R_i$) was the most volatile parameter which followed closely with the gate diode leakage. For example, $R_i$ was the

highest as $V_{DS}$ and $V_{GS}$ approached 0 V and +0.7 V, respectively, which is the two-terminal bias condition for forward-bias Schottky gate leakage. The optimal $R_i$ occurs when the electron channel is formed at higher $V_{DS}$ but with $V_{GS}$ < +0.7 V to prevent the gate diode from turning on. The output conductance, $g_{ds}$, remains low for the entire biasing range, which is due to the excellent electrostatics afforded by the 3D NW channel multi-gate. The intrinsic gain, $g_o = g_{mi} / g_{ds}$, an important figure of merit for high $f_{max}$ (Figure 41(a)) clearly shows improvement with $V_{DS}$. For $L_G$ = 150 nm, a high $g_o$ ~ 25 was extracted. The significance of low terminal and intrinsic resistances combined with low output conductance for high $f_{max}$ is reiterated below:

$$f_{\max} = \frac{f_T}{2\sqrt{g_{ds}\left(R_G + R_i + R_S\right) + 2\pi f_T R_G C_{gd}}} \propto \frac{g_m}{\sqrt{g_m + g_{ds}}} \tag{22}$$

Figure 28 illustrated the unique layout of the NW-HEMT structure which has parasitic capacitance due to the T-gate structure and the NW spacing. Figure 28(a) and (b) emphasize the bi-directionality of the planar VLS process introducing gaps between parallel sites. The current gain cutoff frequency, $f_T \approx g_m / (2\pi \cdot C_g)$, requires large $g_m / C_g$ ratio where $C_g = C_{g,I} + C_{g,e}$ and $C_{g,e}$ is the extrinsic fringing gate capacitance. Both $C_{g,i}$ and $C_{g,e}$ can be separated into gate-source ($C_{gs,i}$ and $C_{gs,e}$) and gate-drain ($C_{gd,i}$ and $C_{gd,e}$) components as illustrated in Figure 28(c).

For the $L_G$ = 150 nm NW-HEMT device, the $C_{g,i}$ and $C_{g,e}$ were extracted and analyzed. The $L_G$-independent $C_{g,e}$ can be extracted from the intercept of a $C_g$ versus $L_G$ plot in Figure 41(c). For each gated device, the $C_g$ is normalized by taking the three-sided gated perimeter of each NW multiplied by the number of NWs. $C_{gs,e}$ and $C_{gd,e}$ were found to be 15.8 fF and 6.8 fF, respectively. The slope of $C_{gs}$ and $C_{gd}$ versus $L_G$ defines the $L_G$-dependent elements, $C_{gs,i}$ and $C_{gd,i}$, which are 7.5 fF and 3.5 fF, respectively.

When comparing these values to the total extracted $C_{gs}$ and $C_{gd}$ in Figure 41(a)-(b), we find $C_{gs,i}/C_{gs}$ and $C_{gd,i}/C_{gd}$ are 33% and 35%, respectively. In other words, ~2/3 of the total extracted $C_g$ is parasitic. Most of $C_{g,p}$ is likely caused by the bi-directional VLS NW growth which can be optimized on (110) GaAs substrate orientation for unidirectional NW assembly and immediately enhance the $g_m$ / $C_g$ ratio for higher $f_T/f_{max}$ [82].

The total intrinsic delay, $\tau_i$, is expressed as

$$\tau_\mathrm{i} = \frac{C_{g,i}}{g_{m,i}} \qquad \text{(sec)} \qquad (23)$$

which is approximately 1.86 ps for the NW-HEMT device with $L_G$ = 150 nm. The corresponding electron velocity, $v_e$, is

$$v_\mathrm{e} = \frac{L_G}{\tau_i} \qquad \text{(cm/sec)} \qquad (24)$$

which is approximately $0.8 \cdot 10^7$ cm/s. Removing the fringing capacitance, a theoretical $f_T$ can be determined by

$$f_T = \frac{1}{2\pi\tau_i} \qquad \text{(Hz)} \qquad (25)$$

and is calculated to be 85 GHz. A theoretical ideal $f_{max}$ can be expressed as

$$f_\mathrm{max} = \sqrt{\frac{f_T}{8\pi R_G C_{gd,i}}} \qquad \text{(Hz)} \qquad (26)$$

and is approximately 248 GHz. Both of these theoretical values represent the upper limits of the NW-HEMT and are difficult to achieve without extreme optimization of the NW assembly and device contacts. Despite this, the reported extrinsic $f_{max}$ = 78 GHz is highest compared to other VLS NW FETs with planar NWs along the substrate surface. The high $f_{max}$ is attributed to low device resistance and good intrinsic gain. High $C_{g,p}$

limiting RF performance can be improved with device engineering and unidirectional planar VLS NW growth on future samples.

## 5.6 Figures and Tables

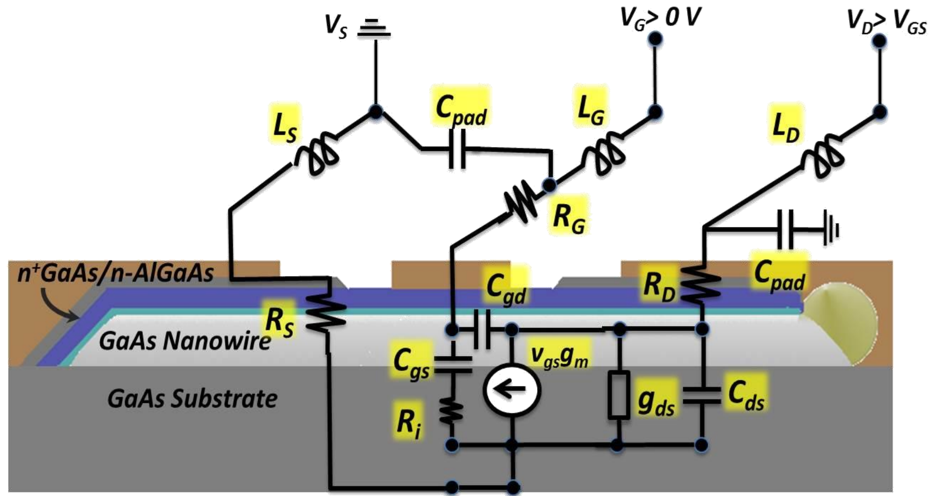



**Figure 25**: Conventional HEMT small-signal model with extrinsic and intrinsic (inside blue box) passive elements.

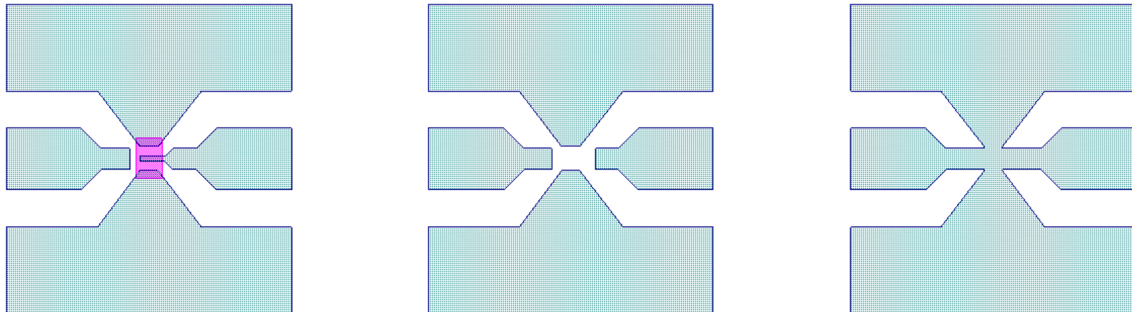
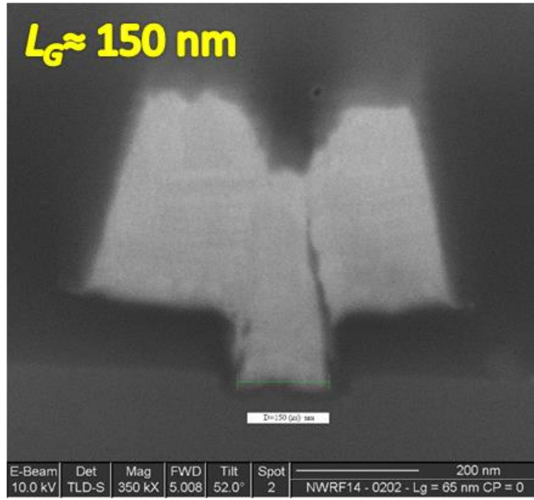
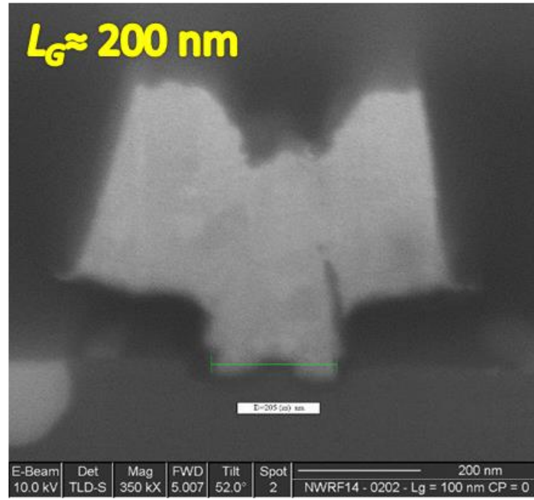
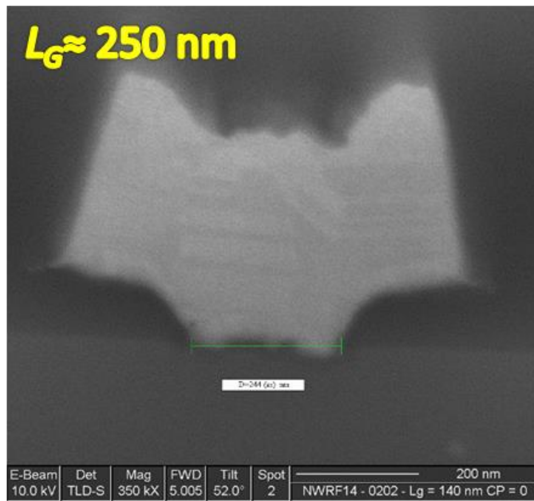


**Figure 26**: (left) NW-HEMT device showing pads and mesa in the center, (middle) open calibration structure without mesa, and (right) short calibration structure.



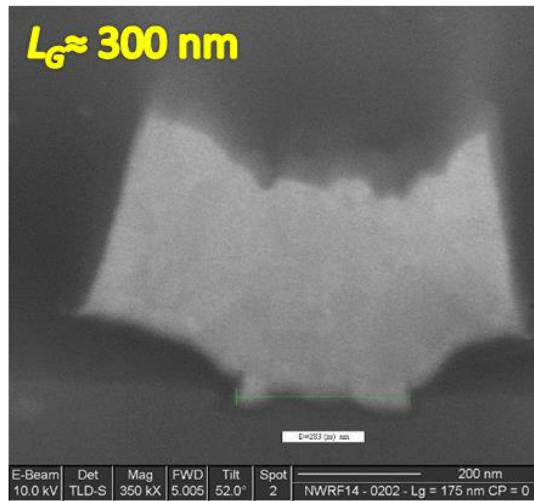




**Figure 27**: Focus ion beam cross-section showing incremental increase of gate length from 150 nm to 300 nm. The scale bar in the lower-right corner is 200 nm.

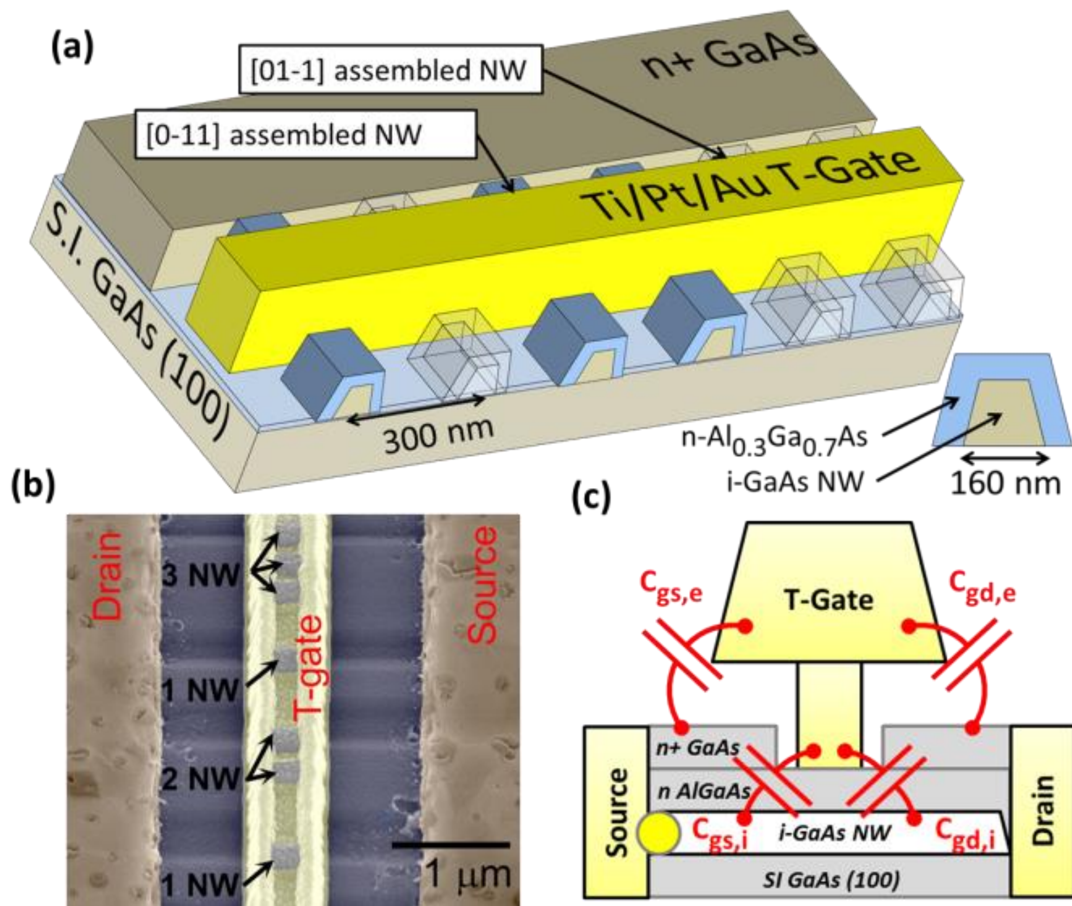



**Figure 28**: (a) NW-HEMT device schematic in the gate recess region depicting the bi-directional VLS GaAs NW self-assembly on SI GaAs (100) substrate. Approximately half of the NWs are used for transistor fabrication. (b) Magnified top-view false color SEM of the NW-HEMT channel region. (c) A capacitive diagram of the NW-HEMT illustrating both extrinsic and intrinsic gate capacitance.

(a) (b)

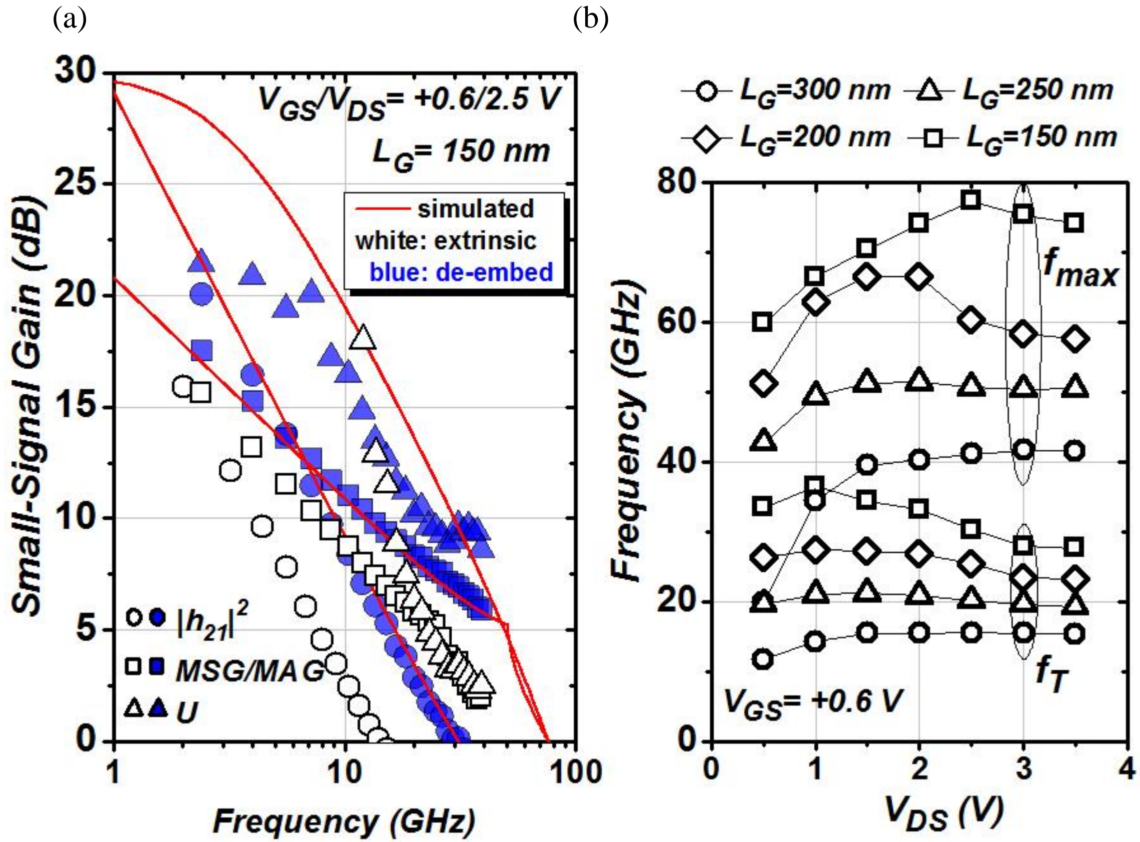



**Figure 29**: (a) Representative simulated (red line), extrinsic (clear symbol) and de-embedded (blue symbol) $f_T$ and $f_{max}$ at $V_{GS}/V_{DS}$ = +0.6/2.5 V for $L_G$ = 150 nm. (b) De-embedded $f_T$, $f_{max}$ vs. $V_{GS}$, $V_{DS}$ for $L_G$ = 300 nm, 250 nm, 200 nm, 150 nm at the $G_{M\cdot peak}$ gate bias.

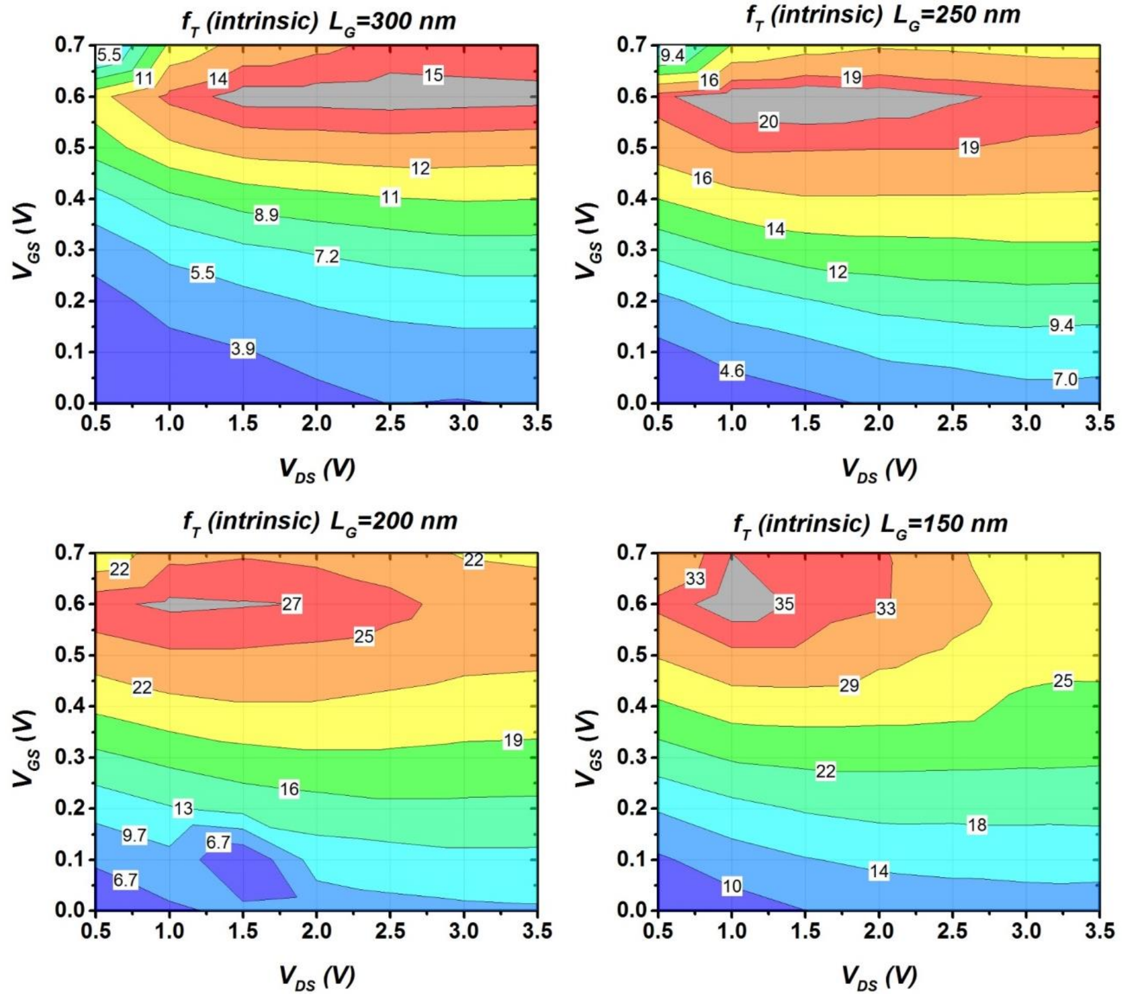



**Figure 30**: De-embedded $f_T$ vs. $V_{GS}$, $V_{DS}$ for $L_G$ = 300 nm, 250 nm, 200 nm, 150 nm.

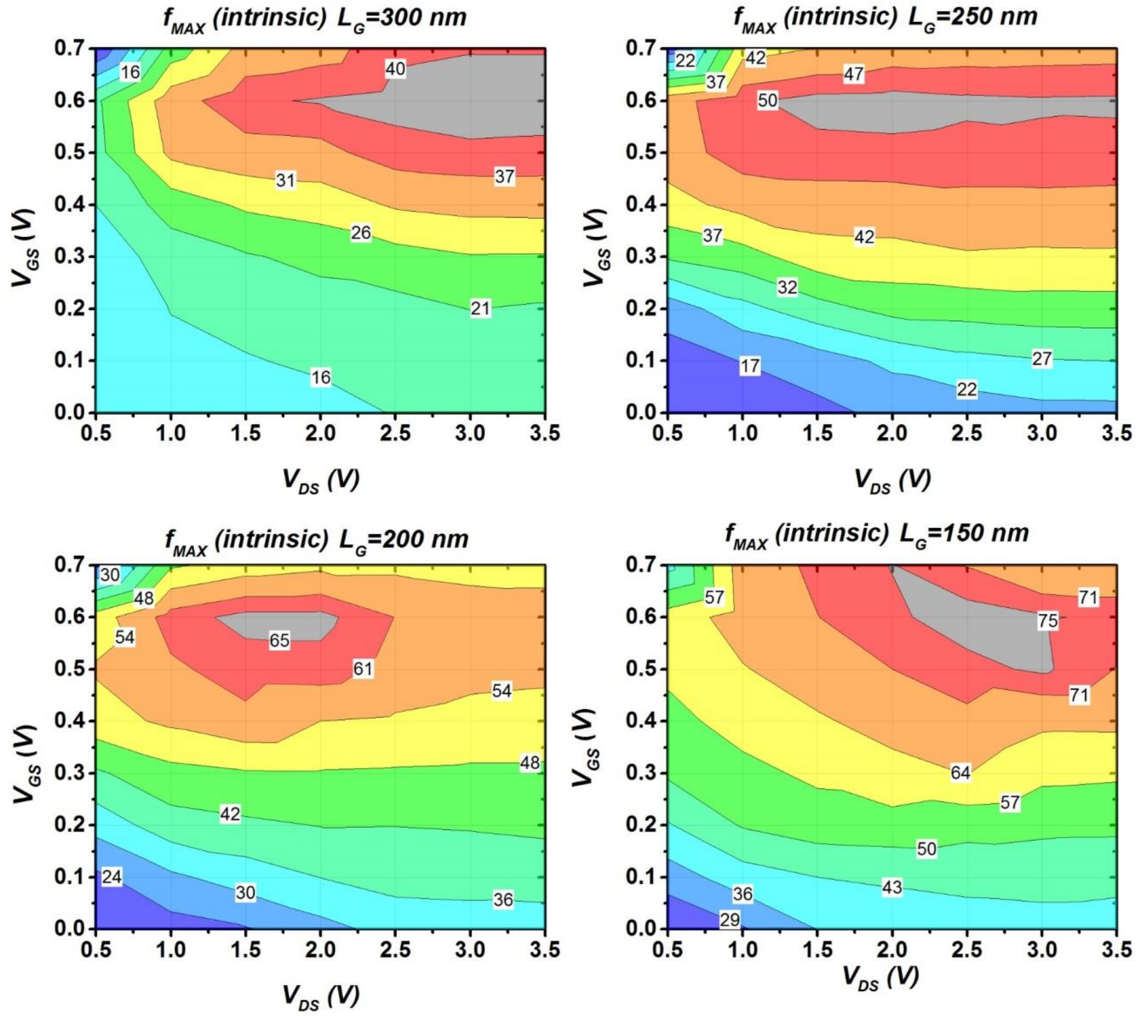



**Figure 31**: De-embedded $f_{max}$,UPG vs. $V_{GS}$, $V_{DS}$ for $L_G$ = 300 nm, 250 nm, 200 nm, 150 nm.

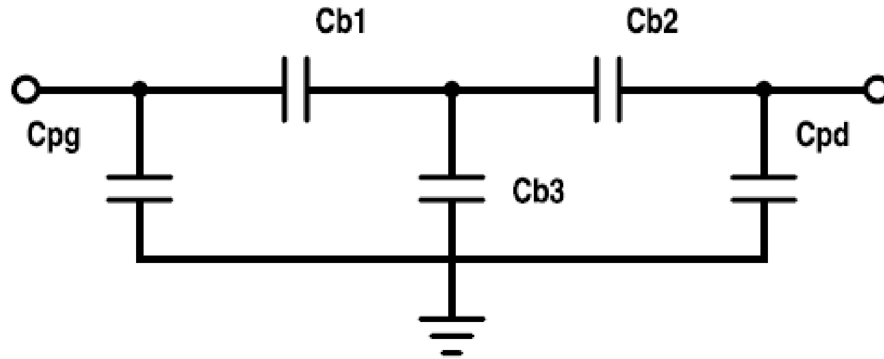



**Figure 32**: Small-signal equivalent circuit of a NW-HEMT biased in depletion at low frequency (< 6 GHz).

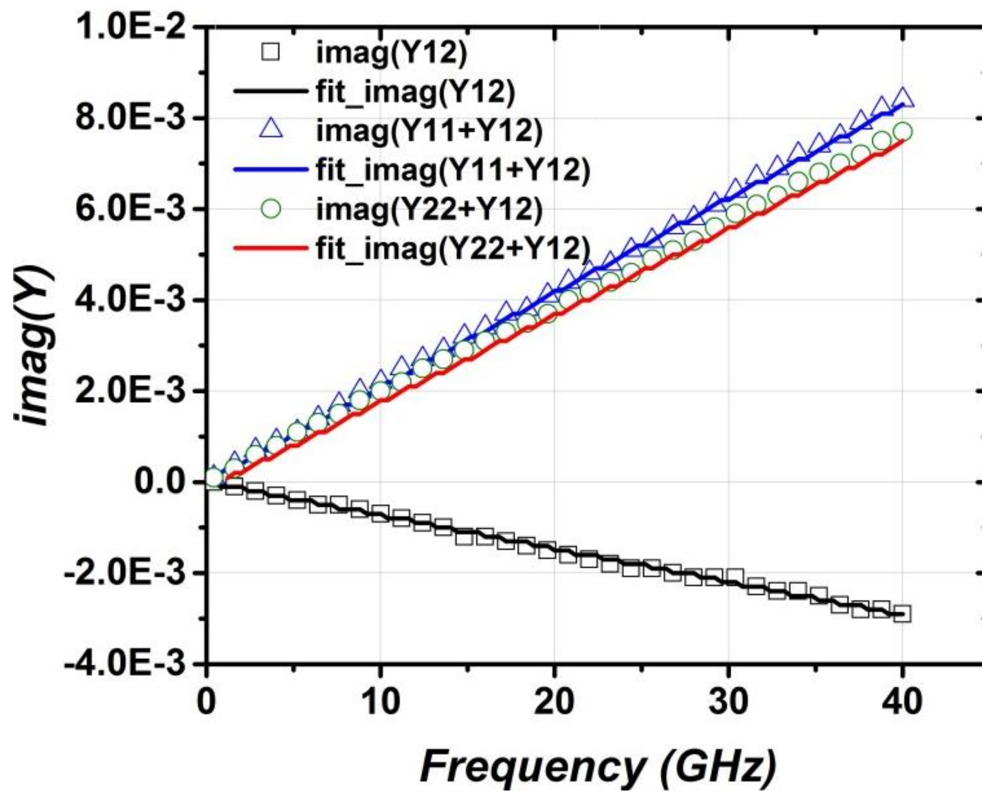



**Figure 33**: Measured admittance parameters (imaginary component) versus frequency for extracting pad capacitance.

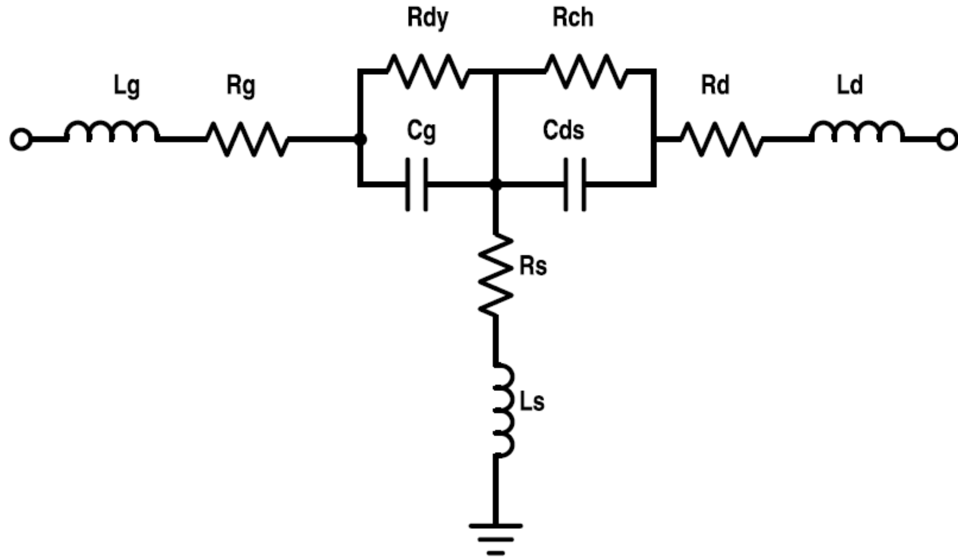



**Figure 34**: Small-signal equivalent circuit of a NW-HEMT with zero-bias.

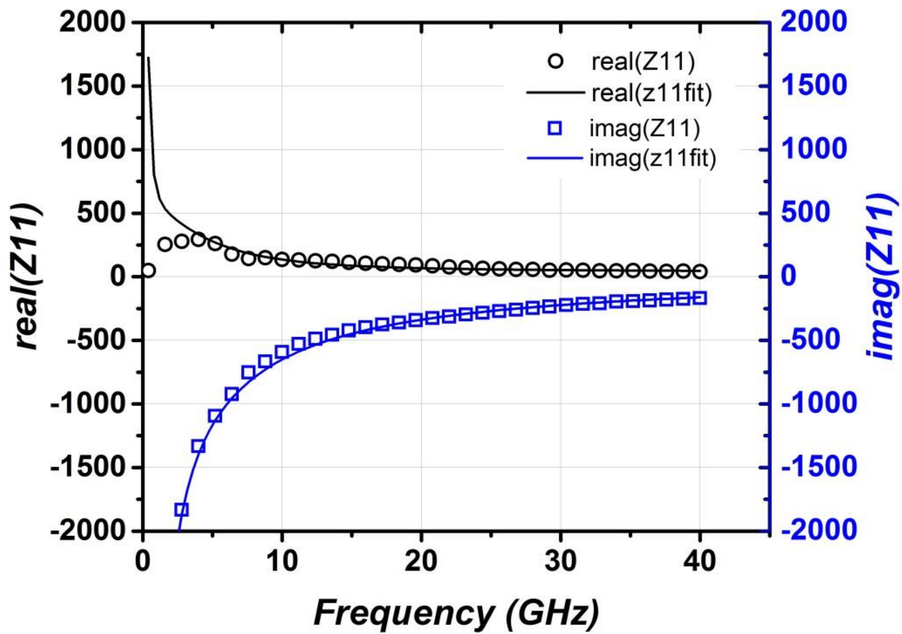



**Figure 35**: NW-HEMT measured vs. simulated open-channel (zero-bias) $Z_{11}$ parameters.

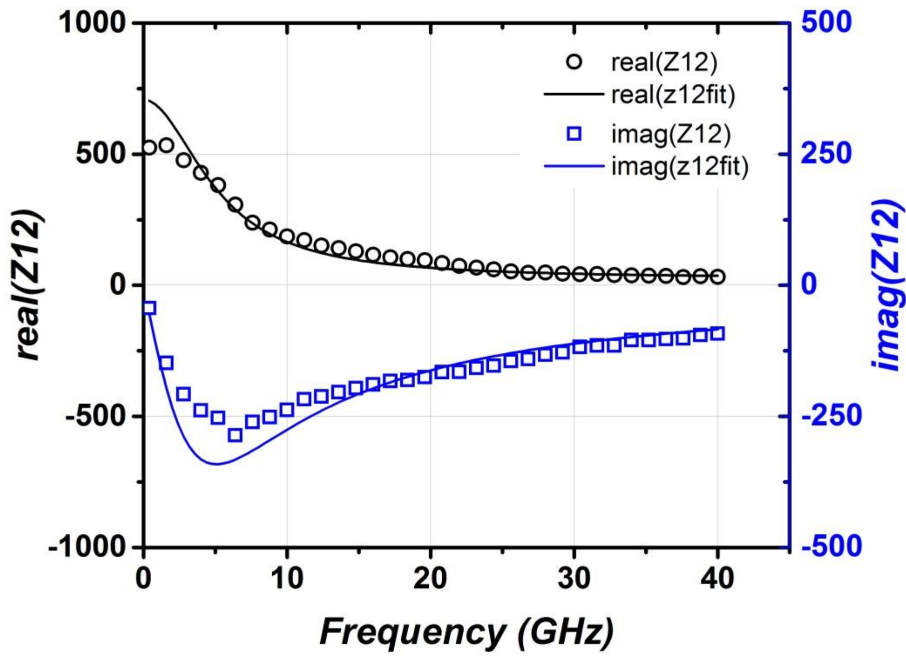



**Figure 36**: NW-HEMT measured vs. simulated open-channel (zero-bias) $Z_{12}$ parameters.

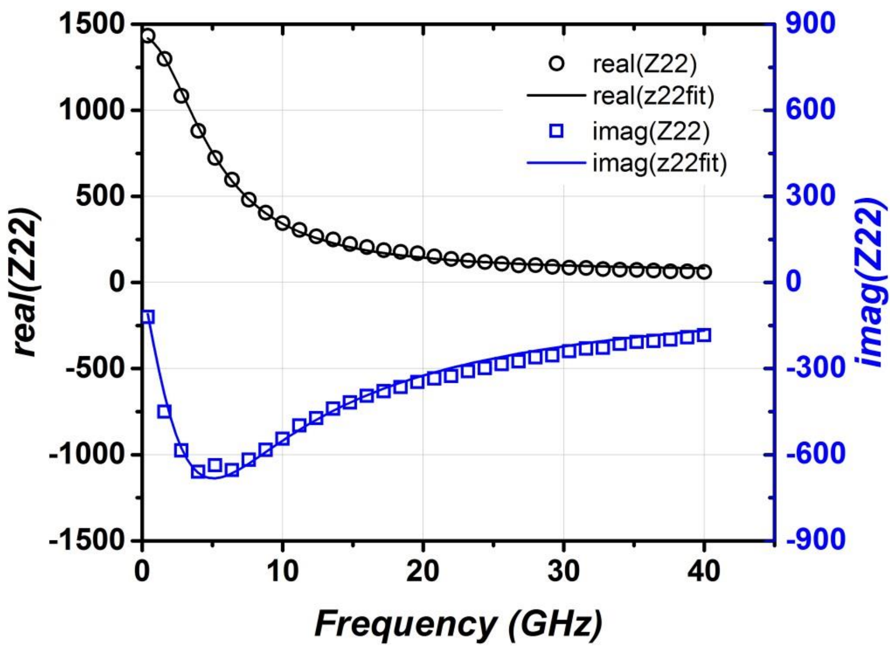



**Figure 37**: NW-HEMT measured vs. simulated open-channel (zero-bias) $Z_{22}$ parameters.

**Table 3**: NW-HEMT Small-Signal Circuit Variable Values; the Extracted Values Shown Are For $L_G$ = 150 nm at a Bias of $V_{GS}/V_{DS}$ = +0.6/2.0 V

| **Extrinsic** | | **Intrinsic** | |
|---|---|---|---|
| $\mathbf{C_{pg}}$ | 25 fF | $\mathbf{C_{gs}}$ | 23 fF |
| $\mathbf{C_{pd}}$ | 25 fF | $\mathbf{C_{gd}}$ | 10 fF |
| $\mathbf{L_s}$ | 6.0 pH | $\mathbf{C_{ds}}$ | 14 fF |
| $\mathbf{L_d}$ | 7.3 pH | $\mathbf{g_{mi}}$ | 5.9 mS |
| $\mathbf{L_g}$ | 48 pH | $\mathbf{g_{ds}}$ | 0.3 mS |
| $\mathbf{R_s}$ | 24 Ω | $\mathbf{R_i}$ | 16 Ω |
| $\mathbf{R_d}$ | 34 Ω | $\mathbf{R_{gd}}$ | 70 Ω |
| $\mathbf{R_g}$ | 16 Ω | **tau** | 0.23 ps |

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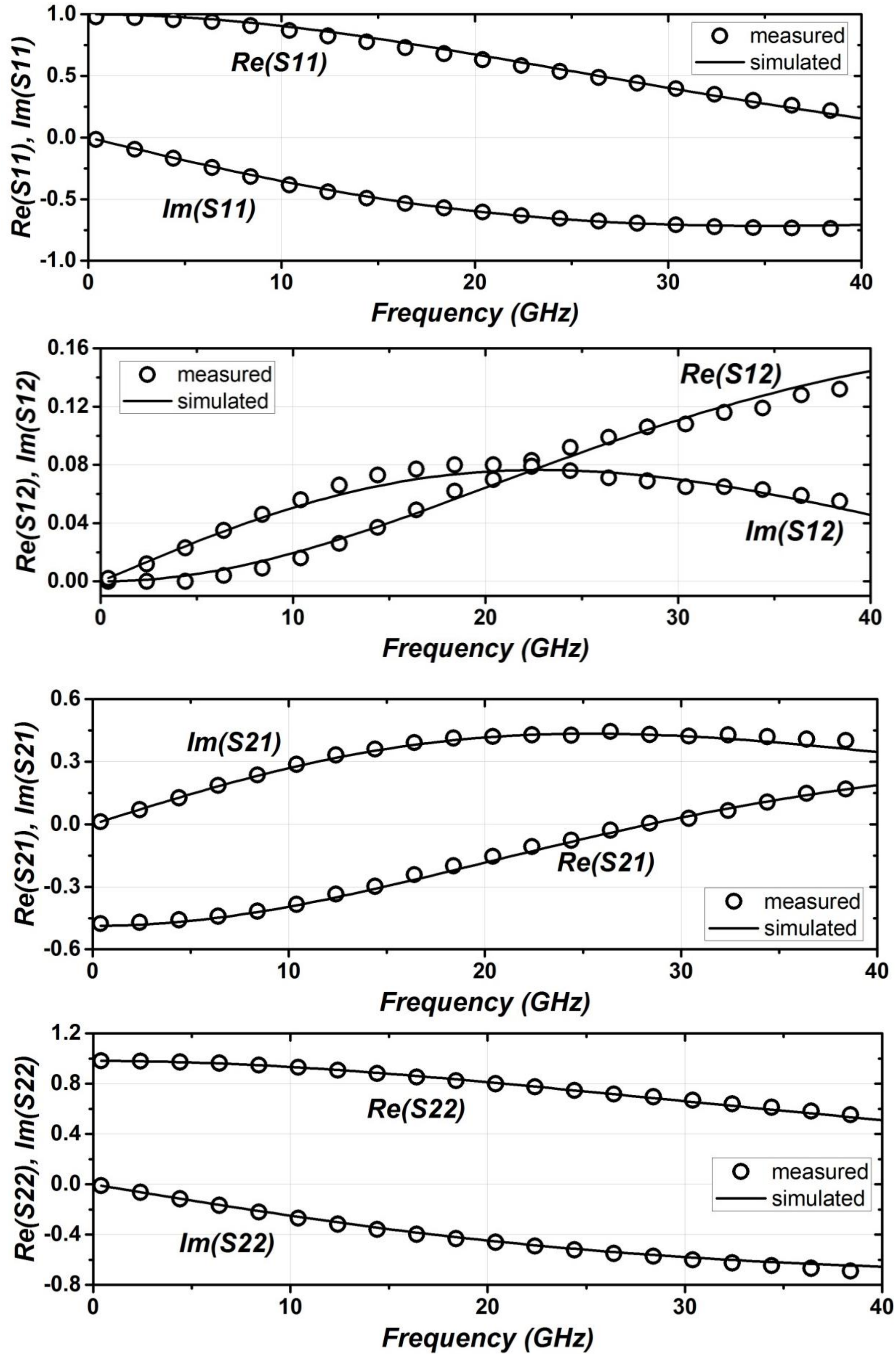


**Figure 38**: NW-HEMT measured vs. simulated S-parameters for $L_G$ = 150 nm at a bias of $V_{GS}/V_{DS}$ = +0.6/2.0 V.

**Table 4**: Extracted NW-HEMT Small-Signal Circuit Variable Values for Various $V_{DS}$ and $L_G$ with $V_{GS}$ = +0.6 V

| Vds (V) | Lg (nm) | Cgs (fF) | Cgd (fF) | Cds (fF) | gmi (mS) | gds (mS) | Ri (Ω) | Rgd (Ω) | Rs (Ω) | Rd (Ω) | Rg (Ω) | ft (GHz) | fmax (GHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.5 | 300 | 16.83 | 14.66 | 14.62 | 2.12 | 0.46 | 74.60 | 25.80 | 26.26 | 24.84 | 8.80 | 10.71 | 22.03 |
| 1 | 300 | 18.42 | 12.81 | 14.56 | 2.51 | 0.18 | 62.40 | 35.50 | 26.26 | 24.84 | 8.80 | 12.77 | 39.10 |
| 1.5 | 300 | 19.97 | 11.79 | 14.52 | 2.71 | 0.15 | 55.39 | 49.29 | 26.26 | 24.84 | 8.80 | 13.58 | 45.44 |
| 2 | 300 | 21.40 | 10.98 | 14.48 | 2.83 | 0.14 | 51.69 | 64.63 | 26.26 | 24.84 | 8.80 | 13.89 | 48.75 |
| 2.5 | 300 | 22.62 | 10.31 | 14.37 | 2.88 | 0.12 | 50.38 | 79.87 | 26.26 | 24.84 | 8.80 | 13.90 | 51.12 |
| 3 | 300 | 23.61 | 9.80 | 14.28 | 2.89 | 0.11 | 49.88 | 94.47 | 26.26 | 24.84 | 8.80 | 13.75 | 52.58 |
| 0.5 | 250 | 19.86 | 13.64 | 13.47 | 3.60 | 0.40 | 50.27 | 48.82 | 27.63 | 18.14 | 6.98 | 17.12 | 40.53 |
| 1 | 250 | 21.42 | 12.37 | 13.42 | 3.84 | 0.26 | 40.35 | 64.75 | 27.63 | 18.14 | 6.98 | 18.09 | 53.03 |
| 1.5 | 250 | 23.05 | 11.60 | 13.41 | 3.96 | 0.23 | 34.93 | 80.53 | 27.63 | 18.14 | 6.98 | 18.18 | 57.59 |
| 2 | 250 | 24.61 | 10.94 | 13.35 | 4.00 | 0.20 | 31.94 | 97.63 | 27.63 | 18.14 | 6.98 | 17.91 | 60.51 |
| 2.5 | 250 | 25.98 | 10.40 | 13.25 | 3.99 | 0.18 | 31.20 | 114.37 | 27.63 | 18.14 | 6.98 | 17.46 | 61.98 |
| 3 | 250 | 27.28 | 9.94 | 13.14 | 3.95 | 0.16 | 31.54 | 131.07 | 27.63 | 18.14 | 6.98 | 16.90 | 62.56 |
| 0.5 | 200 | 17.38 | 13.24 | 14.91 | 4.72 | 0.61 | 52.65 | 8.80 | 24.62 | 29.06 | 13.22 | 24.55 | 42.84 |
| 1 | 200 | 19.17 | 11.71 | 14.56 | 4.99 | 0.35 | 38.71 | 24.65 | 24.62 | 29.06 | 13.22 | 25.71 | 56.70 |
| 1.5 | 200 | 20.90 | 10.89 | 14.43 | 5.06 | 0.30 | 31.27 | 39.15 | 24.62 | 29.06 | 13.22 | 25.32 | 60.66 |
| 2 | 200 | 22.66 | 10.21 | 14.29 | 5.06 | 0.27 | 27.31 | 54.92 | 24.62 | 29.06 | 13.22 | 24.50 | 62.73 |
| 2.5 | 200 | 24.34 | 9.66 | 14.12 | 5.00 | 0.23 | 25.82 | 70.99 | 24.62 | 29.06 | 13.22 | 23.38 | 63.70 |
| 3 | 200 | 26.06 | 9.18 | 13.99 | 4.90 | 0.21 | 25.70 | 87.42 | 24.62 | 29.06 | 13.22 | 22.11 | 63.55 |
| 0.5 | 150 | 17.17 | 13.35 | 14.73 | 5.61 | 0.78 | 40.06 | -7.50 | 24.33 | 33.49 | 15.63 | 29.26 | 46.14 |
| 1 | 150 | 19.24 | 11.68 | 14.14 | 5.92 | 0.44 | 25.80 | 7.26 | 24.33 | 33.49 | 15.63 | 30.46 | 60.35 |
| 1.5 | 150 | 21.24 | 10.80 | 13.97 | 5.97 | 0.41 | 19.09 | 20.96 | 24.33 | 33.49 | 15.63 | 29.65 | 62.77 |
| 2 | 150 | 23.33 | 10.06 | 13.81 | 5.93 | 0.30 | 15.72 | 36.54 | 24.33 | 33.49 | 15.63 | 28.27 | 66.98 |
| 2.5 | 150 | 25.41 | 9.42 | 13.62 | 5.83 | 0.26 | 15.05 | 53.48 | 24.33 | 33.49 | 15.63 | 26.65 | 67.65 |
| 3 | 150 | 27.50 | 8.92 | 13.44 | 5.66 | 0.22 | 15.75 | 70.57 | 24.33 | 33.49 | 15.63 | 24.73 | 67.13 |

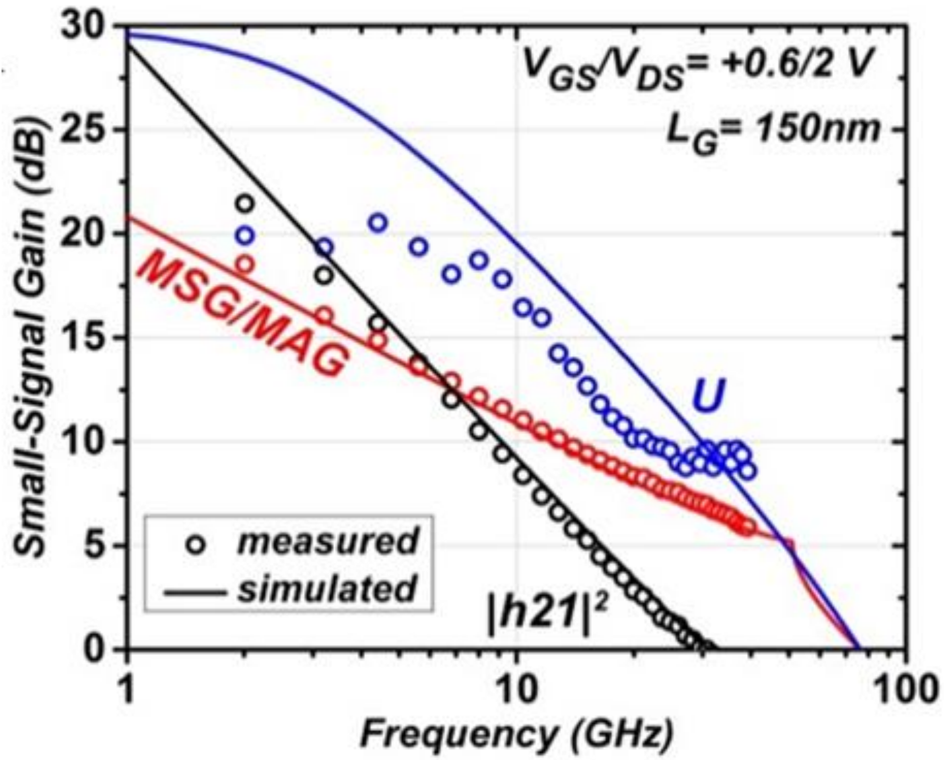


**Figure 39**: Measured vs. simulated small-signal gain for $L_G$ = 150 nm at a bias of $V_{GS}/V_{DS}$ = +0.6/2.0 V.

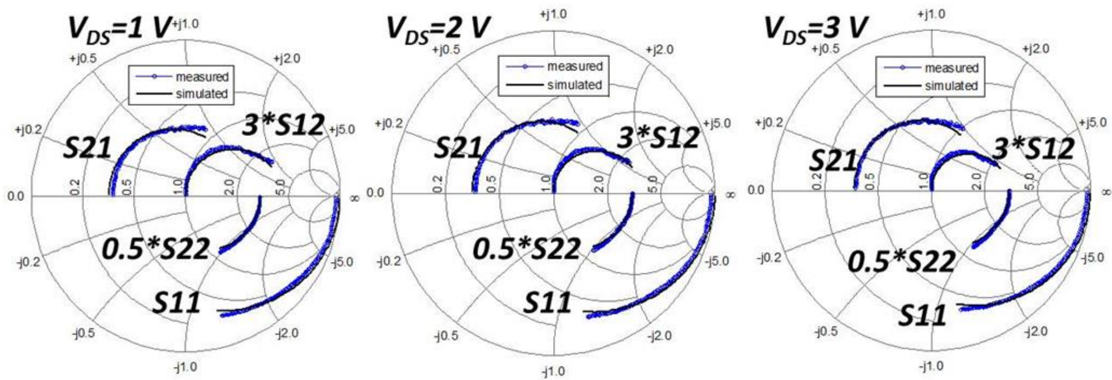


**Figure 40**: Measured versus simulated S-parameters for various $V_{DS}$ at $V_{GS}$ = 0.6 V and $L_G$ = 150 nm showing excellent agreement.

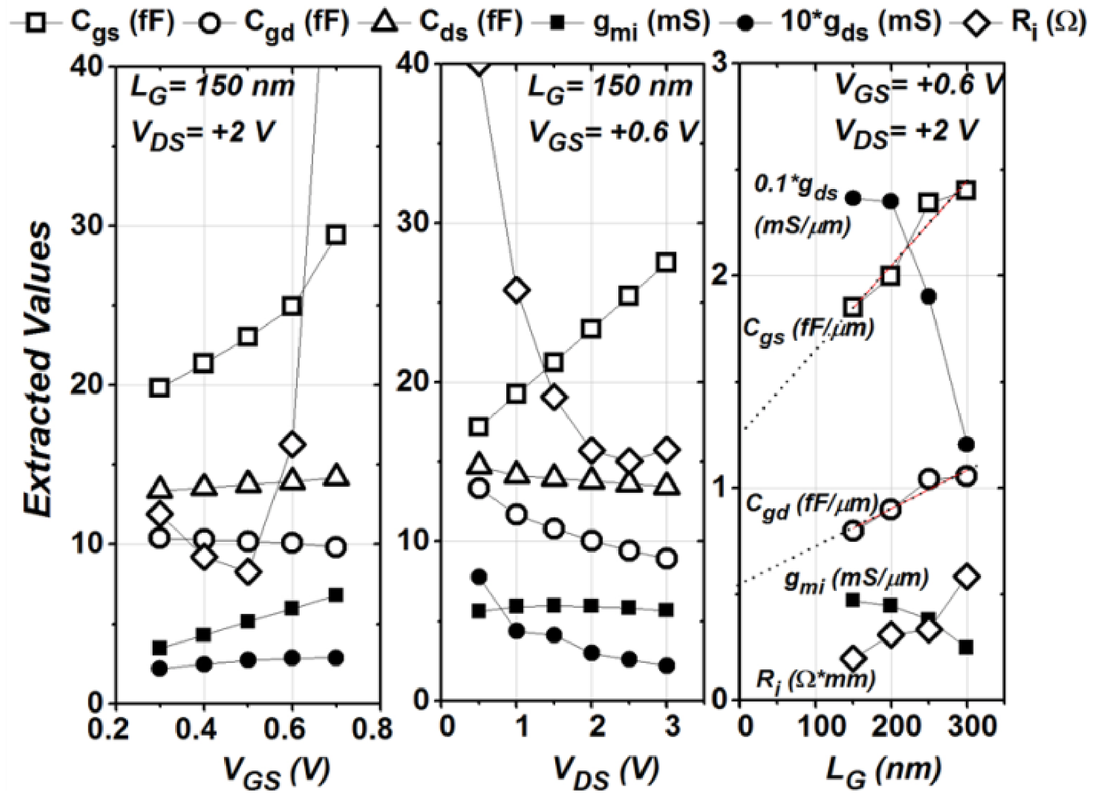


**Figure 41**: Extracted SSM parameters for high $f_{max}$ as a function of (left) $V_{GS}$, (center) $V_{DS}$ and (right) $L_G$. On the right, the values are normalized to the total NW width.

# 6. TOWARD TOP-DOWN NW $Ga_2O_3$ MOSFETS

Gallium oxide ($Ga_2O_3$) is emerging as a potential disruptive electronic material for high-voltage electronics applications. The excitement of this material is due to its (1) ultra-wide bandgap of ~4.8 eV with ~8 MV/cm theoretical critical field strength [101], (2) up to four-inch native substrate availability and capability of melt-growth synthesis [102], and (3) wide range of n-type doping achievable by halide vapor phase epitaxy (HVPE) [103], molecular beam epitaxy (MBE) [104], low-pressure chemical vapor chemical deposition (LPCVD) [105], MOCVD [106], and metal-organic vapor phase epitaxy (MOVPE) [107, 108]. The β-phase $Ga_2O_3$ unit crystal has a monoclinic structure and is reported as the most thermally stable and conducive for single-crystal homoepitaxial growth [109, 110]. For heterogeneous integration, a notable cleavage plane is located along the (100) crystal plane which has incited nanomembrane research for integration with arbitrary substrates and two-dimensional semiconductors [111-113].

The first transistor device by homoepitaxial $Ga_2O_3$ was demonstrated in 2012 with a Sn-doped $Ga_2O_3$ channel grown by MBE on (010) semi-insulating β-$Ga_2O_3$ substrates [101]. MOSFETs with Si-doping and channel implantation grown by MBE rapidly followed with breakdown exceeding 750 V with a field-plate [114, 115]. To complement this, here, the first β-$Ga_2O_3$ transistors on alternative (100) β-$Ga_2O_3$ substrates by MOVPE were fabricated and characterized.

The purpose of this chapter is to (1) understand the effects of channel thickness and doping on the electrical performance using planar $Ga_2O_3$ MOSFETs which leads to (2) a high-performance device verifying beyond-GaN critical field strength [116].

Finally, (3) the results of this study feed into the design and fabrication of the first 3D NW-array $Ga_2O_3$ MOSFET with excellent early performance [117].

## 6.1 Device Development of $Ga_2O_3$ MOSFETs

Mg-doped semi-insulating (100) 10 x 10 $mm^2$ β-$Ga_2O_3$ substrate pieces were synthesized using the Czochralski method as reported in [118]. Then, Sn-doped $Ga_2O_3$ was homoepitaxially grown by MOVPE with varying thickness and chemical Sn concentration according to Table 5 [107, 108]. Two-finger MOSFETs were fabricated using the process flow described in Figure 42. First, device isolation was achieved using $BCl_3$ dry etching of the active layer [119]. Ohmic contacts were formed by Ti/Al/Ni/Au metal evaporation followed by a 470 °C rapid thermal anneal for one minute in nitrogen, similar to the process reported by Higashiwaki et al. [101]. The contacts exhibited ohmic behavior, although optimization is needed and planned for future samples. A 20 nm $Al_2O_3$ gate oxide layer was thermally deposited by atomic layer deposition (ALD) at 250 °C. Finally, Ti/Au interconnects and 2-$\mu$m optical gate length ($L_G$) layers were deposited on the gate oxide after selectively removing $Al_2O_3$ on the ohmic contacts by either BOE or $CF_4$ RIE.

The MOSFETs are a two-finger split-gate type with a ground-signal-ground layout for automated electrical characterization using RF probes. The $L_G$ and total width ($W_G$) is ~2 $\mu$m and 100 $\mu$m, respectively, and the gate-source spacing ($L_{GS}$) is ~0.5 $\mu$m. The gate-drain spacing ($L_{GD}$) varies with the following distances: 0.5, 5, 10, 15, and 20

$\mu$m. Figure 43 shows a representative MOSFET with $L_{GS}$ = 0.5 $\mu$m, $L_G$ = 2 $\mu$m and $L_{GD}$ = 0.5 $\mu$m.

## 6.2 $Ga_2O_3$ Doping and Thickness Study

Growth and device fabrication of homoepitaxial $Ga_2O_3$ MOSFETs are at its infancy stages. As a reminder, these are the first $Ga_2O_3$ MOSFETs fabricated by MOVPE and little is known about Sn-concentration (target during growth) versus electron concentration ($N_D$) (what is activated). During this work, capacitance-voltage ($C$-$V$) measurements were not readily available; however, we were able to extract the electron concentration using the transfer-length method (TLM) and Hall-effect Van der Pauw (VDP) test structures and measurements. Sheet resistance ($R_{SH}$) and contact resistance ($R_C$) were measured using TLM structures with varying gaps from 5-30 $\mu$m in increments of 5 $\mu$m by forcing current and measuring voltage in a standard four-point probe setup. An automated Keithley 450 was used to measure ~18 test structures on the 10 mm x 10 mm samples. From the measured $R_{SH}$, the resistivity ($\rho$) can be calculated by

$$\rho = (q\mu N_D)^{-1} = R_{sh} d \qquad (\Omega\cdot\text{cm}) \qquad (27)$$

where $d$ is the thickness of the epitaxial Sn-doped $Ga_2O_3$ layer. Resistivity normalizes the $R_{SH}$ measurements by $d$ to evenly compare all samples versus doping concentration. The results are valuable in identifying an optimal $\mu$ x $N_D$ product for future MOSFET epitaxial design. The results in Figure 44 show the measured resistivity versus chemical Sn concentration. An optimal window appears between ~1.0 – 1.2 x $10^{18}$ $cm^{-3}$. The $R_C$ was also extracted from the TLM gaps by measuring the resistance versus gap and

extrapolating to 0 $\mu$m and dividing by two. The $R_C$ statistical results of Figure 45 mirror those of Figure 44 since, essentially, resistivity is related to doping level, or the placement of the Fermi level ($E_F$) within the bandgap of $Ga_2O_3$; closer to the conduction band would lower the energy barrier for electron transport between the ohmic metal and semiconductor. $R_C$, as expected, was small for the lowest resistivity samples measured. For most of the samples in this study, the $R_C$ was ~10-20 Ω·mm which still requires significant improvement for low series resistance for the MOSFETs. Implant ionization or including a highly conductive ohmic cap layer are solutions to be investigated in the future [115].

The $\mu$ and electron sheet charge density, $n_s$, were measured using VDP Hall effect test structures. The $\mu$ versus Sn concentration during growth is shown in Figure 46. The results indicate the mobility is independent of doping (~17 - 20 $cm^2/Vs$) between Sn concentrations of 1 – 2 x $10^{18}$ $cm^{-3}$. For MOVPE on (100) substrate orientation, it has been documented that $\mu$ is largely dominated by stacking faults and twin defects that may originate from the miscut of the (100) growth plane [108]. The slight miscut orientations of identically doped Sn-concentration samples are likely the reason for $\mu$ variations observed at 1.4 and 1.7 x $10^{18}$ $cm^{-3}$ in Figure 46. The lower $\mu$ at the lowest doping concentration was also reported in [108]. It should be noted, during this work, 3-4x improvement in $\mu$ was observed near the end of this dissertation research with the same doping concentration on (010) Fe-doped semi-insulating $Ga_2O_3$ substrates and miscut (100) Mg-doped semi-insulating substrates which will be the subject of future research.

Finally, with measured $\mu$ and $R_{SH}$, equation (27) can be solved for $N_D$ to calculate the ionized donor concentration versus chemical Sn-concentration. The results are

plotted in Figure 47 and illustrate a generally increasing trend in electron concentration from 0.8 – 1.5 x $10^{18}$ $cm^{-3}$. The variability at higher doping requires further investigation. Regardless, there is a clear discrepancy comparing doping concentration versus electron concentration. This observation is somewhat expected because of the ultra-wide bandgap of $Ga_2O_3$ where dopants reside deeper in the bandgap. However, the problem is complicated due to the lack of understanding of Ga-O vacancies, mid-gap compensating acceptors, etc.

The next step was to measure planar $Ga_2O_3$ MOSFET $I_D$-$V_G$ performance as a function of doping concentration and epitaxial thickness to understand the effect on $V_{TH}$, $g_M$ and $I_{DS}$. $I_D$-$V_G$ transfer characteristics were measured at $V_{DS}$ = 10 V for the first three doping study samples from Table 5 with constant 200 nm channel thickness. Then, the second set of three with nearly the same Sn-doping concentration ~1.2 x $10^{18}$ $cm^{-3}$ were measured as a function of channel thickness. The samples were not in saturation near $I_{DSS}$ ($V_G$ = 0 V) because of high on-resistance ($R_{ON}$) and negative $V_{TH}$ yielding a high $V_{DS,sat} = |V_{GS} - V_{TH}|$. The device geometry was identical to that shown in Figure 43.

Figure 48(a) illustrates the expected tradeoff between doping concentration vs. $I_{DS}$ and $V_{TH}$; a higher doping level required large negative bias to pinch off the channel. The $g_M$ sweeps are shown in Figure 48(b) and show an increase in both magnitude and broadness of peak $g_M$ as the doping concentration increases. The relationship between doping and $V_{TH}$ can be expressed by the following equation:

$$V_{TH} = V_{FB} - qN_D W_d \left( \frac{1}{C_{ox}} + \frac{W_d}{2\varepsilon_o \varepsilon_S} \right) \quad \text{(V)} \qquad (28)$$

where $V_{FB}$ is the flatband voltage, $W_d$ is the thickness of the depleted channel at pinch-off conditions, $C_{ox}$ is the gate oxide capacitance, and $\varepsilon_o$ and $\varepsilon_s$ are the permittivity and

dielectric constants of $Ga_2O_3$. Equation (28) illustrates that $N_D$ (ionized donors) and $W_d$ have the largest influence on $V_{TH}$. The $V_{FB}$ assuming no interface charge is defined as:

$$V_{FB} = \Phi_M - \Phi_S = \phi_M - (\chi_S + \Phi_B) \qquad \text{(V)} \qquad (29)$$

where

$$\Phi_B = (E_C - E_F) = -V_t \ln\left(\frac{N_D}{N_C}\right) \qquad \text{(V)} \qquad (30)$$

and $\Phi_M$, $\chi_s$, and $N_C$ are gate metal work function, $Ga_2O_3$ electron affinity, and effective density of states in the $Ga_2O_3$ conduction band ($E_C$) [120], respectively. At room temperature, $V_t$ is the thermal voltage (~26 mV at 300 K). When the doping is sufficiently high, $\Phi_B \rightarrow 0$ since ($E_C$ - $E_F$) is small compared to $\chi_s$. Therefore, a good approximation for $V_{FB}$ is $V_{FB} \approx \Phi_M$ (Ti = 4.3 V) – $\chi_s$ (~ 4 V) ≈ +0.3 V. By using Ni and Pt as the gate electrode, the $V_{TH}$ can be shifted another ~1-2 V by simple metal work function engineering. It should be noted that when $V_{GS} > V_{FB}$, the channel should be in accumulation mode and forming a higher density channel near the oxide-$Ga_2O_3$ interface. Using the estimated electron concentration from Figure 47 we can calculate the expected $V_{TH}$ for a certain doping and thickness design using equations (29) - (30). For example, for 200 nm channel and chemical Sn concentration ~1.7 x $10^{18}$ $cm^{-3}$ ($N_D$ ~ 4.8 x $10^{17}$ $cm^{-3}$), a $V_{TH}$ = -21.1 V which is in excellent agreement with Figure 48.

Likewise, Figure 48(c)-(d) shows the dependence of Sn-doped channel thickness with approximately the same Sn-doping concentration ~1.2 x $10^{18}$ $cm^{-3}$. While the 150 nm and 200 nm channels can be sufficiently pinched-off by the gate bias, the 300 nm channel was too thick and the vertical field cannot penetrate deep enough into the channel. This trend suggests 6.7:1 $L_G/d$ aspect ratio is too small for SCE mitigation and

$L_G/d$ > 10:1 is a good a rule of thumb. The 300-nm sample requires a wrap-gate to pinch-off the channel which is described in Section 6.4.

## 6.3 Critical Field Strength Potential of $Ga_2O_3$ MOSFETs[3]

With an understanding for doping and channel thickness dependence on the electrical properties, we fabricated a high-performance depletion-mode planar $Ga_2O_3$ MOSFET to evaluate its early potential as a power MOSFET. Interest in β-$Ga_2O_3$ as the next generation power semiconductor has grown quickly due to its potential in high power switching supported by the high critical field strength about 8 MV/cm as a result of the 4.8 eV bandgap. For low conduction loss, minimizing the on-state resistance ($R_{ON}$) and maximizing operating voltage are key as described by Baliga [121]. The combination of projected breakdown field and mobility gives β-$Ga_2O_3$ a $V_{BK}^2/R_{ON,SP}$ figure of merit (FoM) of 34,000 MW/cm$^2$, where $V_{BK}$ and $R_{ON,SP}$ are breakdown voltage and $R_{ON}$ normalized for device area. β-$Ga_2O_3$ devices with electron mobility values near 100 cm$^2$/Vs at 300 K have been reported in the literature [122, 123]. High blocking voltages approaching 0.75 kV have also be demonstrated [114]. However, due to the very early stage of the development, the advantage of $V_{BK}^2/R_{ON,SP}$ FoM has not been shown. Here, a β-$Ga_2O_3$ metal-oxide semiconductor field effect transistor (MOSFET) with record observed gate-to-drain electric field strength > 3.8 MV/cm ($V_{BK}/L_{GD}$) is

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[3] The content in this chapter is adapted with permission from A. J. Green, K. D. Chabak, E. R. Heller, R. C. Fitch, M. Baldini, A. Fiedler, et al., "3.8-MV/cm breakdown strength of MOVPE-grown Sn-doped β-$Ga_2O_3$ MOSFETs," *IEEE Electron Device Letters,* vol. 37, pp. 902-905, 2016 [116]. Copyright (2016) IEEE

achieved. Although not reaching the theoretical limit, this is the highest field strength measured in a transistor surpassing theoretical bulk critical field strengths for GaN (3 MV/cm) and SiC (3.18 MV/cm).

Sn-doped β-$Ga_2O_3$ was homoepitaxially grown by metalorganic vapor phase epitaxy (MOVPE) on a Mg-doped (100) β-$Ga_2O_3$ single crystal substrate. The substrate was cut from a two-inch boule grown via the Czochralski method [124]. The 200 nm epitaxial layer was doped with Sn donor concentration of 1.7 x $10^{18}$ $cm^{-3}$ measured *by C-V* as-grown [108]. MOSFET fabrication was identical to Section 6.1 and Figure 42. The post-processed carrier concentration was measured via Hall effect to be ~4.8 x $10^{17}$ $cm^{-3}$ after the ohmic contact anneal.

Standard DC *I-V* measurements were made with ground-signal-ground probes on a Cascade automated test station with a slight overpressure of nitrogen. Figure 49 shows transfer characteristics for several MOSFETs taken at $V_{DS}$ = 10 V. The $I_{ON}/I_{OFF}$ ratio was measured as high as $10^7$. The maximum drain current ($I_{DS}$) typically was around 60 mA/mm. Figure 50 shows the DC family of output curves for a MOSFET from $V_{GS}$ = 0 to $V_{GS}$ = −30 V with a gate step of −2 V. Positive gate bias was found to degrade the devices and was therefore avoided. This is consistent with observations of trap assisted tunneling through an $Al_2O_3$ gate dielectric as reported by Hung et al. [125]. The output curves were power limited at 10 mW to avoid thermally induced degradation. The inset of Figure 50 shows gate and drain leakage in the pinch off condition of −30 V on the gate. VDP test structures were used to measure average mobility and sheet resistance values of 19.7 ± 1.5 $cm^2$/Vs and 33 ± 3.7 kΩ/sq via the Hall effect. $R_C$ was calculated to be 16 Ω·mm by subtracting the channel resistance from $R_{ON}$. Three-terminal breakdown

tests were conducted by sweeping $V_{DS}$ up to 200 V with $V_{GS} = -30$ V without catastrophic breakdown. A lower bound on the maximum field strength of 3.8 MV/cm is calculated using a linear electric field gradient approximation for a $V_{GD} = -230$ V potential difference across 0.6 $\mu$m gate-drain separation as verified by cross-sectional SEM. Repeated high-voltage drain sweeps induced catastrophic gate dielectric breakdown as evidenced by orders of magnitude increase in gate current.

This early high critical field strength result can be benchmarked using $R_{ON,SP}$ versus $V_{BK}$ against state-of-the-art Si, GaN, and previous $Ga_2O_3$ results. Plotting $R_{ON,SP}$ versus $V_{BK}$ gives a theoretical BFOM limit for a particular material technology. Here, an $R_{ON,SP}$ of 4.86 m$\Omega \cdot cm^2$ is calculated by normalizing measured $R_{ON}$ (at $V_{GS} = 0$) multiplied by the device area ($L_{SD} \cdot W_G$) according to Amato [126]. The results are plotted for the maximum observed blocking voltage at $V_{GD} = -230$ V in Figure 51 and compared against maximum theoretical power performance for Si, GaN, and β-$Ga_2O_3$. A power figure of merit ($V_{BK}^2$ / $R_{ON,SP}$) of 11 MW/cm$^2$ is calculated from the measured data for our un-optimized device. A roadmap to obtain a BFOM surpassing GaN is indicated in Figure 51.

## 6.4 Top-Down NW $Ga_2O_3$ MOSFET[4]

For power electronics applications, a normally-off transistor is preferred for safe high-voltage operation and to mitigate off-state power dissipation. To achieve high-

[4] The content in this chapter is adapted with permission from K. D. Chabak, N. Moser, A. J. Green, D. E. Walker, S. E. Tetlak, E. Heller, et al., "Enhancement-mode $Ga_2O_3$ wrap-gate fin field-effect transistors on native (100) β-$Ga_2O_3$ substrate with high breakdown voltage," *Applied Physics Letters,* accepted for publication, 2016 [117]. Copyright (2016) AIP Journals

current density, $Ga_2O_3$ MOSFETs require high doping concentration resulting in negative $V_{TH}$. To shift toward positive $V_{TH}$, 3D fin-shaped channels offer enhanced electrostatic control of the channel by depleting it from the side walls without sacrificing doping. Achieving dense, parallel arrays of NW, or fin, channels is most easily achieved by top-down plasma etching though reports of fin channels formed by metal-catalyzed wet-etching [127] and self-assembly [128] are promising to avoid plasma etch damage.

GaN-based 3D devices have been reported with Si-doped GaN junctionless nano-channels and high-electron mobility AlGaN/GaN heterostructure where the gate wraps around the channel with enhanced electrostatics to nearly or fully deplete the channel [12, 80, 129]. However, the main drawbacks for GaN are cost and availability of native substrates for low-defect density homoepitaxial growth. In this section, parallel arrays of Sn-doped $Ga_2O_3$ NW (NW) channels formed by top-down plasma etching to achieve normally-off operation on native (100) semi-insulating $\beta$-$Ga_2O_3$ substrate are presented. The results show feasibility of wrap-gate architecture to shift the $V_{TH}$ to positive values while maintaining volume current densities for consideration in future high-voltage device design.

FinFET devices were fabricated from a 300 nm Sn-doped $Ga_2O_3$ channel grown homoepitaxially by MOVPE on 100 $mm^2$ Mg-doped semi-insulating (100) $\beta$-$Ga_2O_3$ substrate [107, 108, 124]. First, arrays of ~300 nm wide fin channels with a ~900 nm pitch were formed by electron beam lithography followed by 150 nm Cr metal evaporation as the hard mask. A second 200 nm Cr hard mask was superimposed on the fin mask by projection lithography to create bulk mesa contacts for source and drain electrodes. Both Cr layers were etched by inductively coupled plasma (ICP) etching

using $BCl_3$ chemistry [119]. The etch conditions were 120 W reactive ion etching (RIE) power and 300 W coil power with 20 sccm $BCl_3$ and 16 mTorr chamber pressure. The etch selectivity of $Ga_2O_3$:Cr was approximately ~2:1. To sufficiently remove the entire 300 nm channel between fins, an over-etch was required which completely etched the fin Cr mask resulting in triangular-shaped fins. Residual Cr on the source and drain mesas was removed by commercially available Cr wet-etchant. Ohmic contacts consisted of Ti/Al/Ni/Au (20/100/50/50 nm) rapidly annealed for 1 min at 470 °C in nitrogen. A 20 nm $Al_2O_3$ gate dielectric was deposited by atomic layer deposition (ALD) at 250 °C and patterned by fluorine-based RIE to allow for Ni/Au (20/480 nm) interconnects and ~2 $\mu$m long optical gate metal evaporation. Finally, a second 20 nm ALD $Al_2O_3$ layer was deposited and patterned on the sample to passivate the etched $Ga_2O_3$ surfaces between interconnects. The fabrication process is illustrated in Figure 52(a).

The finFET has a centered two-finger gate layout with each gate finger wrapping along 48 fins. The total source to drain distance ($L_{SD}$) is ~4 $\mu$m, and the fin-array spans approximately ~3 $\mu$m of this source-drain distance. A tilted SEM image of the NW channel array with wrap-gate and bulk-like ohmic contacts is shown in Figure 52(b). The sidewall morphology appears relatively smooth as previously observed using high-power ICP plasma etching with $BCl_3$ [119]. A representative cross-sectional SEM image of three NWs is shown in Figure 53(a). The darker contrast observed in the NW core compared to the substrate is indicative of the Sn-doped channel and adequate NW electrical isolation. Figure 53(b) depicts the fins are approximately ~300 nm at the base with tapered sidewalls joining at ~200 nm thickness. The 20 nm $Al_2O_3$ gate dielectric and Ni/Au gate metal conform to the fin on all sides.

The mobility and doping concentration of the fins were measured from on-wafer VDP test structures and device $C$-$V$ measurements. It is widely reported that ionized donor concentration, $N_D$, can vary significantly from the chemical Sn-doping concentration [108, 116]. The $R_{SH}$ and electron mobility $\mu$ were measured on a VDP structure near the reported device as ~40 kΩ/sq and ~24 $cm^2$/Vs, respectively. We observed the larger geometry of the Cr mask used for the VDP mesa etched slower compared to the Cr fin-array mask; therefore, the VDP mesa was protected during the fin-array definition process. A forward and reverse $C$-$V$ measurement of the finFET is shown in Figure 54 indicating ~0.8 V of hysteresis which has been previously reported as mobile border traps in accumulation [130]. In the inset, an $N_D$ ~ 2.3 x $10^{17}$ $cm^{-3}$ was extracted from the linear region of $1/C^2$ as a function of $V_{GS}$. The area was estimated as $L_G \cdot W_{fin} \cdot N_{fin}$ where $W_{fin}$ is ~200 nm after considering a ~70 nm backside depletion width and using a 3:2 width-to-height triangular fin cross-section. Finally, the flat-band capacitance, $C_{FB}$, can be calculated by the measured oxide capacitance ($C_{ox}$ ~ 225 fF) in series with the semiconductor capacitance ($C_S$) [131]. The corresponding forward and reverse sweep flat-band voltage, $V_{FB}$, is 1.3 V and 2.1 V, respectively.

In the absence of accurate models for $Ga_2O_3$, one-dimensional analytical expressions were used to estimate the $W_d$ on the two sides and bottom facet of the Sn-doped fins. The partial depletion width of the sides in the ungated region can be estimated by the built-in energy potential ($V_{bi}$) using the energy band lineup at the $Al_2O_3/Ga_2O_3$ interface [12]:

$$E_G^{Al2O3} = E_{VBM}^{Al2O3} + \Delta E_C + \left(E_C^{Ga_2 0_3} - E_F\right) + V_{bi} \qquad \text{(V)} \qquad (31)$$

where $E_G$, $\Delta E_C$ and $E_{VBM}$ are the bandgap, conduction band offset and valence band maximum with respect to the $Ga_2O_3$ Fermi level energy ($E_F$), respectively. $V_{bi(ug)}$ represents band-bending in the ungated $Ga_2O_3$ due to the presence of interface traps. Kamimura et al. reported on the $Al_2O_3/Ga_2O_3$ interface with $E_G$ ~ 6.8 eV, $\Delta E_C$ ~ 1.5 – 1.7 eV [125, 130], and $E_{VBM}$ ~ 3.8 eV [130] using XPS measurements. For $N_D \sim 2.3 \times 10^{17}$ $cm^{-3}$ the semiconductor $E_C - E_F$ energy difference can be expressed from equation (30) This analysis shows $E_C - E_F$ is ~ 73 meV and leaves a non-negligible $V_{bi(ug)}$ ~ 1.4 eV which may be related to interface traps and/or pinning which is neither well-understood nor reported.

A similar study of GaN finFETs deduced a $V_{bi}$ ~ 0.74 eV in the ungated region and was explained by $Al_2O_3/Ga_2O_3$ interfacial chemistry by XPS [12, 132]. Furthermore, in the gated region, the band-bending can increase an additional ~1.15 eV due to the difference in metal work functions of Ni ($\Phi_m$ = 5.15 eV) and $Ga_2O_3$ ($\Phi_S = \chi_s + E_C - E_F$ ) [12] where $\chi_s$ is the electron affinity of $Ga_2O_3$ (~3.5-4.0 V) [125, 133]. However, this does not consider trap-assisted tunneling for thin $Al_2O_3$ gate oxide [125], and it remains unclear how the $V_{bi(ug)}$ compensates for the band-bending normally induced by a gate contact without thorough XPS characterization of our particular interface. For a simple case, however, where both energy barriers are combined in the gated region, the $V_{bi(g)}$ is ~2.5 V which is reasonably close to the measured reverse sweep $V_{FB}$. The maximum depletion width, $W_d$, for each region is calculated by:

$$W_d = \sqrt{\frac{2\varepsilon_o \varepsilon_S V_{bi(ug,g)}}{qN_D}} \quad \text{(nm)} \qquad (32)$$

where $\varepsilon_o$ and $\varepsilon_S$ are the permittivity of free space and $Ga_2O_3$ dielectric constant, respectively. This yields $W_d$ ~ 83 nm and ~110 nm in the ungated and gated regions, respectively. A backside depletion width from the semi-insulating substrate is found to be ~70 nm assuming a mid-gap interface trap density of ~2 x $10^{17}$ $cm^{-3}$ [116, 134]. Therefore, we estimate an undepleted fin with approximately ~26 nm (base) x ~17 nm (height) in the ungated region contributes to the volume conduction mechanism in the finFET. In contrast, the depletion from the sides and substrate fully deplete the fin dimensions in the gated region to realize normally-off operation. It should be noted that once $V_{GS} > V_{FB}$, the finFET is operating in accumulation similar to 3D normally-off junctionless GaN finFETs [12, 135].

Figure 55(a) shows the family of $I_D - V_D$ curves from $V_{GS}$ = +4 V to 0 V. At $V_{GS}$ = +4 V, the on-current ($I_{ON}$) reaches ~3.5 $\mu$A. An upper bound on expected current in the partially depleted fin-arrays can be approximated by the open channel current density ($J_n$) where $V_{DS} < |V_{GS} - V_{TH}|$ using the drift current equation:

$$J_n = q\mu N_D E_{CH} \qquad \text{(kA/cm}^2\text{)} \qquad (33)$$

where $E_{CH} = V_{DS} / L_{CH}$ is the potential across the source-drain channel ($L_{CH}$). Using the partially depleted fin-array cross-sectional area at $V_{DS}$ = 2 V and $L_{CH}$ = 3 $\mu$m, $J_n$ = 5.9 kA/cm$^2$ or $I_D \approx$ 1.3 $\mu$A which is close to the measured value in Figure 55(a). For comparison, this simple analysis is also in agreement at $V_{DS}$ = 1 V ($I_{DS}$ = 0.55 mA) for the planar Sn-doped $Ga_2O_3$ MOSFET reported by Green et al. using the surface and substrate depletion widths with the reported $N_D$ and Ti/Au gate [116]. The gate width, $W_G = W_{fin} \cdot N_{fin}$, is ~19 $\mu$m corresponding to an $I_{ON}$ ~ 0.18 $\mu$A/$\mu$m. The low $I_{ON}$ is a main limitation of the fin-array topology reported here, but can be drastically improved in the

future with higher-mobility materials and $R_{ON}$ optimization. For this device, the gate swing was limited by the conduction band offset of $Al_2O_3/Ga_2O_3$ which can be improved with, for example, ALD $SiO_2$ [136]. The gate leakage characteristics are shown in Figure 55(b) and indicates ultra-low gate leakage near $10^{-12}$ Amps before an onset of trap-assisted tunneling at forward bias appears [125].

Figure 55(c) shows the $I_D$-$V_G$ characteristics at $V_{DS}$ = 10 V. Despite $I_{ON}$ limitations, the NW-MOSFET has > $10^5$ $I_{ON}/I_{OFF}$ ratio. The device reaches an off-state approaching $10^{-12}$ amps between 0 to +1 $V_{GS}$ indicating enhancement-mode operation. To rule out parasitic conduction in the substrate between fins, an identical MOSFET with the epitaxial channel etched away was fabricated and shows minimal modulation of the remaining etched SI substrate. We attribute this parasitic modulation to uncompensated free carriers in the substrate being accumulated at the $Al_2O_3$/SI-$Ga_2O_3$ interface. The forward and reverse sweeps reveal trapping effects that may be a combination of the unoptimized $Al_2O_3/Ga_2O_3$ interface and density of interface traps ($D_{it}$) caused by the plasma etching of the fin side walls. Despite no surface treatment optimization, the subthreshold slope ($SS$) is 158 mV/dec which is superior to previously reported $Ga_2O_3$ MOSFETs. The $D_{it}$ can be estimated by the shift in forward and reverse $V_{FB}$ from Figure 54 using the following expression:

$$D_{it} = \frac{C_{ox}\Delta V_{FB}}{qE_G^{Ga_2O_3}} \qquad (\text{cm}^{-2}\text{eV}^{-1}) \qquad (34)$$

which is approximately ~3.9 x $10^{11}$ $\text{cm}^{-2}$ $\text{eV}^{-1}$ where $C_{ox}$ ~ 3.8 fF/$\mu\text{m}^2$. The area for $C_{ox}$ is calculated using the measured $C_{ox}$, 20 nm thickness and a gate dielectric constant of 8.5; though, estimating the area using the sum of the fin side facets multiplied by $L_G$ gives nearly the same value. This $D_{it}$ value is similar to previously reported $Al_2O_3/Ga_2O_3$ and

$SiO_2/Ga_2O_3$ MOS capacitors on (-201) $n^+$ $\beta$-$Ga_2O_3$ substrates with $D_{it} < 1.0 \times 10^{12}$ $cm^{-2}$ $eV^{-1}$ after surface treatment optimization [136, 137]. The effect of surface plane orientation in the triangular sidewall facets on the dielectric-$Ga_2O_3$ interface quality is unclear and requires further investigation.

NW-MOSFET high-voltage operation on wider devices with $L_{GD}$ = 16 $\mu$m and 21 $\mu$m was characterized with an Agilent B1505A on a Cascade Tesla probe station. At $V_{GS}$ = 0 V, the $I_{DS}$ is < $10^{-7}$ Amps until a breakdown voltage ($V_{BK}$) is reached. For each $L_{GD}$, a $V_{TH}$ = +0.8 is measured at $V_{DS}$ = 10 V which is shown by the inset of Figure 56. It should be noted the on-current for large $L_{GD}$ devices have extremely high on-resistance and do not saturate at $V_{DS}$ = 10 V. At $V_{GS}$ = 0 V, a $V_{BK}$ was measured at 567 and 612 V for $L_{GD}$ = 16 and 21 $\mu$m, respectively. As indicated in Figure 56, $V_{BK}$ is destructive and limited by peak electric fields in the gate oxide.

To conclude, the first enhancement-mode $Ga_2O_3$ MOSFET enabled by a wrap-gate Sn-doped NW array on semi-insulating $\beta$-$Ga_2O_3$ substrate was fabricated. A $V_{BK}$ exceeding 600 V at $V_{GS}$ = 0 V off-state was demonstrated and represents the highest breakdown voltage measured without field-plate for $\beta$-$Ga_2O_3$ transistors. This is also the highest breakdown for any transistor technology utilizing 3D device channels [12, 80, 81, 129, 138, 139]. Future work includes understanding the role of traps at the dielectric-$Ga_2O_3$ interface and optimizing on-resistance by reducing the NW channel length and using highly doped ohmic cap layer.

## 6.5 Figures and Tables

**Table 5**: Sn-Doped $Ga_2O_3$ Homoepitaxial Sample Set

| Sample ID | Epitaxy Thickness (nm) | Sn-concentration ($cm^{-3}$) | Substrate | Purpose |
|---|---|---|---|---|
| 200-1 | 200 | $7.9 \times 10^{17}$ | S.I. (100) $Ga_2O_3$ | Doping Study |
| 200-2A | 200 | $1.3 \times 10^{18}$ | S.I. (100) $Ga_2O_3$ | Doping Study |
| 200-3 | 200 | $1.7 \times 10^{18}$ | S.I. (100) $Ga_2O_3$ | Doping Study |
| 150-1 | 150 | $1.4 \times 10^{18}$ | S.I. (100) $Ga_2O_3$ | Thickness Study |
| 200-2B | 200 | $1.3 \times 10^{18}$ | S.I. (100) $Ga_2O_3$ | Thickness Study |
| 300-1 | 300 | $1.0 \times 10^{18}$ | S.I. (100) $Ga_2O_3$ | Thickness Study |
| 300-2 | 300 | $1.0 \times 10^{18}$ | S.I. (100) $Ga_2O_3$ | 3D Channel |

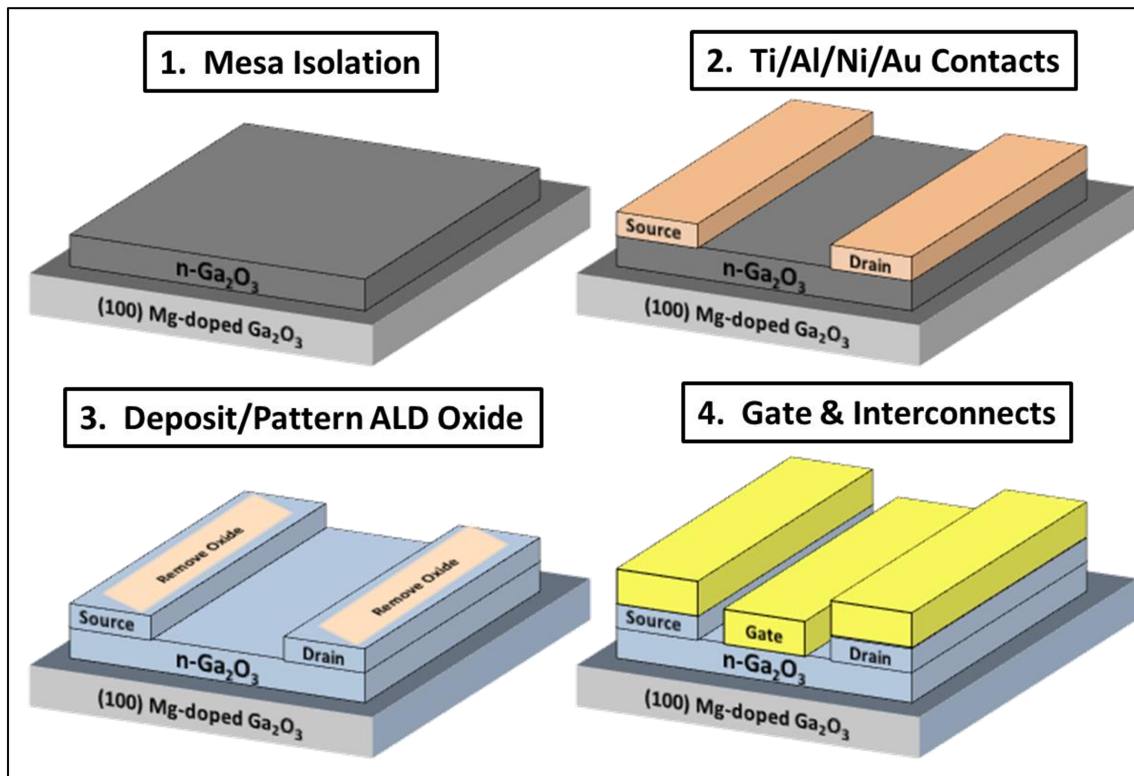



**Figure 42**: Fabrication process for $Ga_2O_3$ planar MOSFET devices.

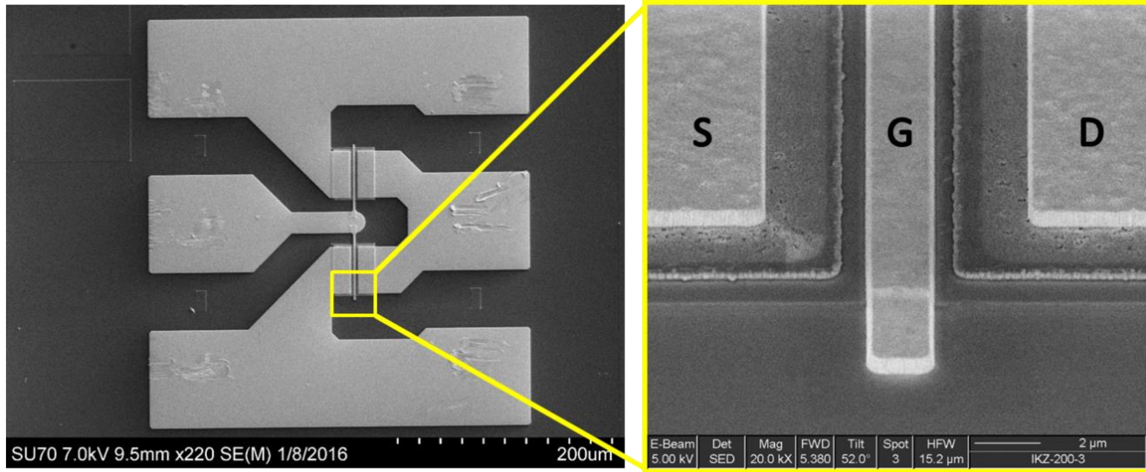



**Figure 43**: (left) SEM of representative two-finger $Ga_2O_3$ MOSFET with $W_G/L_G$ = 100 $\mu$m/2 $\mu$m and centered gate with $L_{SD}$ = 3 $\mu$m. (right) A magnified tilted SEM view of the source, gate and drain terminals.

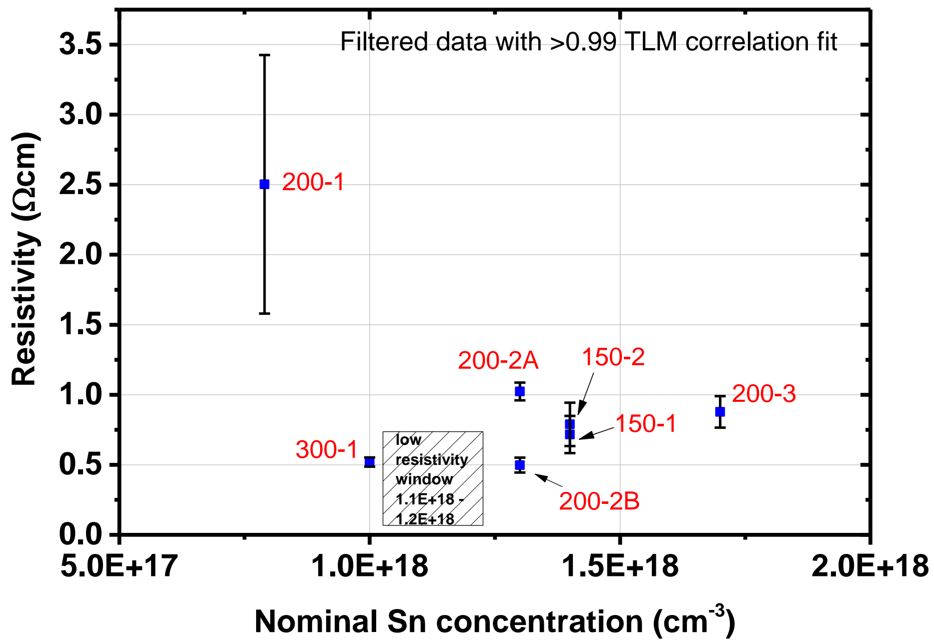



**Figure 44**: Sn-doped $Ga_2O_3$ resistivity versus chemical Sn concentration. An optimum window for doping concentration was identified in the ~1.0 – 1.1 x $10^{18}$ $cm^{-3}$.

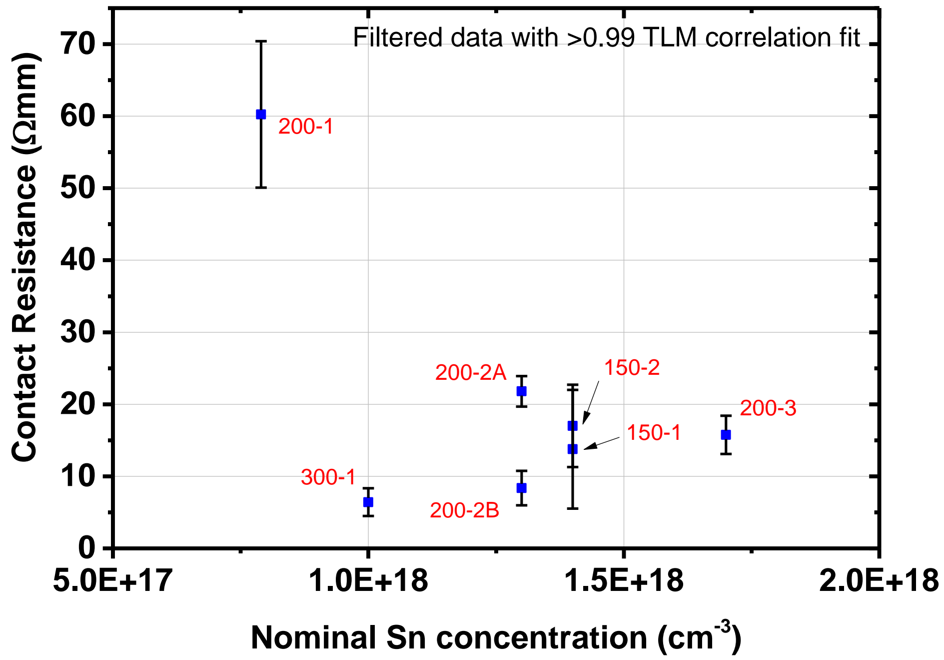



**Figure 45**: Sn-doped $Ga_2O_3$ contact resistance versus chemical Sn concentration.

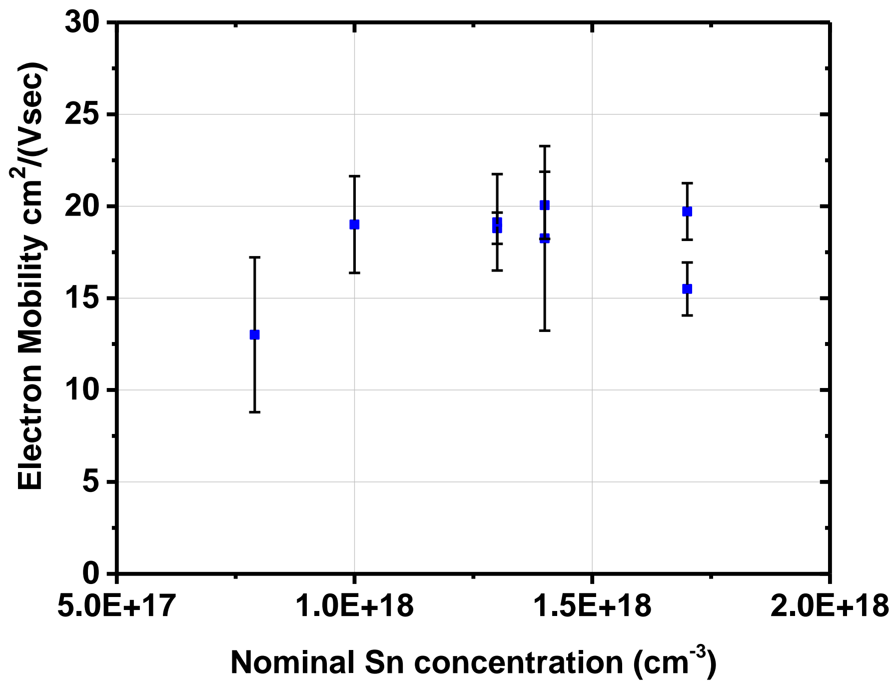



**Figure 46**: Sn-doped $Ga_2O_3$ electron mobility measured by Hall effect test structures versus chemical Sn concentration.

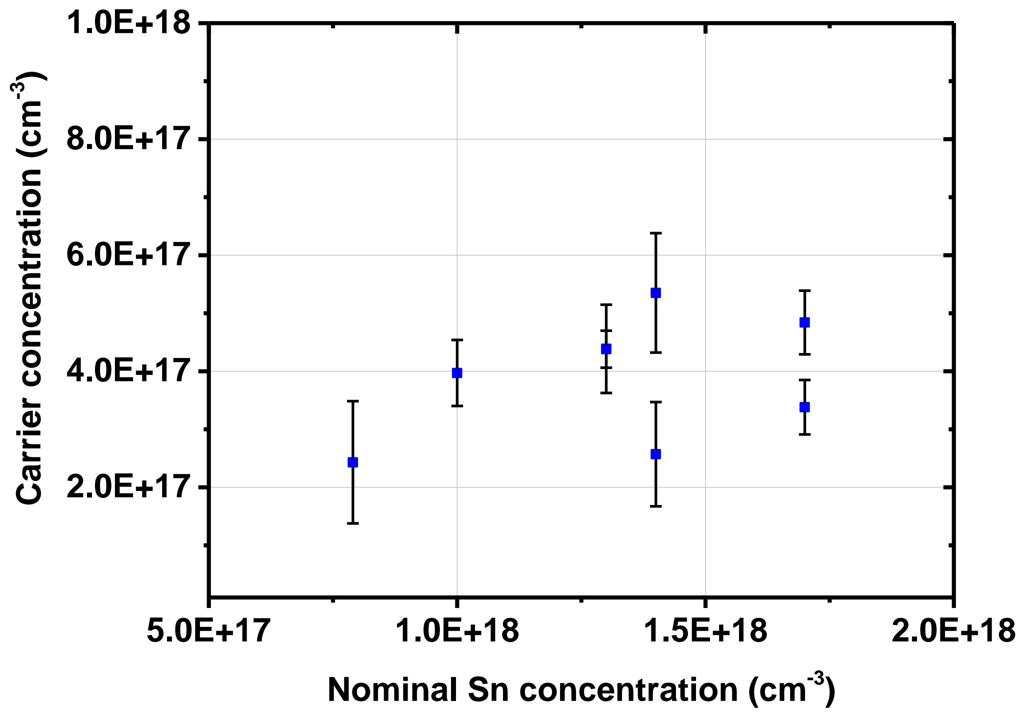



**Figure 47**: Sn-doped $Ga_2O_3$ $N_D$ calculated by Hall effect test structures versus chemical Sn concentration.

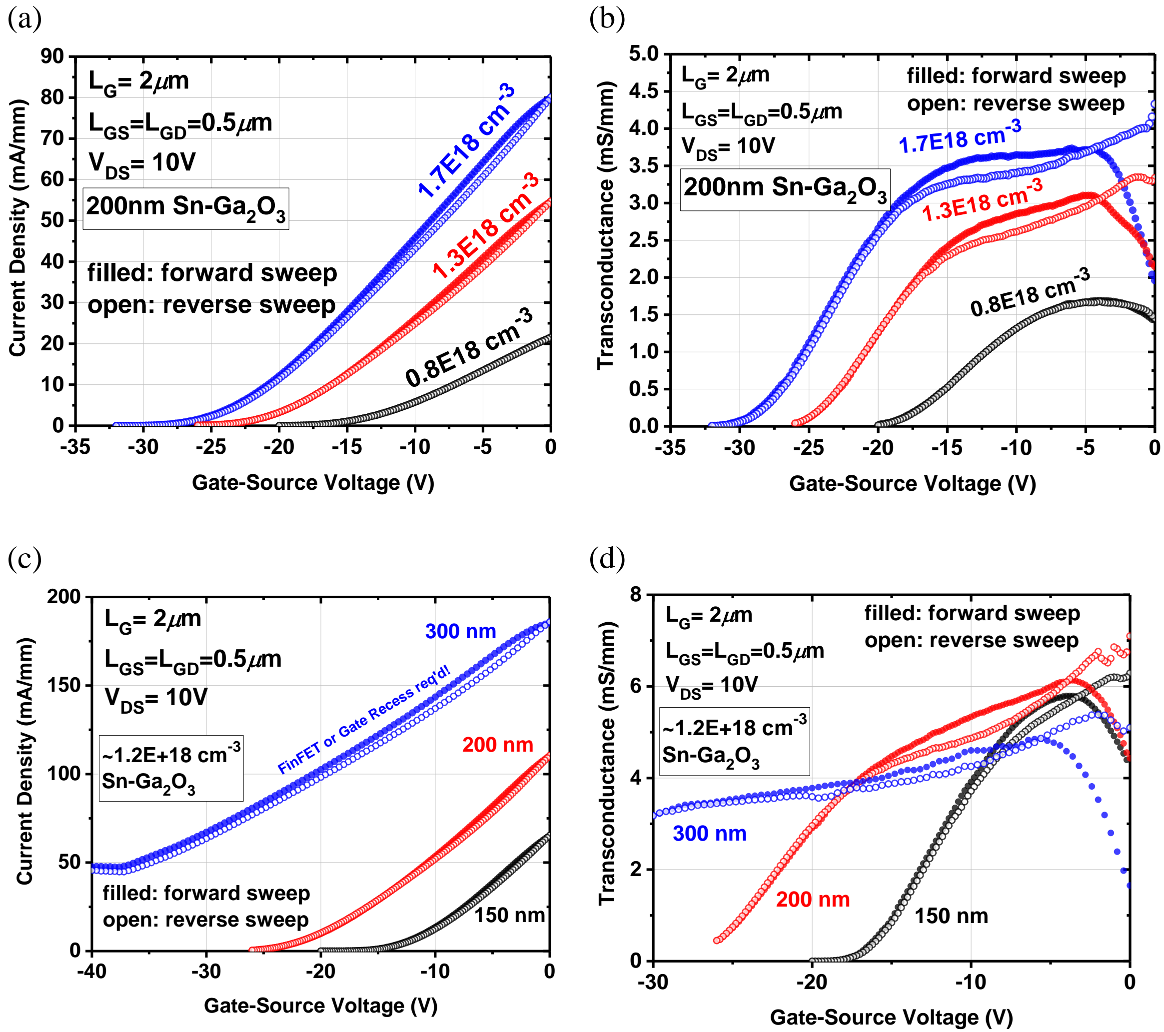



**Figure 48**: (a) $I_{DS}$ vs. $V_{GS}$ and (b) $g_M$ vs. $V_{GS}$ for 2 x 50 $\mu$m 200 nm Sn-doped $Ga_2O_3$ MOSFETs with varied Sn concentration. (c) $I_{DS}$ vs. $V_{GS}$ and (b) $g_M$ vs. $V_{GS}$ for 2 x 50 $\mu$m ~ 1.2 x $10^{18}$ $cm^{-3}$ Sn-doped $Ga_2O_3$ MOSFETs with varied channel thickness.

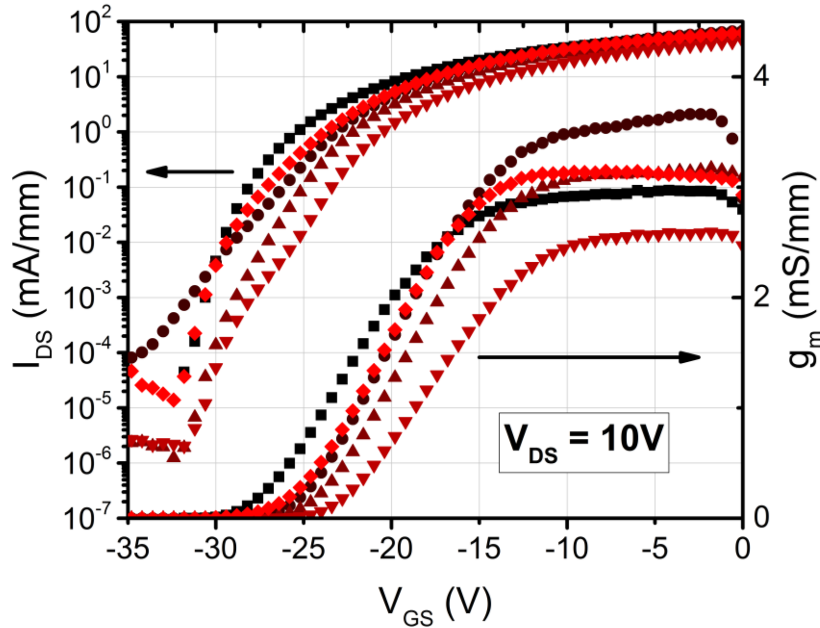



**Figure 49**: $I_{DS}$ vs. $V_{GS}$ transfer characteristics for multiple 2 x 50 $\mu$m 200 nm Sn-doped $Ga_2O_3$ MOSFETs with $N_D$ ~ 4.7 x $10^{17}$ $cm^{-3}$, $L_G = 2$ $\mu$m and $L_{SD} = 3$ $\mu$m.

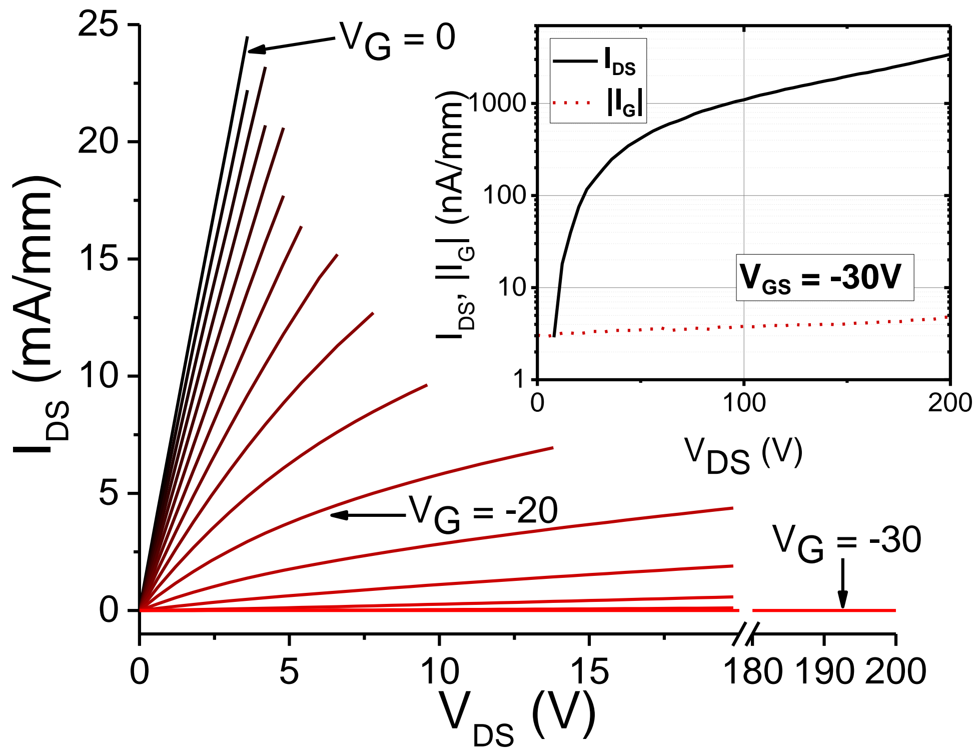



**Figure 50**: $I_{DS}$ vs. $V_{DS}$ for 2x 50 $\mu$m 200-nm Sn-doped $Ga_2O_3$ MOSFET with $N_D$ ~ 4.7 x $10^{18}$ $cm^{-3}$, $L_G = 2$ $\mu$m and $L_{SD} = 3$ $\mu$m. The inset shows log drain and gate current in pinch-off condition to a maximum 200 $V_{DS}$.

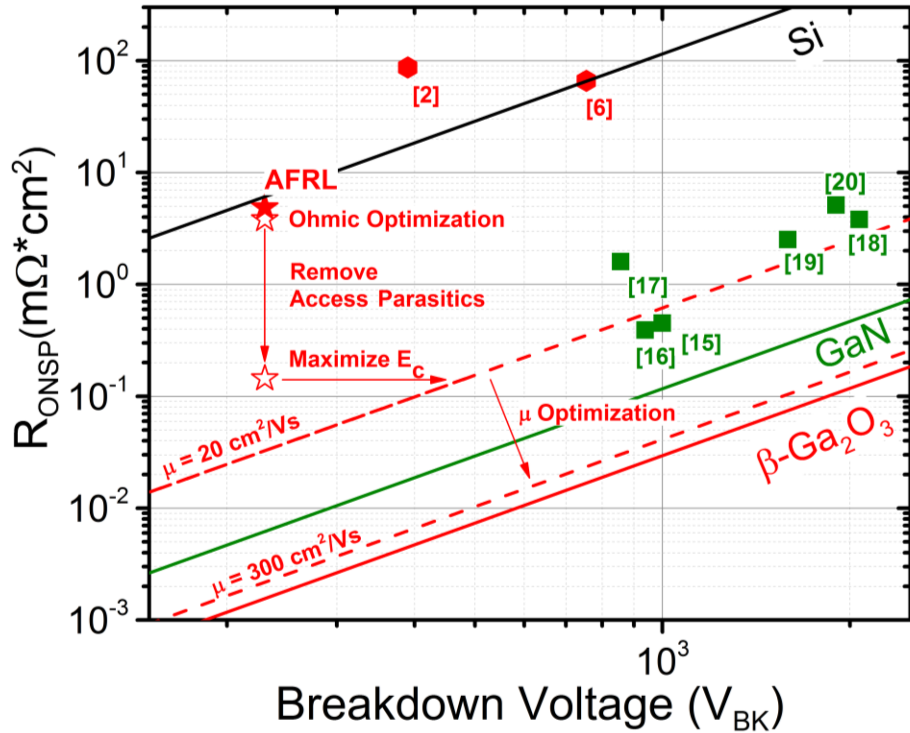
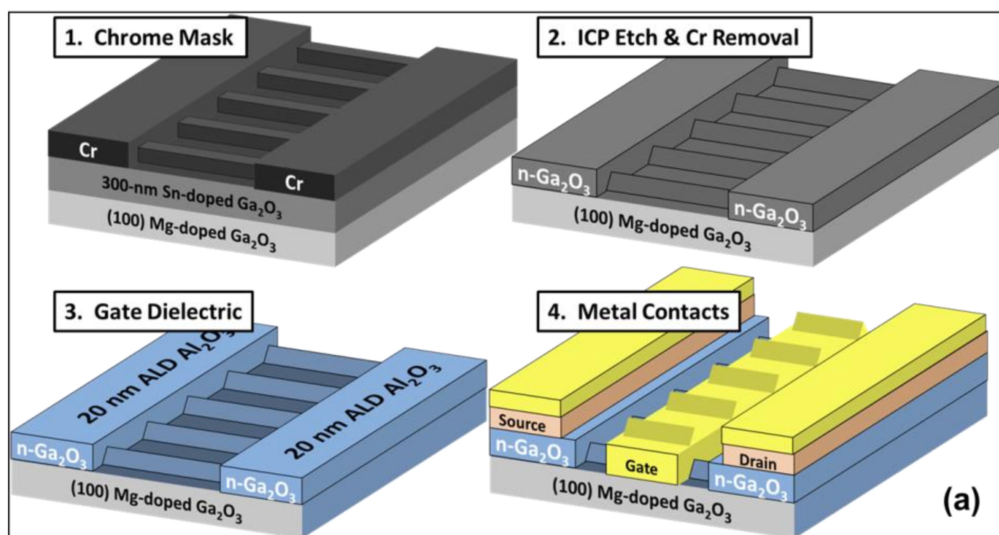



**Figure 51**: Theoretical limits for $R_{ONSP}$ vs. $V_{BK}$ for Si, GaN, and β-$Ga_2O_3$. The filled red star represents this work. The open stars are projections based on layout adjustments and optimization of $R_C$ and $E_{crit}$. The dashed lines represent BFOMs for a given mobility. If the mobility reaches bulk values in the low doping limit, the second dashed line would be reached. The green squares are state-of-the-art lateral GaN devices [140-145]. Performance improvements are achievable through contact and on-resistance reduction to achieve the top open stars. Further optimization is expected through realization of the full 8 MV/cm critical field strength of β- $Ga_2O_3$ compared to our experimentally observed 3.8 MV/cm. In this case, a $V_{BK}^2/R_{ONSP}$ of 1,600 MW/cm$^2$ could be realized (top dashed line). Optimization of the mobility toward the projected bulk mobility of 300 cm$^2$/Vs will increase the figure of merit to 24,000 MW/cm$^2$ (bottom dashed line). The discrepancy between the bottom dashed line and theoretical limit arise from the finite contact resistance assumption used and not operating the reported device at positive $V_{GS}$ to achieve minimum $R_{ON}$.



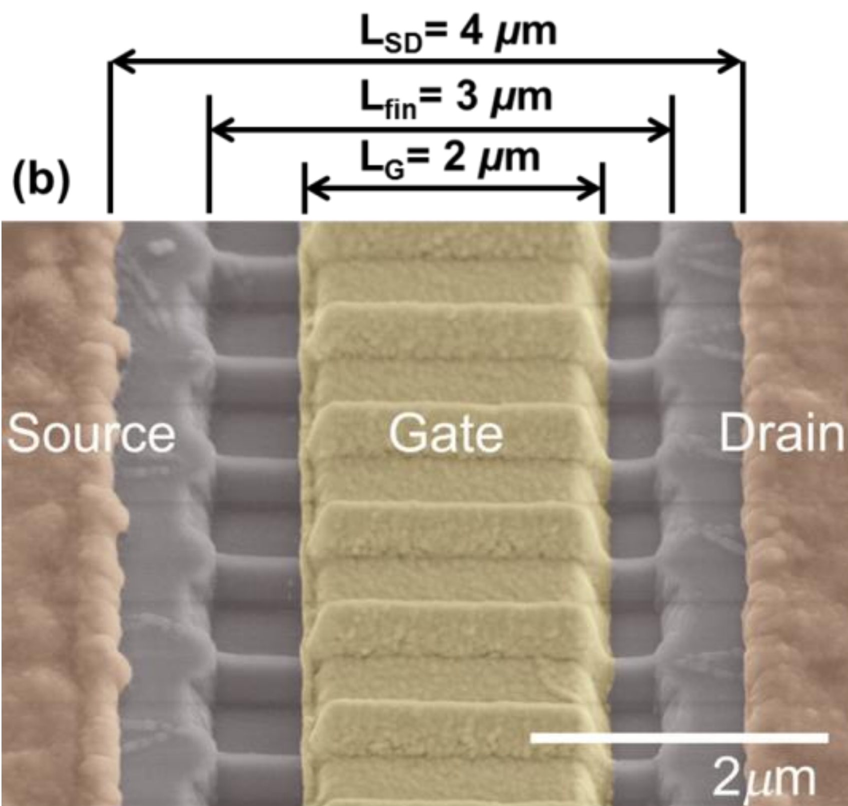




**Figure 52:** (a) Fabrication process for enhancement-mode $Ga_2O_3$ NW-MOSFETs and (b) tilted SEM image of a $L_{SD}$ = 4 $\mu$m MOSFET depicting the geometry of $Ga_2O_3$ NW channels and contacts.

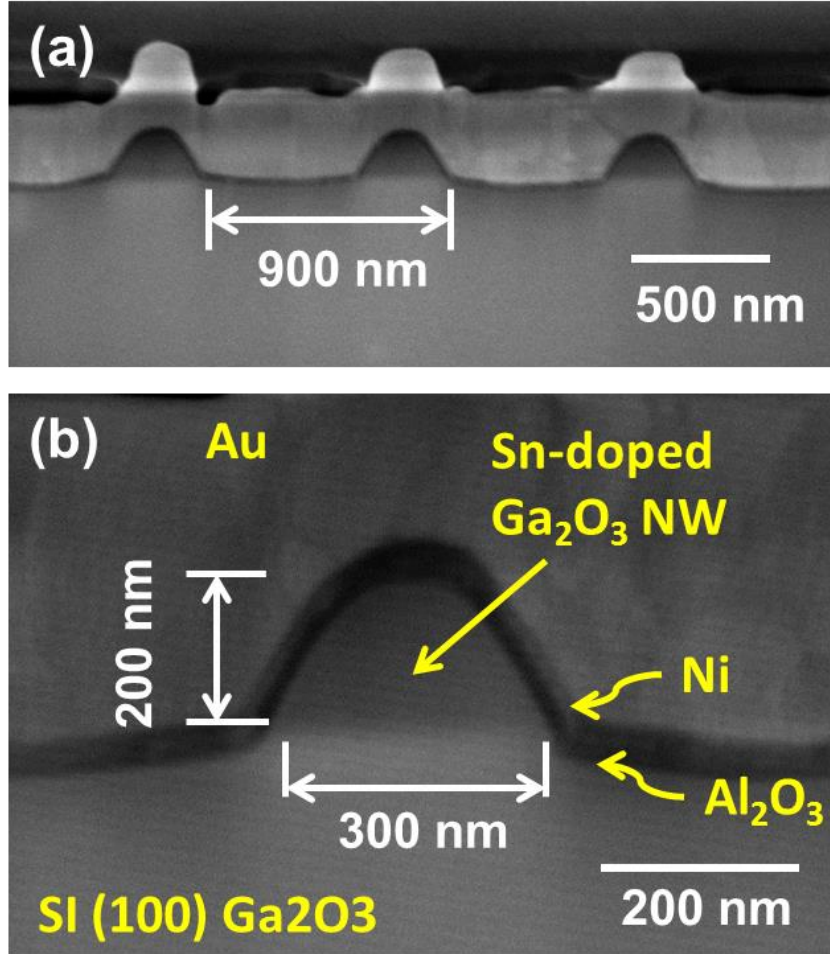



**Figure 53**: (a) SEM cross-section image of three $Ga_2O_3$ NWs formed by FIB milling and (b) high magnification SEM image of one $Ga_2O_3$ NW channel with associated dimensions.

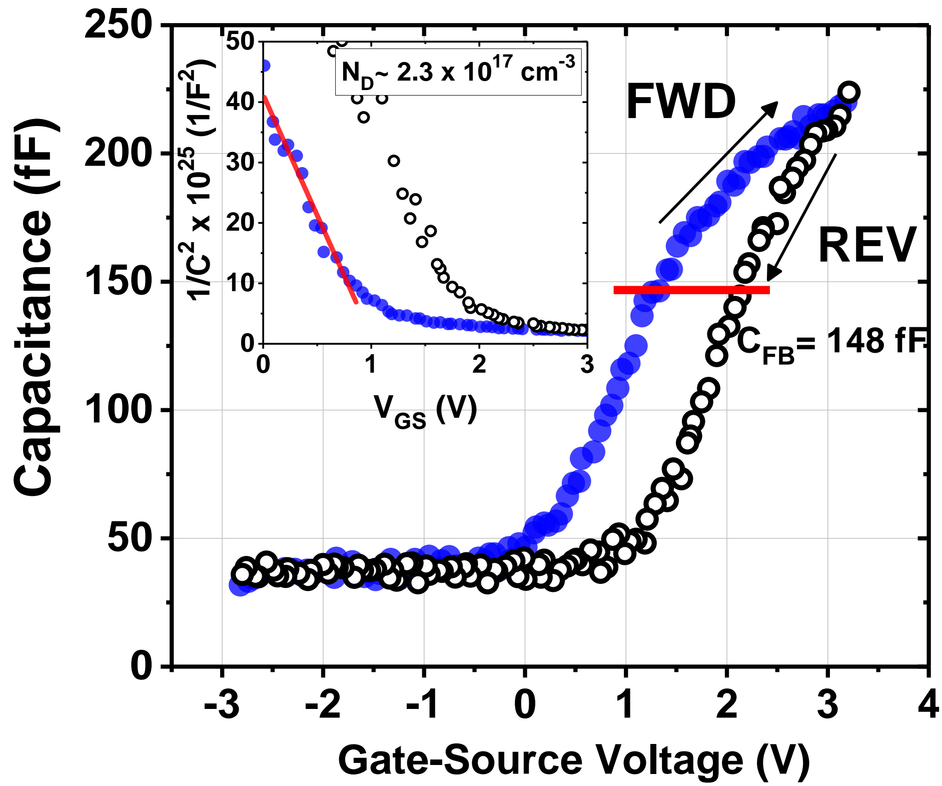



**Figure 54**: Forward and reverse $C$ - $V_{GS}$ sweep of the finFET indicating the calculated flat band and oxide capacitance; and, (inset) $C^{-2}$ - $V_{GS}$ characteristics to extract carrier concentration.

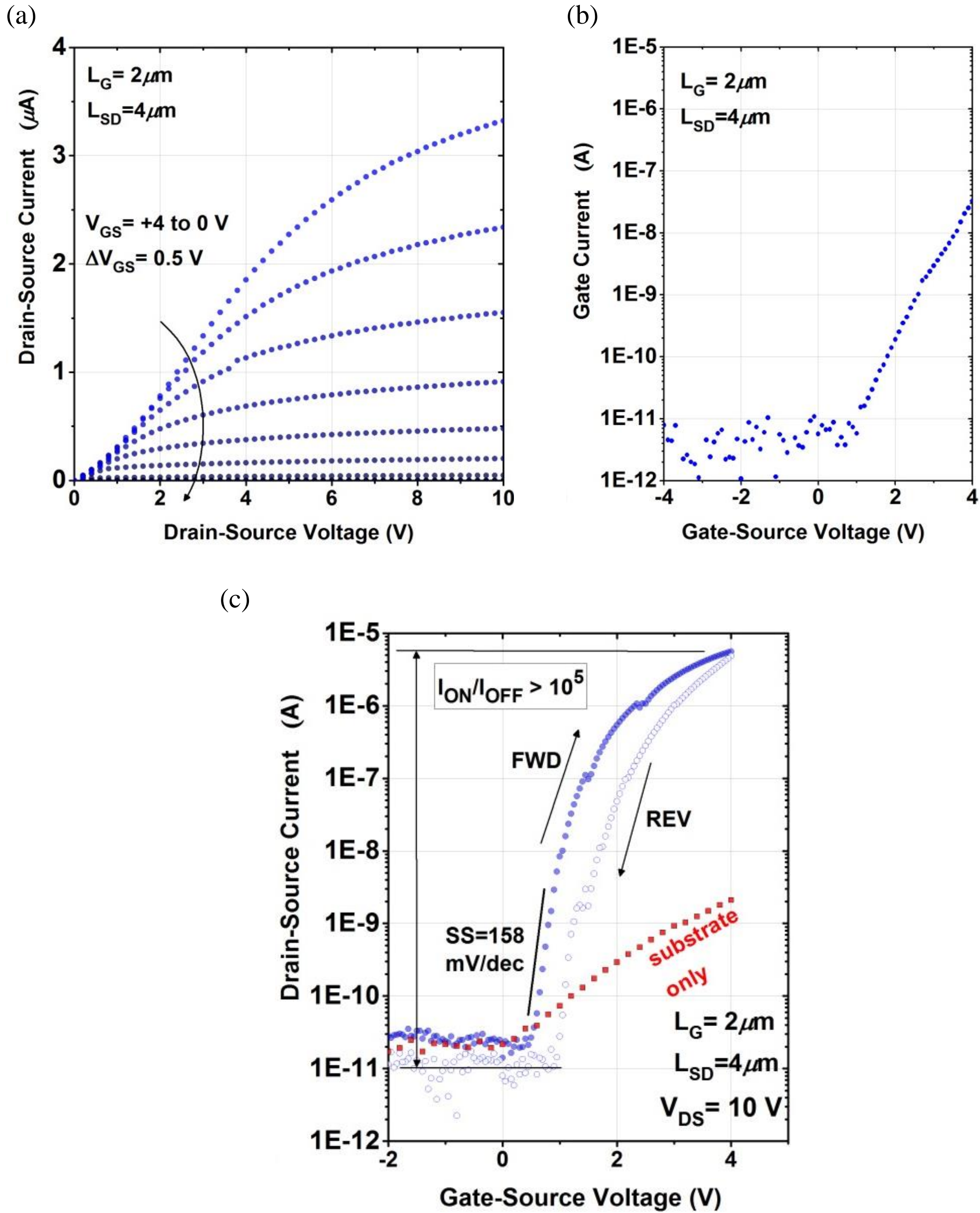



**Figure 55**: (a) $I_D$-$V_D$ family of output curves from $V_{GS}$ = +4 to 0 V; (b) Two-terminal log($I_G$) - $V_G$ gate leakage performance from off-to-on state; and, (c) log($I_D$) - $V_G$ forward and reverse sweeps indicating enhancement mode operation. An identical device without NWs is included to illustrate the effect of parasitic substrate conduction.

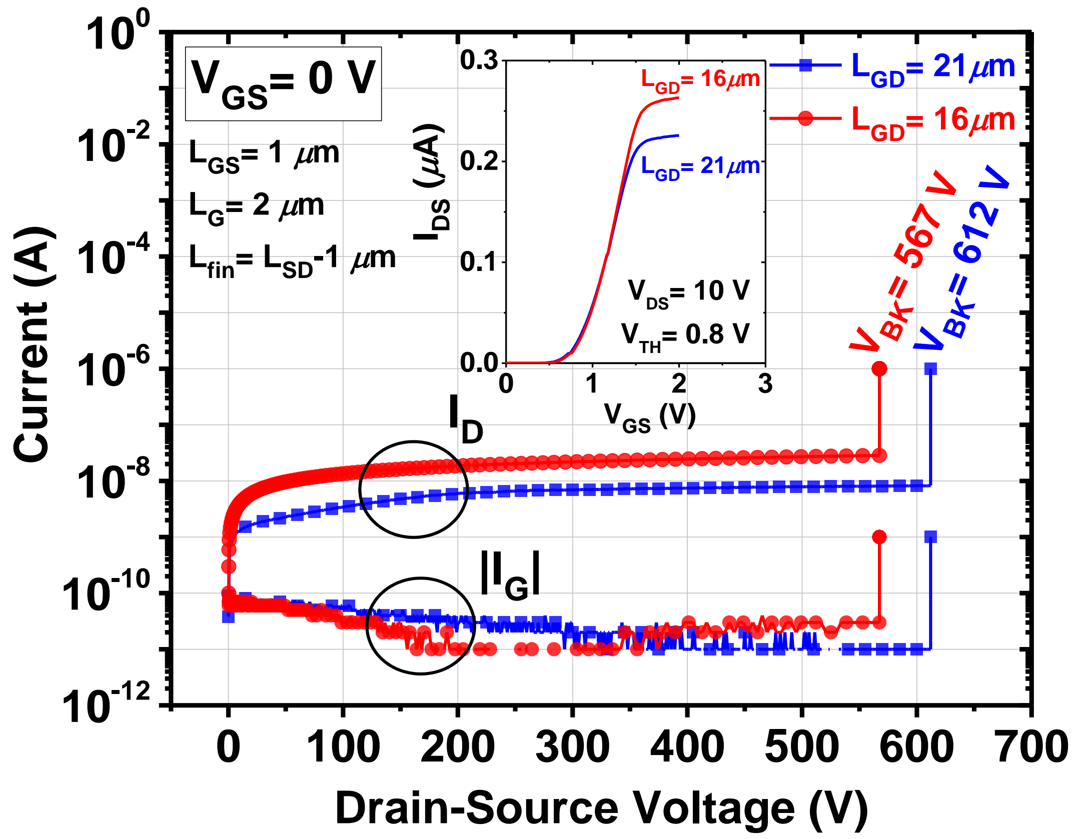



**Figure 56**: Breakdown voltages of $Ga_2O_3$ MOSFETs with $L_G$ = 2 μm and $L_{GD}$ = 16, 21 μm while biased in the off-state at $V_{GS}$ = 0 V. The inset shows the transfer characteristics of the same device indicating a $V_{TH}$ = +0.8 V.

# 7. CONCLUSIONS AND FUTURE WORK

## 7.1 Research Achievements

This research dissertation has achieved breakthrough dc and RF device performance using bottom-up GaAs NWs and top-down $Ga_2O_3$ NW-arrays as novel transistor channels. The following achievements have been made in this dissertation:

**Bottom-up GaAs NWs by lateral VLS epitaxy**

1. Wafer-scale AlGaAs/GaAs NW-array HEMTs with excellent dc and RF performance. An $f_{max}$ > 75 GHz with < 2 V supply voltage and $I_{ON}/I_{OFF} > 10^4$ was measured which is superior compared to carbon-based nanoelectronics and "spin-on III-V NWs".
2. A comprehensive small-signal model was used to extract the contributing and limiting factors to the RF performance of AlGaAs/GaAs NW-array transistors and predict future performance.
3. A process was developed to show III-V NWs on sacrificial epitaxial templates can be transferred to arbitrary substrates.

**Toward top-down $Ga_2O_3$ NWs by plasmas etching**

4. Doping and thickness study to understand effects of Sn-doping on the electrical characteristics of $Ga_2O_3$ MOSFETs.
5. Exploring high critical field strength potential of $Ga_2O_3$ revealed record-high measured critical field strength (3.8 MV/cm) and surpassing GaN and SiC.

6. $Ga_2O_3$ NW-MOSFET fabricated by $BCl_3$ plasma etching. A new wrap-gate transistor demonstrated normally-off (enhancement-mode) operation with a high breakdown voltage exceeding 600 V which is superior to any transistor using a similar 3D channel.

## 7.2 Future Work

While state-of-the-art electrical performance was reported in this dissertation using NW-array transistor channels, there is significant room for improvement. The following sections list ideas to consider continued research in this area.

### 7.2.1 Bottom-Up III-V Planar NW-Arrays

In this research effort, the planar III-V NWs were epitaxially attached to the III-V substrate. However, one must keep in mind that as long as the III-V substrate is attached, it will have marginal improvement, if any, when compared to conventional thin-film III-V epitaxy. Therefore, establishing methods to heterogeneously integrate III-V NWs must be the priority. The transferring of III-V NWs in this effort was one step toward that goal. However, ultimately, one should explore how to monolithically integrate NWs on, for example, silicon substrates. Consider the case where the n-type As-based NWs could assemble bottom-up; then cover them with $SiO_2$; finally, proceed with the p-type Sb-based NW growth to realize a high-speed CMOS platform. Alternatively, if pursuing the mechanical transferring, one should integrate them onto flexible substrates for conformal

electronics (wearable, electronic skin, etc.). Characterizing NW transistors as a function of bending radius and stress would be a valuable contribution to the literature.

### 7.2.2 Top-Down $Ga_2O_3$ NW-Arrays

The performance of top-down $Ga_2O_3$ requires higher-mobility materials and on-resistance optimization. Toward the end of this research, our collaborator at IKZ-Berlin reported nearly 4x higher mobility films when doped with silicon on (010) $\beta$-$Ga_2O_3$ substrate (vs. Sn-doped (100) substrate in this research). Additionally, a thin ohmic capping layer degenerately doped with silicon was successfully demonstrated to have $< 1$ $\Omega \cdot$mm ohmic contact resistance (nearly 20x less than reported in this work). However, this layer must be etched away underneath the gate metal similar to the epitaxial design for homoepitaxial GaAs MESFETs.

The effect of dry etching $Ga_2O_3$ has not been well characterized. If available, detailed surface analysis using XPS should be investigated to fully understand energy barriers related to the oxide/semiconductor interface after an etching process. Likewise, C-V measurements of a matrix of designs varying dielectric material, anneal temperature and surface treatment could provide invaluable information for device engineers and present several publication opportunities.

Finally, sub-micron gate-length scaling in conjunction with a gate recess and the above on-resistance optimization should easily reach X-band range RF frequencies. So far, no reports of small-signal gain have been reported, but it appears the materials are now ready for the first RF demonstration. This would be an interesting device

technology that could combine high-voltage switching and RF amplifiers in a cost-effective monolithically microwave integrated circuit process.

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# APPENDIX A. NANOSCALE RF TRANSISTOR TABLES

**Table 6**: State-of-the-Art Carbon Nanotube-Array RF Devices

| Year | Ref. | Group | Channel | $L_G$ (nm) | $f_T$ (GHz) | $f_{max}$ (GHz) | Substrate | Direction, Assembly, Alignment |
|---|---|---|---|---|---|---|---|---|
| 2013 | [46] | USC | SW-CNTs | 100 | 102 | 9 | quartz | CVD catalyzed |
| 2012 | [47] | IBM | CNTs | 100 | 153 | 30 | $SiO_2$/Si | dielectrophoresis |
| 2009 | [48] | IEMN | SW-CNTs | 300 | 80 | 3 | silicon | spin-on film |

**Table 7**: State-of-the-Art 2D Nanosheet RF Devices

| Year | Ref. | Group | Title | Channel | $L_G$ (nm) | $f_T$ (GHz) | $f_{max}$ (GHz) | Substrate |
|---|---|---|---|---|---|---|---|---|
| 2012 | [34] | GA Tech | Record maximum oscillation frequency in C-face epitaxial graphene transistors | graphene | 100 | 110 | 70 | SiC |
| 2012 | [33] | UCLA | High-frequency self-aligned graphene transistors with transferred gate stacks | graphene | 46 | 212 | 8 | glass |
| | | | | | 220 | 60 | 29 | glass |
| 2012 | [35] | UTA | 25 GHz embedded-gate graphene transistors with high-k dielectrics on extremely flexible plastic sheets | graphene | 550 | 25 | 2.8 | flexible plastic |
| 2012 | [97] | IBM | State-of-the-art graphene high-frequency electronics | graphene | 140 | 120 | 44 | SiC |
| 2013 | [36] | Columbia | Graphene field-effect transistors with gigahertz-frequency power gain on flexible substrates | graphene | 500 | 10.7 | 3.7 | flexible PEN |
| 2012 | [146] | USC | Self-aligned fabrication of graphene RF transistors with T-shaped gate | graphene | 110 | 23 | 10 | $SiO_2$/Si |
| 2014 | [147] | EPFL | $MoS_2$ transistors operating at gigahertz frequencies | $MoS_2$ (3) | 240 | 6 | 8.1 | $SiO_2$/Si |
| 2014 | [38] | UCLA | Few-layer molybdenum disulfide transistors and circuits for high-speed flexible electronics | $MoS_2$ (2) | 68 | 42 | 50 | $SiO_2$/Si |
| | | | | | | 13.5 | 10.5 | flexible |
| 2014 | [41] | USC | Black-phosphorus radio frequency transistors | black-phosphorus | 300 | 12 | 20 | $SiO_2$/Si |

**Table 8**: Relevant Cited Works of VLS NW Transistors

| Year | Ref. | Title | Novelty | Drawback | Implied Application |
|---|---|---|---|---|---|
| 2001 | [61] | Indium phosphide NWs as building blocks for nanoscale electronic and optoelectronic devices | n- and p-type III-V NWs | electric-field assembly | post-silicon, optoelectronics |
| 2006 | [148] | Vertical high-mobility wrap-gated InAs NW transistor | VLS III-V on silicon | vertical processing | post-silicon, nanoscale RF |
| 2006 | [149] | Dopant-free GaN/AlN/AlGaN radial NW heterostructures as high electron mobility transistors | radial 2D electron gas | NW assembly | post-silicon, chem/bio sensor |
| 2007 | [150] | High electron mobility InAs NW field-effect transistors | VLS III-V on silicon dioxide | NW assembly | post-silicon |
| 2012 | [58] | A III-V NW channel on silicon for high-performance vertical transistors | VLS III-V on silicon | vertical processing | post-silicon |
| 2009 | [151] | Vertically integrated, three-dimensional NW complementary metal-oxide-semiconductor circuits | VLS n-InAs integrated with p-Ge/Si NWs | complexity | 3D CMOS; post-silicon |
| 2009 | [152] | InAs NW transistors as gas sensor and the response mechanism | VLS III-V on silicon dioxide | NW assembly | chemical sensor |
| 2006 | [153] | Fabrication and characterization of pre-aligned gallium nitride NW field-effect transistors | VLS III-nitride on silicon dioxide | non-parallel growth direction | post-silicon |
| 2010 | [24] | Parallel array InAs NW transistors for mechanically bendable, ultrahigh frequency electronics | III-V on flexible | NW mesh assembly | nanoscale RF |

**Table 9**: State-of-the-Art NW/Nanotube-Array RF Devices

| Year | Ref. | Group | Title | Channel | $L_G$ | $f_T$ | $f_{max}$ | Substrate | Direction, Assembly, Alignment |
|---|---|---|---|---|---|---|---|---|---|
| 2009 | [73] | UMich | Radio-frequency operation of transparent NW thin-film transistors | n-$SnO_2$ | 3.8 $\mu$m | 0.11 GHz | 0.29 GHz | glass | planar, VLS-printed, mesh |
| 2014 | [154] | Lund | High-frequency gate-all-around vertical InAs NW MOSFETs on Si substrates | n-InAs | 150 nm | 103 GHz | 155 GHz | silicon | vertical, VLS, parallel-aligned |
| 2010 | [24] | UCB | Parallel array InAs NW transistors for mechanically bendable, ultrahigh frequency electronics | n-InAs | 1.4 $\mu$m | 1 GHz | 1.8 GHz | flexible polyimide | planar, VLS-printed, mesh |
| 2015 | [79] | UIUC | High-speed planar GaAs NW arrays with $f_{max} > 75$ GHz by wafer-scale bottom-up growth | GaAs | 150 nm | 30 GHz | 78 GHz | SI GaAs | planar, VLS, parallel-aligned |
| 2013 | [46] | USC | T-gate aligned nanotube radio frequency transistors and circuits with superior performance | SWCNTs | 100 nm | 102 GHz | 9 GHz | quartz | CVD catalyzed |
| 2012 | [47] | IBM | High-frequency performance of scaled carbon nanotube array field-effect transistors | CNTs | 100 nm | 153 GHz | 30 GHz | $SiO_2$/Si | dielectrophoresis |
| 2009 | [48] | IEMN | 80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes | SWCNTs | 300 nm | 80 GHz | 3 GHz | silicon | spin-on film |

**Table 10**: State-of-the-Art Nanoscale FinFET RF Devices

| Year | Ref. | Group | Title | Channel | $L_G$ | $f_T$ | $f_{max}$ | Substrate | Fin-Channel Synthesis |
|---|---|---|---|---|---|---|---|---|---|
| 2014 | [15] | Lund | $In_{0.53}Ga_{0.47}As$ multiple-gate field-effect transistors with selectively regrown channels | n-$In_{0.53}Ga_{0.47}As$ | 32 nm | 210 GHz | 250 GHz | SI InP | selective area regrowth |
| 2014 | [93] | Lund | Radio-frequency characterization of selectively regrown InGaAs lateral NW MOSFETs | n-$In_{0.63}Ga_{0.37}As$ | 32 nm | 280 GHz | 312 GHz | SI InP | selective area regrowth |
| 2011 | [155] | MIT | High-electron-mobility transistors based on InAlN/GaN nanoribbons | GaN | ~1 $\mu$m | 13.5 GHz | 29 GHz | SiC | ECR-RIE |
| 2006 | [156] | IMEC | Dependence of FinFET RF performance on fin width | Si | 60 nm | 85 GHz | 95 GHz | Si | top-down etching |

**Table 11**: Relevant Single NW RF Device Measurements

| Year | Ref. | Group | Title | Channel | $L_G$ | $f_T$ | $f_{max}$ | Substrate | NW Placement |
|---|---|---|---|---|---|---|---|---|---|
| 2009 | [72] | Harvard | 12 GHz $f_{max}$ GaN/AlN/AlGaN NW MISFET | GaN | 500 nm | 5 GHz | 12 GHz | sapphire | dry transfer |
| 2010 | [92] | Korean Univ | Microwave characterization of a field effect transistor with dielectrophoretically-aligned single silicon NW | Si | 10 $\mu$m | 0.34 MHz | ~0.34 MHz | $SiO_2$/Si | dielectrophoresis |
| 2012 | [157] | NTU | Short channel effects on gallium nitride/Ga2O3 NW transistors | GaN | 50 nm | 150 GHz | 180 GHz | sapphire | VLS |
| 2010 | [71] | UDE | High-frequency measurements on InAs NW field-effect transistors using coplanar waveguide contacts | n-InAs | 1.4 $\mu$m | 7.5 GHz | 15 GHz | SiN/GaAs | spin-on |

**Table 12**: State-of-the-Art Heterogeneously Integrated FETs

| Year | Ref. | Group | Title | Channel | $L_G$ | $f_T$ | $f_{max}$ | Substrate | Method |
|---|---|---|---|---|---|---|---|---|---|
| 2012 | [18] | UCB | Self-aligned, extremely high frequency III–V metal-oxide-semiconductor field-effect transistors on rigid and flexible substrates | InAs | 75 nm | 165.5 GHz | 45.4 GHz | $SiO_2$/Si | wet-etch/PDMS |
| | | | | | 75 nm | 105 GHz | 22.9 GHz | flex polyimide | wet-etch/PDMS |
| 2013 | [16] | UWisc. | Fast flexible electronics with strained silicon nanomembranes | Si | 1.5 $\mu$m | 5.1 GHz | 15.1 GHz | flex PET | release w/ flex mech substrate |
| 2011 | [158, 159] | IEMN | Microwave performance of 100 nm-gate $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ high electron mobility transistors on plastic flexible substrate | $In_{0.53}Ga_{0.47}As$ | 100 nm | 160 GHz | 290 GHz | flex polyimide | substrate-etch/bonded upside-down/metal vias |
| 2006 | [160] | UIUC | Gigahertz operation in flexible transistors on plastic substrates | GaAs | 2 $\mu$m | 1.55 GHz | 1.68 GHz | flex PET | wet-etch/PDMS |
| 2014 | [161] | HRL | Microwave and millimeter-wave flexible electronics | InGaAs | 100 nm | 215 GHz | 202 GHz | flex polyimide | substrate-etch/top-side flex/metal vias |
| 2009 | [162] | AFRL | High-frequency ZnO thin-film transistors on Si substrates | ZnO | 1.2 $\mu$m | 2.45 GHz | 7.45 GHz | $SiO_2$/Si | direct PLD deposition |
| 2012 | [163] | HKU-ST | Fabrication of 100-nm metamorphic AlInAs/GaInAs HEMTs grown on Si substrates by MOCVD | $Ga_{0.47}In_{0.53}As$ | 100 nm | 210 GHz | 146 GHz | Si | direct MOCVD deposition |
| 2009 | [164] | IQE | Monolithic integration of InP-based transistors on Si substrates using MBE | InGaAs | $A_E$ = 0.25 $\mu m^2$ | 224 GHz | 219 GHz | Ge/ $SiO_2$/Si | direct MBE deposition |

# APPENDIX B. SMALL-SIGNAL MODEL EXTRACTION CODE

```
clc;
clear all;

device = char('(Lg=150nm Vgs=0.6V Vds=1V)');

plots='on';
q=2;
%==================================================
%read in frequency
%==================================================

S_cold=dlmread('S_cold.txt','\t');

freq=S_cold(:,1);
if max(freq)< 111
    freq=freq*1E9; %convert to Hz
end
fset=find(freq>0.1E9); %filter out very low measurement with
error
freq=freq(fset,1)
w=freq*2*pi;
fGHz=freq/1E9;
hf=length(freq);
mf=round(length(freq)/2);
lf=2;
extract_high=find(freq>35E9);
extract_low=find(freq<26E9);
extract=find(freq>20E9);
%==================================================
%read in S-parameter
%==================================================

s11r_cold=S_cold(fset,2);
s11i_cold=S_cold(fset,3);
s21r_cold=S_cold(fset,4);
s21i_cold=S_cold(fset,5);
s12r_cold=S_cold(fset,6);
s12i_cold=S_cold(fset,7);
s22r_cold=S_cold(fset,8);
s22i_cold=S_cold(fset,9);
s11cold=s11r_cold+j*s11i_cold;
s21cold=s21r_cold+j*s21i_cold;
s12cold=s12r_cold+j*s12i_cold;
s22cold=s22r_cold+j*s22i_cold;

S_zero=dlmread('S_zero.txt','\t');
s11r_zero=S_zero(fset,2);
s11i_zero=S_zero(fset,3);
s21r_zero=S_zero(fset,4);
```

```
s21i_zero=S_zero(fset,5);
s12r_zero=S_zero(fset,6);
s12i_zero=S_zero(fset,7);
s22r_zero=S_zero(fset,8);
s22i_zero=S_zero(fset,9);
s11zero=s11r_zero+j*s11i_zero;
s21zero=s21r_zero+j*s21i_zero;
s12zero=s12r_zero+j*s12i_zero;
s22zero=s22r_zero+j*s22i_zero;

S_hot=dlmread('S_hot.txt','\t');
s11r_hot=S_hot(fset,2);
s11i_hot=S_hot(fset,3);
s21r_hot=S_hot(fset,4);
s21i_hot=S_hot(fset,5);
s12r_hot=S_hot(fset,6);
s12i_hot=S_hot(fset,7);
s22r_hot=S_hot(fset,8);
s22i_hot=S_hot(fset,9);
s11hot=s11r_hot+j*s11i_hot;
s21hot=s21r_hot+j*s21i_hot;
s12hot=s12r_hot+j*s12i_hot;
s22hot=s22r_hot+j*s22i_hot;

%=================================================
%compute pad capacitance
%=================================================

[y11cold,y12cold,y21cold,y22cold]=s2y(s11cold,s12cold,s21cold,s22
cold);

Cb_fit=polyfit(w,imag(y12cold),1);
Cb= -3*Cb_fit(1)*1E15;

Cgpad_fit=polyfit(w,imag(y11cold+y12cold),1);
Cgpad=Cgpad_fit(1)*1E15-(Cb/3)

Cdpad_fit=polyfit(w,imag(y22cold+y12cold),1);
Cdpad=Cdpad_fit(1)*1E15-(Cb/3)

%=================================================
%de-embed pad capacitance from unbiased y-parameters
%=================================================

[y11zero,y12zero,y21zero,y22zero]=s2y(s11zero,s12zero,s21zero,s22
zero);

y11zero=y11zero-j.*w*Cgpad/1E15;
y22zero=y22zero-j.*w*Cdpad/1E15;

%=================================================
%Setup LSQ fitting
```

```
%==================================================


[z11zero,z12zero,z21zero,z22zero]=y2z(y11zero,y12zero,y21zero,y22
zero);

    %estimates for LSQ fit

    Rch=    real(z22zero(lf)-z22zero(hf));
    Rd_Rs=  real(z22zero(hf));
    Cds=    (1/w(mf)/Rch).*((Rch/(real(z22zero(mf)-
z22zero(hf))))-1)^0.5;
    Ld_Ls=  (1/w(hf)).*imag(z22zero(hf)-
(Rch/(1+j*w(hf)*Cds*Rch)));
    Rs=     real(z12zero(hf));
    Ls=     (1./w(hf)).*imag(z12zero(hf)-
(0.5*Rch./(1+j.*w(hf)*Cds*Rch)));
    Cg=     -(1./w(lf)).*(imag(z11zero(lf)-
(Rch./3./(1+j.*w(lf)*Cds*Rch)))).^(-1);
    Rdy=    ((w(lf).*Cg).^(-2)).*(real(z11zero(lf)-
(Rch./3./(1+j.*w(lf)*Cds*Rch)))).^(-1);
    Rg_Rs=  real(z11zero(hf));
    Lg_Ls=  (1./w(hf)).*imag(z11zero(hf)-
(Rch/3./(1+j.*w(hf)*Cds*Rch)) - (Rdy./(1+j.*w(hf)*Cg*Rdy)));

    %bounds for LSQ fit

    options = optimset('TolX',1E-10,'TolFun',1E-
8,'Display','iter');



    ubRch=      3000;       lbRch=      1000;
    ubRd_Rs=    50;        lbRd_Rs=    25;
    ubCds=      50E-15;    lbCds=      10E-15;
    ubLd_Ls=    200E-12;    lbLd_Ls=    10E-12;
    ubRs=       100;        lbRs=       1;
    ubLs=       100E-12;    lbLs=       0.1E-12;
    ubCg=       100E-15;    lbCg=       1E-15;
    ubRdy=      10^6;       lbRdy=      10^2;
    ubRg_Rs=    200;        lbRg_Rs=    1;
    ubLg_Ls=    100E-12;     lbLg_Ls=    1E-12;

    %simulated Z-equations

    z11fit= Rg_Rs + j*w*Lg_Ls + (Rch./(3*(1+j*w*Cds*Rch))) +
Rdy./(1+j*w*Cg*Rdy);
    z12fit= Rs + (0.5*Rch./(1+j*w*Cds*Rch)) + j*w*Ls;
    z22fit= Rd_Rs + (Rch./(1+j*w*Cds*Rch)) + j*w*Ld_Ls;

%==================================================
%Fit Rch, Rd+Rs, Cds, Ld+Ls
```

```
%==================================================

    F=@(x,xdata) real(x(1) + (x(2)./(1+j*xdata*x(3)*x(2))) +
j*w*Ld_Ls); %fit equation
        x0=[Rd_Rs; Rch; Cds];
    x=lsqcurvefit(F,x0,w,real(z22zero),x0./q,x0.*q,options);
        Rd_Rs=x(1);
        Rch=x(2) ;
        Cds=x(3);
        z22fit= x(1) + (x(2)./(1+j*w*x(3)*x(2))) + j*w*Ld_Ls;

%==================================================
%Fit Ld_Ls
%==================================================

    G=@(y,ydata) imag(Rd_Rs + (Rch./(1+j*ydata*Cds*Rch)) +
j*ydata*y(1)); %fit equation
        x0=Ld_Ls; %guess
    y=lsqcurvefit(G,x0,w,imag(z22zero),(x0/q),(x0*q),options);
        Ld_Ls=y(1);
        z22fit= x(1) + (x(2)./(1+j*w*x(3)*x(2))) + j*w*y(1);

%==================================================
%Fit Rs, compute RD
%==================================================

    H=@(z,xdata) real(z(1) + (0.5*Rch./(1+j*xdata*Cds*Rch)) +
j*xdata*Ls); %fit equation
        x0=Rs; %guess
    z=lsqcurvefit(H,x0,w,real(z12zero),Rs/q,Rs*q,options);
        Rs=z(1);
        z12fit= Rs + (0.5*Rch./(1+j*w*Cds*Rch)) + j*w*Ls;
        Rd=Rd_Rs-Rs;

%==================================================
%Fit Ls, compute Ld
%==================================================

    K=@(a,xdata) imag(Rs + (0.5*Rch./(1+j*xdata*Cds*Rch)) +
j*xdata*a(1)); %fit equation
        x0=Ls; %guess
   a=lsqcurvefit(K,x0,w,imag(z12zero),x0/q,x0*q,options);
        Ls=a(1);
        z12fit= Rs + (0.5*Rch./(1+j*w*Cds*Rch)) + j*w*Ls;
        Ld = Ld_Ls-Ls;

%==================================================
%Fit Lg_Ls, Rdy, Cg; compute Rg, Lg
%==================================================
```

```
    L=@(b,xdata) real(b(1) + j*xdata*Lg_Ls +
(Rch./(3*(1+j*xdata*Cds*Rch))) + b(2)./(1+j*xdata*b(3)*b(2)));
%fit equation
        x0=[Lg_Ls; Rdy; Cg]; %guess

b=lsqcurvefit(L,x0,w,real(z11zero),abs([x0/q]),abs([x0*q]),option
s);
        Lg_Ls=b(1); Rdy=b(2); Cg=b(3);
        z11fit= Rg_Rs + j*w*Lg_Ls + (Rch./(3*(1+j*w*Cds*Rch))) +
Rdy./(1+j*w*Cg*Rdy);
        Rg = Rg_Rs - Rs;
        Lg = Lg_Ls - Ls;

%=================================================
%De-embed extrinsic parameters above from measurements
%Lg=50E-12; Ld=50E-12; Ls=1E-12;
%Rs=500; Rd=500; Rg=30;
%=================================================

[y11hot,y12hot,y21hot,y22hot]=s2y(s11hot,s12hot,s21hot,s22hot);

[z11hot,z12hot,z21hot,z22hot]=y2z(y11hot,y12hot,y21hot,y22hot);

        z11hot=z11hot-j*w*Lg;
        z22hot=z22hot-j*w*Ld;


[y11hot,y12hot,y21hot,y22hot]=z2y(z11hot,z12hot,z21hot,z22hot);

        y11hot=y11hot-j*w*Cgpad/1E15;
        y22hot=y22hot-j*w*Cdpad/1E15;


[z11hot,z12hot,z21hot,z22hot]=y2z(y11hot,y12hot,y21hot,y22hot);

        z11hot=z11hot-Rs-Rg-j*w*Ls;
        z12hot=z12hot-Rs-j*w*Ls;
        z21hot=z21hot-Rs-j*w*Ls;
        z22hot=z22hot-Rs-Rd-j*w*Ls;

        %intrinsic y-parameters


[y11hot,y12hot,y21hot,y22hot]=z2y(z11hot,z12hot,z21hot,z22hot);

%=================================================
%Calculate intrinsic parameters
%=================================================
        Gfd=    -real(y21hot);
        Gfd=0;
        Gfs=    real(y11hot)-Gfd;
        Gfs=0;
```

```
        Cgd.w=    (-
imag(y12hot)./w).*(1+((real(y12hot)+Gfd)./imag(y12hot)).^2);
        Cgs.w=
((imag(y11hot)+imag(y12hot))./w).*((1+((real(y11hot)+real(y12hot)
-Gfs).^2.)./((imag(y11hot)+imag(y12hot)).^2)));
        Cds.w=    (imag(y22hot)+imag(y12hot))./w;

        Cgd.c=mean(Cgd.w(extract));
        Cgs.c=mean(Cgs.w(extract));
        Cds.c=mean(Cds.w(extract));

        Ri.w=       (real(y11hot)+real(y12hot)-
Gfs)./w./(Cgs.w.*(imag(y11hot)+imag(y12hot)));
        Ri.c=       mean(Ri.w(extract));

        D1=         1+(w.*Cgs.w.*Ri.w).^2;
        gm.w=       ((((real(y21hot)-real(y12hot)).^2)  +
((imag(y21hot)-imag(y12hot)).^2)).*D1).^0.5;
        gm.c=       mean(gm.w(extract)); %mS

        tau.w=      (1./w).*asin((imag(y12hot)-imag(y21hot)-
w.*Cgs.w.*Ri.w.*(real(y21hot)-real(y12hot)))./gm.w);
        tau.c=      mean(tau.w(extract)); %psec

        gds.w=      real(y22hot) + real(y12hot);
        gds.c=      mean(gds.w(extract_low)); %mS

        Rgd.w=      (real(y12hot)+ Gfd)./
(w.*Cgd.w.*imag(y12hot));
        Rgd.c=       mean(Rgd.w(extract));

%=================================================
%Simulated S-parameters
%=================================================
D1=     1+(w.*Cgs.c.*Ri.c).^2;
D2=     1+(w.*Cgd.c.*Rgd.c).^2;

y11sim= Gfs + Gfd + ((Ri.c.*(w.*Cgs.c).^2)./D1) +
((Rgd.c.*(w.*Cgd.c).^2)./D2) + j*w.*((Cgs.c./D1)+(Cgd.c./D2));
y12sim= -Gfd - ((Rgd.c.*(w.*Cgd.c).^2)./D2) - j*w.*(Cgd.c./D1);
y21sim= -Gfd + ((gm.c.*exp(-j*w.*tau.c))./(1+j*w.*Ri.c.*Cgs.c)) -
j*((w.*Cgd.c)./(1+j*w.*Rgd.c.*Cgd.c));
y22sim= Gfd + gds.c + ((Rgd.c.*(w.*Cgd.c).^2)./D2) + j*w.*(Cds.c
+ (Cgd.c./D2));

[z11sim,z12sim,z21sim,z22sim]=y2z(y11sim,y12sim,y21sim,y22sim);

z11sim  =   z11sim - (-Rs-Rg-j*w*Ls);
z12sim  =   z12sim - (-Rs-j*w*Ls);
z21sim  =   z21sim - (-Rs-j*w*Ls);
```

```
z22sim  =   z22sim - (-Rs-Rd-j*w*Ls);

[y11sim,y12sim,y21sim,y22sim]=z2y(z11sim,z12sim,z21sim,z22sim);

y11sim  =   y11sim - (-j*w*Cgpad/1E15);
y22sim  =   y22sim - (-j*w*Cdpad/1E15);

[z11sim,z12sim,z21sim,z22sim]=y2z(y11sim,y12sim,y21sim,y22sim);

z11sim  =   z11sim - (-j*w*Lg);
z22sim  =   z22sim - (-j*w*Ld);

[y11sim,y12sim,y21sim,y22sim]=z2y(z11sim,z12sim,z21sim,z22sim);
[s11sim,s12sim,s21sim,s22sim]=y2s(y11sim,y12sim,y21sim,y22sim);
```