MODULARIZING THE LDO TO OPTIMIZE PERFORMANCE BASED ON APPLICATION DESIGN CONSTRAINTS

BY

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THESIS

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ABSTRACT

This thesis aims to construct a modular low-dropout regulator that gives designers more freedom in building a highly efficient regulator that meets application demands. This modular design is able to separate DC regulation and high-frequency supply rejection while not compromising on either of the two. Flexibility is a key requirement during both design and post-design. The proposed regulator is able to achieve all the required goals with full spectrum power supply rejection. By splitting the pass device, this design is able to achieve the best of both internal pole dominant and external pole dominant linear regulators.

To my parents, for their love and support.

ACKNOWLEDGMENTS

I would like to thank my advisor, Dr. Pavan Kumar Hanumolu, for believing in me even when I didn't believe in myself and for pushing me to keep going. I am truly grateful for the opportunity to work with him. I also want to thank Mrunmay and Timir for helping me get started on this project. I would like to thank my Mom, Dad, Sana, Arham, Ivan, Rafat Masi, Mark, Istvan and Torin for always being there and supporting me through thick and thin. I would like to thank my friends, Achal, Asad, Estefany, Gerard, Kadur, Mahika, Nikhil, Reddy, Sid, Taj, Vinay, Vishwa and Vrishin, who have helped me blow off steam while pushing me to stay motivated the last few years. I would also like to acknowledge the contribution of the ECE department at UIUC. My undergraduate and graduate experience was largely defined by the courses and structure the department provides so effectively.

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LIST OF ABBREVIATIONS

BJT	Bipolar Junction Transistor
FOM	Figure of Merit
FFNC	Feed Forward Noise Cancellation
FVF	Flipped Voltage Follower
LDO	Low-Dropout Regulator
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NMOS	N-channel Metal Oxide Semiconductor Field-Effect Transistor
PMOS	P-channel Metal Oxide Semiconductor Field-Effect Transistor
SMPS	Switched Mode Power Supply
VDO	Dropout Voltage

CHAPTER 1

INTRODUCTION

With advances in technology, the last decade has seen a significant rise in portable electronic products. These portable electronics are all battery powered and have increased the need for high-efficiency power management. This chapter discusses a current list of DC-DC converters some of which are very commonly used in portable electronics. Table 1.1 summarizes the different converters. Some of the important characteristics associated with these converters are power efficiency, supply rejection, transient response, load and line regulation. All of these terms will be explained in detail in Chapter 2.

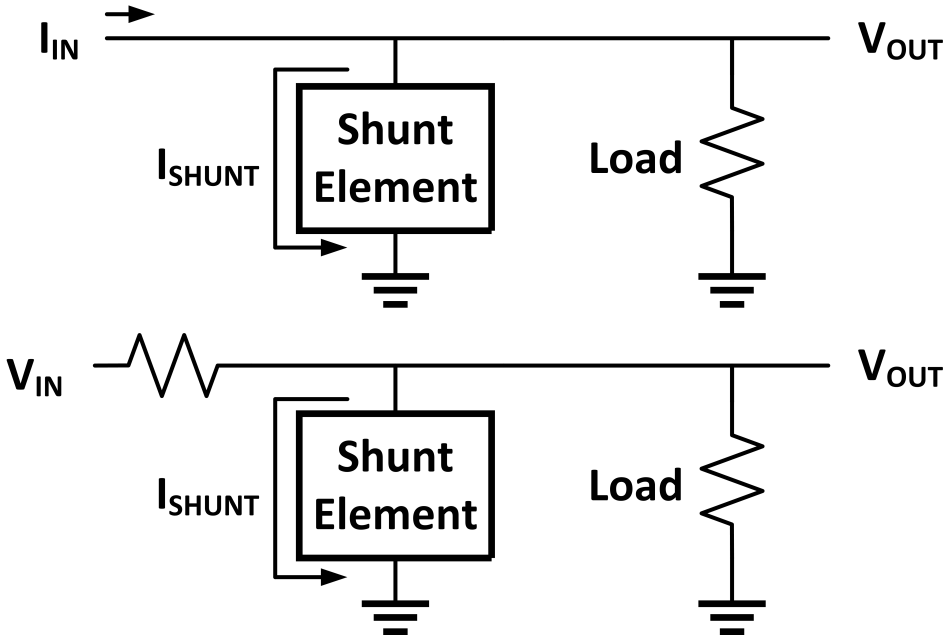
Table 1.1: Comparison of DC-DC Converters

	Shunt Regulator		**Series Regulator**	
	Passive	**Active**	**Non-Linear**	**Linear**
Power Efficiency	×	×	✓	×
Supply Rejection	×	✓	×	✓
Transient Response	×	×	×	✓
Load Regulation	✓	✓	✓	✓
Line Regulation	×	×	✓	✓

1.1 Shunt Regulator

This regulator works on the principle of shunting extra current. It therefore requires a current input. However, if the input is a voltage, a series pass element (such as a resistor) can be used. Figure 1.1, shows both current-in and voltage-in versions of the regulator. The shunt element in the regulator can be of two different types: active or passive. For example a Zener diode can be used as a passive shunt regulator, while an NMOS transistor could be used for an active version.

Figure 1.1: Shunt Regulator



Supply rejection and load regulation of this type of regulator depends on the particular performance and type of shunt element used. A shunt element that can sink higher currents and respond faster would have better supply rejection and load regulation [1]. Line regulation, however, would be based on the series pass element. Equation 1.1 shows the efficiency[1] of a shunt regulator.

$$\eta = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{V_{\text{IN}} \times I_{\text{IN}}} = \frac{V_{\text{OUT}} \times (I_{\text{IN}} - I_{\text{SHUNT}})}{V_{\text{IN}} \times I_{\text{IN}}} \tag{1.1}$$

$$\eta = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times (1 - \frac{I_{\text{SHUNT}}}{I_{\text{IN}}}) \tag{1.2}$$

In a current-in system, $V_{\text{IN}} = V_{\text{OUT}}$, which simplifies Equation 1.2 to Equation 1.3.

[1]Note: All efficiency calculations in this section are based on the systems themselves and do not include amplifier/quiescent currents.

$$\eta = 1 - \frac{I_{\text{SHUNT}}}{I_{\text{IN}}} \tag{1.3}$$

The regulator needs a large I_{SHUNT} to have good supply rejection and load regulation. From Equation 1.3 it is clear that the shunt regulator is not very efficient.

1.2 Series Regulator

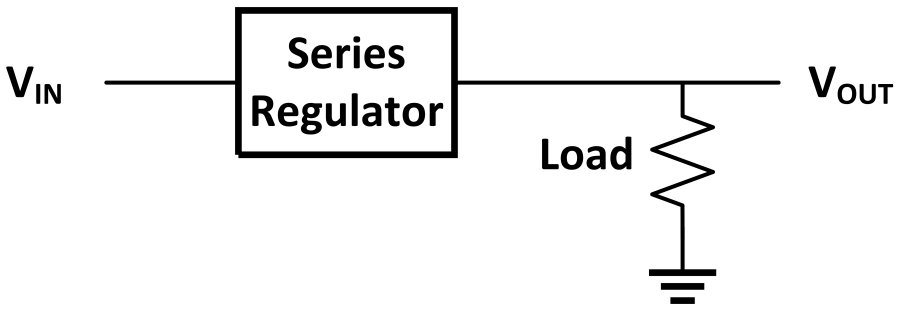
A simple black-box diagram of a series regulator is shown in Figure 1.2. A series regulator can be of two different types: linear and non-linear. The rest of this section discusses each type separately.

1.2.1 Non-Linear Regulator

Non-linear converters are most commonly made with switches and energy storage elements. Based on the storage, non-linear regulators can further subdivide these converters into switched capacitor or switched inductor converters. Since both are very similar, when comparing them to other DC-DC converters, they are discussed together.

As these converters are continuously switching during operation, this creates a ripple in the output. This converter-induced ripple is the reason these converters are not optimal for supply rejection. The transient response of these systems depends on switching frequency and loop bandwidth. As en-

Figure 1.2: Series Regulator



ergy transfer is transferred using energy storage elements (capacitors or inductors), if switching and parasitic losses are ignored, then efficiency η can even approach 1 (or a no power loss conversion) [2].

The very high efficiencies of these systems have made them very popular. However, with integrated systems, due to small passive components, output noise is reasonably high [3]. This has introduced the need for regulators with good supply rejection to overcome the disadvantage of non-linear converters.

1.2.2 Linear Regulator

A conventional linear regulator uses the series pass device to modify the output voltage. These systems can be designed to have good power supply rejection. Linear regulators can also be constructed to have a very fast bandwidth and, consequently, good transient response. The efficiency of this converter is dependent on the ratio of voltage across the linear regulator itself (called the V_{DO}) to the input voltage it is given by Equation 1.5.

$$\eta = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}} = \frac{V_{\mathrm{OUT}} \times I_{\mathrm{OUT}}}{V_{\mathrm{IN}} \times I_{\mathrm{IN}}} = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{V_{\mathrm{IN}} - V_{\mathrm{DO}}}{V_{\mathrm{IN}}} \tag{1.4}$$

$$\eta = 1 - \frac{V_{\mathrm{DO}}}{V_{\mathrm{IN}}} \tag{1.5}$$

Linear regulators with a small dropout voltage are called LDOs. The dropout voltage is limited by V_{DSon} of a power MOSFET or BJT and can be driven to lower values to increase efficiency while sacrificing other design metrics. Also, as V_{IN} scales to lower supply voltages, with newer technologies the fraction $\frac{V_{\mathrm{DO}}}{V_{\mathrm{IN}}}$ becomes more significant. Chapter 2 describes LDOs in more detail as well as some common terminology associated with DC-DC converters.

1.2.3 Concatenated Converters

To get the best of the advantages without the efficiency losses, the converters can be concatenated together [4]. The most typical is the placement of a linear regulator after a non-linear regulator [5], [6], [7]. An LDO for a linear regulator makes the combination efficient while having a good supply rejection. In some cases, like in [8], the combination of linear regulator with a shunt regulator makes the system more efficient.

CHAPTER 2

LDO TERMINOLOGY

As explained in Chapter 1, a linear regulator with a relatively lowdrop out voltage is known as an LDO. A typical LDO is shown in Figure 2.1. The rest of this section describes terms used to describe LDOs.

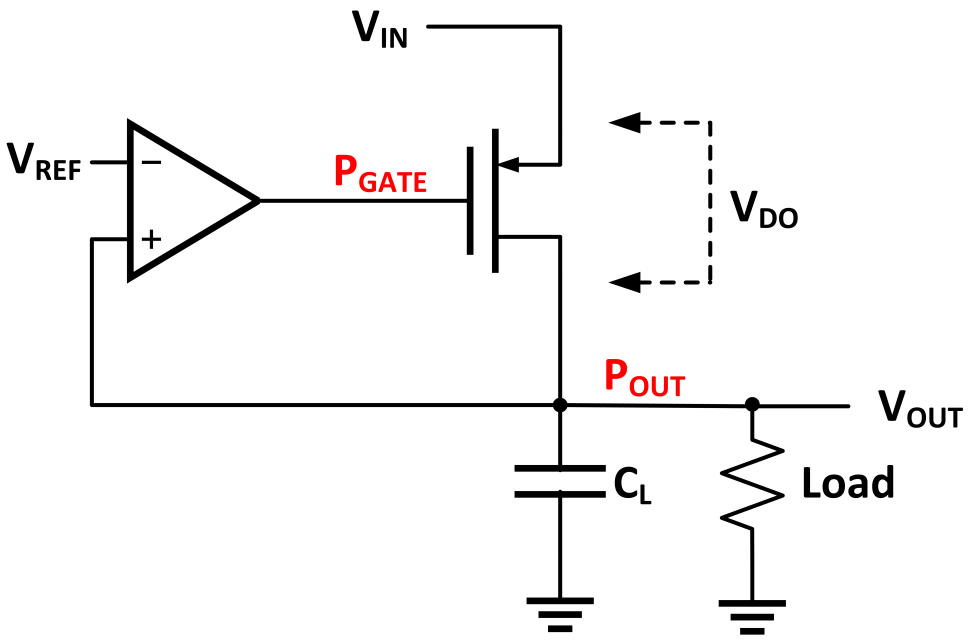
2.1 Dropout Voltage

The difference between the input and output voltage in an LDO is known as the dropout voltage. This voltage is marked in Figure 2.1 as V_{DO}. The value can range from 20 mV to 500 mV depending on the implementation and requirements. As shown in Chapter 1, the higher V_{DO} degrades power efficiency, while having too low of a voltage can drive the pass transistor far into the linear region, which can have a negative impact on line regulation and supply rejection.

2.2 Quiescent Current

I_Q, or quiescent current, is the minimum current required to power the amplifiers and circuits of the LDO when there is a minimum (or no) output load, also known as standby current. This is an important metric in battery operated devices as during sleep/standby modes this power is continuously drawn. To have good efficiency and improve battery life a low quiescent current is desired.

Figure 2.1: LDO



2.3 Line and Load Regulation

The terms used to quantify DC regulation are line and load regulation. The ratio of the change of output voltage to the change in input voltage is called line regulation. Load regulation is the ratio of the change in output voltage to the change in load current. The formulae for the above are given in Equation 2.1 and Equation 2.2 respectively.

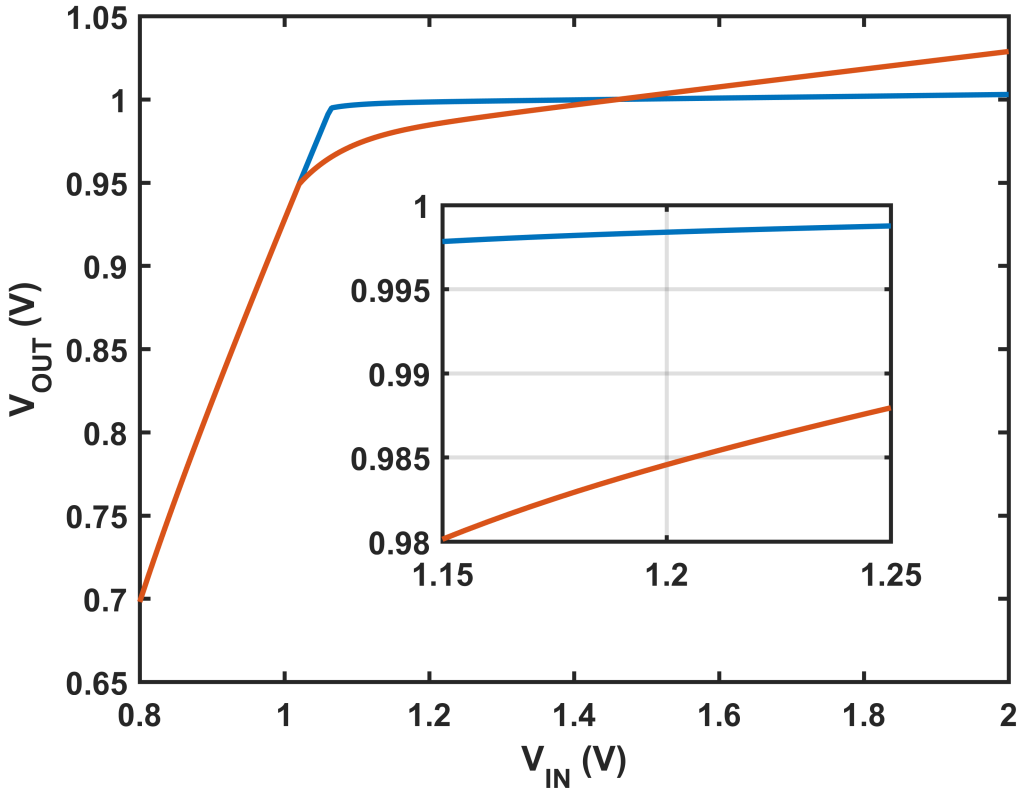
$$\text{Line Regulation} = \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} \tag{2.1}$$

$$\text{Load Regulation} = \frac{\Delta V_{\text{OUT}}}{\Delta I_{\text{OUT}}} \tag{2.2}$$

Figure 2.2 and Figure 2.3 show what typical load and line regulation graphs look like. The curves in blue represent designs with good regulation while the curves in red represent designs with poor regulation.

In Figure 2.2, the reason for a minimum dropout voltage is noticeable. In

Figure 2.2: Line Regulation



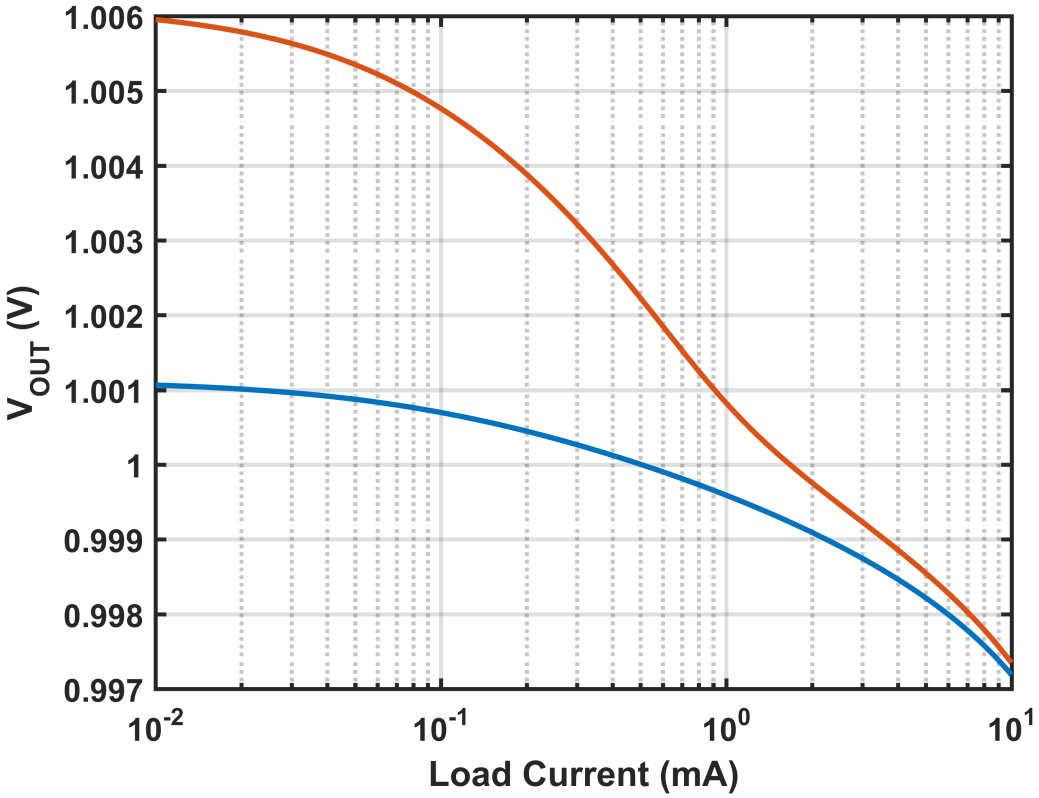
the case shown, V_{OUT} levels off after $V_{IN} >$ 1.1 V. Therefore a $V_{DO} <$ 100 mV would cause a severe degradation in line regulation.

Figure 2.3 shows the degradation of load regulation at very low output currents. To understand why, let us consider the extreme case of no-load current. Due to leakage, some current gets through the pass transistor to the output node. The no-load case can be resolved by having some quiescent current (which is greater than leakage current) drawn from the output node instead of the input node.

2.4 Efficiency

Efficiency is usually discussed in terms of power. However in the case of an LDO, it is commonly described as current efficiency, which is the ratio of

Figure 2.3: Load Regulation



I_{OUT} to I_{IN}. Since an LDO has a dropout voltage, this efficiency can be converted to a power efficiency as shown in Equation 2.4.

$$\eta = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{V_{\text{IN}} \times I_{\text{IN}}} = \frac{V_{\text{IN}} - V_{\text{DO}}}{V_{\text{IN}}} \times \eta_{\text{Current}} \tag{2.3}$$

$$\eta = (1 - \frac{V_{\text{DO}}}{V_{\text{IN}}}) \times \eta_{\text{Current}} \tag{2.4}$$

2.5 Supply Rejection

Supply rejection of an LDO is the ability of the LDO to suppress noise that appears on the input from showing up as an output. The best representation of supply rejection is a gain graph over frequency as shown in Figure 2.6, on page 13. To discuss supply rejection, the first important detail is to decide a pass device.

Section 2.5.1 details PMOS and NMOS pass devices with respect to supply rejection, and Section 2.5.2 discusses amplifiers for them. Section 2.5.3 details pole placement and how it affects supply rejection. Section 2.5.4 discusses different sources of noise that affect LDO design and performance.

2.5.1 Pass Device

In this research, CMOS technology was used. Therefore, the decision of a pass device is between a PMOS and NMOS. An NMOS device can be used but requires either a large dropout voltage or a charge pump for the error amplifier to raise the gate node so as to have a lower dropout voltage. The charge pump, however, introduces more noise into the system and is not ideal from a supply rejection point of view.

For an NMOS, the drain is connected to the supply node and the gate is the control node. This setup would suppress noise from the supply to the source (V_{OUT}) if there is no noise at the control node.

On the other hand, for a PMOS device, the source is connected to the supply node, and the drain is the output node. The gate remains the control node. Since supply noise is at the source, it has to be replicated at the gate (control node) to keep the supply noise from being amplified as well as to keep the output free of noise.

PMOS and NMOS pass devices therefore require specifically designed amplifiers.

2.5.2 Conventional Differential Amplifiers and Supply Noise

Figure 2.4 shows a differential amplifier with an NMOS input pair with its small signal model, and Figure 2.5 shows the same with a PMOS input pair. Equations evaluate the output supply noise for both architectures and clearly show that the output of an NMOS input pair amplifier mimics the supply node at a small signal level. However, the same is not true for the PMOS version. This makes the NMOS input pair differential amplifier ideal for a

Figure 2.4: NMOS Differential Amplifier

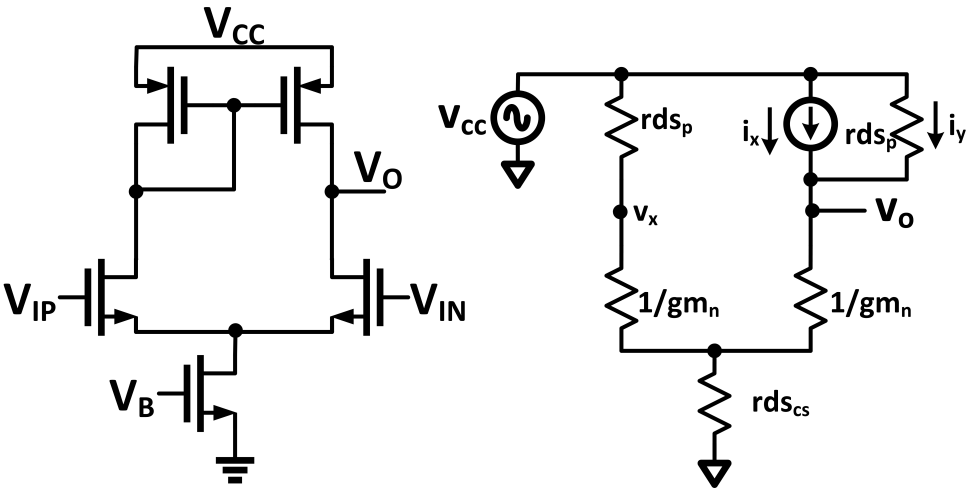
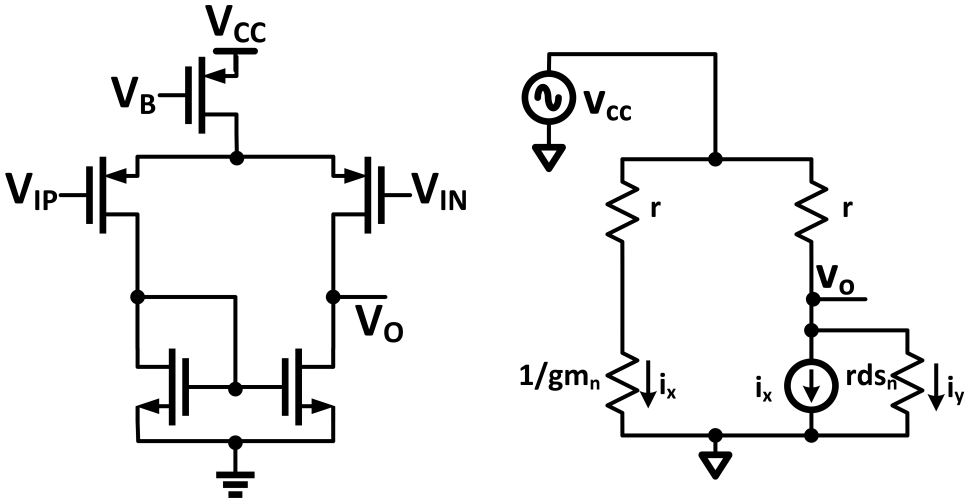


Figure 2.5: PMOS Differential Amplifier



PMOS pass transistor and vice versa.

For the NMOS pair, it can assumed that $rds_P \gg \frac{1}{gm_N}$

$$v_X = v_{CC} \times \frac{\frac{1}{gm_N}}{\frac{1}{gm_N} + rds_P} \approx v_{CC} \tag{2.5}$$

Further:

$$i_X = gm_P \times (v_{CC} - v_X) \approx 0 \tag{2.6}$$

And, therefore:

$$v_O = v_{CC} \times \frac{rds_P}{\frac{1}{gm_N} + rds_P} \approx v_{CC} \tag{2.7}$$

For the PMOS input pair:

$$v_O = v_{CC} \times \frac{rds_N}{rds_N + r} - i_X \times \frac{rds_N \times r}{rds_N + r} \tag{2.8}$$

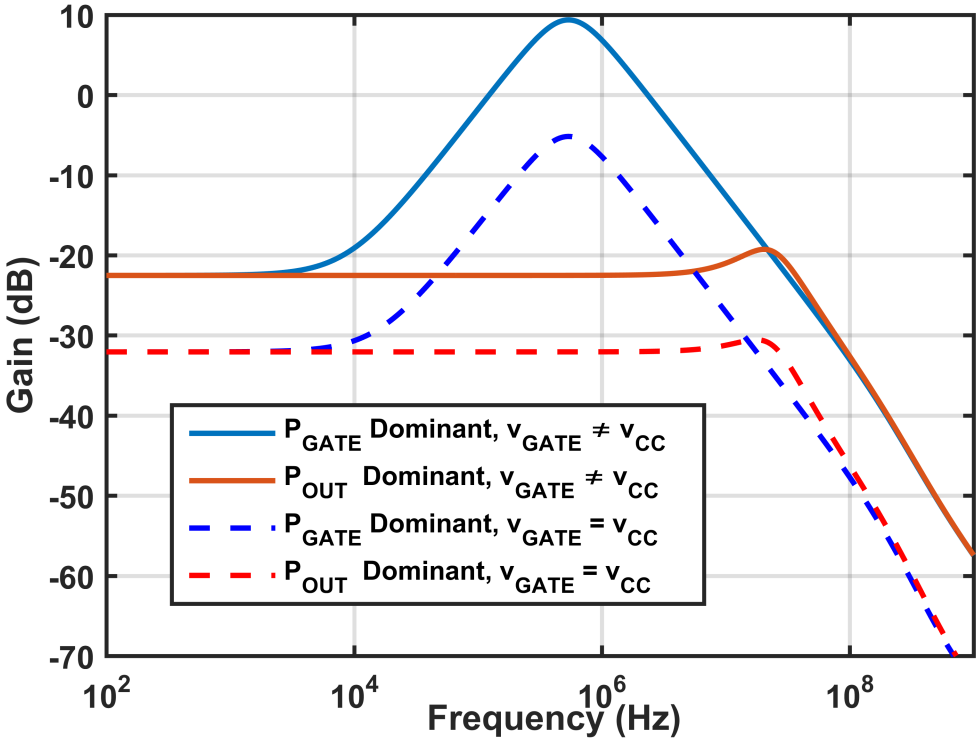
$$v_O \approx v_{CC} \times \frac{rds_N}{rds_N + r} - \frac{v_{CC}}{r} \times \frac{rds_N * r}{rds_n + r} = 0 \tag{2.9}$$

It is possible to have it the other way around instead, as the noise at the output depends on the placement of the active loads. So, a folded cascode would be one way of flipping the input pair and output supply noise.

2.5.3 Pole Placement and Effect on Supply Rejection

Figure 2.6 is a graph of supply rejection with P_{GATE} moving between being the dominant and non-dominant node (Refer to Figure 2.1 for circuit diagram). The systems were simulated using a PMOS pass transistor. The

Figure 2.6: PSR and Pole Placement



dashed curves are results with supply noise at the gate node as recommended by Section 2.5.1 and Section 2.5.2, while the solid curves are without. This clearly shows that a system with an output dominant pole has the best supply rejection. It is also clear that introducing supply noise at the control node (in a PMOS controlled LDO) is beneficial for low-frequency supply rejection as well as high-frequency supply rejection.

2.5.4 Understanding Noise Sources

There are two nodes at which noise is introduced into the system which are relevant in this discussion: the input node and output node.

At the input node, noise can be introduced from either a switching regulator, which would add a large amount of switching noise, or from other digital circuits on the same supply line. The switching regulator noise could be a large portion of the total magnitude of the noise, yet this is all at a

given switching frequency and can be reduced significantly if required.

Another source of noise not often discussed is the noise introduced by the load itself. This noise is introduced to the output node directly and is due to the load changing fast enough where the regulation loop is too slow and unable to track the output node. This can cause the output to droop or spike significantly if the value of the charge required or dumped is high enough. Let us take an example of a buffer in a communication chain running at high frequencies. The buffer′s output might need to swing from rail to rail very quickly. Assuming a significant capacitor at the buffer output node, a large charge is required from the LDO output node or could be dumped onto the LDO output node, which could have a detrimental effect on other parts of the circuit.

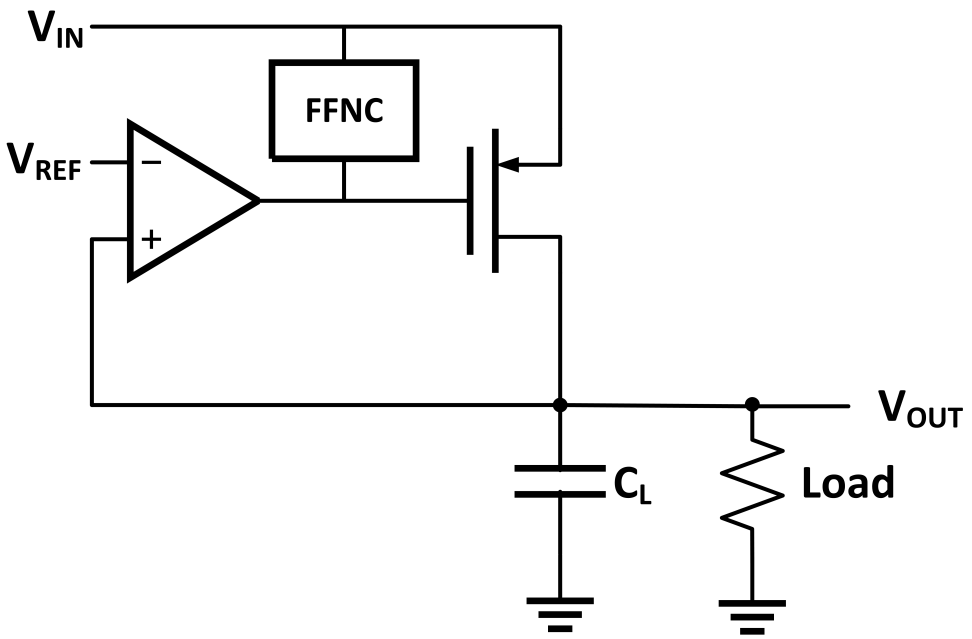
CHAPTER 3

LITERATURE REVIEW

3.1 Feed Forward Noise Cancellation

Feed forward noise cancellation is a method of noise cancellation that observes supply noise and tries to cancel the noise at the output. A typical implementation of this method has been shown in Figure 3.1. This method has been proven and tested in [9] and [10]. However, in these designs the overall system is internal pole dominant, which leads to degradation of noise rejection at high frequencies (in [10] $>$ 4 MHz). This system can increase noise rejection over a range of frequencies. However, it does not help with transient response or line/load regulation.

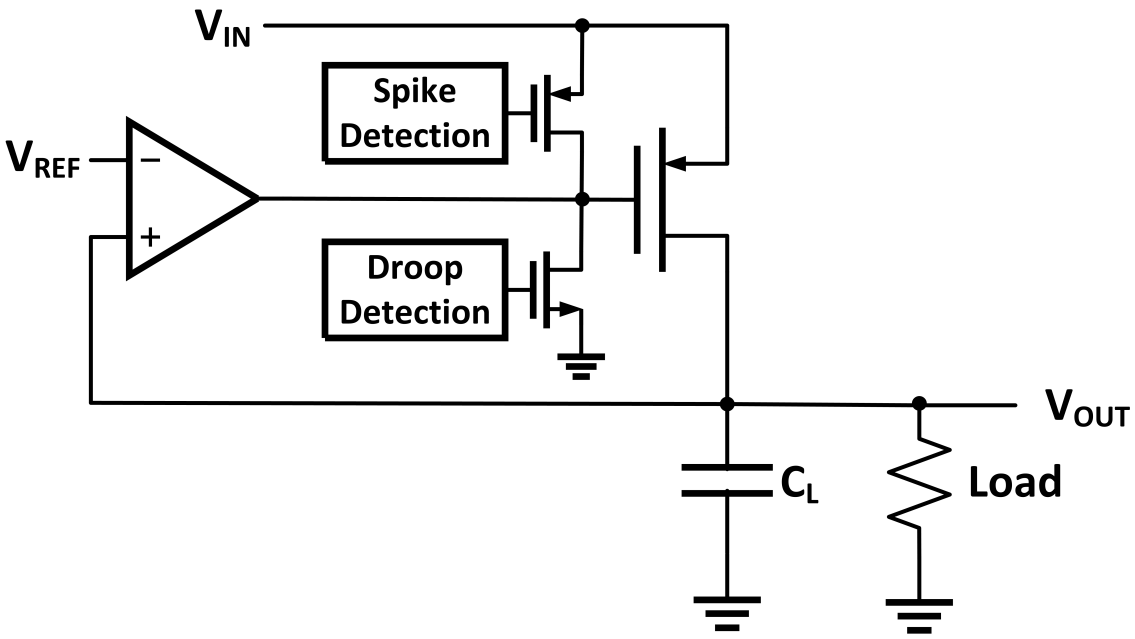
Figure 3.1: Feed Forward Noise Cancellation



3.2 Switch Based Transient Enhancement

Transient enhancement is a method to quickly charge or discharge the nodes with high capacitances. A block diagram showing an example implementation is shown in Figure 3.2. This can help the system to settle quicker and improve transient response; however, this method does not improve supply rejection and comparators can draw significant quiescent power. This method has been used in [11] to help improve transient response.

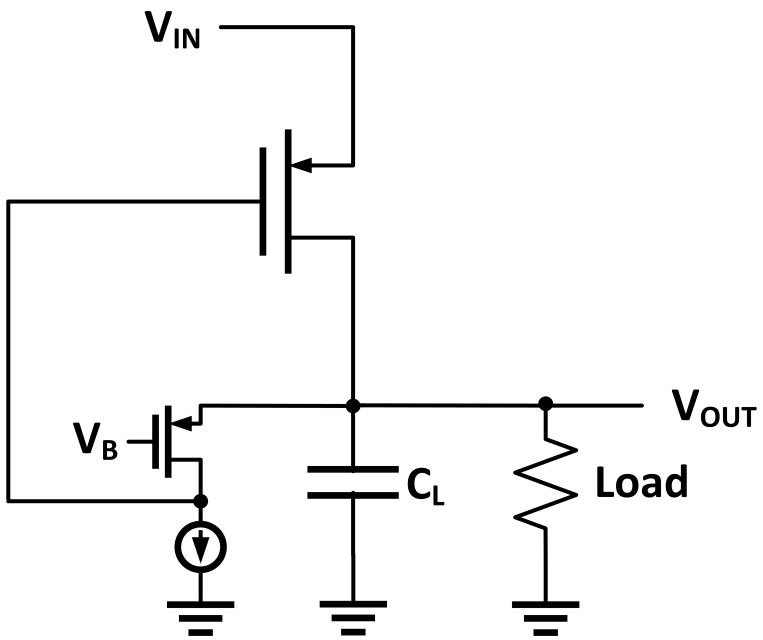
Figure 3.2: Transient Enhancement



3.3 Flipped Voltage Follower

Figure 3.3 demonstrates the use of a FVF circuit, which is the most efficient way of powering the single transistor amplifier [12]. The gain of a system like this, however, can be limited leading to poor line and load regulation. However, in [13] and [14] using multiple loops and buffer impedance attenuation, some of these shortcomings are overcome. Since it is a single-ended solution, it does provide a quiescent current benefit.

Figure 3.3: Flipped Voltage Follower



3.4 Dynamic Biasing

In [15], the LDO is dynamically biased based on the load to provide a better solution for different load currents. Dynamic biasing can also reduce quiescent current at no load, improving overall efficiency; however, this does mean that transient response to load steps can be sluggish.

CHAPTER 4

MODULAR LDO DESIGN

To modularize the LDO, the required design characteristics that have been decided for this research are as follows:

- Supply rejection
- DC regulation
- Transient response

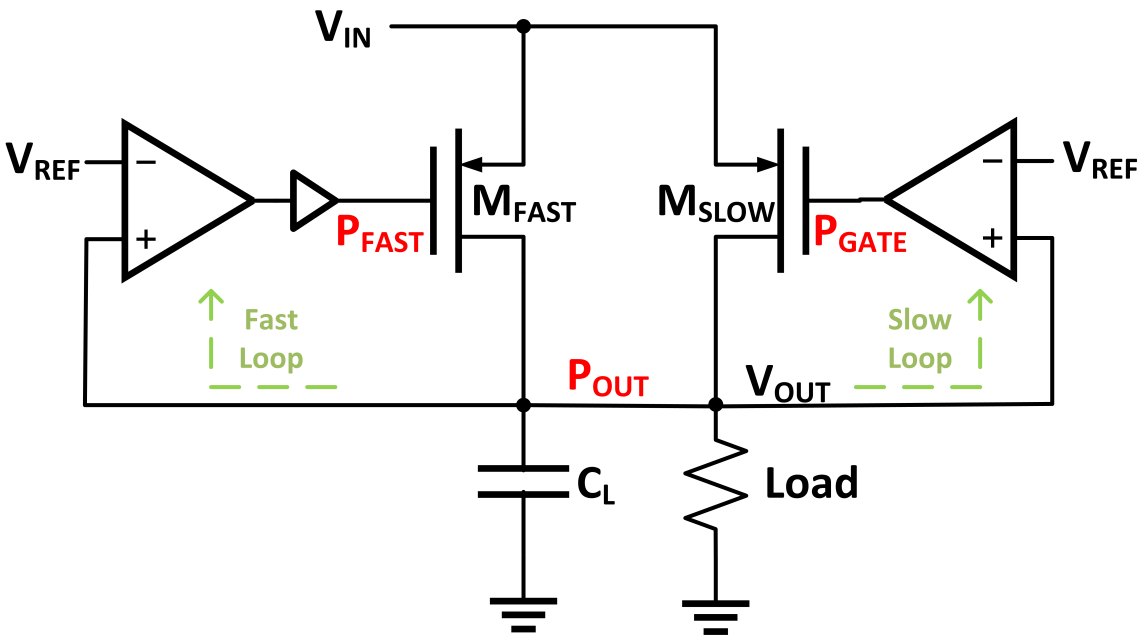
The transient response block has been discussed widely in the literature and no work has been done on it in this design. The following sections discuss each module in detail.

4.1 Supply Rejection

The most important device in supply rejection is the output/load capacitor. It sets an important pole in the system and helps reduce the supply noise by filtering high-frequency current to ground. A higher value of this capacitor almost always aids design. The rest of this subsection discuses active methods used for supply rejection.

For the purpose of this research, it is assumed that a majority noise contributor to the load circuits is due to a switching regulator. Noise from an SMPS can be at varying switching frequencies going as high as the GHz range. Fully integrated SMPS designs usually have high switching frequency so as to keep the size of energy storage elements low. The assumptions made for the purpose of this design are that (1) the SMPS has a high (>100 kHz) switching frequency and (2) the SMPS has ripples as large as 100 mVpp. Since the majority noise contributor is the SMPS, switching noise from dig-

Figure 4.1: Split Transistor LDO



ital circuits is ignored.

For high-frequency supply rejection, shown in Section 2.5.3, the systems dominant pole should be at the output node, P_{OUT}. Pass transistors of LDOs can be very large, leading to high capacitance at the gate node, which can make it incredibly difficult to have an output pole dominant structure. The ideal structure would have P_{OUT} as the dominant node and P_{FAST} as the non-dominant node, with all other poles lying at frequencies at least twice that of the unity gain bandwidth of the system.

4.2 Split Pass Transistor Approach and Sizing

If the pass transistor is split up, it becomes possible to use a small portion of the pass transistor to control the high-frequency content, and the larger portion to supply additional required load current. The approach to choosing the split depends on the magnitude of noise needed to be suppressed. If M_{FAST} (refer to Figure 4.1) is too small, it cannot effectively cancel out large noise sources, and if M_{FAST} is too large, it would require more power to push the P_{FAST} pole out far enough. However, unless the smaller size causes

removal of a stage in the buffer, the additional power is not exorbitant. A drawback of having M_{FAST} too large is that it reduces the gain of the slow loop, which reduces DC regulation.

In this technology and design, a split of 70-30 is able to cancel out 100 mVpp of input noise while a split of 80-20 causes the pass transistor to clip. Therefore, a 70-30 split is chosen.

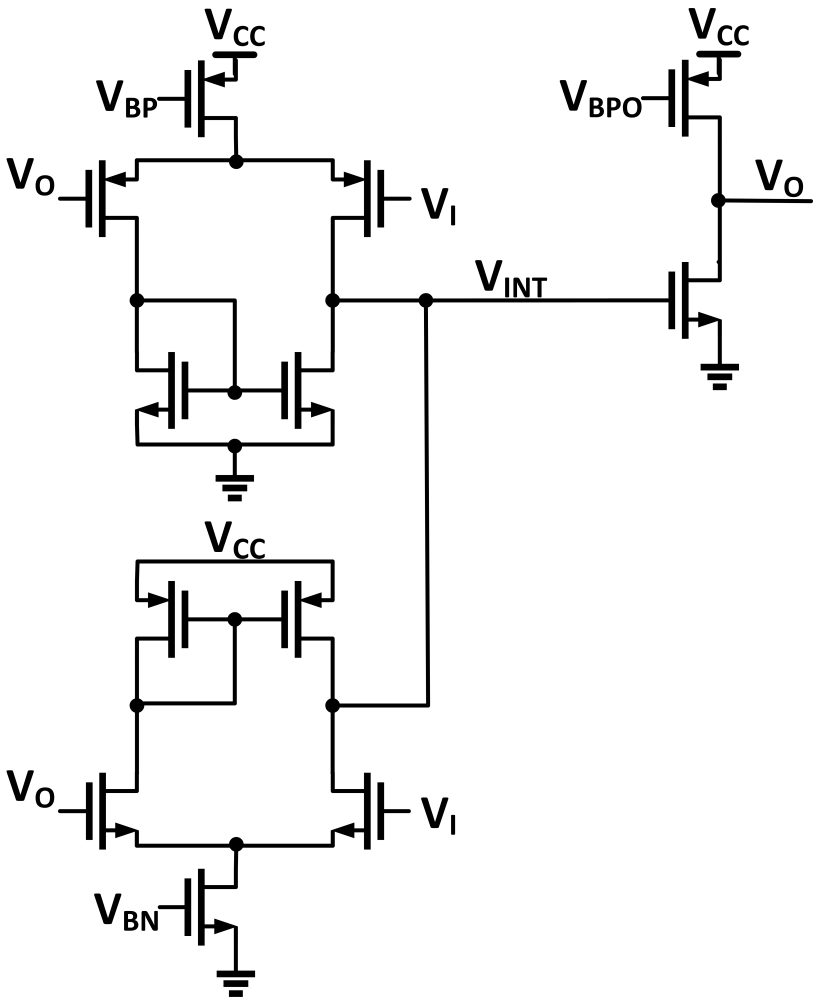
4.3 Buffer Design

There are multiple choices for buffers; however, the following criteria narrow the selection process. Rail-to-rail input and output as the fast loop is required to cancel out the large transient noise. A single-ended structure would be power efficient but achieving rail-to-rail input would be difficult. The choice is therefore to use a single-ended output stage, efficiently using a large chunk of the power and an input differential stage. To achieve rail-to-rail input, both an input NMOS and PMOS pair are used. The buffer used is shown if Figure 4.2. So as to not overdesign, it is important to note that the NMOS stage does not need to be as fast as the PMOS stage. This is because the NMOS would only be active when the input and output are at high values. This implies that the regulator has a low output load and, conversely, both the P_{GATE} and P_{OUT} would have reduced significantly.

4.4 Amplifier Choice

The FVF is an ideal choice for the fast loop because it is single ended and therefore is efficient in consumption of power. The FVF also provides a positive gain from the output node and can be used as a one-transistor amplifier, which is perfect for a fast-low-gain loop. Another advantage of using a FVF is that it consumes current from the output node, which slightly helps with load regulation of the system. One downside to a FVF design is that it is not easy to produce a path from the supply to the output of the FVF circuit. This is overcome by M_{PSR}, which is shown in Figure 4.3. It is sized to provide 0 dB gain from the supply to the input of the buffer so as to introduce small

Figure 4.2: Buffer Design



signal supply noise at the output of the FVF stage. Another disadvantage of the FVF is that it does not provide the best regulation on its own, but in this design, the fast loops purpose is to provide good supply rejection, not good regulation. The workaround for the poor DC regulation is discussed in the next section

4.5 DC Regulation

Regulation of the LDO at DC is based solely on DC loop gain and low offset amplifiers. Having a high DC gain, however, could be tricky if the system is external pole dominant. Here, the slow loop's internal pole is kept as the dominant node so as to have the best possible DC regulation. This enables a low quiescent current as well as a high DC gain. The bandwidth of the slow loop would be relatively low, implying the transient response and supply rejection of the loop on its own would not be very good. Nevertheless, with the transient response module and supply rejection module in the system, the overall system functions as desired with acceptable supply noise elimination and transient performance.

One issue with DC regulation is the fast loop; it does not track V_{REF} as it has no reference. At high load currents, this is acceptable as the slow loop can compensate for the offset in DC regulation. At low load currents, however, the gain of the slow loop is reduced as most of the current is going through M_{FAST}, which can reduce DC regulation with M_{SLOW} turned off. One way to solve this issue is to force the FVF output node to increase when the load current increases. Another solution is to amplify the difference between the two gate nodes using a design as shown in Figure 4.4. A simulation to compare the different solutions discussed in this section is shown in Figure 4.5.

Figure 4.3: FVF Design

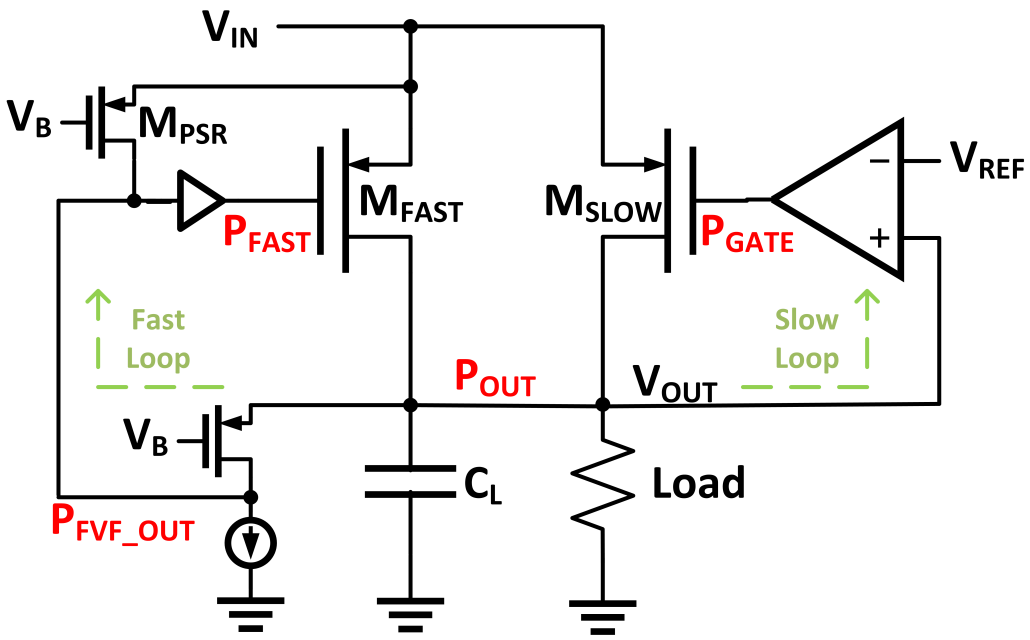


Figure 4.4: FVF with Comparator

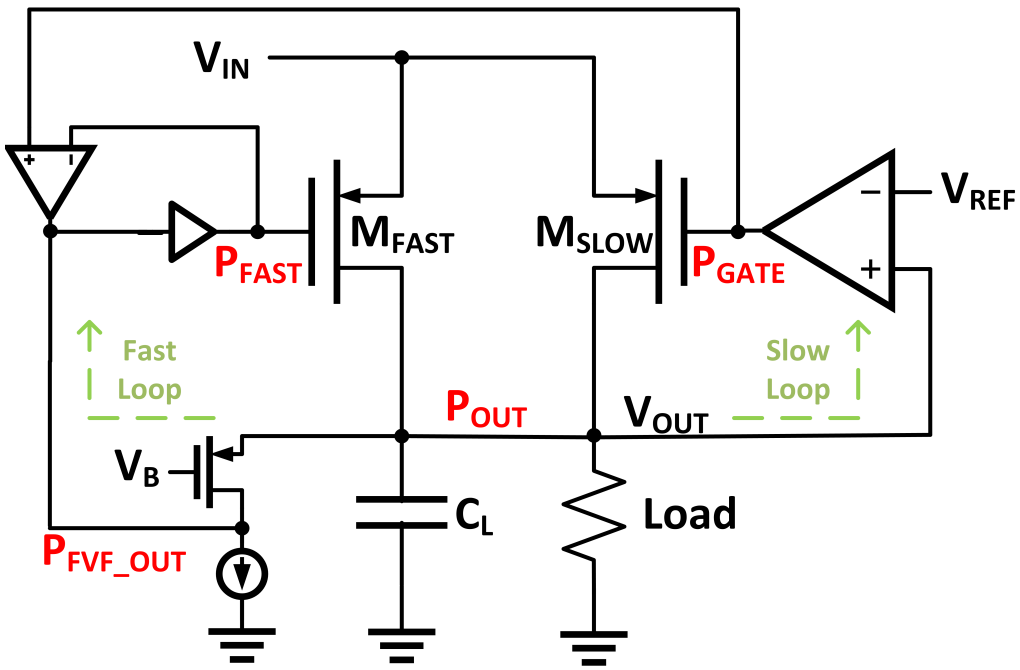
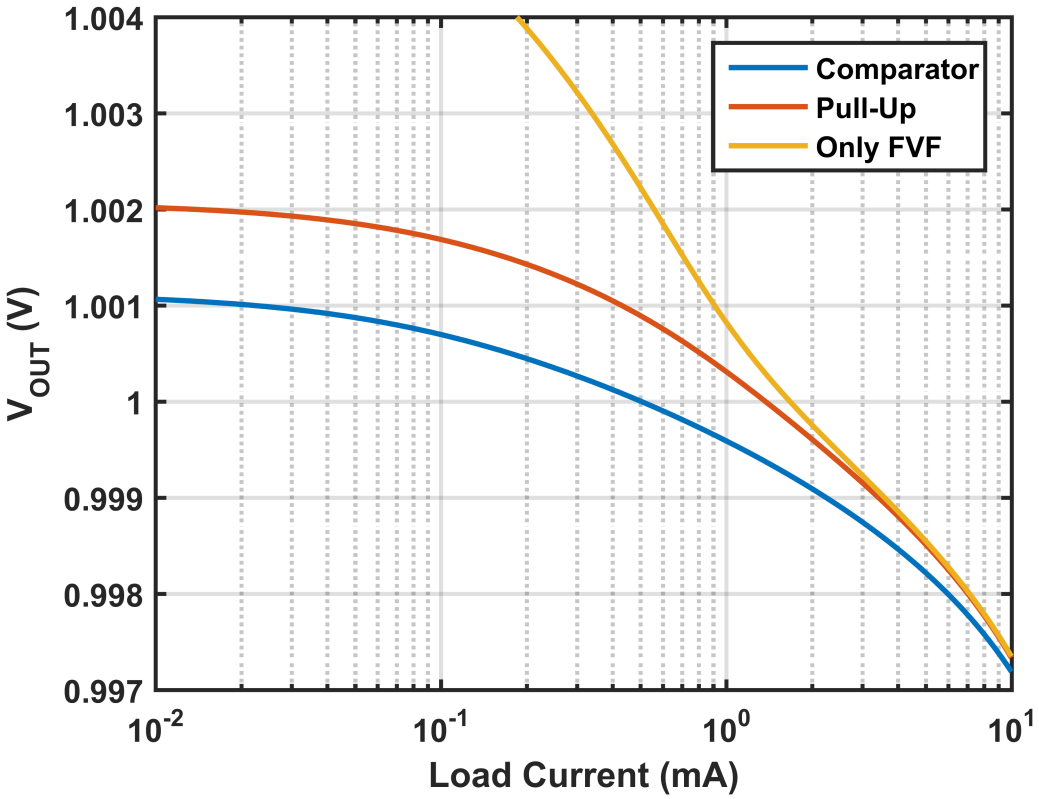


Figure 4.5: Load Regulation Comparison



4.6 Analysis

A block diagram with corresponding small signal parameters is shown in Figure 4.6, while Figure 4.7 shows the buffer.

Figure 4.6: LDO with Small Signal Parameters

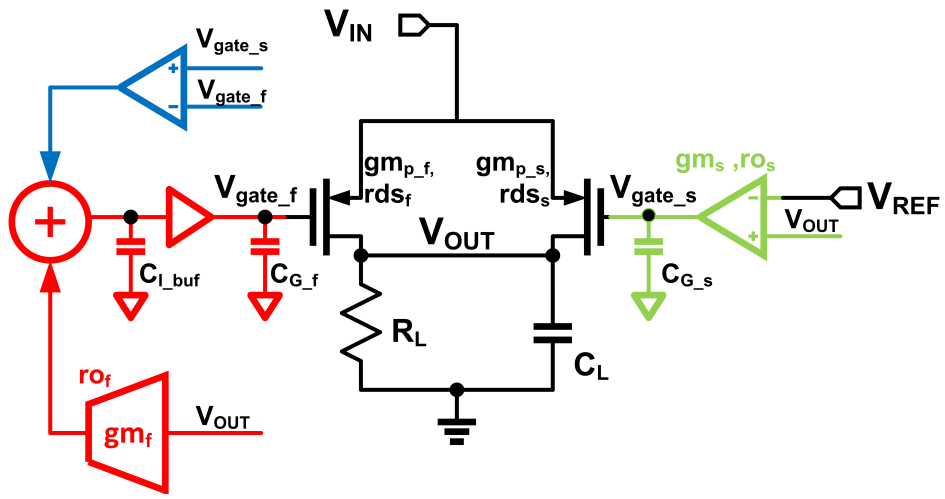
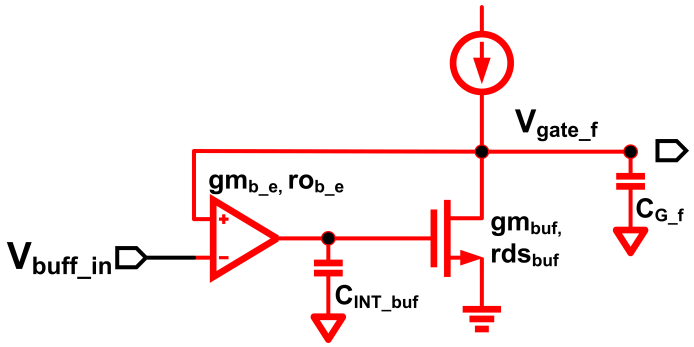


Figure 4.7: Buffer with Small Signal Parameters



4.6.1 Slow Loop

$$R_{OUT} = R_L \parallel rds_S \parallel rds_F \tag{4.1}$$

$$Av_S = gm_S ro_S \tag{4.2}$$

$$Av_{Ps} = gm_{Ps} Ro_{OUT} \tag{4.3}$$

$$\omega_S = \frac{1}{ro_S C_{Gs}} \tag{4.4}$$

$$\omega_{OUT} = \frac{1}{R_{OUT} C_{OUT}} \tag{4.5}$$

$$=> \frac{v_{OUTs}}{v_{REF}} = (\frac{Av_{Ps}}{1 + \frac{s}{\omega_{OUT}}})(\frac{Av_S}{1 + \frac{s}{\omega_S}}) \tag{4.6}$$

4.6.2 Comparator Loop

$$ro_3 = rds_3 \parallel rds_{31} \tag{4.7}$$

$$Av_3 = gm_3 ro_3 gm_4 ro_4 \tag{4.8}$$

$$\omega_3 = \frac{1}{ro_3 C_C} \tag{4.9}$$

$$\omega_F = \frac{1}{ro_F C_{Ibuff}} \tag{4.10}$$

$$\omega_{Pf}, \omega_F, \omega_{Buff} \gg \omega_3 \tag{4.11}$$

$$=> \text{Loop } 3 = \frac{v_{Gatef}}{v_{Gates}} \approx \frac{Av_3}{Av_3 + (1 + \frac{s}{\omega_3})(1 + \frac{s}{\omega_F})} \approx \frac{Av_3}{Av_3 + (1 + \frac{s}{\omega_3})} \tag{4.12}$$

$$\text{For low load currents } Av_3 \gg 1 => \text{Loop } 3 \approx \frac{1}{1 + \frac{s}{\omega_3 Av_3}} \tag{4.13}$$

4.6.3 Buffer

$$Av_B = gm_{Be} ro_{Be} gm_{buf} ro_{buf} \tag{4.14}$$

$$\omega_{Be} = \frac{1}{ro_{Be} C_{INTbuf}} \tag{4.15}$$

$$\omega_{Pf} = \frac{1}{rds_{buf} C_{Gf}} \tag{4.16}$$

$$=> Av_{BUF}(s) = \frac{v_{Gatef}}{v_{BUFFin}} \approx \frac{Av_B}{Av_B + (1 + \frac{s}{\omega_{Be}})(1 + \frac{s}{\omega_{Pf}})} \tag{4.17}$$

4.6.4 Fast Loop

$$Av_F = gm_F ro_F \tag{4.18}$$

$$Av_P f = gm_{Pf} R_{OUT} \tag{4.19}$$

$$\omega_F = \frac{1}{ro_F C_{Ibuff}} \tag{4.20}$$

$$=> \frac{v_{OUTf}}{v_{REF}} = [\frac{Av_F}{1+\frac{s}{\omega_F}} + (\frac{Av_S}{1+fracs\omega_S})Loop_3(s)]A_{BUF}(s)(\frac{Av_Pf}{1+\frac{s}{\omega_{OUT}}}) \quad (4.21)$$

4.6.5 Total Open Loop Gain

$$Av_{REF}(s) = \frac{v_{OUT}}{v_{REF}} = \frac{v_{OUTf}}{v_{REF}} + \frac{v_{OUTs}}{v_{REF}} \quad (4.22)$$

$$= (\frac{Av_Ps + Av_Pf}{1+\frac{s}{\omega_{OUT}}})[(\frac{Av_F}{1+\frac{s}{\omega_F}} + (\frac{Av_S}{1+\frac{s}{\omega_S}})Loop_3(s))A_{BUF}(s) + \frac{Av_S}{1+\frac{s}{\omega_S}}] \quad (4.23)$$

4.6.6 Supply Rejection

C_X =Effective Capacitance from V_{IN} or V_{CC} to the V_{OUT}.

$$\frac{v_{OUT}}{V_{CC}} = \frac{R_L rds_{PASS} C_X s + R_L}{R_L rds_{pass}(C_L + C_X)s + R_L + rds_{PASS}} \times \frac{1}{1 + Av_{REF}(s)} \quad (4.24)$$

CHAPTER 5

RESULTS

The proposed LDO was designed in 180 nm CMOS and simulated using LT-Spice. This section discusses the results of the design.

The maximum load of the circuit is 10 mA. A capacitance of 400 pF is used in this implementation. Using a smaller capacitor is possible, but as it is very expensive in power to push internal nodes to high frequencies, it is not feasible. The pull-up design from Section 4.5 is used for the design. Even though the comparator version gives a slightly better load regulation (Figure 4.5), it does so only because the differential amplifier used as the comparator is heavily unbalanced. This causes supply noise to leak through the comparator and detrimentally effect the overall supply rejection of the system. Figure 5.1 shows that the load regulation for this implementation is 6.2 mV / 10 mA. The line regulation of the design is 1.5 mV / 100 mV as shown in Figure 5.2.

As described in Section 3.4 the quiescent current of this system scales with output current. The majority of the quiescent current for this design, as expected, is drawn by the buffer and FVF stage to have high frequency poles. While scaling the buffer current has been accomplished in this design, the FVF stage is a lot trickier to scale and therefore is a majority quiescent current burner at low load currents. However, this helps with transient response and removes the need for any transient enhancement blocks for fast turn-on purposes. Figure 5.3 shows the total quiescent current as a function of the output current.

Figure 5.1: Load Regulation

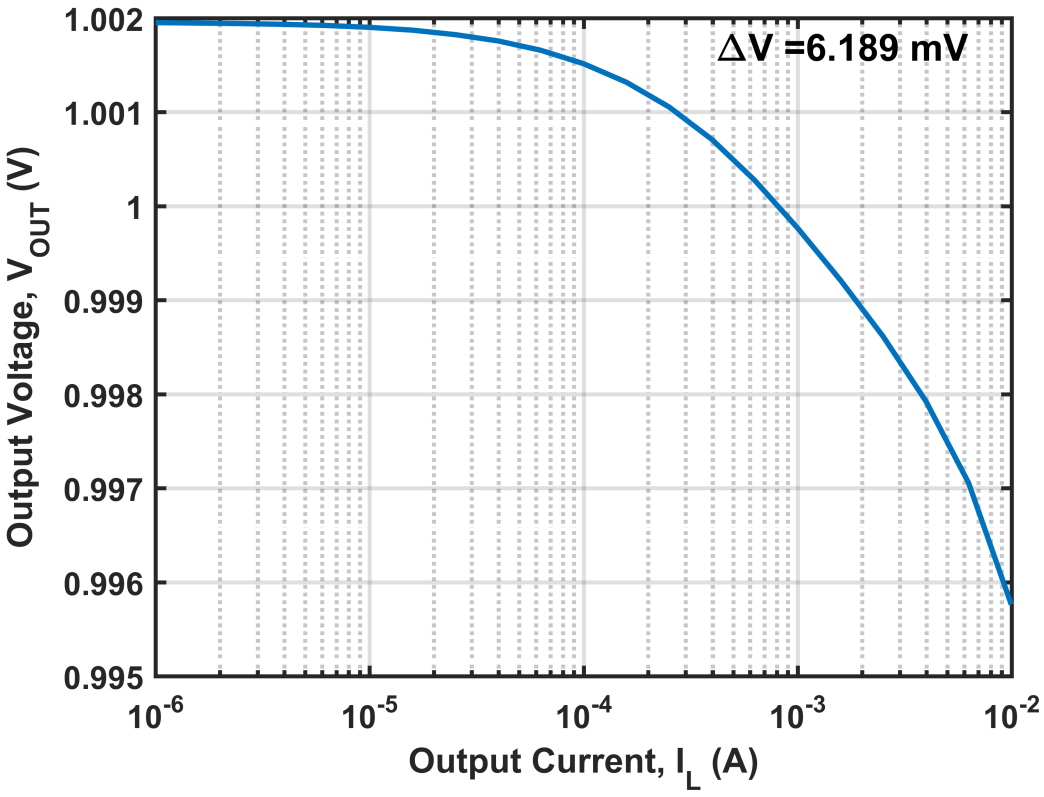


Figure 5.2: Line Regulation

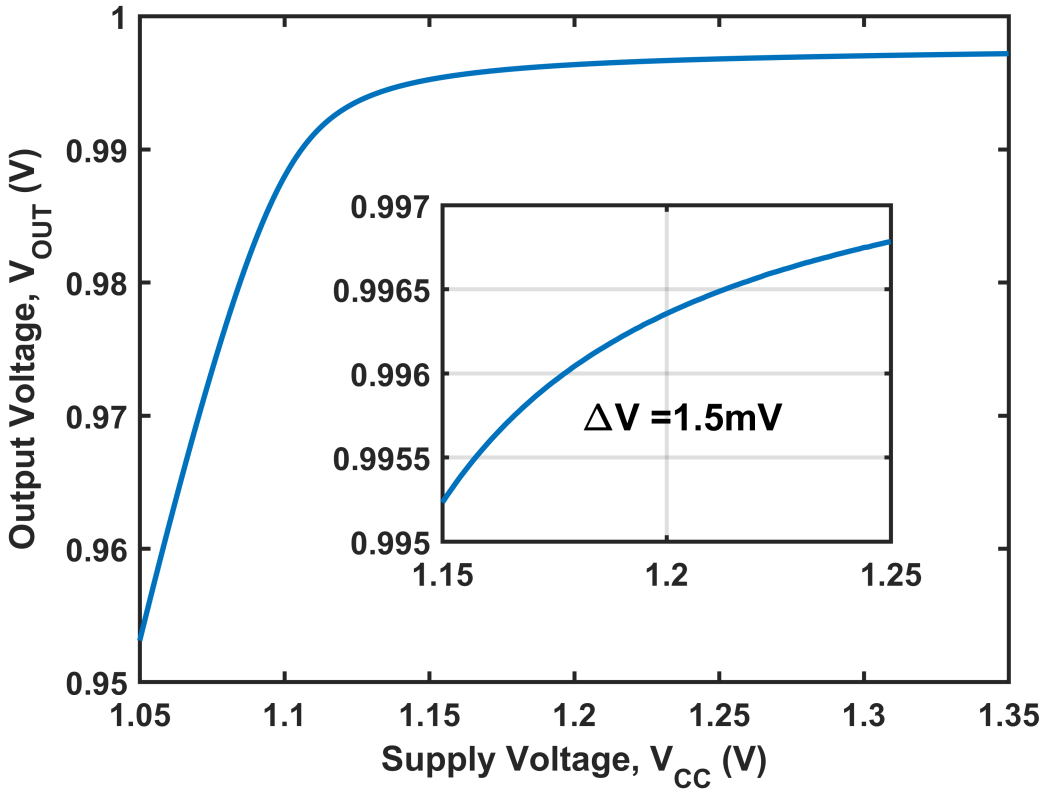


Figure 5.3: Quiescent Current Consumption

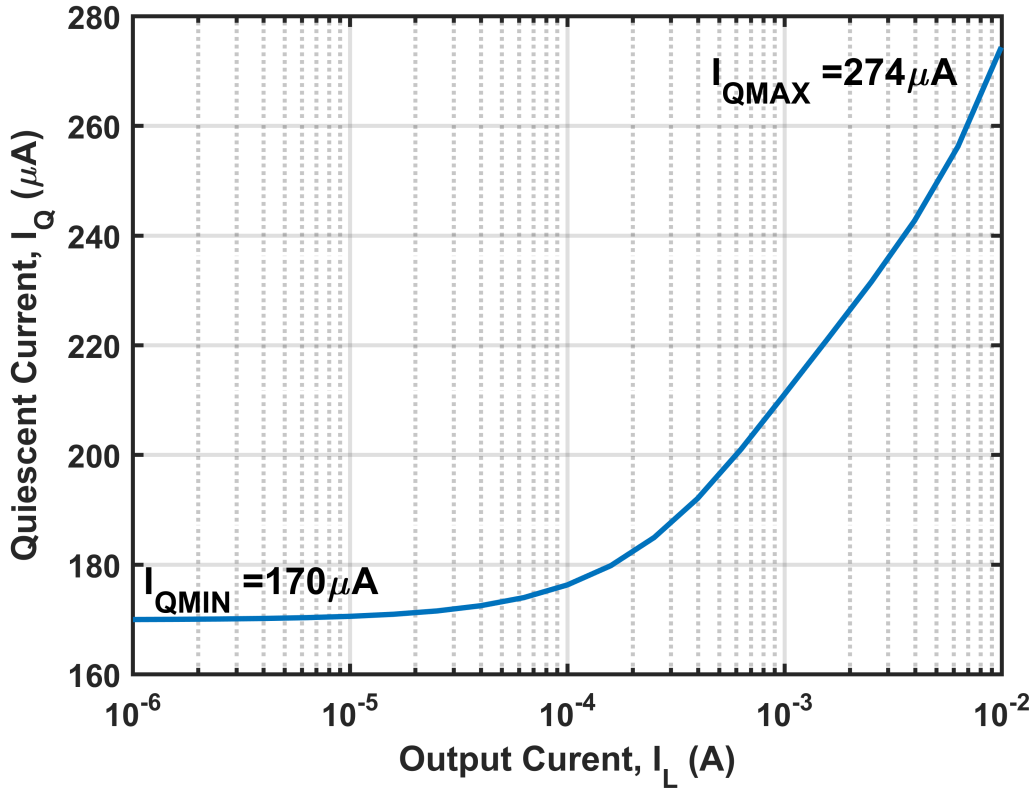


Figure 5.4: Supply Rejection

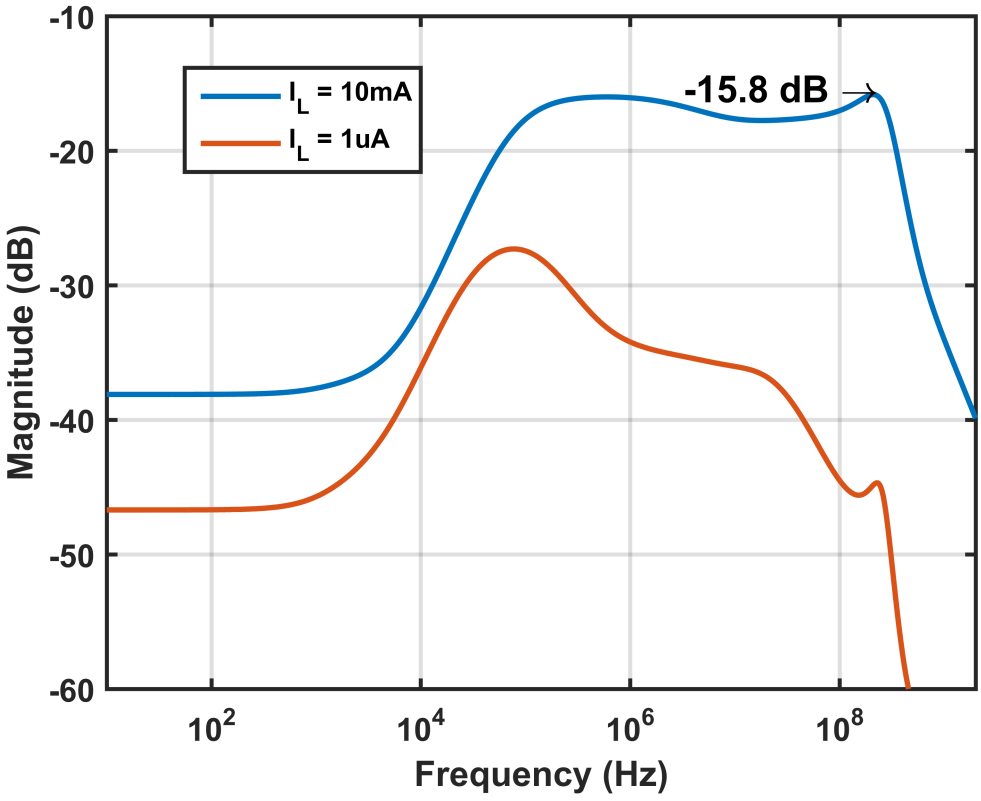


Figure 5.4 shows the supply rejection of full load and almost no-load. Since the FVF draws power from the output node, reducing load current any further would not have significant effect on the PSR graph. For the fast loop, the worst case (at max load) phase margin is 61° (refer to Figure 5.6 on page 35), which is why we see a slight peaking in the supply rejection graph. To remove peaking completely a phase margin of >75° is required which is expensive from a quiescent current point of view.

Figure 5.5 shows the open loop gains of the slow loop with different load currents. Even though the slow loop looks unstable, feed-forward compensation from the fast loop keeps the system stable [16]. To simulate this the loop was broken at the gate of the pass transistor, with a dummy circuit as the capacitive load.

Figure 5.5: Slow Loop Gain

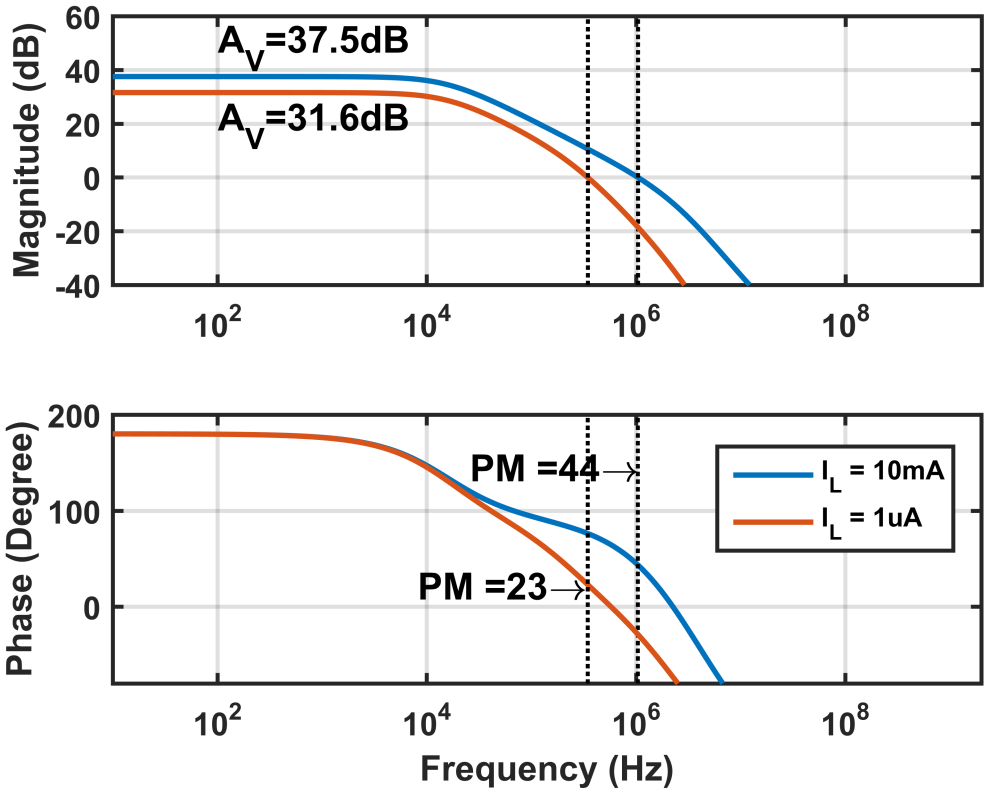


Figure 5.6: Fast Loop Gain

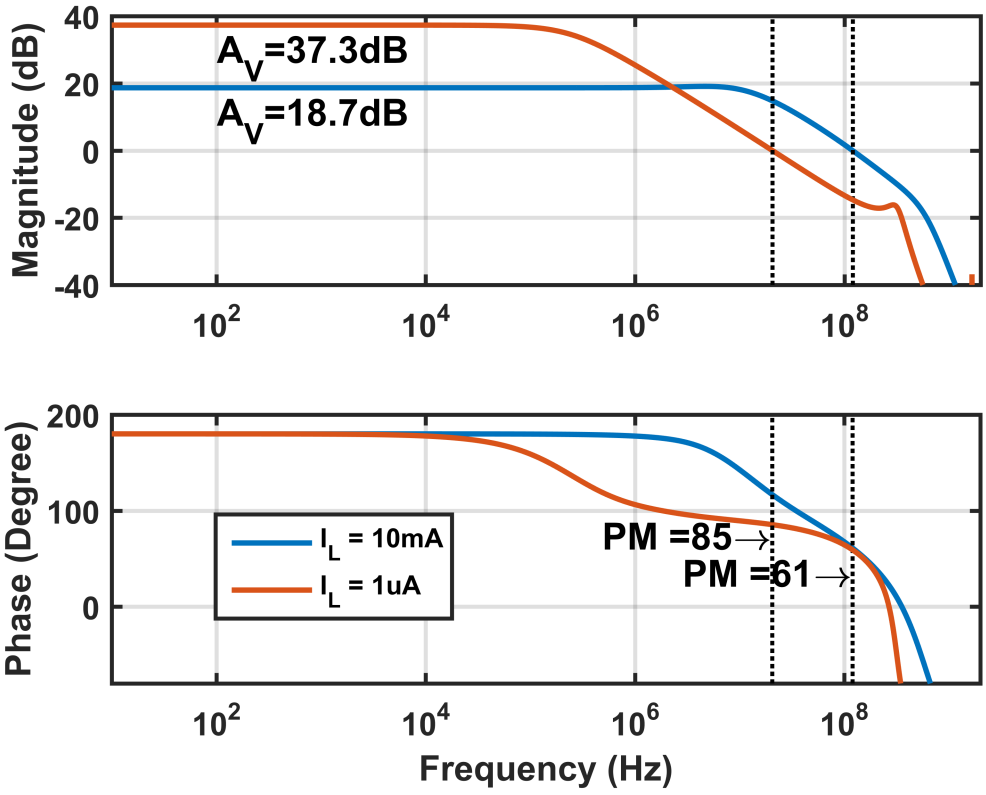


Figure 5.6 shows the open loop gains of the fast loop for full and no load current. To simulate the open loop gain, the loop was broken at the input of the buffer (or output of the FVF) as all the other possible nodes in the loop are low-impedance nodes. Like in the case of the slow loop, a dummy circuit was used as a capacitive load so as to get an accurate result.

Figure 5.7 shows the effect of a load step from no-load to full-load in a time-spam of 100 ps. The subplot below is a zoomed in version of the same graph showing the droop more clearly. Even though the circuit responds to the step within 4 ns, it takes more than 7.1 μs to settle. This is because of the high-gain slow loop. The little dip around 6 ns on this graph is due to the crossing over of V_{GATEs} and V_{GATEf}. These are plotted on the same time-scale in Figure 5.8.

Figure 5.7: V_{OUT} Response to a Load Step

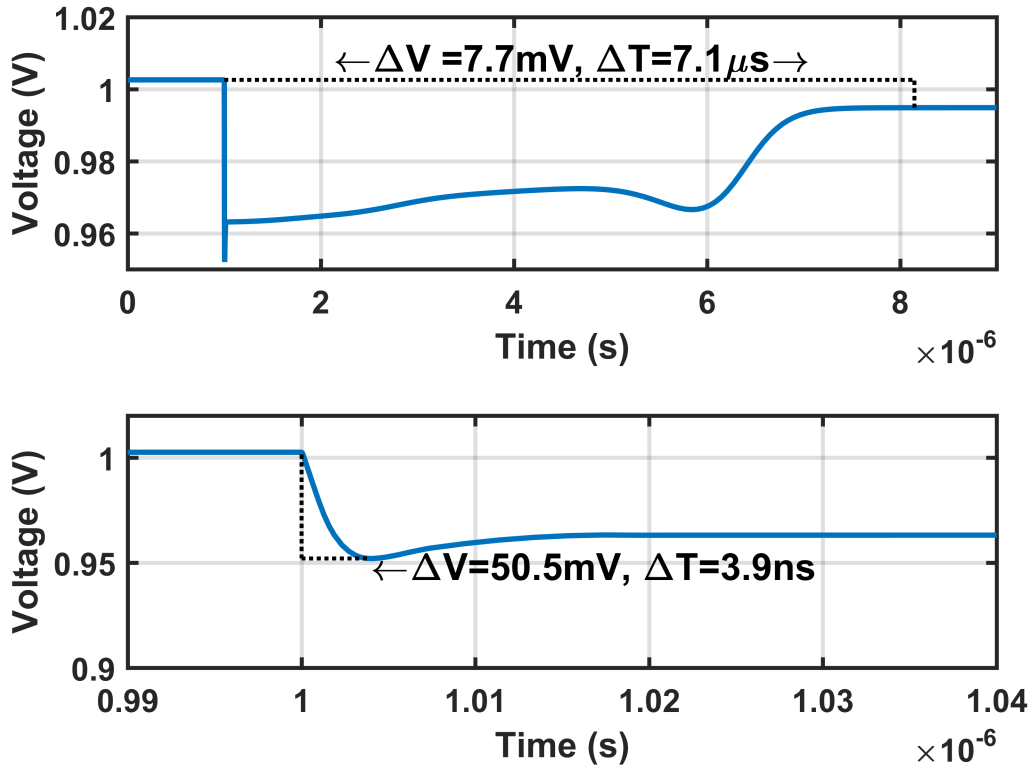
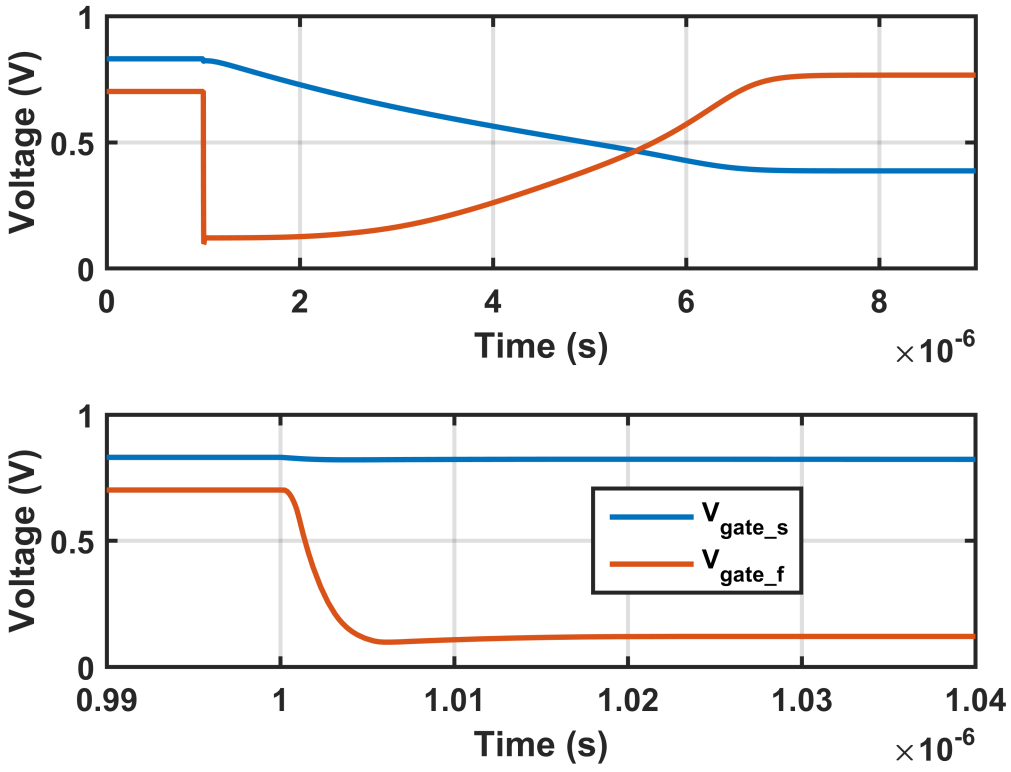


Figure 5.8: Internal Nodes Response to a Load Step



CHAPTER 6

CONCLUSION

Research for this thesis involved setting up a system to decouple the design of DC regulation and supply rejection. The aim of the design is also to have a state-of-the art LDO that has full spectrum supply rejection. As we can see from Table 6.1, the current design is comparable to if not better than other designs in the literature, while maintaining full spectrum supply rejection.

As mentioned in Chapter 5, most of the quiescent current in the current design at low load currents is through the FVF stage. However, as we can see from Figure 5.6, with really high phase margin the FVF's current can be significantly reduced to improve current efficiency. Additional work can be done to implement this current scaling FVF stage, as well as a transient block which would be required if the quiescent current of the FVF stage is reduced. With reduced gate capacitors in newer technologies, this design will only improve.

$$FOM = T_R \times \frac{I_Q}{I_{LMAX}} = \frac{\Delta V \times C_{OUT} \times I_Q}{I_{LMAX} \times I_{LMAX}} \tag{6.1}$$

Table 6.1: Comparison of State-of-the-Art LDOs

Publication	[13]**TCIS14**	[10]**JSSC13**	[17]**JSSC12**	**This Work**
Technology	65nm	180nm	45nm	180nm
V_{OUT}(V)	1	1.6	0.9-1.1	1.0
V_{DO}(V)	0.15	0.2	0.085	0.2
I_{Q}(A)	50-90μ	55μ	12m	170-274μ
I_{MAX}(mA)	10	50	42	10
Cap(pF)	140	128	1460	400
V_{PSR} (dB@Hz)	-15@1G -12@5G	-70@1M -37dB@10M	N/A	Worst Case -15.8dB@150M
$\Delta V@T$ (mV@ns)	82@0.2	80@100	N/A	51@0.1
Load Reg (mV/mA)	11/10	7/100	3.5/42.4	6.2/10
Line Reg (mV/V)	37.1	N/A	N/A	15
Tr(s)	1.15n	N/A	288p	3.9n
FOM(ps)	5.74	264	62.4	34.6

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