# PHASE-LOCKED LOOP USING TIME-BASED INTEGRAL CONTROL

BY

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THESIS

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# ABSTRACT

This thesis explores the time-based techniques in the context of phase-locked loop (PLL) implementation. Many studies of the topic have been performed in the past. Functioning as an effective replacement of passive capacitors, time-based integrators using oscillators prove to be more area efficient and highly digital when implemented in integrated circuits. To better explore their potential area saving benefits, the time-based techniques are implemented to serve the integral control of a type-II PLL. A comprehensive analysis is performed to evaluate the pros and cons of the new techniques. In particular, the noise and power trade-off of having additional oscillators in the system is explained in detail. The analyses are verified with a prototype PLL fabricated in 65 nm CMOS technology. The prototype PLL occupies an active area of only 0.0021 $mm^2$ and operates across a supply voltage range of 0.6 V to 1.2 V providing 0.4-to-2.6 GHz output frequencies. At 2.2 GHz output frequency, the PLL consumes 1.82 mW at 1 V supply voltage, and achieves 3.73 $ps_{rms}$ integrated jitter. This translates to an $FoM_J$ of -226.0 dB, which compares favorably with state-of-the-art designs while occupying the smallest reported active area. With the application of time-based techniques in clocking circuitry, the proposed time-based integral control PLL shall present a viable alternative to the conventional purely analog or digital PLL architectures.

# ACKNOWLEDGMENTS

The project would not be possible without the support of many people. Many thanks to my advisor, Professor Hanumolu, who patiently read and edited numerous revisions of my poor writings for publication. Also thanks to my group members, Guanghua and Romesh, who stayed up late and made the tapeout experience less formidable as the deadline approached. Also, thanks to my parents who have supported me throughout the years and provided me with such a great opportunity to study at the University of Illinois. Finally, special thanks to the project for giving me a good taste of exhausting tapeout preparation yet an overwhelming sense of achievement when the output signals showed up on the scope.

# TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

# CHAPTER 1

# INTRODUCTION

Phase-locked loops (PLLs) are widely used in analog, digital, RF, and embedded systems to generate a high frequency clock from a low frequency reference clock. Modern communication systems have developed sophisticated schemes to transmit multi-media data in a power efficient manner. Thanks to the invention of integrated circuits (ICs) and sustaining Moore's law of IC process technology, system-on-chips (SoCs) of modern communication systems support customers with functionalities way beyond text or voice data transmission. To make such high-level utility possible, modern processors of SoCs are improved from the aspect of not only processing speed but, more importantly, the potential to handle information transmitted through various carrier media, ranging from commonly observed audio voice to high speed Ethernet for sharing photos and video streams. To prevent the data transmission from interfering with daily conversation, analog and digital modulation have to be applied to the raw data, converting it to a dedicated frequency band for further processing. To properly coordinate such process, a high frequency clock signal is required, which is usually obtained through usage of a frequency synthesizer. Most frequency synthesizers employ phase-locking to achieve desired high frequency clock with accuracy defined by system specifications [1]. Modern SoCs usually employ multiple PLLs to cater to varying demands of modules such as multi-core processors, memories, I/O interfaces, and power management [2]. If each of these PLLs occupies large area, the total area occupied by PLLs will become a significant portion of the SoC area. Therefore, it is important to implement these PLLs in an area efficient manner without degrading their jitter or increasing power consumption.

## 1.1 Charge-pump Based Analog PLL

Figure 1.1 shows one commonly employed phase-locked loop (PLL) architecture, in which such a frequency synthesizer could be implemented [3]. A phase/frequency detector (PFD) first measures the phase difference between the input reference and feedback clock signal and generates an output pulse accordingly. The output pulse of PFD then controls the charge-pump block and generates control current which changes according to the measured phase difference at the input of PFD. The control current is converted to control voltage after passing through a loop filter, which is implemented as a series connection of resistor and capacitor (shown in Fig. 1.1). The control signal

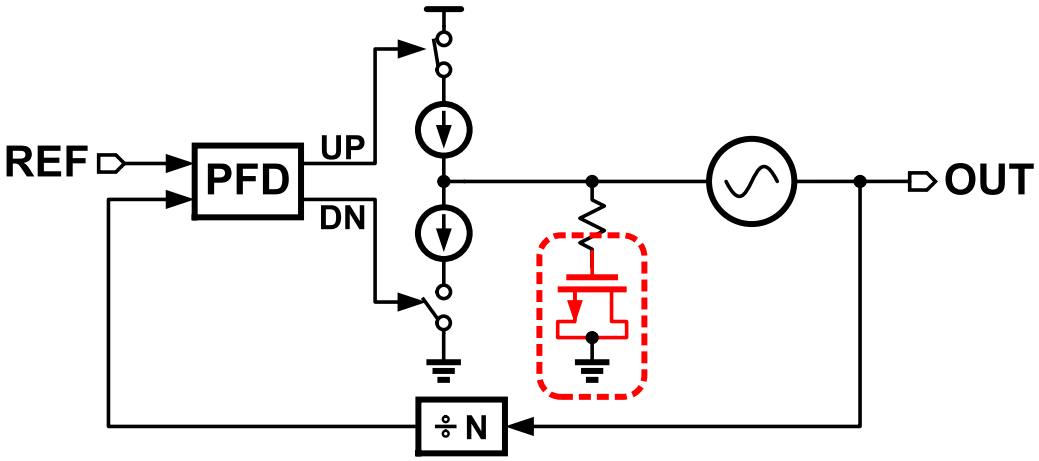


Figure 1.1: Schematics of a charge-pumped based analog PLL.

then adjusts the output frequency of the voltage-controlled oscillator (VCO) to minimize the phase error between reference and feedback clock. Therefore, the operation of the PLL could be viewed as a negative feedback system which forces the phase error (measured between reference and feedback clock) to be zero in steady state. Notice that a divider is inserted in the feedback path, which implies that the output frequency would be locked to $N \cdot F_{REF}$, where $F_{REF}$ represents the frequency of the reference signal. The divider ratio, N, could be independently selected to produce the desired high frequency signal as shown in Fig. 1.2. In this case, the simulation testbench is run with divider ratio $N = 4$. The performance of the PLL is usually described using time domain metric number, jitter, which quantizes the uncertain positions of clock transition edges at a given frequency due to the presence of noise. Since PLL essentially functions as a feedback loop in phase domain, the phase

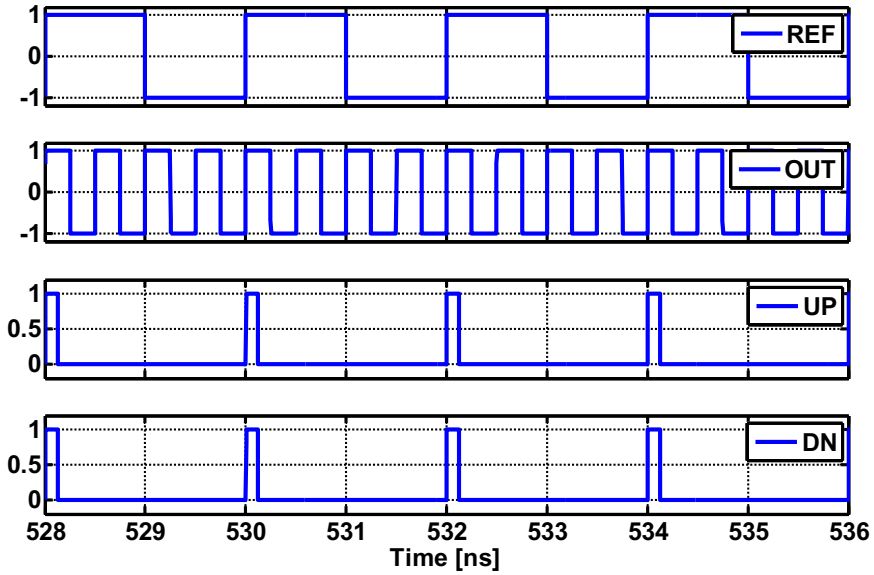


Figure 1.2: Time domain waveforms of charge-pumped based analog PLL.

noise output with respect to all noise sources is shown in Fig. 1.3. The time domain jitter can be calculated from the total output phase noise using Eq. (1.1):

$$\sigma_{\Delta T} = \sqrt{\int_0^{\infty} S_{\Phi_{OUT}}^{Total}(f)} \cdot \frac{T_{VCO}}{2\pi} \tag{1.1}$$

where $T_{VCO}$ is the period of the output frequency. Referring to Fig. 1.3, we can easily identify the low-pass behavior of the total output phase noise, and also band-pass behavior of the VCO phase noise measured at the output. Furthermore, in most cases of PLL design, the phase noise of the VCO is the dominant noise source. In order to reduce the noise contribution from the VCO, one way is to allow more power consumption for the VCO design which helps improve the phase noise to some extent. On the other hand, as we have seen from the output phase noise plot, the bandwidth of the PLL shall be increased so that more inherent suppression of the VCO noise is provided by the feedback loop. To ensure the loop stability while pushing the bandwidth higher, the loop response must place a zero at the appropriate frequency to keep the phase margin of the loop. As a result, the capacitor value of the loop filter tends to become difficult to integrate on chip. For example, achieving a PLL bandwidth of 3 MHz and phase margin of 70° requires a capacitance of 300 pF (with R = 1 KΩ) to place the loop stabilizing zero

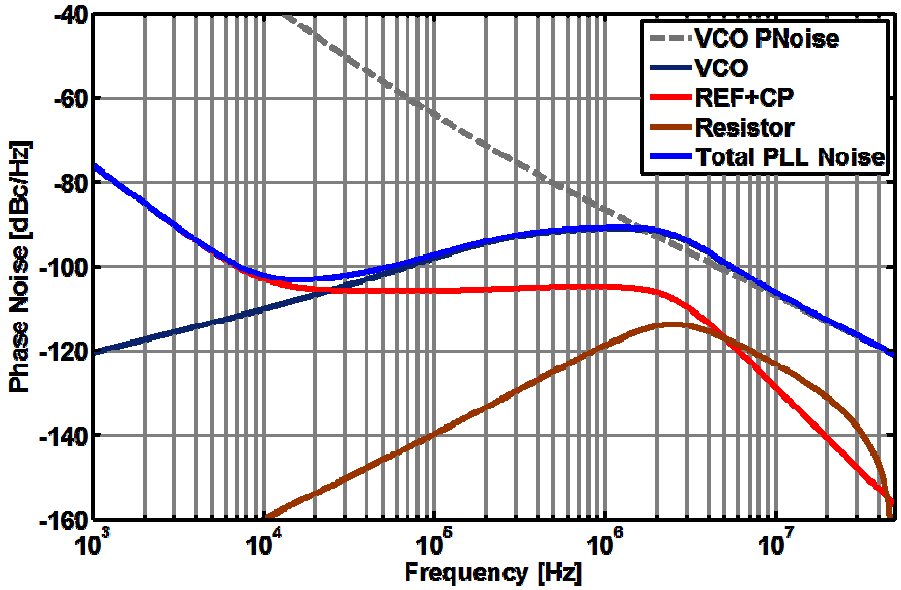


Figure 1.3: Simulated output phase noise of charge-pump based PLL.

frequency at 10 times lower than the PLL bandwidth. In 65 nm CMOS process, with capacitor density of 1fF/$\mu$m$^2$, this capacitance occupies an active area of 0.3 mm$^2$. For this reason, loop filter capacitor occupies large area and is typically the major bottleneck in reducing PLL area. Process scaling further exacerbates this issue because: (a) increasing oscillator gain increases the needed capacitor value, and (b) leakage current prohibits the usage of high-density MOS capacitors.

## 1.2 Digital PLL

To circumvent the noise-power trade-off discussed in Section 1.1, digital PLLs (DPLLs) offer a means to eliminate the capacitor by implementing a loop filter in the digital domain [4]. As shown in Fig. 1.4, integral control of the digital PLL is realized by using a digital accumulator in place of a capacitor. A time-to-digital converter (TDC) acts as a digital phase detector (DPD), digitizing phase difference between the reference clock and divider output and feeding it to the digital loop filter (DLF). A digital-to-analog converter (DAC) converts the DLF output to analog voltage and drives the VCO, implementing a digitally-controlled oscillator (DCO), towards phase/frequency

lock. A major drawback of a DPLL is the degraded jitter performance due to

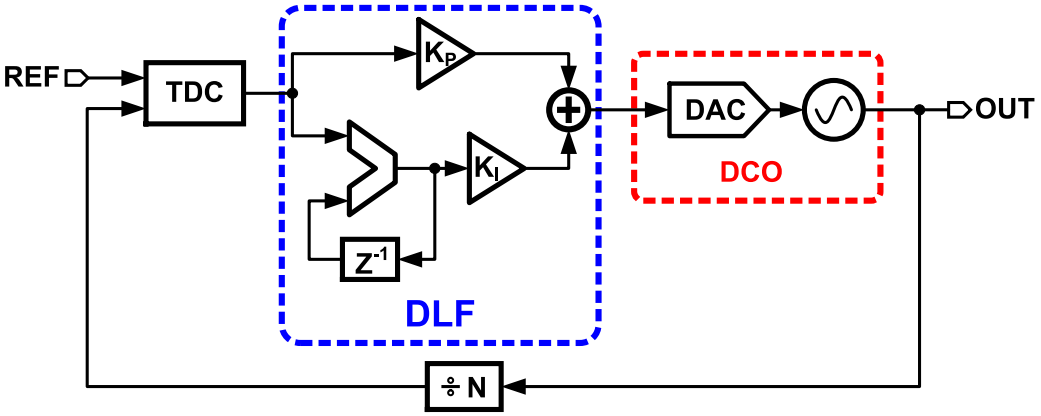


Figure 1.4: Schematics of a digital PLL.

the quantization error of TDC. In contrast to the analog PFD, under locked condition of the loop, TDC output dithers between two states. During the dithering, the digitally-controlled VCO output phase accumulates following the TDC output pulses. This behavior is illustrated in Figure 1.5. The direction of the phase accumulation changes according to the TDC output so that on average the overall output phase remains locked with respect to the reference signal. However, the output phase error attributed to TDC is limited by the resolution of the TDC, eventually measured as deterministic jitter at the PLL output [4]. Furthermore, in most cases, the proportional path gain of

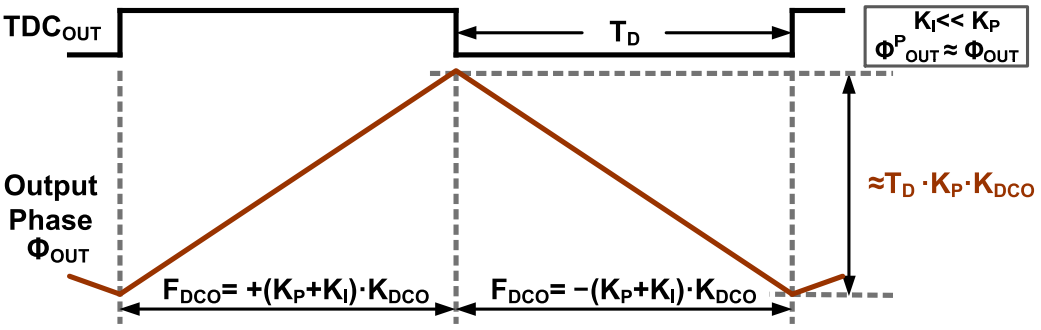


Figure 1.5: Illustration of TDC dithering and DCO phase accumulation.

DPLL is designed to be much larger than the integral path gain to make the loop response over-damped. As a result, the TDC quantization noise leaks to the output through a proportional path, appearing as one of the dominant noise sources in the system. Besides TDC, DCO also introduces quantization noise into the system. Specifically, the DAC that is used to interface between

DLF and VCO inevitably quantizes and converts the input analog signals to digital control words. The main sources of quantization noise in the DPLL system are summarized in Figure 1.6. Compared to analog implementation,

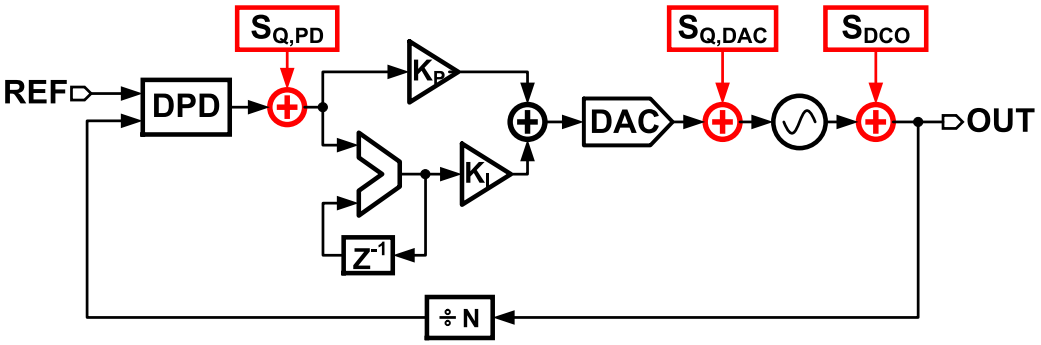


Figure 1.6: Quantization noise in DPLL.

DPLL introduces quantization noise in addition to existing phase noise of the VCO. This issue is best explained considering two main noise sources of DPLL, namely the quantization noise due to TDC and phase noise due to the VCO block of the DCO. The noise transfer function, defined as the ratio of output phase noise to input noise source, is plotted with respect to TDC quantization noise and DCO phase noise. As shown in Fig. 1.7, the loop

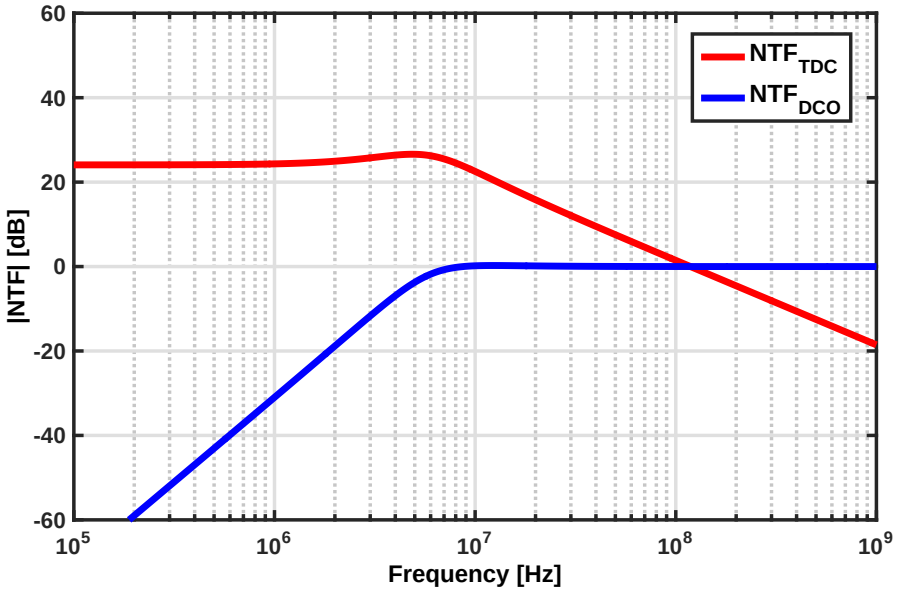


Figure 1.7: Noise transfer function of $S_{Q,TDC}$ and $S_{Q,DCO}$.

suppression to TDC behaves as a low-pass filter, yet that to DCO behaves

as a high-pass filter. The bandwidth of the two filtering response is exactly equal to the DPLL loop bandwidth. Consequently, reducing the contribution of TDC quantization error by filtering imposes conflicting noise bandwidth requirements. For instance, suppressing TDC quantization error by lowering the PLL loop bandwidth increases the contribution of VCO phase noise and vice versa. On the other hand, designers could improve the jitter performance by reducing the noise source through usage of a high resolution TDC or a VCO with better phase noise performance. However, the high-performance requirements of both lead to increase of power consumption.

## 1.3 Hybrid PLL

Based on the observation that most of the TDC quantization error in a DPLL leaks to the output through the digital proportional path, a hybrid architecture was proposed to utilize quantization-free proportional path and digital integral path [5]. As shown in Fig. 1.8, hybrid PLL (HPLL) implements the proportional path very similarly to the analog architecture, measuring the input phase error with PFD instead of TDC. A bang-bang phase detector (BBPD) is then connected to provide additional sign information and serve as a 1-bit TDC for the digital integral control. The conflicting noise-power

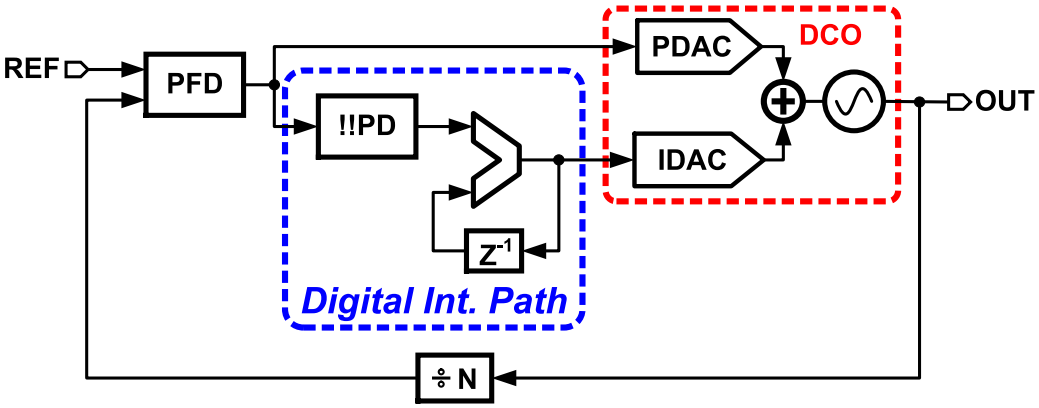


Figure 1.8: Schematics of a hybrid PLL.

trade-off seen in the DPLL is resolved since the analog proportional path completely eliminates the quantization error and the loop bandwidth could be independently designed to suppress VCO phase noise. The quantization noise from the digital control path could be easily suppressed by lowering

the noise-bandwidth for the integral control path, which has negligible effect on VCO phase noise suppression thanks to the hybrid implementation [5]. However, HPLL often requires a high resolution DAC, for the same reason as in the DPLL design, that converts accumulator output into a control voltage for the VCO. One way to implement high-resolution DAC consists of programmable arrays of capacitors, which usually take up a large area [6]. An alternative DAC implementation using a delta-sigma architecture may reduce the number of unit elements in the DAC, but the low pass filter required to filter high frequency quantization error typically occupies large area [5]. The published hybrid architecture circumvents conflicting noise bandwidth trade-offs in conventional DPLL [4] by combining an analog PLL based proportional path with a digital PLL based integral path. Yet area consumption of digital implementation counteracts the benefits brought by the architecture.

## 1.4 Overview

The simplicity of the analog PLL provides excellent jitter performance, yet the passive capacitor needed for the loop filter takes up large chip area. On the other hand, the digital PLL better utilizes the process scaling advantage, yet addition of quantization noise degrades the PLL performance and overall power efficiency of the system. To overcome the drawbacks of the conventional analog/digital architectures, we seek a novel implementation approach to serve as an alternative to state-of-the-art PLL designs. The rest of the thesis is organized to illustrate our proposed time-based architecture and discusses the trade-offs we made in comparison to the conventional architectures. Chapter 2 reviews the concept behind time-based integrators and illustrates the proposed PLL architecture using a time-based integrator. Chapter 3 discusses design challenges of the architecture, and demonstrates both advantages and disadvantages compared to analog, digital and hybrid approaches mentioned. Chapter 4 presents the method we used to overcome the drawbacks of applying the pulse-width-modulated control signal when implementing the time-based integrator. The measurement results are presented in Chapter 6, and Chapter 7 concludes the thesis with a summary of key points.

# CHAPTER 2

# TIME-BASED PLL: THEORY AND ARCHITECTURE

Figure 2.1 shows the block diagram of the time-based integrator [7]. It consists of a duty-cycle-to-current, or for short D2I, converter, ring oscillator, and phase detector (PD). The D2I converter, $D2I_{INT}$, takes input duty cycle and converts it to a control current for the current controlled ring oscillator $CCRO_I$. The oscillator output is then passed into a PD which measures the phase difference with respect to a reference input. The details of the time-based integrator are presented in the rest of the chapter.

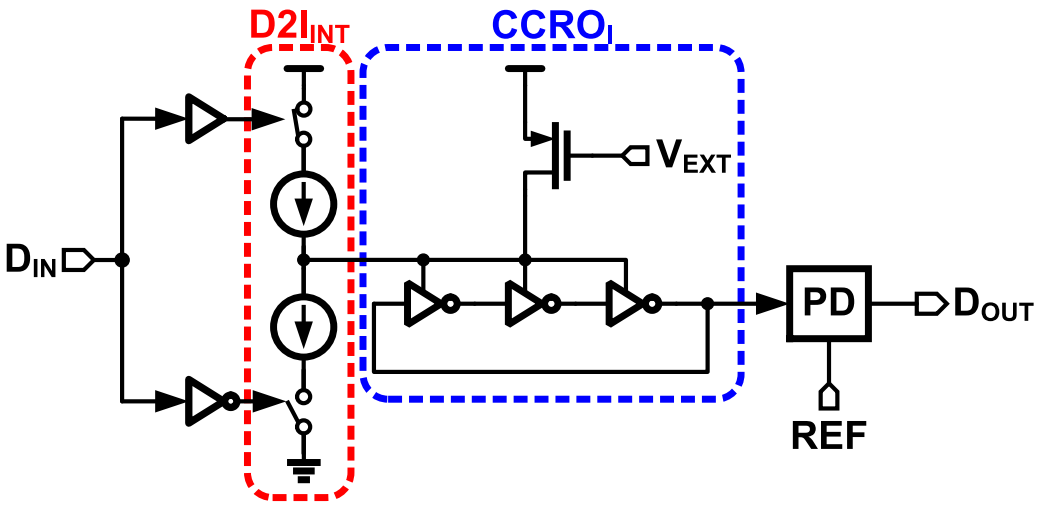


Figure 2.1: Schematic of a time-based integrator.

## 2.1 Ring Oscillators as Integrators

To elaborate the function of an oscillator as an integrator, it is instructive to review the behavior of a voltage (or current) controlled ring oscillator based integrator [7, 8, 9]. Consider a voltage controlled ring oscillator or VCRO, which takes an input signal x(t). Then the output of the VCRO y(t) can be

calculated as:

$$y(t) = \cos(2\pi f(t) + \Phi) \tag{2.1}$$

Therefore, a VCRO converts an input voltage to a clock signal with a variable frequency f(t) (Fig. 2.2). For an ideal oscillator, the output frequency would be proportional to the input voltage such that

$$f(t) = K \cdot x(t) \tag{2.2}$$

where K denotes the constant of proportionality between the voltage and frequency. The constant is defined as the oscillator gain and is commonly denoted as $K_{VCRO}$ (Fig. 2.3). While oscillator application typically lies in

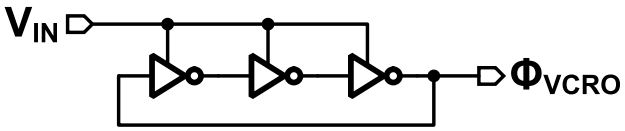


Figure 2.2: VCRO converts input control voltage to a clock frequency.

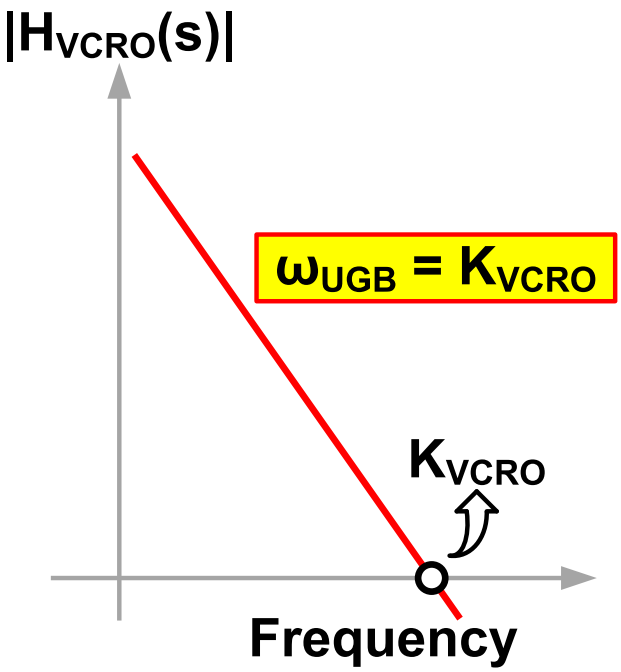


Figure 2.3: Illustration of VCRO gain.

the output frequency as a controlled clock source, the phase of the oscillator output often proves to be useful. For instance, in PLL design the output

oscillator phase is used to compare with the reference phase, and the phase error serves the feedback loop to reduce the jitter at the output. To use oscillators as integrators, what we are interested in is the output phase instead of output frequency. Because output frequency of a VCRO phase is proportional to its input voltage, and phase is the integral of frequency, VCRO acts as a voltage to phase integrator with the following transfer function:

$$\frac{\mathrm{F_{VCRO}(s)}}{\mathrm{V_{in}(s)}} = \mathrm{K_{VCRO}} \implies \frac{\Phi_{\mathrm{VCRO}}(\mathrm{s})}{\mathrm{V_{in}(s)}} = \frac{\mathrm{K_{VCRO}}}{\mathrm{s}} \tag{2.3}$$

where $\mathrm{V_{in}}$ and $\Phi_{\mathrm{VCRO}}$ denote VCRO input voltage and output phase, respectively. Following Eq. (2.3), we observe that the oscillator can be viewed as an integrator with voltage input and phase output. Note that the integration from frequency to phase is a true lossless integration independent of transistor imperfections and supply voltage. In practical implementation, the parasitics may show up as a pole to the overall transfer function, yet the functionality of the integrator is not affected for frequencies below the parasitic pole. To better characterize the frequency response of the integrator, we observe that the time constant of the VCRO integrator is equal to the inverse of its voltage-to-frequency gain, $\mathrm{K_{VCRO}}$. Up to this point, we realize that an alternative to integrator other than passive capacitor could be through a voltage-controlled oscillator, which could be implemented as a ring oscillator to save the chip area.

In the implementation of the time-based PLL, current controlled ring oscillators are used, which work similarly to VCRO, except that the input control is realized as current. This is for the simplicity of implementing the addition function in the loop response. Voltage-mode addition requires additional complexity in the circuits, while current-mode addition could be realized by simply shorting at the summing nodes. In the following discussion we will show the proposed time-based PLL architecture, and present the loop analysis for the PLL design.

## 2.2 Proposed Architecture

Refer to the block diagram shown in Fig. 2.1; note that the time-based integrator includes additional blocks besides the ring oscillator. This is due

to the fact that the integrator through the oscillator is only voltage/current to phase. While voltage/current could be easily accessed in the circuits, phase-domain information is typically beyond reach without explicit interface between phase and voltage/current. As a result, in order to use CCRO as an alternative integrator to a capacitor, a means to convert CCRO output phase into a voltage (or current) signal is needed. To implement such conversion, a phase detector (PD) is used. The PD's operation is explained as follows. It takes two input signals, compares them and generates output pulses that match the difference between them, for example, the rising edges of the two input signals. Hence, the PD output pulse reflects the phase difference if one of the inputs is chosen to be a fixed reference clock, and the average DC output of the PD would correspond to a phase difference measure. In this case, the CCRO phase will be compared with the phase of a reference clock, and generates a pulse width modulated signal as shown in Fig. 2.4 [7, 8]. The pulse width, or equivalently the duty cycle, of the PD output is a measure of the CCRO output phase. Note that if the CCRO free running frequency is not equal to the reference frequency, phase error accumulates indefinitely, which saturates the PD output. Therefore, to prevent PD saturation, any system using a CCRO integrator must ensure that CCRO frequency is equal to the reference frequency in steady state. Now consider

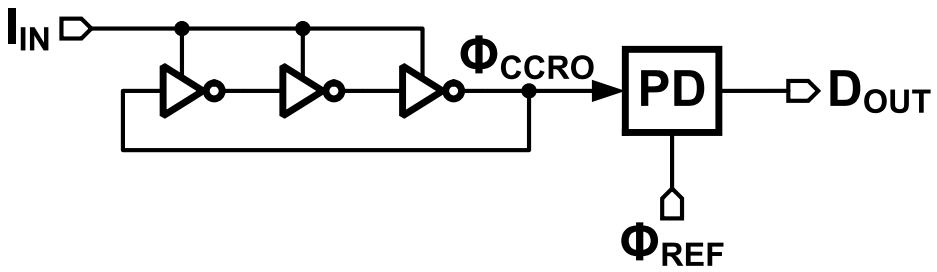


Figure 2.4: Schematic of ring oscillator based integrator.

the time-based integrator in the context of a PLL as shown in Fig. 2.1. The PLL compares input reference clock with output clock using a PFD which generates UP and DN pulses. The PFD output is first converted to current by $D2I_{PROP}$ and directly passed to the output oscillator. This implements the proportional path of the PLL much similarly to [5]. Meanwhile, PFD output is converted to current through $D2I_{INT}$ and subsequently integrated by a CCRO denoted as $CCRO_I$. Because output of $CCRO_I$ is in phase do-

main, it is first converted into a 2-level pulse width modulated voltage signal by a phase detector (PD). As shown in Fig. 2.5, the PD output with a phase difference of $\pi$ radians between $CCRO_I$ and reference shows a duty cycle of 50%. The duty cycle changes to 25% when the phase difference is changed to $0.5\pi$. A D2I converter, $D2I_{PD}$, converts 2-level PD output into current

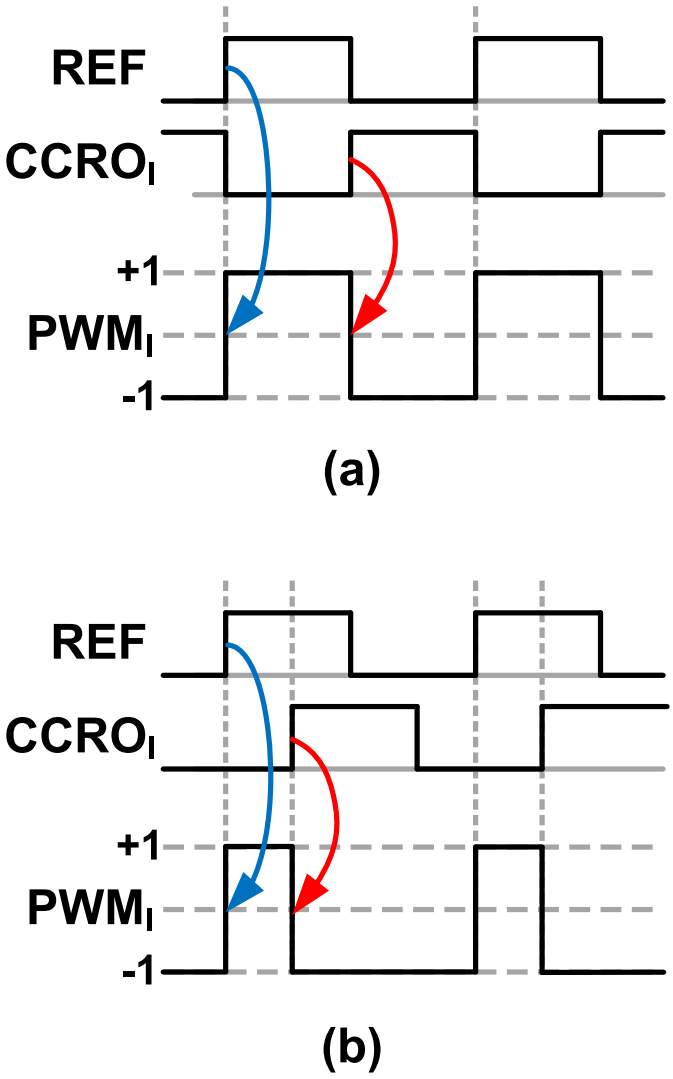


Figure 2.5: Time domain waveforms of time-based integrator with input phase difference of (a) $\pi$, and (b) $0.5\pi$.

and feeds it into the main CCRO, $CCRO_M$, thus implementing the integral control of the Type-II response. It is worth mentioning that even though PD output takes only CMOS levels, no quantization error is introduced by the time-based integrator.

Figure. 2.1 is redrawn as a block diagram shown in Fig. 2.6 to facilitate

the small signal analysis of the PLL loop. Output oscillator $CCRO_M$ is controlled via the proportional and integral path D2I converter currents, denoted as $I_{PROP}$ and $I_{INT}$, respectively. The pulse-width modulated PD output is converted into current using D2I converters. The gain of the D2I

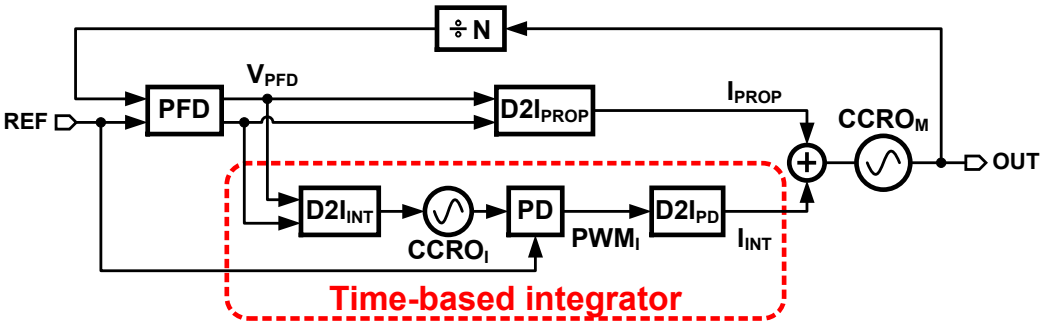


Figure 2.6: Type-II PLL with time-based integrator in the integral path.

converter, $K_{D2I}$, is equal to:

$$K_{D2I} = I_{D2I} \tag{2.4}$$

where $I_{D2I}$ is the output current of the D2I converter when the input duty cycle is equal to 100%. PFD output is converted to equivalent current by $D2I_{PROP}$ in the proportional path resulting in a proportional path gain of:

$$K_P = \frac{I_{PROP}}{V_{PFD}} = K_{D2I,PROP} \tag{2.5}$$

where $K_{D2I,PROP}$ is the gain of $D2I_{PROP}$ and is equal to $I_{D2I,PROP}$. On the other hand, PFD output is integrated by $CCRO_I$, and the PD converts $CCRO_I$ phase to a pulse-width modulated signal, which is converted to current output, $I_{INT}$, by $D2I_{PD}$. Denoting PFD output by $V_{PFD}$, the transfer function of the time-based integrator is equal to:

$$H_{INT}(s) = \frac{I_{INT}(s)}{V_{PFD}(s)} = K_{D2I,INT} \cdot K_{PD} \cdot K_{D2I,PD} \cdot \frac{K_{CCRO_I}}{s} \tag{2.6}$$

Therefore, integral path gain is then equal to:

$$K_I = K_{D2I,INT} \cdot K_{PD} \cdot K_{D2I,PD} \cdot K_{CCRO_I} \tag{2.7}$$

Loop gain of the proposed PLL is thus calculated as:

$$\mathrm{LG(s)} = \frac{1}{\mathrm{N}} \cdot \mathrm{K_{PFD}} \cdot \frac{\mathrm{K_{CCRO_M}}}{\mathrm{s}} \cdot \left( \mathrm{K_P} + \frac{\mathrm{K_I}}{\mathrm{s}} \right) \tag{2.8}$$

By equating this to the loop gain of a conventional charge-pump based PLL, loop parameters needed to achieve the desired loop bandwidth and phase margin can be calculated.

# CHAPTER 3

# TIME-BASED PLL: DESIGN CHALLENGES

As shown in Chapter 2, the proposed time-based PLL architecture realizes integral control based on the pulse width modulated (PWM) signal at the output of the PD. While CMOS level control signal introduces no quantization into the system, the usage of PWM signal to directly control oscillator frequency in the time-based integrator introduces spurious tones at the output. These tones should be carefully managed to reduce the impact on the jitter performance of the PLL. In this chapter, we first discuss the mechanisms behind the spurious tones introduced by the PWM control. Specifically, it will be shown that spurious tones are caused by: (i) frequency mismatch between reference frequency $F_{REF}$ and free-running frequency of $CCRO_I$ and (ii) high frequency contents of PWM signal fed to $CCRO_M$ without adequate filtering. Then, we present the noise analysis of the time-based PLL, identifying major noise contributors in the system.

## 3.1 Spurious Tones due to Frequency Offset

The time-based integrator requires additional PD to convert the phase-domain integrated output to either voltage or current domain. In order for PD to properly generate an output with varying duty cycle, additional reference clock signal has to be provided. Consider an alternative representation of the integral path shown in Fig. 3.1. The PFD output, $V_{PFD}$, is converted

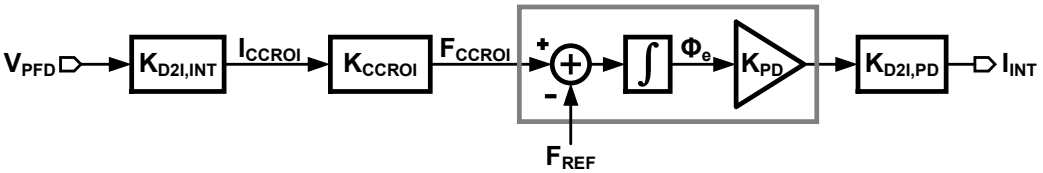


Figure 3.1: Small signal model of the time-based integral path.

to current, $I_{CCRO_I}$, by a D2I converter that has a gain of $K_{D2I,INT}$. $CCRO_I$ converts D2I output current to frequency $F_{CCRO_I}$ with a gain of $K_{CCRO_I}$. The phase error, $\Phi_e$, seen by the PD is proportional to the integral of frequency offset defined as $F_{CCRO_I} - F_{REF}$ and is equal to:

$$\Phi_e(t) = \int_0^t (F_{CCRO_I}(\tau) - F_{REF})d\tau \tag{3.1}$$

Because of the integration of frequency error, $CCRO_I$ frequency must be equal to $F_{REF}$ in steady state to prevent PD output from saturating. Otherwise, the phase error accumulates indefinitely and causes the PD output duty cycle to keep increasing from 0% to 100% and wrap around continuously. Denoting frequency of $CCRO_I$ as the sum of its free-running frequency, $F_{FR}$, and additional deviation due to the input control current, $F_{CCRO_I}$ is equal to:

$$F_{CCRO_I} = F_{FR} + I_{CCRO_I} \cdot K_{CCRO_I} \tag{3.2}$$

where the sign of the current is consistent with the sign of the measured frequency error between $F_{CCRO_I}$ and $F_{REF}$. Equations (3.1) and (3.2) indicate that the average $CCRO_I$ input current shall be zero, or in other words the phase error reaches zero in steady state, if and only if the $CCRO_I$ free-running frequency $F_{FR}$ is equal to $F_{REF}$. Under this condition, average PFD output equals zero and the PLL locks without any static phase offset, barring any offsets introduced in the proportional path.

On the other hand, if the free-running frequency of $CCRO_I$ is not equal to $F_{REF}$, the loop must account for the frequency difference ($\Delta F = F_{REF} - F_{FR}$) by applying adequate control current to $CCRO_I$ such that:

$$F_{CCRO_I} = (F_{REF} - \Delta F) + I_{CCRO_I} \cdot K_{CCRO_I} \tag{3.3}$$

Because $\Delta F$ causes PD output duty cycle to constantly increase (or decrease if $\Delta F$ is negative), $CCRO_M$ frequency also increases constantly. The PFD detects $CCRO_M$ frequency deviation and produces UP/DN pulses that minimize frequency errors associated with both $CCRO_I$ and $CCRO_M$. From Eq. (3.3), control current necessary to make $F_{CCRO_I} = F_{REF}$ is equal to:

$$I_{CCRO_I} = \frac{\Delta F}{K_{CCRO_I}} \tag{3.4}$$

Because non-zero $I_{CCRO_I}$ requires PFD output to be non-zero in steady state, PLL has to lock with a static phase offset so as to simultaneously achieve $F_{CCRO_I} = F_{REF}$ and $F_{CCRO_M} = N \cdot F_{REF}$. The static phase offset resulting from $\Delta F \neq 0$ can be calculated as:

$$\Phi_{OS} = \frac{I_{CCRO_I}}{K_{D2I,INT} \cdot K_{PFD}} \tag{3.5}$$

Static phase offset causes modulation of $CCRO_M$ control through the proportional path, which manifests as reference spur. Using narrow-band approximation [10], the magnitude of the reference spur can be calculated as:

$$\text{Spur magnitude [dB]} = 20 \log \left( \frac{F_{BW}}{F_{REF}} \cdot N \cdot \Phi_{OS} \right) \tag{3.6}$$

where $F_{BW}$ is the loop bandwidth, and N is the feedback division ratio. The deterministic jitter resulting from the reference spur is equal to:

$$DJ_{OUT} = \frac{2}{\pi} \cdot T_{OUT} \cdot 10^{\text{Spur[dBc]}/20} \tag{3.7}$$

With $F_{REF} = 275$ MHz, and 10 MHz bandwidth, a 1% error in $CCRO_I$ free-running frequency gives rise to a reference spur of -27 dB, which translates to a deterministic jitter of 12.9 ps at an output frequency of 2.2 GHz.

## 3.2 Spurious Tones due to PWM Control

The second set of spurious tones in the proposed time-based controller arises from controlling $CCRO_M$ with PD output in the form of pulse width modulated signal as explained in Chapter 2. The PD output is a 2-level signal with the requisite duty cycle that tunes $F_{CCRO_M}$ to be equal to $N \cdot F_{REF}$. While modulating the frequency with current output of $D2I_{INT}$ makes the average frequency of $CCRO_M$ to be equal to $N \cdot F_{REF}$, perturbations of $CCRO_M$ frequency by the PWM signal manifest as spurious tones at the PLL output. In order to quantify the effect of PWM spurs, direct calculation following the loop analysis presented earlier (see Chapter 2) may be too complicated for an intuitive understanding of the possible degradation. To better illustrate the spurious tones caused by the PWM control signal, we take into account

the spurious tones when the PLL is locked. Under this circumstance, the integral path oscillator settles to a fixed frequency, thereby PD generating a pulse with fixed duty cycle. As a result, the control signal is simply a square pulse with duty cycle corresponding to the possible phase offset at the input of the PFD. Consequently, the spurs resulting from PWM control can be calculated by representing steady state integral control signal, $\mathrm{PWM_{INT}}$, assuming its duty cycle is D and amplitude is $\mathrm{I_0}$, using its Fourier series representation as [11]:

$$\mathrm{PWM_{INT}(t) = D{\cdot}I_0 + \sum_{n=1}^{\infty} \frac{4I_0}{n\pi} {\cdot} sinc\left(n\pi \frac{2t_r}{T_{PWM}}\right) {\cdot} sin(n\pi D) {\cdot} cos(n\omega_{PWM} t)} \quad (3.8)$$

where $\mathrm{T_{PWM}} = 2\pi/\omega_{\mathrm{PWM}}$, and $\mathrm{t_r}$ denotes the transition time of $\mathrm{PWM_{INT}}$ (assuming equal rise and fall time of the current pulse). Considering $\mathrm{t_r} = 0$, for simplicity, and only the fundamental component at $\omega_{\mathrm{PWM}}$, it can be shown that the modulation generates $\mathrm{CCRO_M}$ output of the following form [10]:

$$\mathrm{V_{CCRO_M}(t) = \sum_{n=0}^{\infty} J_n(\beta_0) \cdot \cos[(\omega_c \pm n\omega_{PWM})t]} \quad (3.9)$$

where $\mathrm{J_n}(\beta_0)$ represents the $n$th order Bessel function, and $\mathrm{J_0}$ represents the modulation index due to the fundamental component and $\beta_0$ is given by:

$$\mathrm{\beta_0 = \frac{K_{CCRO_M}}{\omega_{PWM}} \cdot \frac{2I_0}{\pi} \cdot \sin(D\pi)} \quad (3.10)$$

Under narrow-band approximation, spurious tones due to PWM modulation can be estimated using Eq. (3.9) and (3.10) as:

$$\mathrm{Spur\ magnitude\ [dB] = 20 \log \left[\frac{K_{CCRO_M}}{F_{PWM}} \cdot \frac{I_0}{\pi} \cdot \sin(D\pi)\right]} \quad (3.11)$$

Because $\mathrm{F_{PWM}} = \mathrm{F_{REF}}$, PLL output contains spurs at integer multiples of reference frequency.

It is possible to greatly suppress PWM modulation induced spurious tones by driving $\mathrm{CCRO_M}$ with the filtered PD output as illustrated in Fig. 3.2. However, a low bandwidth filter needed to adequately suppress the spurious tones may occupy a large area, thereby mitigating the area benefit offered by the time-based control. Using M-phase PWM control as described in [7, 9]

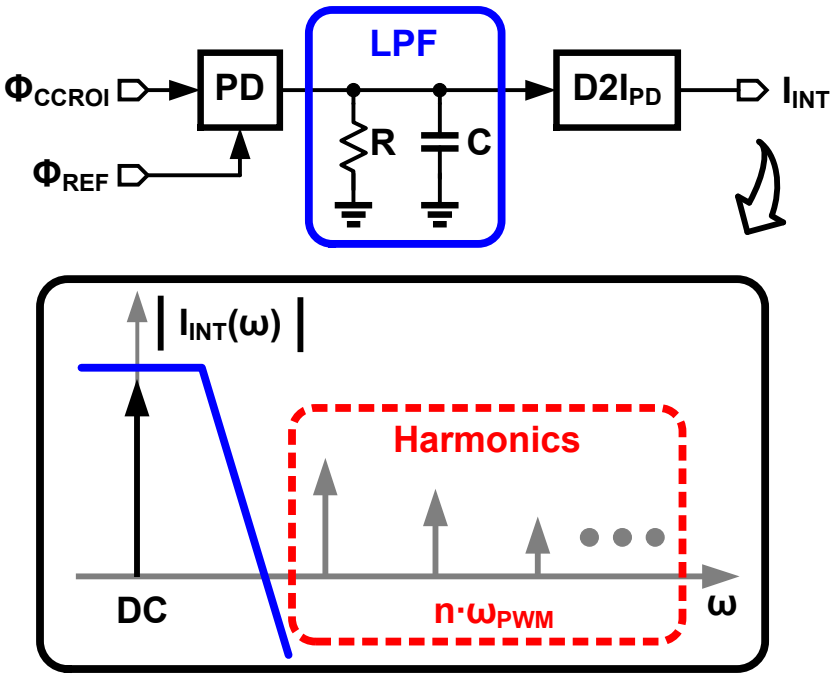


Figure 3.2: Illustration of spurious tones that arise from pulse-width-modulated control signal.

pushes spurious tones to M times the PWM frequency so that they can be filtered by a higher bandwidth filter, thus reducing the area penalty by nearly M times. This technique requires replicating single phase circuitry (CCRO buffer, PD, and D2I converters) M times, which increases the controller area and possibly exacerbates the spurious tones caused by mismatch between oscillator output and reference signal.

## 3.3 Noise Analysis

Besides the spurious tones, total phase noise appearing at the output dominates the measured jitter of the PLL output. In order to identify the phase noise contributor, we present the noise analysis of the time-based PLL in this section. Compared to a conventional capacitor-based integrator, an oscillator-based integrator adds more noise and degrades the PLL phase noise performance. To quantify all noise contribution in the system, the noise model of the proposed time-based PLL is shown in Fig. 3.3. The noise model of the integral path is shown in Fig. 3.3 (a), along with the noise model of the complete PLL shown in Fig. 3.3 (b). The output phase noise power

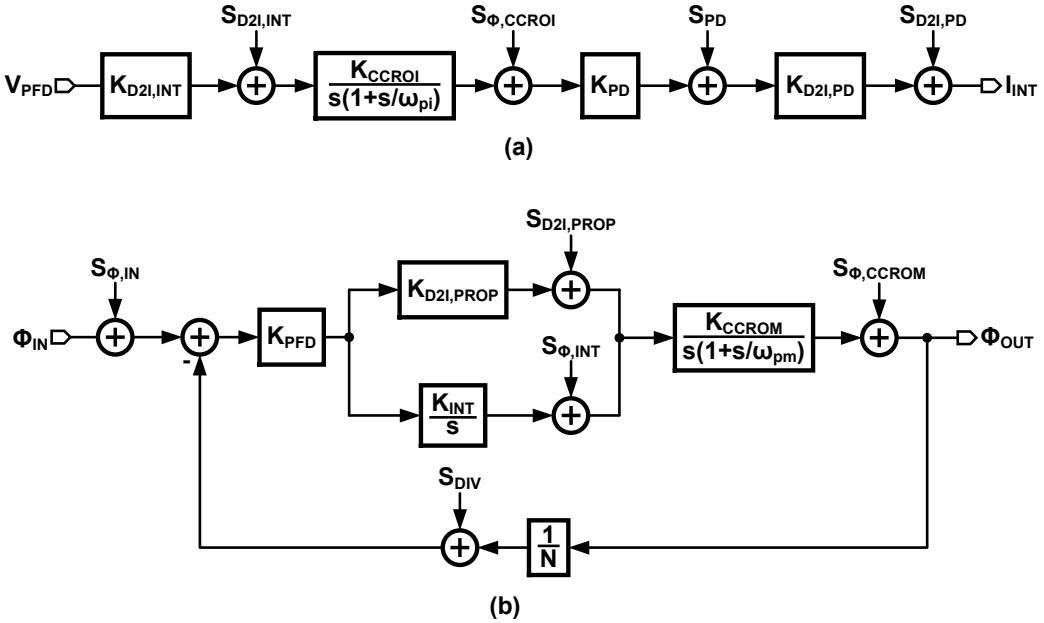


Figure 3.3: Noise model of (a) time-based integrator, and (b) complete PLL loop.

spectral densities of the oscillator, PD, and D2I converter are denoted as $S_{\Phi,CCRO_I}$, $S_{PD}$, $S_{D2I,INT}$, and $S_{D2I,PD}$, respectively. Taking the parasitic poles associated with $CCRO_I$ and $CCRO_M$ into account, the loop gain transfer function shown in Eq.(2.8) changes to:

$$LG(s) = \frac{\Phi_{OUT}(s)}{\Phi_{IN}(s)} = \frac{1}{N}\cdot K_{PFD}\cdot\frac{1}{1+s/\omega_{pm}}\cdot\frac{K_{CCRO_M}}{s}\cdot\left(K_{D2I_{PROP}} + \frac{K_{INT}}{s}\cdot\frac{1}{1+s/\omega_{pi}}\right) \tag{3.12}$$

where $\omega_{pm}$ and $\omega_{pi}$ denote the parasitic poles at the output of $CCRO_M$ and integrator $CCRO_I$, respectively. The noise transfer functions of $CCRO_M$ ($NTF_{OUT}^{CCRO_M}$) and $CCRO_I$ ($NTF_{OUT}^{CCRO_I}$) are equal to:

$$NTF_{OUT}^{CCRO_M}(s) = \frac{1}{1+LG(s)} \tag{3.13}$$

$$NTF_{OUT}^{CCRO_I}(s) = K_{PD}\cdot K_{D2I,PD}\cdot\frac{1}{1+s/\omega_{pm}}\cdot\frac{K_{CCRO_M}/s}{1+LG(s)} \tag{3.14}$$

where LG(s) is given by Eq. (3.12). The output referred noise of $CCRO_M$ and $CCRO_I$ is calculated to be:

$$S_{\Phi,OUT}^{CCRO_M} = \left|NTF_{OUT}^{CCRO_M}\right|^2\cdot S_{\Phi,CCRO_M} \tag{3.15}$$

$$S_{\Phi,OUT}^{CCRO_I} = \left|NTF_{OUT}^{CCRO_I}\right|^2 \cdot S_{\Phi,CCRO_I} \tag{3.16}$$

Plotting magnitude response of the two noise transfer functions, as shown in Fig. 3.4, illustrates that increasing the loop bandwidth helps suppress the in-band phase noise contribution from both $CCRO_M$ and $CCRO_I$. We

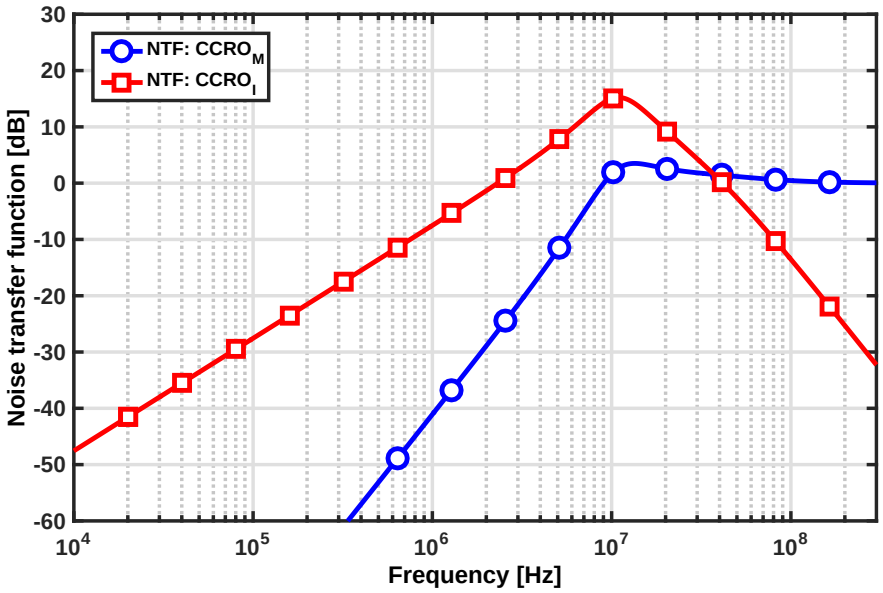


Figure 3.4: Simulated $CCRO_M$ and $CCRO_I$ phase noise transfer functions.

also note that noise from $CCRO_I$ experiences only first-order (slope of -20 dB/dec) suppression and therefore can be expected to contribute more noise as compared to that of $CCRO_M$.

Given with the power spectral density of the output phase noise, the corresponding output jitter can be calculated as follows:

$$\sigma_{\Delta\Phi}^2 = \int_0^\infty S_{\Phi_{OUT}}(f)df \tag{3.17}$$

Usually the jitter is defined in units of time. We can calculate the time-domain jitter using the following equation:

$$\sigma_{\Delta T}^2 = \sqrt{\int_0^\infty S_{\Phi_{OUT}}(f)df} \cdot \frac{T_{OUT}}{2\pi} \tag{3.18}$$

where $T_{OUT}$ is the period of the output clock. The output phase noise plots shown in Fig. 3.5, assuming that $CCRO_M$ and $CCRO_I$ have a phase noise of

-90 dBc/Hz and -94 dBc/Hz, respectively, at 1 MHz offset, show that $\mathrm{CCRO_I}$ dominates in-band phase noise. Using Eq. (3.18), the total integrated jitter obtained by integrating the phase noise is equal to 3 ps, of which $\mathrm{CCRO_I}$ accounts for 2.85 ps and $\mathrm{CCRO_M}$ for 1.06 ps.

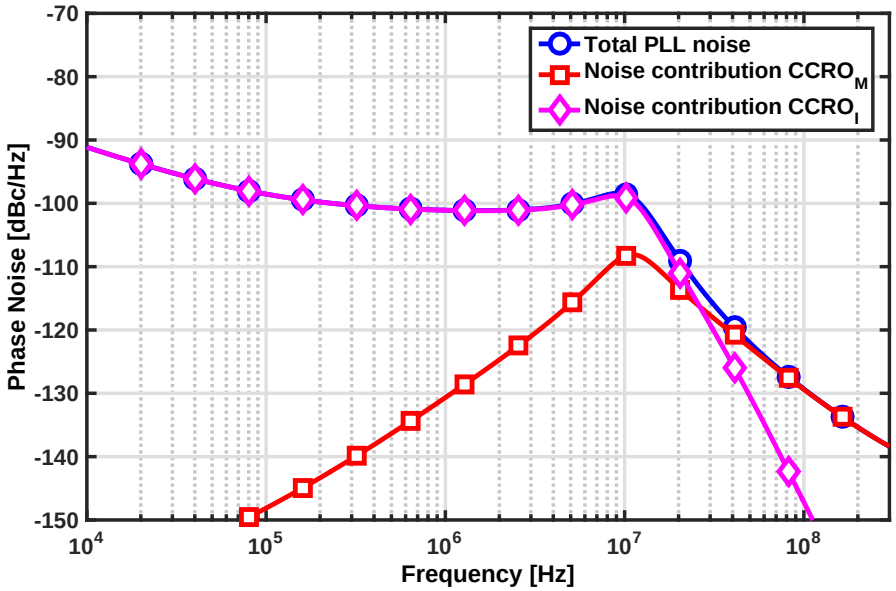


Figure 3.5: Simulated output phase noise plot.

# CHAPTER 4

# SPUR REDUCTION TECHNIQUES

In this chapter, we propose to use pseudo-differential architecture to overcome the spurious tone problems discussed in the previous chapter. The spur analysis in the previous section showed that the two main sources of spurs are: (i) free-running frequency error of $\mathrm{CCRO_I}$ from $\mathrm{F_{REF}}$ and (ii) modulation of $\mathrm{CCRO_M}$ control current by a PWM signal. Before discussing ways to mitigate these spurs, it is instructive to first evaluate the impact of PLL feedback on these spurs. To this end, we first calculate the phase deviations caused by control current perturbations as:

$$\frac{\Phi_{\mathrm{OUT}}(\mathrm{s})}{\mathrm{I_{INT}}(\mathrm{s})} = \frac{\mathrm{K_{CCRO_M}}/\mathrm{s}}{1 + \mathrm{LG}(\mathrm{s})} \tag{4.1}$$

where LG(s) is the loop gain of the PLL and is given by Eq. (2.8). Plotting Eq. (4.1) as shown in Fig. 4.1 (a) indicates a band-pass transfer characteristic with the peak located at around the PLL bandwidth. As a result, output phase is sensitive to control current perturbations that are in the vicinity of PLL bandwidth, while those away from it (either very low or very high frequencies) are suppressed by the loop in proportion to the ratio of PLL bandwidth to the spur frequency. Therefore, spur magnitude can be reduced either by lowering the PLL bandwidth or increasing the spur frequency. Because lowering the PLL bandwidth exacerbates $\mathrm{CCRO_M}$ phase noise, we consider ways to increase the spur frequency to improve spur suppression (Fig. 4.1 (b)).

To this end, we employ the pseudo-differential time-based integrator architecture shown in Fig. 4.2 [7, 8, 12]. Note that the pseudo-differential architecture implements a 2-phase PWM control [13]. The small signal model of the pseudo-differential integrator is shown in Fig. 4.3. It consists of a set of D2Is that convert pseudo-differential duty cycle input into current and drive a pair of matched ring oscillators. Two PDs compare CCRO output phases,

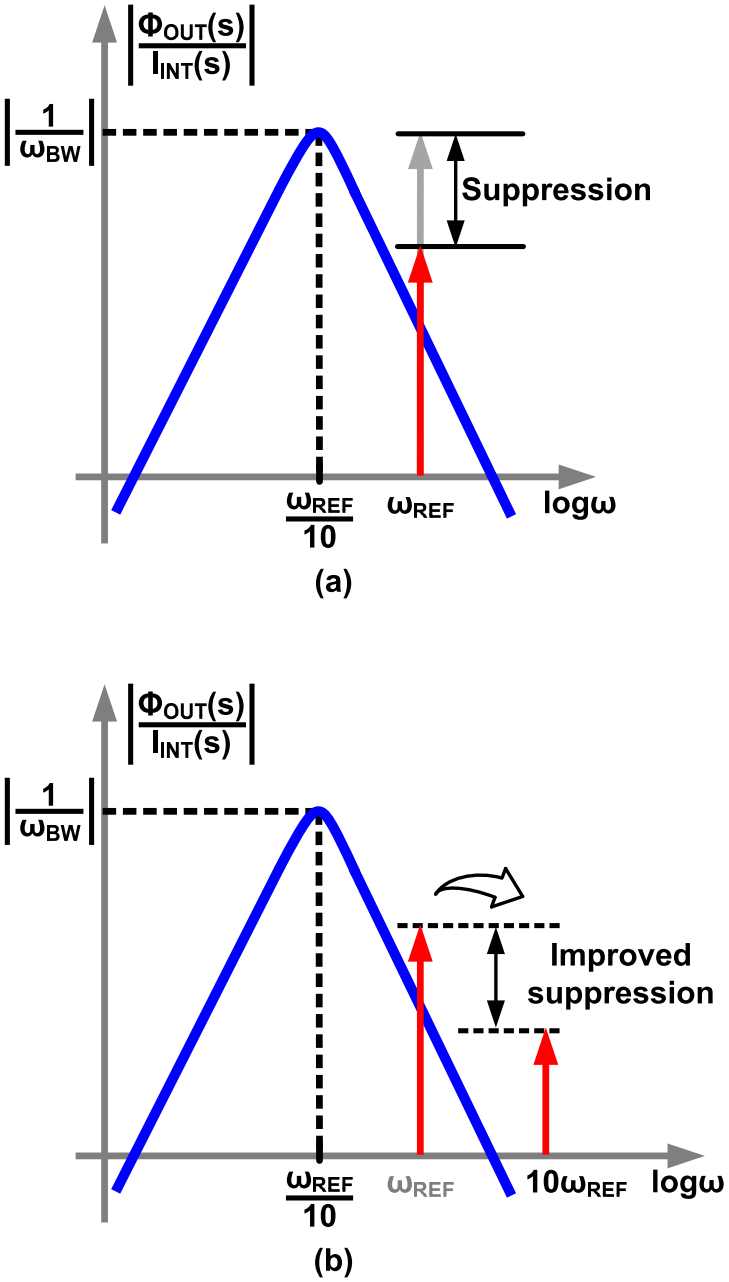


Figure 4.1: Illustration of inherent suppression of high frequency spur by PLL loop.

$\Phi_{INT,0}$ and $\Phi_{INT,180}$, and generate pseudo-differential PWM signals, $D_{OUT}$, and $\overline{D_{OUT}}$. This pseudo-differential integrator offers two main advantages compared to its single-ended counterpart. First, using two matched CCROs allows us to operate the integrator at any switching frequency independent of the reference frequency. Consequently, by choosing the free-running frequency of the two CCROs to be much higher than the reference frequency, the PWM control induced spurs can be pushed to a high frequency where they can be greatly suppressed by the bandpass transfer characteristic of the PLL. Second, ensuring good matching between the two CCROs reduces the static phase offset, which results in a smaller reference spur. However, the effectiveness of the pseudo-differential architecture depends on the matching between CCRO free running frequencies. The difference between the free-

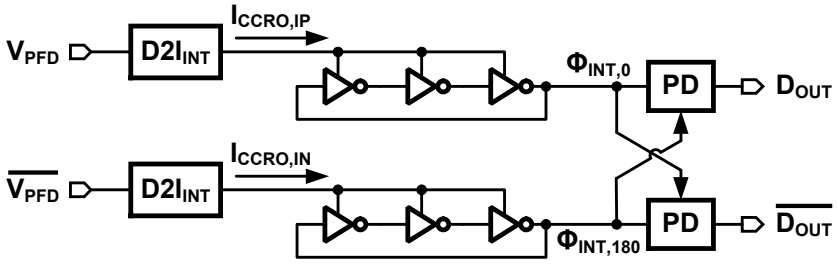


Figure 4.2: Pseudo-differential implementation of time-based integrator.

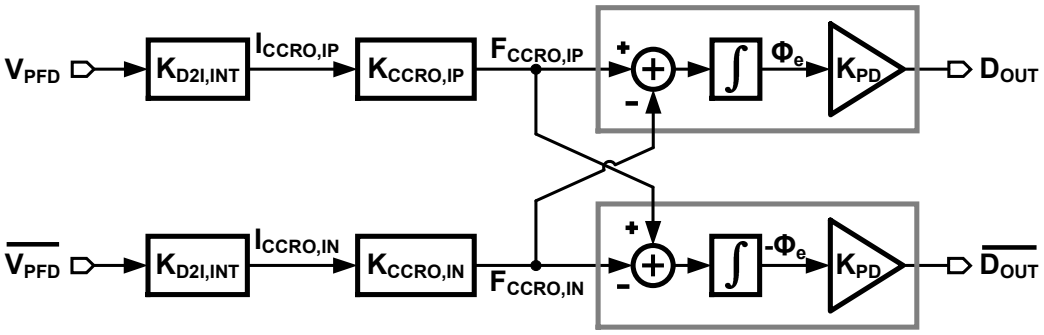


Figure 4.3: Small signal model of pseudo-differential time-based integrator.

running frequencies of the two CCROs, or equivalently $F_{CCRO_{IP}} \neq F_{CCRO_{IN}}$, appears as static phase offset, $\Phi_{OS,diff}$, as described earlier (Section 3.1) and is equal to:

$$\Phi_{OS,diff} = \frac{F_{CCRO_{IP}} - F_{CCRO_{IN}}}{K_{D2I_{INT}} K_{CCRO_I} K_{PFD}} \tag{4.2}$$

Note that Eq. (4.2) assumes no mismatch between the oscillator gain $K_{CCRO_{IP}} =$

$K_{CCRO_{IN}} = K_{CCRO_I}$. Reference spur caused by the pseudo-differential integrator can be calculated similarly to the single-ended case, and is estimated as:

$$\text{Spur magnitude[dB]} = 20\log\left(\frac{F_{BW}}{F_{REF}} \cdot N \cdot \Phi_{OS,diff}\right) - 20\log\left(\frac{F_{REF}}{F_{pm}}\right) \quad (4.3)$$

where $F_{pm}$ denotes the parasitic pole of $CCRO_M$. Spur magnitude calculated based on Eq. (4.3) is plotted in Fig. 4.4 assuming $CCRO_I$ free running frequency of 1 GHz and $K_{CCRO_I} = 3\,\text{MHz}/\mu\text{A}$. Spur magnitude obtained

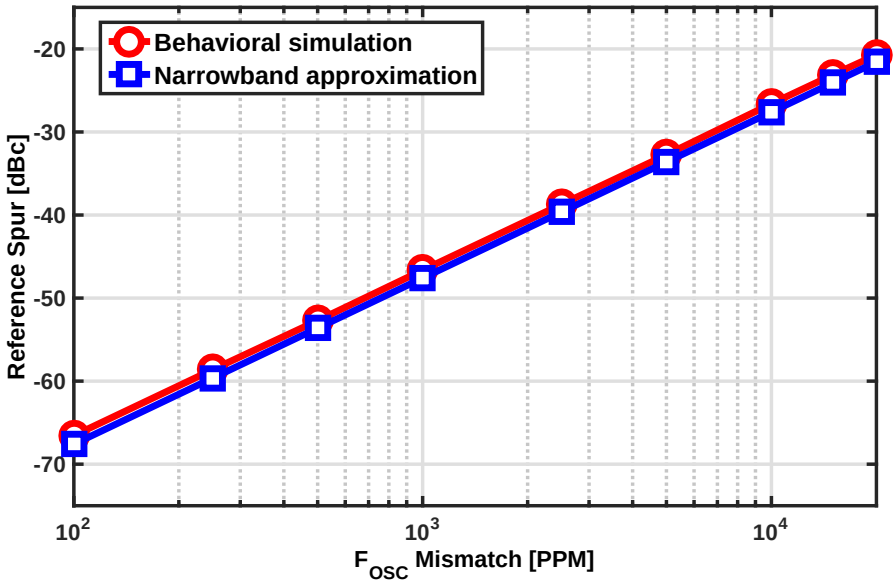


Figure 4.4: Reference spur versus free running frequency mismatch between pseudo-differential oscillators with (a) behavioral simulation, and (b) narrow-band approximation.

from behavioral simulations of the PLL is also plotted in Fig. 4.4. Compared to the simulation, calculation based on Eq. (4.3) indicates that narrow-band approximation well captures the spur performance degradation caused by $CCRO_I$ mismatch. Nevertheless, the analysis/simulations indicate that a spur magnitude of -45 dB can be achieved if the mismatch is kept within 1000 ppm, or 0.1% of the free-running frequency. In order to limit the spur magnitude caused by the integrator oscillator pairs, additional calibration shall be implemented to ensure the matching requirement is met. However, due to the time limitation we are not able to include additional circuitry, yet we do want to present our thoughts regarding the matching problem ex-

isting in the practical fabrication. For the time-based PLL, we choose to use inverter-based ring oscillators to save chip area. It is possible, however, for the frequency mismatch to exceed 0.1% easily between the free running frequencies of the two integral path oscillators. Monte-Carlo simulation of our oscillators is shown in Fig. 4.5. Based on the Monte-Carlo simulation,

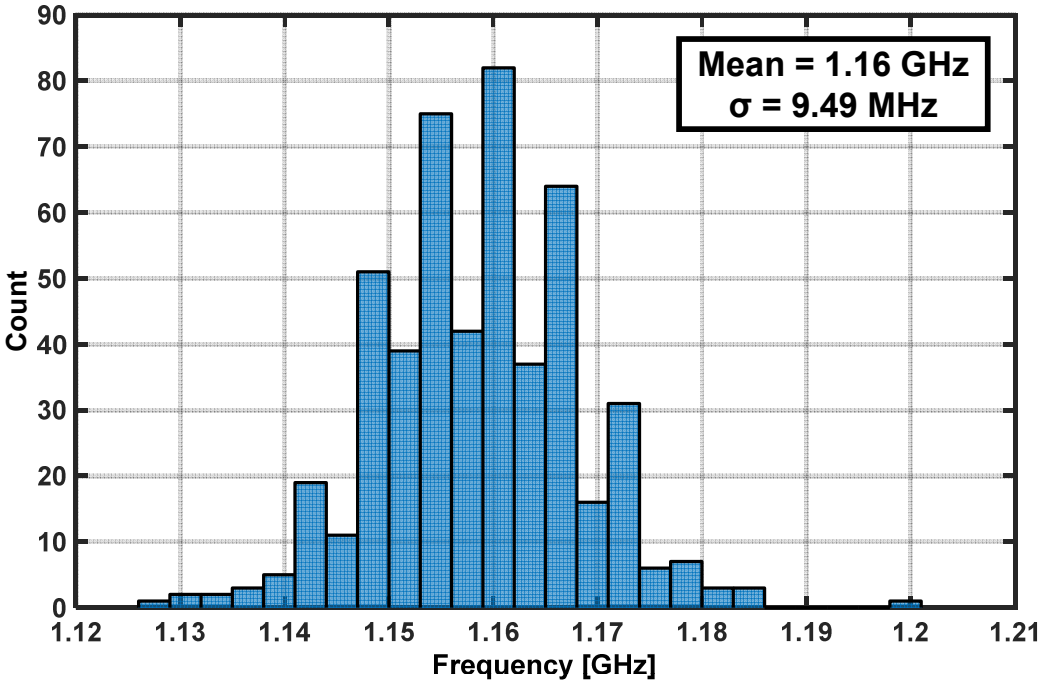


Figure 4.5: $\mathrm{CCRO_{IP/N}}$ Monte-Carlo simulation (500 points).

at a nominal frequency of 1.16 GHz, the standard deviation ($1\sigma$) of the mismatch is 9.49 MHz, which is equal to 0.8% or equivalently 8000ppm of the center frequency. If not corrected, this large frequency mismatch can lead to a large reference spur of magnitude -28 dB, severely degrading the jitter performance. To overcome such mismatch in chip fabrication, additional calibration loop must be implemented along with the core components of the PLL. In a practical realization, a coarse (5-bit) frequency locked loop can be used at start-up to bring $\pm 5\sigma$ frequency mismatch down to 1000ppm. Based on the tuning characteristic shown in Fig. 4.6, a frequency lock loop (FLL) must provide an offset current of about 25 $\mu$A at a nominal oscillation frequency of 1 GHz. With $\mathrm{K_{CCRO_{IP/N}}}$ estimated to be 3 MHz/A, the estimated area penalty of the FLL to cover the mismatch and process variation is about 0.0004 $\mathrm{mm^2}$, a very small portion of measured active area (0.0021 $\mathrm{mm^2}$) of the prototype PLL.

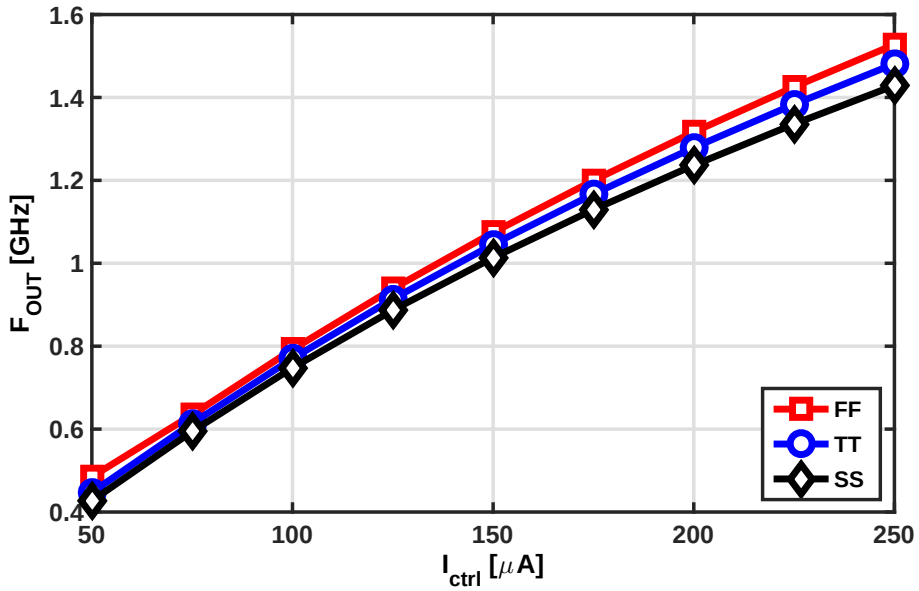


Figure 4.6: $\mathrm{CCRO_{IP/N}}$ tuning curve versus control current across process corners.

# CHAPTER 5

# BUILDING BLOCKS

In this chapter, the circuit implementation of the building blocks is presented. The complete block diagram of the prototype PLL is shown in Fig. 5.1. Section 5.1 discusses the implementation of the current-controlled ring os-

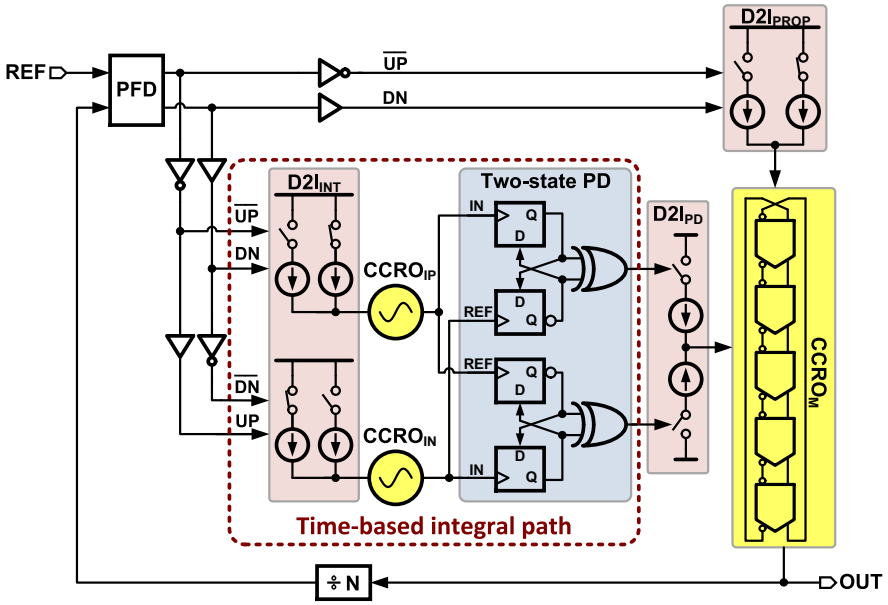


Figure 5.1: Complete block diagram of proposed time-based PLL.

cillator as well as the D2I converter which has been incorporated into the control portion of the CCRO. Section 5.2 describes the implementation of the phase detector.

## 5.1 Current-Controlled Ring Oscillator

The schematic of the current controlled ring oscillator is shown in Fig. 5.2. It is implemented using five current-starved pseudo-differential stages connected in a ring oscillator topology. The delay cell is composed of two CMOS

inverters whose outputs are coupled in a feed-forward manner using transmission gates to ensure differential operation [14]. An output buffer (not

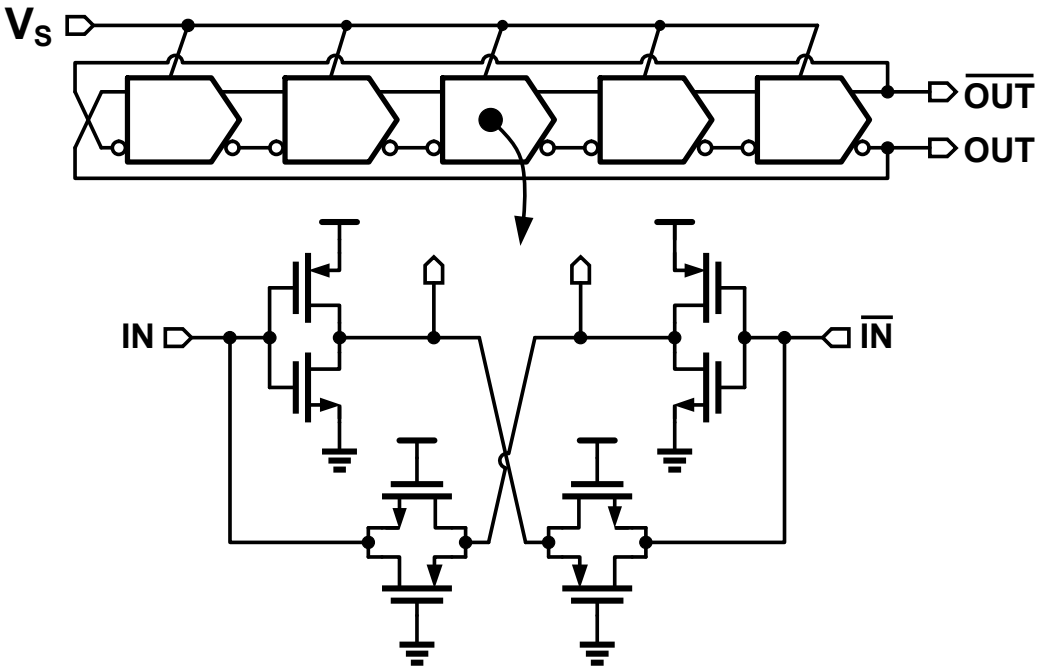


Figure 5.2: Schematic of current controlled ring oscillator.

shown in the figure) is used to convert CCRO output to rail-to-rail CMOS levels. A small inverter-based latch is added at the outputs of the buffer to minimize duty cycle error and achieve close to 50% duty cycle [7]. The pseudo-differential time-based integrator uses two such oscillators. Output oscillator, $CCRO_M$, uses the same topology but with transistor dimensions adjusted to achieve the target output frequency range of 0.4 GHz to 2.6 GHz under all process corners.

The tuning of oscillator $CCRO_M$ by the proportional and integral control paths is implemented as shown in Fig. 5.3. Fixed bias current $I_B$ tunes the CCRO frequency coarsely and brings it close to the target frequency. Proportional ($I_{D2I,PROP}$) and integral ($I_{D2I,PD}$) currents are summed at the virtual supply node, $V_S$, of the CCRO. Proportional control current, $I_{D2I,PROP}$, takes 3 values, $2I_P$, $I_P$, and 0, corresponding to the 3 PFD states, UP, Reset, and DN, respectively. This mapping is performed by the 2 switches that are controlled by $\overline{UP}$ and DN [5]. Integral control is similarly implemented by mapping the two states of the PD to two current values, $I_{PD}$ and 0, by using one switch. Because the CCRO integrator is implemented in a

pseudo-differential manner, two switches controlled by the two PD outputs are necessary to generate the integral control current $I_{D2I,PD}$ as depicted in Fig. 5.3.

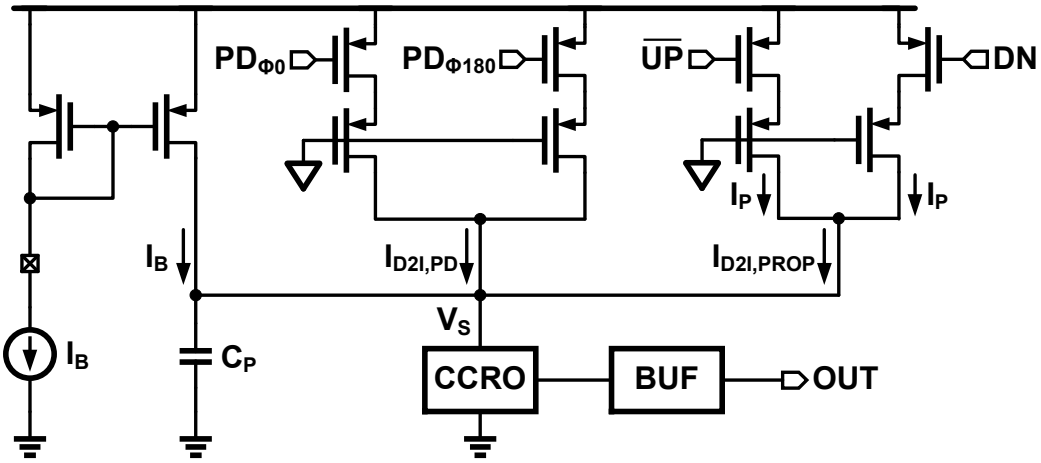


Figure 5.3: Schematic of duty-cycle to current converter.

## 5.2 Phase Detector

Phase detector used in the CCRO integrator is implemented using the two-state architecture shown in Fig. 5.4 (a). The linear range and gain of the PD are equal to $2\pi$ radians and $1/2\pi$ Volt/radian, respectively. Compared to a conventional 2-state PD [15], $\overline{Q}$ output of FF2 is used instead of its Q output. This shifts the PD transfer characteristic by $\pi$ radians resulting in zero average output when the input phase difference is equal to $\pi$ radians as depicted in Fig. 5.4 (b). Consequently, if the two oscillators in the time-

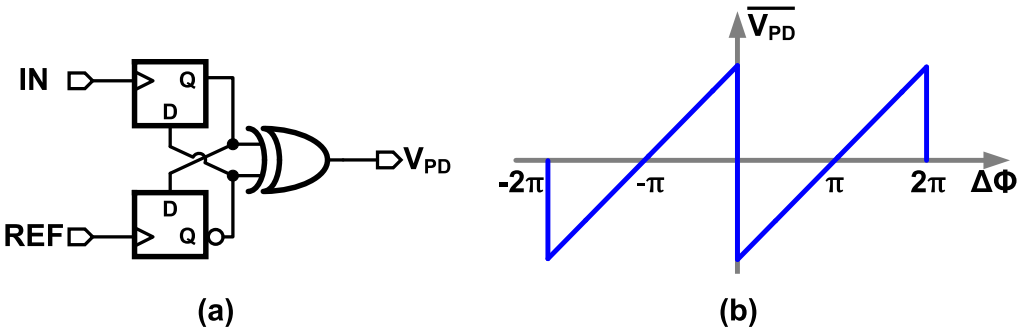


Figure 5.4: (a) Two-state phase detector and (b) transfer characteristic.

based integrators are matched, the PLL locks with a phase difference of $\pi$ radians at the PD input, which results in a PD output duty cycle of 50%. This maximizes the tuning range of the integral control path. The XOR gate is implemented using a fully symmetric architecture shown in Fig. 5.5. The symmetric architecture helps to improve the matching between rise and fall time of the XOR output, improving the overall linearity of the two-state PD with respect to the 50% center point of the output duty cycle.

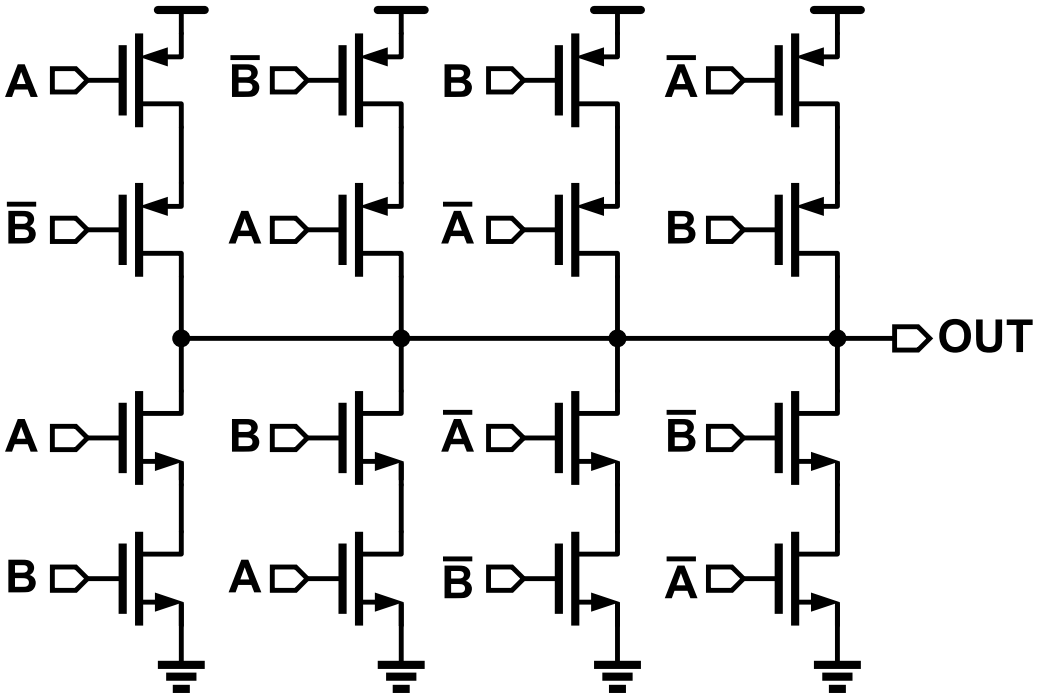


Figure 5.5: Schematics of a fully symmetric XOR gate.

# CHAPTER 6

# MEASUREMENT RESULTS

In this chapter, the measurement results of the prototype PLL are presented. The prototype PLL is implemented in a 65 nm CMOS LP process, and the die photograph is shown in Fig. 6.1. The PLL occupies an active area of 0.0021 $mm^2$ (52 $\mu$m $\times$ 40 $\mu$m). Thanks to its highly digital implementation,

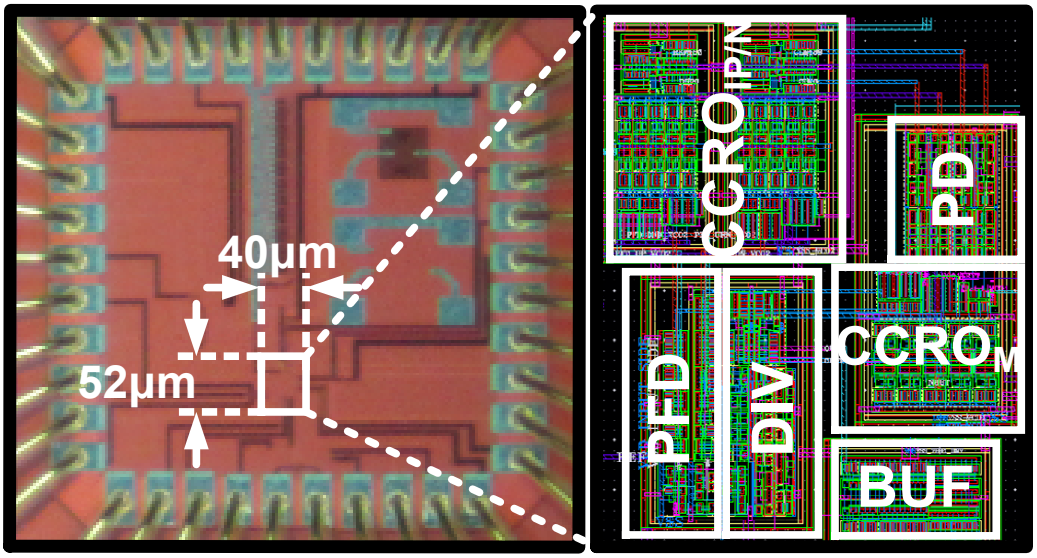


Figure 6.1: Die micrograph.

the prototype PLL operates across a supply voltage range of 0.6 to 1.2 V, and achieves an operating range of 0.4 to 2.6 GHz while consuming a total power of 0.16 to 2.38 mW. The measured output phase noise plot is shown in Fig. 6.2. The phase noise at 1 MHz offset is -103 dBc/Hz and the root mean square (r.m.s.) jitter obtained by integrating the phase noise from 10 kHz to 300 MHz is 3.73 ps. The peaking observed in the plot is caused by phase margin degradation due to more than expected integral path gain resulting from underestimation of $K_{CCRO_I}$. The spectrum of 2.2 GHz PLL output generated from a 275 MHz reference clock is shown in Fig. 6.3. The measured reference spur magnitude is -40.5 dBc. Fig. 6.4 plots the integral path phase

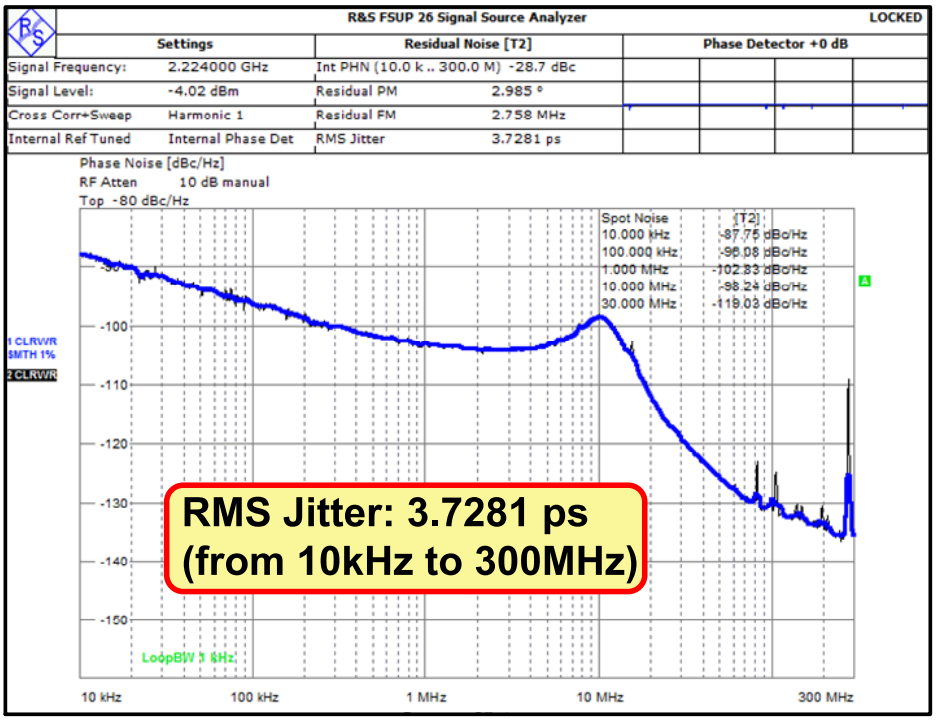


Figure 6.2: Phase noise plot at 2.2 GHz output frequency.

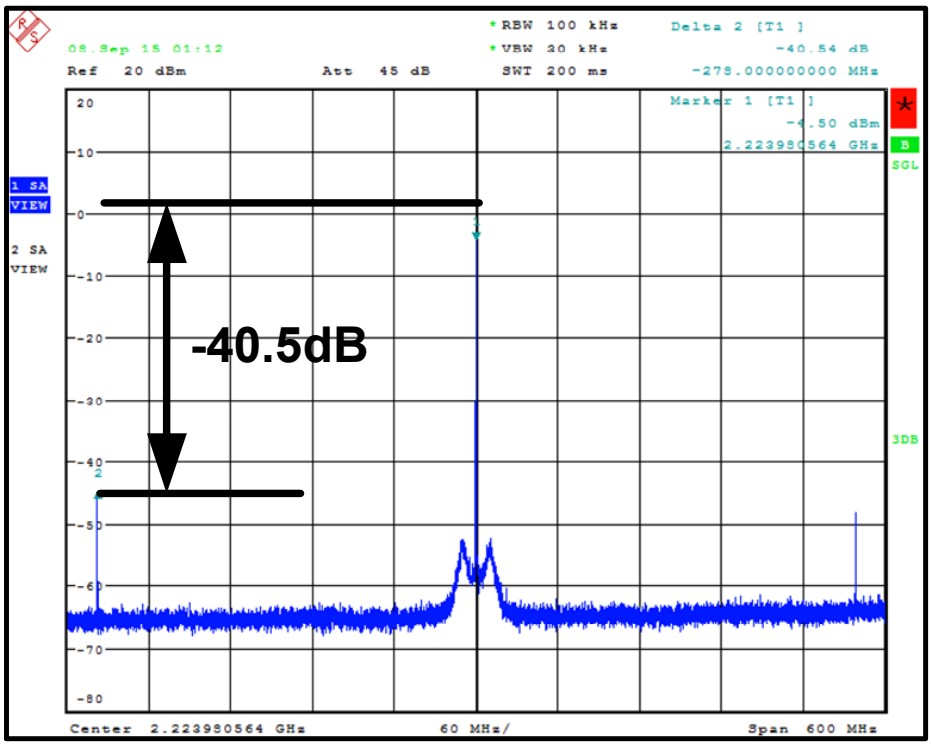


Figure 6.3: Measured reference spur at 2.2 GHz output spectrum.

detector output duty cycle as a function of $CCRO_M$ frequency deviation from the target PLL output frequency. The output duty cycle changes from 25% to 75% as the deviation is varied by ±40 MHz. Therefore, the tracking range of the integral path is about ±40 MHz, which can be further extended by increasing $D2I_{PD}$ converter current at the expense of increased high frequency spur at the PWM frequency and phase noise contribution from $CCRO_I$. Note that the reference spur stays unaltered if the ratio of proportional path to integral path gain is maintained sufficiently high (see Chapter 3). So in a practical realization, an alternative to increasing the tracking range is to add a double integral path as outlined in [5]. The integrated jitter and

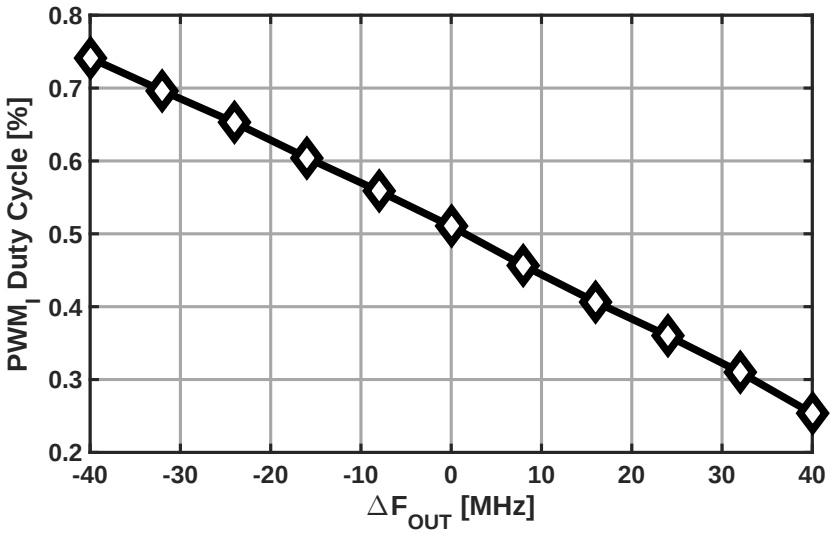


Figure 6.4: Phase detector output duty cycle versus oscillator free running frequency error.

reference spur of the PLL output are measured across the tracking range and the results are shown in Figs. 6.5 and 6.6, respectively. No significant variation of integrated jitter is observed and the reference spur is below -40 dBc across the whole range. At a frequency offset of 24 MHz, the integral path oscillator outputs shown in Fig. 6.7 demonstrate proper operation of the proposed time-based integral control. The measured long-term r.m.s. and peak-to-peak jitter at 2.2 GHz output frequency are equal to 4.9 ps and 46 ps, respectively (see Fig. 6.8). Note that jitter performance degrades when using a lower reference frequency because of reduced loop bandwidth. Under this condition, jitter can be reduced only by burning more power in the oscillators. The performance summary of the prototype PLL is shown in

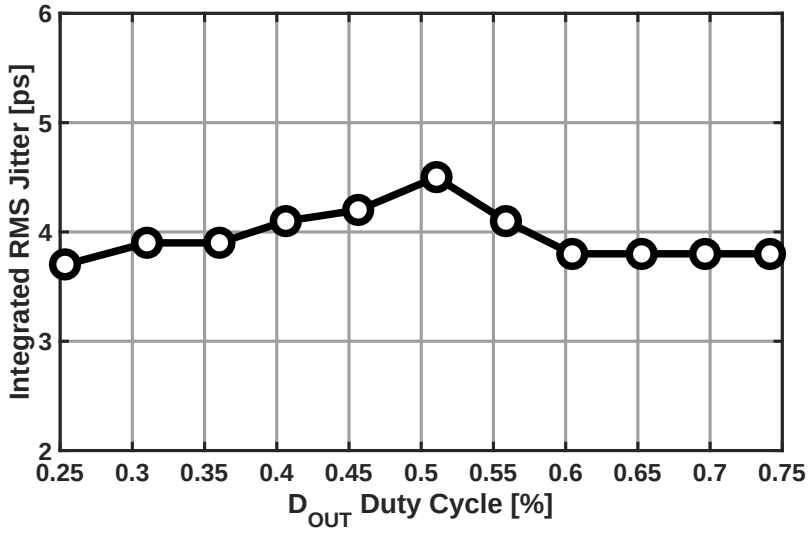


Figure 6.5: Integrated RMS jitter versus phase detector output duty cycle.

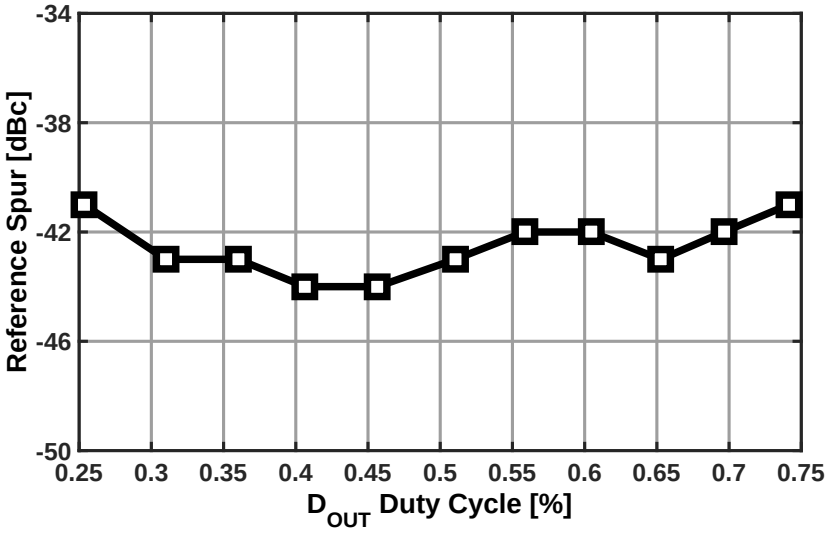


Figure 6.6: Reference spur versus phase detector output duty cycle.


Figure 6.7: Measured $\text{CCRO}_{\text{IP/N}}$ time domain waveforms at frequency offset of 24 MHz.

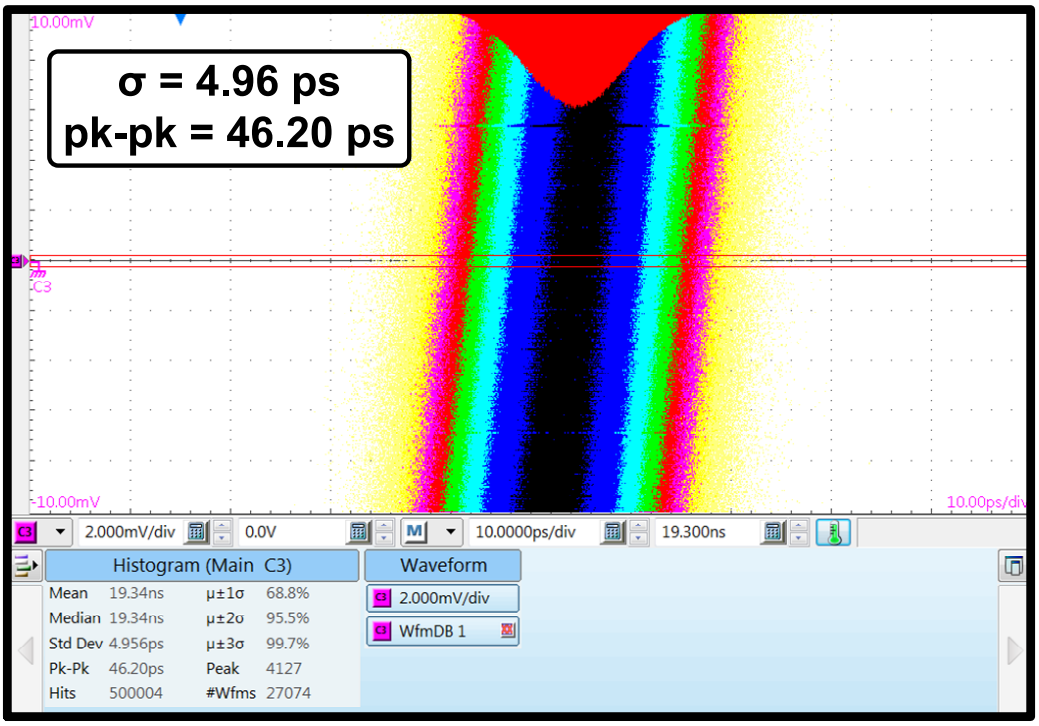


Figure 6.8: Jitter histogram at 2.2 GHz output frequency.

Table 6.1. A comparison with the state-of-the-art design is shown in Table 6.2 featuring PLL designs using FinFET technology ($< 28\,\text{nm}$). With integral path implemented using time-based integrator, the proposed PLL achieves the smallest area among all the reported PLLs. Use of highly digital circuits such as inverters to implement the integral path allows aggressive supply voltage scaling. While the proposed architecture achieves a large reduction in area, excess flicker noise in deeply scaled technologies may warrant increasing the oscillator size, thus reducing the area benefit. Such a trade-off exists in conventional digital PLLs as well because of the increased size of the digital-to-analog converter used to control the oscillator.

Table 6.1: Performance summary of proposed time-based phase-locked loop.

| | This Work | | | |
|---|---|---|---|---|
| Technology | 65 nm | | | |
| Area [mm$^2$] | 0.0021 | | | |
| Normalized Area[1] | 1 | | | |
| Architecture | Time-based PLL | | | |
| Supply [V] | 1.2 | 1.0 | 0.8 | 0.6 |
| Output Freq. [GHz] | 2.6 | 2.2 | 1.0 | 0.4 |
| Ref. Freq. [MHz] | 325 | 275 | 130 | 50 |
| RMS Jitter [ps] | 3.71 | 3.73 | 14.4 | 33.5 |
| Power [mW] | 2.38 | 1.82 | 0.64 | 0.16 |
| Power Eff. [mW/GHz] | 0.92 | 0.83 | 0.64 | 0.4 |
| FoM [dB][2] | -224.8 | -226.0 | -218.8 | -217.5 |

[1] Normalized Area $= \left[\dfrac{\text{Area}}{0.0021\,\text{mm}^2} \cdot \left(\dfrac{\lambda}{65\,\text{nm}}\right)^2\right]$

[2] FoM $= 10\log\left[\left(\frac{\sigma_{\text{rms}}}{1\text{sec}}\right)^2 \cdot \left(\frac{\text{Power}}{1\text{mW}}\right)\right]$

Table 6.2: Performance comparison of proposed time-based phase-locked loops with state-of-the-art designs.

| | This Work | ISSCC'12 [16] | ISSCC'14 [17] | ISSCC'15 [18] |
|---|---|---|---|---|
| Technology | 65 nm | 22 nm | 22 nm | 14 nm |
| Area [mm$^2$] | 0.0021 | 0.017 | 0.012 | 0.009 |
| Normalized Area[1] | 1 | 70.67 | 60.36 | 92.35 |
| Architecture | TB-PLL | BB-DPLL | BB-DPLL | BB-DPLL |
| Supply [V] | 1.0 | 0.5−1.0 | 0.9 | 0.8 |
| Output Freq. [GHz] | 2.2 | 0.3−3.2 | 0.025−1.6 | 0.032−2.0 |
| Ref. Freq. [MHz] | 275 | 40 | 26 | 50 |
| RMS Jitter [ps] | 3.73 | 3.1 | 28 | 18.8 |
| Power [mW] | 1.82 | 3.4 | 3.1 | 2.06 |
| Power Eff. [mW/GHz] | 0.83 | 1.06 | 1.94 | 1.03 |
| FoM [dB][2] | -226.0 | -224.8 | -206.1 | -211.4 |

[1] Normalized Area $= \left[\frac{\text{Area}}{0.0021\,\text{mm}^2} \cdot \left(\frac{\lambda}{65\,\text{nm}}\right)^2\right]$

[2] FoM $= 10\log\left[\left(\frac{\sigma_{\text{rms}}}{1\text{sec}}\right)^2 \cdot \left(\frac{\text{Power}}{1\text{mW}}\right)\right]$

# CHAPTER 7

# CONCLUSION

A time-based integrator based PLL architecture that achieves low active area and excellent power efficiency is presented. The time-based integral path greatly alleviates the area penalty seen in conventional PLL architectures, and provides one alternative implementation of a type-II PLL featuring good scalability with process and no quantization error in the system. Pseudo-differential architecture of the time-based integrator has been proposed to overcome the drawbacks of reference spur degradation when directly applying PWM control to the oscillator. The proposed architecture helps decouple the oscillation frequency choice of the integral path oscillator from the PLL reference, and better leverage the loop response to achieve spur suppression. The prototype time-based PLL operates over a wide range of supply (0.6 to 1.2 V) with output frequencies ranging from 0.4 to 2.6 GHz, and occupies an active area of only 0.0021 $mm^2$. At 2.2 GHz, the time-based PLL consumes only 1.82 mW from a 1 V supply and achieves 3.73 $ps_{rms}$ integrated jitter. The performance of the proposed time-based PLL is summarized in Table 6.1, and is compared with state-of-the-art PLLs in Table 6.2.

# REFERENCES


[1] F. M. Gardner, *Phaselock Techniques*. John Wiley & Sons, 2005.

[2] N. A. Kurd, S. Bhamidipati, C. Mozak, J. L. Miller, P. Mosalikanti, T. M. Wilson, A. M. El-Husseini, M. Neidengard, R. E. Aly, M. Nemani, M. Chowdhury, and R. Kumar, "A family of 32 nm IA processors," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 119–130, Jan. 2011.

[3] M. G. Floyd, "Charge-pump phase-lock loops," *IEEE Transaction on Communications*, vol. 28, no. 11, 1980.

[4] P. K. Hanumolu, G. Y. Wei, U. K. Moon, and K. Mayaram, "Digitally-enhanced phase-locking circuits," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2007, pp. 361–368.

[5] W. Yin, R. Inti, A. Elshazly, B. Young, and P. K. Hanumolu, "A 0.7-to-3.5 GHz 0.6-to-2.8 mW highly digital phase-locked loop with bandwidth tracking," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1870–1880, Aug. 2011.

[6] Y. C. Huang, C. F. Liang, H. S. Huang, and P. Y. Wang, "A 2.4GHz AD-PLL with digital-regulated supply-noise-insensitive and temperature-self-compensated ring DCO," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 270–271.

[7] B. Drost, M. Talegaonkar, and P. K. Hanumolu, "Analog filter design using ring oscillator integrators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3120–3129, Dec. 2012.

[8] J. Zhu, R. K. Nandwana, G. Shu, A. Elkholy, S. J. Kim, and P. K. Hanumolu, "A 0.0021mm2 1.82mW 2.2GHz PLL using time-based integral control in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Jan. 2016, pp. 338–340.

[9] M. Park and M. H. Perrott, "A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time ADC with VCO-based integrator and quantizer implemented in 0.13 $\mu$m CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3344–3358, Dec. 2009.

[10] H. Roder, "Amplitude, phase, and frequency modulation," *Proceedings of the Institute of Radio Engineers*, vol. 19, no. 12, pp. 2145–2176, Dec. 1931.

[11] W. G. Hurley, E. Gath, and J. G. Breslin, "Optimizing the AC resistance of multilayer transformer windings with arbitrary current waveforms," in *30th Annual IEEE Power Electronics Specialists Conference, 1999. PESC 99*, vol. 1, Aug. 1999, pp. 580–585 vol.1.

[12] U. Wismar, D. Wisland, and P. Andreani, "A 0.2V, 7.5 $\mu$W, 20 kHz $\Delta\Sigma$ modulator with 69 dB SNR in 90 nm CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2007, pp. 206–209.

[13] M. Park and M. H. Perrott, "A multiphase PWM RF modulator using a VCO-based opamp in 45nm CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, 2010, pp. 39–42.

[14] J. F. Parker, D. Weinlader, and J. L. Sonntag, "A 15mW 3.125GHz PLL for serial backplane transceivers in 0.13 $\mu$m CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 412–607 Vol. 1.

[15] D. H. Wolaver, *Phase-Locked Loop Circuit Design.* Eaglewood Cliffs, NJ: Prentice-Hall, 1991.

[16] N. August, H. J. Lee, M. Vandepas, and R. Parker, "A TDC-less ADPLL with 200-to-3200MHz range and 3mW power dissipation for mobile SoC clocking in 22nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 246–248.

[17] J. Liu, T. K. Jang, Y. Lee, J. Shin, S. Lee, T. Kim, J. Park, and H. Park, "A 0.012mm$^2$ 3.1mW bang-bang digital fractional-N PLL with a power-supply-noise cancellation technique and a walking-one-phase-selection fractional frequency divider," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 268–269.

[18] M. Song, T. Kim, J. Kim, W. Kim, S. J. Kim, and H. Park, "A 0.009mm$^2$ 2.06mW 32-to-2000MHz 2nd-order $\Delta\Sigma$ analogous bang-bang digital PLL with feed-forward delay-locked and phase-locked operations in 14nm FinFET technology," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.