DESIGN AND IMPLEMENTATION OF A 1.3 KW, SINGLE-PHASE, SEVEN-LEVEL, GAN AC-DC CONVERTER

BY

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THESIS

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ABSTRACT

In todays world, electrical energy meets an increasing amount of the worlds power needs as more countries are transitioning from traditional energy sources such as fossil fuels to renewable energy sources. The importance of power electronics has substantially increased due to their key roles in harnessing and delivering energy efficiently from renewable energy sources. As many modern applications of power electronics such as renewable energy harnessing, electric vehicle, and data center energy management require high-performance power electronics, innovative approaches to more robust, smaller, and efficient power converters are in great demand.

This work presents detailed design process and hardware implementation of 1.3 kW, 90-264 V_{rms} (60 Hz) to 400 V_{DC} converter. As a part of the trend in power electronics, the proposed converter features an innovative topology optimized for size miniaturization and high efficiency: a seven-level flying capacitor multilevel design with Gallium Nitride MOSFETs operating at 120 kHz. The converter is currently in competition for the IEEE International Future Energy Challenge 2016. It has achieved over 96% conversion efficiency at about 300 W output power. The development of fully functional power factor correction and digital control is in steady progress. With the sophisticated digital control and heatsink for better heat dissipation, this converter is projected to have a power density greater than 2 W/cm^3(32.8 W/in^3) with over 98% efficiency.

ACKNOWLEDGMENTS

I would like to thank Professor Robert Pilawa-Podgurski for his support and guidance throughout the project. He opened the door for me to the fascinating field of power electronics. His passion and knowledge about power electronics have been a true inspiration to me. It has been a enjoyable and enriching experience working with him.

This work would not have been possible without the hard work and contributions from my teammates, Shibin Qin, Yutian Lei, Carl Haken, Erik Saathoff, Derek Chou, Ethan Bian, and Steven Sedig. Shibin and Yutian, PhD candidates who originally designed a seven-level GaN inverter, have provided me with valuable feedback from the layout design to hardware prototype. Carl has played a significant role in designing a controller board and energy buffer. Erik not only provided the team with well-functioning GaN switching cells but also manufactured a heatsink for the GaN devices. Derek has helped me understand the mechanical aspects of the project. Ethan and Steven helped me better understand the embedded system and implement the digital control.

Finally, I would like to thank my parents, Chang-Hee Moon and Yun-Hee Kim for their love and support. They have taught me how to be a kind and humble person by example and constantly encouraged me to become the best version of myself. My older brother and best friend, Inyong Moon, has been the one whom I have always admired and counted on for an honest and insightful piece of advice.

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INTRODUCTION

One of the primary applications of the AC-DC converter can be found in a DC power delivery architecture for a data center. A data center provides storage spaces for the data-processing equipment. With the rapid increase in both number and size of data centers, the energy efficiency of data centers has become an important challenge for power engineers [1]. A system-level solution making use of series connection of servers in a rack and differential power processing technique has been proposed to reduce the total amount of total processed power and consequently conversion stages in data centers [2], [3]. A efficient and compact power converter coupled with the system-level method can achieve the power delivery system which is highly efficient as well as space-efficient.

In order to further increase a conversion efficiency, a DC conversion stage can be implemented with a switched-capacitor (SC) DC-DC converter adopting a soft-charging operation. Through soft-charging, the switching loss of a SC converter can be minimized or even eliminated by allowing the output voltage to vary [4]. Recently, much efforts have been made to analyze performance of a SC DC-DC converter and its compatibility with a soft-charging operation in order to achieve not only high conversion efficiency but also high power density thanks to a SC converter's ease of integration [4–6].

The aforementioned application and technique reinforce the roles of lightweight yet efficient and robust power electronics and the reason that they are in a great demand. Aligning with this trend in power electronics, this work presents a seven-level flying capacitor multilevel design which allows for a great overall size reduction and therefore higher power density. This converter is designed to convert 90-264 V_{rms} (60 Hz) to 400 V_{DC} with the maximum output power of 1.3 kW. Its conversion efficiency is expected to be over 96% at full power.

In order to build a small yet highly efficient and robust power converter,

one should possess a breath of knowledge in electrical engineering including electromagnetics, digital and analog IC design, feedback control, embedded system, and thermal and EMI management. This work also presents how the aforementioned fields have been incorporated into designing and building the power converter along with some challenges encountered during the process.

The detailed design process and hardware implementation of the converter are covered throughout the thesis. Chapter 1 clearly states the design requirements as well as design approaches to meet and surpass the specified requirement. Chapter 2 and 3 cover the theory and working of the chosen topology. The design approaches taken toward a heat management and electromagnetic interference are covered in Chapter 4 and 5. Finally, Chapter 7 presents preliminary test results, and Chapter 8 presents the future work to further optimize the performance of the proposed converter.

CHAPTER 1

DESIGN OVERVIEW

The IEEE International Future Energy Challenge 2016 requires design and implementation of a single-phase AC-DC converter system with challenging specifications: over 96% efficiency, power density greater than $1W/cm^3$, and power factor higher than 0.95. To meet and surpass the design requirements, an innovative approach, a seven-level flying-capacitor multi-level (FCML) converter with GaN switches, which will be explained in detail throughout the thesis has been adopted. This seven-level FCML GaN topology was originally adopted by the team put together by Professor Robert Pilawa for the power inverter design competing for the Google Little Box Challenge [7].

The proposed AC-DC converter consists of three power handling stages and a digital control system as shown in Fig. 1.1. The power handling stages consist of a full-bridge active rectifier, followed by a seven-level FCML step-up converter with PFC functionality, and then an energy buffer which consists of electrolytic capacitors to handle the twice line-frequency power ripple due to the instantaneous power mismatch between AC input and DC output. The use of 7-level FCML converter in the prototype allows for high efficiency as well as significant volume miniaturization and therefore higher power density. The proposed prototype uses GaN devices that have excellent switching characteristics as well as low on-resistance. A TI C2000 micro-controller is adopted to implement the digital control, including a power factor correction

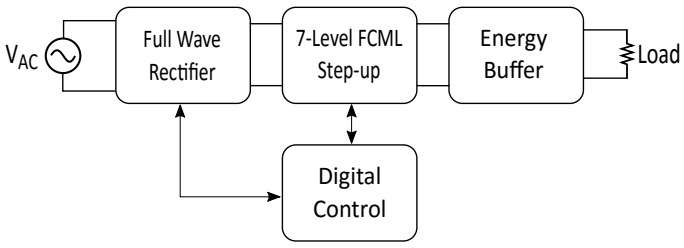

Figure 1.1: Block diagram of the proposed AC-DC converter

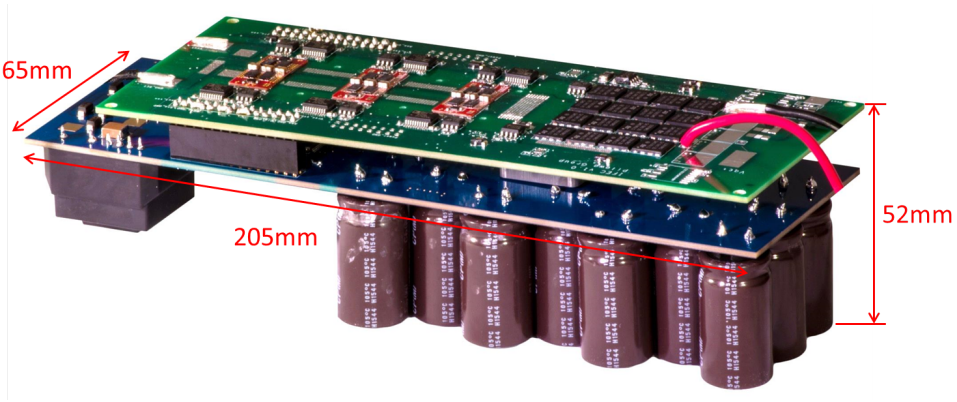

Figure 1.2: 7-level FCML converter and controller prototype

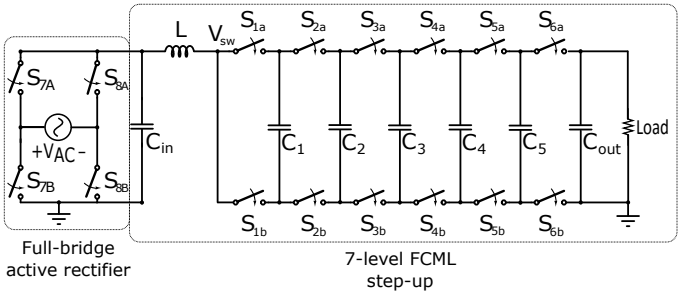

Figure 1.3: Schematic diagram of the proposed AC-DC converter

in the seven-level FCML step-up converter and the synchronization of the active full-bridge rectifier. Finally, a custom heatsink ensures proper cooling of the components, especially GaN devices on the converter board.

The preliminary test of the first version of the hardware prototype has been completed. The hardware prototype including the converter and controller board is shown in Fig. 1.2. The operation of a seven-level FCML converter has been successfully demonstrated. The circuit has been tested up to an output voltage of 245 V_{rms} and output power of 295 W, with higher voltage and power level testing in progress. The current prototype has a rectangular dimensions of 20.57 cm x 6.52 cm x 5.25 cm = 704.11 cm^3 as shown in Fig. 1.2, which results in the expected power density of 1.84 W/cm^3. With the custom heatsink, the estimated power density is calculated to be 1.21 W/cm^3. Once the design concept with the current prototype has been proven, a much more compact design with both smaller circuit volume and smaller heatsink volume will be pursued in the next iteration. The rest of the thesis covers the technical detail in designing and implementing the power converter along with the preliminary test results.

CHAPTER 2

CIRCUIT OPERATION

As illustrated in Fig. 1.1, the power handling stage consists of a full-bridge rectifier, a FCML PFC stage and an energy buffer. The details of each stage are presented in the following sections.

2.1 Full-bridge active rectifier

The schematic drawing of the full-bridge active rectifier is presented in Fig. 1.3. S_{7A} and S_{8B} are turned on when V_{AC} crosses from negative to positive, while S_{7B} and S_{8A} are turned on when V_{AC} crosses from positive to negative. This operation ensures that the rectified sinusoidal signal is seen at the output of the full-bridge rectifier. The digital control system implemented through TI C2000 micro-controller senses the zero-crossings of the input AC signal and controls the switches as described above with the corresponding PWM signals.

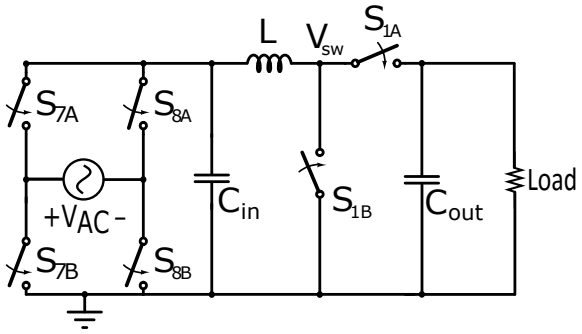

Figure 2.1: Schematic diagram of the conventional AC-DC converter

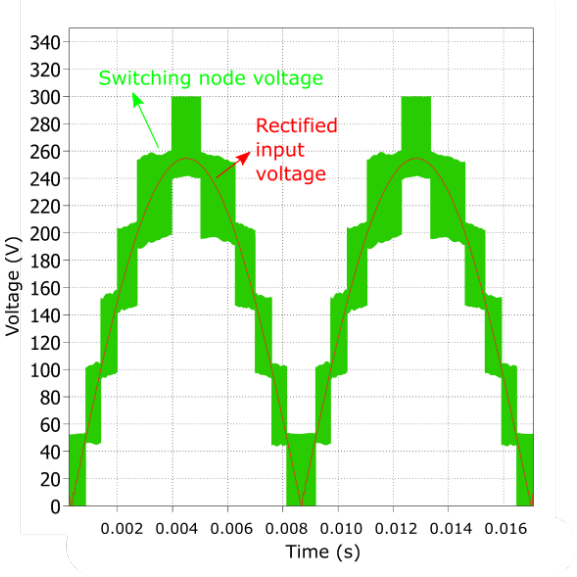

Figure 2.2: Simulated switching node voltage and rectified input voltage of the proposed FCML converter

2.2 Seven-level FCML boost with PFC (power factor correction)

A seven-level FCML boost converter, as shown in Fig. 1.3 is used to boost the rectified AC voltage to the desired output voltage. A switching node voltage, V_{sw}, of the conventional AC-DC converter shown in Fig. 2.1 has a step voltage of either V_{out} or ground, which imposes voltage stress of V_{out} on each switch and results in an effective filtering frequency equivalent to a switching frequency for each GaN, f_{sw}. A simulated switching node voltage, V_{sw}, and rectified input voltage, V_{rec}, of the proposed 7-level FCML topology is shown in Fig. 2.2. In contrast to the conventional design, this topology not only reduces voltage stress on each switch but also increases the effective filtering frequency seen by an inductor by a factor of $N_{levels} - 1$, allowing for the use of a much smaller filtering inductor [8], [9].

Flying capacitors are placed in between the series switches, as seen in Fig. 1.3. The capacitors are called flying because their terminals are not permanently connected to any voltage rail. The flying capacitors hold various fractions of the output voltage. For the capacitors in Fig. 1.3, C_1 holds 1/6 of the DC output voltage, C_2 holds 2/6, C_3 holds 3/6, and so on as shown in Fig. 2.3. By using these capacitors, the seven-level FCML is able to apply

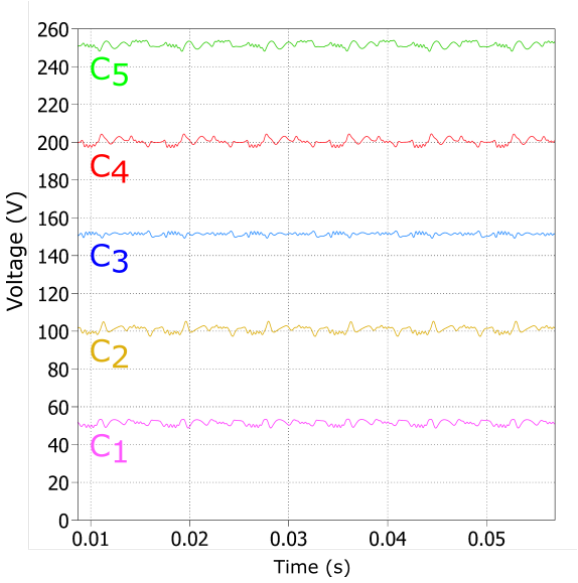

Figure 2.3: Simulated flying capacitor voltages

seven total voltage levels to the switch node V_{sw}. As explained earlier, each individual switch must only block a fraction of the input voltage, allowing for the use of lower voltage rated GaN device along with smaller gate drivers. Equation 2.1 gives the voltage rating of each switch.

$$V_{blocked} = \frac{V_{DC}}{N_{levels} - 1} \tag{2.1}$$

The flying capacitor voltages are inherently self-balancing. In a single switching period, a given flying capacitor is charged and discharged for the same amount of time, so if the voltage is higher than intended, more current will exit during the discharge and less current will enter during the charge, balancing the capacitor.

The switch control signals for a multilevel converter use identical frequencies and duty cycles, but with phase shifts such that they are evenly distributed across a single switching period. The phase shift between any two given signals is given in Equation 2.2.

$$Phase\ Shift\ [degrees] = \frac{360}{N_{levels} - 1} \tag{2.2}$$

Fig. 2.4 demonstrates the phase shift between signals is 60 degrees.

Fig. 2.4 shows an example plot of the switching node voltage, V_{sw} for a seven-level FCML converter. Note that the switching frequency is 120

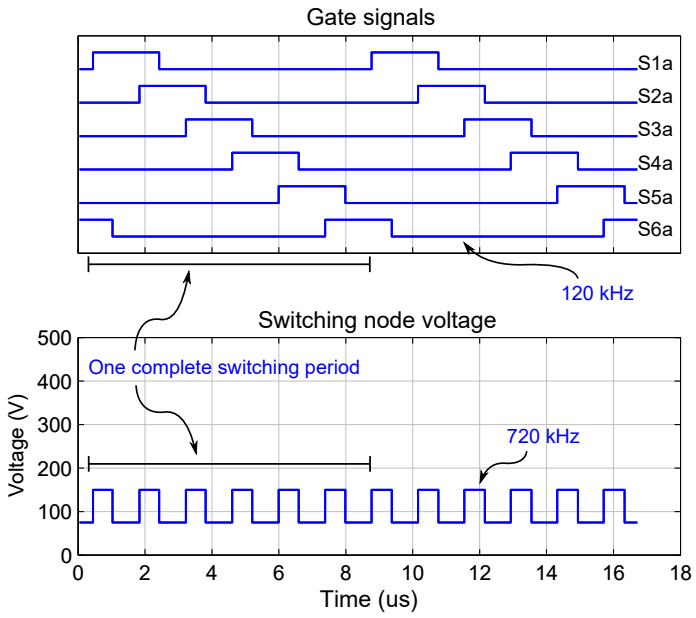

Figure 2.4: Gate signals for a seven-level FCML converter [7]

kHz and the duty cycle is 25%. This example shows another benefit of the FCML converter topology: the effective switching frequency as seen by the filtering elements, is multiplied by $(N_{levels}-1)$. Since the current ripple in the filter inductor is directly proportional to the pulse voltage levels across the inductor and inversely proportional to the pulse frequency, given a certain inductor current ripple, an FCML converter can have an output inductor and capacitor that are $(N_{levels}-1)^2$ times smaller than a two-level converter [6].

The increased switching frequency and reduced voltage swing allow for a significant reduction in the required inductor size, because the volt-second product is drastically reduced. This makes the FCML converter topology desirable for high power density applications. The extra volume occupied by the switches and flying capacitors tends to be smaller compared to the volume spared by reducing the size of the filtering inductor, because the energy density of ceramic capacitors is approximately 100 times the energy density of inductors [10].

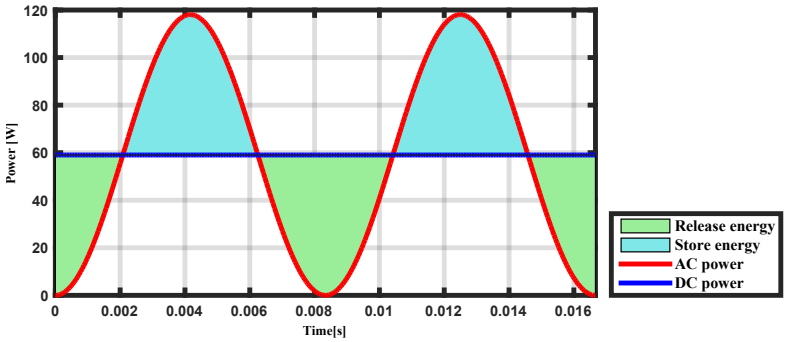

Figure 2.5: Instantaneous power plot [10]

2.3 Energy buffer

Line-interfaced power converters inherently have power ripple on the DC side at twice line frequency. In order to compensate this instantaneous power mismatch, an energy buffer is needed to store and release the energy difference in each cycle as shown in Fig. 2.5 and therefore minimize the voltage ripple across the DC bus. The proposed prototype is equipped with a standard twice line frequency buffering electrolytic capacitor bank. Note that the active buffer circuit which resolves instantaneous power mismatch between the AC input and DC output and takes up much less volume compared to a bank of electrolytic capacitors is planned to be implemented for the next iteration to achieve even higher power density. Details in energy buffer capacitors calculations will be covered in the Chapter 4.

CHAPTER 3

CIRCUIT PROTOTYPE

3.1 Seven-level FCML converter

The converter prototype consists of three parts: a start-up, full-bridge rectifier, and seven-level FCML boost with PFC as shown in Fig. 3.1. A start-up circuitry is necessary since the output capacitor and flying capacitors need to be initially charged to minimize inrush current and ensure stable and safe operation of the converter. For the full-bridge rectifier, four Power MOSFETs (STL57N65M5) are connected in parallel at each leg to handle maximum input current of 15 A and maintain high conversion efficiency across the rectifier.

Table 3.1: Key components in the converter prototype

Component	Value/Part number	Manufacturer
Converter FETs	EPC2033	EPC
Converter Driver	LM5113	Texas Instruments
Rectifier FETs	STL57N65M5	STMicroelectronics
Rectifier Driver	FAN73932MX	Fairchild
Converter Capacitors	C5750X6S2W225K250KA	TDK
Converter Inductor	IHLP8787MZER220M51	Vishay
Microcontroller	TMX320F28377DPTPT	Texas Instruments
Control 450V - 12V	EPM1210SJ	Tamura
Signal Isolators	SI8423BB-D-IS	Silicon Labs
Power Isolators	ADUM5210	Analog Devices
Current Sensing Amplifier	LT1999	Linear Technology

For the seven-level FCML boost stage, the semiconductors that our team employed are EPC GaN devices (EPC2033). This device is rated for 150 V (V_{DS}) and 31 A (I_D). The voltage stress on each GaN device is $\frac{V_{out-max}}{N_{levels}-1} =$

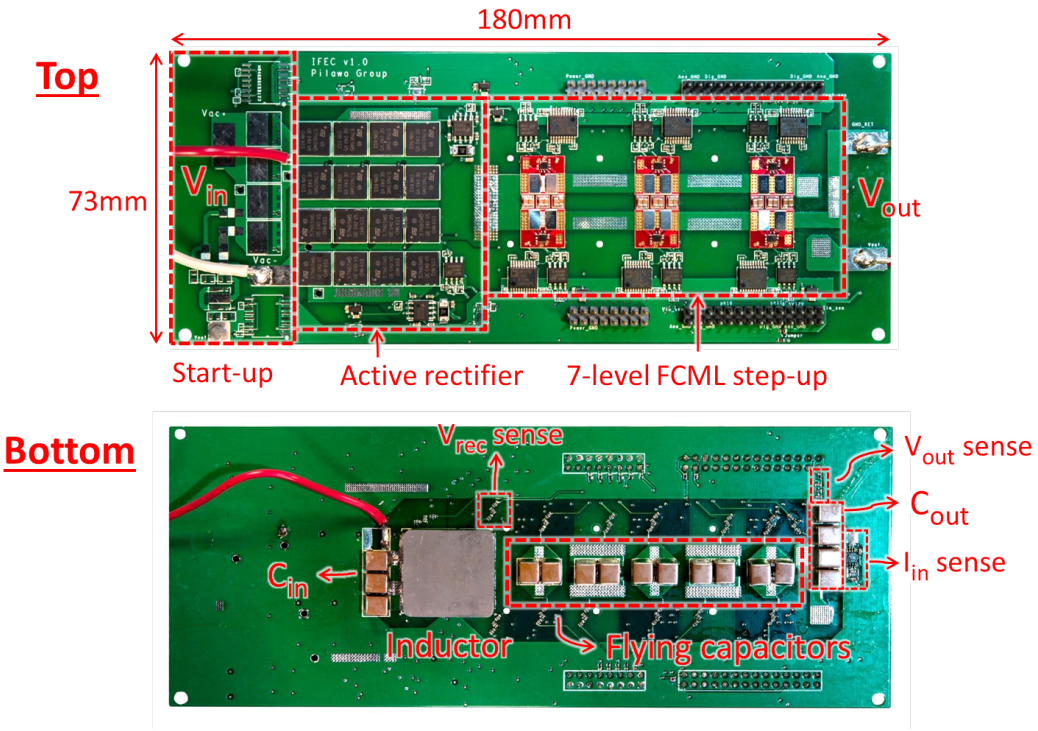

Figure 3.1: The proposed AC-DC converter PCB

$\frac{400}{6} \approx 66.67$ V, which is much smaller than the rated voltage of EPC2033. TI LM5113, a half-bridge gate driver, is used to drive both the high-side and low-side GaN devices. Furthermore, in order to minimize parasitic inductance as well as systematically test GaN devices, our research group has developed the custom GaN switching module as shown in Fig. 3.2.

The key components used in this prototype are shown in Table 3.1. 17.5 A, 22 μF Vishay inductor, which can handle the specified maximum input current of 15 A, is used as a filtering inductor. A flying capacitor which consists of six 2.2 μF, 450 V TDK ceramic capacitors is used to maintain capacitor voltage level during each switching cycle. A digital signal isolator (SI8423) is used to relay the PWM signals generated by the micro-controller to corresponding GaN gate driver, which sits at different voltage domain, while an isolated dc-dc power supply IC (ADUM5210) provides the power for corresponding signal isolator. Finally, LT1999 (Current sensing amplifier) along with a shunt resistor is used to scale the input current properly for the microcontroller Analog-to-Digital conversion and maintain good resolution of the signal.

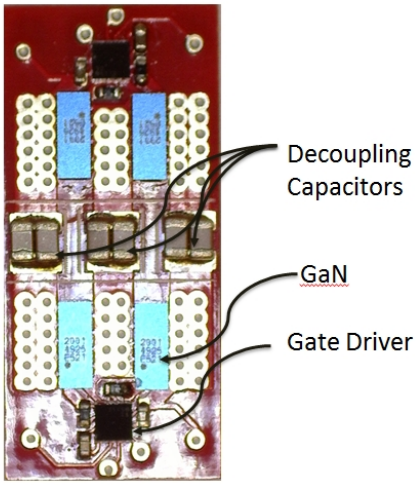

Figure 3.2: Custom GaN switching module

3.2 Switching cells

Two sets of GaN devices, a total of four GaN devices, which are used as the switches in the proposed seven-level FCML converter are soldered onto a daughter board (switching cell) shown in Fig. 3.2. This daughter board is then soldered onto the main converter. As mentioned earlier, this allows for convenient testing of GaN devices which requires a great care to solder properly. The test setup for a switching cell is shown in Fig. 3.5. The soldering and testing procedure of GaN devices will be explained in detail in the next paragraph. Each cell contains two sets of two GaN devices with a half-bridge gate driver operating each set. The boards are 0.4 mm thick and have 2 oz of copper. The bottom of each board has large contacts to be directly soldered to the main PCB. The use of many vias and thin boards allows us to minimize the parasitic inductance of the loop to around 1 nH.

A switching cell is fully assembled through the use of a hot air station and a Finetech SMT placer. 0402 gate resistors, bootstrap capacitors and 0805 decoupling capacitors are first soldered with a hot air station. Next, each switching cell is placed in a milled-out slot of a fiberglass plate mounted on the Finetech machine shown in Fig. 3.4 to allow the board to be heated from both sides. The board is secured in place with polyamide tape and a thermocouple is taped next to the board to provide temperature feedback for the reflow procedure. The pads for the GaN devices and half-bridge drivers are coated in a thin layer of fresh flux and then the devices are placed onto

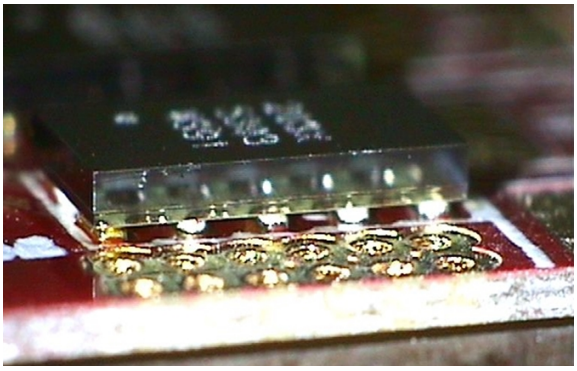

Figure 3.3: Optic view of GaN device seating on the switching cell

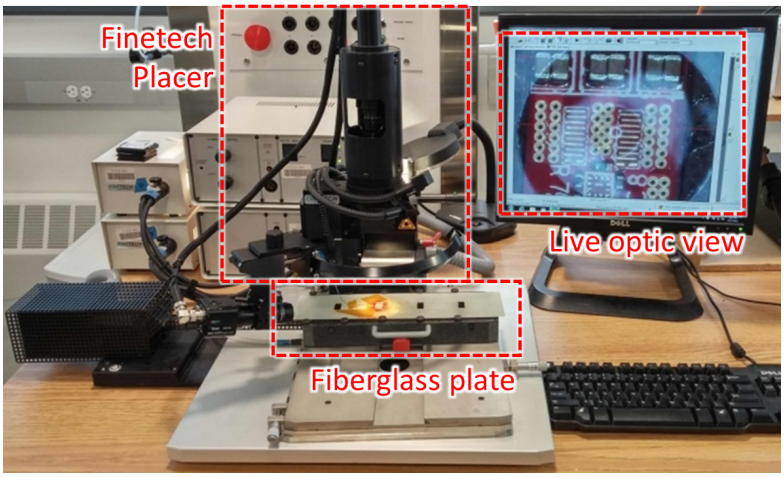

Figure 3.4: Finetech SMT placer

the pads. The Finetech machine provides high-definition live video so that the user can place the BGA package components on the pads with perfect alignment. The system employs a split view system that superimposes a view of the bottom of the component and the pads on the board to allow for such alignment to take place. In addition, there is a side view provided when reflowing components that allows the user to watch as the component properly seat during the reflow procedure as shown in Fig. 3.3.

A fully assembled switching cell is then placed in a bed of nails testing apparatus to confirm correct operation. The testing apparatus can be seen in Fig. 3.5 with a slot to align the switching cell and a retention arm to press the switching cell down with the help of a 3D printed board spacer. The gate driver output signals along with gate-to-source and drain-to-source signals are monitored on an oscilloscope to verify proper operation of GaN devices and gate drives. All cells that pass this step are placed in a 150 °C thermal

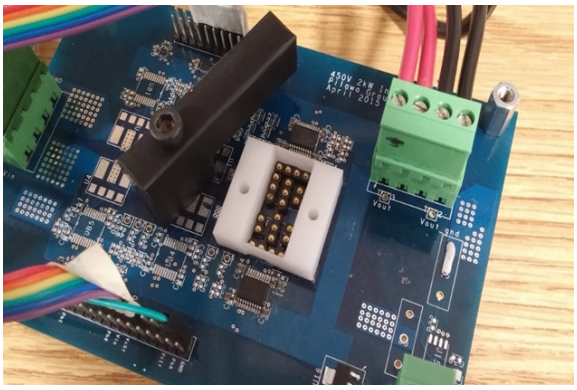

Figure 3.5: GaN switching cell test setup

oven for 35 minutes to cure the flux before finally being soldered onto the main board. The switching cells that do not operate correctly are subject to further signal integrity checks to narrow down a malfunctioning part for replacement. This systematic approach to soldering and troubleshooting GaN submodule has led to consistent yield of well-functioning GaN submodues.

3.3 Energy buffer and Controller board

In addition to the power converter board, a second circuit board to hold the microcontroller, voltage regulators, and buffer capacitors for the converter has been designed as shown in Fig. 3.6. These electrolytic capacitors are used to resolve twice-line frequency due to the instantaneous power mismatch between AC input and DC output.

By competition requirements, the 400 V output is constrained to have no more than 5 V peak-to-peak ripple. Equation 3.1 from [11] shows the energy method for calculating required buffer capacitance. Note that the worst-case average power output of the converter is 1.3 kW, and the worst case frequency is 47 Hz.

$$E_{buffer} = \frac{P_{ave}}{2\pi f_{line}} = \frac{1}{2}CV_{max}^2 - \frac{1}{2}CV_{min}^2 = \frac{1}{2}(V_{max} + V_{min})(V_{max} - V_{min})C \tag{3.1}$$

Using Equation 3.1, it can be found that the required buffering capacitance is 2.2 mF assuming zero ESR. The Nichicon UCP2W121MHD6 capacitor, a 450 $V/120$ μF electrolytic, was chosen due to its superior capacitance density

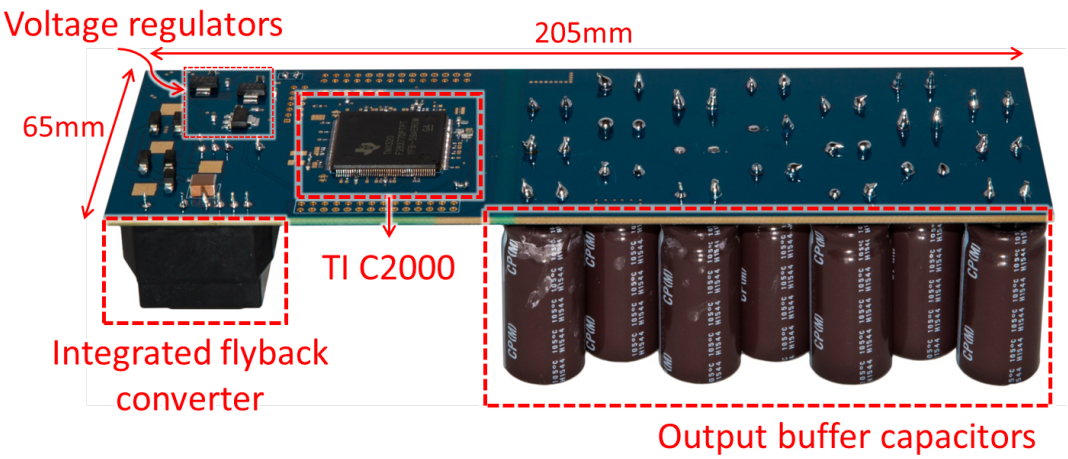

Figure 3.6: The controller PCB

relative to similar options. Just over 18 of these capacitors would be required to provide 2.2 mF of capacitance. The loss tangent of this capacitor is 0.24, and the ESR of each capacitor can be found using Equation 3.2.

$$ESR = (Loss\ Tangent) * X_c \tag{3.2}$$

The capacitive reactance is calculated assuming 47 Hz AC. The resulting ESR is 3.386 Ω per capacitor or 0.188 Ω for eighteen parallel capacitors. The peak current drawn from the capacitors will be equal to the DC current output, which is 3.25 A. When multiplied by ESR, this yields an ESR voltage drop of 0.61 V. The peak-to-peak ripple is increased by twice the ESR voltage drop. In order to compensate for this effect, more buffering capacitance must be used, but increasing the buffering capacitance reduces the ESR. Through a few iterations, it was determined that the optimal number of buffering capacitors would be 23. This value yields a base ripple of 4.0 $V_{peak-to-peak}$, an ESR of 0.147 Ω, an ESR voltage drop of 0.48 V, and a total ripple of 4.96 $V_{peak-to-peak}$.

The theoretical power dissipation in the buffering capacitors was calculated using Equation 3.3. The current through the capacitors is sinusoidal, so the RMS current will be the peak current divided by $\sqrt{2}$. The capacitor power dissipation is therefore approximately 0.77 W, which is well within acceptable limits.

$$P_{loss} = I_{RMS}^2 * R_{ESR} \tag{3.3}$$

The two boards are connected using a pair of 28-pin headers as shown in Fig. 1.2. The microcontroller is a Texas Instruments F28377D, part of the Texas Instruments C2000 series which is intended for control of power electronics and feedback applications. Having the microcontroller on a dedicated PCB allows for reduced noise throughout the system compared to using an external microcontroller development board. The board provides regulated 1.2 V, 3.3 V digital, and 3.3 V analog voltage rails for the microcontroller, as well as 12 V and 6.5 V rails for the power stage gate drivers and isolators. To produce these voltages, the design uses an integrated flyback converter to step the 400 V output voltage down to 12 V, and then several small integrated switching and linear regulators to produce the other voltage rails. The flyback converter draws power from the output to help improve the power factor of the converter. During start-up, when the output voltage is low, the flyback draws power from the input instead. This functionality is achieved by an diode-ORing of the AC input terminals with the output terminal so that a current to the flyback converter can be drawn from either the input or output. The buffer capacitors are also mounted on the microcontroller PCB for volume efficiency. The high voltage input and output connections are never run directly underneath the microcontroller.

3.4 Digital control

TI Delfino F28377D micro-controllers are used to coordinate the switching of the GaN devices in the multilevel step-up converter as well as MOSFETs in the full-bridge active rectifier. The digital control continuously calculates a switching duty ratio, which directly results in high power-factor and regulated output voltage. Therefore, much efforts have been made to optimize the digital control, as it plays a key role in the efficiency of the converter. The specific algorithm is laid out in more detail over the next paragraphs.

The Delfino contains four Analog-to-Digital Converters (ADCs) which can run in parallel. These ADCs are necessary for continuously measuring the signals that are used in calculating a duty ratio. The rate at which

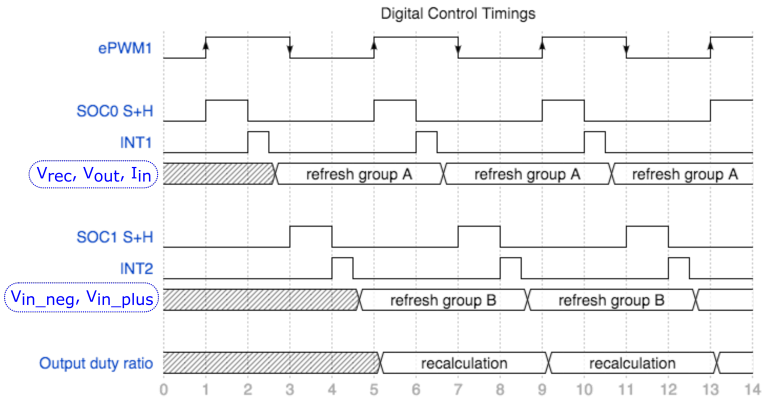

Figure 3.7: Timing diagram for signal-sampling and duty-ratio calculation

the signals are captured is controlled by using an on-board pulse-width modulator (PWM) to trigger ADCs in groups. These groups are managed by configuration sets called start-of-conversions (SOCs). A single SOC can group up to four simultaneous ADC conversions, but since five signals (V_{in_plus}, V_{in_neg}, V_{rec}, V_{out}, *and* I_{in}) need to be read to generate a corresponding duty ratio for PFC, five readings split into SOC0 and SOC1. A PWM signal is set to trigger SOC0 every up-edge and SOC1 every down-edge, such that the controller constantly receives fresh data. Each SOC fires an interrupt after conversion (SOC0 fires INT1 and SOC1 fires INT2), which triggers the respective routine to save the refreshed data to variables. After every second SOC, the duty cycle is recalculated. Timings for signal sampling and duty ratio calculation are demonstrated in Fig. 3.7.

A digital PFC scheme is implemented in order to achieve the required power factor. A block diagram of the PFC scheme is seen in Fig. 3.8. A TI-2000 microcontroller senses the rectified input voltage, V_{rec}, output voltage, V_{out} and inductor current, I_{in} and controls the converter using two feedback loop. While the outer loop which has a slower response regulates the output DC voltage, V_{out}, the inner loop with a much faster response shapes the input current [12]. The error term between the reference voltage, V_{ref}, and V_{out} is calculated. This error term is fed into the voltage loop compensator block that outputs U_{NV}. The voltage loop compensator's output, U_{NV}, is then fed into K_mABC block whose purpose is to scale the product of V_{rec} and U_{NV} and produce a reference current, I_{ref}, that has a shape of V_{rec} and peak current of the maximum allowable input current. The error term between I_{ref}

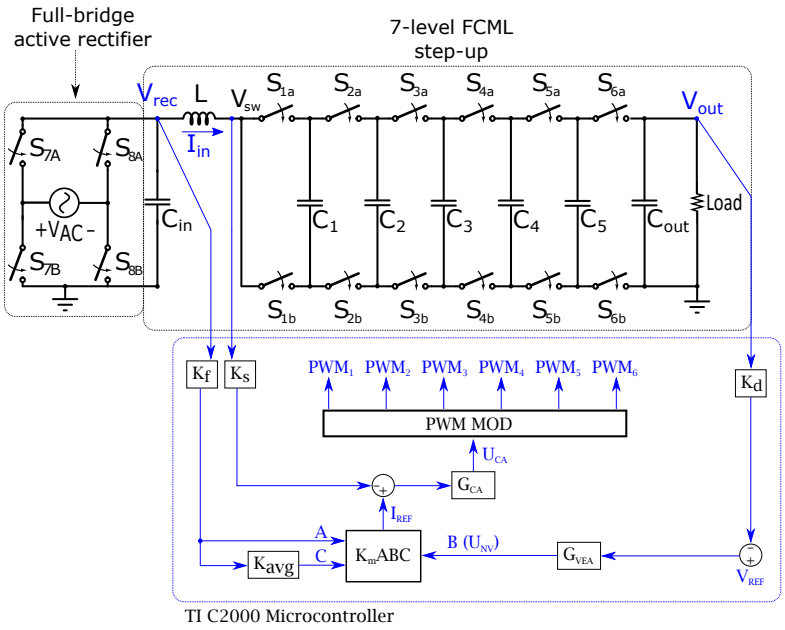

Figure 3.8: Block diagram of the power factor correction scheme [12]

and I_{in} is then fed into the current loop compensator, G_{CA}, whose output, U_{CA} goes to *PWM MOD* block to generate the PWM signal for each set of switches. As discussed in Chapter 2.2, a phase shift between any neighboring gate-driving PWM signals is $\dfrac{360^\circ}{N_{levels}-1} = 60^\circ$.

CHAPTER 4

THERMAL MANAGEMENT

A custom heatsink is fabricated to allow for proper cooling of the GaN switches, electrical isolation, and controlled thermal interface pressure as shown in Fig. 4.1. To make contact with the GaN devices, the mating surface has two parallel bars with an isolation channel in the middle. The channel accounts for the decoupling capacitors on the switching cell, which are taller than the GaN devices. The channel is also covered with polyamide tape to prevent arcing due to minimal capacitor to heatsink clearance.

Six more extrusions are placed on the mating surface to contact the main board and set the distance with the GaN devices and their associated contact bars. These legs are necessary to prevent too much pressure exerting on the switches as too much force can cause mechanical failure of the transistors.

To provide electrical isolation between the heatsink and GaN devices, a thermal gap-pad (Berquist GP000S35) is placed between the switches and the contact bars. This thermal interface material prevented arcing from occurring and provided thermal conductivity of 5 W/mK. The gap between the GaN devices and contact bars is set at 17 mil, which results in a thermal resistance of approximately 0.23 $^{\circ}Cin^2/W$.

The GaN devices are expected to generate a total loss of power as indicated in Fig. 4.2. This plot is generated by the script put together by Christopher Barth, Thomas Foulkes, and Dr. Modeer at the University of Illinois Urbana-Champaign. As the maximum average current through the switches is approximately 15 A, the maximum power loss in the GaN devices is approximately around 11-12 W. The size of the heatsink and the surface area of each fin is accordingly designed to dissipate this much power given an adequate amount of externally provided air circulation.

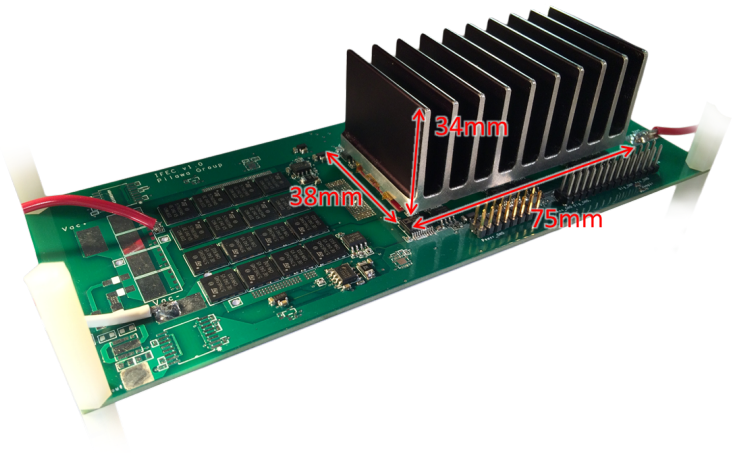

Figure 4.1: Seven-level FCML converter with the custom heatsink

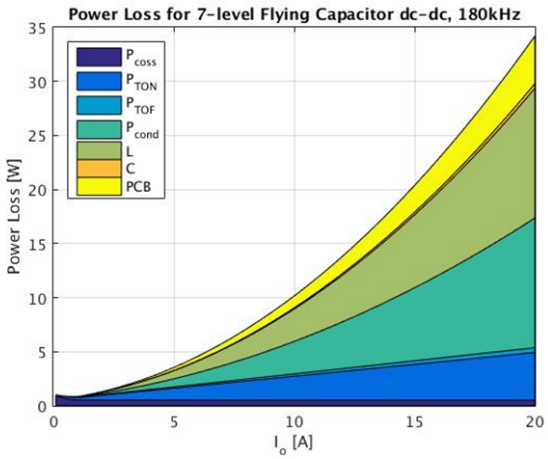

Figure 4.2: Power loss plot for GaN devices

CHAPTER 5

ELECTROMAGNETIC COMPLIANCE

Although a great deal of focus has not been placed on EMI compliance at this stage in the design process, the current prototype includes important features that improve its performance. The design of the PCB has led to a high minimization of current loops and switching loops that have very low inductance. As a result, reasonable suppression of common and differential mode EMI are expected. As a final note, the multi-level design greatly reduces EMI, since each switching node switches between 0 and $V_{DC}/6$ rather than the full 0 and V_{DC}.

An EMI filter implementation is work in progress. A successfully implemented EMI filter on the AC input will reduce the amount of EMI being fed back into the power line while a full enclosure will serve to remove the issue of radiated EMI. In addition, further reduction of current loops and a more compact design should result in better EMC.

The power research laboratory at Illinois is equipped to perform conducted EMI measurements to CISPR Class A with advanced spectrum analyzers and line impedance stabilization networks. An anechoic chamber in the antenna research lab will be used to perform radiated EMI measurements. With all of this equipment to provide detailed feedback on what areas of EMC need to be improved, optimizing EMI compliance for the final design will be made possible.

CHAPTER 6

TEST RESULTS

In order to demonstrate the functionality and performance of the seven-level FCML converter, the DC-DC and AC-DC tests were performed. Shown in Fig. 6.1 is the oscilloscope capture taken while the converter was running at 50 V DC input. Voltage, current, and power readings were taken through YOKOGAWA WT310 Digital Power Meter as shown in Fig. 6.2 and organized in Table 6.1. Note that the effective pulse frequency seen by the filtering inductor at V_{sw} is about 720 kHz which is $N_{levels} - 1$, 6 times larger than the switching frequency, f_{sw} of 120 kHz as mentioned earlier in Chapter 3.2.

Table 6.1: DC-DC Measurements taken from YOKOGAWA power meter

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Efficiency (%)
50	1.23	61.43	238.64	0.238	56.78	92.4

Table 6.2: Measurements from the AC-DC test

Duty = 0.4, $R_{LOAD} = 125\ \Omega$						
V_{in-RMS} (V)	I_{in-RMS} (A)	P_{in} (W)	$V_{out-RMS}$ (V)	$I_{out-RMS}$ (A)	P_{out} (W)	Efficiency (%)
10	1.24	3.71	20.24	0.16	3.20	86.1
20	1.26	15.34	42.19	0.33	13.93	90.7
30	1.92	34.85	64.15	0.50	32.18	92.3
40	2.58	62.54	86.35	0.67	58.30	93.2
50	3.24	97.85	108.37	0.85	91.80	93.8
60	3.89	140.91	130.44	1.02	132.75	94.2
$R_{LOAD} = 200\ \Omega$						
70	3.12	124.53	154.64	0.76	118.18	94.1
80	3.56	162.60	176.91	0.87	154.50	95.0
90	4.01	205.88	199.33	0.98	196.10	95.2
100	4.48	254.40	221.87	1.09	242.90	95.5
110	4.93	307.84	244.28	1.20	294.30	95.6

Shown in Table 6.2 are the measurements taken from the AC-DC test with the fixed duty cycle. Note that power factor measurements were not recorded

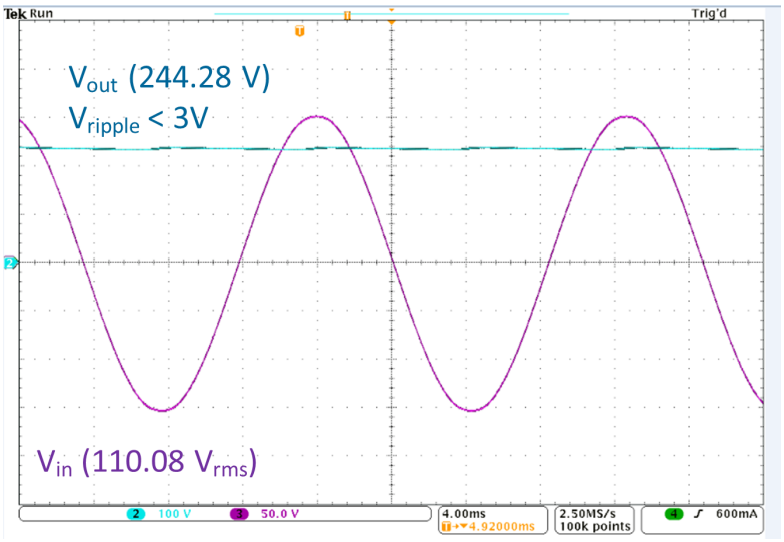

Figure 6.1: Oscilloscope capture at 50 V DC input

Figure 6.2: Measurements through YOKOGAWA WT310 Digital Power Meter at 50 V DC input

as the PFC scheme was not fully implemented yet. Fig. 6.3 and Fig. 6.4 show the oscilloscope capture at V_{in-RMS} = 110.08 V and thermal picture of the converter running at the same input voltage level, respectively. The thermal picture demonstrates well-planned heat distribution throughout the converter board. Finally, the plot of conversion efficiency, η vs P_{out} is shown in Fig. 6.5. Note that the efficiency increases as P_{out} increases. This is due to the fact that the switching loss dominant at the light load gradually becomes insignificant as P_{out} increases. Note that the tested power is still much lower than the targeted power of 1.3 kW, so the efficiency was measured to be relatively low. The efficiency will improve significantly to above 97%

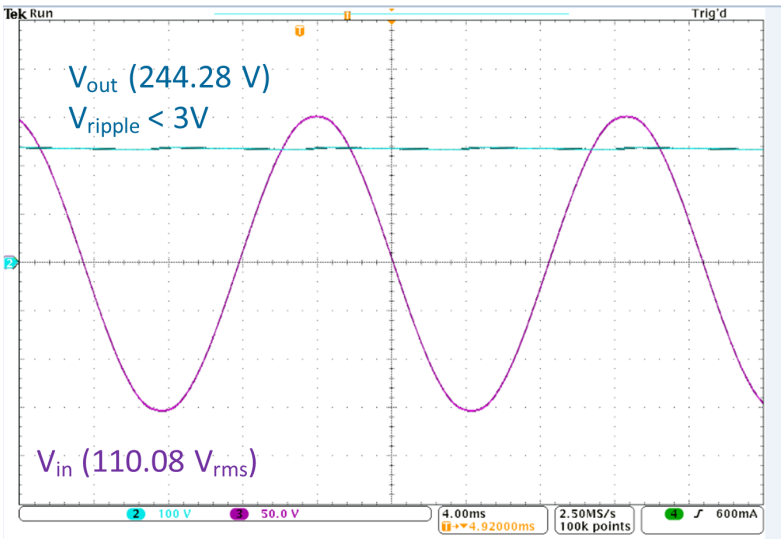

Figure 6.3: Oscilloscope capture at $V_{in} = 110.08\ V_{rms}$ and $P_{out} = 294.3$ W

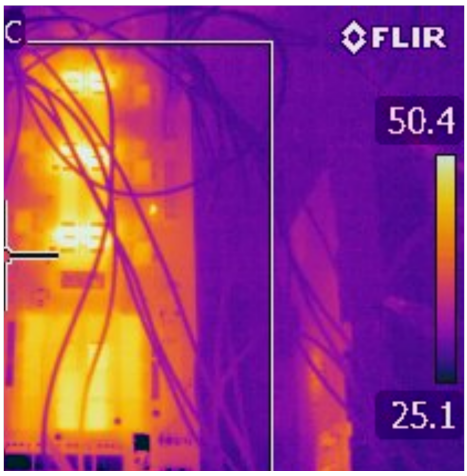

Figure 6.4: Thermal picture taken at $V_{in} = 110.08\ V_{rms}$ and $P_{out} = 294.3$ W

(design target) as the full power level is approached. The PFC is still under development at this point. Nevertheless, the output power of 294.3 W at 95.6% efficiency with the fixed duty cycle was achieved.

At this stage, the most critical and challenging problem, i.e., the design, implementation, and control of the FCML converter have been successfully demonstrated. Other aspects of the system, such as full power operation, PFC control, etc. are in steady progress. The performance which has been measured so far is in good alignment with the circuit analysis, and based on the available information, the performance of the proposed design in full functionality is projected in Table 7.1

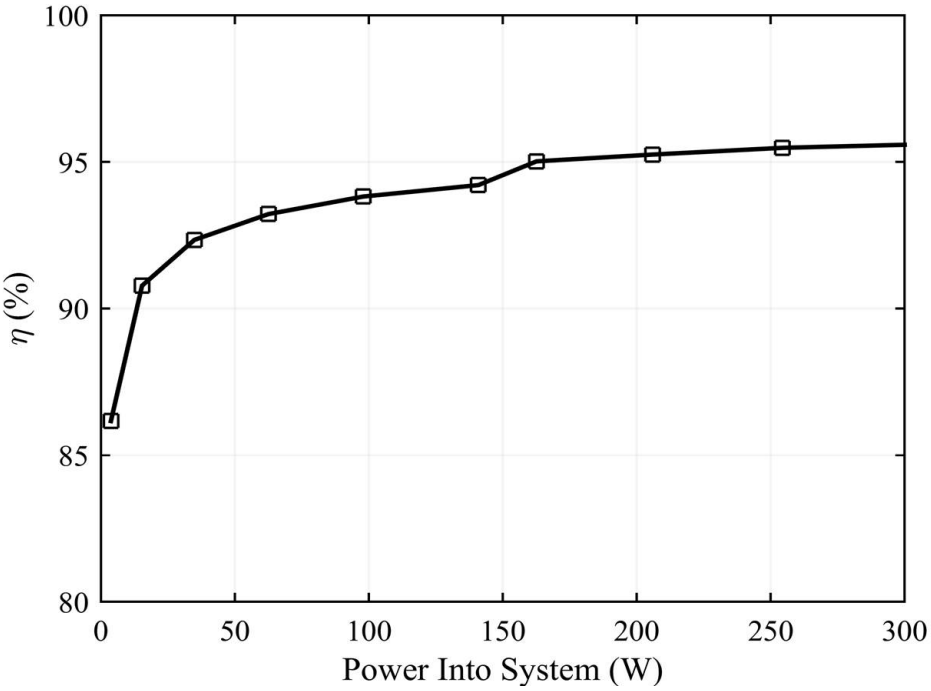

Figure 6.5: Plot of efficiency vs P_{out}

CHAPTER 7

CONCLUSION AND FUTURE WORK

Table 7.1: Projected performance of the prototype

$V_{in}(RMS)$ (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Efficiency	Power Density (W/cm^3)
115	11.90	1368.42	400	3.25	1300	0.95	2.0
230	5.83	1340.21	400	3.25	1300	0.97	2.0

Significant progress toward the completion of this project has been demonstrated. Specifically, the FCML converter has been successfully designed and operated, which is considered to be the most challenging part of this project. The PWM control of the FCML converter has been successfully developed through the TI C2000 micro-controller, and the performance of the AC-DC converter to about 300 W has been recorded and verified. The immediate next step is to extent the power and voltage level. In the meantime, the development of digital control for PFC operation is in steady progress. In the next few week, a new revision of the PCB and heatsink will be made to improve the overall form factor and further shrink the overall volume. Double the power density of the system is expected after such a revision. If time permits, an active energy buffer with a sophisticated digital control will be implemented to replace the electrolytic capacitor bank with the carefully chosen ceramic capacitors through the extensive capacitor evaluation performed by our research group [13]. This will result in a further volume miniaturization and therefore higher power density [10], [11]. Based on the current progress, it is likely to implement a prototype that meets or surpasses the projection in Table 7.1.

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