TIME-BASED LOW DROPOUT REGULATOR

BY

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THESIS

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Abstract

The low dropout regulator (LDO) is an essential building block for modern integrated circuits. Traditional analog design faces formidable challenges as technology scales down, such as lower supply voltage and channel length modulation. Digital LDOs do not have the problems that analog LDOs have, but they usually have worse performance metrics. Therefore, a time-based LDO is proposed to combine the merits of both analog and digital together. In the end, the LDO achieves 0.6-1 V supply voltage range and 0.5-0.9 V output voltage range. The maximum output current is 50 mA and the worst case transient time is 1.58 μs under 0.6 V supply voltage. The maximum current efficiency is 99.98%.

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1. Introduction

In the past 30 years, the semiconductor industry followed Moore's law to develop very-large-scale integration (VLSI). The law predicts that the number of transistors in an integrated circuit chip doubles every two years. Although complementary metal oxide semiconductor (CMOS) technology scaling provides faster speed, higher density and lower cost for digital circuits, it also leads to challenges to analog design—higher randomness, reduced voltage supply, channel length modulation, etc.

Analog blocks are used as peripheral circuits for digital blocks, and power management is one of the most important ones. Modern power management circuits usually consist of two parts: switched-mode power converters and linear regulators. While the former is used as an interface between power-rail supply (110 V) and on-chip supply (1~5 V), the latter is used to further reduce switching noise. Traditional LDO uses an operational amplifier (op-amp) to provide feedback control. However, under low supply voltage, an op-amp may suffer from insufficient voltage headroom. Therefore, an LDO using time-based control scheme is proposed to address these issues.

This thesis is organized as follows: chapter 2 covers the background of LDO design and reviews prior art in low voltage LDOs; chapter 3 explains system-level analysis of time-based LDO; chapter 4 presents detailed circuit implementations; chapter 5 shows

simulation results from Cadence Spectre; chapter 6 states the possible future work; and chapter 7 concludes the thesis.

2. Background and Review

The basic topology of LDO is shown in Fig. 1. It consists of four parts: a pass transistor, an op-amp, a load capacitor and the load (represented by a load resistor). In this circuit, if everything works properly and the negative feedback loop is stable, v_{fb} should be the same as v_{ref} for any input voltage v_{in}. The load current I_L is calculated to be $\frac{v_{ref}}{R_L}$.

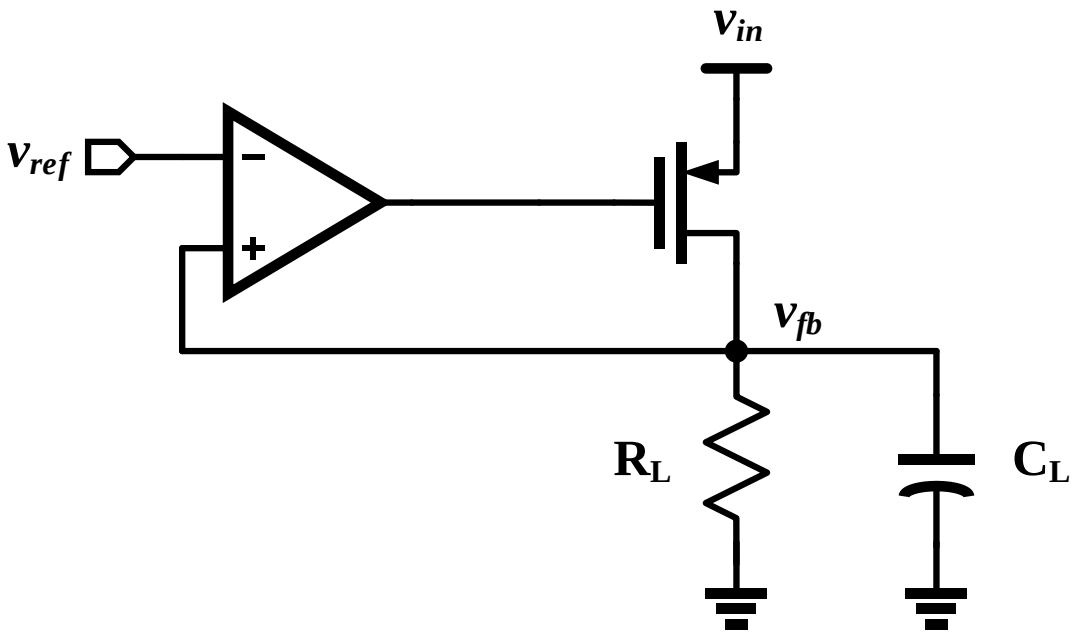

Figure 1: Traditional analog LDO schematic

2.1 LDO Metrics

In this section, design metrics of the LDO are discussed [1].

Input/Output Voltage Range

An LDO is first characterized by the operation range. A wide range of operation is desired for different load conditions. For different applications, the range can be widely different. Most analog environments require output to be greater than 1 V while in sub-micron digital, output voltage can be as low as 0.5 V.

Maximum/Minimum Load Current

Maximum load current indicates the maximum power available from an LDO and minimum load current is the point where LDO can operate before going into unstable.

Dropout Voltage

Since $v_{fb} = v_{ref}$, the voltage drop across the pass transistor is $v_{in} - v_{ref}$ and the wasted power is therefore $(v_{in} - v_{ref})*I_L$. We thus define the dropout voltage as

$$v_{dropout} \equiv v_{in} - v_{ref}$$

For power efficiency, we want as low $V_{dropout}$ as possible. However, a certain voltage headroom is required to maintain the pass transistor in saturation for reasonable power supply rejection ratio (PSRR). Typically a 0.2 V headroom is required for >1 V v_{in} and 0.05-0.1 V for >0.5 V v_{in}.

Quiescent Current

There is a small amount of current consumed by the controlling circuit to make the LDO work properly, which is defined as quiescent current I_Q. In Fig. 1, it is the current consumed by the op-amp.

Power Supply Rejection Ratio (PSRR)

PSRR is an important metric measuring the LDO's ability to reject the supply noise. It is defined as

$$\text{PSRR} \equiv \frac{v_{o,ripple}}{v_{i,ripple}}$$

Transient Response

Transient response measures the settling time of the output when there is a step change in the output current. It is decided by many factors: loop bandwidth, op-amp slew rate, output capacitor, etc.

2.2 Design Considerations and Literature Review

Loop Stability

Loop stability directly indicates the functionality of an LDO—a working LDO must be stable. Further, the phase margin should be good enough such that the transient response is reasonable. To analyze the loop gain characteristic, a small signal model is

shown in Fig. 2, where $G_{m,a}$ is the transconductance of the error amplifier, r_o is the output resistance of the error amplifier, G_m is the transconductance of the pass device, r_{ds} is the equivalent output resistance of the pass device, C_{gg} is the total parasitic gate capacitance of the pass device, and β is the feedback factor.

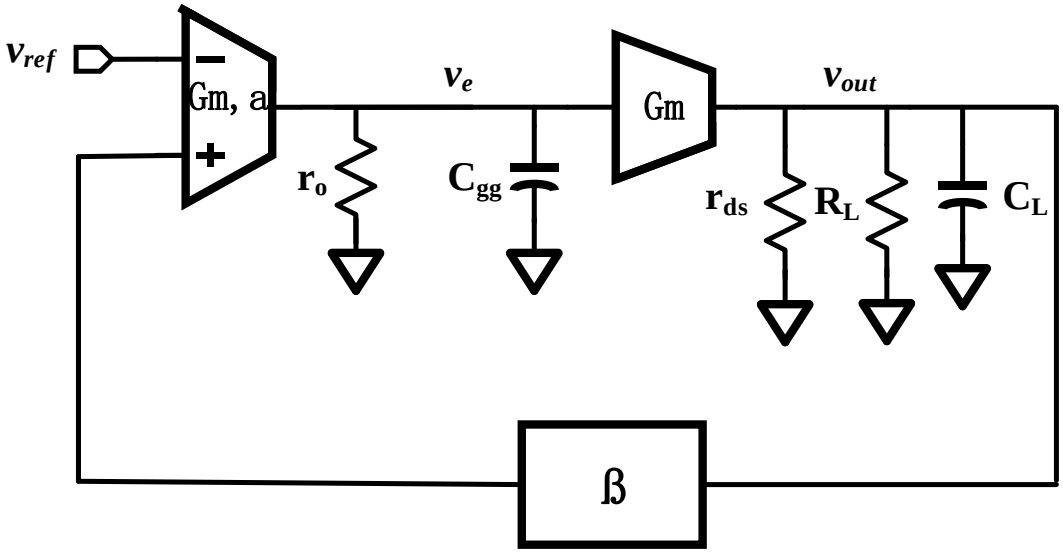

Figure 2: Traditional LDO small signal model

Obviously, there are two poles in the system: one at the output, formed by the output capacitor and the effective output resistance (R_L in parallel with $r_{ds,\ PMOS}$), the other at the output of the error amplifier, formed by its output resistance r_0 and pass device's gate capacitance C_{gg}. Usually when the LDO is designed to support a big output current, the size of the pass device will be extremely big, making C_{gg} big as well. A stability problem arises since these two poles might be close to each other. In addition, the output pole may vary a lot, further degrading the loop phase margin. As a result, compensation

techniques are usually adopted to stabilize the loop. There is yet another interesting question unsolved: Which should be dominant, the output pole or the one at the gate of the pass device? This question will be illustrated next.

PSRR

PSRR is an important parameter of an LDO—it tells to what extent an LDO can reject supply noise. To figure out how PSRR behaves with respect to frequency, a small signal analysis needs to be conducted.

The small signal model for PSRR analysis is shown in Fig. 3. Note that r_{ds} is in the input path and is not in parallel with R_L anymore.

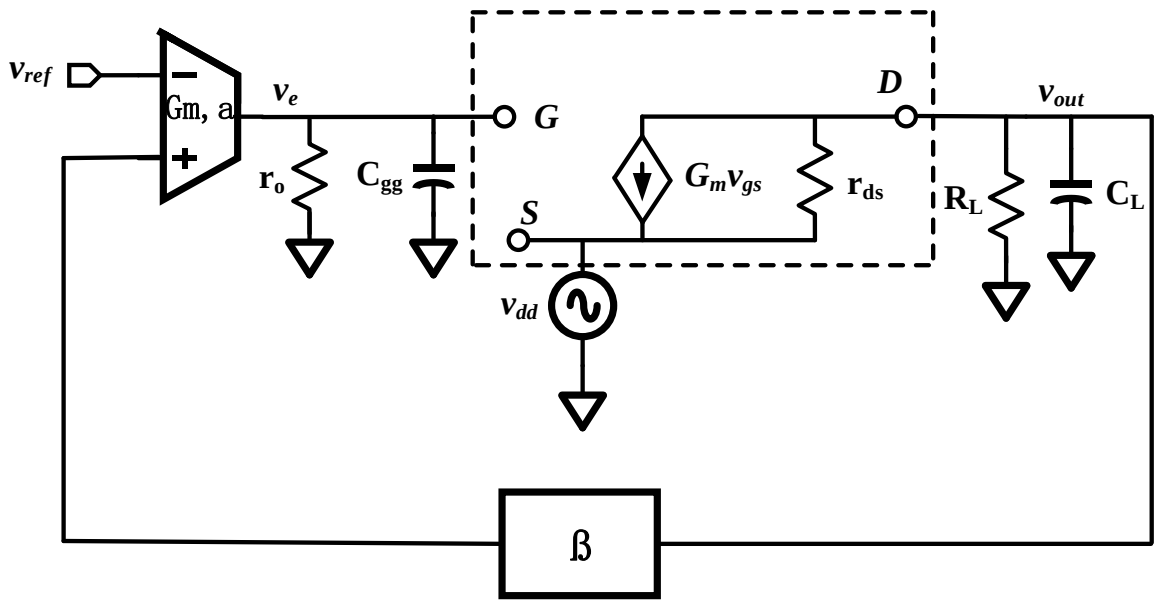

Figure 3: Small signal for PSRR analysis

Now the transfer function of PSRR could be written as:

$$\mathrm{PSRR(s)} = \frac{vout}{vdd} = \frac{1 + G_m r_{ds}}{1 + \frac{r_{ds}}{R_L // \frac{1}{sC_L}} + G_m \beta g_{m,a} (r_o // \frac{1}{sC_{gg}}) r_{ds}}$$

Note that there is one assumption—the op-amp is immune to supply noise. This is generally a valid assumption since a properly designed op-amp should have PSRR better than or equal to that of the LDO.

From the expression, in the denominator there are three terms: the second term represents the effect of the output pole and the last term represents the effect of the error amplifier. Ideally, when the error amplifier's gain is infinite, that term and thus the denominator both become infinite and PSRR becomes 0. As a result, we want the parasitic pole to be greater than the output pole. As shown in Fig.4, PSRR is plotted vs. frequency under two conditions: (1) output pole is dominant; (2) parasitic pole is dominant.

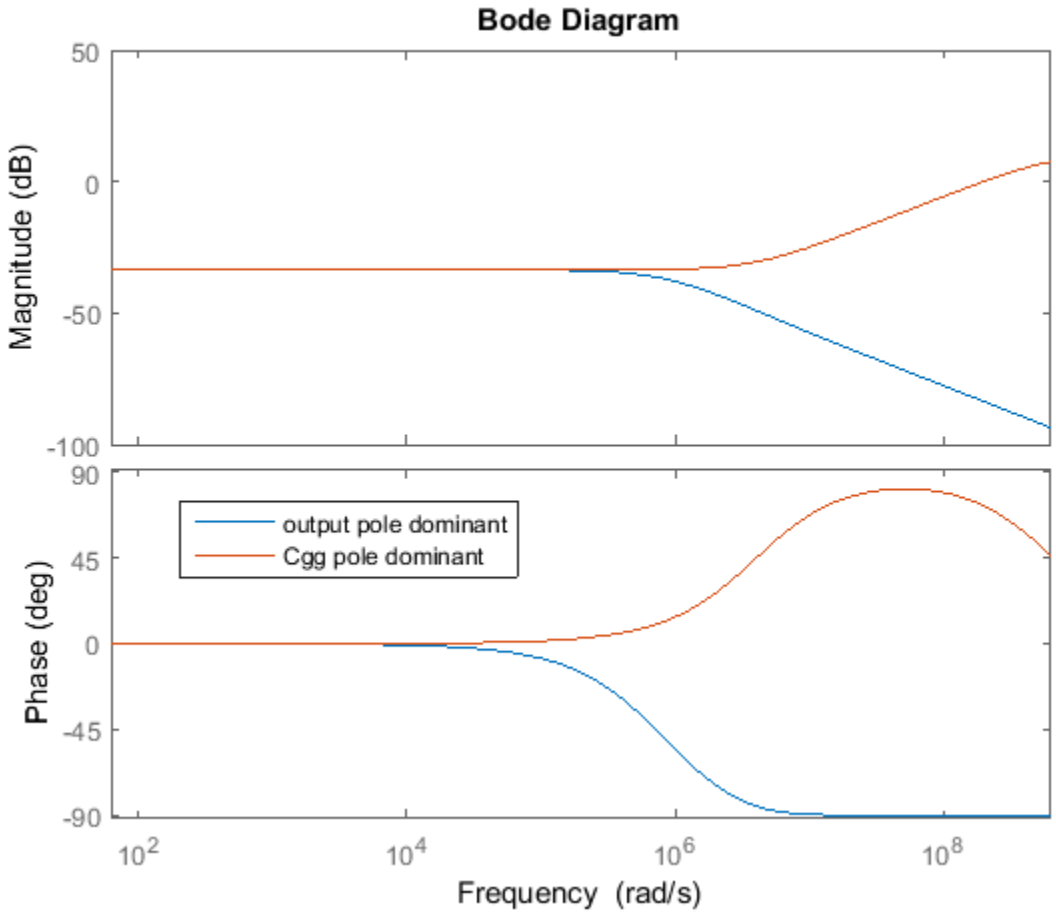

Figure 4: PSRR of an error amplifier based LDO

From Fig. 4, PSRR quickly deteriorates when the parasitic pole is dominant. This makes sense because, intuitively, the loop begins to lose the property of negative feedback when the loop gain decreases, and when there is no gain from the op-amp, the pass

transistor just acts as a common gate amplifier for the supply noise. Therefore, for applications where high PSRR is necessary, the output pole must be dominant.

Transient Response

There are two types of transient response: small scale and large scale. The former happens when the magnitude of load transient change is small. Under this condition, the settling time will be governed by the loop bandwidth as well as the phase margin. On the other hand, the latter happens when the load transient is too big such that the small signal loop analysis does not hold. For example, when a load transient from 1 mA to 100 mA happens, the gate voltage cannot react fast enough to respond to such big change. Therefore, the output voltage will drop significantly and the op amp will slew. The output voltage drop will be inversely proportional to the output capacitor size as the rate of change ($\frac{dv_{out}}{dt}$) is the same as ($\frac{I_{out}}{C_L}$). To improve this, one can increase the output capacitor, at the cost of lower bandwidth and slow small-scale settling. Also, if the output pole is not dominant, stability might be impaired.

Capacitor vs. Capacitorless and Analog vs. Digital

Traditional LDOs require a huge off-chip output capacitor for PSRR and transient response consideration. While the LDO's performance is good, it is impossible to integrate on chip since the capacitor is too big (at the range of a few microfarads). In addition, as technology scaling continues, several formidable challenges appear for

analog design, especially channel length modulation and lower supply voltage. For example, in [2] an LDO with -56 dB PSRR at 10 MHz and maximum load current of 25 mA was proposed. However, it required an off-chip capacitor and could not work under low supply voltage.

Digital LDO usually employs an analog-to-digital converter (ADC) in the feedback loop to perform control mechanism in digital domain, and then convert the signal back to analog using a digital-to-analog converter (DAC). Although it can work under low supply voltage, its performance such as PSRR and transient response is not as good as analog LDO. In [3], a digital capacitor-less LDO using a comparator and a shift register as control loop was proposed. Although it achieves low voltage operation, its maximum load current is only 0.2 mA and its settling time is very long. In [4], a successive approximation analog-to-digital converter based control was proposed and achieved a maximum output current of 200 mA with peak efficiency of 99.6%. However, it still required a load capacitor of 1 μF and could not operate in low voltage range.

3. Proposed Time-Based LDO

As previously pointed out, traditional analog control suffers from design difficulties due to lowered supply voltage from technology scaling. Digital capacitorless LDO, on the other hand, has poor PSRR even if it can operate at low supply voltage. We therefore proposed a time-based control technique for LDO such that it can achieve both low supply voltage and reasonable PSRR at the same time. Also, its load current range was chosen to be 100 times, from 0.5 mA to 50 mA.

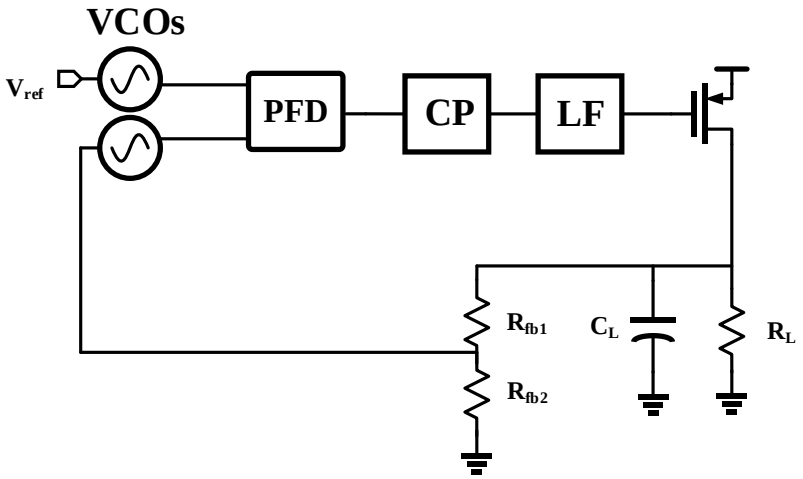

Figure 5: Proposed LDO block diagram

As shown in Fig. 5, the control path comprises two voltage controlled oscillators (VCOs), a phase and frequency detector (PFD), a charge pump (CP) and a loop filter (LF). The VCO acts as an integrator in phase domain, providing infinite DC gain as long as it is oscillating. The PFD generates an error signal in the form of pulse width modulation

(PWM) by comparing the phase difference between the two VCOs. The CP converts the PWM error signal into current, and then passes it through the LF to finally convert it into voltage domain. In steady state, the phases of the two VCOs will align and the PFD will have average zero output, thus achieving phase lock. Therefore, the output voltage will be the same as the reference voltage. Compared with a traditional analog phase locked loop (PLL), the only difference is that the pass device and the load appear in the loop. To understand how the loop dynamics will deviate from a PLL, a small signal loop model needs to be developed.

3.1 System-level Block Diagrams

VCO

As discussed before, a VCO acts as an ideal voltage-to-phase integrator. The mathematical model for a VCO can be written as

$$f_{osc}(V) = f_{fr} + V * K_{VCO}$$

where f_{osc} is the oscillation frequency, f_{fr} is the free-running frequency when no voltage is applied, and K_{VCO} is the frequency-to-voltage gain. The graphical transfer characteristic is shown in Fig. 6. Since phase is the integral of frequency, in Laplace domain the transfer function can be simply written as

$$\mathrm{H(s)} = \frac{K_{VCO}}{s}$$

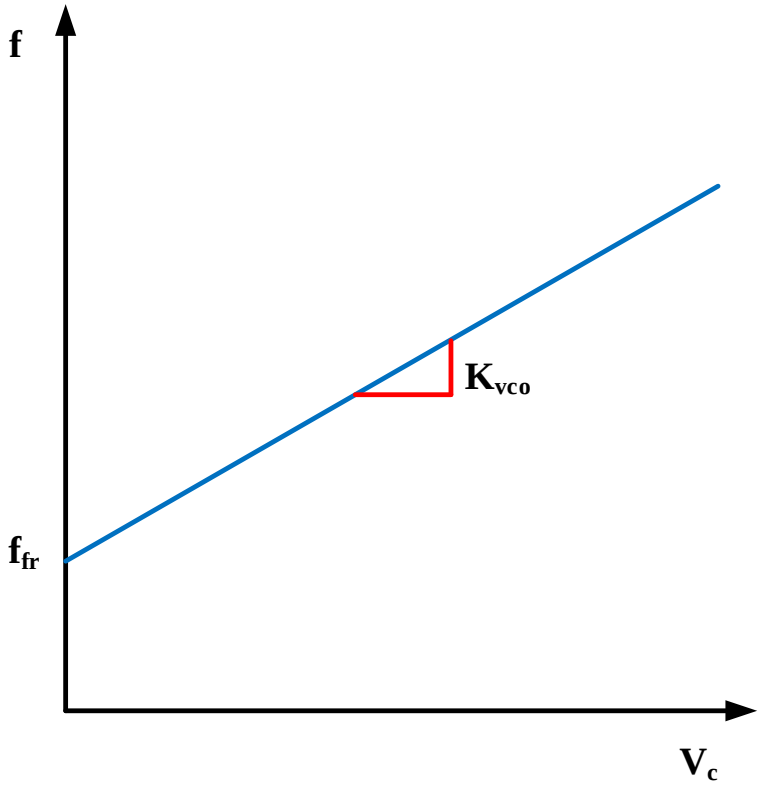

Figure 6: Ideal VCO transfer characteristic

PFD

A PFD compares the phase and frequency differences between two VCOs and outputs two PWM signals: UP and DOWN that represent phase lead/lag as shown in Fig. 7.

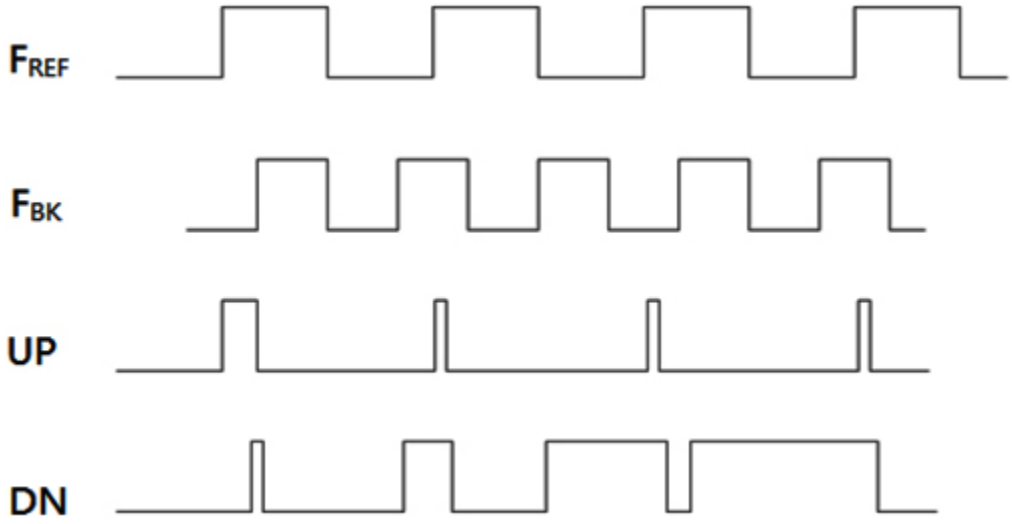

Figure 7: PFD output waveform

Although a PWM signal is essentially nonlinear, its average on time (a.k.a. duty cycle) carries the useful information. The reason a PFD is used here instead of a phase detector (PD) is because of one unique feature of PFD—it also tells the frequency difference. A PD, usually implemented using an XOR gate, can only tell the phase difference between two signals and therefore has finite input range. Once the input phase difference exceeds the boundary, the output polarity will flip, changing the loop from negative to positive feedback. A PFD, however, does not have this problem.

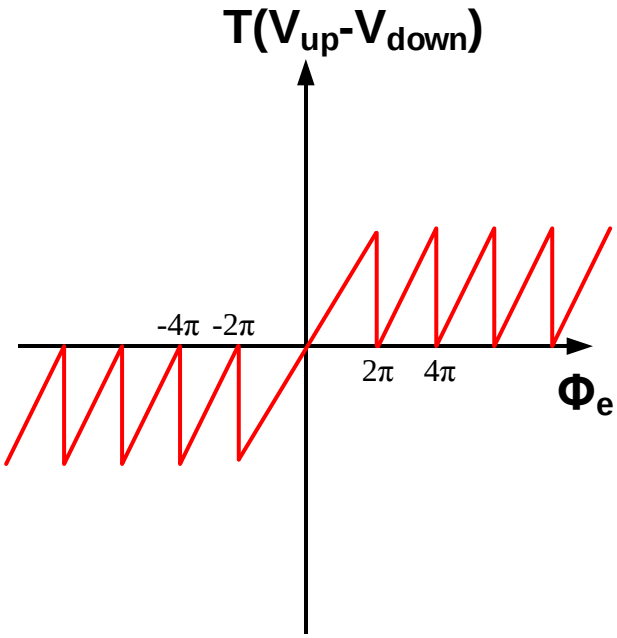

Figure 8: PFD transfer function

Illustrated in Fig. 8, the on time (the period of UP signal minus that of DOWN signal) is plotted against the phase difference. On the positive x-axis, the output is always greater than zero, indicating that the frequency difference is discovered by the PFD.

The transfer function that relates the average on time and the phase difference can be written as

$$H(s) = \frac{1}{2\pi}$$

CP

A CP's functionality is to output a positive or negative current based on the PD's output. Since it operates in the case of period, it can be characterized by its average output current as output and phase difference as input. When the phase difference varies from 0 to 2π, the output current changes by I_{CP}. Therefore, its transfer function can be written as

$$H(s) = I_{CP}$$

LF

An LF converts the output from the CP from current to voltage such that the VCO can be properly controlled. From a control theory perspective, a system that has nth-order pole at DC (s=0) can track input signals with k-th polynomial degrees, where k<n. Since there is already an integrator (the VCO), the system is at least type-I and can track phase step input without any steady state error. However, in reality frequency step also happens quite often and therefore a second integrator is needed. This does lead to a stability problem on the other hand, due to the fact that an integrator gives -90 degrees phase shift and there will be no phase margin if there are two integrators in the loop. As a result, a left-half-plane zero needs to be created to give enough phase margin. The combined analysis indicates that a proportional-integral control scheme is needed and will be constructed by the LF. The transfer function of an LF can be therefore written as

$$H(s) = \frac{K_I}{s} + K_P$$

where K_I is the integral-path gain and K_P is the proportional-path gain.

Pass Device

As previously characterized, the pass device can be modeled as a g_m stage, an output resistance and a gate capacitor. The load is simply an RC network, creating a pole at a potentially low frequency.

There is yet another problem that has not been taken into account—the gate leakage current. This is a unique drawback for sub-micron devices, caused by the dioxide becoming very thin; as a result, the probability of an electron at the gate tunneling through the oxide increases significantly. Shown in Fig. 9, the gate leakage current is plotted vs. temperature under different load conditions. When under full load, the leakage current is 0.97 μA and it can vary ± 0.2 μA for different temperatures. As load current decreases, the leakage current decreases and is negligible at light load. The reason is that higher load current i_{sd} leads to higher voltage drop v_{sg}, which makes i_{leak} bigger. Considering that the gate is directly connected to the charge pump, its effect on the loop dynamics must be investigated.

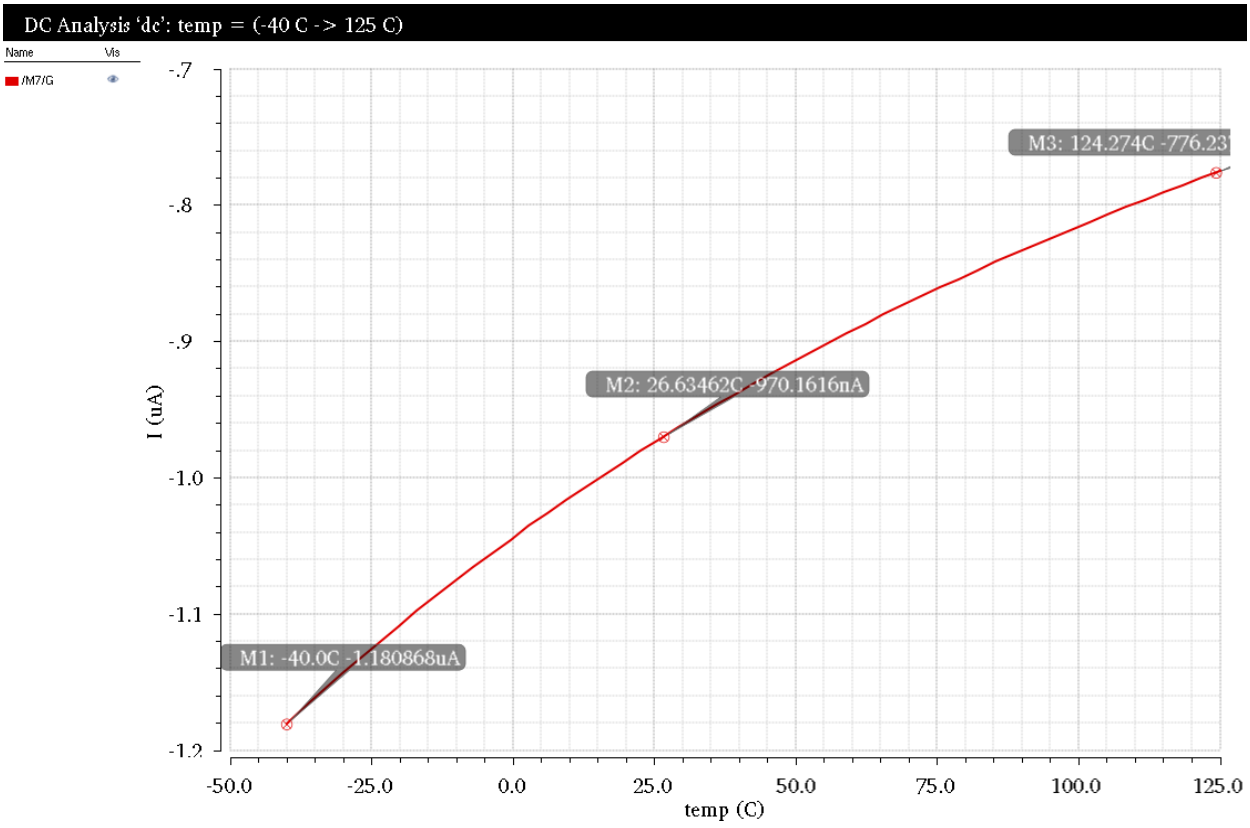

Figure 9: Leakage current vs. temperature

Figure 10 shows the part of the model of the loop with the leakage current being modeled as a constant current source connecting from VDD to the gate. In steady state, the charge pump must turn on for a small period of time in order to offset the charges coming from i_{leak}. In other words, this will lead to a static phase offset. Mathematically, from charge balance, an equation can be derived as follows:

$$i_{leak} * T = I_{CP} * D * T \Rightarrow D = \frac{i_{leak}}{I_{CP}}$$

where T is the clock period and D is the percentage of the on-time of the charge pump. From the expression, intuitively if one wants to reduce D, he or she should make I_{CP} larger since i_{leak} cannot be easily changed.

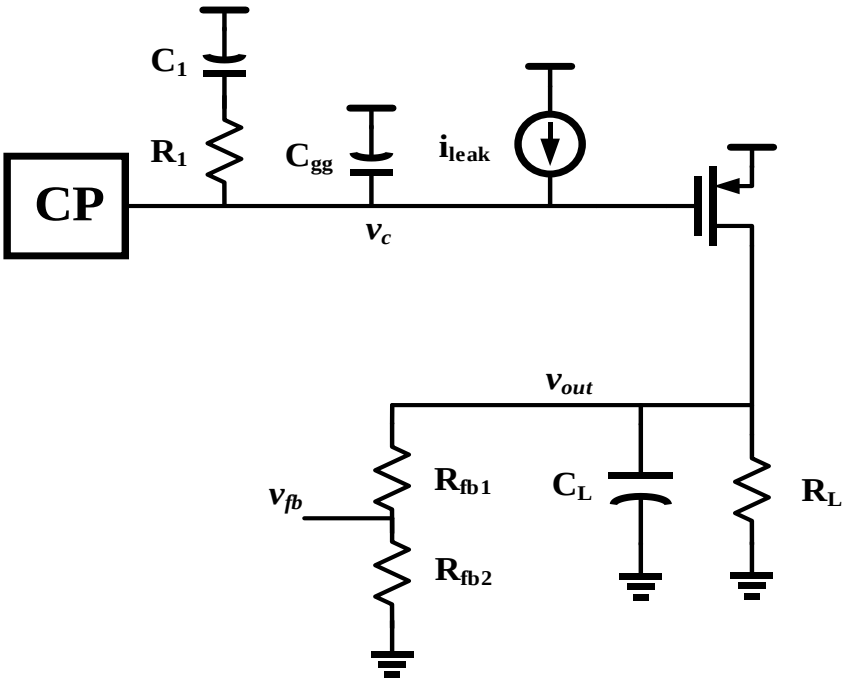

Figure 10: Circuit model of leakage current

One consequence of the static phase error is the voltage ripple at v_c (and therefore v_{out}). The expression for change in v_c is

$$\Delta v_c = \frac{I_{CP} - i_{leak}}{C_{eff}} DT = \frac{i_{leak}}{C_{eff}} (1 - D)T$$

where C_{eff} is the effective capacitance seen at v_c. Recall that to make D smaller one might increase I_{cp}. This way, however, will increase the voltage ripple. There are thus two design tradeoffs: (1) for fixed device size, D decreases as I_{cp} increases, but voltage ripple increases and $\Delta v_{c,max} = i_{leak} * T/C_{eff}$ when D=0; (2) for fixed I_{cp}, D decreases as device size decreases, but voltage ripple increases (assuming C_{eff} and i_{leak} both scale linearly with device area). Of course, the clock frequency can always be increased to reduce voltage ripple and phase offset, at the cost of more power.

To verify these, Verilog-A based simulations are run and shown in Figs. 11-13. Figure 11 shows the output voltage ripple for a smaller I_{CP} and Fig. 12 shows the ripple for a larger I_{CP}. It can be clearly seen that although static phase offset decreases, the output ripple voltage increases. Figure 13 shows the output voltage ripple for the same I_{CP} as Fig. 11 but bigger device size.

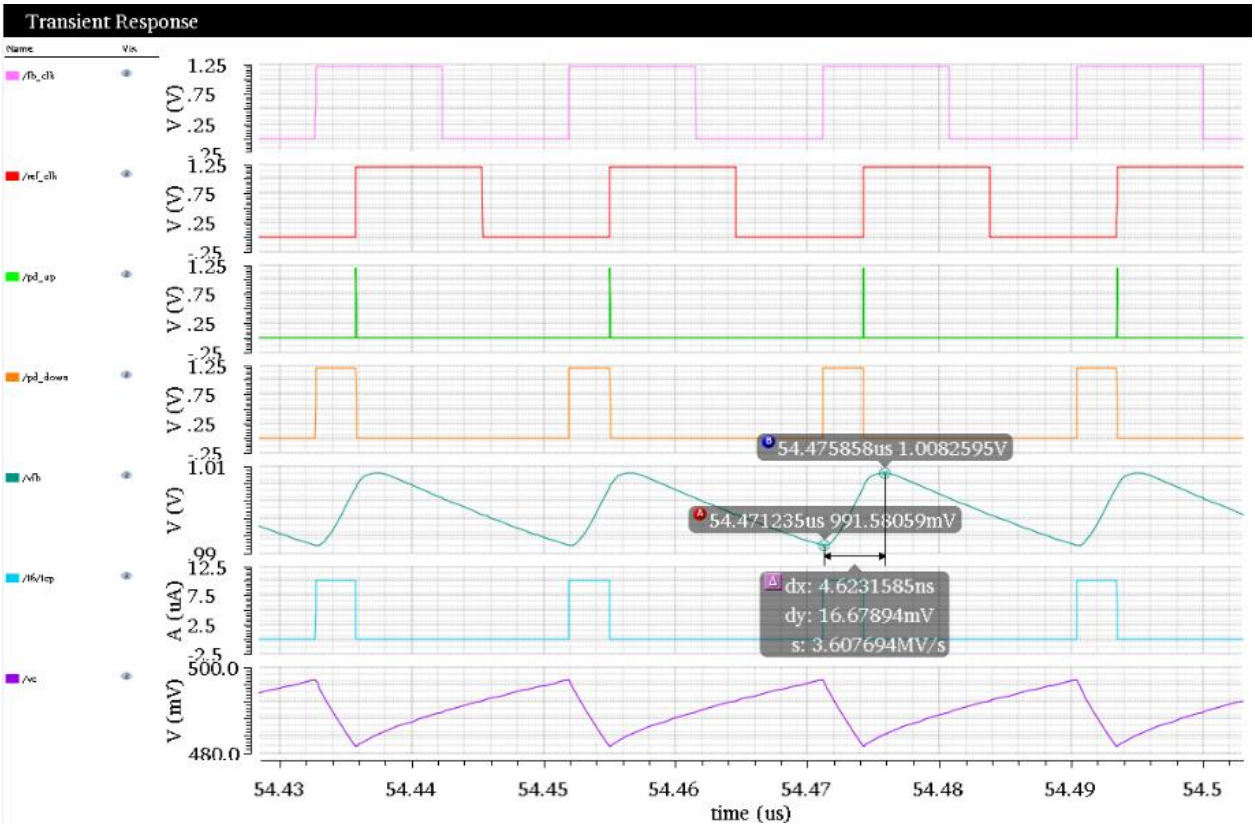

Figure 11: Steady-state behavior with small I_{cp} and small device

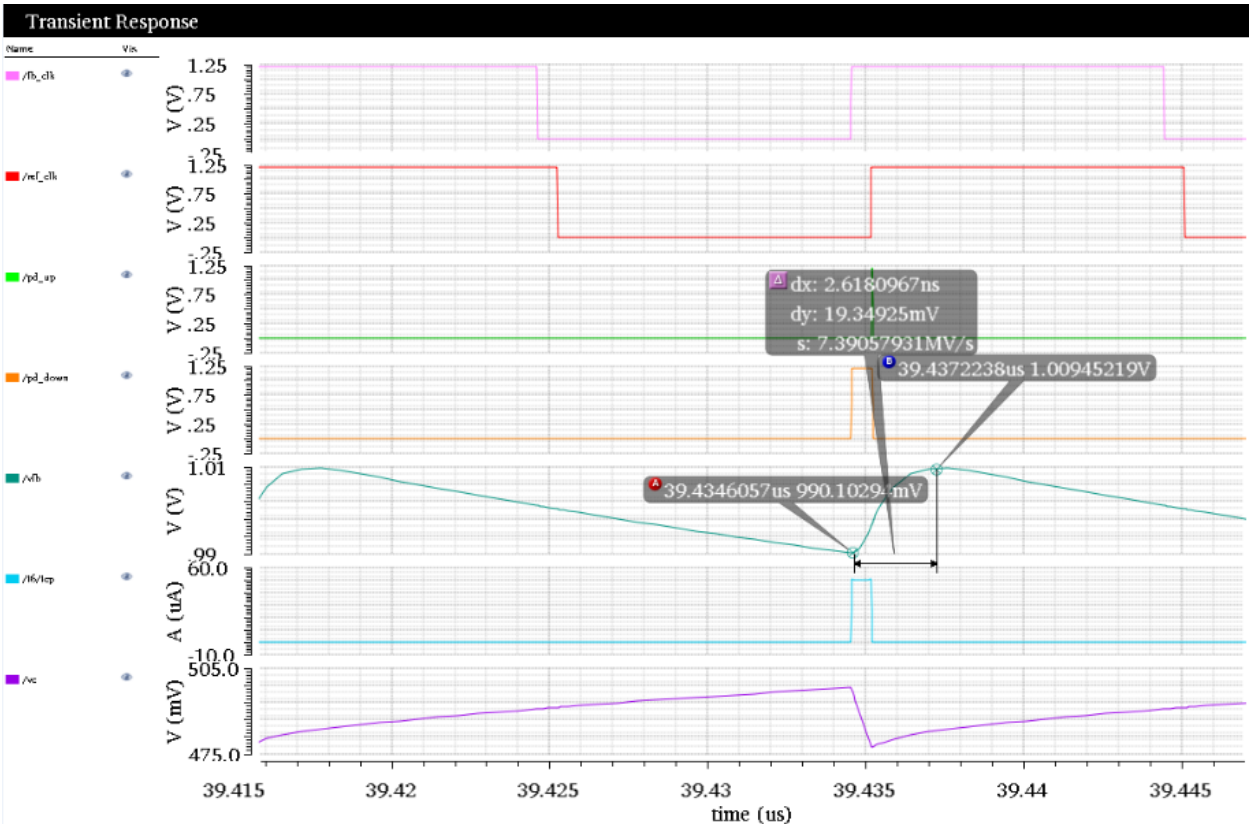

Figure 12: Steady-state behavior with big I_{cp} and small device

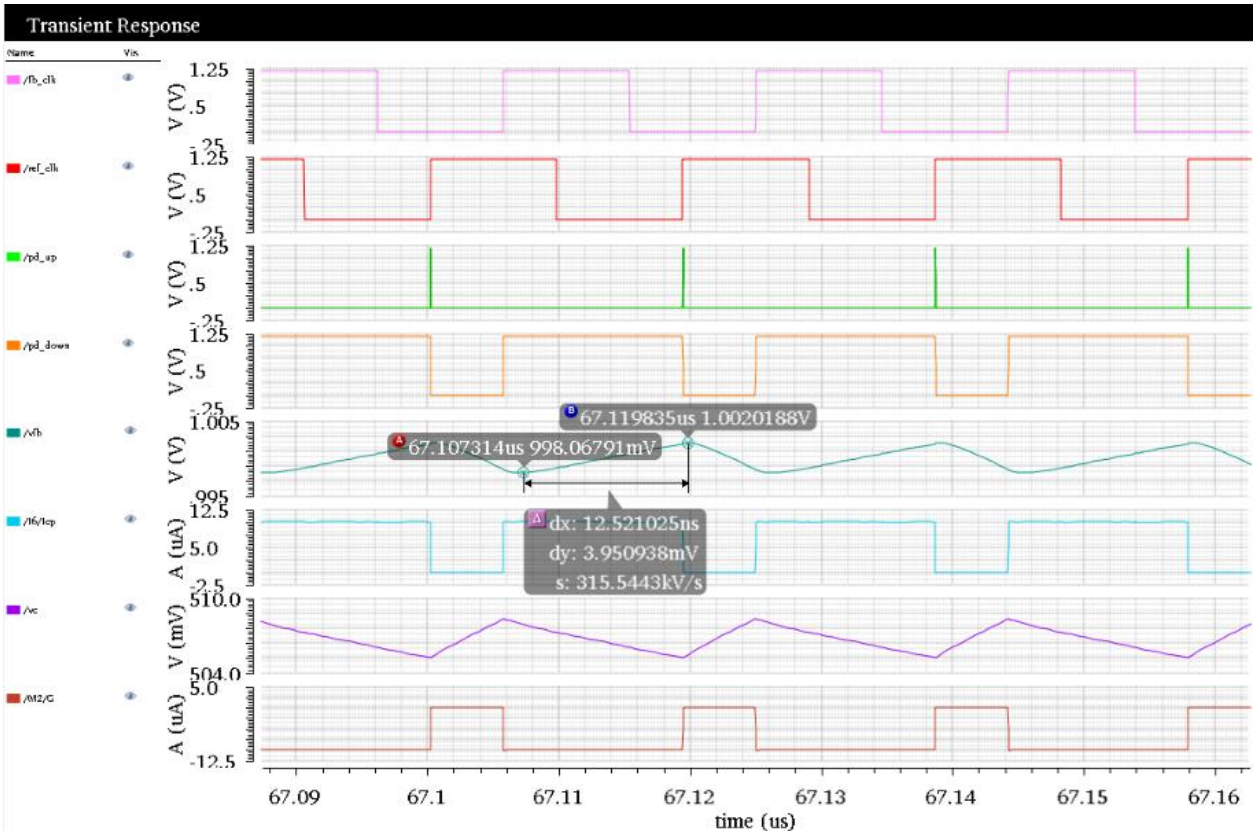

Figure 13: Steady-state behavior with small I_{cp} and big device

Summarized in Tables 1 and 2, the simulated static phase offset is the same as the calculated. As a result, there is a phase offset vs. output voltage ripple tradeoff that must be considered carefully for different applications.

Table 1: Steady-state behavior summary for fixed size

Icp	Δv_c	Δv_{fb}	Δt	**T**	**D(Δt/T)**	**D(i_{leak}/I_{cp})**
10 µ	15.49 m	16.68 m	3.1 n	19.23 n	0.1612	0.1589
50 µ	20.67 m	19.35 m	0.63 n	19.84 n	0.032	0.0318

Table 2: Steady-state behavior summary for fixed I_{CP}

Size	Δv_c	Δv_{fb}	Δt	**T**	**D**
Small	15.49 m	16.68 m	3.1 n	19.23 n	0.1612
Big	5.58 m	3.95 m	13.66 n	19.23 n	0.71

There is another way to reduce both static phase offset and output voltage ripple: use thicker oxide device. However, in this design it was too big to fit both 50 mA load current and 0.6 V supply voltage.

3.2 System-level Loop Analysis

Having every building block's small signal model, the loop dynamics can be simulated in Matlab. The small signal model of the entire loop is shown in Fig. 14. Loop gain analysis for different load conditions is shown in Fig. 15 and phase margin and bandwidth are shown in Fig. 16. The worst phase margin is 48 degrees at full load and the worst bandwidth is 0.4 MHz at full load as well. One thing to note here is that the maximum available phase margin and bandwidth at full load are actually larger than those under light load. If the magnitude of the loop gain can be adaptively increased, the loop dynamics will get better at heavier loads.

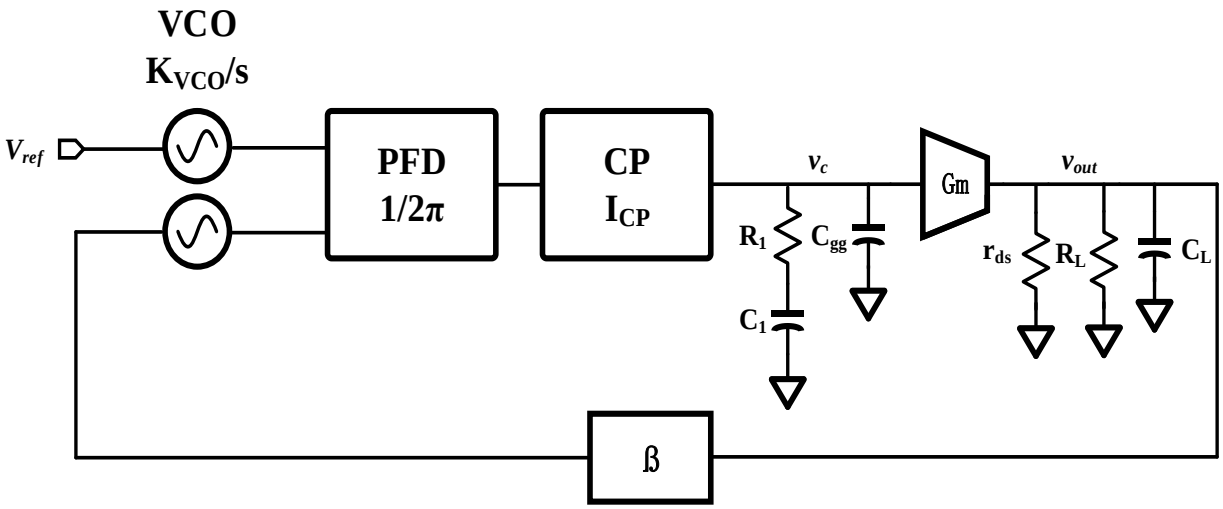

Figure 14: Small signal model of proposed LDO

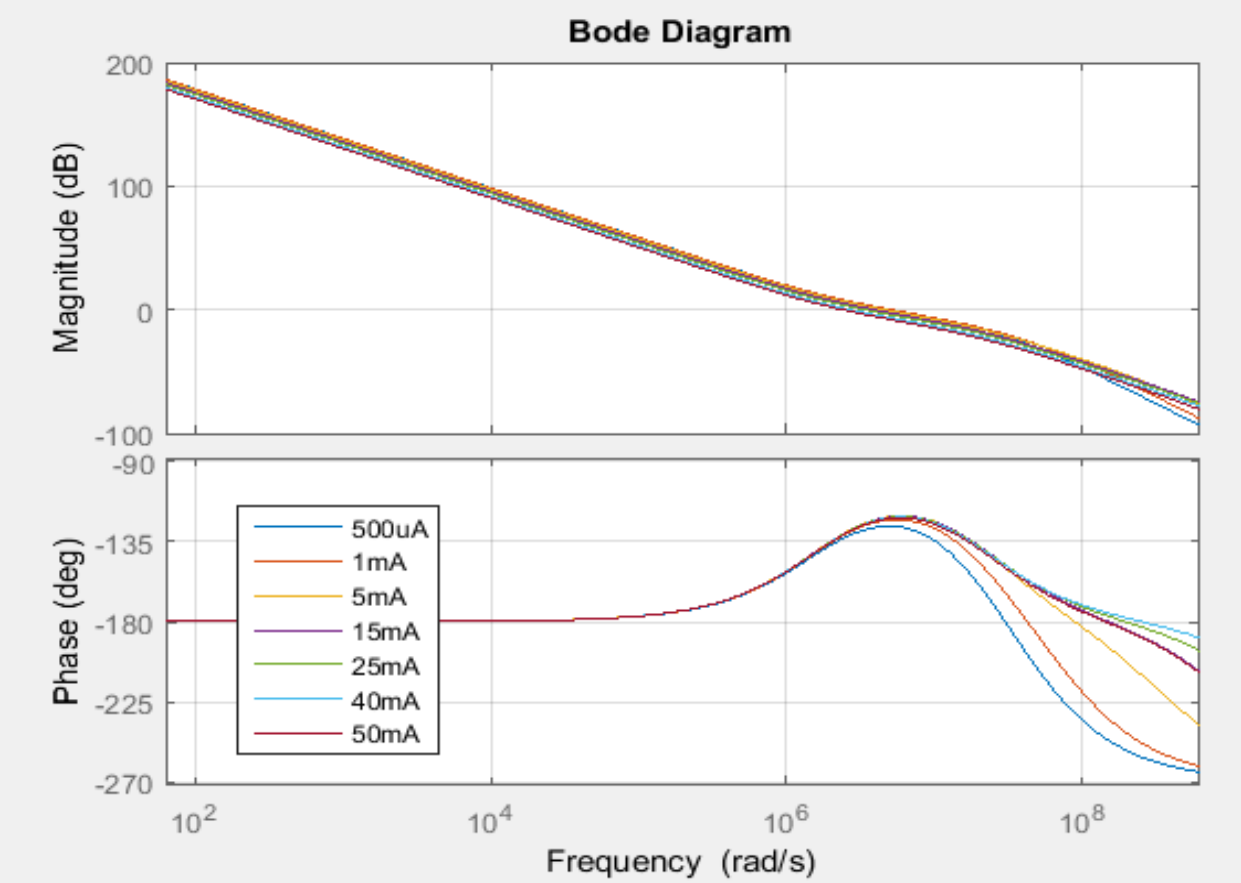

Figure 15: Loop gain analysis

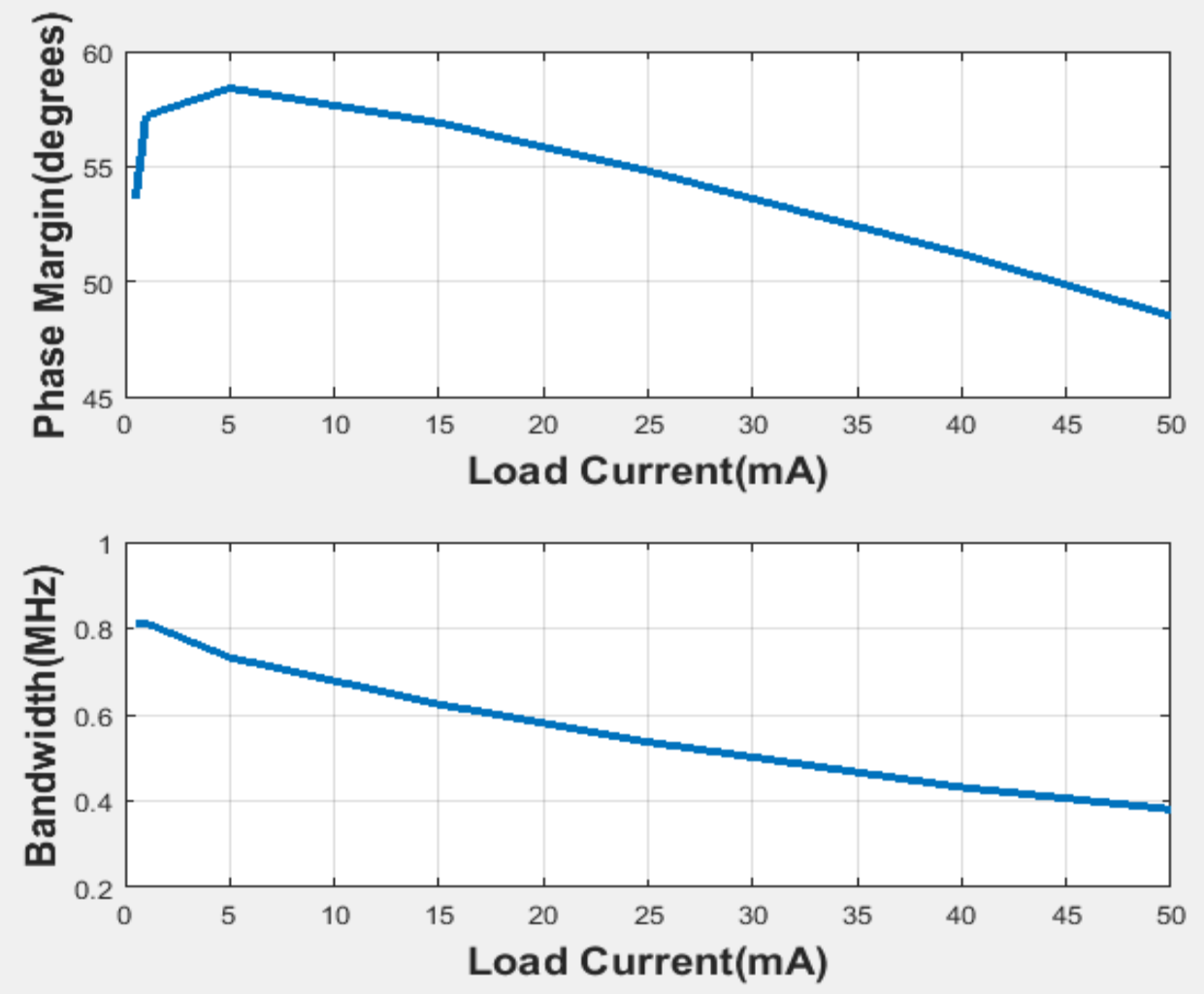

Figure 16: Phase margin and bandwidth summary

4. Circuit Implementations of LDO

From system-level and behavioral model analysis, all components' parameters are found and the next step is transistor-level circuit implementation of each building block. In this chapter, detailed circuits schematics are shown in accordance with the previous chapter.

VCO

Since the LDO must work for a supply voltage from 0.6 V to 1 V, the loop dynamics should remain as unchanged as possible. It turned out that VCO could be the most susceptible block to supply voltage variation. Traditional CMOS inverter based ring oscillator's frequency is directly proportional to supply voltage, which modifies the on-current of each delay cell. Therefore, a supply voltage immune VCO is needed.

The proposed VCO schematic is shown in Fig. 17. Its charging and discharging current are set by the current mirror, which is composed of two high-threshold voltage (HVT) PMOS transistors. The reason to use HVT devices is that their output resistance is much higher than those of regular-threshold or low-threshold devices, thus providing more shielding from supply voltage variations. The VCO has seven delay cells and each delay cell's schematic is shown in the dashed box. It is basically just a standard CMOS inverter with a tuned time-constant load. The NMOS that is controlled by the control voltage acts as a resistor, and is connected in series with a capacitor. Intuitively, when v_c

is zero, the NMOS is cut off and therefore the effective capacitance seen by each inverter is just the intrinsic capacitance of its own and the extrinsic capacitance of the following delay cell. When v_c is high, the NMOS acts as a wire, and the effective capacitance is intrinsic and extrinsic capacitances plus the added capacitance. The advantage of this topology is that the VCO can oscillate with whatever value the control voltage takes. However, it needs a buffer to convert the output signal to full swing, which burns additional power.

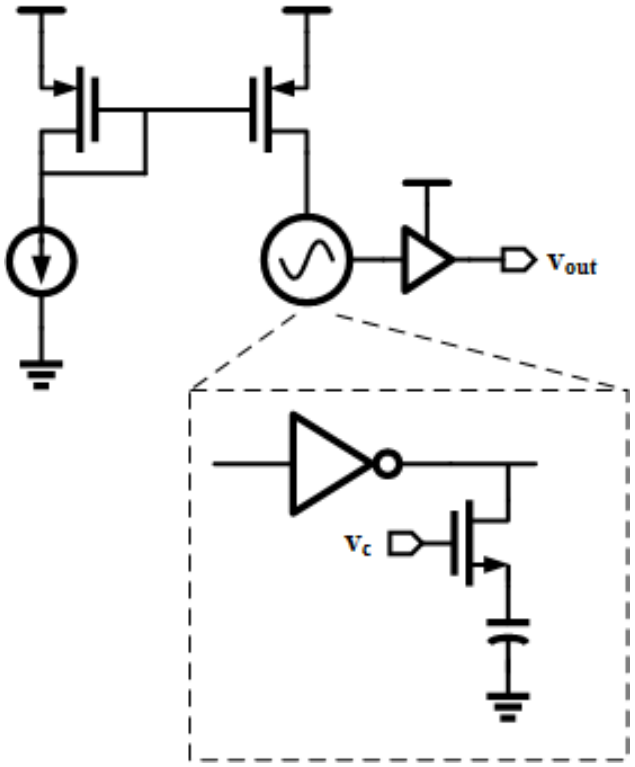

Figure 17: VCO circuit schematic

The simulated frequency vs. control voltage plots under 0.6 V and 1 V supply voltages are shown in Figs. 18 and 19. It can be seen that $K_{VCO} \approx 15.8$ MHz/V and is nearly constant for a wide range of v_c.

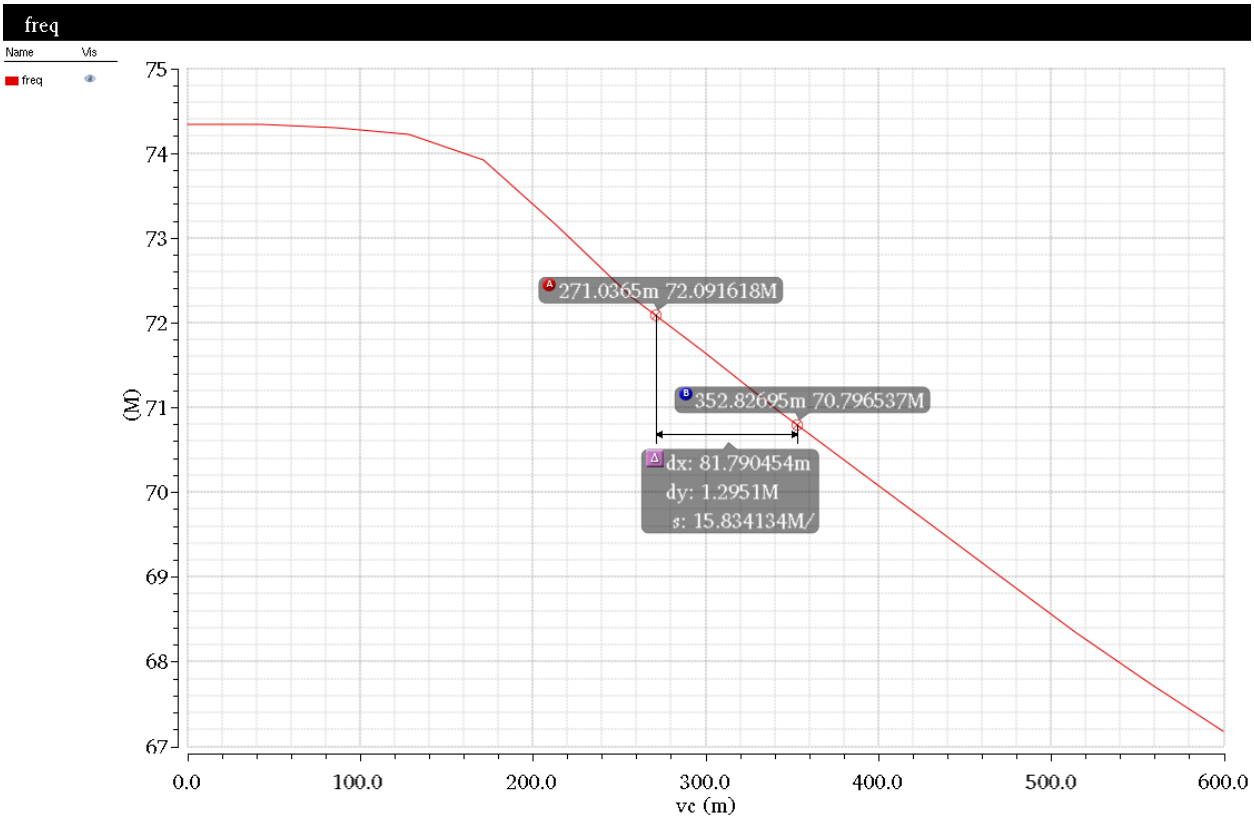

Figure 18: K_{VCO} simulation under 0.6 V supply

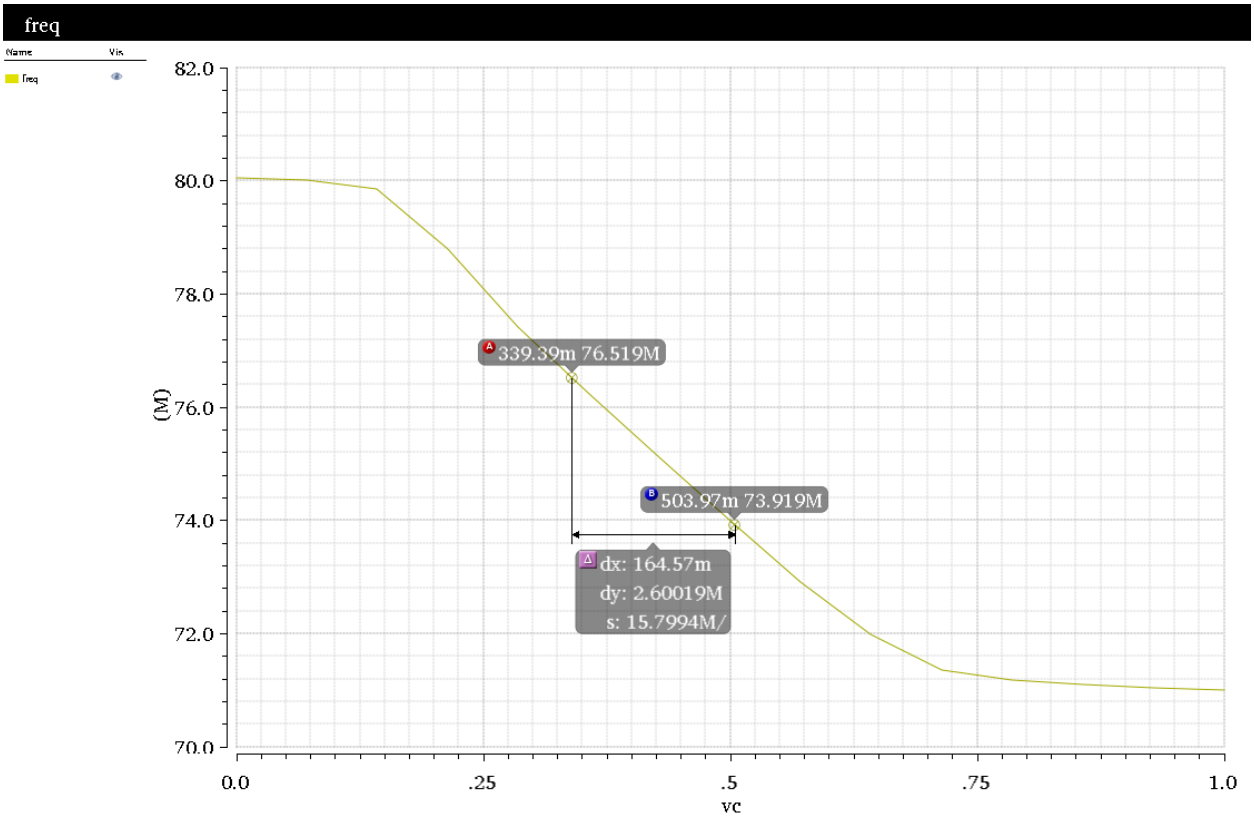

Figure 19: K_{VCO} simulation under 1 V supply

PFD

The typical implementation of a PFD is by using two D flip-flops and an AND gate, as shown in Fig. 20.

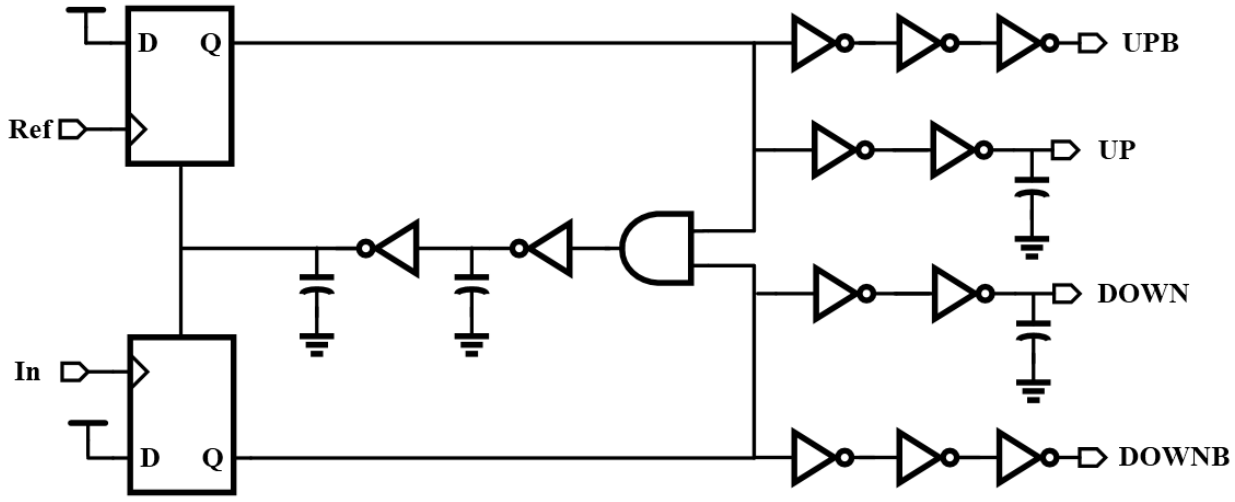

Figure 20: PFD circuit schematic

The four output signals—UP and DOWN and their complements—enable the positive and negative current source of CP, respectively. The added capacitor at UP and DOWN is to make sure that the delays from the D flip-flop to UP and UPB (and DOWN and DOWNB) are the same. Note that the AND gate is followed by two inverters with added capacitors to increase delay in the reset path. This reset delay is actually desired. The reason is that any CP cannot turn on for a small period of time, also called "deadzone". This is because of the finite rise and fall time that is caused by parasitic

capacitances at each node [5]. If this happens, the loop gain will drop to zero and the loop will not lock. In addition, the VCO can accumulate as much jitter as it can during that period until the charge pump turns back on.

To eliminate the deadzone, researchers introduce an intentional reset delay at the PFD such that both UP and DOWN current sources are on for a period of time greater than the deadzone period. Then the charge pump can quickly switch to other states.

CP

There are many possible implementations of charge pump, including drain switched, source switched, gate switched, etc. While these topologies do not have static current (except bias current) in steady state, each parasitic cap will be charged/discharged fully for each cycle, resulting to charge sharing, clock feedthrough, or long settling time. Therefore, they are not suited for this application. As shown in Fig. 21, a current-switched charge pump is used [6]. Although it has static current consumption in steady state, it provides high-speed operation and reduces clock feedthrough. Its nominal output value is chosen to be 10 μA.

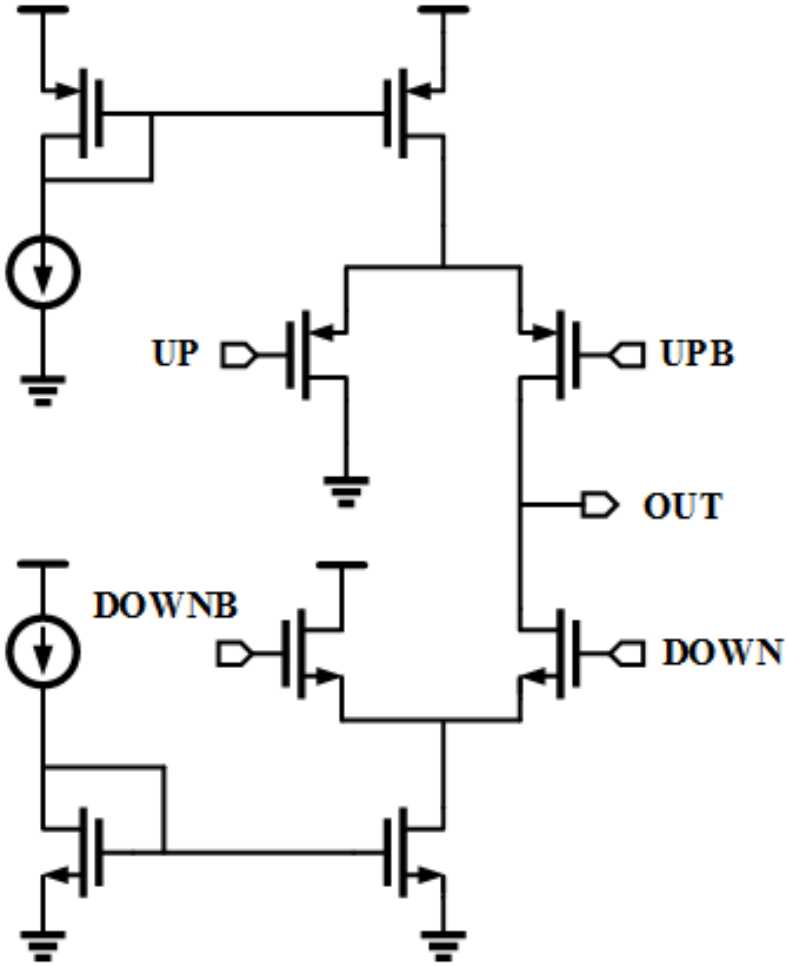

Figure 21: CP circuit schematic

LF

Ideally, an LF should act as a PI controller. It can be easily implemented using series resistor and capacitor as shown in Fig. 22 since the input signal is in current domain.

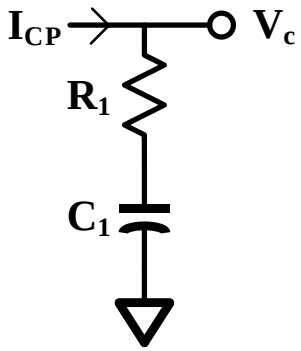

Figure 22: LF that realizes PI control

There is a potential problem, however, given that there will always be some mismatch from the CP. In steady-state, the mismatch current will flow into the LF and thus create a voltage spur (also called reference spur)

$$\Delta v = \Delta i_{CP} * R$$

In a CP-PLL, a common technique to reduce the reference spur is to add a bypass capacitor C_2 as shown in Fig. 23.

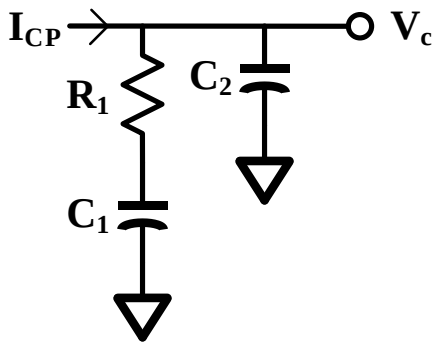

Figure 23: LF circuit schematic

The magnitude of C_2 should be relatively small compared with C_1 in order to sustain the phase margin. However, for better ripple suppression it might be desired to increase C_2, leading to a stability vs. ripple tradeoff. Nevertheless, the ripple will be suppressed by the loop dynamics because it appears every reference cycle and the loop bandwidth is typically much smaller than the reference. The nominal ratio of C_2/C_1 is around 10.

In this design, the capacitor C_2 is simply the effective gate capacitance C_{gg} of the pass transistor and its value is around 2-2.5 pF depending on the gate voltage range that is needed to support the output current. Based on this, R_1 is chosen to be 20 kΩ and C_1 is chosen to be 30 pF.

Transient Accelerator

Another practical issue that cannot be predicted in the previous loop dynamics analysis is the large-signal transient response. When the LDO switches from the lightest load to full load, the change is not small signal anymore and therefore the settling time will be much longer. Furthermore, the output voltage drop due to full load transient will be very big, which is extremely undesired. To improve the settling time and voltage drop, a transient accelerator is proposed.

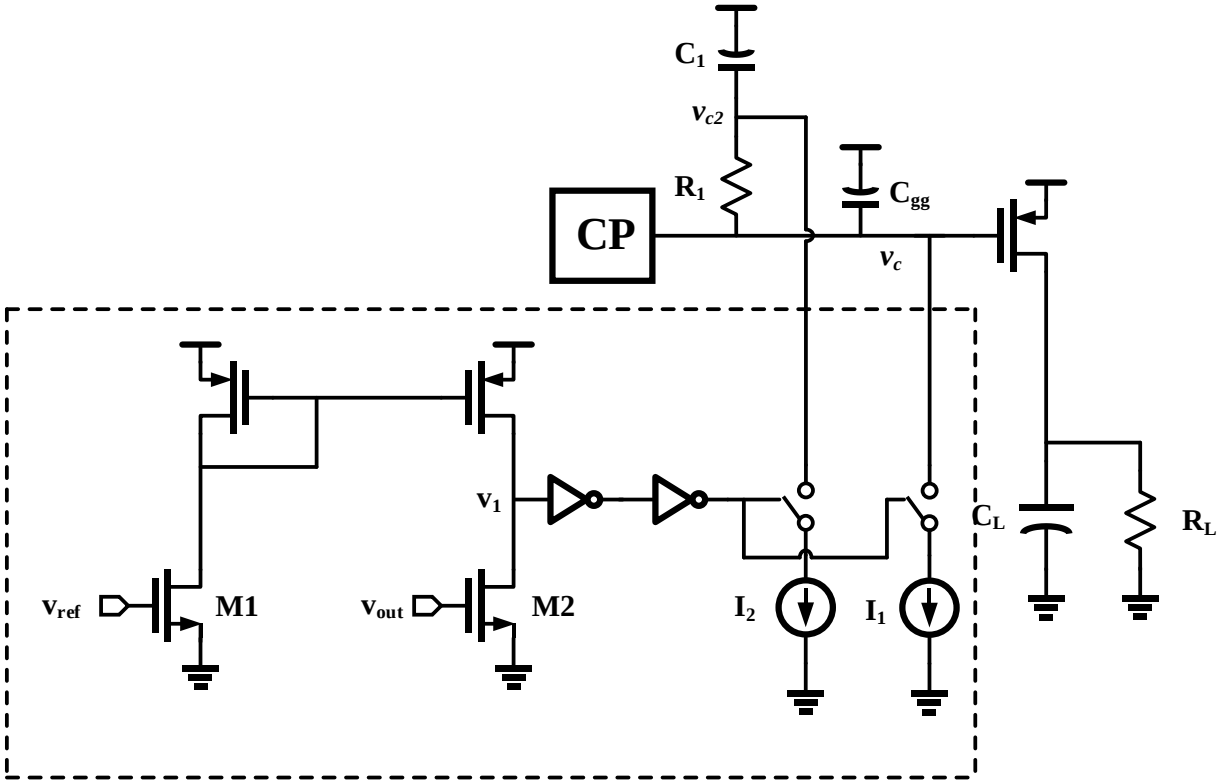

Figure 24: Transient accelerator schematic

As shown in Fig. 24, the transient accelerator is shown in the dashed box. It is essentially a current comparator formed by M1 and M2. M1 and M2 both generate some currents based on v_{ref} and v_{out}, and the generated currents are compared through the top PMOS current mirror. As a result, the intermediate node voltage v_1 will be either pulled up to the supply voltage or pulled down to the ground. In steady-state, the output voltage is always greater than the reference voltage because only part of the output voltage is compared with the reference. Therefore, v_1 is always ground.

When load transient happens, the output voltage will suddenly drop at a rate of $\frac{I_{out}}{C_L}$ and when it becomes less than v_{ref}, the node voltage v_1 will be pulled up to VDD, turning on the current sources I_1 and I_2. Then the voltages v_c and v_{c2} will be quickly discharged, letting the pass device enter proper operation state faster. Once v_{out} is greater than v_{ref}, transient accelerator will be disabled and small signal loop analysis will apply.

5. Simulation Results

In this chapter, simulation results from Cadence Spectre are presented and summarized. Figures 25 and 26 show the load transient from 0.5 mA to 50 mA. Without transient accelerator, the settling time under 0.6 V supply is 5.42 µs and is 4.59 µs under 1 V supply. The voltage drops are very big, more than 40 0mV. With transient accelerator, the settling time is only 1.58 µs and the voltage drop is only 91 mV (the output current changes with an edge time of 300 ns), as shown in Fig. 27.

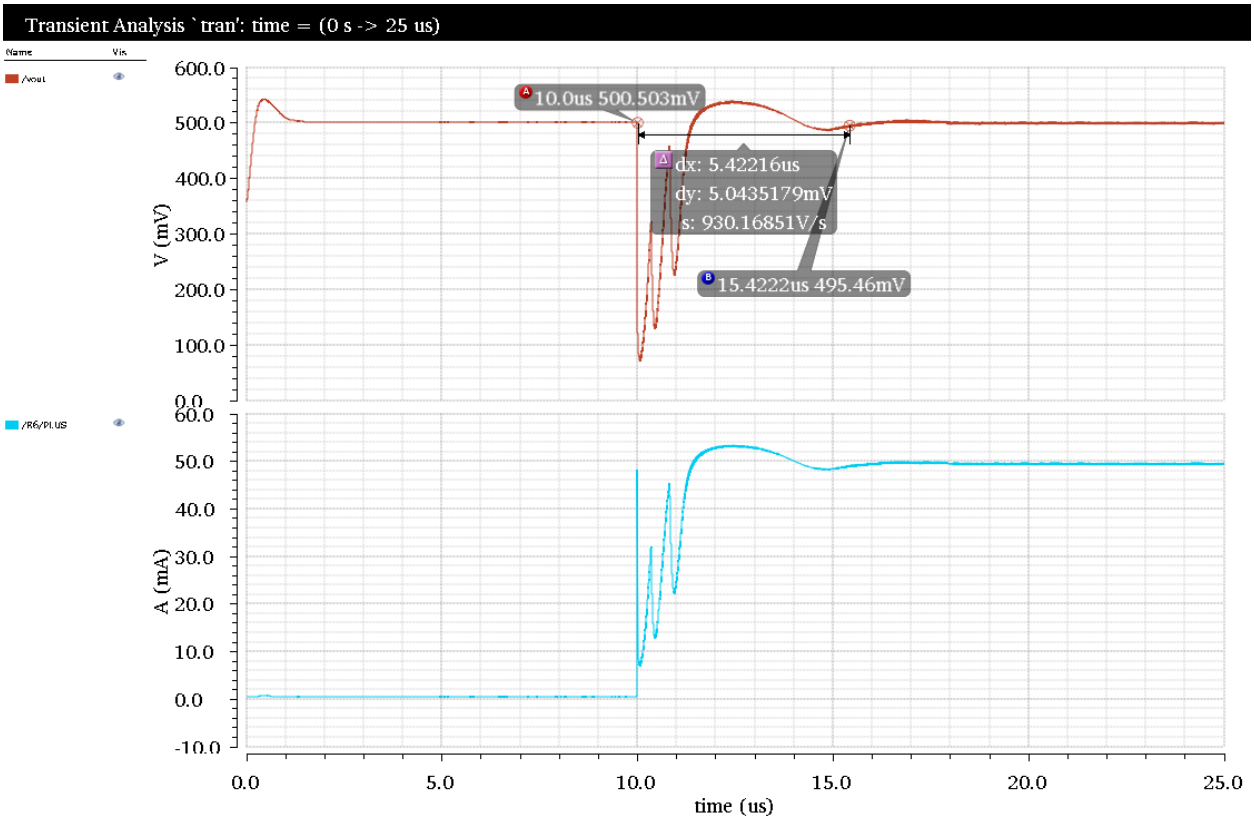

Figure 25: Load transient with 0.6 V supply

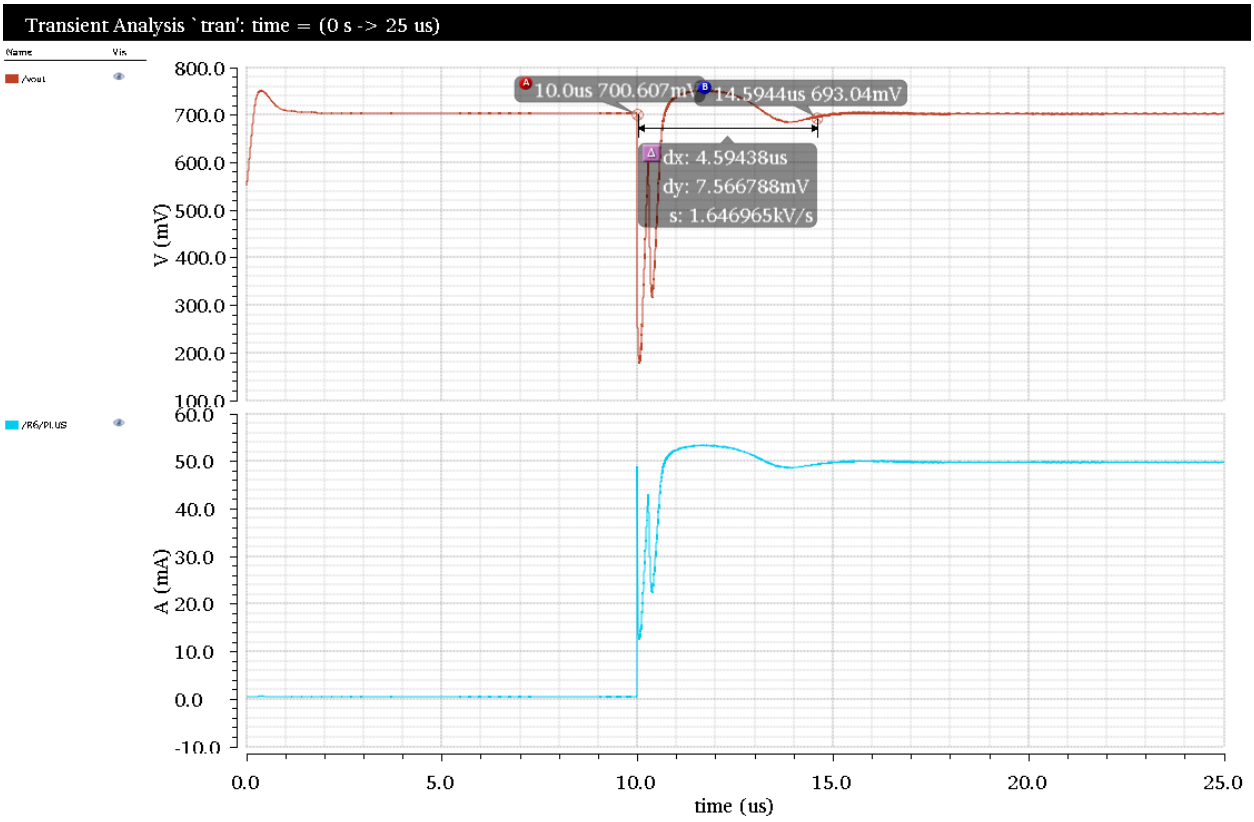

Figure 26: Load transient with 1 V supply

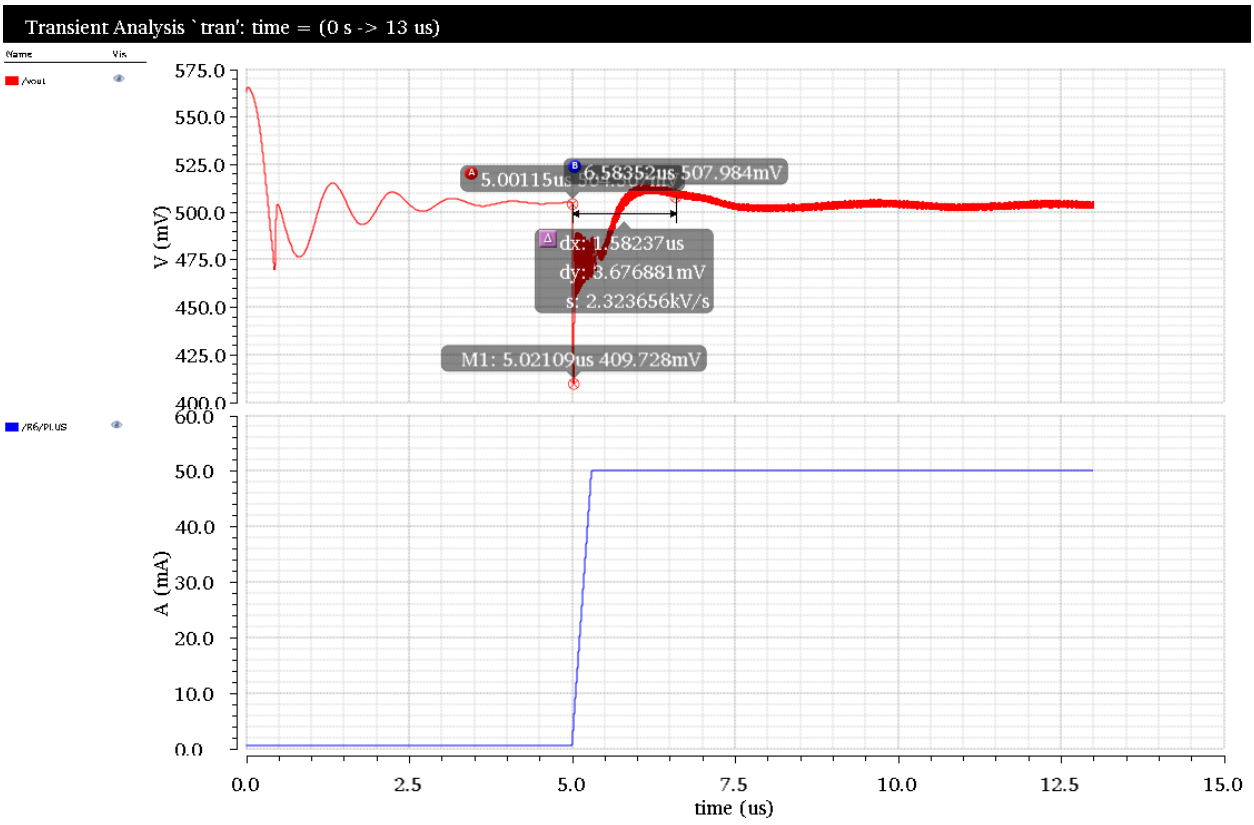

Figure 27: Load transient with transient accelerator and 0.6 V supply

There is a circumstance under which a low-voltage LDO will be used to output 0.5 V while under 1 V supply. Figure 28 shows the transient response under this condition. The loop is stable and the settling time is 1.855 µs, even better than before.

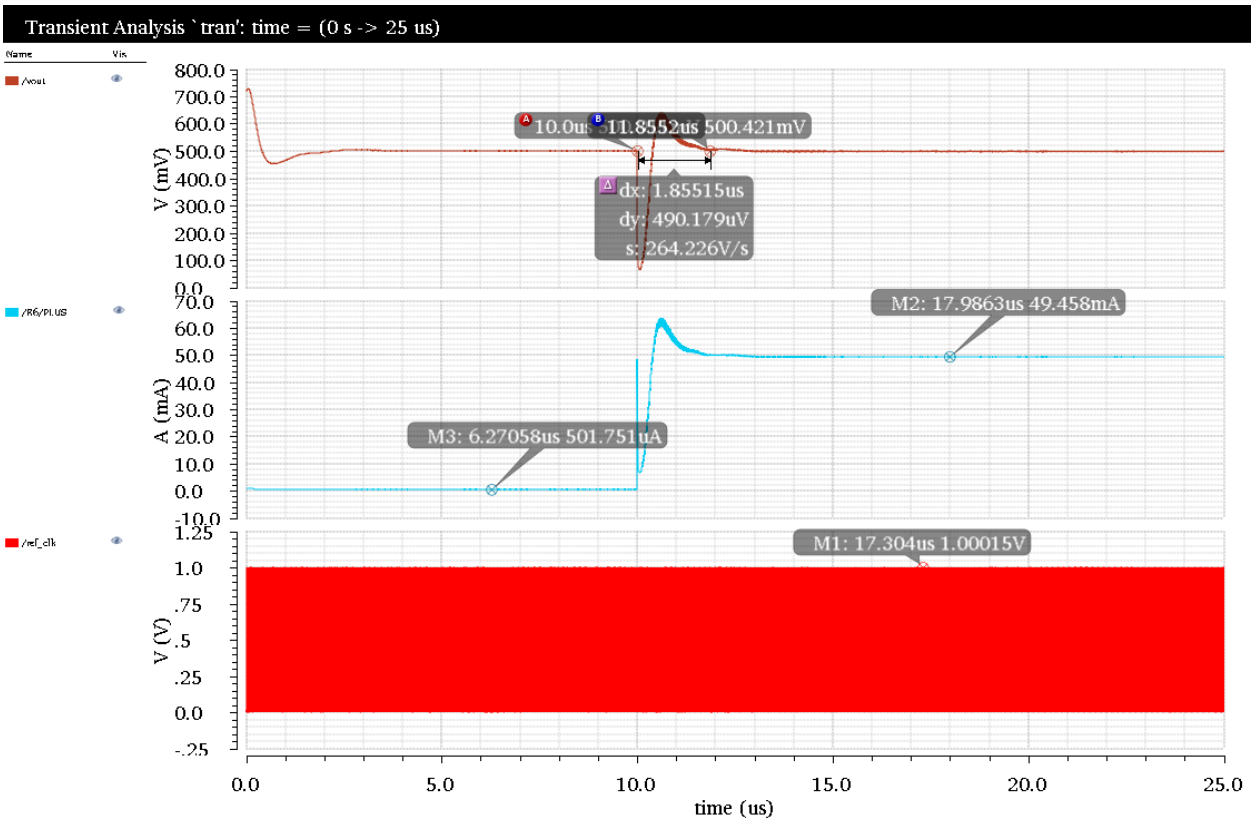

Figure 28: Load transient with 1 V supply and 0.5 V output

Lastly, steady state phase offset and voltage ripple under full load and 0.6 V / 1 V supply are shown in Figs. 29-32. The static phase offsets are 13.2% and 8.46% and the output voltage ripples are 4.06 mV and 4.33 mV.

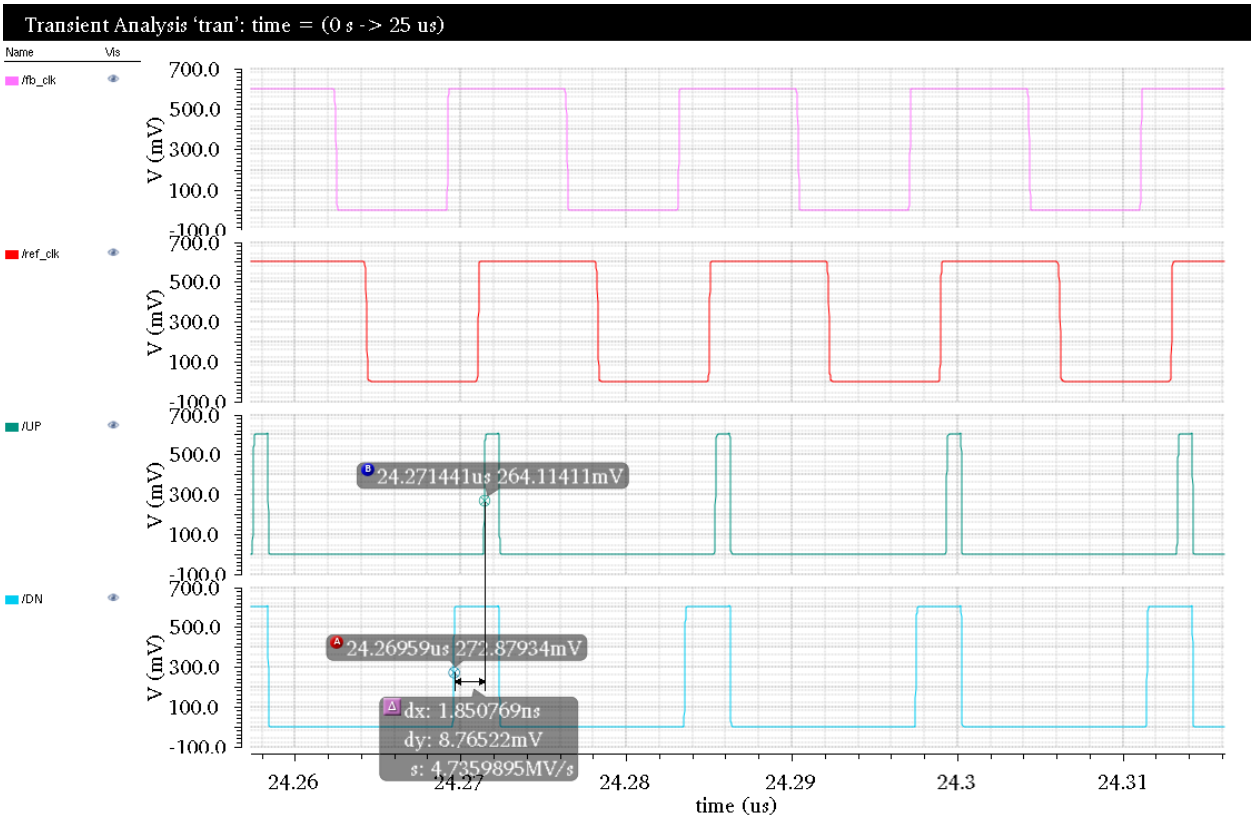

Figure 29: Steady-state phase offset with 0.6 V supply

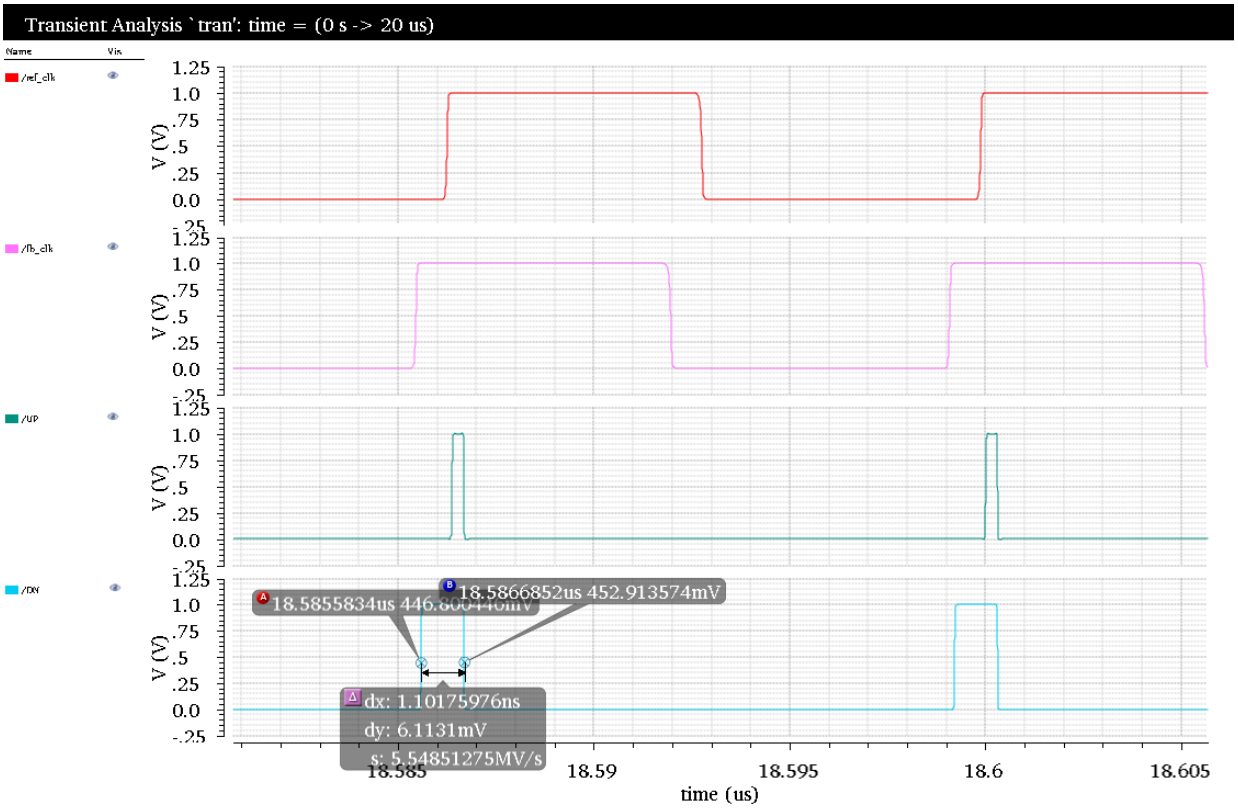

Figure 30: Steady-state phase offset with 1 V supply

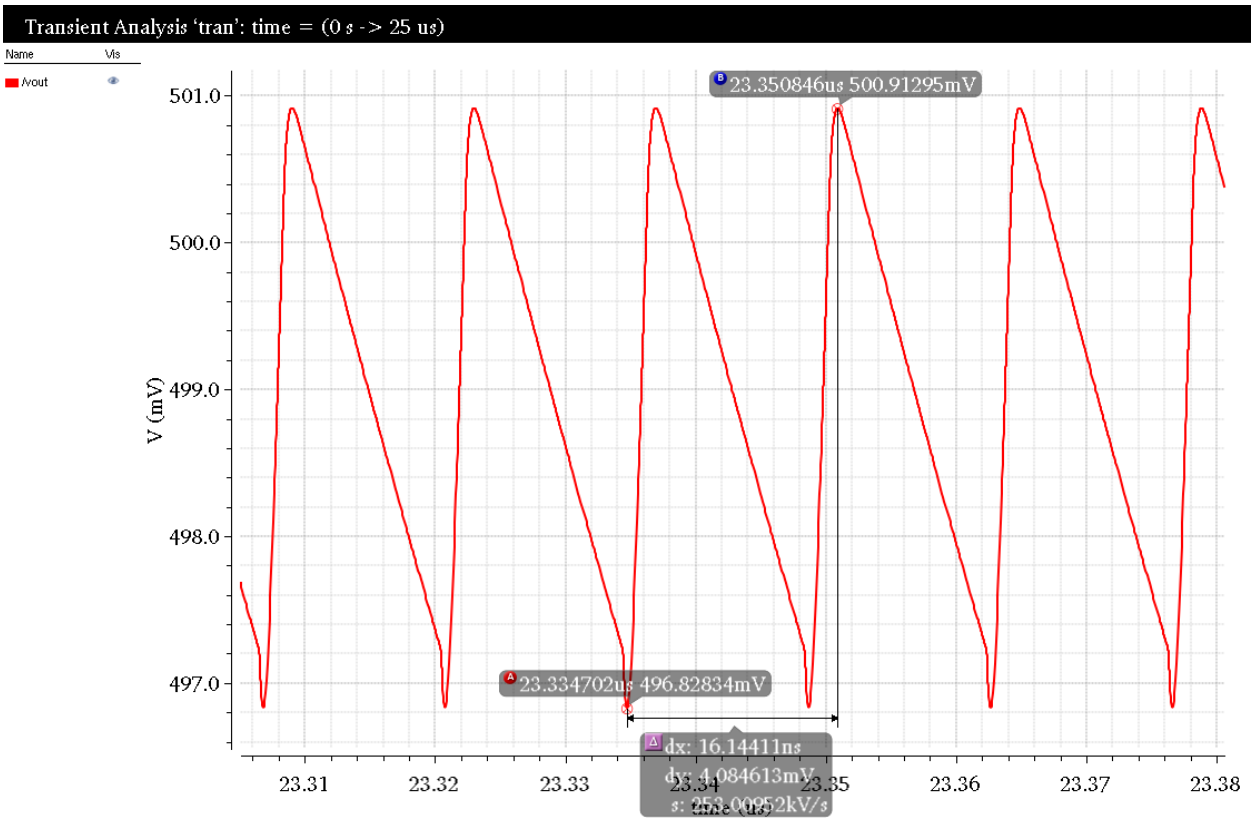

Figure 31: Output voltage ripple with 0.6 V supply

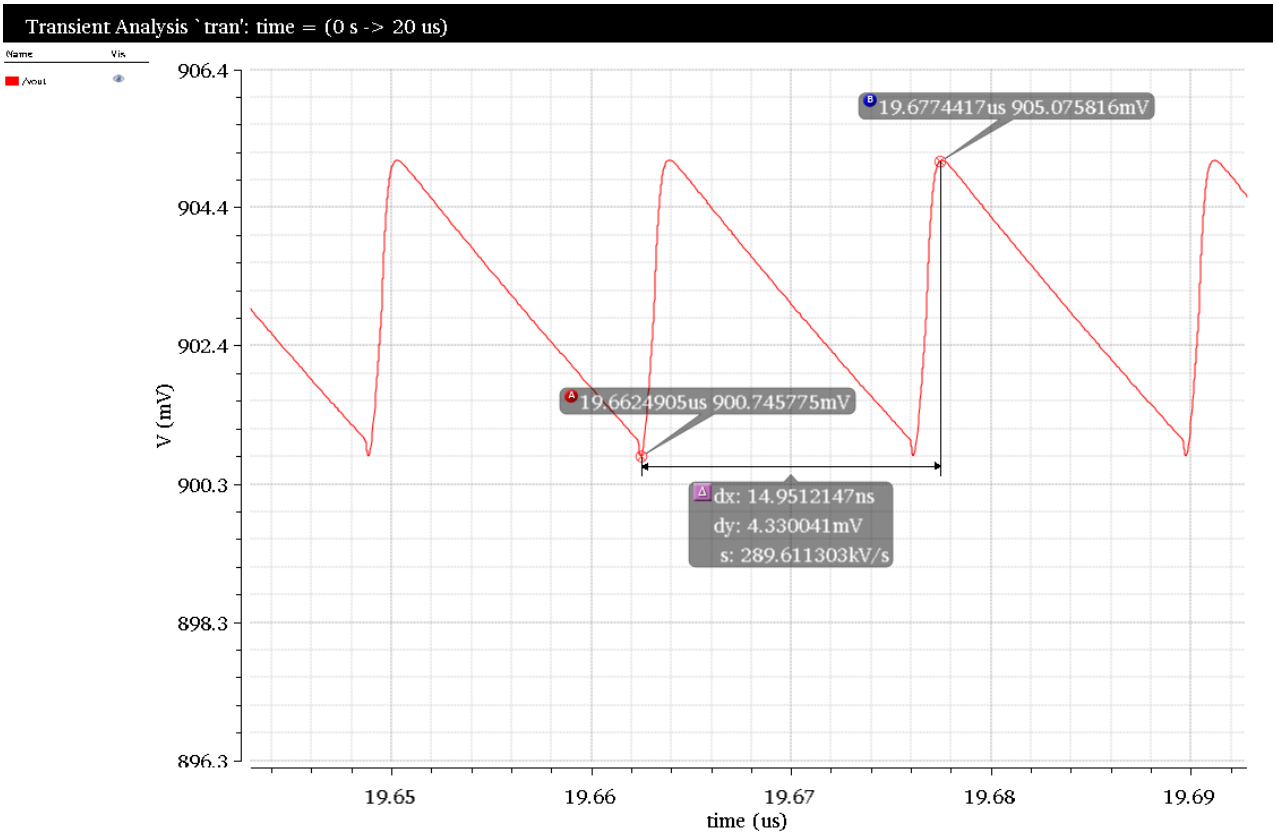

Figure 32: Output voltage ripple with 1 V supply

The power consumption is summarized in Table 3. At full load and 0.6 V supply, the total quiescent current is 97.05 µA. Therefore the maximum current efficiency is 99.98%.

Table 3: Quiescent current summary

PFD	**10.49 µA**
CP	27.06 µA
VCO	59.5 µA
Total	97.05 µA

6. Future Work

6.1 Layout

Due to time limitations, the LDO project is only based on schematic simulation. Any real integrated circuit chip, though, has to go through post-layout simulations. Performance variations between schematic and layout could be significant due to parasitics and signal routing.

6.2 Process, Temperature Variations and Mismatch

There are three main uncertainties for any circuit: process, voltage and temperature (PVT) variations. This LDO is designed to operate under a wide range of voltage so it is immune to voltage variation. However, process and temperature could make the LDO fail under some extremes. Offset due to mismatch between two components can make this happen too. For example, the mismatch between the two VCOs might create a frequency/phase offset that is beyond the acquisition range of the loop. More rigorous simulations (e.g. Monte Carlo) should be performed in order to ensure the proper functionality of the LDO.

7. Conclusion

In this thesis, a novel design of LDO using time-based control is discussed. The LDO achieves low -oltage operation, high current efficiency as well as large output current at the same time.

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