TOWARD REALIZING POWER SCALABLE AND ENERGY PROPORTIONAL HIGH-SPEED WIRELINE LINKS

BY

TEJASVI ANAND

DISSERTATION

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Doctoral Committee:

Associate Professor Pavan Kumar Hanumolu, Chair
Associate Professor Rakesh Kumar
Professor Elyse Rosenbaum
Professor Naresh R. Shanbhag

ABSTRACT

Growing computational demand and proliferation of cloud computing has placed high-speed serial links at the center stage. Due to saturating energy efficiency improvements over the last five years, increasing the data throughput comes at the cost of power consumption. Conventionally, serial link power can be reduced by optimizing individual building blocks such as output drivers, receiver, or clock generation and distribution. However, this approach yields very limited efficiency improvement. This dissertation takes an alternative approach toward reducing the serial link power. Instead of optimizing the power of individual building blocks, power of the entire serial link is reduced by exploiting serial link usage by the applications.

It has been demonstrated that serial links in servers are underutilized. On average, they are used only 15% of the time, i.e. these links are idle for approximately 85% of the time. Conventional links consume power during idle periods to maintain synchronization between the transmitter and the receiver. However, by powering-off the link when idle and powering it back when needed, power consumption of the serial link can be scaled proportionally to its utilization. This approach of rapid power state transitioning is known as the rapid-on/off approach. For the rapid-on/off to be effective, ideally the power-on time, off-state power, and power state transition energy must all be close to zero. However, in practice, it is very difficult to achieve these ideal conditions. Work presented in this dissertation addresses these challenges.

When this research work was started (2011-12), there were only a couple of research papers available in the area of rapid-on/off links. Systematic study or design of a rapid power state transitioning in serial links was not available in the literature. Since rapid-on/off with nanoseconds granularity is not a standard in any wireline communication, even the popular test equipment does not support testing any such feature, neither any formal measurement

methodology was available. All these circumstances made the beginning difficult. However, these challenges provided a unique opportunity to explore new architectural techniques and identify trade-offs. The key contributions of this dissertation are as follows.

The first and foremost contribution is understanding the underlying limitations of saturating energy efficiency improvements in serial links and why there is a compelling need to find alternative ways to reduce the serial link power.

The second contribution is to identify potential power saving techniques and evaluate the challenges they pose and the opportunities they present.

The third contribution is the design of a 5Gb/s transmitter with a rapid-on/off feature. The transmitter achieves rapid-on/off capability in voltage mode output driver by using a fast-digital regulator, and in the clock multiplier by accurate frequency pre-setting and periodic reference insertion. To ease timing requirements, an improved edge replacement logic circuit for the clock multiplier is proposed. Mathematical modeling of power-on time as a function of various circuit parameters is also discussed. The proposed transmitter demonstrates energy proportional operation over wide variations of link utilization, and is, therefore, suitable for energy efficient links. Fabricated in 90nm CMOS technology, the voltage mode driver, and the clock multiplier achieve power-on-time of only 2ns and 10ns, respectively. This dissertation highlights key trade-off in the clock multiplier architecture, to achieve fast power-on-lock capability at the cost of jitter performance.

The fourth contribution is the design of a 7GHz rapid-on/off LC-PLL based clock multiplier. The phase locked loop (PLL) based multiplier was developed to overcome the limitations of the MDLL based approach. Proposed temperature compensated LC-PLL achieves power-on-lock in 1ns.

The fifth and biggest contribution of this dissertation is the design of a 7Gb/s embedded clock transceiver, which achieves rapid-on/off capability in LC-PLL, current-mode transmitter and receiver. It was the first reported design of a complete transceiver, with an embedded clock architecture, having rapid-on/off capability. Background phase calibration technique in PLL and CDR phase calibration logic in the receiver enable instantaneous lock on power-on. The proposed transceiver demonstrates power scalability with a wide range of link utilization and, therefore, helps in improving overall system efficiency. Fabricated in 65nm CMOS

technology, the 7Gb/s transceiver achieves power-on-lock in less than 20ns. The transceiver achieves power scaling by 44x (63.7mW-to-1.43mW) and energy efficiency degradation by only 2.2x (9.1pJ/bit-to-20.5pJ/bit), when the effective data rate (link utilization) changes by 100x (7Gb/s-to-70Mb/s).

The sixth and final contribution is the design of a temperature sensor to compensate the frequency drifts due to temperature variations, during long power-off periods, in the fast power-on-lock LC-PLL. The proposed self-referenced VCO-based temperature sensor is designed with all digital logic gates and achieves low supply sensitivity. This sensor is suitable for integration in processor and DRAM environments. The proposed sensor works on the principle of directly converting temperature information to frequency and finally to digital bits. A novel sensing technique is proposed in which temperature information is acquired by creating a threshold voltage difference between the transistors used in the oscillators. Reduced supply sensitivity is achieved by employing junction capacitance, and the overhead of voltage regulators and an external ideal reference frequency is avoided. The effect of VCO phase noise on the sensor resolution is mathematically evaluated. Fabricated in the 65nm CMOS process, the prototype can operate with a supply ranging from 0.85V to 1.1V, and it achieves a supply sensitivity of 0.034^{o}C/mV and an inaccuracy of $\pm$0.9^{o}C and $\pm$2.3^{o}C from 0-100^{o}C after 2-point calibration, with and without static nonlinearity correction, respectively. It achieves a resolution of 0.3^{o}C, resolution FoM of 0.3(nJ/conv)res^2, and measurement (conversion) time of 6.5μs.

To my parents and almighty God, for their love and support.

ॐ भूर्भुवः स्वः तत्सवितुर्वरेन्यं । भर्गो देवस्य धीमहि, धीयो यो नः प्रचोदयात् ॥

Oh God! Thou art the Giver of Life,
Remover of pain and sorrow,
The Bestower of happiness,
Oh! Creator of the Universe,
May we receive thy supreme sin-destroying light,
May Thou guide our intellect in the right direction.

Gayatri Mantra

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TABLE OF CONTENTS

CHAPTER 1 MOTIVATION 1
1.1 Why Serial Link Power Consumption Is a Matter of Concern 3
1.2 Power Reduction Methodology 6

CHAPTER 2 POWER SCALING AND ENERGY PROPORTIONAL OPERATION TECHNIQUES 9
2.1 Serial Link Architecture and Simulation Model 11
2.2 Serial Link Power Scaling with DVFS 13
2.3 Serial Link Power Scaling with Rapid-On/Off 15
2.4 DVFS versus Rapid-On/Off 20
2.5 Conclusion 21

CHAPTER 3 A 5Gb/s TRANSMITTER FOR ENERGY PROPORTIONAL LINKS (EPL) 22
3.1 Limitations of Conventional Transmitter for Rapid-On/Off Links 23
3.2 Proposed Fast Power-On Transmitter Architecture 25
3.3 Power-On Transient Modeling of MDLL 31
3.4 Clock Multiplier Building Blocks 35
3.5 Measurement Results 40
3.6 Conclusion 50

CHAPTER 4 A 7GHz FAST POWER-ON-LOCK PLL FOR ENERGY PROPORTIONAL LINKS 53
4.1 MDLL Limitations and Motivation for Fast Power-on-Lock LC-PLL 53
4.2 Fast Power-On LC-PLL Evolution 55
4.3 Complete PLL Architecture 59
4.4 PLL Building Blocks 62
4.5 PLL Modes and Power-On Sequence 65
4.6 Measurement Results 66
4.7 Conclusion 72

CHAPTER 5 A 7Gb/s EMBEDDED CLOCK TRANSCEIVER FOR ENERGY PROPORTIONAL LINKS 74
5.1 Transceiver Architecture 74
5.2 Transmitter 76

5.3 Receiver 78
5.4 Measurement Results 88
5.5 Conclusion 96

CHAPTER 6 A HIGHLY DIGITAL TEMPERATURE-TO-FREQUENCY-TO-DIGITAL BASED TEMPERATURE SENSOR 97
6.1 Temperature Sensor Concept 99
6.2 Making Sensor Less Sensitive to Supply Voltage Variations 102
6.3 Temperature Sensor Architecture 104
6.4 Effect of Phase Noise on Sensor Resolution 108
6.5 Measurement Results 111
6.6 Conclusion 117

CHAPTER 7 CONCLUSION 119

APPENDIX A LIST OF SERIAL LINK PAPERS SURVEYED 120

REFERENCES 126

CHAPTER 1

MOTIVATION

Low cost and reliable data communication is key in enabling technologies such as cloud computing, big-data, parallel processing, and video streaming applications. High-speed wireline communication is one of the most critical fabric in the present communication infrastructure. Electronic gadgets such as smartphones, tablets, laptops, servers and even smart watches contain several wireline links. Wireline links, also known as serial links, can be categorized into various standards, as shown in Table 1.1.

Table 1.1: Wireline Link Standard and Data Rates

Standard Name	**Data Rates**
DDR4	3.2Gb/s
MIPI-M PHY	5Gb/s
QPI	8Gb/s
USB 3.1	10Gb/s
PCIe 3.0	8Gb/s
HDMI 2.0	18Gb/s
IEEE 802.3bj	25Gb/s
InfiniBand	25Gb/s
...	...

An example of serial links present on a server motherboard, which forms a part of cloud infrastructure, is shown in Fig. 1.1. The motherboard has four processor slots, which can be identified as P1, P2, P3, and P4. An interface between a processor and a DRAM module is known as double data rate (DDR) interface. Processor-to-processor interface is known as QuickPath Interconnect (QPI) or HyperTransport (HT) interface, and it is often used in parallel processing. An interface between a processor and other peripherals is known

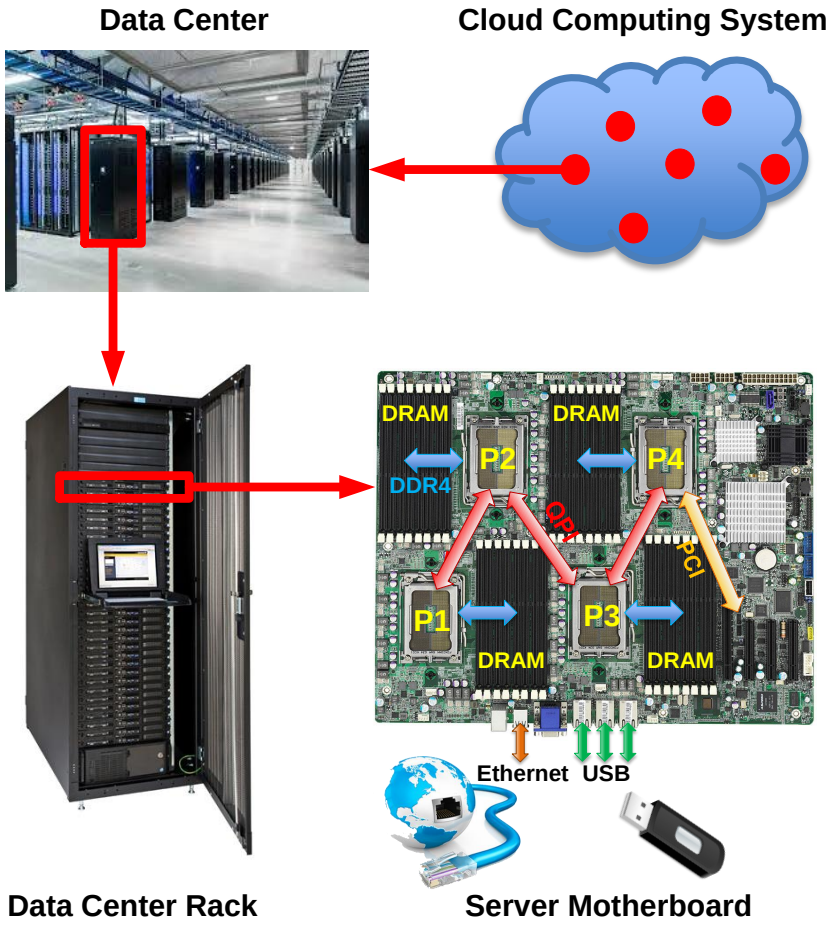


Figure 1.1: High-speed wireline links in a server motherboard and server as part of a cloud infrastructure.

as peripheral component interconnect (PCI), and a universal serial bus (USB) interface. Finally, an interface to router or switch is known as an Ethernet interface.

Basic building blocks of a serial link is shown in Fig. 1.2. It consists of three components, a transmitter, channel, and receiver. The transmitter includes a serializer and an output driver. The channel is made up of copper trace on FR4, twisted copper wire or a shielded cable. The receiver consists of a sampler and a deserializer. Channel loss results in inter-symbol interference (ISI), which closes the data eye at the receiver input. To compensate for the channel loss, equalization is provided in the receiver and sometimes on the transmitter end. As the channel length increases, for the same data rate, the loss also increases, and, therefore, more equalization is needed to compensate for the loss. Equalization increases

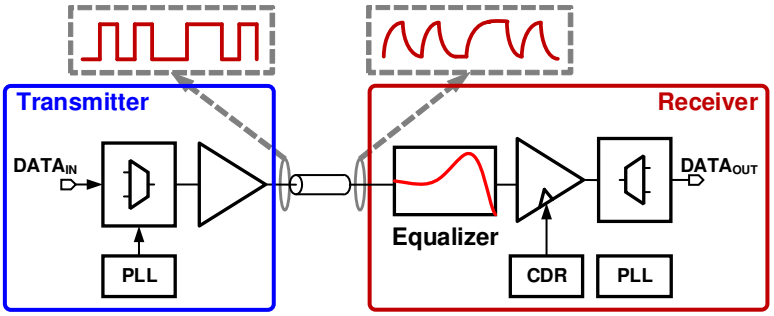


Figure 1.2: Architecture of a serial link.

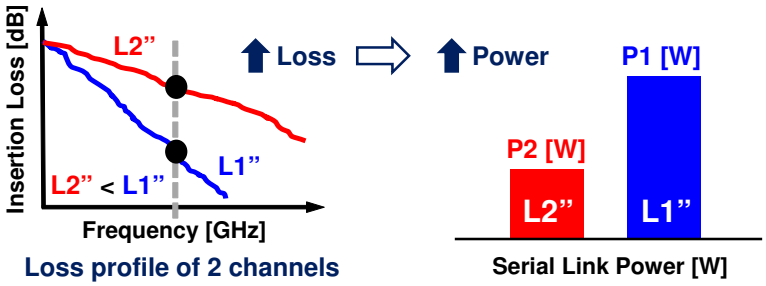


Figure 1.3: Effect of channel loss on power consumption.

the power consumption of serial links, as shown in Fig. 1.3. In server class processors, serial links today consume approximately 20% of power [1, 2]. Despite consuming only a fraction of processor power, serial link power consumption is becoming a matter of concern.

1.1 Why Serial Link Power Consumption Is a Matter of Concern

Growing appetite for high-performance computing has resulted in a consistent increase in the number of processing cores every year [3]. Consequently, this has resulted in an increase in the demand of off-chip I/O bandwidth. For example, IBM's Power-7 with eight cores has 4.7Tb/s off-chip bandwidth. While the IBM Power-8 with twelve cores has a 7.6Tb/s off-chip bandwidth [4]. The processor's package is typically constrained by the number of I/O pins, and, therefore, bandwidth demand is usually met by increasing the per-pin data rate or per-pin bandwidth, as shown in Fig. 1.4(a).[1] It can be observed that serial links are keeping up with the bandwidth demand. Figure 1.4(b) plots the energy-per-bit versus year

[1]The data plotted in Fig. 1.4(a), (b), (c) and (d) was collected from over 129 papers published in leading conferences. Details of the serial link data used in Fig. 1.4 are available in Appendix A.

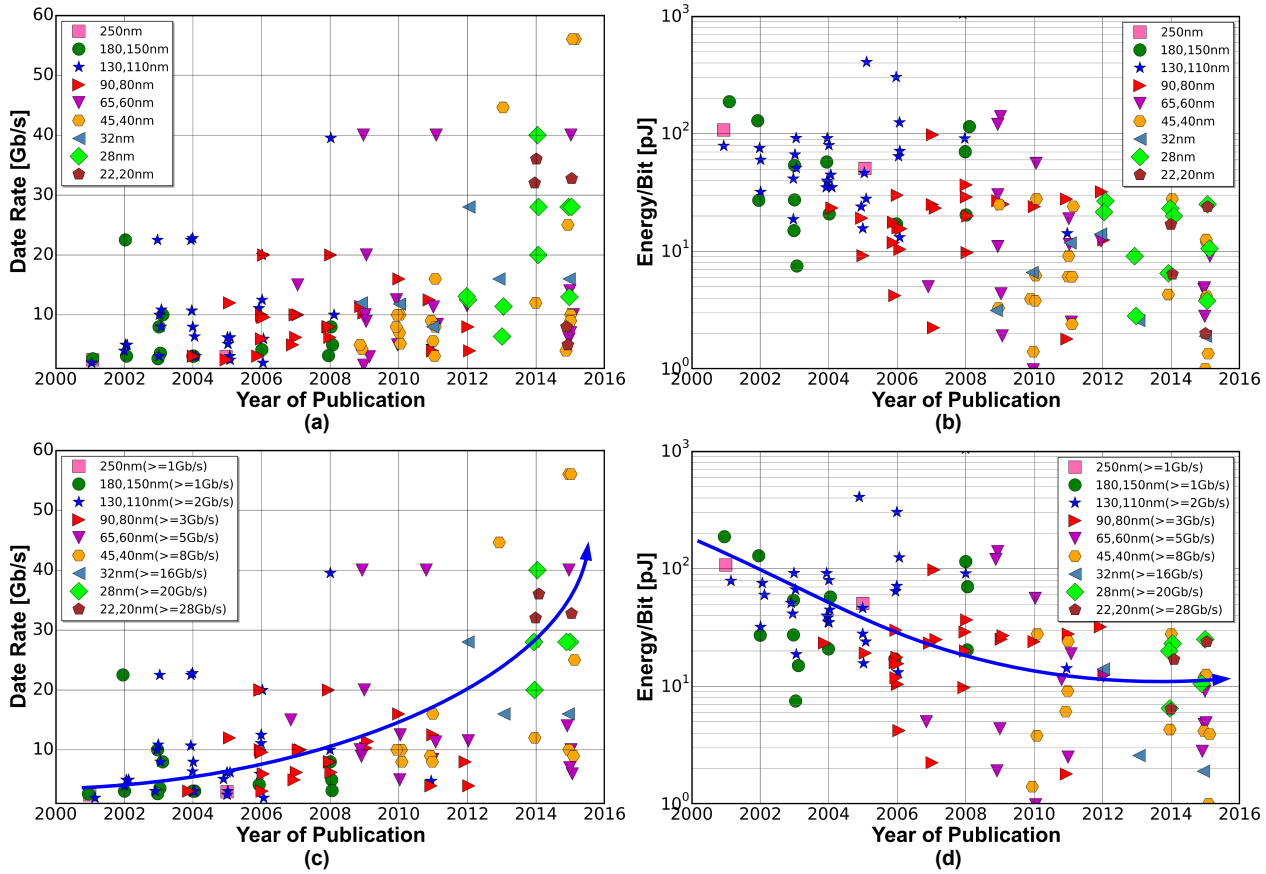


Figure 1.4: Serial link trends. (a) Data rate versus year of publication of off-chip links. (b) Energy efficiency versus year of publication. (c) Data rate versus year of publication filtered by the data rate for a given technology node. (d) Energy efficiency versus year of publication filtered by the data rate for a given technology node.

of publication. It can be observed that the energy efficiency improvement of these links has started to taper-off in recent years.

Voltage and process scaling have been the biggest contributors in improving energy efficiency over the last 15 years. However, as the supply voltage scaling has saturated in finer technology nodes, the energy efficiency improvement due to voltage scaling has diminished. Porting a serial link, which was designed at a fixed data rate, to a finer process node helps in improving energy efficiency. However, if the data rate requirement of a serial link increases while moving to a fine process node, then it can be observed from Fig. 1.4(d) that there is no net efficiency improvement beyond 65nm. This behavior is explained as follows: Over the last several years, the channel length of serial links has stayed more or less fixed. Channel

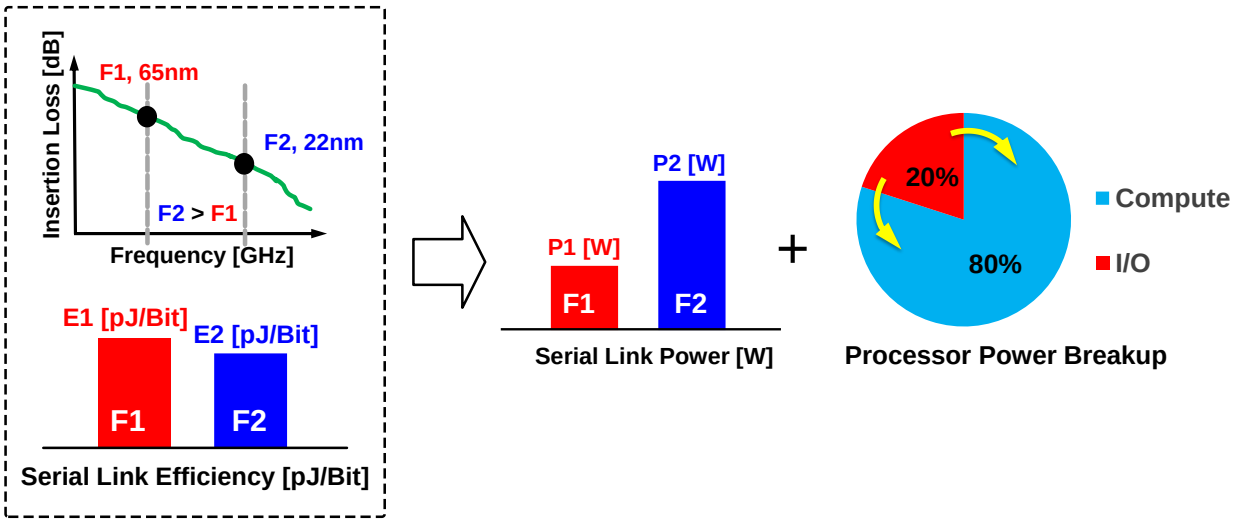


Figure 1.5: Reason for saturating energy efficiency in fine process nodes and its effect on the I/O power component in a processor.

lengths did not change because changing channels incurs a high cost, while the data rates continued to increase. This has resulted in increased channel loss at Nyquist frequencies, and consequently more equalization is required to offset the loss, which translates to increased power consumption. Therefore, energy efficiency improvements provided by process scaling is offset by the energy needed to compensate for channel loss. As a result, energy efficiency improvement in finer process nodes is not significant [5].

The combined effect of increasing bandwidth and saturating energy efficiency would eventually result in increased power consumption of serial links. Today, serial links consume approximately 20% of processor power, but if the above-mentioned trend continues, this portion will increase in the future, as shown in Fig. 1.5. The trend of increasing serial link power share is catalyzed by the fact that the logic power would continue to reduce with every new technology node until it hit the minimum power limits [6]. Once the logic power hits the minimum power limit or when the rate of power reduction in the logic core gets slower than the rate of increase in the serial links power, at that point, due to thermal constraints of the processor package, increasing serial link power could potentially constrain the power budget allocated for the computational cores. Consequently, increasing a processor's computational capacity in the future would be challenging, and serial link power will become the bottleneck. Therefore, a paradigm shift in reducing serial link power is needed.

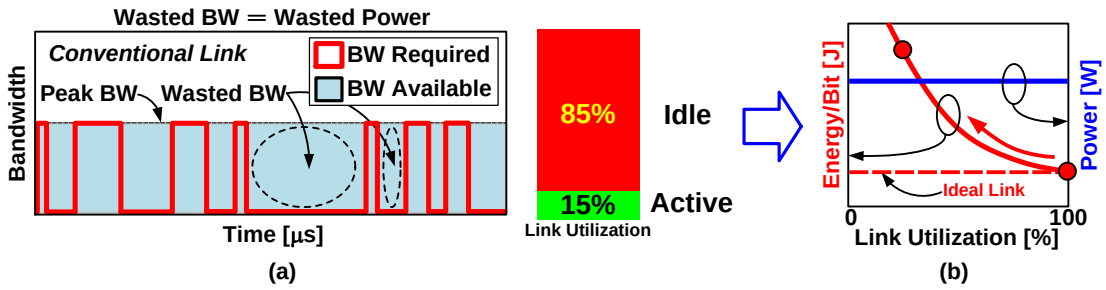


Figure 1.6: (a) Instantaneous bandwidth versus time in a conventional serial link. (b) Energy efficiency and power versus link utilization.

1.2 Power Reduction Methodology

Conventionally, both system and circuit designers have attempted to solve the power problem in their best possible ways. System designers optimize the design parameters such as data rate, the number of I/O lanes, communication medium, supply voltage, or the technology node used. Circuit designers optimize individual circuit blocks such as phase locked loop (PLL) power, or analog to digital converter's (ADC) figure of merit. The combined effort of both these groups results in a serial link system whose energy efficiency is optimized at its peak performance level. However, there is a problem with this design approach. This design approach fails to account for the usage pattern of applications that utilize these serial links.

In practical systems, serial links are only sporadically used. They are used whenever there is a miss in the last level of a cache, and then the processor fetches data from DRAM, or if there is a request to download a web page, and the request packet is sent to the server. Figure 1.6(a) shows the instantaneous bandwidth demand versus time in a conventional serial link. Even though almost peak bandwidth is available all the time, approximately 85% of the time, this bandwidth is not being used [7, 8]. This wastage of bandwidth, when the serial link is idle, results in idle power consumption. In a conventional serial link, this idle power is necessary to maintain synchronization between the transmitter and the receiver. Even if serial links are designed and optimized for the best energy efficiency at their peak performance level, due to idle power consumption, energy efficiency of links degrades as the link utilization is reduced, as shown in Fig. 1.6(b). Ideally, constant energy-per-bit across

all utilization levels is desirable.

One possible way to overcome drawbacks of a conventional design approach is to co-optimize both the system and circuit designs. Instead of optimizing links efficiency at their peak performance, the energy efficiency of serial links must be optimized at their average utilization levels. The focus of this dissertation is to develop circuit and system architectures that are optimized to leverage the usage pattern of applications in order to save power. A summary of research presented in this dissertation and its organization is illustrated in Fig. 1.7.

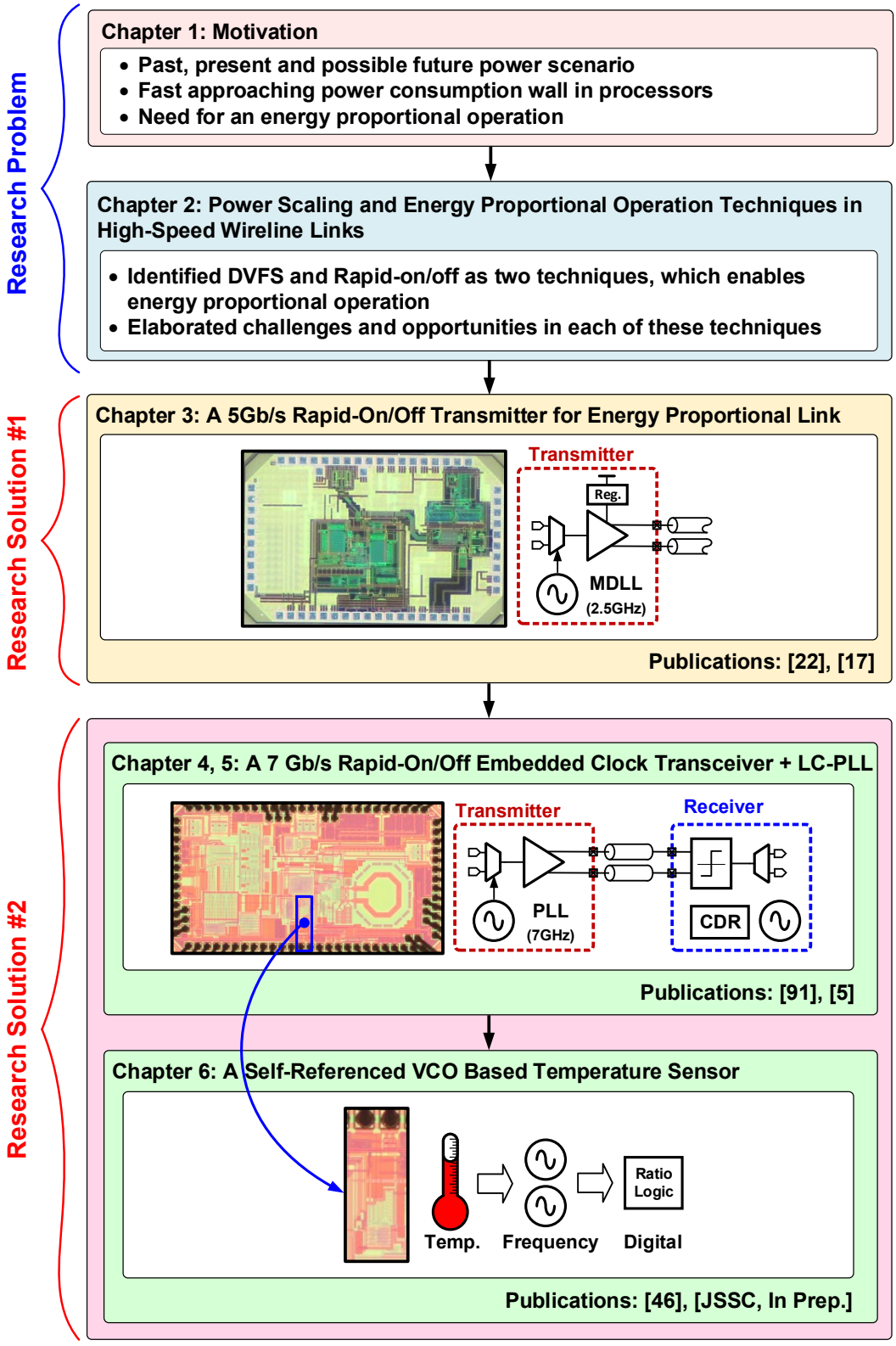


Figure 1.7: Research and organization summary of this dissertation.

CHAPTER 2

POWER SCALING AND ENERGY PROPORTIONAL OPERATION TECHNIQUES

In a system, serial links can be treated as a resource to accomplish either a computational or a processing task. In a practical scenario, these serial links are utilized sporadically by the applications that run on a processor. Therefore, instantaneous bandwidth demand (utilization) of the serial links varies over time. As shown in Fig. 2.1(a), when a conventional serial link is idle, it consumes idle power to maintain synchronization between transmitter and receiver. As a result, energy efficiency of such a link, as quantified by the energy-per-bit metric, degrades at lower link utilization levels.

The impact of degradation in energy efficiency is perceivable in data centers where approximately 7% of data center power is spent in off-chip serial links [1, 2, 9], which include both the memory and data networks. It is estimated that by 2016, data centers in North America are expected to consume approximately 13,250MW of power [10]. With an average server utilization of 15% [7], these data centers could potentially save 1,420MW as idle link power (assuming power usage effectiveness (PUE)[1] of 1.8). Using a nationwide average electricity rate of \$0.07/kWh for an industrial complex, this amounts to saving approximately \$870M annually.

By scaling the serial link power to match its utilization, idle power wastage could be eliminated. The elimination of wasted power will ensure that the link will maintain a constant energy-per-bit across all utilization levels. Such a mode of operation of the serial link is also known as the energy proportional operation [8]. Figure 2.2 shows the energy proportionality

[1]Power usage effectiveness (PUE) is a measure of how efficiently a data center uses energy.

$$PUE = \frac{Total\ Facility\ Energy}{IT\ Equipment\ Energy} \tag{2.1}$$

This ratio remains constant for a data center. For example, if IT equipment energy consumption increases, this results in overall increase in data center energy consumption by a factor of PUE.

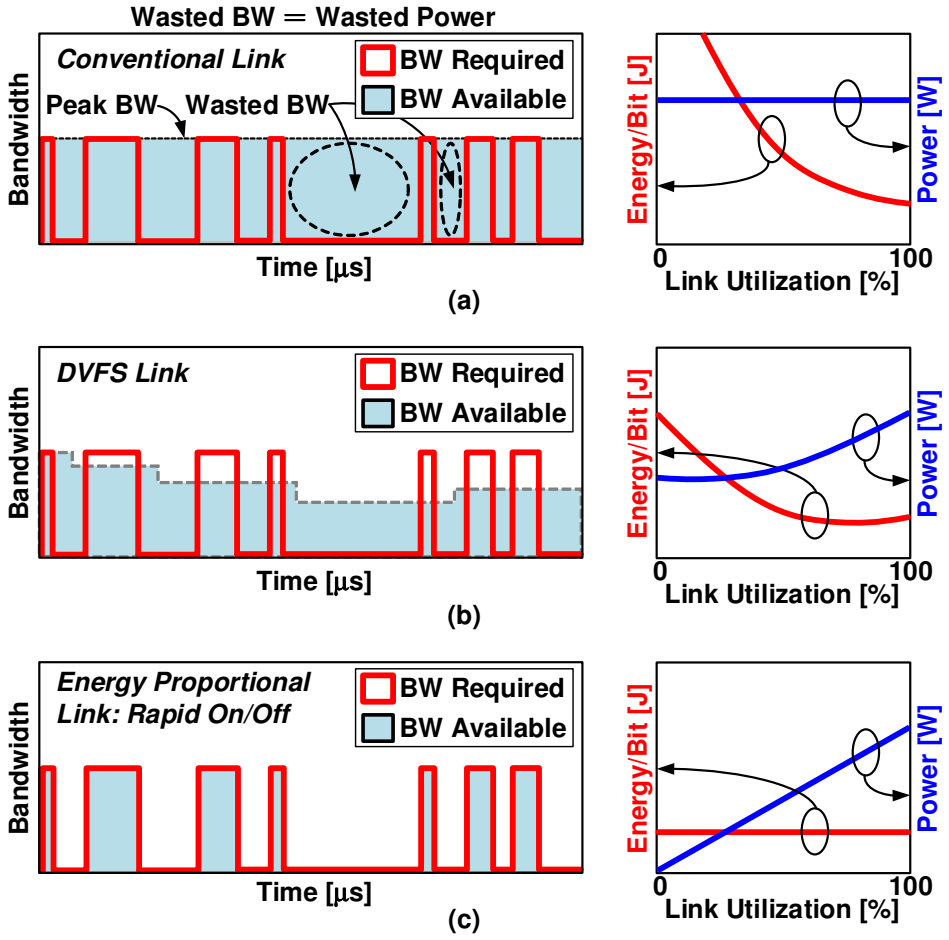


Figure 2.1: Instantaneous bandwidth versus time demand along with power consumption and energy-per-bit of (a) conventional serial link, (b) dynamic voltage and frequency scaling (DVFS) based link, and (c) rapid-on/off approach based link.

concept in serial links. If x amount of energy is required to transfer 1 bit of data across the channel, then to transfer 10bits, 10x energy would be needed, irrespective of link utilization, i.e., energy is proportional to the amount of data transmitted and is independent of link utilization.

Dynamic voltage and frequency scaling (DVFS) and rapid-on/off approach are two known techniques to achieve the energy proportionality goal. In DVFS, the supply voltage and link rate are adaptively scaled based on the bandwidth demand [11–13], as shown in Fig. 2.1(b). Note that in DVFS technique, while the instantaneous bandwidth demand exceeds the available bandwidth, the average bandwidth available in serial link matches with the average bandwidth demand, i.e. average area under the red curve and shaded region are equal. Fig-

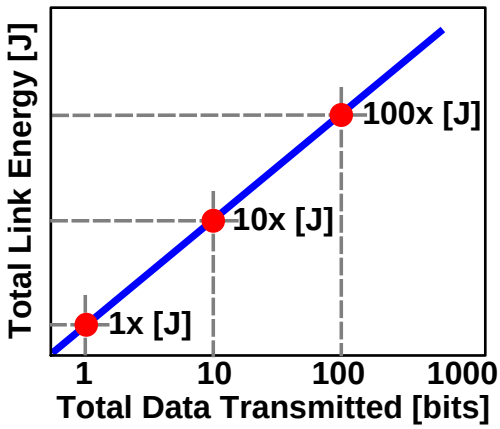


Figure 2.2: Concept of energy proportional operation in serial links.

ure 2.1(c) shows the energy proportional behavior of an ideal rapid-on/off communication scheme. In this technique, the link is powered down when idle and powered up instantaneously when the data is ready to be transferred [14–18], resulting in the most energy-efficient use of link bandwidth. In such systems, power consumption scales linearly with link utilization, resulting in energy consumption to become proportional to the transferred data.

DVFS and rapid-on/off operation have their own merits and challenges to achieve the desired power scalability and energy proportionality objective. This chapter presents a comparative study of both these techniques by pointing out their limitations and enumerates key challenges. The comparison is done with the help of a Matlab simulation of an abstract serial link model. The rest of the chapter is organized as follows. Section 2.1 describes the serial link architecture and model used for simulation. Section 2.2 discusses the DVFS theory, challenges, and simulation results. Section 2.3 presents the rapid-on/off non-idealities, simulation results, and key challenges. Section 2.4 presents comparative analysis with DVFS. Section 2.5 concludes this chapter.

2.1 Serial Link Architecture and Simulation Model

Figure 2.3 shows the block diagram of a high-speed serial link with embedded clock architecture and its approximate power break down. The transmitter consists of a phase locked loop

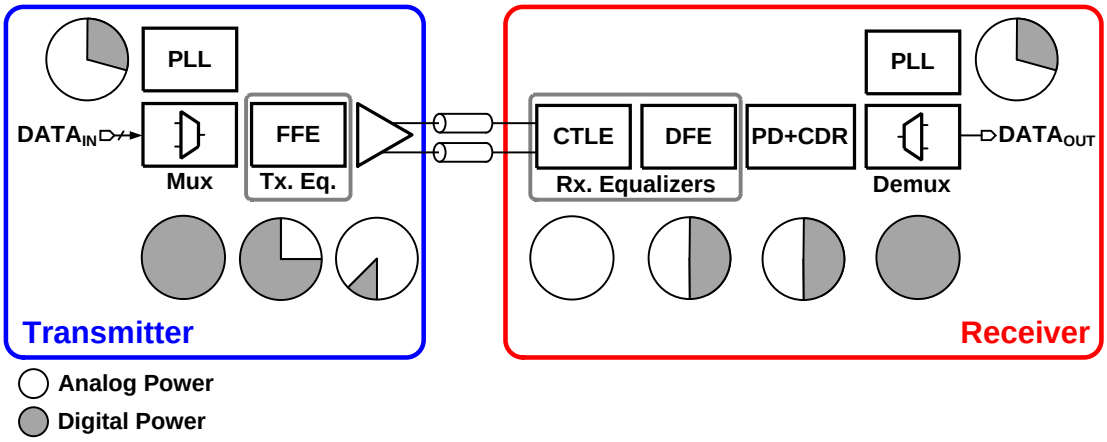


Figure 2.3: Embedded clock serial link architecture, and an approximate power break down of each block into analog and digital component.

(PLL) as a clock multiplier, serializing multiplexer (Mux), feed forward equalizer (FFE), and an output driver. The receiver consists of continuous time linear equalizer (CTLE), decision feedback equalizer (DFE), phase detector (PD), clock and data recovery loop (CDR), de-multiplexer block (Demux), and PLL. Mux and Demux blocks consist mostly of digital logic gates. The transmitter output driver, which can be either current mode logic (CML) or voltage mode based, has a majority of its power attributed to the analog component. The CTLE is a pure analog block and the current mode logic based DFE has both analog and digital components. It is difficult to scale power in analog circuits because voltage scaling is limited by the available bias margins and signal swing. Therefore, in the analysis, it is assumed that the analog power does not scale with the supply voltage or the data rate. Hence, understanding the composition of a serial link power in terms of its analog and digital components is essential to understand the efficacy of DVFS. For the modeling purpose, a serial link with digital and analog power component of 50% each is assumed. The simulation model consists of a serial link operating at 16Gb/s with an energy efficiency of 5pJ/bit.

2.2 Serial Link Power Scaling with DVFS

In the DVFS mode of operation, during periods of low bandwidth demand, the link data rate is reduced and digital supply voltage is scaled so as to barely meet the timing requirements. Section 2.2 presents a mathematical model of a serial link for DVFS and points out the challenges in using DVFS approach.

2.2.1 Mathematical Modeling and Simulation

Maximum achievable data rate in a serial link is inversely proportional to the delay through the CMOS logic, which can be expressed as

$$DataRate(V_{DD}) \propto \frac{\beta}{2}\frac{(V_{DD}-V_{TH})^{\alpha}}{V_{DD}C_L} \tag{2.2}$$

where β is a function of mobility, device size, and capacitance, V_{DD} is the instantaneous supply voltage of the link, V_{TH} is the threshold voltage, C_L is the load capacitance, and α is a constant close to 1.3 for short channel devices [19]. V_{DD} is scaled from V_{DDmax} of 1V to V_{DDmin} which is 0.45V ($1.5V_{TH}$). Below V_{DDmin}, the supply voltage is kept constant, and only the data rate is scaled so as to reduce power at lower link utilization.

To eliminate the device size and technology constants from the analysis, the data rate is normalized for a given V_{DD}, which is written as

$$DataRate_{norm}[Gb/s] = 16.\frac{DataRate(V_{DD})}{DataRate(V_{DDmax})} \tag{2.3}$$

where a factor of 16 is for the 16Gb/s link. The digital component of the serial link power at a given V_{DD} is written as

$$P_{DIG} = \left(\frac{V_{DD}}{V_{DDmax}}\right)^2 \frac{P_{LINK}.DataRate_{norm}}{2} \tag{2.4}$$

where P_{LINK} is serial link power at peak data rate, the factor or 2 in the denominator corresponds to 50% digital power. The analog component of link power remains constant irrespective of voltage scaling or data rate changes and is expressed as $P_{ANA} = 0.5P_{LINK}$.

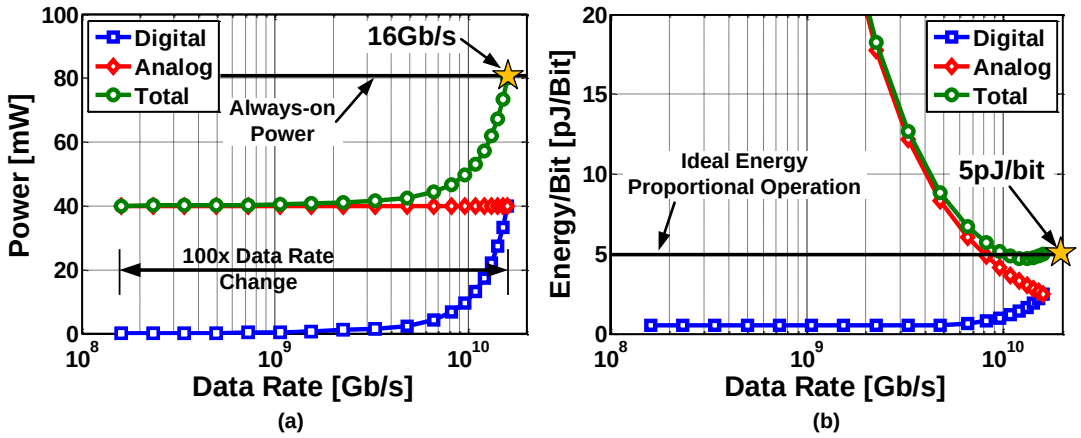


Figure 2.4: Matlab simulation of DVFS. (a) Power versus effective data rate. (b) Energy-per-bit versus effective data rate.

By using (2.3) and (2.4), energy-per-bit of the serial link is written as

$$\frac{Energy}{Bit} = \frac{P_{DIG} + P_{ANA}}{DataRate_{norm}} \tag{2.5}$$

Figure 2.4(a) and (b) show a plot of serial link power versus effective data rate and energy-per-bit versus effective data rate respectively. At high effective data rates, link power scales down rapidly as the digital component reduces. However, at very low data rates the link power stays constant and consequently energy-per-bit increases, thereby deviating from ideal energy proportional operation.

2.2.2 Challenges and Opportunities in DVFS

It can be observed from Fig. 2.4 that analog power in a serial link is the biggest bottleneck in achieving energy proportionality with DVFS technique. At low data rates (1Gb/s-to-2Gb/s), low-loss short channels, and fine technology nodes, the majority of serial link power is attributed to digital power due to the absence of equalization and termination requirements. Therefore, DVFS is more suitable for links, which are mostly digital.

Time needed for voltage regulators and PLLs to settle supply voltage and frequency to a new value could be of the order of hundreds of nanoseconds or a couple of microseconds.

During this time, the link sits idle and consumes power, which further degrades the energy-per-bit. The voltage regulator and PLL settling time result in performance penalty because the processor has to wait for the serial link to stabilize before it can begin moving data. The processor continues to be clocked and consume power during this wait period. Consequently, the overall system energy efficiency is reduced. The energy analysis of DVFS presented in the Section 2.2.1 did not account for the loss in processor performance.

2.3 Serial Link Power Scaling with Rapid-On/Off

In rapid-on/off mode of operation, the serial link has two power states, namely on-state and off-state, as shown in Fig. 2.5(a). The link is powered-off when idle and powered-on instantaneously when there is data to be transferred, as shown in Fig. 2.5(b). The on/off transition time must be of the order of nanoseconds so that the link can be powered-on/off with very fine granularity. In this way, the power consumption scales linearly with link utilization (see Fig. 2.1(c)), resulting in energy consumption to become proportional to the transferred data, and the serial link, therefore, achieves energy proportional operation.

2.3.1 Effect of Non-Idealities on Rapid-On/Off Links

Practical serial links have finite power-on time, non-zero off-state power, and finite power-cycling energy. The effect of these parameters on the link's energy efficiency (energy-per-bit) can be mathematically captured as:

$$\frac{Energy}{Bit} = \frac{P_{ON}T_{ON} + P_{ON}T_{POWER-ON} + P_{OFF}T_{OFF} + E_{ON-OFF}}{Total\ number\ of\ bits\ transmitted} \tag{2.6}$$

where P_{ON} is the on-state power, P_{OFF} is the off-state power, T_{ON} is the on-state time, T_{OFF} is the off-state time, $T_{POWER-ON}$ is the power-on time and E_{ON-OFF} is the energy consumed during on/off transition.

Finite power-on time is due to the time required to charge/discharge bias nodes, and time needed for the clock multiplier to achieve frequency and phase lock. Energy wasted

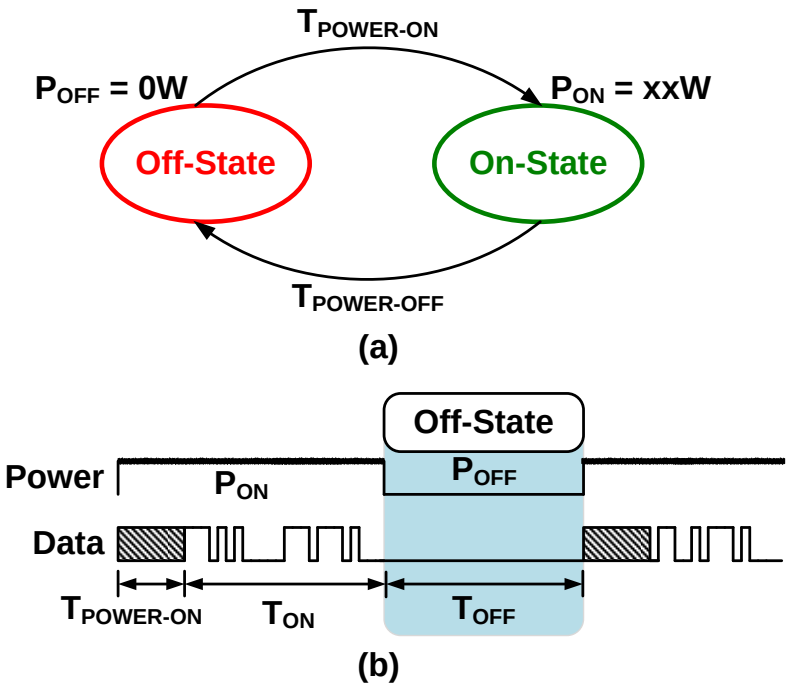


Figure 2.5: (a) Power states in rapid-on/off mode of operation. (b) Timing diagram in rapid-on/off mode of operation.

during power-on time degrades the energy proportional behavior of the link. Assuming the link consumes approximately peak power during the power-on transition, this wasted energy equates to $P_{ON}T_{POWER-ON}$. The effect of power-on time on link efficiency is shown in Fig. 2.6(a). For a constant burst length, power-on energy ($P_{ON}T_{POWER-ON}$) increases the energy-per-bit by a fixed amount across all link utilization values.

Finite off-state power in the link is mainly due to current biases that were left powered-on to reduce power-on time and leakage in logic gates. Figure 2.6(b) illustrates the effect of static off-state power on link energy-efficiency. At lower link utilization ($T_{OFF} >> T_{ON}$), even with a small off-state power (P_{OFF}), the off-state energy ($P_{OFF}T_{OFF}$) starts to dominate link energy-efficiency. Therefore, the off-state power must be close to zero to achieve constant energy-per-bit at extremely low data rates.

Power-cycling energy is the energy consumed in charging/discharging nodes in each power cycle or data burst event. Therefore, more frequent data bursts incur larger energy penalty. Figure 2.6(c) shows the effect of burst length on energy-per-bit for a fixed effective data

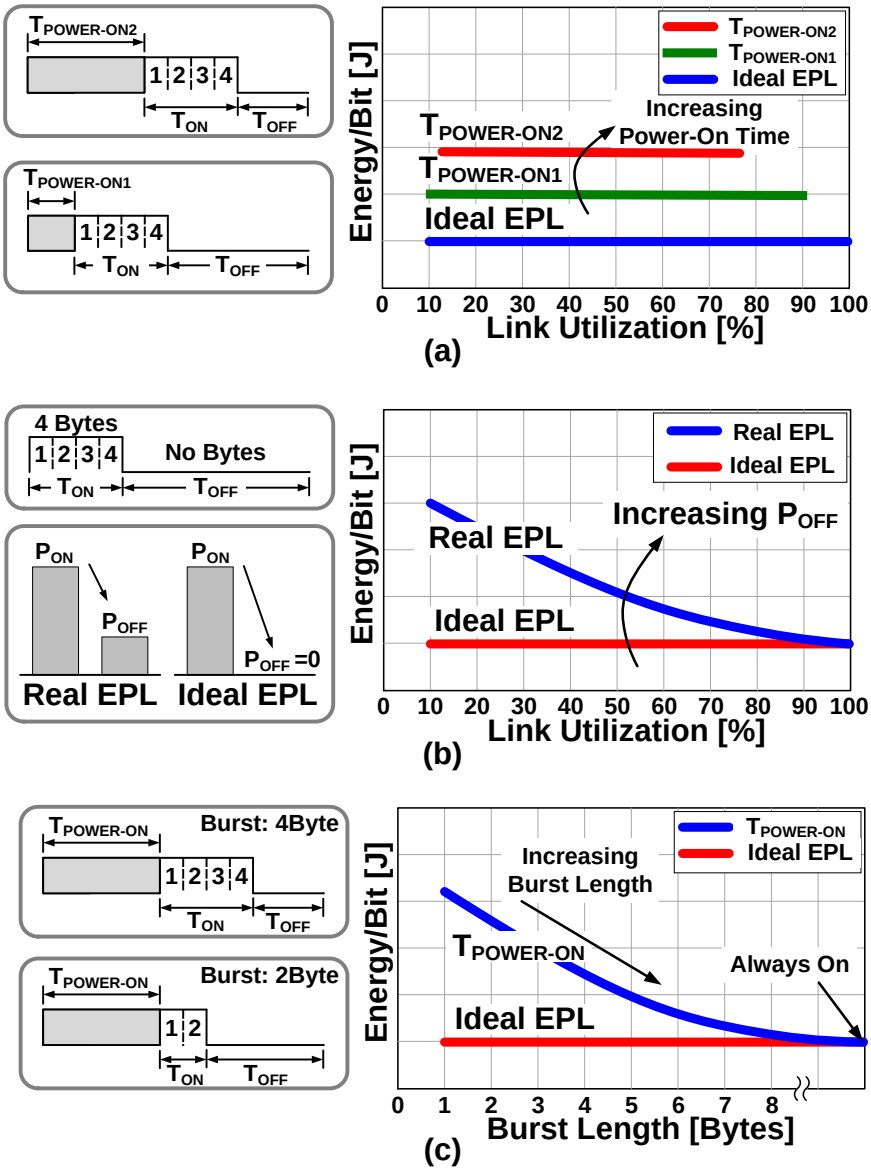


Figure 2.6: Effect of non-ideal behavior of rapid-on/off links. (a) Effect of power-on time on link energy efficiency. (b) Effect of static off-state power on link energy efficiency. (c) Effect of data burst length on link energy efficiency.

rate. When the data is transferred in smaller bursts, energy spent in powering-on the link ($P_{ON}T_{POWER-ON}$) and power cycling energy (E_{ON-OFF}) becomes comparable to the on-state energy ($P_{ON}T_{ON}$) and consequently leads to increased energy-per-bit.

The plot of energy-per-bit versus utilization captures essential features of power scalable or energy proportional links. With the help of energy-per-bit versus utilization plot, energy

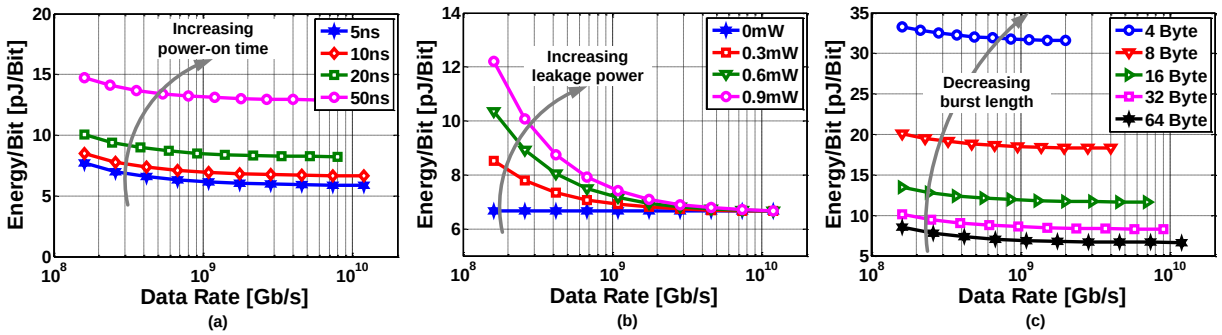


Figure 2.7: Matlab simulation of burst mode operation. (a) Energy-per-bit versus effective data rate for various power-on time. (b) Energy-per-bit versus effective data rate for various off-state power values. (c) Energy-per-bit versus effective data rate for various data burst lengths.

consumption estimates can be made for a given link usage scenario of an application. Thus, it forms one of the important metrics to characterize and compare such links.

For simulating non-idealities in rapid-on/off mode, a serial link operating at 16Gb/s with an energy efficiency of 5pJ/bit is used. This serial link consumes 80mW of power in the on-state. Figure 2.7 shows the simulated results in the presence of non-idealities. P_{OFF} of 300μW, burst length of 64 bytes, $T_{POWER-ON}$ of 10ns and E_{ON-OFF} of 50pJ are used in these simulations unless otherwise stated. The effect of power-on time from 5ns to 50ns on the link's energy-per-bit is shown in Fig. 2.7(a). The effect of off-state power from 0μW to 900μW on the link's energy-per-bit is shown in Fig. 2.7(b). The effect of data burst length from 4 bytes to 64 bytes on the link's energy-per-bit is shown in Fig. 2.7(c).

2.3.2 Challenges and Opportunities in Rapid-On/Off Operation

Voltage mode output drivers, though more efficient than current mode logic based drivers, require a voltage regulator to set the output swing. However, this regulator cannot be powered-on/off instantaneously. Even if we keep the regulator powered-on during the off-state at the expense of small power penalty, voltage droop caused due to the limited load transient response reduces the eye margin on the samplers at the receiver end. Current mode output drivers are immune to supply noise variation. However, the bias current needed to

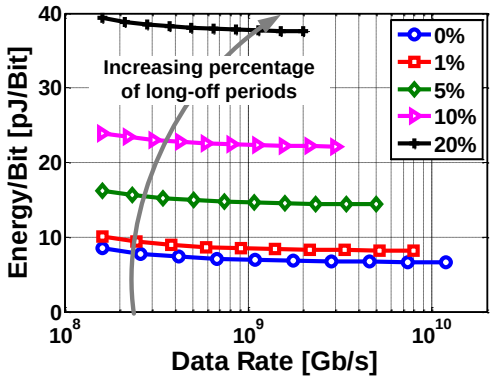


Figure 2.8: Energy-per-bit versus effective data rate for the various percentages of time long off-periods could occur.

bias the output driver must be powered-on instantaneously, which is difficult to achieve in practice.

During the long off-periods, due to change in temperature, the oscillator frequency could drift from the locked position. Limited load transient response of the voltage regulator could also change the oscillator frequency during power-on. Therefore, during the power-on period, both frequency and phase of the oscillator must be locked to the reference. Phase and frequency settling in the phase locked loop are governed by the loop bandwidth, which is limited to one-tenth of the reference frequency due to stability reasons [20]. Consequently, PLLs could take several hundred nanoseconds to achieve the phase and frequency lock. The effect of long frequency locking time due to temperature drift on the link's energy efficiency is simulated for various percentages of time such an event could happen, and the results are shown in Fig. 2.8. Frequency locking time of 1μs is assumed in this simulation. For applications where long off periods could happen 20% of the time, the energy efficiency degrades by almost 7x at high data rates.

Recently, PLL with 100ns of phase lock time has been demonstrated [21]. However, it is not sufficient to achieve the energy proportional objective. Multiplying delay locked loop (MDLL) [22] and multiplying injection locked oscillator (MILO) [14] have also demonstrated phase locking in 10ns ($\approx 3T_{REF}$) and less. However, performing fast frequency locking in PLL, MDLL and MILO remains a challenging research problem.

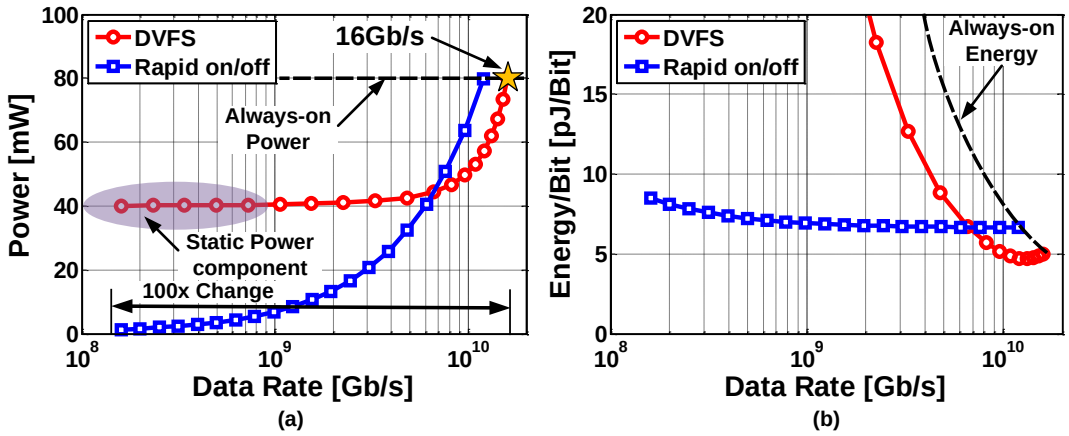


Figure 2.9: Comparison of DVFS and rapid-on/off operation. (a) Power versus effective data rate. (b) Energy-per-bit versus effective data rate.

On the receiver end, detecting a start of transition and powering-up the receiver in a few nanoseconds is a non-trivial design problem. Powering up the equalization chain and synchronizing the clock and data recovery loop with the incoming data remains unaddressed in the literature.

2.4 DVFS versus Rapid-On/Off

Comparison of DVFS with the rapid-on/off based link is made with the help of an abstract model presented in Section 2.1, and the results are shown in Fig. 2.9. It can be observed that, for a 100x change in data rate (16Gb/s - 160Mb/s), the energy-per-bit for the DVFS is increased by 50x (5pJ-250pJ), while for the burst mode it is increased by only 1.7x (5pJ-8.5pJ). For the data rates between 8Gb/s-16Gb/s, DVFS seems to perform better than the burst mode. This is due to the fact that the digital power in DVFS scales down rapidly. However, at lower data rates, the component of analog power dominates the serial link power and results in energy efficiency degradation in DVFS. Consequently, for a broad range of link utilizations, rapid-on/off performs better than DVFS.

2.5 Conclusion

DVFS and rapid-on/off operation are two key techniques to achieve power scalability and energy proportional operation in the serial links. In this chapter, an abstract model of a serial link was presented, and comparative study of DVFS and rapid-on/off operation was done. DVFS was found to be limited by the analog component of serial link power and is, therefore, useful for all-digital short-channel serial links. Rapid-on/off operation is an attractive way to achieve energy proportional operation as both the analog power and digital power can be scaled depending on the utilization. Therefore, the rapid-on/off approach can be effectively used for high-speed serial links.

In this dissertation, the rapid-on/off approach is used to achieve power scalability and energy proportional operation. The focus of the next chapters is on addressing non-idealities in rapid-on/off based serial links by designing novel architectures.

CHAPTER 3

A 5Gb/s TRANSMITTER FOR ENERGY PROPORTIONAL LINKS (EPL)

In this chapter, we present a rapid-on/off transmitter consisting of a voltage mode driver and a clock multiplier. Fabricated in 90nm CMOS process, the prototype transmitter achieves 100x effective data rate range (5Gb/s-0.048Gb/s) while scaling the power by 50x(4.8mW-0.095mW) and energy efficiency by only 2x(1-2pJ/Bit). Such energy proportional operation is achieved by using a fast power-on voltage mode driver and fast power-on lock multiplying delay locked loop (MDLL) based digital clock multiplier. In this work, wide effective data rate range is achieved by duty cycling the transmitter at a fixed data rate of 5Gb/s and not by changing active data rate. By adopting a digital voltage regulator, the prototype voltage mode driver achieves 2ns power-on time, less than 11μW off-state power, 32pJ energy overhead for on/off transition, and 2.6mW on-state power at 5Gb/s output data rate. By employing a highly scalable digital architecture with accurate frequency presetting and instantaneous phase acquisition, the prototype 8x/16x clock multiplier achieves 10ns (3 reference cycles) power-on time, 2ps$_{rms}$ long-term absolute jitter, less than 25μW off-state power, 12pJ energy overhead for on/off transition, and 2.2mW on-state power at 2.5GHz output frequency [22].

The rest of the chapter is organized as follows. Section 3.1 discusses the building blocks of a conventional transmitter and their limitations for rapid-on/off application. Section 3.2 introduces the proposed transmitter architecture. A mathematical modeling of MDLL power-on transient is presented in Section 3.3. Circuit details of the clock multiplier are discussed in Section 3.4. Section 3.5 presents the measured results. Section 3.6 concludes the chapter.

3.1 Limitations of Conventional Transmitter for Rapid-On/Off Links

3.1.1 Output Driver

Voltage-mode (VM) drivers dissipate a quarter of the power as compared to the current-mode logic (CML) output drivers [23]. However, voltage regulators required to set output swing and termination impedance cannot be powered-on instantaneously. Keeping these regulators always-on, severely impacts energy-per-bit at lower data rates [15]. Digital voltage regulators [24,25], provide a means to power-on/off rapidly while consuming no static power in the off-state. The pass transistor in the digital regulator also helps in power-gating the logic, resulting in low leakage power in the off-state. For these reasons, digital regulators are employed in the proposed VM driver.

3.1.2 Clock Multiplier

The long locking time of conventional clock multipliers implemented using phase locked loops (PLLs) presents the biggest bottleneck in achieving energy proportional operation. Increasing the PLL bandwidth reduces the locking time. However, to ensure loop stability, loop bandwidth cannot exceed one-tenth the reference frequency [20]. As a result, even if the VCO frequency is precisely set digitally, the sluggish phase acquisition limits the phase locking time to at best a few hundred nanoseconds [15,26]. Techniques such as dynamic phase error compensation [27], edge-missing compensation [28], and hybrid PLLs [29] improve the phase acquisition time. By calibrating the phase of the feedback clock, the best power-on time of forty reference cycles has also been reported [21]. However, such improvements are inadequate to achieve the energy proportional operation goal.

The multiplying injection locked oscillator (MILO) provides a means to reduce power-on time. Figure 3.1(a) shows an MILO, which is phase locked to four times the reference frequency. A pulse train generated at the reference frequency is injected into the oscillator to achieve fast phase locking. The spectrum of this pulse train is rich in frequency components

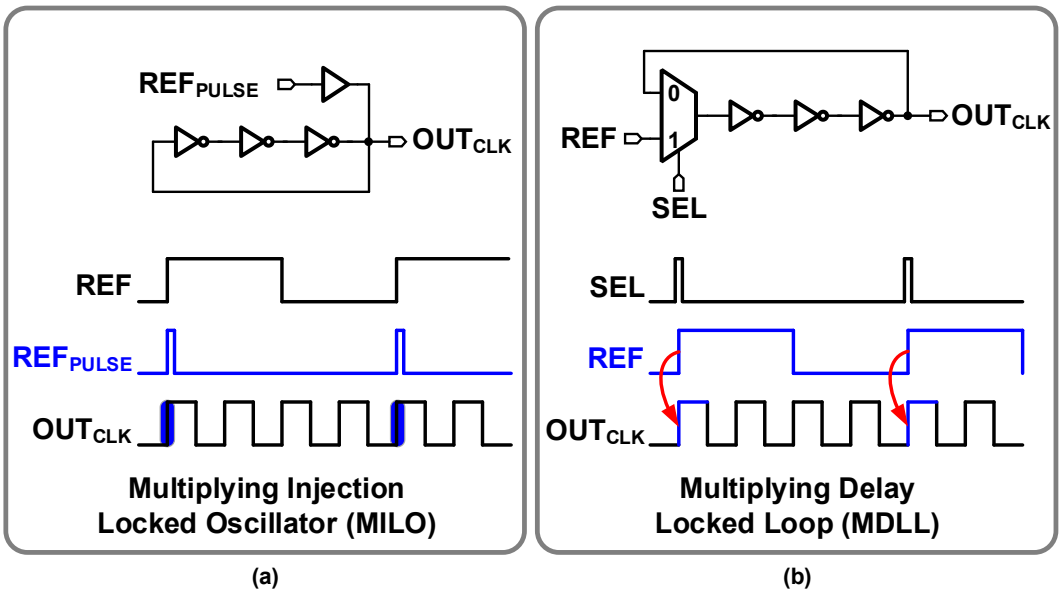


Figure 3.1: (a) Simplified schematic and timing diagram of a multiplying injection locked oscillator (MILO). (b) Simplified schematic and timing diagram of a multiplying delay locked loop (MDLL).

at reference, and its harmonics and these harmonics appear as spurs at the output. By increasing MILO's bandwidth with stronger injection strength, locking time can be reduced. However, wide bandwidth results in large spurs at the injection frequency [30]. Filtering of MILO's output with a second injection locked oscillator (ILO) could reduce these spurs. However, it comes at the cost of extra power [31]. This trade-off, which compromises the lock time, limits the use of MILOs for fast power-on applications.

Multiplying delay locked loop (MDLL) provides a means to overcome the drawbacks of MILOs. Figure 3.1(b) shows an MDLL, which is phase locked to four times the reference frequency. In MDLL, every N^{th} VCO edge is replaced by the clean reference edge by opening up the ring oscillator for a brief period using a narrow pulse [32–34]. This edge replacement results in instantaneous phase locking, which is independent of the bandwidth. Inserting a clean reference edge every reference cycle resets all accumulated jitter in the VCO and results in superior jitter performance [35, 36]. A perfect edge replacement results in no reference spurs at the output. These features make MDLL a suitable candidate for fast power-on applications.

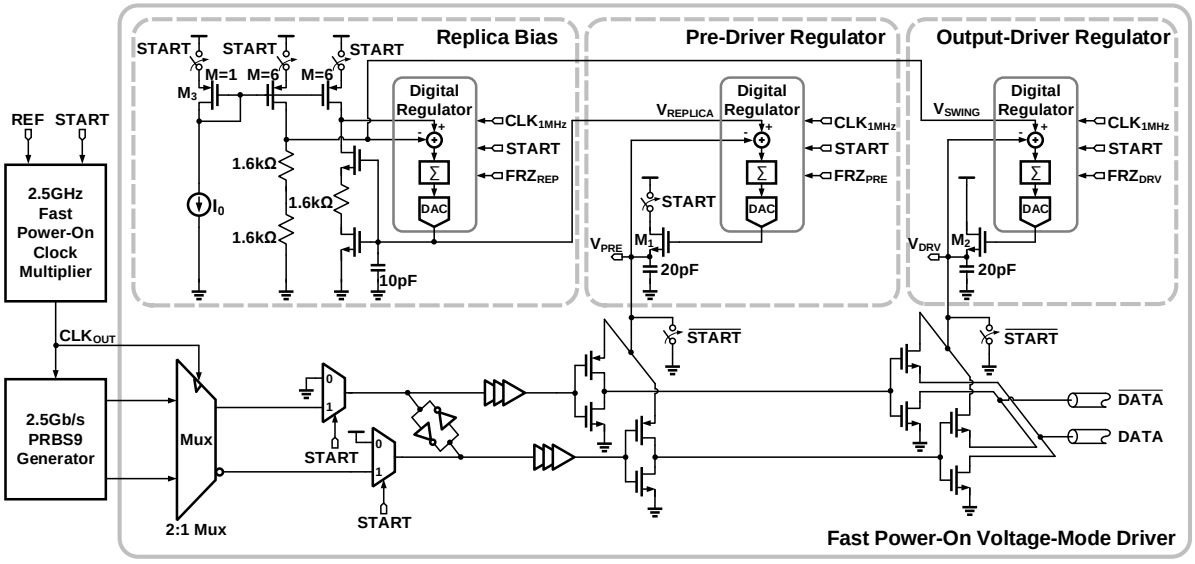


Figure 3.2: Schematic diagram of the proposed fast power-on transmitter.

3.2 Proposed Fast Power-On Transmitter Architecture

Figure 3.2 shows the block diagram of the proposed transmitter. It consists of a fast power-on lock clock multiplier, a 2:1 latch based multiplexer, and a voltage mode driver output stage. The clock multiplier, implemented using a digital multiplying delay-locked loop (MDLL), generates a 2.5GHz output from a 312.5MHz reference clock. The PRBS9 generator outputs data at 2.5Gb/s, which is serialized to get a valid PRBS9 pattern and transmitted at 5Gb/s with 250mV differential peak-to-peak output swing.

The proposed voltage mode driver consists of a replica bias, pre-driver, and an output driver. The replica bias circuit generates reference voltages $V_{REPLICA}$ and V_{SWING} for the pre-driver and output driver regulators, respectively. $V_{REPLICA}$ needed to create 50 ohm output impedance is generated by enclosing a replica of the output driver [37], which is $1/16^{th}$ the original size, in a closed loop. V_{SWING} sets the differential output driver swing. Pre-driver and output driver regulators use the replica bias output to generate virtual supply voltages for the pre-driver (V_{PRE}) and output driver (V_{DRV}), respectively. These regulators are implemented using digital feedback loops, which help in storing states during the power-off event and in restoring states during power-on.

Figure 3.3 shows the schematic of the proposed digital voltage regulator. It consists of

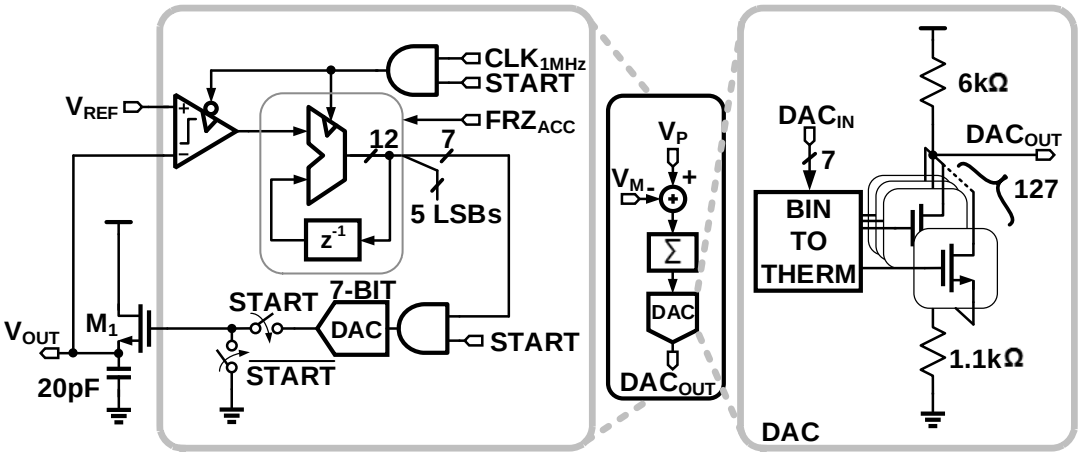


Figure 3.3: Schematic diagram of the proposed digital voltage regulator.

a clocked comparator, an accumulator, and a resistive DAC. V_{OUT} is compared with V_{REF}, and the output is fed to the 12-bit accumulator. The accumulated output drives a 7-bit resistive DAC to minimize the error between V_{REF} and V_{OUT}. The lower 5LSBs of the accumulator output are ignored to reduce voltage ripple due to loop delay. The DAC uses high V_{th} transistors to avoid leakage in the off-state. A 1.1k ohm resistor at the bottom of the DAC provides desired voltage offset. A 20pF decoupling capacitor at the output of transistor M_1 helps in suppressing noise on the output voltage. A large capacitor helps in suppressing more noise, but it increases the power-on time and the energy consumed during power-on/off cycle.

3.2.1 Power-On Transient Response of the Transmitter

Figure 3.4 shows the transient response of the transmitter. When the $START$ signal is de-asserted, the pre-driver and output driver regulators output V_{PRE} and V_{DRV} nodes are discharged to ground. The gates of transistors M_1 and M_2 are pulled low (see Fig. 3.2), the clock to all comparators is gated, and bias current of the replica bias block is turned off. In this state, only the leakage current in digital logic contributes to off-state power consumption. During the off-state, regulator states are saved in their respective accumulators.

When the $START$ signal is asserted, the DACs rapidly restore the accumulator's state

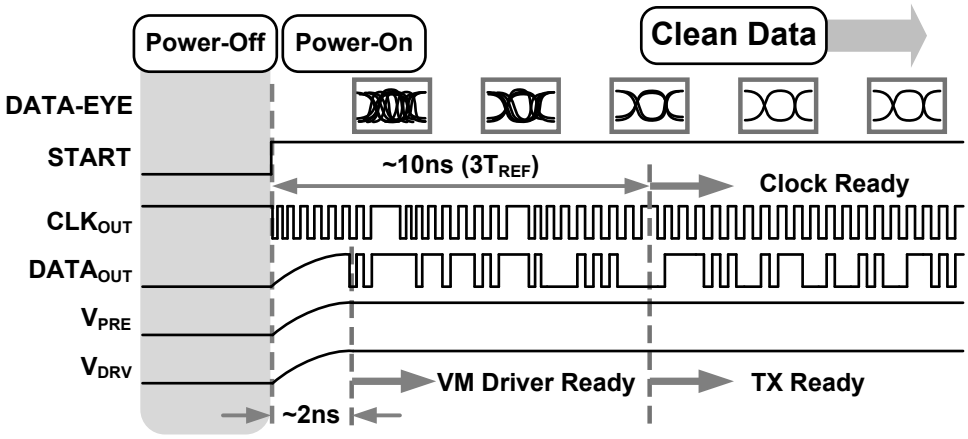


Figure 3.4: Transient response of the proposed fast power-on lock transmitter.

and set the gate voltages of transistors M_1 and M_2, which quickly bring V_{PRE} and V_{DRV} to the desired value. The 20pF decoupling capacitor charges up in 2ns, after which the driver is ready for transmitting data. The MDLL based clock multiplier limits the transmitter start-up time, which takes around 10ns (three reference cycles) to start.

During the power-on state, the PMOS diode (M_3) in the replica bias settles slowly with a large time constant. This results in a slow settling of $V_{REPLICA}$ and V_{SWING} nodes after power-on. To avoid the effect of these variations on the regulator output (V_{PRE} and V_{DRV}), the accumulators of pre-driver and output driver regulators are frozen using FRZ_{PRE} and FRZ_{DRV} signals. Once the $V_{REPLICA}$ and V_{SWING} nodes settle, the FRZ_{PRE} and FRZ_{DRV} signals are de-asserted, and the regulators go back in closed-loop operation.

3.2.2 Effect of Power Supply Droop on Output Driver

Burst mode operation requires fast load transient response linear regulators [38–40] to power the transmitter. When the output driver is powered-on, the output of the regulator droops momentarily before regaining its original value. The amount of droop and transient response time are a function of loop dynamics of an external regulator and current step. To capture this effect, the output driver including the multiplexer is simulated with a fast load transient response regulator. Figure 3.5 shows the current step, power supply droop and the output eye diagram at various time instants. Droop in the power supply increases output jitter,

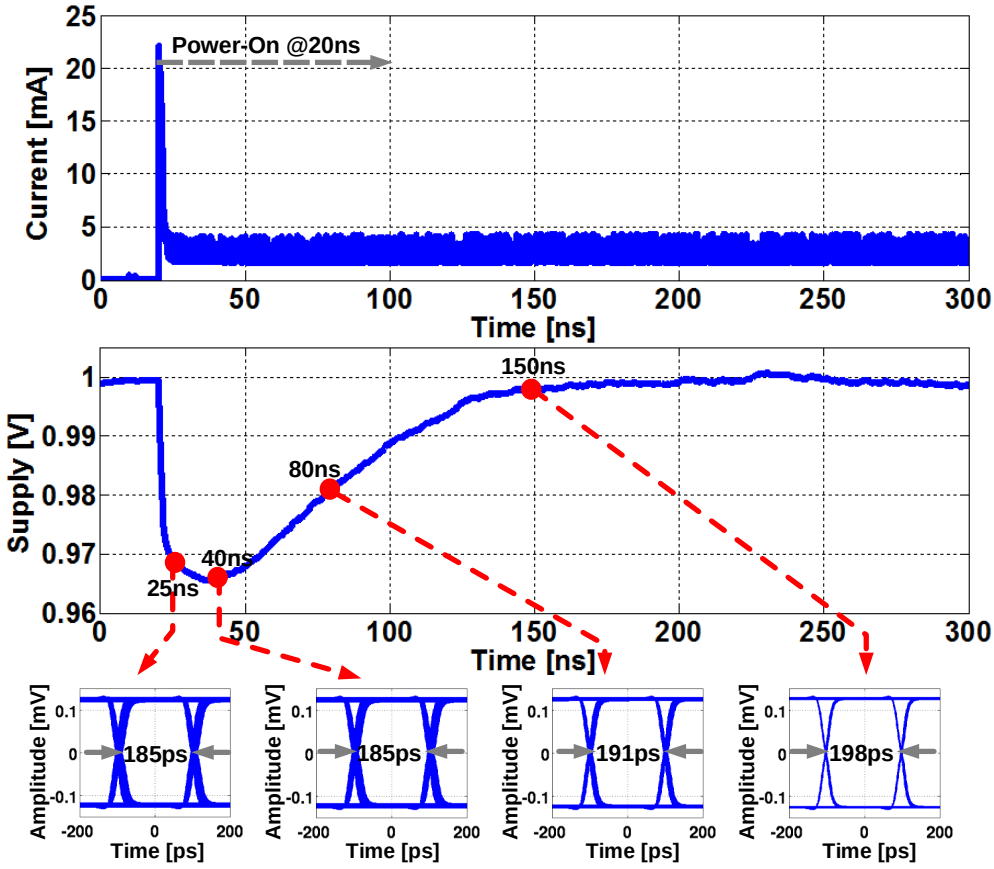


Figure 3.5: Simulated power supply droop on the output driver.

which will eventually reduce the sampling margin on the receiver.

3.2.3 Fast Power-On Clock Multiplier

Figure 3.6 shows the block diagram of the proposed MDLL based digital clock multiplier. It employs a split tuned architecture in which a frequency locked loop (FLL) drives the ring oscillator close to the frequency lock, and an integral control that brings the oscillator frequency to the desired output frequency. The proportional path ensures stability by periodically resetting the oscillator output phase with the input reference clock phase using edge replacement logic (ERL). Frequency locked loop consists of a frequency detector, 12-bit accumulator clocked at $F_{REF}/256$, fast settling DAC and a constant current source I_1. Integral path uses a bang-bang phase detector, 13-bit accumulator, and 8-bit DAC. The phase

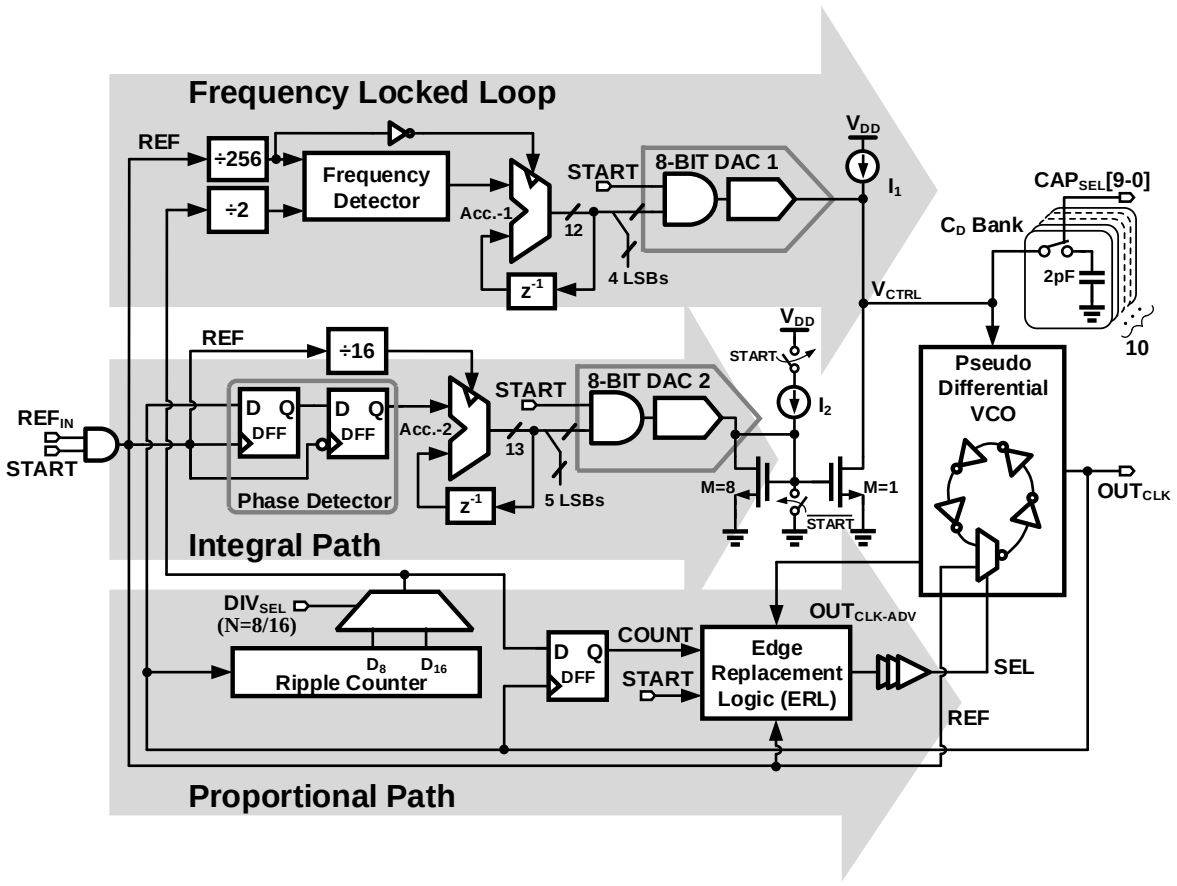


Figure 3.6: Schematic diagram of the proposed fast power-on MDLL based digital clock multiplier.

detector consisting of two D flip-flops, clocked at the reference frequency, produces lead/lag phase information with a 1-bit output. The accumulator clocked at $F_{REF}/16$ integrates the sub-sampled bang-bang phase detector output. Sub-sampling has no adverse effect on the jitter performance because the accumulated sub-sampled output is used only to track frequency drifts due to voltage and temperature changes during normal operation that are slower than $F_{REF}/16$.

The proportional path consists of a programmable divider and edge replacement logic (ERL). The edge replacement logic generates a narrow SEL signal pulse, which opens up the ring oscillator momentarily and passes the clean reference edge. To have a perfect edge replacement, care is taken to generate the SEL signal with sharp rise and fall times.

The digital accumulators store the frequency information of the oscillator in the digital

form during the power-off state. They are synthesized with high V_{th} devices to reduce leakage. Four LSBs from the frequency locked loop accumulator and five LSBs from the fine integral path accumulator are ignored to avoid ripple on control voltage node, V_{CTRL}, due to loop delay. To reduce the power-on time penalty caused by slow settling transients, the DAC bias circuitry is not turned-off in the power-off state. The bias voltages are maintained at the expense of a small power penalty during the off-state. When the MDLL is powered-on, the frequency information is rapidly restored to the oscillator using fast Nyquist-rate DACs, thus bringing the oscillator to frequency lock quickly. Once frequency lock is achieved, the rising edge of the reference replaces the N^{th} oscillator edge thus achieving instantaneous phase lock.

Periodic edge replacement results in current being drawn periodically from V_{CTRL}, thereby causing a supply ripple at the reference frequency and its harmonics. Despite the pseudo differential nature of VCO, current drawn by VCO is not constant, which causes a ripple on V_{CTRL}. Deterministic jitter (DJ) resulting from V_{CTRL} ripple can be reduced with a decoupling capacitor. However, a large decoupling capacitor increases the time constant on the V_{CTRL} node, thereby increasing the time it takes for the frequency to settle to the right value, which eventually increases power-on lock time. To quantify this trade-off between DJ and power-on lock time, a bank of programmable decoupling capacitor (C_D bank) is added on the V_{CTRL} node and the measured results are presented in Section 3.5.

3.2.4 Power-On Transient Response of the Clock Multiplier

Figure 3.7 shows the power-on transient response of the proposed clock multiplier. When the multiplier is powered-off, REF signal is gated, SEL signal is asserted high, and the VCO stops oscillating. Once the VCO is open, it no longer sinks current. This causes the V_{CTRL} node to charge up to V_{DD}, which eventually shuts down current source I_1. When the multiplier is powered-on, the SEL signal is de-asserted, and the VCO starts to oscillate. The V_{CTRL} node then settles to the desired value with a finite time constant. During the time when the V_{CTRL} node is settling, the VCO oscillates at a higher frequency, which causes the rising edge of the divider output $COUNT$ signal to appear earlier than desired. On the

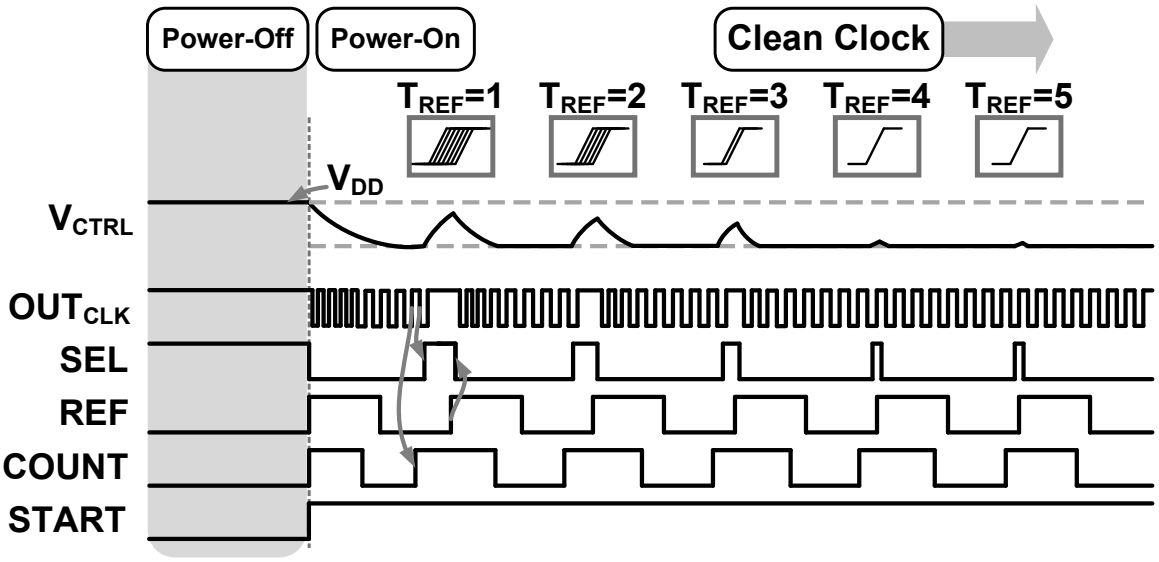


Figure 3.7: Transient response of the proposed fast power-on clock multiplier.

rising edge of the $COUNT$ signal, the SEL signal is asserted high, and the VCO opens up and waits for the rising edge of the REF signal to pass through. During this waiting period, VCO stops, and the V_{CTRL} node again rises toward V_{DD}. On the subsequent rising edge of the reference, the SEL signal is de-asserted, and the VCO begins to oscillate again. In the second reference cycle, the V_{CTRL} node again settles to the desired value but the initial high oscillation frequency again causes a rising edge of the divider output $COUNT$ signal to appear earlier than desired. However, this time it appears closer to the rising edge of the reference signal, which causes smaller disturbance on the V_{CTRL} node. This results in smaller oscillator frequency variation as compared to the first reference cycle. In the third reference cycle, the disturbance on the V_{CTRL} node is even smaller, and the multiplier is close to achieving frequency and phase lock. Thus, in the proposed MDLL architecture, the power-on time is mainly limited by the time constant on the V_{CTRL} node.

3.3 Power-On Transient Modeling of MDLL

MDLL in the locked state satisfies the following relationship: $N.T_{VCO} = T_{REF}$, where N is the multiplication ratio, T_{VCO} is the VCO's time period, and T_{REF} is the reference clock time period. However, while acquiring a lock, the V_{CTRL} node varies, and T_{VCO} does not

remain constant for all N VCO cycles (see Fig. 3.7). Consequently N VCO cycles finish earlier than expected. The accumulated jitter, T_j, during N VCO cycles can be written as

$$T_j = T_{REF} - T_{NVCO} \tag{3.1}$$

where T_{NVCO} is the time required to complete N VCO cycles and can be written as

$$T_{NVCO} = \sum_{i=1}^{N} T_{VCOi} \tag{3.2}$$

where T_{VCOi} is the VCO's time period in the i^{th} VCO cycle. The MDLL is considered completely powered-on when T_j is below the desired value.

A simplified schematic diagram of VCO, for two SEL signal conditions, is shown in Fig. 3.8(a). The DAC and current source I_1 are together shown as one current source I_{VCO}. The capacitors C_{PAR} and C_D are together shown as one capacitor, C_{VCO}, on the V_{CTRL} node. When the SEL signal is low, VCO is replaced with an equivalent resistor R_{VCO}, which sinks current I_{VCO}. When the SEL signal is high, the VCO no longer sinks current, and the V_{CTRL} node starts to settle toward V_{DD}. This causes the current source I_{VCO} transistor to operate in the linear region and is modeled as resistor R_{LIN}. The time constants on the V_{CTRL} node are $R_{VCO}C_{VCO}$ and $R_{LIN}C_{VCO}$ when the SEL signal is asserted low and high, respectively.

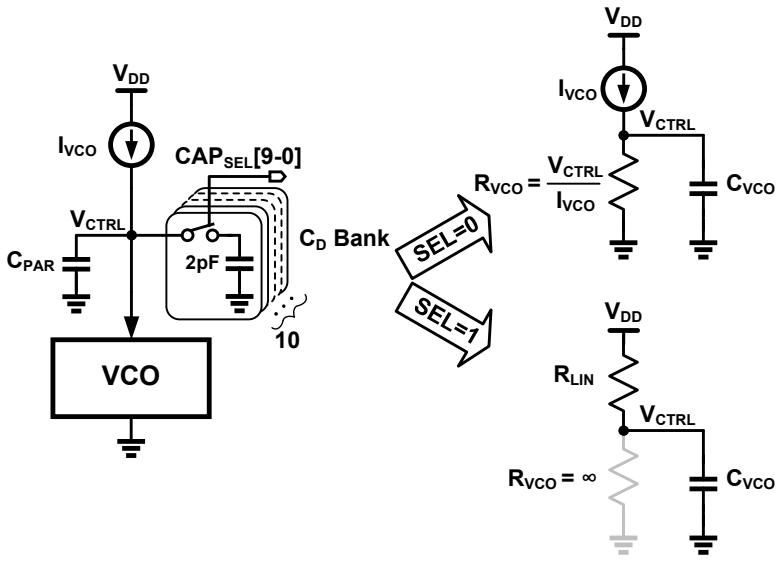
Figure 3.8(b) shows magnified startup transient during the first reference cycle. When the multiplier is powered-on, the instantaneous VCO's oscillation frequency is equal to

$$f_{VCO}(t) = K_V V_C + K_V(V_{DD} - V_C)e^{-t/\tau} \tag{3.3}$$

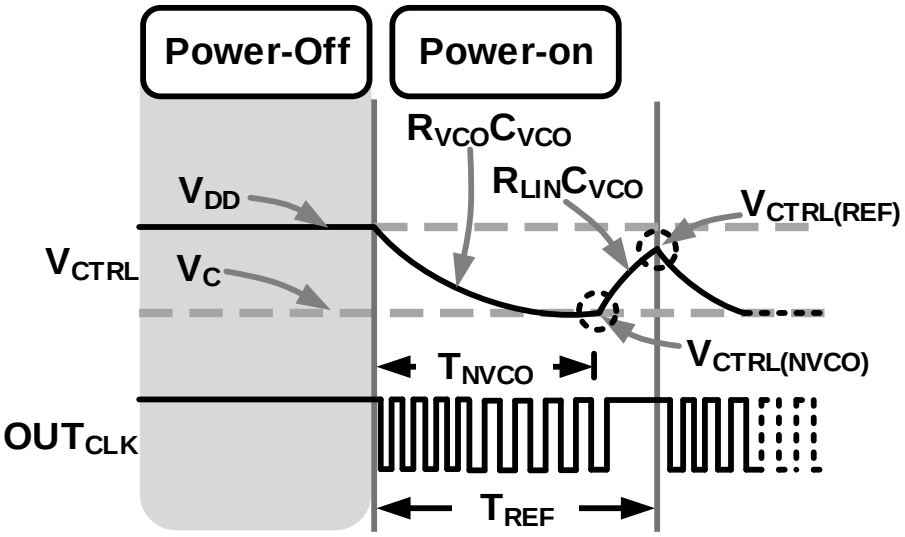
where K_V is the VCO's gain in Hz/V, V_C is the steady-state V_{CTRL} value and $\tau = R_{VCO}C_{VCO}$ forms the VCO's time constant. Integrating (3.3) from 0 to T_{NVCO} gives

$$\int_0^{T_{NVCO}} f_{VCO}(t)dt = \int_0^{T_{NVCO}} K_V(V_C + (V_{DD} - V_C)e^{-t/\tau})dt \tag{3.4}$$

$$\Rightarrow N = K_V(V_C T_{NVCO} + \tau(V_{DD} - V_C)(1 - e^{-T_{NVCO}/\tau})) \tag{3.5}$$



(a)



(b)

Figure 3.8: (a) Simplified schematic diagram of oscillator for modeling power-on transient. (b) Power-on transient of VCO during the first reference cycle.

For a given N, K_V, V_C, V_{DD} and τ, equation (3.5) can be solved numerically for T_{NVCO}. T_j is obtained by substituting T_{NVCO} in (3.1). If $T_j \neq 0$ then during time T_j, the V_{CTRL} rises toward V_{DD} with the time constant of $R_{LIN}C_{VCO}$. The voltage at V_{CTRL} at the end of the

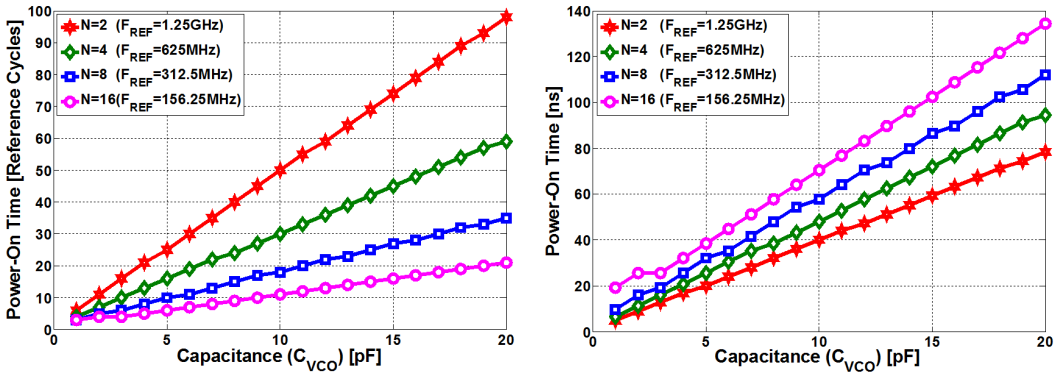


Figure 3.9: Modeling result of settling time in terms of reference cycles and absolute time versus C_{VCO} for various values of N (settled T_j ¡ $10ps$). $F_{VCO} = 2.5$GHz, $V_C = 0.8$V, $R_{VCO} = 1$K ohm, $K_V = 3.125$GHz/V, $R_{LIN} = 4$k ohm, and $V_{DD} = 1.1$V.

first reference cycle is given as

$$V_{CTRL(REF)} = V_{DD} - (V_{DD} - V_{CTRL(NVCO)})e^{-T_j/R_{LIN}C_{VCO}} \tag{3.6}$$

where $V_{CTRL(NVCO)}$ is V_{CTRL} at the end of first N VCO cycles and is written as

$$V_{CTRL(NVCO)} = V_C + (V_{DD} - V_C)e^{-T_{NVCO}/\tau} \tag{3.7}$$

In the second reference cycle, V_{CTRL} settles toward V_C starting from $V_{CTRL(REF)}$. By using (3.1) and (3.5) and replacing V_{DD} with $V_{CTRL(REF)}$, T_j is calculated for the second reference cycle. This process is continued until T_j reaches below the desired value.

Equations (3.1)-(3.7) were coded in Matlab, and the plot of power-on time in terms of reference cycles and absolute time as a function of C_{VCO} for various multiplication ratios N is shown in Fig. 3.9. The settling time increases linearly with C_{VCO}. For small values of C_{VCO} (smaller time constant $R_{VCO}C_{VCO}$), the V_{CTRL} settles to V_C before completing N VCO cycles. As a result, the value of T_j at the end of first few reference cycle stays independent of the multiplication factor N. Hence, for small time constants and a fixed VCO frequency, the number of reference cycles to power-on the MDLL is independent of the multiplication factor N.

For large values of C_{VCO} and small multiplication factor N, VCO's time constant τ

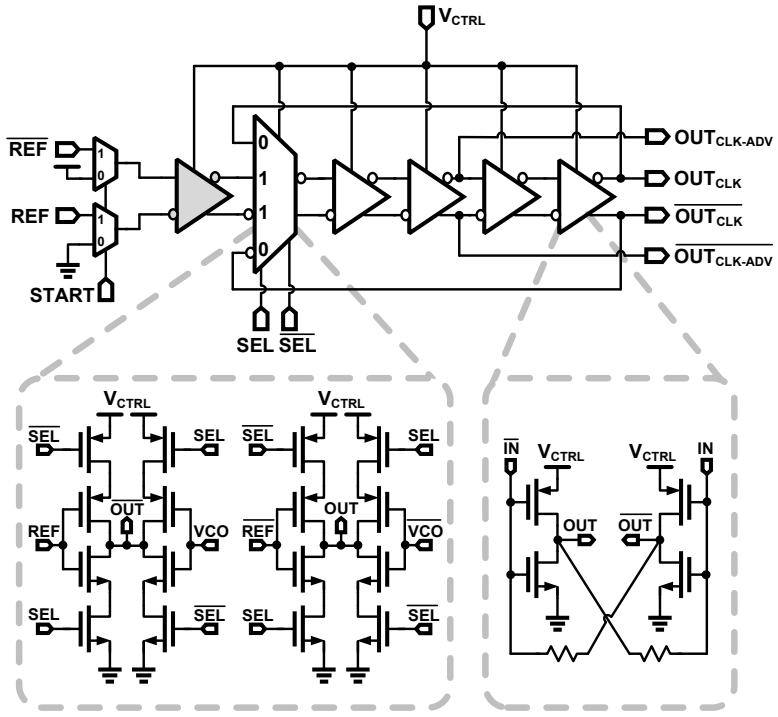


Figure 3.10: Schematic diagram of the voltage controlled oscillator.

($R_{VCO}C_{VCO}$) becomes comparable to the reference time period T_{REF}. Consequently, for initial few reference cycles, the V_{CTRL} node does not settle all the way to V_C at the end of N VCO cycles. As a result, in this case, the value of T_j depends on the multiplication factor N. Smaller N will have large T_j at the end of first few reference cycle. Therefore, an MDLL with a smaller multiplication factor N takes a few more reference cycles to power-on. However, in terms of absolute settling time, for a fixed VCO frequency, a smaller multiplication factor N corrects the MDLL's output phase more often and results in smaller power-on time.

3.4 Clock Multiplier Building Blocks

3.4.1 Voltage Controlled Oscillator (VCO)

A schematic diagram of VCO is shown in Fig. 3.10. It consists of five stages connected in a ring configuration. One of these five stages is an inverting multiplexer and the other four are cross-coupled inverters. The $OUT_{CLK-ADV}$ signal is tapped from the middle of the VCO.

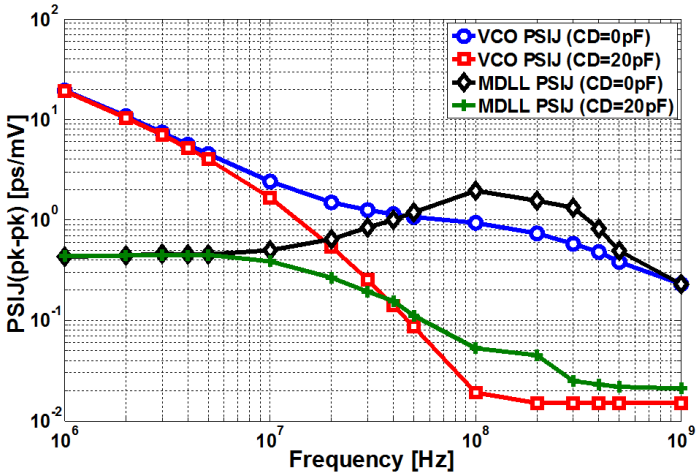


Figure 3.11: Simulated power supply induced jitter (PSIJ) of VCO (including DAC) and MDLL.

This signal is used to meet timing requirements in the edge replacement logic. The REF signal to the multiplexer is driven by a VCO delay cell, shown as a shaded cell in Fig. 3.10. Passing the REF signal through the VCO buffer matches the rise time of the REF edge with the OUT_{CLK} edge resulting in a lower reference spur at the output. The choice of five stages in the oscillator was made carefully to achieve sharp rise and fall times, which helps in reducing deterministic jitter caused due to imperfect reference edge replacement. Resistive cross coupling on the multiplexer was avoided to reduce noise coupling from the OUT_{CLK} edge to the clean REF edge during the edge replacement operation. The choice of pseudo-differential stages was made to achieve a smaller self-induced ripple on the V_{CTRL} node, resulting in better jitter performance with a smaller decoupling capacitor. When simulated at 2.5GHz, the VCO consumes approximately 550μA from a 1.1V supply.

Power supply induced jitter (PSIJ) of the VCO (including DACs) and MDLL are a strong function of decoupling capacitor C_D on the V_{CTRL} node. The simulated $PSIJ_{pk-pk}$ value for C_D = 0pF and 20pF is shown in Fig. 3.11. At 100MHz sinusoidal supply disturbance, simulated $PSIJ_{pk-pk}$ of MDLL for C_D = 0pF and 20pF is 2ps/mV and 0.053ps/mV, respectively. At 1MHz sinusoidal supply disturbance, simulated $PSIJ_{pk-pk}$ of MDLL for C_D = 0pF and 20pF is 0.43ps/mV.

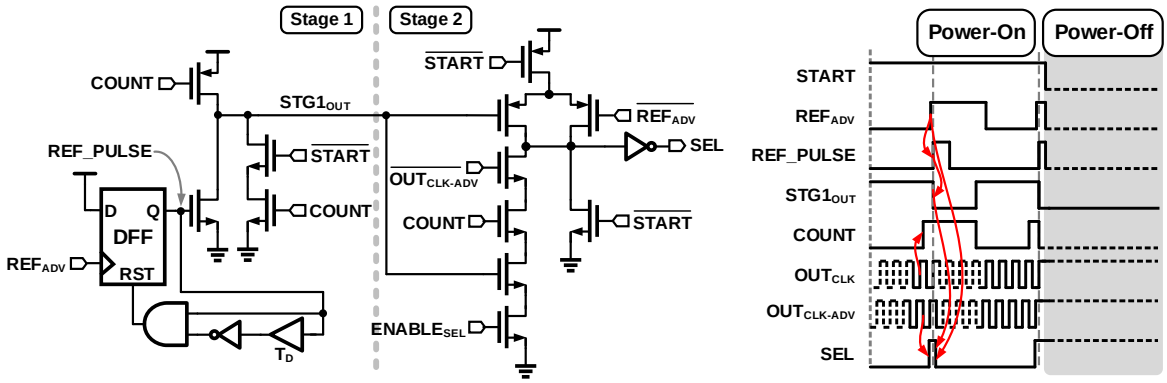


Figure 3.12: Schematic and timing diagram of the proposed edge replacement logic (ERL).

3.4.2 Edge Replacement Logic (ERL)

Edge replacement logic is responsible for generating a narrow pulse to pass the clean reference edge every N^{th} VCO cycle. The width of this pulse is typically $T_{VCO}/2$. Conventional select logic requires synchronous thermometric counter running at VCO frequency to generate periodic pulses of one VCO period width [32]. However, running a synchronous counter at VCO frequency results in large power dissipation. Moreover, the initial VCO frequency is required to be higher than $N*F_{REF}$, which limits this circuit [32] to be used for fast power-on applications where the VCO frequency is very close to $N * F_{REF}$ during power-on. During normal operation, the SEL signal must be de-asserted after the rising edge of REF signal and before the falling edge of the VCO output, and within time $T_{VCO}/4$ in the best case. The select logic in [36] avoids thermometric counter but suffers from $T_{REF\uparrow-SEL\downarrow}$ timing constraint, which is difficult to meet at higher VCO frequencies. In this work, the proposed ERL employ ripple counter to reduce power consumption and uses advanced reference signal to overcome the $T_{REF\uparrow-SEL\downarrow}$ timing constraint.

Figure 3.12 shows the schematic and timing diagram of the proposed ERL circuit. When the $COUNT$ signal is low, the output of the first stage, $STG1_{OUT}$ is pre-charged to logic high. After the completion of N VCO cycles, the $COUNT$ signal is asserted high. The SEL signal is asserted high on the falling edge of $\mathrm{OUT}_{CLK-ADV}$. The SEL signal opens up the oscillator and waits for the REF rising edge to pass. The REF_{ADV} signal is generated by tapping the REF signal before the delayed REF goes into the VCO. On the rising edge of

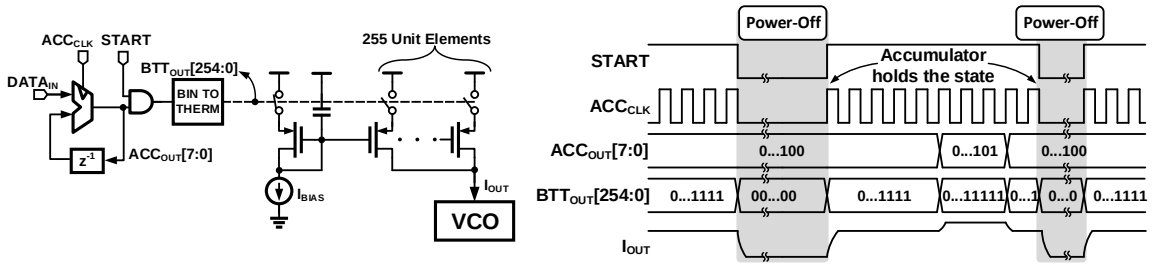


Figure 3.13: Schematic and timing diagram of the Nyquist-rate DAC.

the REF_{ADV}, the output of Stage 1 is discharged, and the SEL signal is de-asserted. The timing by which the REF_{ADV} signal must be advanced with respect to the REF signal is given by the following equation:

$$T_{REFADV\uparrow-REF\uparrow} = T_{REFADV\uparrow-SEL\downarrow} - T_{VCO/4} \tag{3.8}$$

where $T_{REFADV\uparrow-SEL\downarrow}$ is the time between the REF_{ADV} rising edge to the SEL falling edge.

3.4.3 DAC

Delta-sigma DACs followed by post filter offer a compact way to achieve high-resolution frequency control of the VCOs. However, a large time constant of the post-filter increases the frequency settling time. The proposed Nyquist-rate DAC and its timing diagram is shown in Fig. 3.13. The DAC is implemented using thermometer-coded current-mode architecture to ensure monotonicity and fast settling. Single-ended source switched PMOS current elements are used to minimize area. By employing current mode Nyquist-rate DACs, use of low bandwidth post filter is avoided, thereby achieving high bandwidth to rapidly set VCO frequency during power-on/off events. When the system is powered-off, the clock to the accumulator is gated, and the accumulator holds its state. De-asserting the $START$ signal causes the output of binary to thermometric logic to go down to zero, which shuts down the DAC. When the system is powered-on, the previous state of the DAC is restored, and I_{OUT} quickly reaches the desired value.

The choice of DAC's resolution and frequency tuning range is governed by tolerable fre-

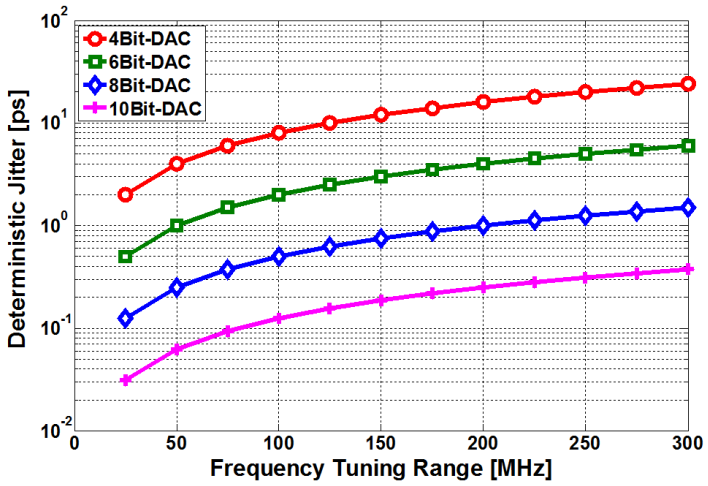


Figure 3.14: Simulated deterministic jitter as a function of frequency tuning range for $N = 8$ and $F_{VCO} = 2.5$GHz.

quency quantization error. Frequency quantization error results in the accumulation of VCO phase for one reference cycle, which results in deterministic jitter and consequently reference spurs. For a given DAC resolution and frequency tuning range, deterministic jitter ϕ_{DJ} can be estimated mathematically as follows:

$$\phi_{DJ} = \frac{F_{TUNE}.N.T_{VCO}}{2^{DAC-BIT}.F_{VCO}} \tag{3.9}$$

where F_{TUNE} is the frequency tuning range, N is the frequency multiplication factor, $DAC-BIT$ is the size of DAC, F_{VCO} is the VCO frequency, and T_{VCO} is the VCO period. Using (3.9), the plot of deterministic jitter as a function of frequency tuning range for various DAC sizes is shown in Fig. 3.14. Increasing the DAC resolution on the one hand reduces the frequency quantization error, and on the other hand it increases the area and parasitic capacitance on the V_{CTRL} (virtual supply node of VCO), which eventually increases the power-on time of MDLL. Design of fast power-on MDLL with wide frequency tuning range VCO remains a challenging problem. In the proposed architecture, an 8 bit integral path DAC provides up to 125MHz of tuning range.

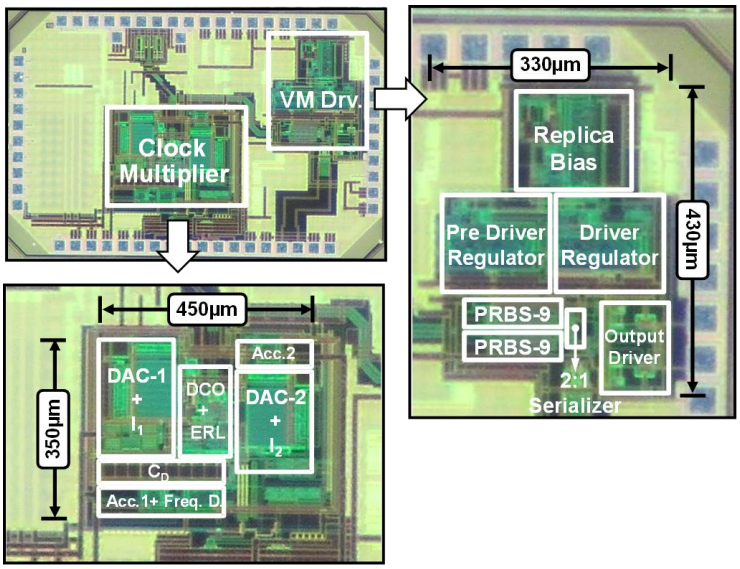


Figure 3.15: Die micrograph of the proposed transmitter.

3.5 Measurement Results

The die micrograph of the prototype transmitter, implemented in a 90nm CMOS process, is shown Fig. 3.15. It occupies an active area of 0.3mm^2 of which the voltage mode driver occupies 0.14mm^2 (330μm x 430μm) and the MDLL occupies 0.16mm^2 (450μm x 350μm). The chip is packaged in a 48-pin QFN plastic package.

Measurement setups to measure the transmitter in an always-on, and in rapid-on/off mode are shown in Fig. 3.16 and Fig. 3.17, respectively. The reference clock for the clock multiplier is generated from an arbitrary waveform generator (Tektronix AWG7122B), and the output spectrum and jitter of the MDLL is measured on a spectrum analyzer (Tektronix RSA3308B) and communication signal analyzer (Tektronix CSA8200), respectively. Reference is used as a trigger signal for Tektronix CSA8200. The transmitter output eye is measured on Tektronix CSA8200 with reference as a trigger signal. The transmitter is powered using a set of linear voltage regulators manufactured by the Analog Devices (part# ADP123).

In the case of rapid-on/off measurements, the transmitter is power cycled using a $START$ signal, which is generated from the AWG7122B, and the same $START$ signal is used as a trigger to capture the output transient of the transmitter on a communication signal analyzer (Tektronix CSA8200). The MDLL's settling behavior (in this case, period jitter) is measured

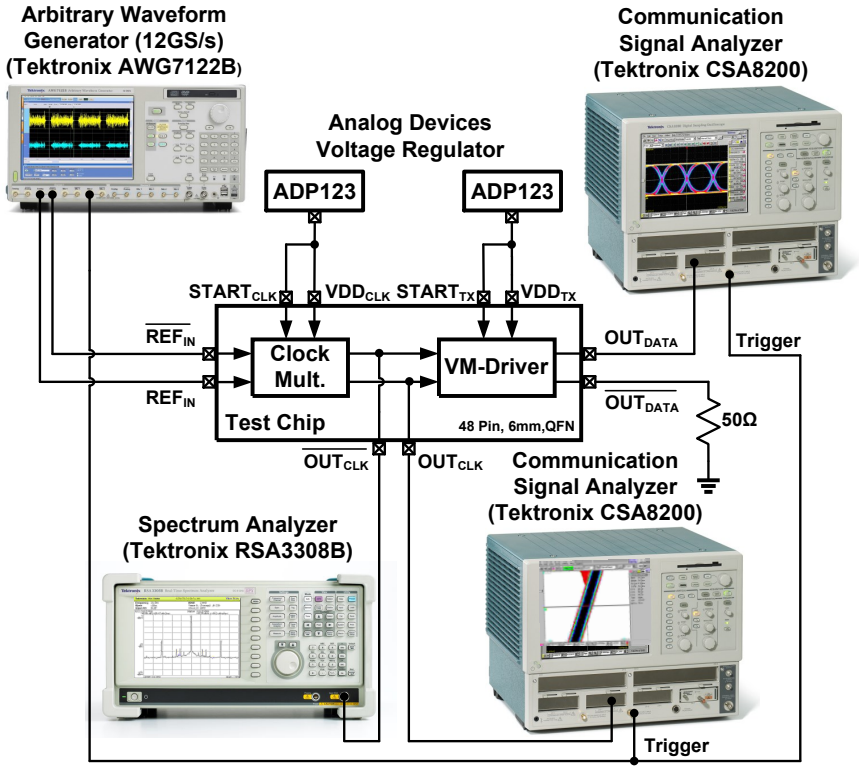


Figure 3.16: Measurement setup for always-on measurements.

by capturing the OUT_{CLK} signal on an oscilloscope (Tektronix TDS7404).

A wide range of measurements were conducted to quantify the trade-offs between performance and power-on time. For all the measurements, a multiplication ratio of 8, the reference frequency of 312.5MHz and a 0pF decoupling capacitor (C_D) for MDLL were used, unless otherwise stated. At 5Gb/s, the transmitter consumes 4.8mW (excluding PRBS generators) with the voltage mode driver consuming 2.6mW from a 1V supply and the MDLL consuming 2.2mW from a 1.1V supply. Figure 3.18 shows the on-state and off-state power break-up of the transmitter. In the power-off state the transmitter consumes 33μW of which 11μW is consumed by the voltage mode driver and 25μW by the MDLL. Off-state power in the voltage mode driver is largely due to leakage in digital circuits such as accumulators and multiplexers. In MDLL, out of the measured 2.2mW on-state power, 1.38mW is consumed in the digital logic, and the remaining 0.82mW is consumed in the DACs and the oscillator. In the off-state, out of measured 25μW, 17μW is consumed in bias circuits and leakage in

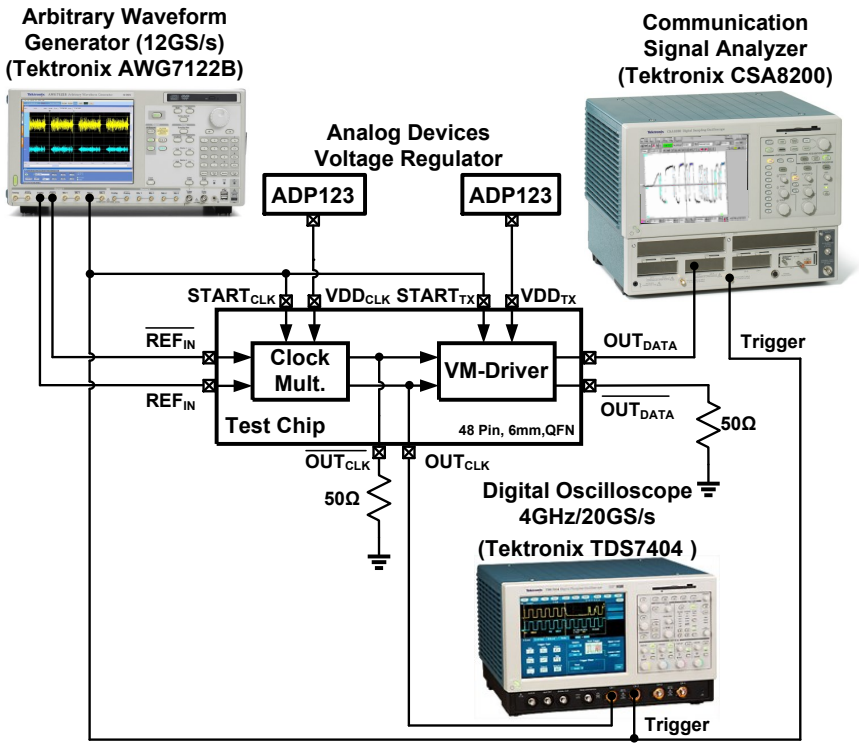


Figure 3.17: Measurement setup for on/off measurements.

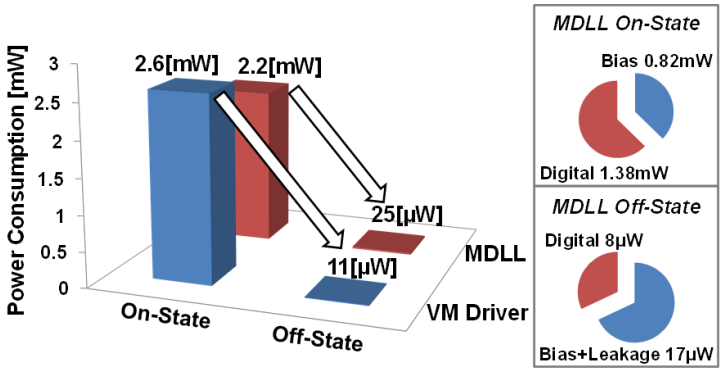


Figure 3.18: Measured power breakup of the proposed transmitter.

DAC's decoder logic, and 8μW is due to leakage in the rest of logic circuits.

Figure 3.19 shows the captured transient of 2.5GHz clock waveform, while power cycling the MDLL for a multiplication factor of 8(312.5MHz reference) and 16(156.25MHz reference). Figure 3.20 plots the measured peak period jitter versus power-on time. In both cases,

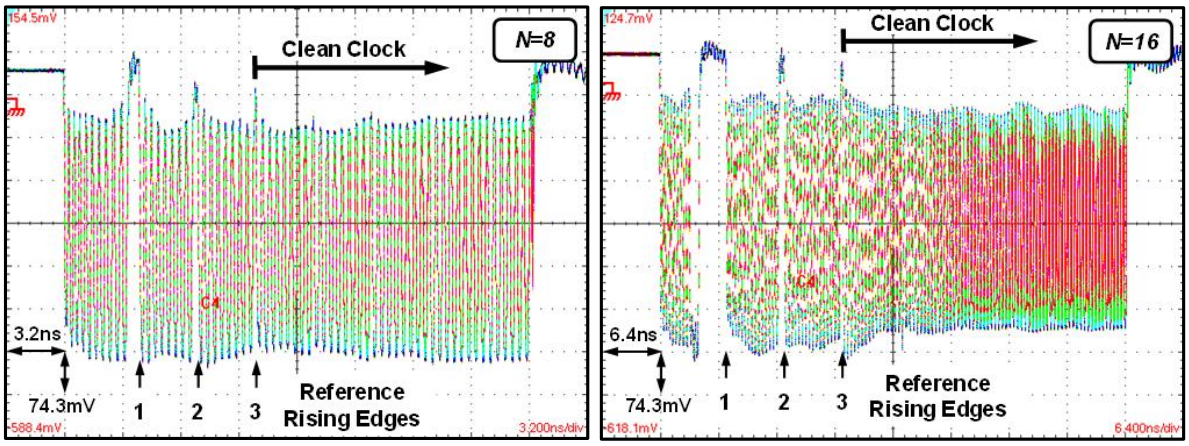


Figure 3.19: Measured power-on/off transient of the proposed MDLL for multiplication factors of 8 and 16.

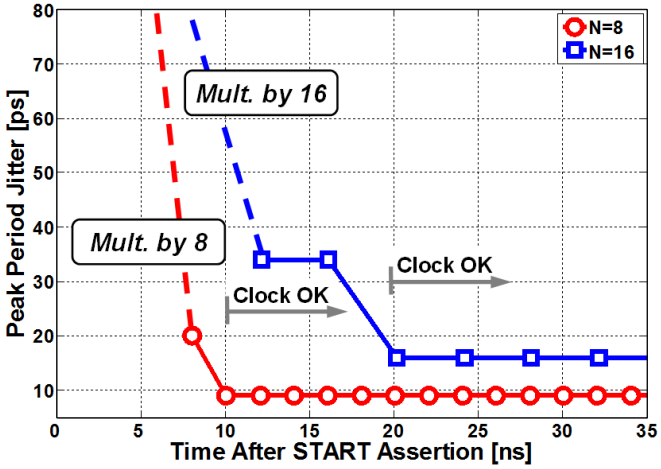


Figure 3.20: Measured period jitter of the proposed MDLL for multiplication factors of 8 and 16.

the MDLL locks in approximately three reference cycles. Mathematically, it was shown in Section 3.3 that a small time constant on the V_{CTRL} node makes settling time, in terms of reference cycles, to be independent of the multiplication factor N.

Figure 3.21 shows the captured $DATA_{OUT}$ and $START$ signals while power cycling the transmitter. The delay difference between the $START$ signal captured on the CSA8200 and the one which goes inside the chip is 1ns, as seen in the power-off event. The measured power-on time of the voltage mode driver is around 2ns and is dominated by the time needed to charge 20pF decoupling capacitors of the output driver and per-driver regulators. The

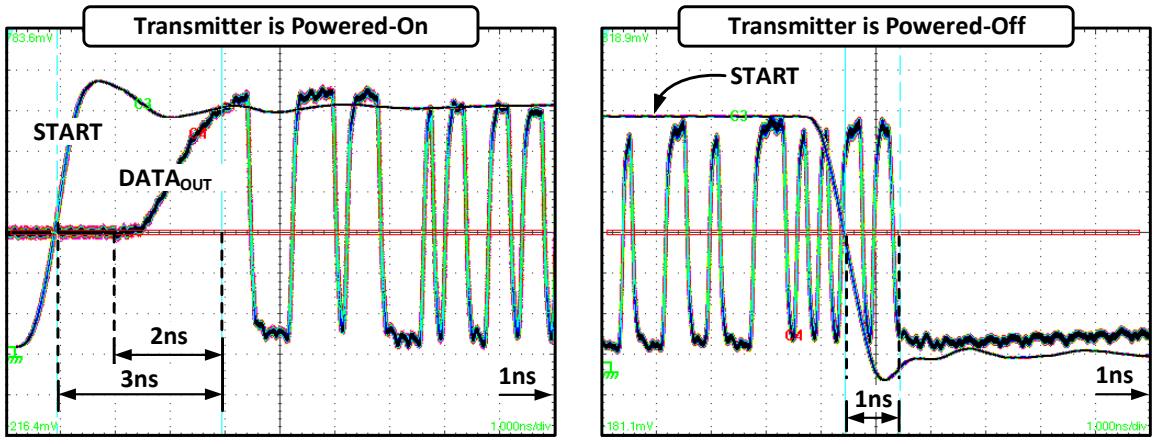


Figure 3.21: Measured power-on/off transient of the proposed transmitter.

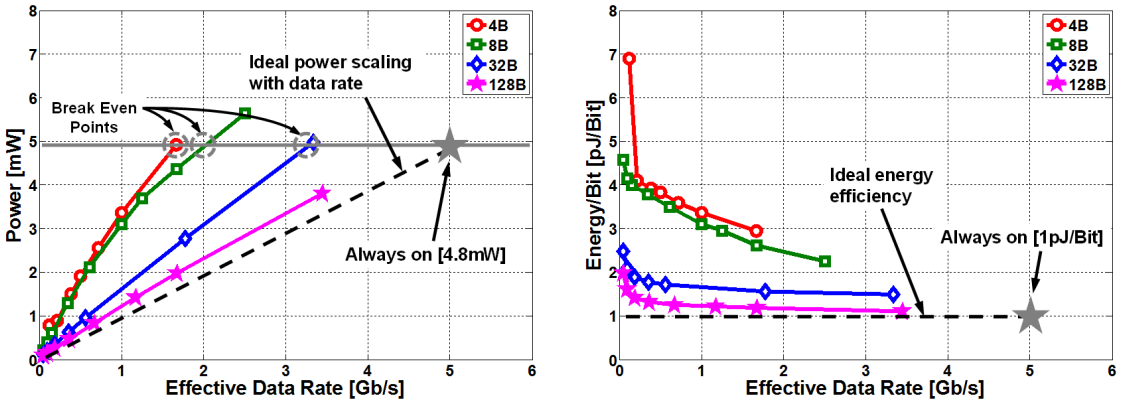


Figure 3.22: Measured power consumption and energy-per-bit of the proposed transmitter as a function of effective data rate for various burst lengths in bytes.

voltage mode driver thus does not limit the power-on time of the whole transmitter. The power-on time is limited by the MDLL's power-on time, which is 10ns. The measured energy overhead of power cycling is 44pJ of which 32pJ is consumed in the voltage mode driver and the remaining 12pJ in the MDLL. Charging and discharging of capacitors on V_{DRV} and V_{PRE} nodes (see Fig. 3.2) are the major contributors to this overhead.

Figure 3.22 plots the power consumption and energy efficiency of the transmitter versus effective data rate for different data burst lengths (in bytes). Ideally, the power consumption must scale linearly with the data rate, as shown by dashed line in the power consumption versus effective data rate plot. However, the power overhead due to power cycling and finite

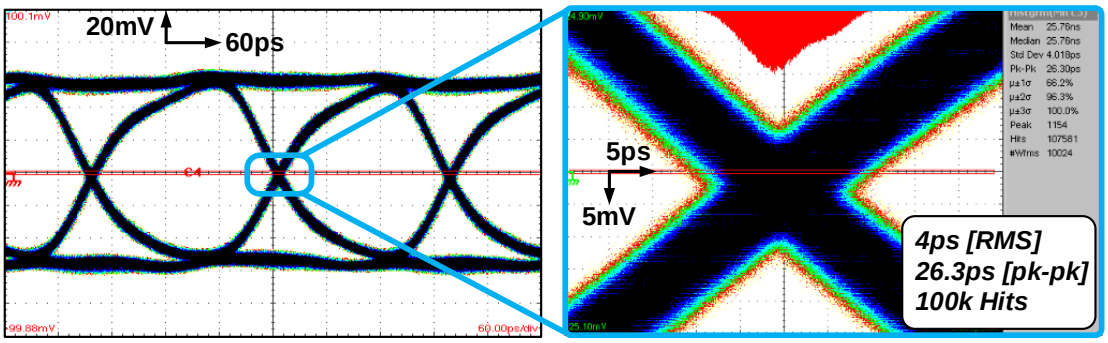


Figure 3.23: Measured eye diagram of the proposed transmitter at 5Gb/s with PRBS9 output data.

power-on time increases the slope of the power versus the effective data rate curve at smaller burst lengths (4 bytes). For longer burst lengths, the power overhead due to power cycling is a smaller portion of the total power consumed during data transmission. Therefore, energy proportional behavior, which is closer to the ideal case, is achieved. For 128 byte packet size, the power consumption varies from 4.8mW to 0.095mW (50x change) and the energy efficiency varies from 1pJ to 2pJ (2x change) when the effective data rate varies from 5Gb/s to 48Mb/s (100x change). The 32 byte packet size data burst reaches the break-even power point at 3.33Gb/s, and any increase in the bandwidth demand beyond this point must be met by keeping the transmitter in an always-on state.

Figure 3.23 shows the captured transmitter output eye diagram with the PRBS9 data. The differential output swing is $250mV_{ppd}$, and the measured long-term jitter is $4ps_{rms}$ and $26.3ps_{pk-pk}$ with 100k hits. Figure 3.24 shows the MDLL output phase noise plot at 2.5GHz. The measured phase noise at 1MHz offset is -116.9dBc/Hz and the jitter obtained by integrating phase noise from 3.125KHz to 100MHz is 752fs.

The trade-off between power-on time and jitter performance is measured using programmable capacitor bank C_D(see Fig. 3.6). Figure 3.25 shows the measured period jitter for different decoupling capacitor values. These measurements were conducted by enabling the capacitors one at a time while the MDLL is power cycled. As expected, a big decoupling capacitor increases the power-on time by increasing the time for the control voltage V_{CTRL} to settle. The measured settling time is 256ns for a 20pF capacitor and 10ns for 0pF capacitor.

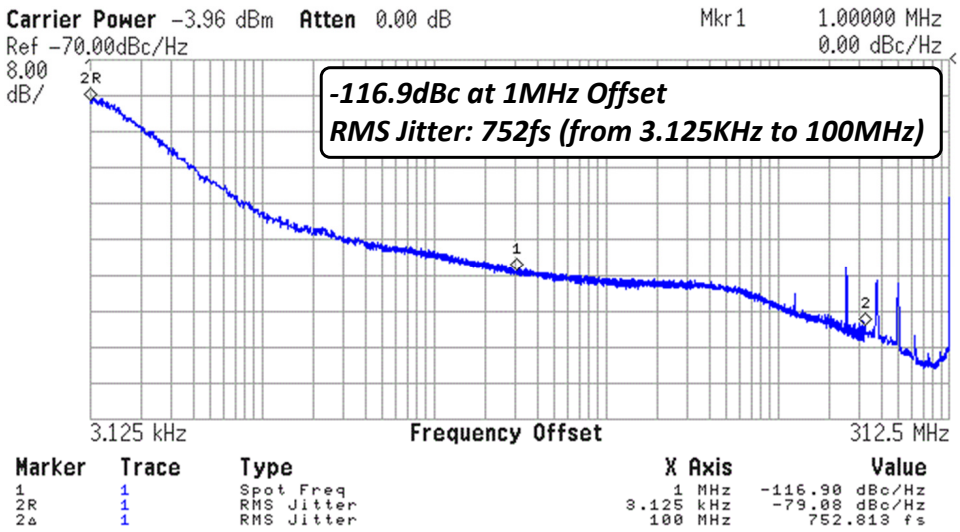


Figure 3.24: Measured phase noise spectrum of the proposed MDLL at 2.5GHz output frequency.

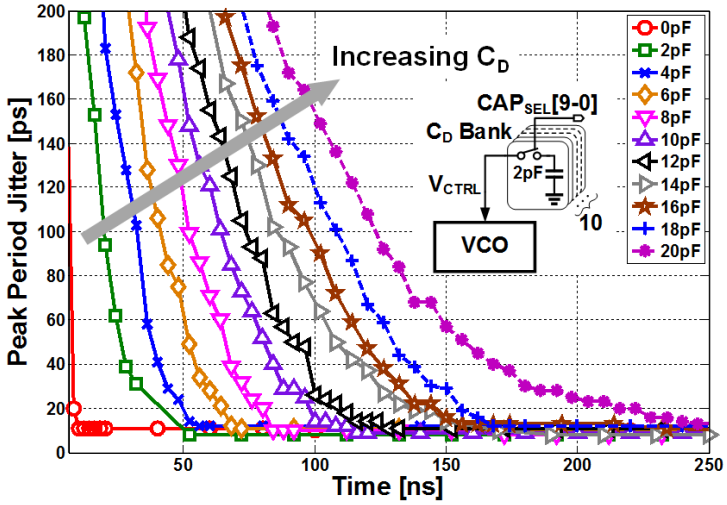


Figure 3.25: Measured peak period jitter as a function of time for different decoupling capacitor (C_D) settings.

Figure 3.26 shows the measured MDLL jitter performance for two extreme capacitor values. The measured long-term absolute jitter over 100k hits for a 20pF decoupling capacitor is $1.1ps_{rms}/10ps_{pk-pk}$, and for a 0pF capacitor is $2ps_{rms}/18.6ps_{pk-pk}$. A big decoupling capacitor filters the noise from current sources and supply thereby achieving superior performance. A big decoupling capacitor also helps in reducing reference spurs. Figure 3.27 shows the measured MDLL's output spectrum for two capacitor values.

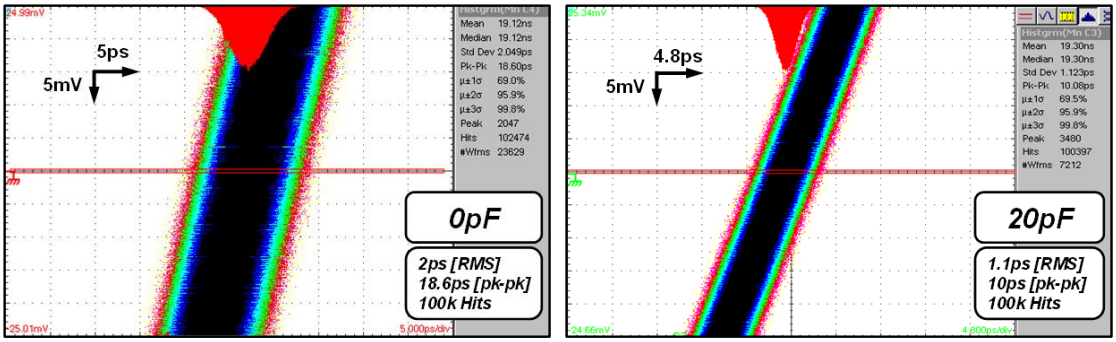


Figure 3.26: Measured long-term jitter histogram of the proposed MDLL for 0pF and 20pF decoupling capacitor cases.

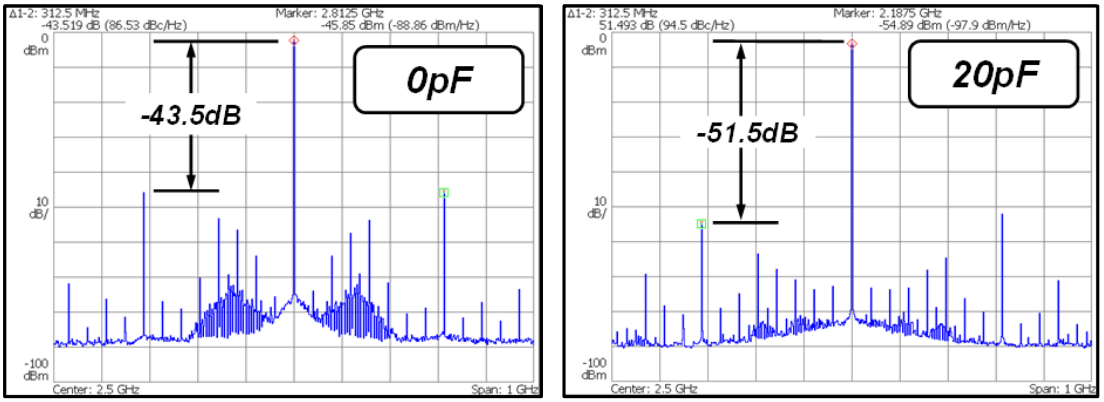


Figure 3.27: Measured spectrum of the proposed MDLL for 0pF and 20pF decoupling capacitor cases.

The measured reference spur for a decoupling capacitor of 20pF and 0pF is -51.5dB and -43.5dB, respectively. We believe use of common ground pins between the ripple counter, digital logic, and VCO is the main reason for this spur and the spurs appearing at subharmonic reference frequencies.

Energy proportional performance of the stand-alone MDLL is measured separately. Figure 3.28 shows the measured power consumption and energy-per-cycle versus utilization when the MDLL is power cycled at four different on/off periods. The power scales linearly with utilization. The average energy overhead of on-to-off and off-to-on transition is 12pJ. A non-zero y-intercept indicates finite turn-on time and non-zero off-state power. In a conventional multiplier, the energy-per-cycle increases at lower utilization. The proposed

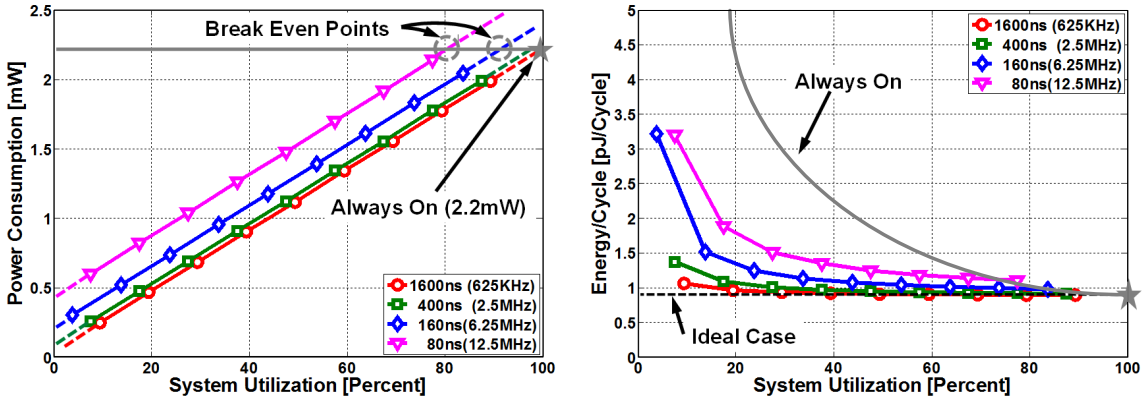


Figure 3.28: Measured MDLL power consumption and energy-per-cycle as a function of utilization for various power-cycling periods.

MDLL achieves almost constant energy-per-cycle when power cycled with a cycle time of 1600ns. For this case, the energy-per-cycle changes from 0.88pJ to 1pJ when the utilization changes from 100% to 9%. When MDLL is power cycled with a cycle time of 400ns, the energy-per-cycle changes from 0.88pJ to 1.4pJ when the utilization changes from 100% to 7.5%.

Table 3.1 compares the proposed transmitter with state-of-the-art designs. The proposed voltage mode driver compares favorably and achieves the smallest power-on time. The transmitter as a whole achieves the smallest power-on time in terms of reference cycles. Comparison of the proposed transmitter with prior-art is made using normalized energy-per-bit versus effective data rate and normalized power versus effective data rate plots. Burst length of 8 bytes is used in this comparison. Comparison plots were obtained based on the power-on time, off-state power, and on-state power of the prior-art and proposed transmitter. Normalization of energy-per-bit versus effective data rate was done such that the proposed transmitter and prior-art have unity energy efficiency at their respective peak data rates. Normalization of power versus effective data rate was done such that the proposed transmitter and prior-art have unity power at their respective peak data rates.

Figure 3.29 shows the comparison plot of normalized power versus the effective data rate and energy-per-bit versus effective data rate. At an effective data rate of 10Mb/s, normalized

Table 3.1: Performance Comparison of the Proposed Fast-On Transmitter with State-of-the-Art Designs

	This Work	[14]VLSI'11	[15]JSSC'10
Technology	**90nm**	40nm	40nm
Supply[V]	**1 (VM Driver)**	N/A	1.1
	1.1 (MDLL)		
Peak data rate[Gb/s]	**5**	2.5-5.6	2.7-4.3
Power-on time[ns]	**10**	8	241.8
Power-on time (Reference Cycles)	**3**	5.6	130
Ref. freq.[MHz]	**312.5**	700	537.5
On-state power[mW]	**4.8***	13.4**	14.2***
Off-state power	**36μW**	0mW	50μW†
Output swing[mV]	**250(Diff$_{pk-pk}$)**	N/A	200(Diff$_{pk-pk}$)

† 0.4mW for 8 channels reported
*Output driver and clock power at 5Gb/s
**Ouput driver, clock and receiver power at 5.6Gb/s
***Ouput driver, clock and receiver power at 4.3Gb/s

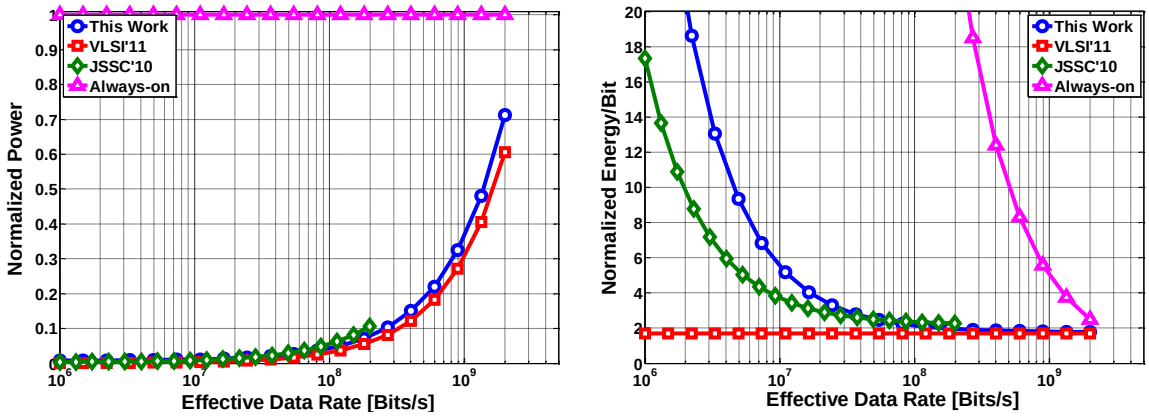


Figure 3.29: Normalized power consumption and energy-per-bit of the proposed transmitter and prior-art as a function of effective data rate for 8 byte burst length.

energy-per-bit of the proposed transmitter, [15], and [14][1] is approximately 5.2, 3.6 and 1.7

[1]The reason behind a flat normalized energy-per-bit versus effective data rate plot (see Fig. 3.29) for [14] even at relatively low data rates is due to 0mW off-state power reported in [14]. However, a non-zero (even few microwatts) off-state power could increase the energy-per-bit at lower effective data rates as seen in the energy-per-bit versus data rate plot in [14].

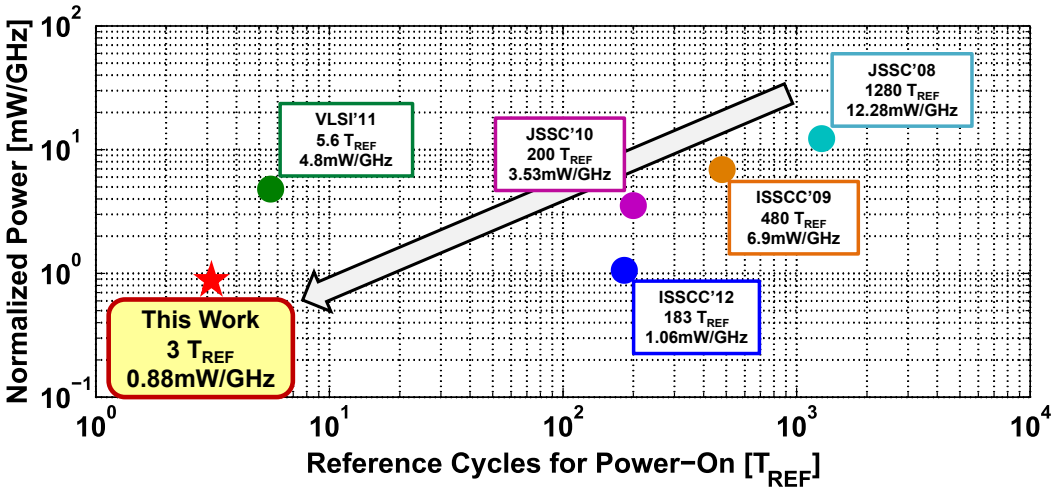


Figure 3.30: Visual comparison of the proposed MDLL with the state-of-the-art fast power-on frequency multipliers.

respectively. Table 3.2 compares the proposed MDLL with the state-of-the-art fast power-on frequency multipliers, and a visual comparison is shown in Fig. 3.30. The proposed MDLL achieves smallest power-on time (three reference cycles) and competitive power efficiency (0.88mW/GHz).

3.6 Conclusion

Despite being energy efficient at their peak data rates, conventional links suffer from efficiency degradation at lower link utilization. Power cycling technique is employed to achieve constant energy-per-bit operation across all utilization levels of a link. In this work, a fast rapid-on/off transmitter architecture, which demonstrates energy proportional operation over wide variations of link utilization was presented. The transmitter architecture combines architectural and circuit design techniques to achieves fast power-on lock capability in the voltage mode output driver by using a fast-digital regulator, and in the MDLL based clock multiplier by accurate frequency pre-setting and instantaneous phase acquisition. An improved edge replacement logic circuit for the MDLL was presented to ease timing requirements. The prototype fast power-on lock transmitter was fabricated in 90nm CMOS

technology and occupies an active die area of 0.3mm^2. The proposed rapid-on/off transmitter architecture achieves 10ns total power-on time, which is limited by the clock multiplier, and consumes 4.8mW/36μW on/off-state power from 1.1V supply. The voltage mode driver achieves power-on time of only 2ns, and the clock multiplier achieves a power-on lock time of 10ns. The transmitter achieves 100x effective data rate scaling (5Gb/s-0.048Gb/s), while scaling the power and energy efficiency by only 50x(4.8mW-0.095mW) and 2x(1-2pJ/Bit), respectively.

Table 3.2: Performance Comparison of the Proposed Fast-On Clock Multiplier with State-of-the-Art Designs

	This Work	[21]VLSI'13	[31]CICC'12	[14]VLSI'11	[26]ISSCC'12	[15]JSSC'10
Technology	**90nm**	40nm	65nm	40nm	22nm	40nm
Supply[V]	**1.1**	N/A	1.1	N/A	1	1.1
Output frequency[GHz]	**2.5**	25	2.3-4	2.8	3.2	4.3
Reference fequency[MHz]	**312.5**	390	790†	700	100	537.5
Jitter long-term [rms/pp] [ps]	**2/18.6(0pF)** **1.1/10(20pF)**	N/A	N/A	N/A	6/N/A	N/A
Power efficiency[mW/GHz]	**0.88**	2.56	30.4†	4.8*	1.06	N/A
Power[mW]	**2.2**	64	96†	13.44	3.4	N/A
Power-On time[s]	**10ns**	100ns	12.65ns†	8ns◇	1.83μs‡	241.8ns
Power-On time [Reference cycles]	**3**	40	10	5.6	183	130
Area[mm^2]	**0.16**	0.1	0.149	N/A	0.017	N/A
Architecture	**MDLL**	PLL	MILO	MILO	PLL	PLL

† Results reported at 3.16GHz
* Individual MILO power is not reported in [14]
◇ Power-On time of the transmitter including MILO
‡ Power-on time is reported at 3GHz

CHAPTER 4

A 7GHz FAST POWER-ON-LOCK PLL FOR ENERGY PROPORTIONAL LINKS

In this chapter, a 7GHz fast power-on-lock LC-PLL is presented. Fabricated in a 65nm CMOS process, the prototype PLL achieved 1ns power-on lock time. Operating from 1V supply, proposed PLL achieves on and off-state power of 4.8mW and 41.6μW, respectively. Integrated jitter in always-on mode is 435fs$_{\text{rms}}$ while multiplying 109.375MHz reference by 64x. It occupies an active area of 0.22mm^2.

This chapter is organized as follows. Section 4.1 discusses the limitations of the MDLL based clock multiplier and motivates the reader toward the need for fast power-on-lock PLL. Evolution of conventional PLL to fast power-on-lock PLL is discussed in Section 4.2. Section 4.3 presents the proposed PLL architecture. Section 4.4 discusses the key building blocks schematic and architecture used in the proposed PLL. PLL power-on modes for the transceiver are discussed in Section 4.5. Section 4.6 presents the measured results and Section 4.7 concludes this chapter.

4.1 MDLL Limitations and Motivation for Fast Power-on-Lock LC-PLL

The MDLL based fast power-on-lock clock multiplier as discussed in Chapter 3 suffers from certain limitations, which could hinder large-scale adoption of rapid-on/off techniques in high-speed links.

The first limitation comes from the fact that MDLL technique is limited to ring oscillators. Ring oscillators have poor phase noise compared to LC based oscillators, and for that reason, oscillators used in the wireless and wireline (beyond 28Gb/s) are primarily LC based.

The second limitation comes from the very basic principle of MDLL i.e. generating a

narrow pulse, which opens up the oscillator to pass a clean reference edge. Sharp rise and fall times of this pulse are necessary for a clean selection of the reference edge. The technology node adds constraints on the minimum width of the pulse generated by the edge replacement logic and rise/fall time of the reference edge, which will pass though the oscillator. Consequently, this limits the maximum achievable MDLL oscillation frequency. In the present literature, 2.5GHz and 4GHz MDLL have been demonstrated [17, 18] using 90nm CMOS technology. Fine technology nodes (below 22nm) may help to overcome the rise/fall time limitations.

During long power-off, the die temperature could change and during on/off transient, the supply rails could witness large droops. Compared to the LC oscillators, ring oscillators are more sensitive to supply and temperature variations (at least 10x or more). MDLL, in particular, is more sensitive to the oscillation frequency variations. High sensitivity is due to the fact that MDLL could easily lose lock if the MDLL oscillates slower than the desired frequency.

Finally, the MDLL power-on-lock time is a function of reference time periods. So far in the literature, power-on time of three reference cycles [17, 18] has been reported. The clean reference clock is usually derived from the crystal, and its frequency is of the order of 100MHz. This results in power-on time of approximately 30ns. If a high-frequency reference is provided to the MDLL (as in the case of some wireline links), then the power consumption of the reference PLL, which is kept always-on, must be accounted for in the off-state power of the link. Large off-state power degrades the energy efficiency of the link at lower link utilization.

Because of all these limitations of the MDLL based clock multiplier, a rapid-on/off PLL is proposed with a power-on-lock time of 1ns. The power-on lock time of the proposed PLL is independent of the reference frequency used. Although the rapid-on/off PLL concept is demonstrated with an LC oscillator oscillating at 7GHz, the proposed idea is independent of the type of oscillator used. Power-on-lock time in the proposed PLL is independent of the LC oscillation frequency, so even a PLL designed for mm-wave applications can use the same technique. This key advantage comes from the fact that the proposed rapid-on/off technique operates in the reference frequency domain, instead of the VCO frequency domain.

4.2 Fast Power-On LC-PLL Evolution

The proposed Type-II LC-PLL is based on the conventional hybrid PLL architecture shown in Fig. 4.1(a). The proportional control is implemented in the analog domain by driving the oscillator directly with UP/DN signals generated by the PFD. Integral control is realized in the digital domain by detecting the sign of the phase error at the output of PFD and driving the oscillator with integrated phase error provided by the digital accumulator. Lock time, defined as the time needed to achieve phase lock (assuming frequency error is zero), is an important consideration in the design of the PLL. Because hybrid PLL exhibits linear loop dynamics, its lock time is dictated by the loop bandwidth and the initial phase error between Φ_{REF} and Φ_{FB} ($\Phi_{\mathrm{ERROR}} = \Phi_{\mathrm{REF}} - \Phi_{\mathrm{FB}}$). While it is possible to reduce lock time by increasing bandwidth, reference clock frequency, $\mathrm{F_{REF}}$ sets an upper limit on the maximum PLL bandwidth to about $\mathrm{F_{REF}}/10$ for stability reasons [20]. Gear shifting techniques can alleviate this trade-off [41], but the lock time is still of the order of several microseconds. Oversampling the output of feedback divider or the use of TDC can achieve fast phase locking [42, 43], but it results in large jitter, which is unacceptable for high-speed wireline applications. An alternate approach to reducing lock time is to make the initial phase error to be zero, so that the loop starts in the locked condition, independent of PLL bandwidth. In this work, we seek to explore this approach to reduce PLL lock time. To this end, we will first evaluate the sources of initial phase error and present techniques to make the error zero.

There are three main sources of initial phase error as depicted in the timing diagram of Fig. 4.1(a). First, the initial VCO output phase ($\Delta\Phi_{\mathrm{VCO}}$) is unknown as it depends on the thermal noise dependent start-up profile of the oscillator. Second, the initial state of the feedback divider ($\Delta\Phi_{\mathrm{IC\text{-}DIV}}$) is unknown as it depends on the state in which it was powered off and leakage during the off period (if dynamic flops are used). Third, delay in the feedback path ($\Delta\Phi_{\mathrm{DEL}}$) is unknown because it depends on layout parasitics and is also sensitive to process variations.

A conventional LC-tank builds up oscillations by amplifying thermal noise voltage. The start-up time of the oscillator depends on the initial thermal noise amplitude and is of

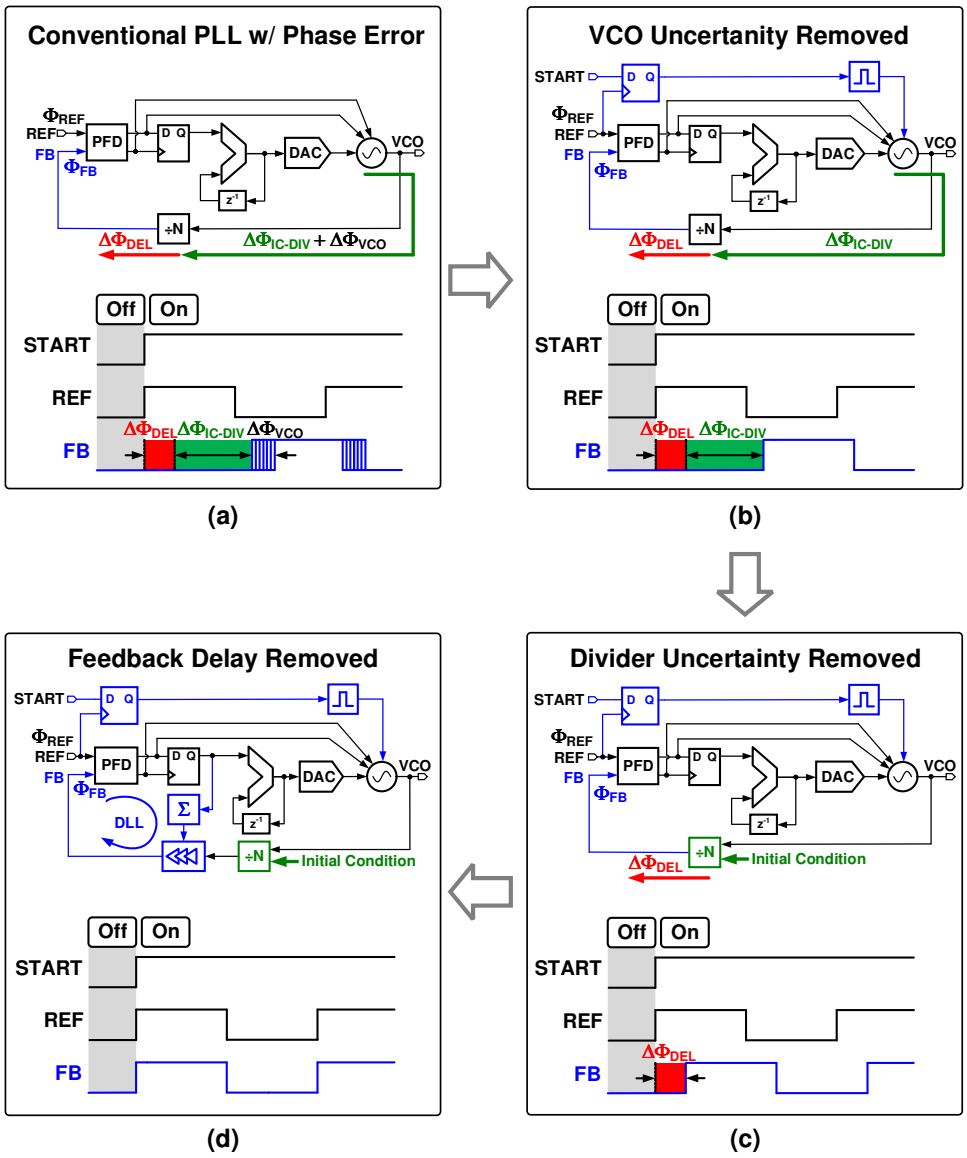


Figure 4.1: Evolution of a conventional PLL into a fast power-on-lock PLL. (a) Conventional PLL with random initial phase error. (b) PLL with fixed initial phase error. (c) PLL with fixed initial phase error of max one VCO time period. (d) PLL with zero initial phase error.

the order of several nanoseconds. The startup time can be reduced by providing an initial condition to the LC-tank [44]. Mathematically, amplitude build-up phenomenon and startup time can be analyzed with the help of the Van der Pol equation. An approximate solution to the Van der Pol equation is:

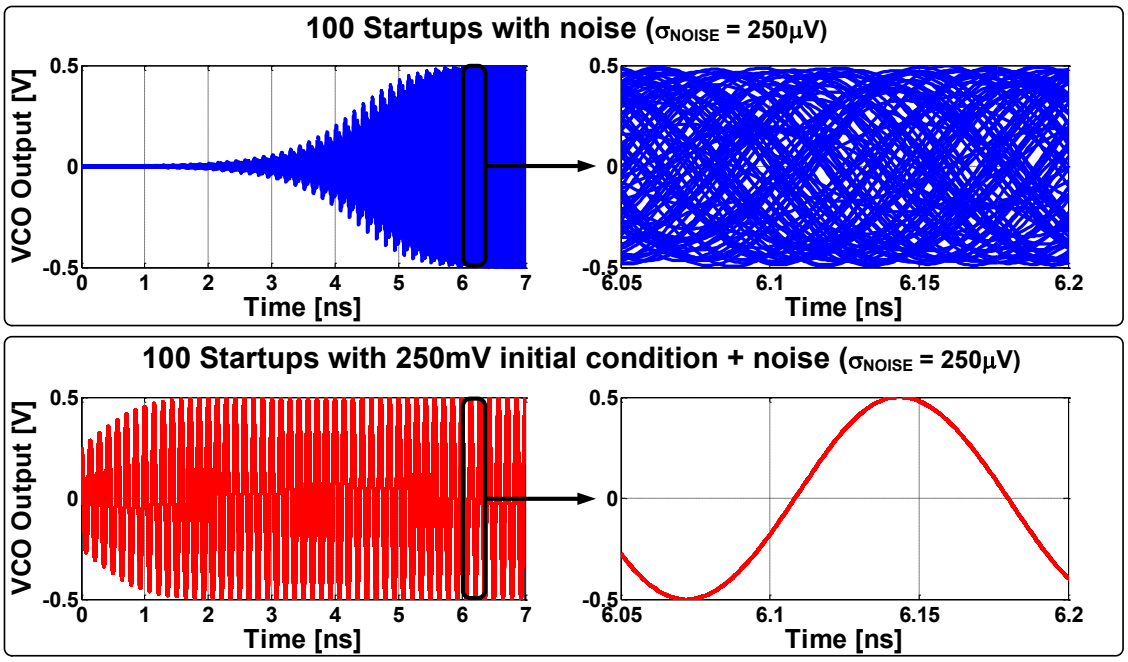


Figure 4.2: Matlab simulation of the Van der Pol equation solution in the presence of noise, with and without initial condition.

$$v(t) \approx \frac{2v_o}{\sqrt{1+\left(\left(\frac{2v_o}{v(0)}\right)^2-1\right)e^{-\epsilon\omega t}}}\cos(\omega t-\phi) \tag{4.1}$$

where v(t) is the output voltage of tank, v_o represents the output amplitude, v(0) is the initial condition, ω is the natural frequency of oscillator, ϵ is a damping factor and ϕ is the oscillator phase.

Based on the solution of the Van der Pol equation, it was observed that if the initial condition is fixed for every power-on event, then the output phase trajectory of an oscillator is deterministic, as shown in Fig. 4.2.

In this PLL, the initial condition is given to the oscillator in the form of a narrow pulse injected into the oscillator. This pulse is generated from the START signal and has a known phase relation to the phase of the reference clock, as shown in Fig. 4.1(b).

While using the initial condition removes the uncertainty in the oscillator output phase, $\Delta\Phi_{VCO}$, initial feedback divider state, and delay in the feedback path, $\Delta\Phi_{DEL}$ cause Φ_{FB}

to be a fixed offset from Φ_{REF}. Therefore, this phase offset must be canceled to achieve instantaneous phase locking. A simple digital delay locked loop (DLL) in which the feedback clock is appropriately tuned such that its phase is aligned to the reference phase can be used for this purpose. Because the phase offset can be as large as one reference time period (≈10ns), a 14-bit accurate delay line is needed to keep the quantization error to within 1ps. The design of such a wide range and high-resolution delay line is difficult, especially in a 65nm CMOS process that has an FO4 delay of approximately 16ps. To alleviate this requirement, we propose use of the feedback divider to first reduce the phase offset to be within one VCO period and then use a 7bit digitally controlled delay line with a range spanning approximately 250ps (≈1.7x VCO period) to correct the residual offset.

To illustrate how the divide-by-64 feedback divider can provide programmable delay, we can treat it like a 64-state finite state machine clocked at the VCO frequency. FB output is asserted high after reaching the 64^{th} state. If the divider is powered-on in the 1^{st} state, then the first positive edge of the FB clock is asserted high after a delay of 64 VCO clock periods. In general, if the divider is powered-on in the N^{th} state, then the first FB clock edge occurs after 65-N VCO clock cycles. Therefore, by setting the initial state of the divider, the FB clock can be delayed in steps of VCO period, thereby making the unknown phase difference between Φ_{REF} and Φ_{FB} to be within one VCO period, as shown in Fig. 4.1(c). In this PLL, the optimal initial state of the divider is set based on simulations.

The remaining unknown phase was compensated using a delay locked loop (DLL) (see Fig. 4.1(d)). Thanks to the coarse delay adjustment provided by the divider, the DLL has to cover a range of only one VCO period. This unknown phase also includes the unknown delay in the pulse generation path, and residual frequency error even after precisely setting the oscillator frequency. By accumulating the sign of the phase error between Φ_{REF} and Φ_{FB} measured immediately after a power-on event, the DLL shifts Φ_{FB} by one LSB of the digitally controlled delay line and forces $\Phi_{\mathrm{REF}} - \Phi_{\mathrm{FB}}$ to zero after several power-on events. The DLL is updated on the falling edge of $\mathrm{START}_{\mathrm{LCH}}$ after stopping the PLL. As a result, the DLL has no impact on the PLL loop dynamics. A graphical representation of phase setting versus time of the proposed PLL, getting evolved from a conventional PLL, is shown in Fig. 4.3.

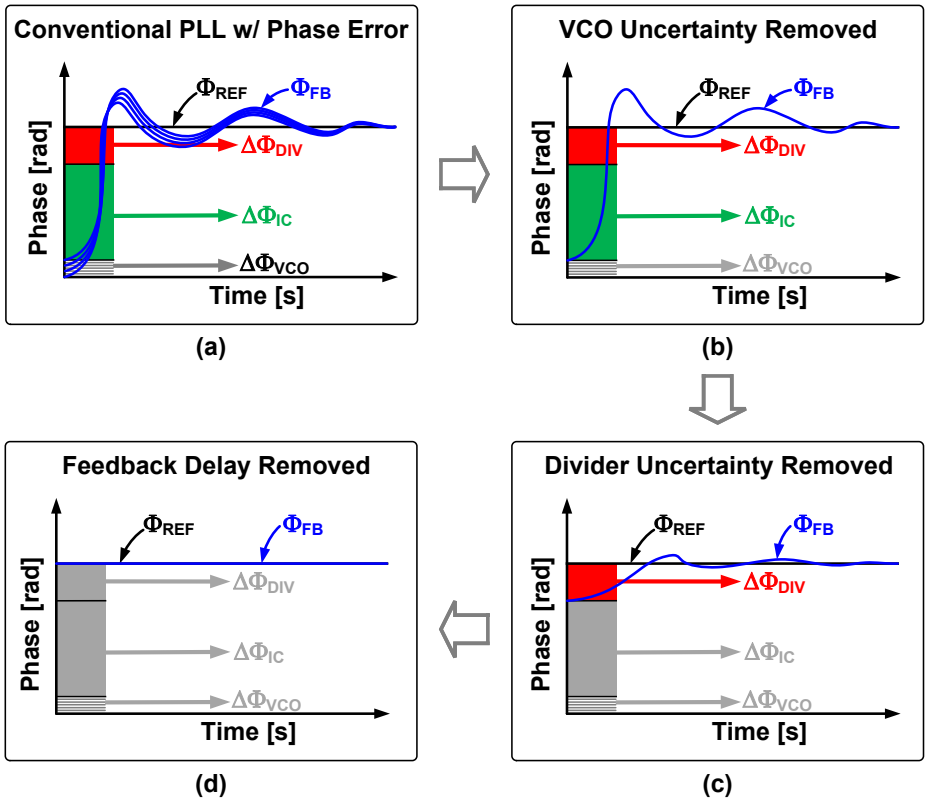


Figure 4.3: Evolution of a conventional PLL into a fast power-on-lock PLL based on output phase settling. (a) Conventional PLL phase with random initial phase error. (b) PLL phase with fixed initial phase error. (c) PLL phase with fixed initial phase error of max one VCO time period. (d) PLL phase with zero initial phase error.

4.3 Complete PLL Architecture

The proposed PLL architecture along with the timing diagram of phase calibration logic is shown in Fig. 4.4. Registers in the integral path are clocked with REF while registers in the DLL path are clocked with $\text{START}_{\text{LCH}}$. The PLL multiplies 109.375MHz reference clock by 64 and generates 7GHz output clock. It employs a hybrid architecture [45] in which the proportional path is implemented in the analog domain and integral path in the digital domain. It can be reconfigured to operate in a bang-bang mode, where only the sign of the phase error is used in the proportional control path. The 8-bit integral path accumulator output, which acts as the digital frequency control word is stored during the off-state and restored back on power-on to ensure that the PLL starts in a frequency-locked condition.

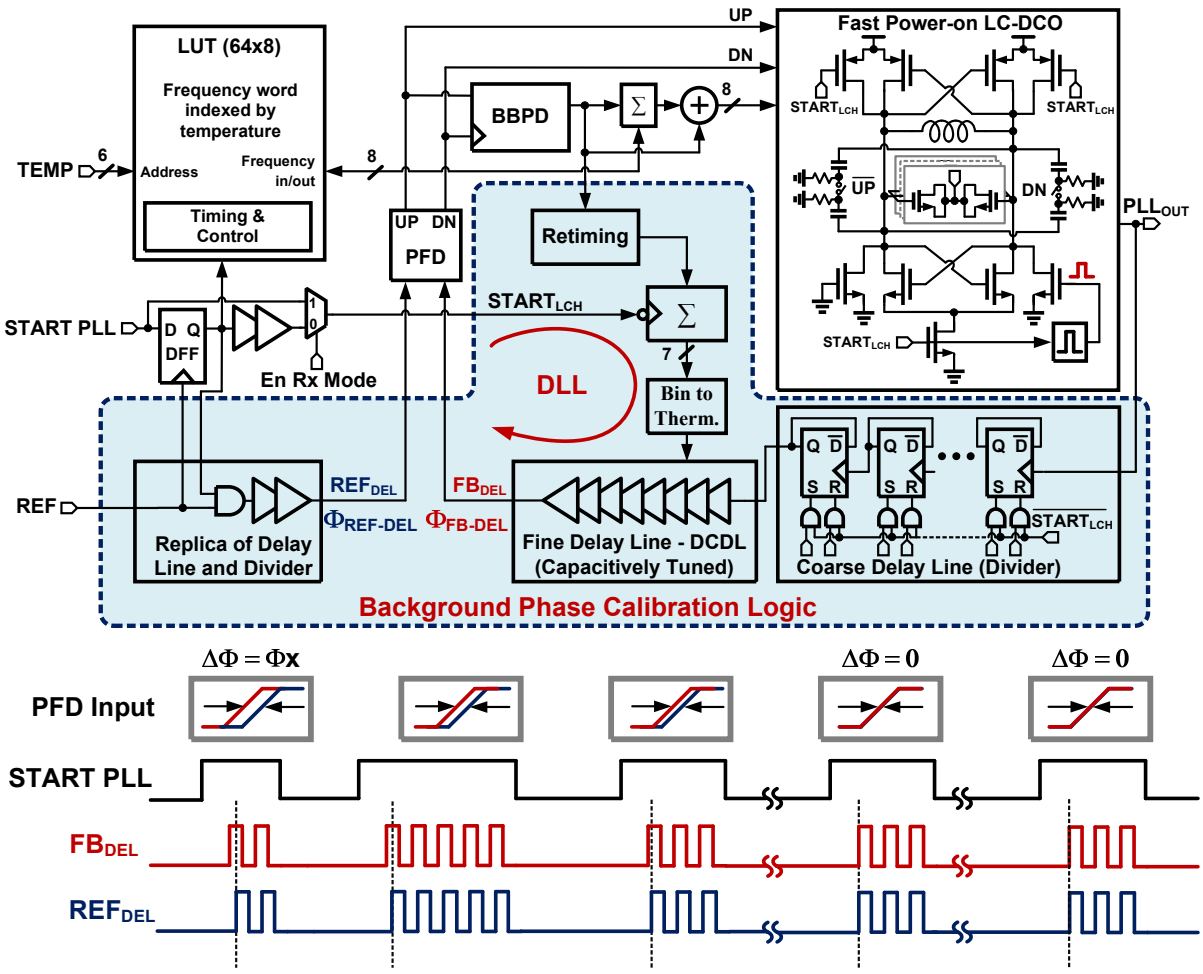


Figure 4.4: Proposed fast power-on-lock LC-PLL architecture and phase calibration timing diagram.

However, temperature drift during long off-periods may cause the oscillator to start at a different frequency, and the resulting frequency error may increase phase lock time of the PLL. To mitigate this, a lookup table (LUT) based temperature compensation scheme is used, as shown in Fig. 4.5.

The LUT contains the frequency control word as a function of temperature, needed to ensure 7GHz free-running frequency. Using the die temperature measured by the integrated temperature sensor, the corresponding digital frequency control word is read from the 64 x 8

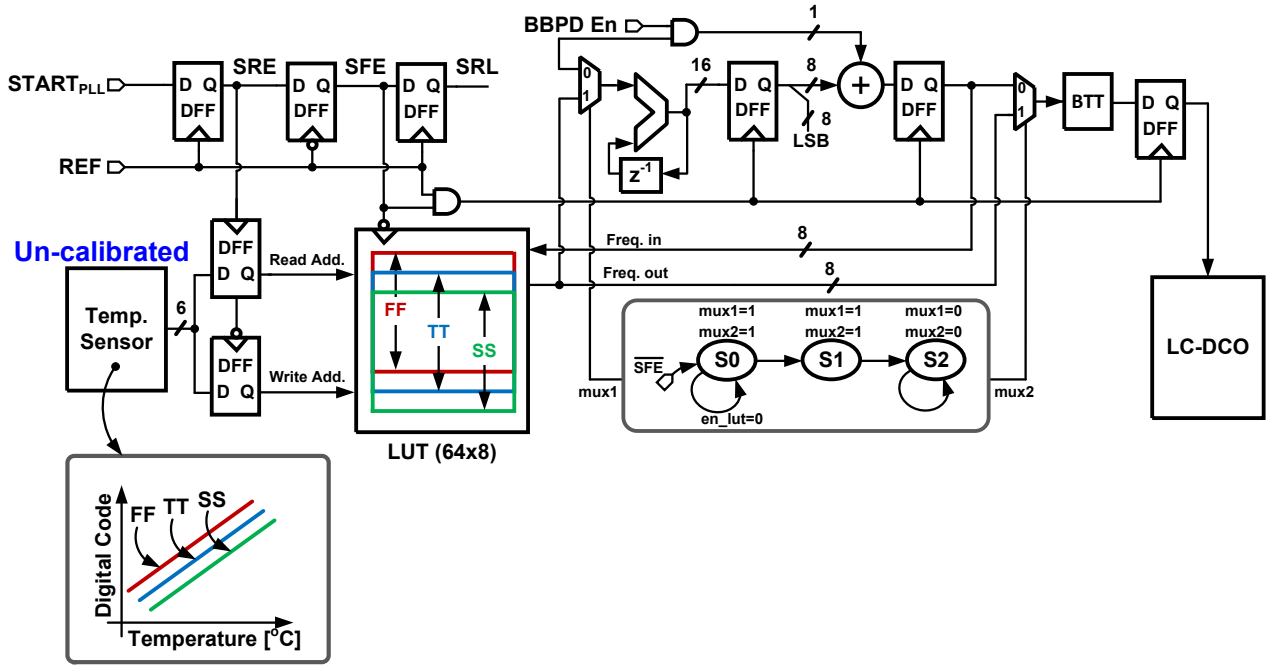


Figure 4.5: Proposed PLL operation in the presence of temperature sensor and LUT.

LUT and is restored into the integral path accumulator. The LUT stores the absolute value of the 8-bit frequency control word. The LUT contents are initially filled with values obtained from transistor-level simulations of the DCO and the temperature sensor and subsequently refreshed at every power-off event. When the PLL is powered-off, the digital control word from the integral path accumulator is written to the address corresponding to the temperature provided by the temperature sensor [46]. A big benefit of using a temperature sensor to map to LUT for the frequency control word is that an uncalibrated temperature sensor can be used. Any offset or non-linearity of the temperature sensor can be compensated by adjusting the LUT size (see Fig. 4.5). Design details of the temperature sensor are discussed in Chapter 6. The LUT operation can be optionally enabled at the expense of one reference cycle power-on latency.

Although LUT can compensate for large frequency errors, limited rows of LUT and quantization of fine frequency tuning in 256 discrete steps could result in residual frequency error. If the PLL is configured in bang-bang mode, then the PLL can tolerate error less than or equal to the bang-bang step size. Any error more than the step size would result in phase

slewing. In this PLL, the bang-bang step size is programmable and ranges from 40ppm (+/-20ppm) to 640ppm. If the PLL is configured in the proportional control mode, then the frequency error would result in phase offset at the input of PFD on power-on. The amount of offset depends on the PLL loop dynamics, multiplication factor and frequency error.

As described earlier, a phase error between Φ_{REF} and Φ_{FB} is made zero on power-on with the help of a DLL, which operates in the background. DLL consists of a delay line, which is digitally controlled with 7-bits, and has a range of 250ps with a step size of approximately 2ps. Assuming the initial condition of the divider is set properly, in the worst case, the phase difference between the feedback clock ($\mathrm{FB_{DEL}}$) and the reference clock ($\mathrm{REF_{DEL}}$) will be at most one VCO period (approximately 142ps). As a result, phase calibration loop takes at most 128 power-on/off cycles to reach steady state. A replica delay line is added on the reference clock path to compensate for the phase drifts in the delay line and divider caused due to temperature variations during long off-periods and voltage variations during on-off events.

4.4 PLL Building Blocks

This section discusses the key building blocks used the the PLL design.

4.4.1 LC-Digitally Controlled Oscillator (LC-DCO)

LC-DCO architecture is shown in Fig. 4.6. It consists of a 7-bit binary weighted coarse frequency selection (CFS) capacitor bank and an 8-bit thermometer coded fine frequency selection (FFS) capacitor bank. The tuning resolution of CFS and FFS is 300ppm and 20ppm, respectively. A single turn 0.44nH inductor is used to achieve a quality factor of approximately 20. Two additional pull-down NMOS transistors are added on either side of LC-DCO to provide the initial condition. On power-on, a narrow pulse derived from the START signal is applied to the gate of one of these NMOS transistors, which pulls down one end of the LC-tank momentarily. This ensures that the oscillator phase trajectory remains fixed on every power-on event.

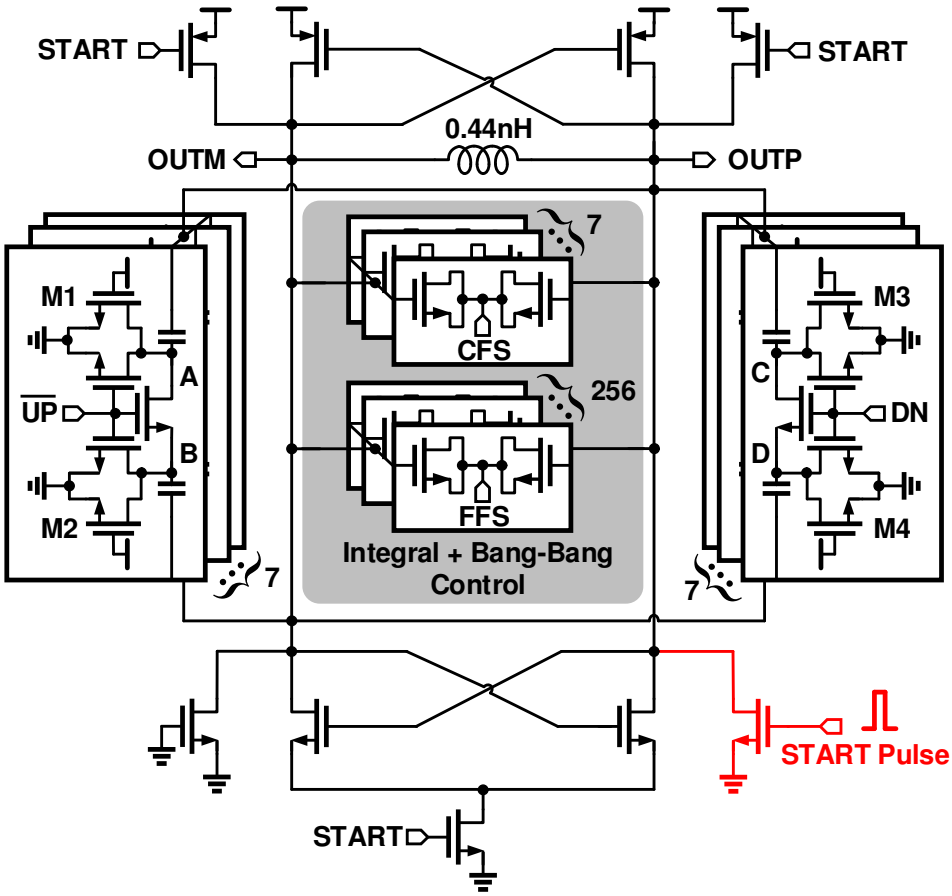


Figure 4.6: Proposed LC-Digitally Controlled Oscillator (LC-DCO) architecture.

A large initial condition helps to reduce the uncertainty in the oscillator phase trajectory. Based on the peak-peak DCO phase error estimated from 100 power-on transient noise simulations, design parameters such as startup pulse width, rise/fall time, and pull-down NMOS transistor size were estimated. Simulation results suggest that a pulse width larger than 100ps with 100ps rise and fall time results in a phase error of $480\text{fs}_{\text{pk-pk}}$. A 16μm/80nm pull-down NMOS transistor results in a pk-pk phase error of $400\text{fs}_{\text{pk-pk}}$, which meets our design goals.

Proportional control is implemented using a seven-step MIM capacitor bank using UP/DN controls with a frequency step of approximately +12,250/-9,750 ppm. This results in a PLL bandwidth of approximately 1.5MHz. Bandwidth of the PLL in proportional control mode

is given by the following expression:

$$\omega_{BW} \approx \frac{K_{PD}K_{VCO-SW}}{N} \tag{4.2}$$

where $K_{PD} = 1/2\pi$ and $K_{VCO\text{-}SW}$ is the VCO frequency switched with UP/DN control signals.

When the oscillator is powered-off, its output nodes OUTP and OUTM settle toward V_{DD}. On power-on, the oscillator output common-mode quickly changes from V_{DD} to $V_{DD}/2$. As a result, nodes A, B, C, and D, which are at the bottom plate of the MIM capacitor bank experience a step-like transition, which decays slowly based on the time constant on these nodes. For an always-on PLL, this transition time is not a problem, but for the rapid-on/off PLL, voltage transition on nodes A, B, C, and D could change the NMOS switch resistance between the MIM caps, and results in slow frequency settling [47]. To address this issue, care was taken to reduce time constants on nodes A, B, C, and D by adding resistors in the form of always-on transistors M1, M2, M3, and M4.

4.4.2 Phase Detector

UP and DN signals used by the integrator to control the DCO frequency, are digitized with the help of a 1 bit time to digital converter (TDC). The TDC used in this PLL consists of two cross-coupled latches, as shown in Fig. 4.7. One of the key requirement in such TDC is to have no offset between the UP and DN signals, i.e., there should be no setup and hold time. Any offset between the UP and DN path will appear as a frequency error and eventually leads to a reference spur. Unlike in the case of conventional flip-flops, in the proposed TDC architecture, both UP and DN see the same path to the output, which ideally results in zero phase offset.

In steady state both UP and DN signals are logic 0, and as a result, the outputs of Latch-1 (STG1P and STG1M) are both logic high. The output of Latch-2 (USD) is low. Due to the action of the three-state PFD, near the reference edge, one of either the UP or DN signal is asserted to logic high, followed by both signals going high, followed by both going low again. If UP is asserted high, Latch-1 acquires a known state in which STG1M goes low and

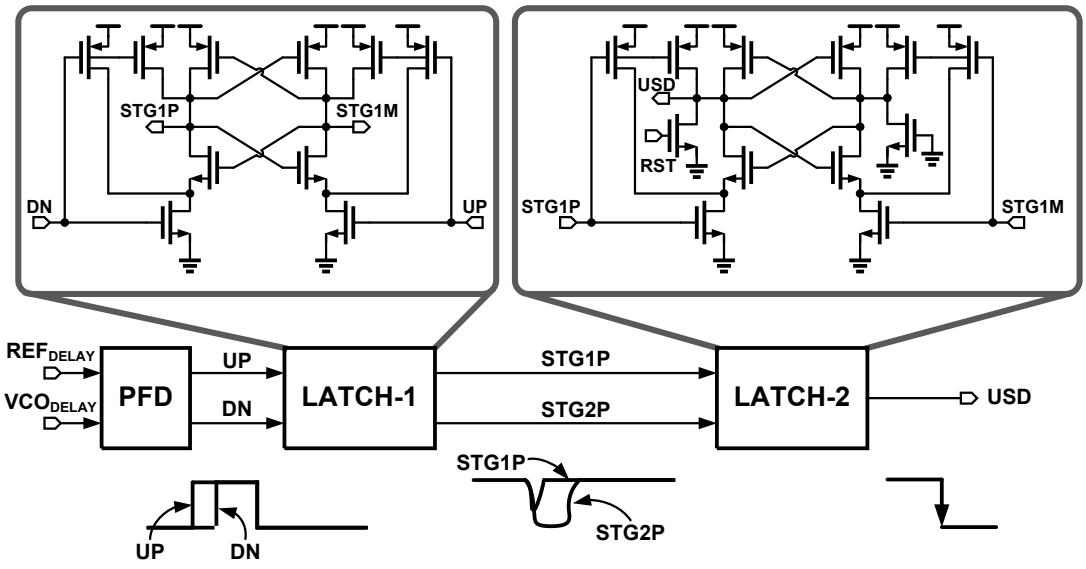


Figure 4.7: Phase detector slicer architecture used for the proposed PLL.

STG1P stay high (see Fig. 4.7). Because STG1P is high, the output of Latch-2 (USD) goes low. When both UP and DN signals go low, both the outputs of Latch-1 are asserted high, and as a result, the output of Latch-2 is held for the entire duration of the reference cycle.

4.5 PLL Modes and Power-On Sequence

Proposed PLL can be configured to operate in four different power-on sequence modes. These modes are Tx PLL without LUT, Tx PLL with LUT, Rx PLL without LUT, and Rx PLL with LUT mode. Use of these modes will become more evident when the complete transceiver architecture is discussed in Chapter 5.

In Tx PLL without LUT mode, PLL is configured to be used for the transmitter. The previously saved frequency control word is restored from the integral path accumulator. PLL starts instantaneously with the START PLL signal that is synchronized with the REF clock.

In Tx PLL with LUT mode, PLL is configured to be used for the transmitter. The previously saved frequency control mode is restored back from the LUT. It takes one reference cycle to perform this operation. Therefore, in this mode the PLL power-on-lock time is increased by one reference cycle.

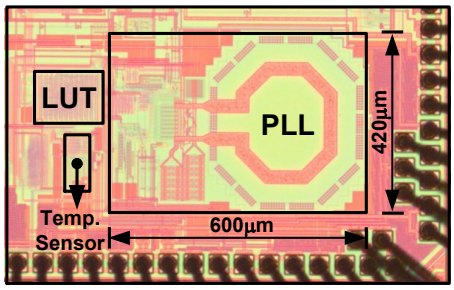


Figure 4.8: Die micrograph of the proposed PLL.

In Rx PLL without LUT mode, PLL is configured to be used in the receiver. The previously saved frequency control mode is restored back from the integral path accumulator. PLL starts instantaneously with the START PLL signal, but in out-of-lock condition.

In Rx PLL with LUT mode, PLL is configured to be used in the receiver. PLL starts instantaneously with the START PLL signal in out-of-lock condition. The previously saved frequency control mode is restored from the LUT. It takes one reference cycle to perform this operation. While the LUT read operation is underway, the PLL output could gain or lose phase in the first reference cycle after power-on. CDR corrects the resulting sampling phase error with the help of phase interpolator (PI).

4.6 Measurement Results

The prototype transceiver was implemented in a 65nm CMOS process, and the die micrograph is shown in Fig. 4.8. The chip was packaged in a 10mm x 10mm 88-pin QFN plastic package. PLL occupies an active area of approximately 0.22mm^2 and operates from a 1V supply. Experimental results to quantify the PLL performance in always-on and rapid-on/off modes are presented in the following subsections.

4.6.1 Measurements in Always-On Mode

Raw PLL performance such as long-term jitter, phase noise, and output spectrum was measured in always-on condition. A measured jitter histogram of the PLL output clock at

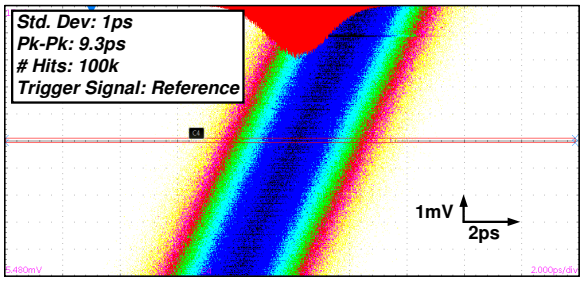


Figure 4.9: Measured PLL jitter in proportional control mode.

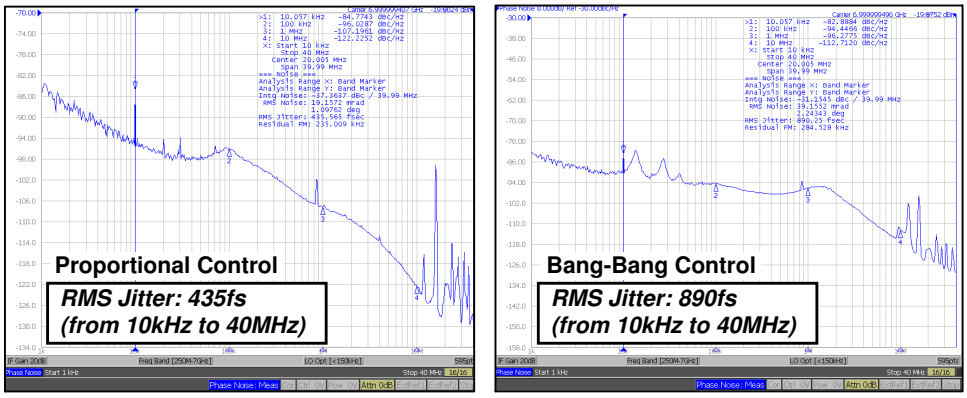


Figure 4.10: Measured PLL phase noise in (a) proportional control mode, and (b) bang-bang control mode.

7GHz is shown in Fig. 4.9. Long-term absolute jitter is $1ps_{rms}$ and $9.3ps_{pk\text{-}pk}$, including the trigger jitter of a Tektronics DSA8300 oscilloscope.

A measured phase noise plot is shown in Fig. 4.10 and the integrated jitter is $435fs_{rms}$ in proportional control mode and $890fs_{rms}$ in bang-bang control mode.

A measured phase noise plot with higher proportional gain in proportional control mode is shown in Fig. 4.11. Integrated jitter is $530fs_{rms}$. Noise from the reference source is the main cause of this jitter.

The measured reference spur is -50.1dB in proportional control mode and -46.8dB in bang-bang control mode, as shown in Fig. 4.12. The measured temperature sensitivity of the LC tank operating at 7GHz is -79.1ppm/^{o}C, as shown in Fig. 4.13.

The measured supply sensitivity of the LC tank operating at 7GHz is -52.85ppm/mV, as shown in Fig. 4.14.

The PLL can track approximately 5120ppm of the frequency offset with 20ppm of fine

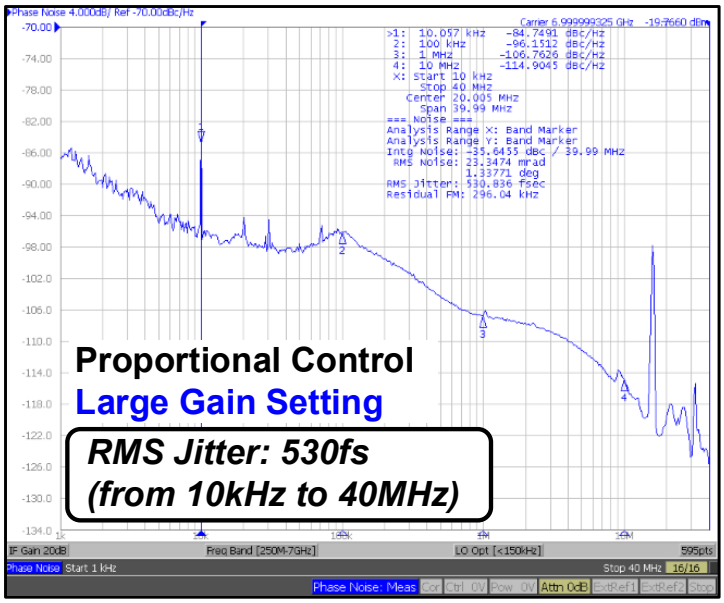


Figure 4.11: Measured PLL phase noise in proportional control mode with large gain.

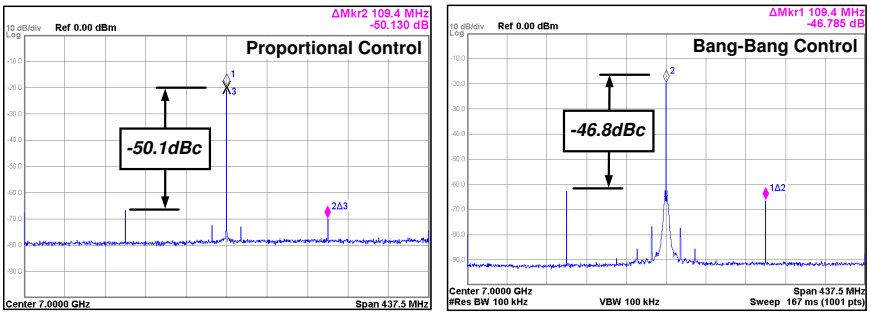


Figure 4.12: Measured PLL spectrum in (a) proportional control mode, and (b) bang-bang control mode.

frequency step (FFS). This 5120ppm translates to approximately 65^{o}C of the temperature range. With 64 entries, LUT can provide approximately 1^{o}C of the temperature resolution. The temperature sensor is placed near the LC-DCO. The update rate of the temperature sensor is programmable with the maximum measured update rate of around 150k samples/second. This is equivalent to around 6.5μs of temperature measurement time.

The PLL power break down in the always-on state, and the always-off state are shown in Figs. 4.15(a) and 4.15(b), respectively. Operating at 7GHz, the PLL consumes 4.8mW of which the LC oscillator and clock buffers consume a majority of this power. The power

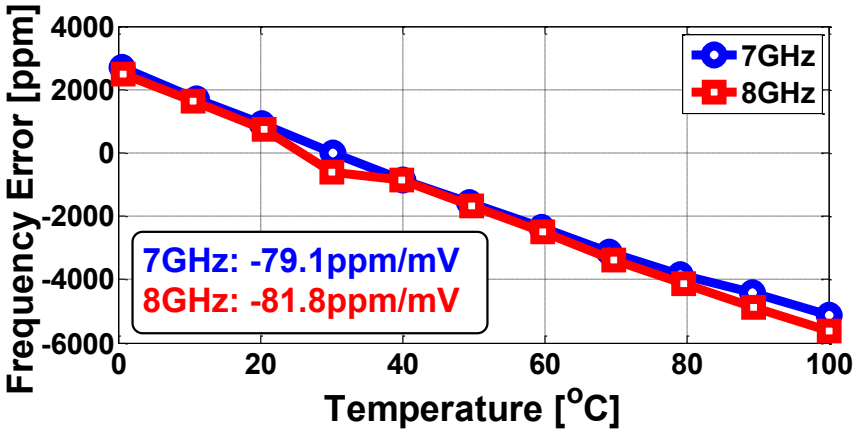


Figure 4.13: Measured LC tank temperature sensitivity.

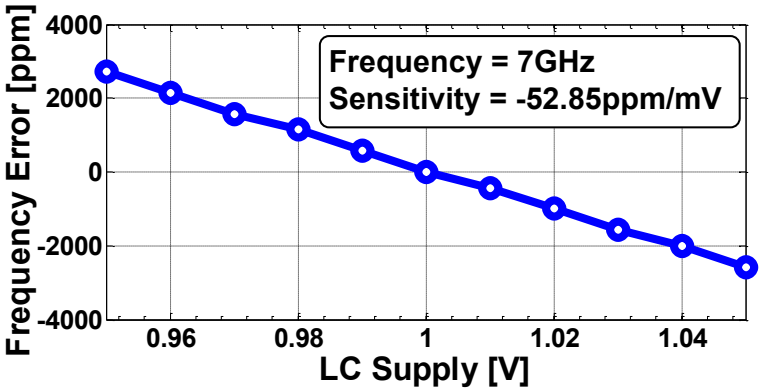


Figure 4.14: Measured LC tank supply sensitivity.

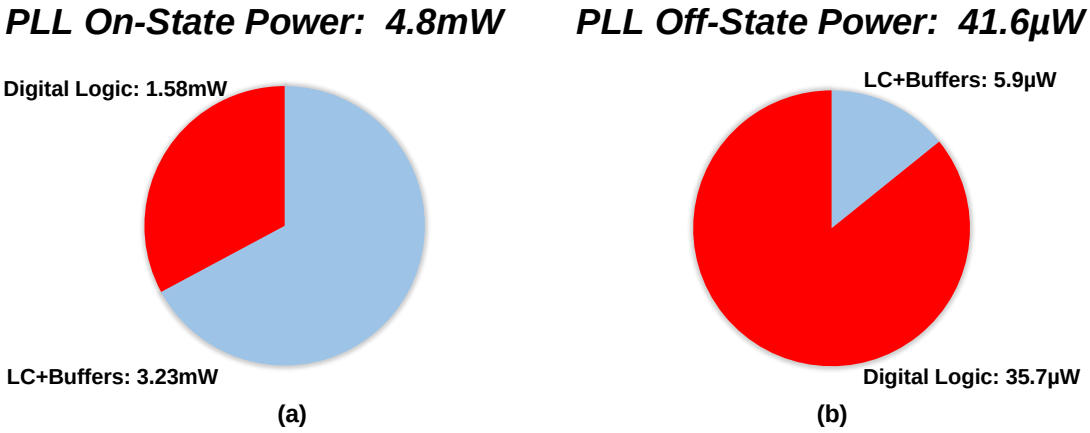


Figure 4.15: Measured power distribution of the proposed PLL (a) On-state power, and (b) off-state power.

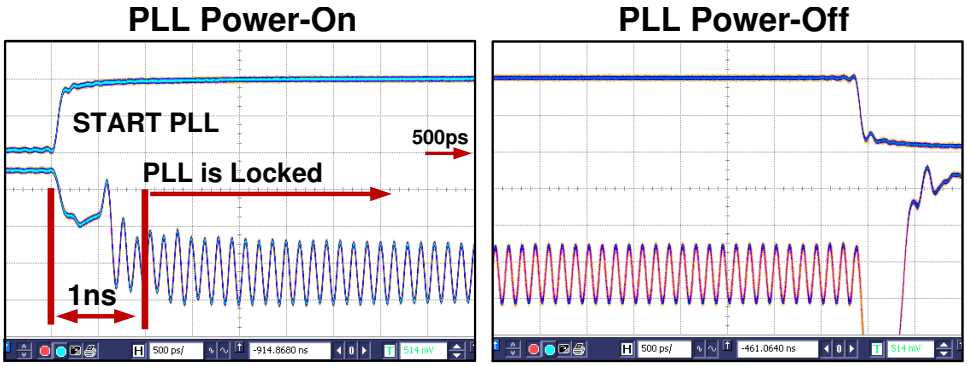


Figure 4.16: Oscilloscope capture of the PLL power-on/off transient.

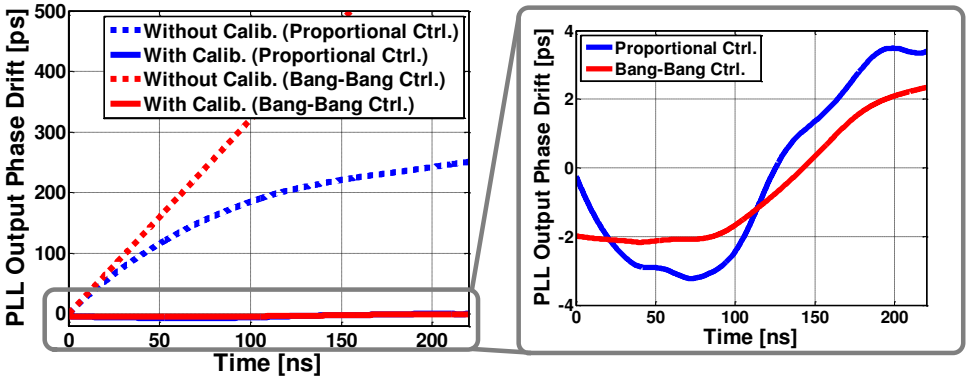


Figure 4.17: Measured absolute phase drift of the PLL in proportional and bang-bang control modes.

consumption in the off-state is only 41.6μW. Leakage in the digital logic makes up an approximately 86% of off-state power consumption.

4.6.2 Measurements in Rapid-On/Off Mode

The measured power-on transient of the PLL, shown in Fig. 4.16, demonstrates that the PLL powers-on/off instantaneously.

To quantify the settling time of the PLL, error in the output time period was calculated from the output waveform captured using a high-frequency sampling scope, Agilent DSO-81204A. The cumulative sum of the period error signifies the absolute phase drift as depicted in Fig. 4.17.

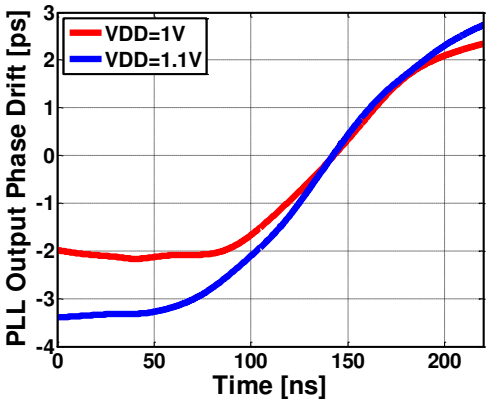


Figure 4.18: Measured absolute phase drift to demonstrate the effectiveness of the replica delay in the presence of voltage variations on the digital power supply.

Mathematically, absolute phase drift can be calculated as:

$$\text{Phase Drift} = \sum_{i=1}^{\infty} \left(P_i - \frac{1}{7 \times 10^9} \right) \tag{4.3}$$

where P_i is the i^{th} measured period. The dotted and solid lines show the phase drift without and with background DLL based phase calibration, respectively. The absolute phase drift with phase calibration is measured to be ±3ps in a measurement span of 220ns, which is approximately 2-3 time constants of the PLL loop. Beyond this span, PLL feedback ensures that the phase does not drift beyond 3ps. Figure 4.18 shows the measured effectiveness of the replica delay line. PLL phase drift measured with 100mV of voltage variation on the feedback divider and delay line during the off-period is less than 2ps, compared to nominal supply case.

Table 4.1 compares the proposed PLL with the state-of-the-art fast power-on-lock frequency multipliers. The proposed PLL achieves the smallest power-on-lock time, which is two orders of magnitude lower than other reported PLL architectures and an order of magnitude lower than reported MDLL and MILO architectures.

4.7 Conclusion

In this chapter, a 7GHz fast power-on-lock LC-PLL was presented. Motivation for designing the fast power-on-lock PLL was discussed, and advantages of PLL over MDLL was elaborated. The temperature sensor and LUT based approach was used to achieve temperature insensitivity during long power-off periods. Fabricated in 65nm CMOS process, the prototype PLL achieved 1ns power-on lock time. Operating from 1V supply, proposed PLL achieves on and off-state power of 4.8mW and 41.6μW, respectively. Integrated jitter in always-on mode is 435fs$_{\text{rms}}$ while multiplying 109.375MHz reference by 64x. It occupies an active area of 0.22mm^2.

Table 4.1: Performance Comparison of the Proposed Fast Power-on-Lock LC-PLL with State-of-the-Art Designs

	This Work	[21]VLSI'13	[15]JSSC'10	[22]ISSCC'13	[14]VLSI'11	[31]CICC'12
Architecture	**PLL**	PLL	PLL	MDLL	MILO	MILO
Technology	**65nm GP**	40nm	40nm LP	90nm	40nm LP	65nm
Supply[V]	**1**	N/A	1.1	1.1	N/A	1.1
Output Freq.[GHz]	**7**	25	4.3	2.5	2.8	2.3-4
Reference Freq.[MHz]	**109.357**	390	537.5	312.5	700	790
Integrated Jitter.[fs]	**435**	394	N/A	752	N/A	N/A
Power-on-Lock Time[ns]	**1**	100	241.8	10	8	10
Efficiency[mW/GHz]	**0.68**	2.56	N/A	0.88	4.8	30.4
On-Power[mW]	**4.8**	64	N/A	2.2	13.44	96
Off-Power[μW]	**41.6**	N/A	N/A	25	0	N/A

CHAPTER 5

A 7Gb/s EMBEDDED CLOCK TRANSCEIVER FOR ENERGY PROPORTIONAL LINKS

In this chapter, a rapid-on/off transceiver for an embedded clock architecture that enables energy proportional communication over the serial link is presented. Architecture and circuit techniques to achieve rapid-on/off in transmitter and receiver are discussed. CDR phase calibration logic in the receiver enables instantaneous lock on power-on. The proposed transceiver demonstrates power scalability with a wide range of link utilization and, therefore, helps in improving overall system efficiency. Fabricated in 65nm CMOS technology, the 7Gb/s transceiver achieves power-on-lock in less than 20ns. The transceiver achieves power scaling by 44x (63.7mW-to-1.43mW) and energy efficiency degradation by only 2.2x (9.1pJ/bit-to-20.5pJ/bit), when the effective data rate (link utilization) changes by 100x (7Gb/s-to-70Mb/s). The proposed transceiver occupies an active die area of 0.39mm^2.

This chapter is organized as follows. Section 5.1 introduces the complete transceiver architecture. Architecture and circuit details of the output driver are presented in Section 5.2. Section 5.3 discusses the fast power-on-lock CDR architecture. Section 5.4 presents the measured results. Section 5.5 concludes the chapter.

5.1 Transceiver Architecture

The proposed 7Gb/s rapid-on/off transceiver architecture is shown in Fig. 5.1. The transmitter consists of a parallel PRBS generator, 16:1 serializer, three tap feed-forward equalizer, and fast power-on current-mode logic (CML) based output driver. The serializer is designed with a series of 2:1 multiplexers. PRBS data generated using synthesized parallel PRBS generators [48] operating at 437.5MHz, is serialized to generate a 7Gb/s true PRBS data stream. Fast power-on biasing is used to power-on the CML based pre-driver and output

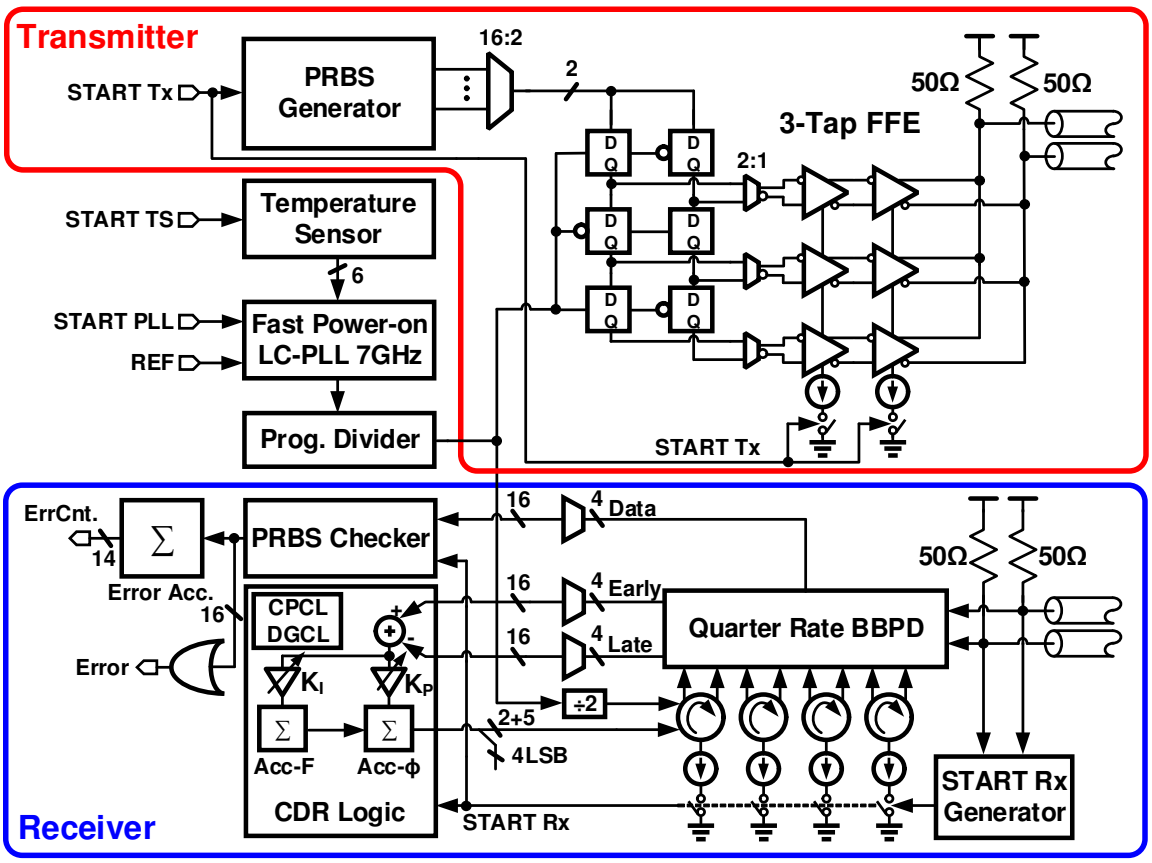


Figure 5.1: Proposed rapid-on/off transceiver architecture.

driver.

The receiver consists of a quarter rate bang-bang phase detector (BBPD), 4:16 deserializer, clock and data recovery (CDR) logic, phase interpolators (PI), PRBS checker and the START Rx Generator circuit (also known as receiver wake-up circuit). Receiver lock time is estimated from the Error signal, which is generated by performing logical OR operation on parallel PRBS checker outputs. Receiver lock is declared when the Error signal goes low. CDR phase calibration logic (CPCL) and dynamic gain calibration logic (DGCL) are the two techniques used to achieve fast phase and frequency locking.

A fast power-on-lock LC-PLL generates a 7GHz clock for both the transmitter and receiver blocks. A programmable divider following the LC-PLL divides the PLL output for operation at lower data rates. Because power-off periods can be of the order of milliseconds [49], frequency drift caused by die temperature change [50] are compensated using an on-chip temperature sensor [46] and a look-up table (see Chapter 4 for details). The proposed

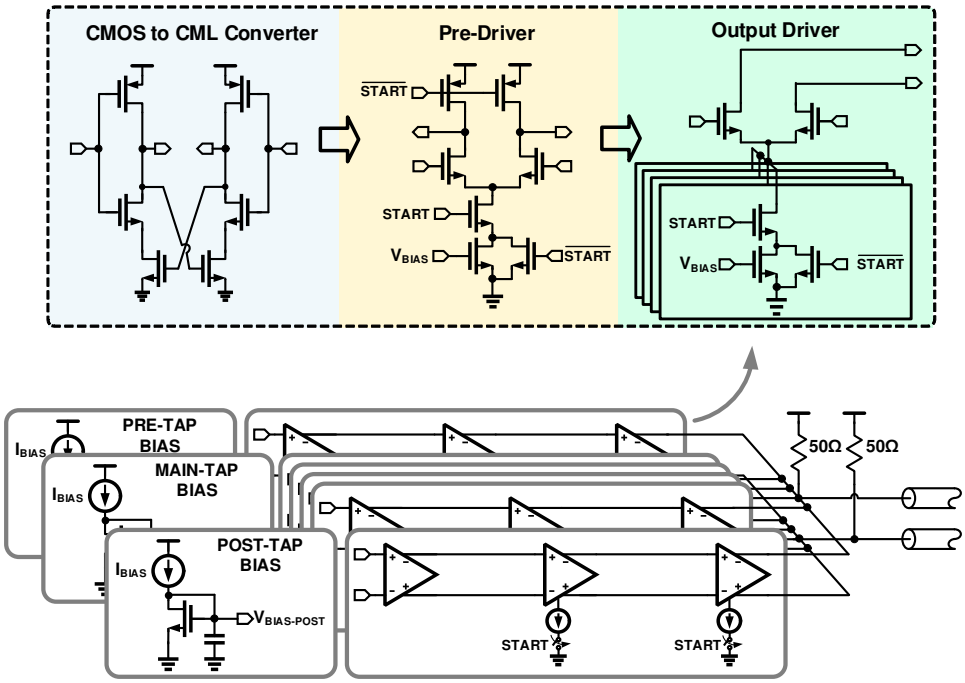


Figure 5.2: Transmitter output driver slice architecture.

transceiver can be configured in either transmitter or receiver mode. In the transmitter mode, the PLL powers-on in a phase locked condition, while in the receiver mode, PLL powers-on without a phase lock. The advantages of starting the PLL in out-of-lock condition are discussed in Section 5.3.2.

5.2 Transmitter

The proposed rapid-on/off CML based transmitter output driver chain is shown in Fig. 5.2. While it is possible to achieve rapid-on/off capability in low power voltage-mode output drivers [15, 17], CML is preferred for its lower sensitivity to supply transients, which occur during the power-on events. Compared to the previously reported rapid-on/off CML drivers [14, 18], the proposed CML driver achieves a smaller power-on time at the expense of a small always-on bias current. The design of the transmitter driver chain is done in a sliced fashion, where each of these slices consists of a CMOS-to-CML converter, pre-driver, and an output driver (see Fig. 5.2). Three tap feed-forward equalization is provided on the transmitter end, and it is integrated into the output driver. Pre-cursor and post-cursor of the equalizer

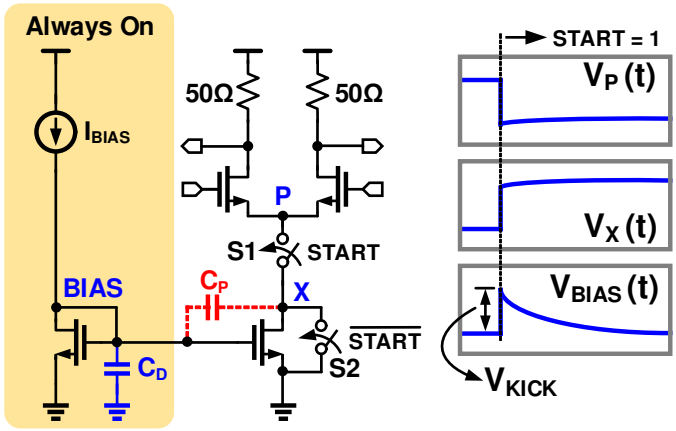


Figure 5.3: Fast power-on biasing scheme for CML based logic.

consist of one slice each while the main cursor consists of four slices. In each slice of the output driver, the tail current source consists of a 2-bit current DAC. By configuring the number of slices and tail current of CML logic, equalization coefficients can be adjusted in a coarse and fine way, respectively.

Fast power-on CML logic and the associated timing diagram is shown in Fig. 5.3. A small bias current I_{BIAS} is kept always-on to achieve the fast power-on capability. During power-off, switch S1 is off, and, as a result, the common-mode voltage of the output driver is at V_{DD}. On power-on, the voltage at node P falls sharply fall from V_{DD} to voltage $V_P = V_{IN\text{-}CM}$ - V_{TH}, where $V_{IN\text{-}CM}$ is the input common-mode voltage of the output driver. At the same time, node X rises from ground to voltage $V_X \approx V_P$. A large jump in V_X causes a kick-back on the BIAS node voltage V_{BIAS}, which is given by the following expression,

$$V_{KICK} = \frac{C_P}{C_P + C_D} V_X \tag{5.1}$$

where C_P is the gate to drain parasitic capacitance, and C_D is the decoupling capacitor on the BIAS node. The decay time of the kick-back depends on the time constant associated with the BIAS node and it is usually of the order of few nanoseconds. Kick-back causes a current overshoot in the output driver, which manifests itself as jitter. Adding a decoupling capacitor C_D on the BIAS node, helps in reducing the magnitude of V_{KICK}, and consequently helps in reducing jitter. A conventional CML driver takes more than 120ns to power-on and settle [18]. With the proposed fast power-on CML technique, the transmitter output driver

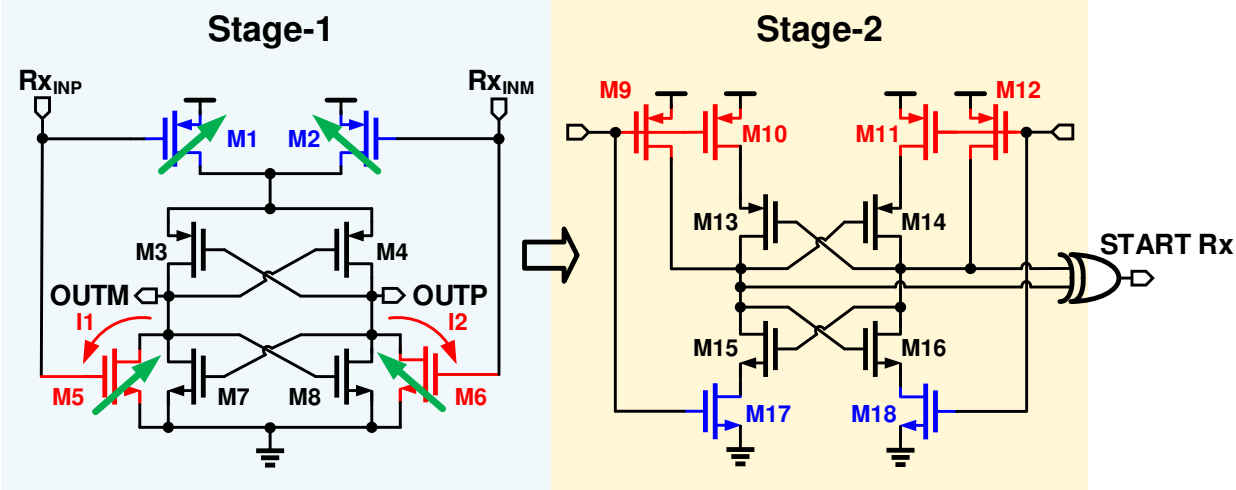


Figure 5.4: Schematic of START Rx Generator circuit.

settles within 500ps (based on measured results).

5.3 Receiver

Rapid-on/off operation requires the receiver to quickly synchronize with the received data and must have the ability to power-on/off instantaneously. Conventional high-speed burst mode receivers can quickly lock to the received data, but cannot be powered down [51, 52]. Gated VCO based burst mode receiver can be powered down [53], but they are limited to low data rates (2.2Gb/s). In view of these limitations, we propose a high-speed burst mode receiver with rapid-on/off capability. Two techniques referred to as CDR phase calibration logic (CPCL) and dynamic gain calibration logic (DGCL), are employed to achieve fast phase and frequency acquisition.

5.3.1 START Rx Generator

START Rx Generator circuit is shown in Fig. 5.4. It consists of two cross-coupled stages denoted as Stage-1 and Stage-2. Stage-1 output does not go all the way to V_{DD} due to the current sinking transistors M5 and M6, and for that reason Stage-2 is used to amplify the Stage-1 output and drive the XOR gate. To ensure reasonable swing at the output of

Stage-1, transistors M1 and M2 are made wider than transistors M5 and M6. Similarly in Stage-2, transistors M17, and M18 are made wider than M9, M10, M11, and M12.

When the transmitter is powered on, common-mode voltage of the output driver drops from V_{DD} to V_{DD} - $V_{SWING}/2$, where V_{SWING} is the transmitter output swing. Transistors M1 and M2 in Stage-1 sense this change, and starts to pump current in the cross-coupled pair consisting of transistors M3, M4, M7, and M8. As a result, the Stage-1 latch acquires a known state, i.e., one output goes high, and its complement goes low. This state depends on the relative value of currents I1 and I2, which are drawn from transistors M5 and M6, respectively. The relative value of current depends on the starting data pattern. For instance, if the incoming data is all 0's ($Rx_{INP} < Rx_{INM}$), then I2 > I1 and $V_{OUTP} < V_{OUTM}$. In this design, the starting data pattern is kept fixed. In the practical usage scenario, it can be fixed by using a fixed preamble on the data packet. When the transmitter is powered-off, both nodes Rx_{INP} and Rx_{INM} are at V_{DD}. Transistor M1 and M2 are off, and transistors M5 and M6 pull down the output of Stage-1 latch to ground. Consequently, both outputs of the Stage-2 latch are at V_{DD}, and the START Rx signal is low. The START Rx generator has a minimum requirement on the common-mode voltage for correct operation. Based on simulations, at a typical corner (TT corner), the START Rx generator fails to operate with a common-mode voltage above 945mV.

The simulated sensitivity of the START Rx signal is shown in Fig. 5.5. START Rx has a sensitivity of -1.4ps/mV to the transmitter signal swing, -2.3ps/^oC to the receiver temperature, -3.2ps/mV to the receiver supply and 2.4ps/mV to the transmitter supply. In the present design, the on-chip temperature sensor is not used to track START Rx phase drift. At higher data rates, large phase drifts due to temperature variation during long off-periods could be detrimental. Therefore, it may be possible to use the temperature sensor to compensate for this drift in future work.

One thousand Monte Carlo mismatch simulations were done for the START Rx generator. The peak-to-peak variation of the START Rx signal is 94ps with the standard deviation of approximately 12.6ps. One thousand transient noise simulations were done for three different transmitter output swings, as shown in Fig. 5.6. Simulated peak-peak jitter of the START Rx signal with 500mV($Diff_{pk\text{-}pk}$) is only 16ps, which is 0.11UI.

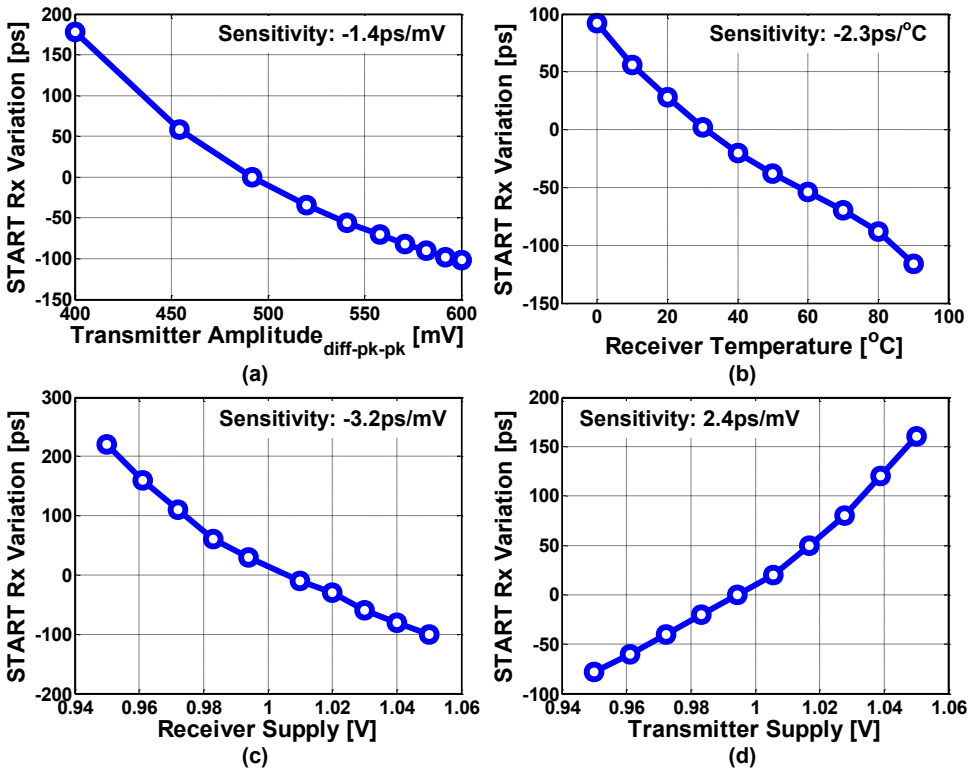


Figure 5.5: (a) Simulated START Rx signal sensitivity to transmitter amplitude. (b) Simulated START Rx signal sensitivity to receiver temperature. (c) Simulated START Rx signal sensitivity to receiver supply voltage. (d) Simulated START Rx signal sensitivity to transmitter supply voltage.

Simulations were done for five different amounts of channel loss to understand the effect of ISI on the START Rx generator. As shown in Fig. 5.7, the START Rx signal delay varies from approximately -150ps to 150ps.

Simulations results indicate that the START Rx signal is generated in less than 1ns after the transmitter is powered on (assuming no channel delay). The fixed phase relationship between the received data on nodes Rx_{INP}, Rx_{INM} and the START Rx signal is leveraged to speedup CDR phase acquisition as discussed next in Section 5.3.2.

5.3.2 CDR Phase Calibration Logic (CPCL)

Receiver architecture and proposed CDR phase calibration logic are shown in Fig. 5.8. In this scheme, the sampling phase of the CDR (Φ_{PI}) at the time of power-on is generated with a fixed phase relation to the data phase (Φ_{DATA}), such that Φ_{PI} becomes independent

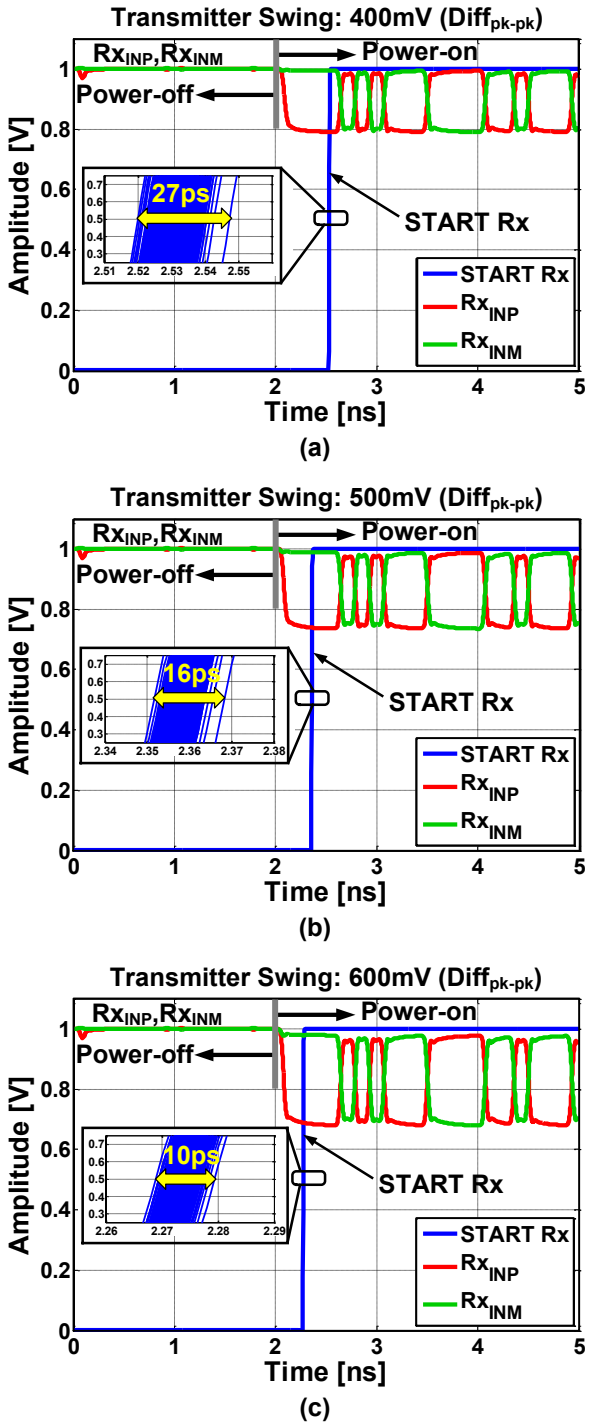


Figure 5.6: Simulated START Rx generator for 1000 transient noise simulations and a transmitter swing of (a) 400mV($\text{Diff}_{\text{pk-pk}}$), (b) 500mV($\text{Diff}_{\text{pk-pk}}$), and (c) 600mV($\text{Diff}_{\text{pk-pk}}$).

of the local reference clock phase (Φ_{REF}). With the help of background calibration, Φ_{PI} is placed at the center of the received data eye to ensure that the CDR starts in a phase locked

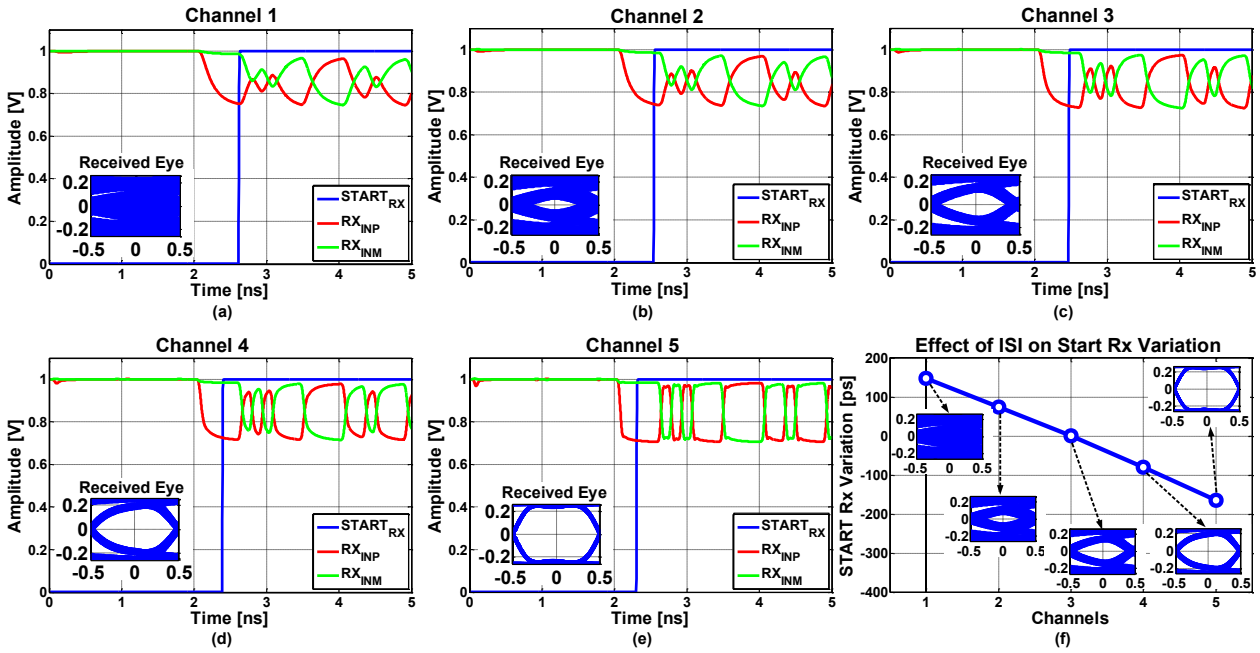


Figure 5.7: (a) Simulated START Rx generator with Channel 1. (b) Simulated START Rx generator with Channel 2. (c) Simulated START Rx generator with Channel 3. (d) Simulated START Rx generator with Channel 4. (e) Simulated START Rx generator with Channel 5. (f) Simulated START Rx signal variation for various channels with PRBS7 data.

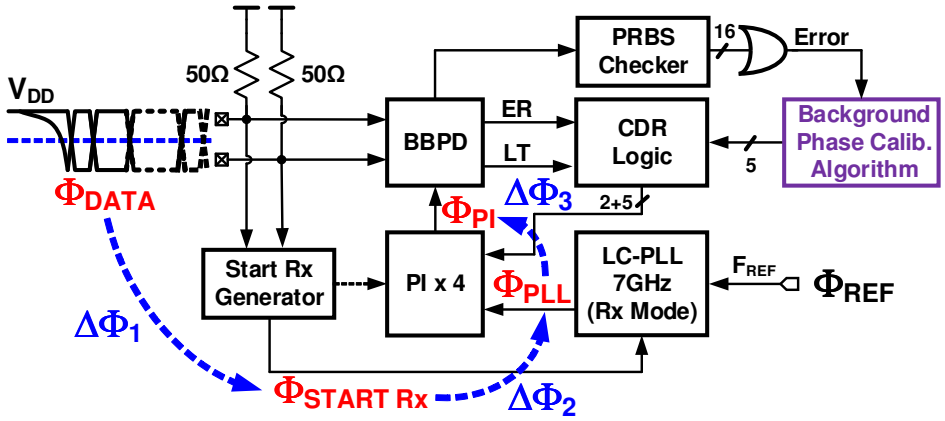


Figure 5.8: Proposed receiver architecture and CDR phase calibration logic (CPCL) concept.

condition, i.e. $\Phi_{\mathrm{DATA}} - \Phi_{\mathrm{PI}} \approx 0.5\mathrm{UI}$.

To meet the above-mentioned phase condition, PLL on the receiver chip is configured to be powered-on without a phase-lock. In this configuration, PLL is powered-on instantly upon receiving the START Rx signal in bang-bang proportional control mode. The advantage of

using bang-bang control for PLL starting in out-of-lock condition is that phase update rate of an oscillator can be well controlled. Care was taken to ensure that PLL phase update rate in the bang-bang mode is smaller than the CDR phase update rate. Note that in contrast to the PLL configured in transmitter mode where the START signal is retimed by the reference clock Φ_{REF}, the START signal used to start receiver PLL is not retimed (En Rx Mode = 1 in Fig. 4.4). This helps in establishing a known phase relation between the phase of START signal (in this case START Rx signal) $\Phi_{\text{START Rx}}$ and PLL output phase Φ_{PLL}, which can be expressed as:

$$\Phi_{\text{PLL}} - \Phi_{\text{START Rx}} = \Delta\Phi_2 \tag{5.2}$$

Using a PI, the phase difference between Φ_{PLL} and Φ_{PI} can be adjusted such that:

$$\Phi_{\text{PI}} - \Phi_{\text{PLL}} = \Delta\Phi_3 \tag{5.3}$$

Based on the discussion on the START Rx Generator circuit, there is a fixed phase relation between Φ_{DATA} and $\Phi_{\text{START Rx}}$, which can be expressed as:

$$\Phi_{\text{START Rx}} - \Phi_{\text{DATA}} = \Delta\Phi_1 \tag{5.4}$$

From (5.2), (5.3), and (5.4), phase relation between Φ_{DATA} and Φ_{PI} is given by:

$$\Phi_{\text{PI}} - \Phi_{\text{DATA}} = \Delta\Phi_1 + \Delta\Phi_2 + \Delta\Phi_3 \tag{5.5}$$

By digitally adjusting $\Delta\Phi_3$, sampling clock phase Φ_{PI} is placed approximately in the middle of received data at the time of power-on. This ensures that CDR starts in phase-locked condition.

Adjustment of $\Delta\Phi_3$ is performed in the background by observing the Error signal on every power-on event. If the sampling phase is not positioned in the middle of the received data at power-on, errors are recorded by the PRBS checker. Since the CDR loop runs in parallel with CPCL, CDR eventually locks to the received data and errors in the received data cease to exist. By observing the time duration of observed errors, $\Delta\Phi_3$ is digitally adjusted by

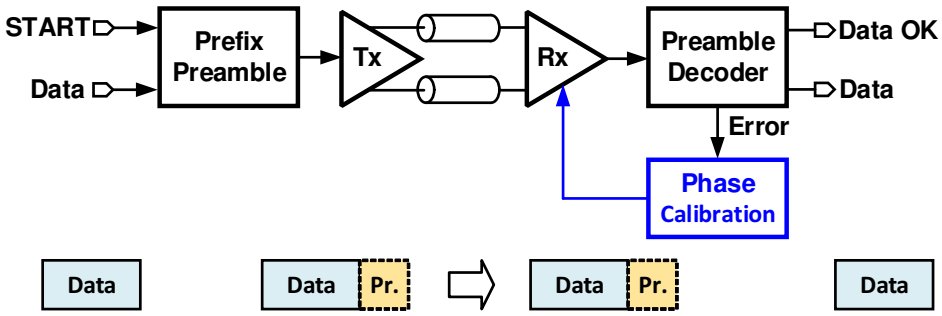


Figure 5.9: Practical usage scenario of the proposed transceiver.

setting the initial 5-bit digital control word for PI, so as to minimize the duration of errors. This adjustment is done once at the end of every power-on/off cycle. Consequently, after a few on/off cycles, CPCL converges, and CDR starts in a phase-locked condition. In this design, monitoring the Error signal and controlling $\Delta\Phi_3$ are performed off-chip.

When the transceiver is powered-on for the first time, the CPCL may start in the non-optimum phase. Consequently, at the end of 20ns (based on measurements) the Error would still exist because CDR has not achieved lock. This will force the CPCL to adjust $\Delta\Phi_3$ for the next power-on event. Since, there are 32 PI steps to cover one unit interval (UI also known as data bit duration), CPCL may take on average 16 on/off cycles to converge. In other words, CPCL has a cumulative training time of 320ns (16 x 20n).

In a practical usage scenario, transmitted data is not a PRBS pattern and therefore, for the operation of CPCL and detection of a CDR lock, a preamble pre-fixed to the data packet could be used (see Fig. 5.9). Correct decoding of this preamble by the receiver could be used to determine if the CDR is locked. The Error signal from the preamble decoder would be used by the CPCL to adjust the initial data sampling phase.

5.3.3 CDR Architecture and Dynamic Gain Calibration Logic (DGCL)

The proposed CDR consists of a quarter rate bang-bang phase detector, which generates early, late and data signals, as shown in Fig. 5.10. The early and late signals go to the digital loop filter, which consists of a proportional and integral path followed by a phase accumulator. The output of the phase accumulator is applied to four PIs, which are used to sample data and the edge in the BBPD.

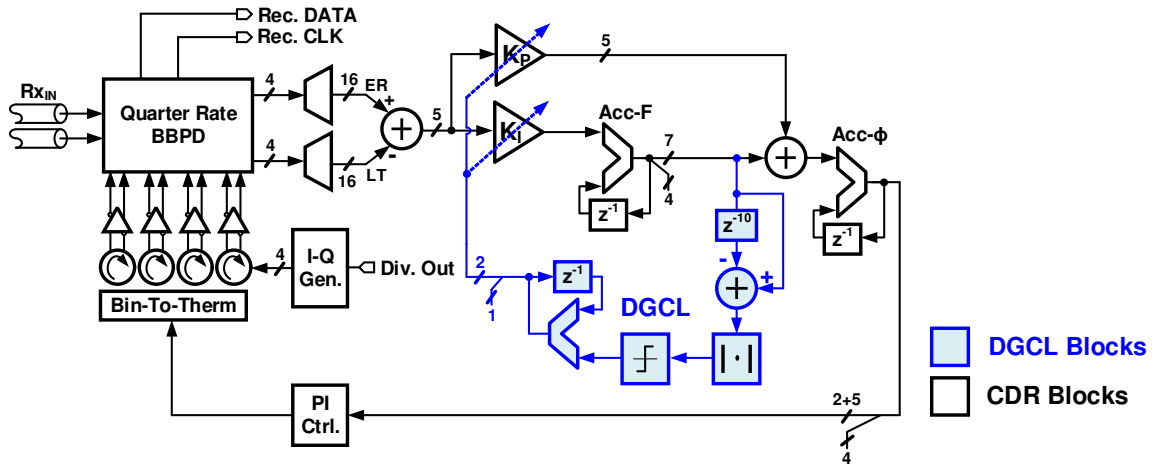


Figure 5.10: Proposed CDR architecture and dynamic gain calibration logic (DGCL) blocks.

Dynamic Gain Calibration Logic (DGCL) helps to achieve fast phase and frequency acquisition and operates in conjunction with CPCL (see Figure 5.10). DGCL starts the CDR loop with a very high gain on power-on. High gain helps with fast phase and frequency acquisition but increases recovered clock jitter. Therefore, to reduce the recovered clock jitter, the loop gain is reduced progressively as the CDR approaches toward frequency lock. Frequency lock can be detected by monitoring the ACC-F output. When the CDR acquires frequency lock, the ACC-F output just moves around a static value. Variations in the ACC-F output around the average value is a function of latency in the system and loop gain. The higher the latency, the higher will be the movement of ACC-F output codes in the steady state. Similarly, higher loop gain also results in large movements of ACC-F output around the steady state.

To identify if the ACC-F output has reached the steady state, the ACC-F output is first differentiated. Because CDR loop latency is around five cycles, with the highest gain setting, it was observed from simulations that the CDR limit cycle has an average period of 10 CDR cycles. Therefore, to identify the variation of ACC-F output, ACC-F output must be differentiated after 10 CDR cycles. In the present architecture, the delay for the differentiator is programmable from 1 to 10. All the measurements were done with a delay of 10.

An absolute value operation is performed on the output of the differentiator so as to obtain

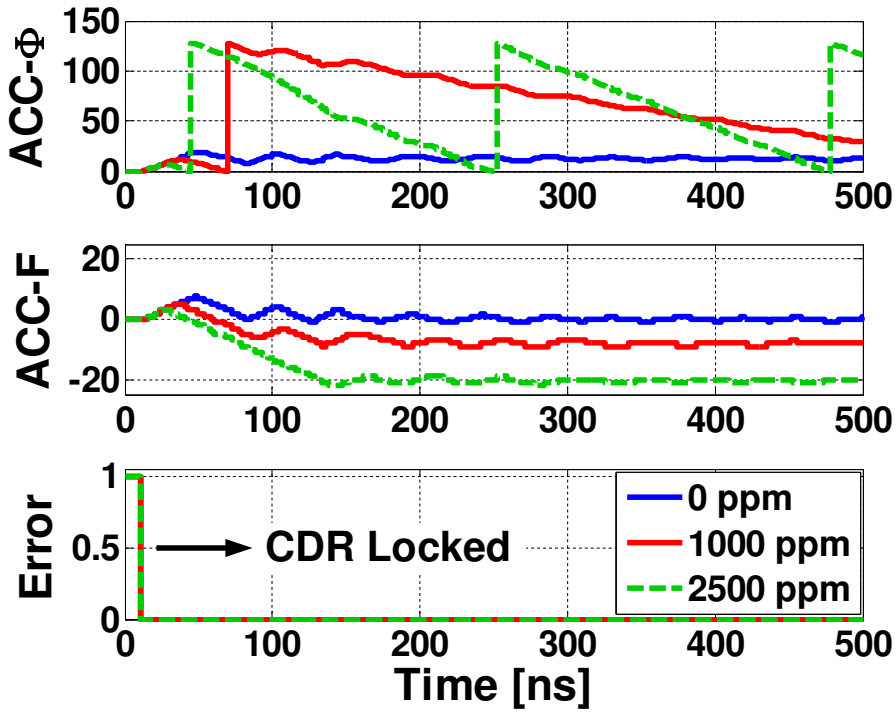


Figure 5.11: Simulated power-on lock profile of transceiver with 0ppm, 1000ppm and 2500ppm of frequency error between the transmitter and the receiver with PRBS7 data.

either zero or a positive value. If the output of the absolute operation is greater than the threshold, this signifies that ACC-F is still settling, and there is no need to change the loop gain setting. Once the output of the absolute operation is less than the threshold, then the 3-bit accumulator increments, which decreases the CDR loop gain. Measurements indicate that at maximum gain setting, the CDR BW is approximately 10MHz and the worst case power-on time without CDR phase calibration logic (CPCL) is 180ns. In steady state, the CDR BW is around 2MHz.

Behavioral simulation of the transceiver in the presence of 0ppm, 1000ppm and 2500ppm of frequency error between the transmitter and the receiver was performed, and the results are shown in Fig. 5.11. The first plot is the output of the accumulator ACC-Φ, which controls the PI. In the presence of frequency error, the ACC-Φ output wraps around, and the rate at which it wraps around is governed by the frequency error. The second plot is the output of accumulator ACC-F, which forms the CDR integral path. The third plot is the Error signal. For all three frequency error conditions, the Error signal goes down at the same time. Thus

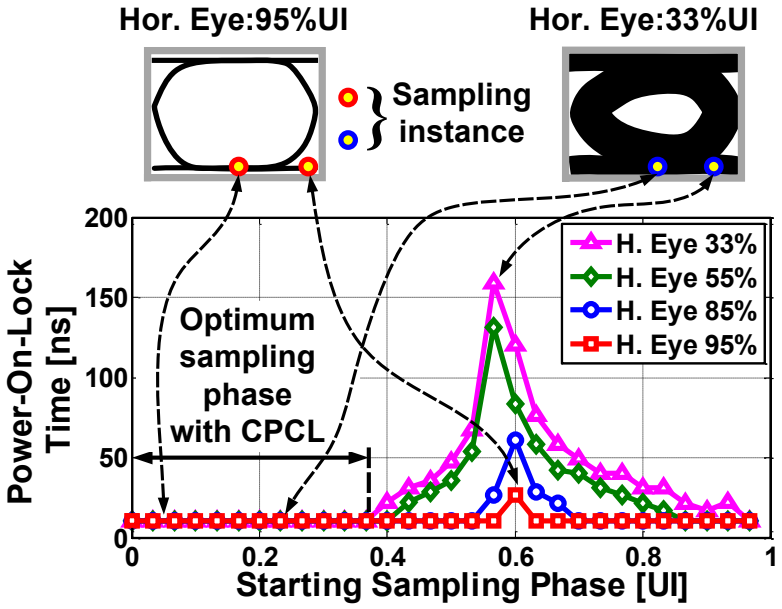


Figure 5.12: Simulated power-on-lock time as a function of starting sampling phase for various horizontal eye openings with PRBS7 data.

the power-on-lock time of the CDR remains the same, regardless of the frequency error.

To understand the effect of ISI on the power-on-lock time for DGCL and CPCL, behavioral simulations of the transceiver in the presence of different amounts of channel loss were performed, and the results are shown in Fig. 5.12. Simulations were done by sweeping the starting sampling phase for four different channels with different percentages of horizontal eye opening. If only the DGCL is used, the data sampling clock has no relation to the received data on power-on. Consequently, power-on-lock time is dependent on the sampling instance and ISI. It can be observed from the simulation that worst-case power-on-lock time increases as the horizontal eye opening reduces. On the other hand, if both CPCL + DGCL are used in the receiver, power-on-lock time becomes fixed and independent of ISI or sampling instance. Thanks to CPCL, the sampling clock has a known phase relation with the received data during power-on. Thanks to DGCL, the CDR is quickly locked to the transmitter frequency, and it continuously tracks the phase.

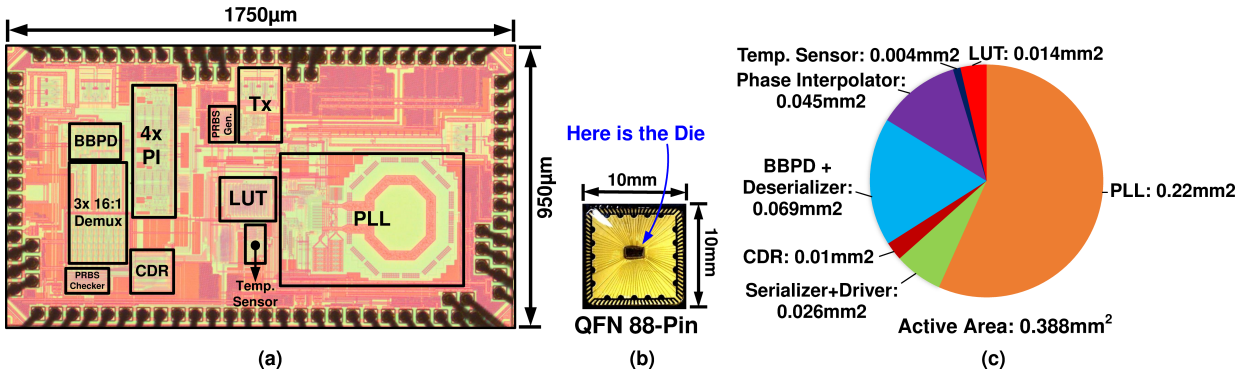


Figure 5.13: (a) Die micrograph of the proposed transceiver. (b) Die packed in 88-pin QFN package. (c) Active area break-up of the proposed transceiver.

5.4 Measurement Results

The prototype transceiver was implemented in a 65nm CMOS process, and the die micrograph is shown Fig. 5.13(a). The chip was packaged in a 10mm x 10mm 88-pin QFN plastic package (see Fig. 5.13(b)). The transceiver occupies an active area of approximately 0.39mm^2, and the area breakup is shown in Fig. 5.13(c). This chip operates on 1V and 1.1V supply (1.1V for BBPD and deserializer).

Because of large current steps during power-on/off events, the design of the power distribution network was done carefully. Several critical supplies, which experience large current steps, are bonded with multiple bonding wires to reduce the parasitic inductance. Both on-chip and off-chip decoupling capacitors were used. The total on-chip decoupling capacitor is approximately 1.5nF. Off-chip decoupling of every supply was done with 100nF, 1μF, and 10μF capacitors. Damping resistors of approximately 1-to-5 ohm are added in series on PCB to dampen out the ringing caused by bond wire inductance and decoupling capacitance. Off-chip voltage regulators manufactured by Analog Devices (part# ADP123) were used. Experimental results to quantify the transceiver performance in always-on and rapid-on/off modes are presented in the following subsections.

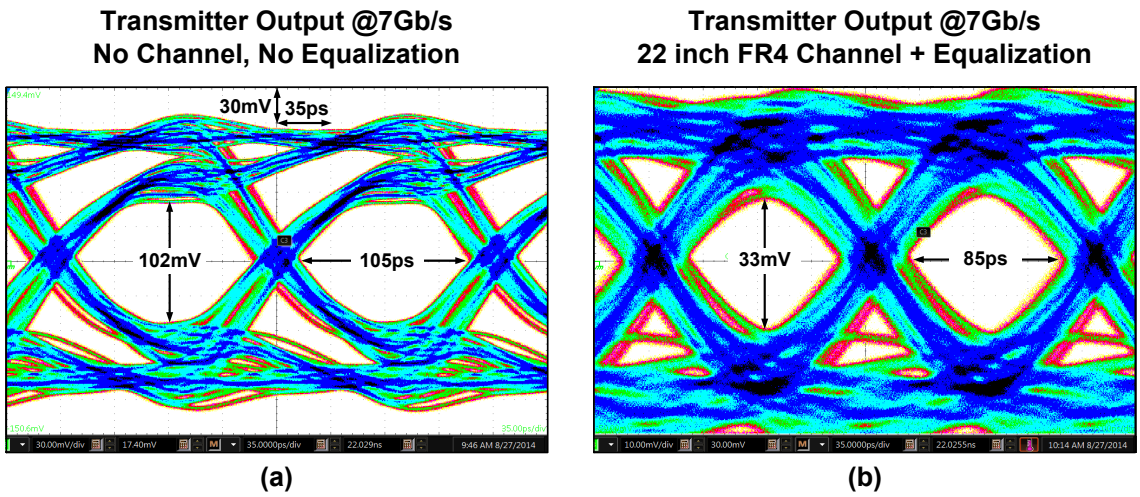


Figure 5.14: (a) Measured transmitter output eye at 7Gb/s without FFE in an always-on condition. (b) Measured transmitter output eye at 7Gb/s with FFE + 22 inch FR4 channel in an always-on condition.

5.4.1 Measurements in Always-On Mode

The measured single-ended eye diagram of the CML output driver is shown in Fig. 5.14(a). Transmitter output swing is 500mV(Diff_{pk-pk}) and single-ended horizontal and vertical eye openings are approximately 105ps and 102mV, respectively. This near-end transmitter measurement was done without enabling FFE. ISI present in the eye is due to package parasitic and impedance discontinuities on the PCB. For the transceiver operation, FFE pre-, main and post-taps are set to 0, 0.75 and -0.25, respectively. The measured single-ended eye diagram of the CML output driver at the end of a 22-inch FR4 channel is shown in Fig. 5.14 (b). FFE taps were enabled to achieve horizontal and vertical eye openings of 85ps and 33mV, respectively.

The measured bathtub plot from BERT-to-receiver is shown in Fig. 5.15. This measurement was performed by synchronizing the BERT clock with the receiver clock and sweeping phase interpolator codes in the CDR loop. For a BER of 1e-12, the measured eye opening is approximately 0.25UI.

The measured lock-in range of the CDR is ±2500ppm. The measured jitter on the recovered clock for 0ppm, 2500ppm, and -2500ppm frequency error is 4.8ps_{rms}, 7.6ps_{rms}, and 8.3ps_{rms}, respectively, as shown in Fig. 5.16.

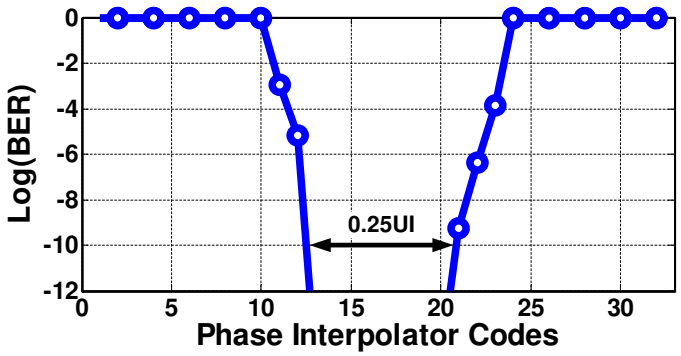


Figure 5.15: Measured bathtub plot of receiver at 7Gb/s in always-on condition.

Figure 5.17 shows the measured CDR's jitter tolerance (JTOL) curve in an always-on condition (steady-state CDR locked condition). JTOL corner frequency is approximately 2MHz. High-frequency JTOL is limited primarily by the ISI caused by package parasitics.

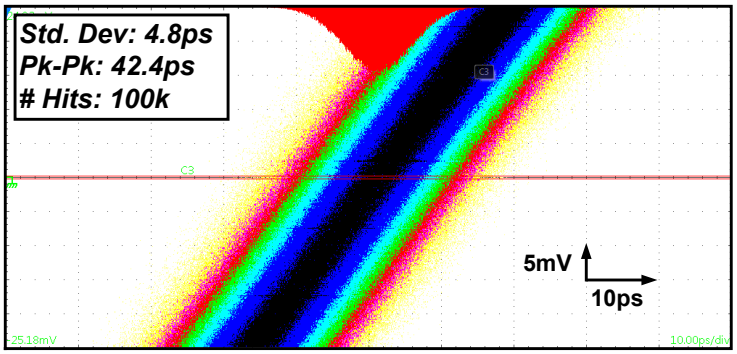
Figure 5.18 shows the measured CDR's jitter tolerance (JTOL) curve in an always-on condition with three different gain settings. Gain setting-1 corresponds to the highest CDR loop gain. The gain is reduced by 2 for gain setting-2, and the gain is further reduced by 2 for the gain setting-3.

Figure 5.19 shows recovered eye of the data at 1.75Gb/s in an always-on condition. Figure 5.20 shows jitter of the recovered data in an always-on condition for various CDR loop gain settings. Measured jitter for the gain setting-1 is $9.8\text{ps}_{\text{rms}}$, gain setting-2 is $6.2\text{ps}_{\text{rms}}$, gain setting-3 is $5.3\text{ps}_{\text{rms}}$, and automatic gain setting is $5.9\text{ps}_{\text{rms}}$.

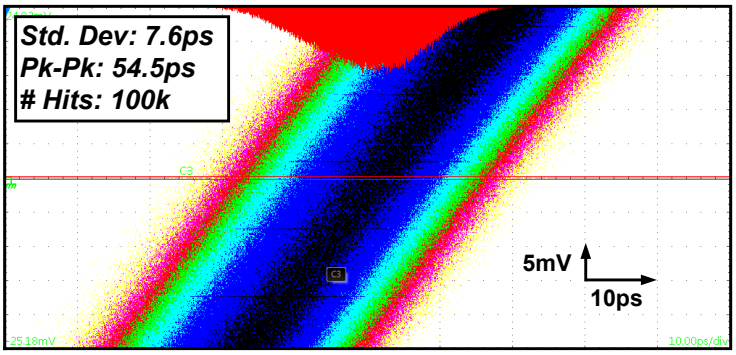
The transceiver power breakup in the always-on and always-off states is shown in Figs. 5.21(a) and 5.21(b), respectively. Operating at 7Gbps, the transceiver consumes 63.7mW of which the serializer and output driver consume nearly 45% of the total power. The power consumption in the off-state is only 740μW, which is approximately 1.16% of the on-state power. Leakage in the BBPD and de-serializer blocks makes up a 61% of off-state power consumption.

5.4.2 Measurements in Rapid-On/Off Mode

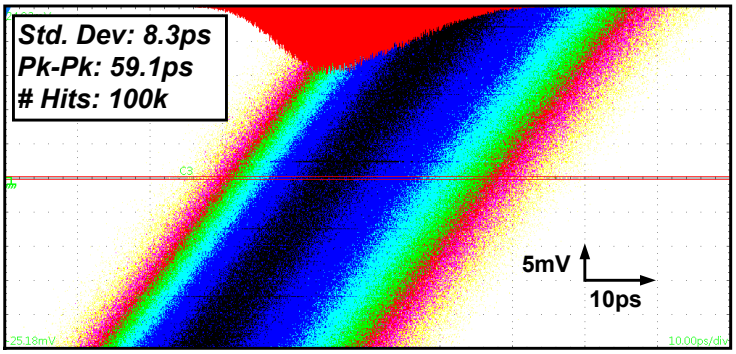
The measured transmitter settling transient during power-on/off cycle is shown in Fig. 5.22. The transmitter powers-on within 500ps. It can be observed that the common-mode drops



(a)



(b)



(c)

Figure 5.16: Measured recovered clock jitter at 1.75GHz for various frequency error between the BERT and the CDR. (a) Frequency error of 0ppm. (b) Frequency error of 2500ppm. (c) Frequency error of -2500ppm.

when the START signal is asserted high, and the common-mode goes to V_{DD} when the START signal is de-asserted.

Measurement capturing the successful transmission and reception of data in rapid-on/off mode is performed using two separate test chips. For this measurement, one chip was configured as the transmitter while the other chip was configured as the receiver. The chips

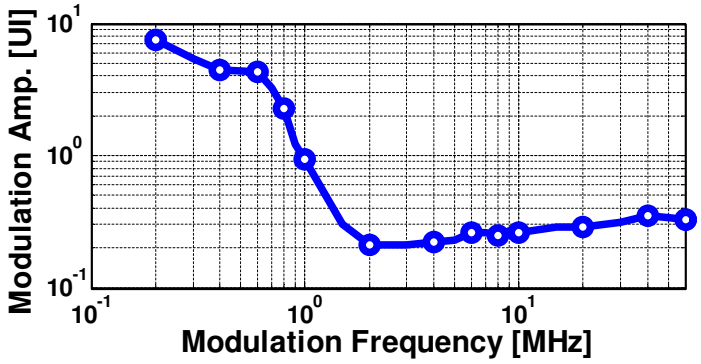


Figure 5.17: Measured jitter tolerance of the CDR at 7Gb/s in automatic gain control setting.

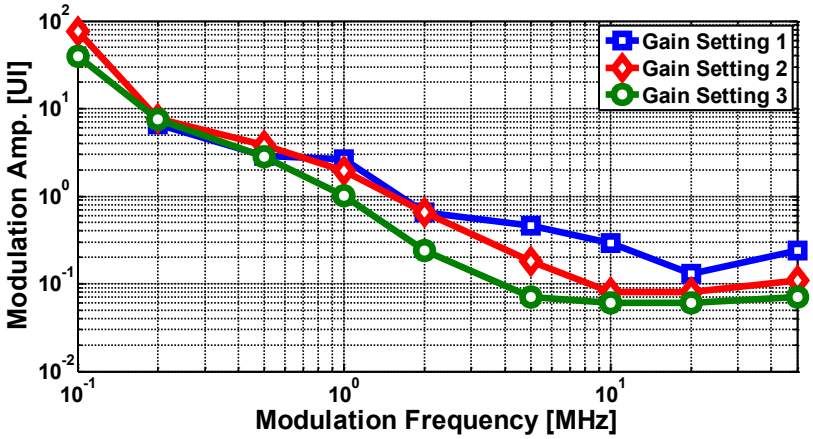


Figure 5.18: Measured jitter tolerance of the CDR at 7Gb/s with various gain settings.

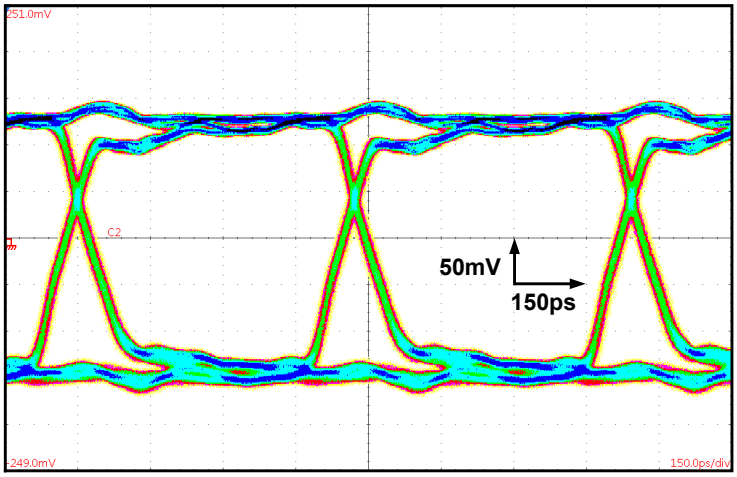


Figure 5.19: Measured received data eye at 1.75Gb/s.

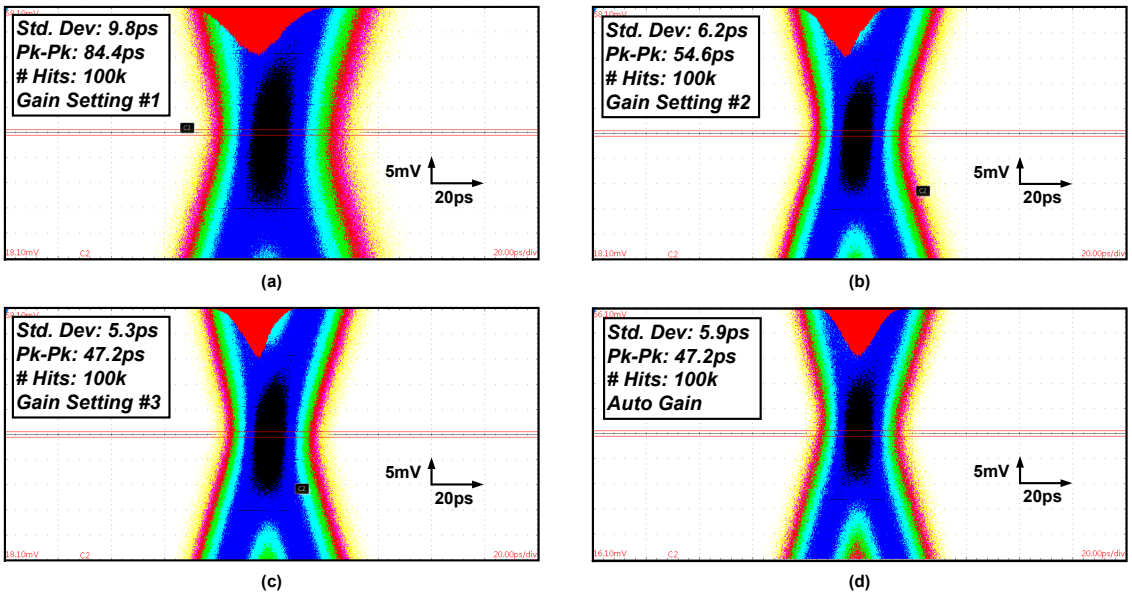


Figure 5.20: Measured jitter of the recovered data in various CDR gain settings. (a) Gain setting-1. (b) Gain setting-2. (c) Gain setting-3. (d) Automatic gain selection.

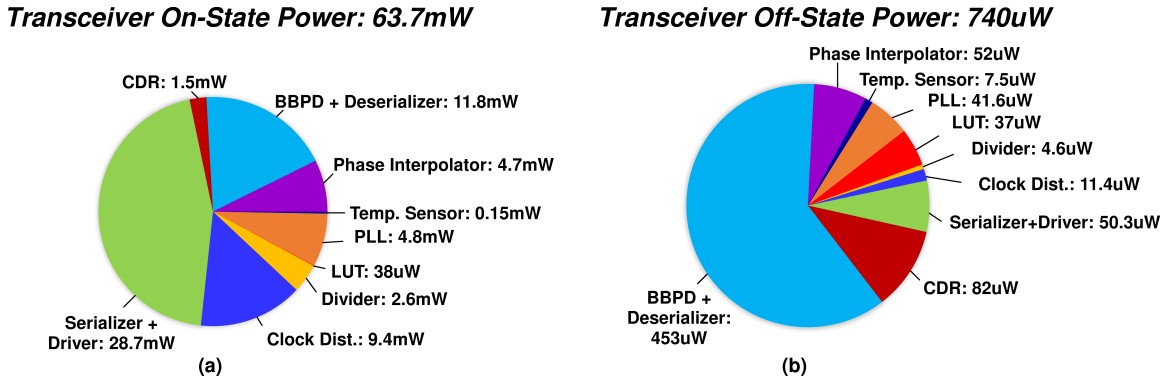


Figure 5.21: (a) Measured transceiver power breakup in an always-on state. (b) Measured transceiver power breakup in an always-off state.

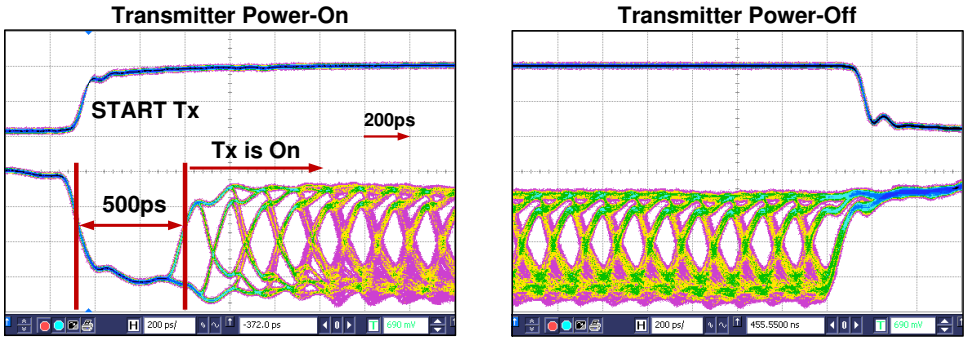


Figure 5.22: Measured CML output driver power-on/off transient.

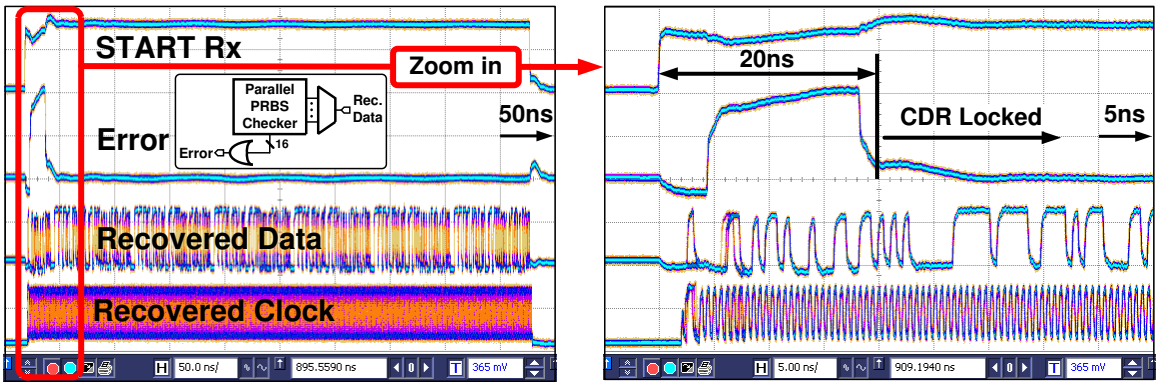


Figure 5.23: Measured transceiver power-on/off transient at 7Gb/s.

were connected by a channel consisting of 3.2-inch FR-4 trace, 6-inch SMA cable, and QFN package. PRBS7 data was transmitted and recovered in this experiment. Approximately 4Billion on/off transactions are captured using an oscilloscope as shown in Fig. 5.23. The duration of each transaction is 450ns. Observed signals at the output of the receiver are: START Rx, Error, Recovered Data, and Recovered Clock. The Error signal is used as an indicator to check if the CDR has locked to the PRBS pattern [54]. In these measurements, the Error signal goes low in less than 20ns (in less than 140bits). PRBS checker seeding latency, which is approximately 3 to 4 CDR clock cycles (≈7-9ns), is included in the observed power-on-lock time of 20ns. A small portion of this time (≈2-3ns) is contributed by the PI+PLL power-on time. We think that the remaining power-on time could be attributed to a power-supply glitch, which could have moved the optimum sampling phase of the CDR to the sub-optimal position because of START Rx generator's sensitivity to supply voltage. Given the 20ns of power-on-lock time, it may not be beneficial to power-off the link if the idle time between very long active times (say 100s of milliseconds) is small (say 20ns).

Figure 5.24 shows the measured power-on-lock time of CDR plotted as a function of the PI starting phase. In this measurement, PI starting code (Φ_{PI} in Fig. 5.8) was swept across 32 codes and the power-on-lock time was measured by observing the Error signal. CPCL helps the CDR to start with the optimal PI code, which ensures minimal power-on-lock time (less than 20ns in this case). If DGCL is used alone, i.e. CPCL is switched-off, the phase of the incoming data will be random with respect to the sampling clock and the measured worst-case power-on-lock time is 180ns.

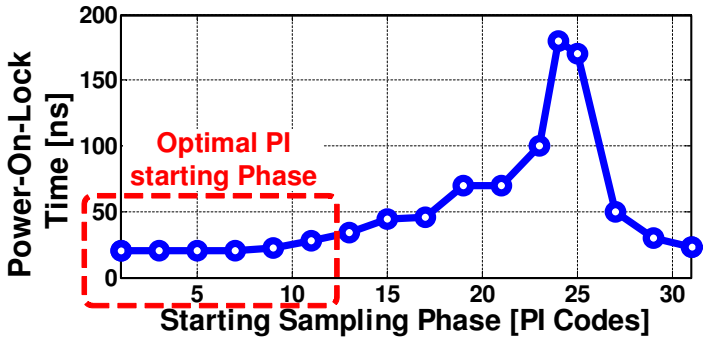


Figure 5.24: Measured power-on-lock time versus starting PI-phase.

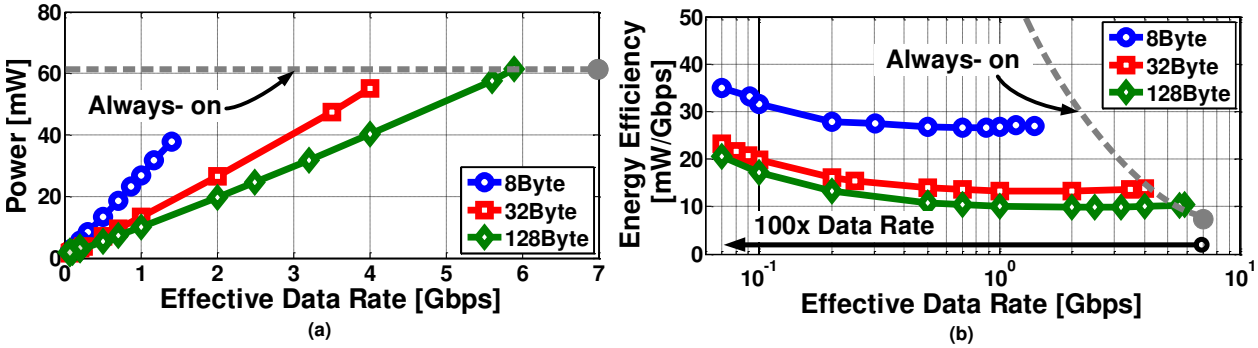


Figure 5.25: (a) Measured transceiver power versus effective data rate. (b) Measured transceiver energy-per-bit versus effective data rate.

The measured transceiver power and energy efficiency is plotted as a function of the effective data rate in Figs. 5.25(a) and 5.25(b), respectively for 8-, 32-, and 128-byte data burst lengths. Effective data rate was obtained by duty cycling the transceiver and is equal to

$$\text{Effective Data Rate} = \frac{\text{Bits transmitted during on-state}}{\text{On-state time} + \text{Off-state time}} \tag{5.6}$$

For the 128-byte burst, a 100x change in the data rate, i.e. from 7 Gb/s to 70Mb/s, the power scales by 44x from 63.7mW to 1.43mW and the energy efficiency changes only by 2.2x from 9.1pJ-per-bit to 20.5pJ-per-bit. This demonstrates the energy proportional feature of the proposed transceiver.

Table 5.1 compares the proposed transceiver with state-of-the-art designs. To the best of our knowledge, the proposed transceiver is the first reported embedded clock architecture with a power-on-lock time of less than 20ns.

Table 5.1: Performance Comparison of the Proposed Transceiver with State-of-the-Art Designs

	This Work	[14]VLSI'11	[15]JSSC'10
Architecture	**Embedded clock**	Forwarded clock	Forwarded clock
Technology	**65nm GP**	40nm LP	40nm LP
Supply[V]	**1/1.1**	N/A	1.1
Data Rate[Gb/s]	**7**	2.5-5.6	2.7-4.3
Power-on-Lock Time[ns]	**Less than 20ns**	8	241.8
Energy Efficiency[pJ/bit]	**9.1**	2.4	3.3
On-State Power[mW]	**63.7**	13.4	14.2
Off-State Power[μW]	**740**	0	50
De/ Serialization ratio	**16:1**	N/A	8:1
Output Swing[mV]	**500($\mathbf{Diff_{pk\text{-}pk}}$)**	N/A	200($Diff_{pk\text{-}pk}$)
Area[mm^2]	**0.39**	N/A	N/A

5.5 Conclusion

The fine-grained rapid power state transition technique is used to reduce the overall serial link power. Architectural design techniques for achieving fast power-on in the transmitter and fast power-on-lock in the receiver were presented. The prototype fast power-on-lock transceiver with embedded clock architecture was fabricated in 65nm CMOS technology and occupies an active die area of 0.39mm^2. It achieves power-on-lock in less than 20ns and consumes 63.7mW/740μW on/off-state power from 1 and 1.1V supply. The proposed transceiver demonstrates power scalability with link utilization and achieves energy proportional operation. To the best of our knowledge, this is the first reported measured results and techniques of rapid-on/off transceiver for embedded clock architecture.

CHAPTER 6

A HIGHLY DIGITAL TEMPERATURE-TO-FREQUENCY-TO-DIGITAL BASED TEMPERATURE SENSOR

Modern day processors and DRAMs utilize several on-chip temperature sensors for thermal monitoring [55]. In the case of processors, temperature sensor helps to maintain performance and reliability by monitoring both the cold and hot spots [56]. On-the-other-hand, DRAMs control the rate of self-refresh operations based on current die temperature to save power [57]. Since it is difficult to predict hot spot locations during the design phase, microprocessors incorporate as many as 10 or more sensors per-core [58]. With the increase in the number of cores-per-processor each year [59] fueled by the ever-growing computational demand, the number of temperature sensors in the processor will continue to increase. Therefore, an efficient and low-cost temperature sensor suitable for integration in processors and DRAMs is highly needed.

Sensors must incorporate several key features to make them amenable for use in processors. First and foremost, sensors must be small and compact so that they can be placed very close to hot spots. A sensor designed to operate with the local (logic) supply voltage helps in reducing the overhead of routing a separate dedicated power supply. However, because of the constant switching of logic gates, the logic supply is very noisy, as shown in Fig. 6.1. Furthermore, due to the use of the dynamic voltage scaling algorithm (DVS) in modern processors, the logic supply voltage varies. Therefore, the sensor must be immune to supply voltage variations [60]. SoCs and processors also employ a dynamic frequency scaling algorithm (DFS), where the switching frequency is scaled to trade power with performance. The use of both dynamic voltage and frequency scaling (DVFS) algorithms constrains the temperature sensor design in such a way that the sensor can no longer rely on using external frequency or supply voltage as a reference. Routing a dedicated reference frequency, voltage and bias current to temperature sensors all over the processor is an expensive endeavor.

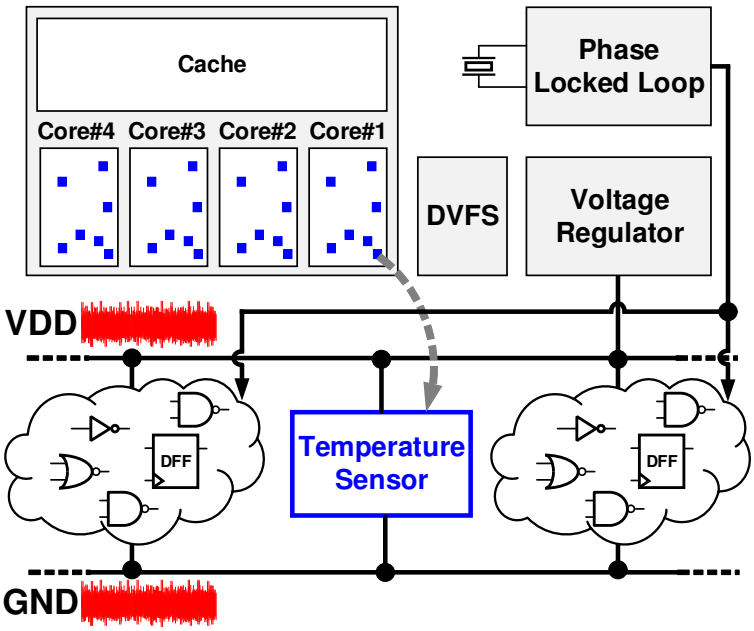


Figure 6.1: An example of a temperature sensor integrated inside a processor.

Therefore, the temperature sensor must be self-referenced. Finally, the temperature sensor architecture should be such that it is relatively easy to design and port to different process nodes.

Several all-CMOS based sensor architectures have been proposed to meet the above-mentioned requirements. DTMOST based sensors [61] offer high accuracy, low power, and sub-1V operation, but occupy a large area. Delay based sensors employing TDCs and DLLs scale well with the technology nodes. However, area penalty due to large delay lines [62–64], requirements for an external reference clock [65–67], need for operational amplifiers [68] and voltage regulators [69], could hinder their integration in processors. Given these drawbacks, we present a highly-digital VCO-based self-referenced sensor with digital readout, reduced supply sensitivity, and compact size.

Fabricated in a 65nm CMOS process, the proposed sensor [46] with a digital readout circuit occupies an active area of 0.004mm^2. The sensor achieves supply sensitivity of 0.034°C/mV. Operating from a 1V supply, measurement time can be as fast as $6.5\mu\text{s}$, for a quantization error of 1°C, resolution of 0.3°C, and a resolution FoM [70] of $0.3(\text{nJ/conv})\text{res}^2$. With two-point calibration at extreme temperatures (compatible with processor testing [56]), the proposed sensor achieves peak-to-peak non-linearity with and without polynomial correction

of ±0.9°C and ±2.3°C, respectively over a 0°C to 100°C temperature range. With one-point calibration, the sensor achieves peak-to-peak non-linearity with and without polynomial correction of ±3.3°C and ±4.3°C, respectively.

The rest of the chapter is organized as follows. Section 6.1 introduces the proposed temperature sensor concept. Design details for making the sensor less sensitive to the supply voltage variations is described in Section 6.2. Architecture and circuit details of the sensor are presented in Section 6.3. Section 6.4 analyzes the effect of VCO phase noise on achievable sensor resolution. Section 3.5 presents the measured results. Section 5.5 concludes the chapter.

6.1 Temperature Sensor Concept

The proposed sensor works on the principle of measuring oscillation frequency, from two different ring oscillators (sensing elements), each having different temperature sensitivity. The ratio of oscillator frequencies, when digitized, represents the temperature. Temperature affects the frequency of a CMOS ring oscillator either through mobility or through the threshold voltage variations. Mathematically, frequency of a ring oscillator, to a first-order approximation, is inversely proportional to the delay of the delay stage ($1/RC_L$), and can be expressed as [71]:

$$F_{VCO} \propto \frac{4}{3}\frac{\mu C_{ox} W/L (V_{DD} - V_{TH})^2}{V_{DD}\left(1 - \frac{5}{6}\lambda V_{DD}\right) C_L} \tag{6.1}$$

where μ is the mobility of electrons/holes, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of the MOS transistors, V_{DD} is the supply voltage of oscillator, V_{TH} is the average threshold voltage of transistors used in the delay stage (assuming NMOS and PMOS have the same threshold voltage), λ is the channel length modulation parameter, and C_L is the load capacitance of the delay stage. Mobility and threshold voltage as a function of temperature (Temp) can be written as:

$$\mu \propto \mu_0 (Temp/T_0)^{-p} \tag{6.2}$$

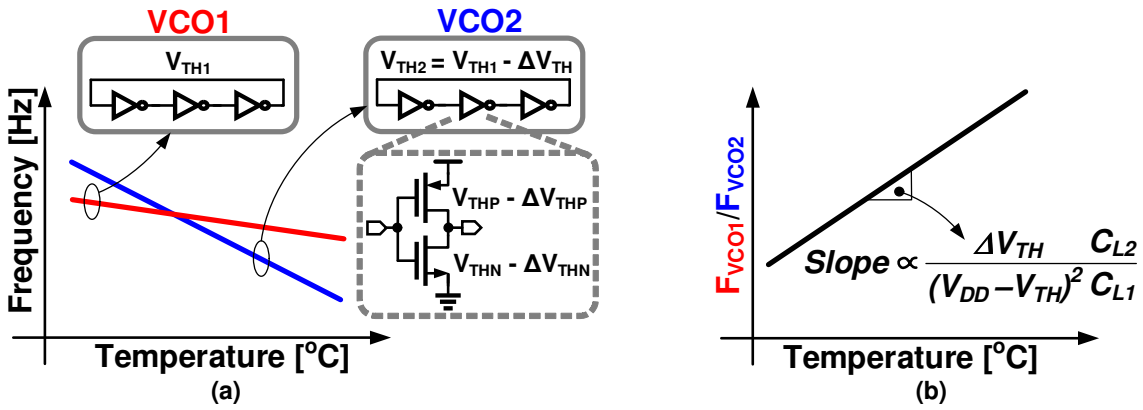


Figure 6.2: Operating principle of the proposed sensor. (a) VCO1 and VCO2 frequency versus temperature. (b) Ratio of VCO1 frequency over VCO2 frequency versus temperature.

$$V_{TH} = V_{TH0} - k(Temp - T_0) \tag{6.3}$$

where p is a fitting parameter typically in the range of 1.2 to 2.0, μ_0 is the mobility at room temperature T_0, V_{TH0} is the threshold voltage at room temperature, and k is approximately in the range of 1 to 3mV/°C.

The temperature sensitivity of an oscillator can be modified by either changing the mobility, threshold voltage or the supply voltage. The designer has no direct control over the mobility, and it is often cumbersome to route two separate power supply rails to a sensor placed deep inside a processor. Therefore, in this design, threshold voltage is used to create temperature sensitivity difference. The proposed sensor incorporates two ring oscillators: VCO1 and VCO2, each having different temperature sensitivities, as shown in Fig. 6.2(a). VCO2 is designed with transistors having smaller threshold voltage as compared to VCO1. That is, the PMOS and NMOS pair in VCO2 has smaller threshold voltage compared to the PMOS and NMOS pair in VCO1. As a result, the effect of mobility variation due to temperature on VCO2 frequency is more dominant than that on VCO1. Consequently, the frequency versus temperature plot of VCO2 has a steeper slope as compared to VCO1 (see Fig. 6.2(a)).

The ratio of frequencies of VCO1 and VCO2, F_{VCO1}/F_{VCO2}, exhibits the desired PTAT characteristic (see Fig. 6.2(b)). This ratio is digitized to obtain the digital output proportional

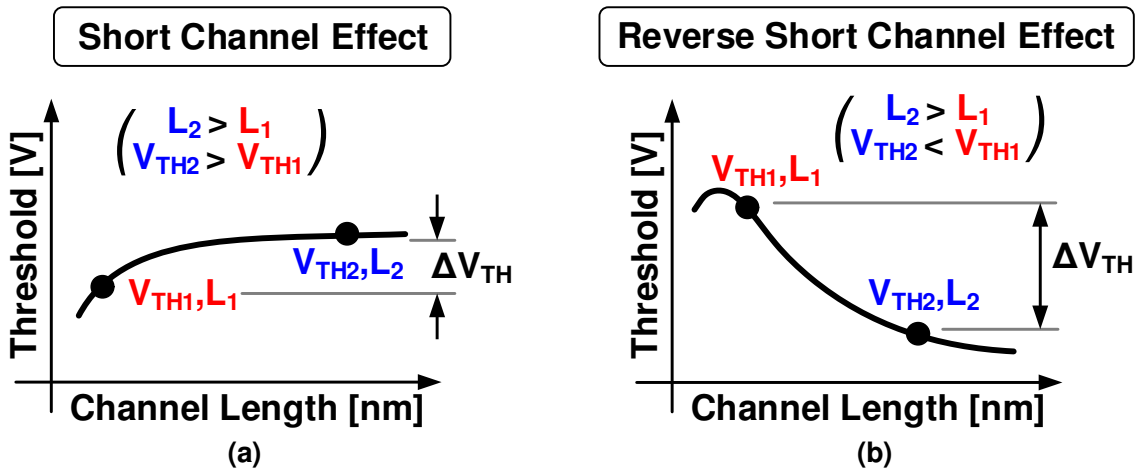


Figure 6.3: (a) Effect of channel length on threshold voltage due to short channel effects. (b) Effect of channel length on threshold voltage due to reverse short channel effects.

to the temperature. In the proposed sensor, the frequency ratio is digitized with the help of a digital logic (explained in Section 6.3). Unlike conventional time-based sensors, the proposed sensor, once calibrated, can operate without the help of an external reference frequency or voltage.

Threshold voltage difference between VCO1 and VCO2 can be introduced in several ways. Primary among them is body biasing the transistors or using two flavors of transistors, i.e. high/low threshold voltages together with the nominal threshold voltage transistors. Body bias may require analog components such as a band-gap reference and voltage regulators to generate and buffer reference voltages. On the other hand, using two flavors of transistors requires an extra mask during the fabrication process. Therefore, in the proposed sensor, reverse short channel effect (RSCE) is leveraged to create a threshold voltage difference. The difference between short channel effect and reverse short channel effect is illustrated in Fig. 6.3. In the case of short channel effect, threshold voltage reduces as the channel length decreases (see Fig. 6.3(a)). On the other hand, reverse short channel effect [72] increases the threshold voltage as the channel length decreases (see Fig. 6.3(b)). Reverse short channel effect happens due to the presence of halo implants in planar devices. In 65nm CMOS, reverse short channel effect is dominant and is, therefore, used to create a difference in the threshold voltages.

In this design, threshold voltage difference was created by using longer channel length

transistors in VCO2 as compared to the transistors used in VCO1. In the case of advance technology nodes where reverse short channel effect is weak or absent, two flavors of transistors could be used to design this sensor.

6.2 Making Sensor Less Sensitive to Supply Voltage Variations

The frequency ratio F_{VCO1}/F_{VCO2} is sensitive to the supply voltage. Mathematically, to a first order, it can be written as:

$$\frac{F_{VCO1}}{F_{VCO2}} \propto \frac{(V_{DD} - V_{TH1})^{\alpha} C_{L2}}{(V_{DD} - V_{TH2})^{\alpha} C_{L1}} \tag{6.4}$$

where V_{TH1} and V_{TH2} are the threshold voltages of transistors in VCO1 and VCO2, C_{L1} and C_{L2} are the load capacitance of the delay stages in VCO1 and VCO2, and α is from the α-power law model [19] ($\alpha \approx 1$ for sub-micron CMOS process). Since the threshold voltage of transistors in VCO1 is larger than that of in VCO2 by ΔV_{TH}, (6.4) can simplified as:

$$\frac{F_{VCO1}}{F_{VCO2}} \propto \left(1 - \frac{\Delta V_{TH}}{V_{DD} - V_{TH}}\right)^{\alpha} \frac{C_{L2}}{C_{L1}} \tag{6.5}$$

where V_{TH} is the threshold voltage of transistors in VCO2. This expression consists of two terms. The first term, which is inside the bracket has a positive sensitivity to the supply voltage, i.e. F_{VCO1}/F_{VCO2} increases as the supply voltage increases, as shown in Fig. 6.4(a).

The second term is the ratio: C_{L2}/C_{L1} where, C_{L2} and C_{L1} are the load capacitances seen at the output node of the delay cells used in VCO1 and VCO2, respectively. In the proposed sensor, the load capacitance ratio is designed such that it has negative sensitivity to the supply voltage, as shown in Fig. 6.4(b). The combined effect of both these terms is such that the ratio F_{VCO1}/F_{VCO2} is made less sensitive to supply voltage variations (see Fig. 6.4(c)).

The load capacitance of a typical delay cell consists of a gate-to-source capacitance (C_{GS}), gate-to-drain capacitance (C_{GD}), wire capacitance (C_W) and drain-to-bulk capacitance (C_{DB}). Of these capacitors, C_{DB} is due to the reverse biased pn junction, and it

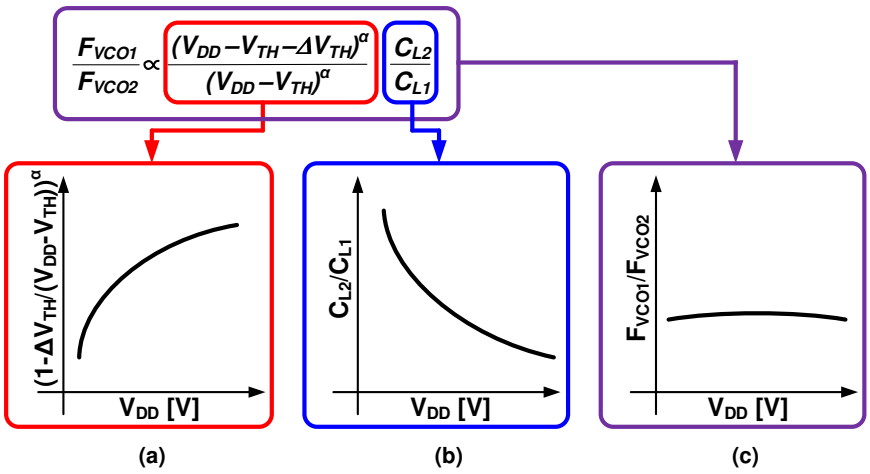


Figure 6.4: Concept of designing supply insensitive sensor. (a) The first term has a positive supply sensitivity. (b) The second term has a negative supply sensitive. (c) Supply insensitivity is achieved in frequency ratio.

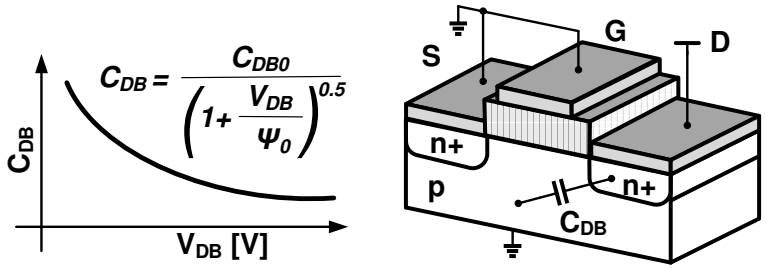


Figure 6.5: Drain to bulk junction capacitance (C_{DB}) versus reverse bias voltage.

reduces when the reverse bias voltage across the pn junction increases [73], as illustrated in Fig. 6.5. In the proposed sensor, delay cells of VCO2 are designed such that the C_{DB} dominates the total load capacitance. The size of C_{DB} in VCO2 was chosen such that supply sensitivity of the ratio of C_{L2}/C_{L1} cancels out the supply sensitivity of the first term. Consequently, the ratio F_{VCO1}/F_{VCO2} becomes less sensitive to supply voltage variations.

The effect of process variation on supply sensitivity is observed with the help of process corner simulation, as shown in Fig. 6.6(a). For a supply voltage variation of 0.85V to 1.05V at room temperature, the worst-case error in the temperature sensor occurs in the slow-slow (SS) corner. Simulated worst-case supply sensitivity is 0.046°C/mV for the SS corner. One thousand mismatched simulations were done for a typical corner at 0°C and 100°C, with supply varying from 0.95V to 1.05V, and the results are shown in Fig. 6.6(b) and Fig. 6.6(c), respectively. At 0°C, and 100°C, the standard deviation of the error is 0.005°C/mV.

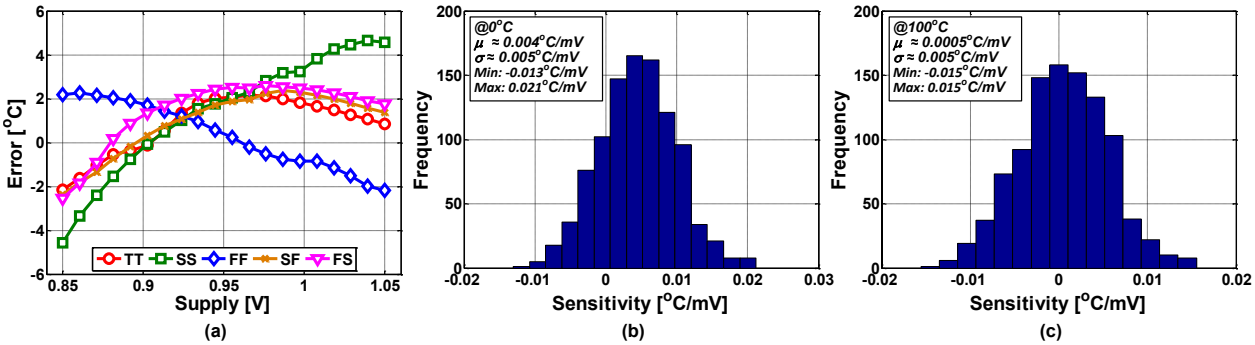


Figure 6.6: (a) Simulated supply sensitivity across process corners at room temperature. (b) Simulated supply sensitivity with 1000 mismatched simulations at TT corner, 0°C with ±50mV DC supply voltage variation. (c) Simulated supply sensitivity with 1000 mismatched simulations at TT corner, 100°C with ±50mV DC supply voltage variation.

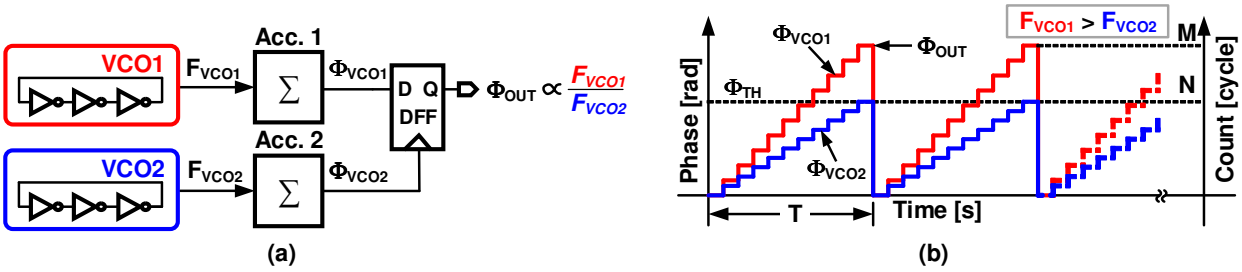


Figure 6.7: (a) Simplified architecture of the proposed temperature sensor. (b) Phase versus time plot of the proposed architecture.

6.3 Temperature Sensor Architecture

The goal of the proposed sensing technique is to design the sensor architecture with all digital logic gates so as to make the design compact, amenable to technology scaling, and portable. A simplified sensor architecture is shown in Fig. 6.7(a). The proposed sensor consists of two VCOs followed by an accumulator and a latch. Accumulator-1 and Accumulator-2 accumulates the VCO1 and VCO2 frequency to produce output phase Φ_{VCO1} and Φ_{VCO2}, respectively. Graphical representation of accumulation of phase in VCO1 and VCO2 versus time is shown in Fig. 6.7(b). When Accumulator-2 output (Φ_{VCO2}) reaches threshold N (Φ_{TH}), output of Accumulator-1 (Φ_{VCO1}) is latched (M). Mathematically the phase of Accumulator-1 at the sampling instant equals:

$$\Phi_{OUT} = 2\pi F_{VCO1} T \tag{6.6}$$

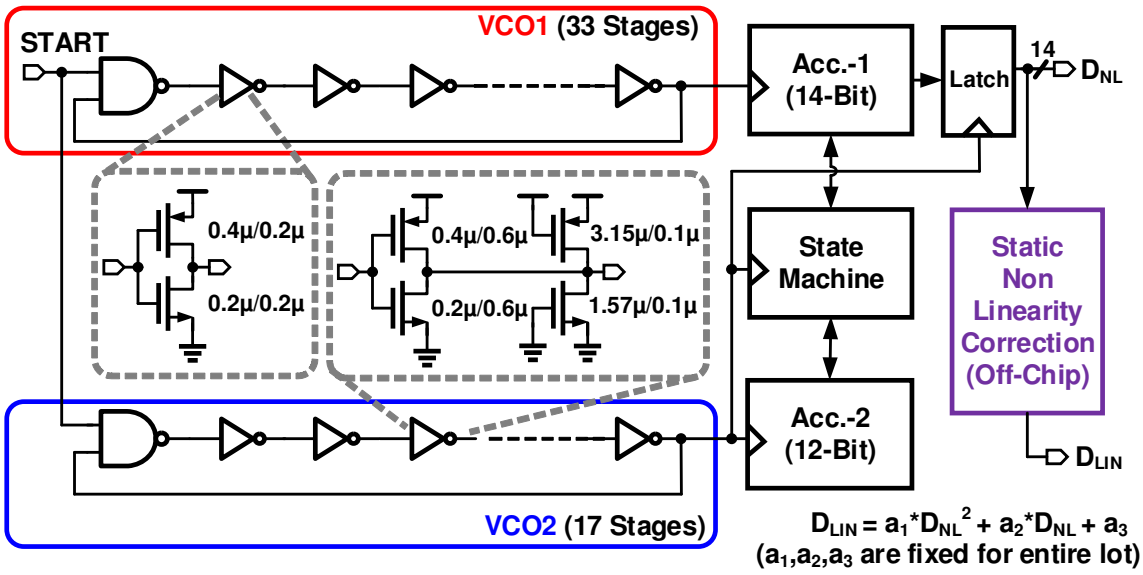


Figure 6.8: Proposed temperature sensor architecture.

where F_{VCO1} is the oscillation frequency of VCO1, and T is the measurement interval. The relationship between the measurement time T, and programmable threshold count N can be established with the following expression:

$$\Phi_{TH} = 2\pi F_{VCO2} T \tag{6.7}$$

where F_{VCO2} is the VCO2 oscillation frequency. Dividing (6.6) by (6.7) we get

$$\Phi_{OUT} = \Phi_{TH} \frac{F_{VCO1}}{F_{VCO2}} \tag{6.8}$$

It can be observed from (6.8) that Φ_{OUT} is proportional to the ratio of VCO frequencies. Thus, the F_{VCO1}/F_{VCO2} ratio can be obtained with the help of a simple accumulate and latch operation.

6.3.1 Detailed Architecture

Detailed sensor architecture is shown in Fig. 6.8. VCO1 consists of 33 inverter stages while VCO2 consists of 17 inverter stages. A larger number of delay stages increases the delay through the loop and lowers the oscillation frequency. Low oscillation frequency helps to

reduce the power dissipation in the synthesized digital processing blocks such as counters and state machine. However, this power reduction comes at the cost of increased conversion time.

Bit widths of Accumulator-1 and Accumulator-2 directly affect the accuracy with which F_{VCO1} and F_{VCO2} are measured. Frequency measurement inaccuracy translates to the quantization step size. Wide accumulators help to accumulate the VCO phase for a longer period of time and reduce quantization error at the cost of increased measurement time and energy/measurement. In this design, accumulator size was chosen based on simulations to achieve a minimum quantization error of approximately 0.1°C. Accumulator-1 is 14 bits wide while Accumulator-2 is 12 bits wide. The quantization step size of the sensor is made programmable by adjusting Φ_{TH} (N). Since VCO1 and VCO2 are not synchronized, metastability could occur while sampling Φ_{OUT}. State machine, which operates on the VCO2 clock is designed to freeze the contents of Accumulator-1 before sampling, thus avoiding any metastable behavior.

The threshold voltage difference between the transistors used in the delay cells of VCO1 and VCO2 is created using the reverse short channel effect. Transistors in VCO2 are designed with 3x channel lengths ($L_2 = 600$nm) as compared to the transistors in VCO1 ($L_1 = 200$nm). In 65nm technology, 3x channel length difference helps to create a threshold voltage difference of approximately 33mV in NMOS and 30mV in PMOS at room temperature.

Supply sensitivity of the sensor is reduced by increasing the junction capacitance C_{DB} of delay stages in VCO2. It is accomplished by adding additional NMOS and PMOS transistors with their gates connected to ground and supply voltages, respectively. In this design, the size of these transistors was chosen based on simulations.

6.3.2 Systematic Non-Linearity Removal

Output of the sensor has a systematic non-linearity with respect to temperature. This non-linearity comes from the fact that the frequency ratio F_{VCO1}/F_{VCO2} has non-linear dependence on temperature. Assuming $\alpha \approx 1$ (for sub-micron CMOS process), (6.5) can be rewritten as

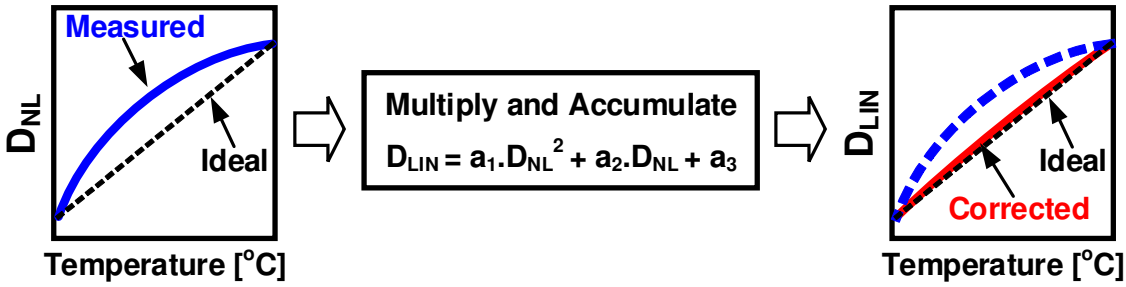


Figure 6.9: Systematic non-linearity correction concept.

$$\frac{F_{VCO1}}{F_{VCO2}} \propto \left(1 - \frac{\Delta V_{TH}}{V_{DD} - (V_{TH0} - k(Temp - T_0))}\right) \frac{C_{L2}}{C_{L1}} \tag{6.9}$$

The denominator is expanded with the help of Taylor series to get:

$$\frac{F_{VCO1}}{F_{VCO2}} \propto \left(1 - \frac{\Delta V_{TH}}{V_{DD} - V_{TH0} - kT_0} \sum_{n=0}^{\infty} \left(\frac{\text{-kTemp}}{V_{DD} - V_{TH0} - kT_0}\right)^n\right) \frac{C_{L2}}{C_{L1}} \tag{6.10}$$

It can be observed from (6.10) that F_{VCO1}/F_{VCO2} is a non-linear function of temperature.

A second-order polynomial correction helps to remove this non-linearity, as shown in Fig. 6.9. The polynomial correction block is a second-order multiply and accumulate unit. The input to the multiply and accumulate unit is a non-linear digital temperature sensor code, and output is a linear digital code. Simulation results suggest that a second-order polynomial with fixed coefficients can correct systematic non-linearity across corners, as shown in Fig. 6.10(a). After polynomial correction, the peak-peak error is ± 0.9°C. The effect of the mismatch on non-linearity is estimated with 1000 mismatched simulations at the typical corner, and the results are shown in Fig. 6.10(b). Simulated non-linearity before and after polynomial correction is approximately ± 1.6°C and ± 0.46°C, respectively.

In the present design, the polynomial correction is implemented off-chip. However, this logic can be easily synthesized on-chip, and can be shared among the several sensors present on a processor. Area overhead of such a synthesized block operating at 10MHz is 0.0042mm^2 in 65nm CMOS. The polynomial multiplication logic features three 13-bit fractional polynomial coefficients, 9-bit input and output, and can support more than 200 temperature sensors in a time multiplexed fashion.

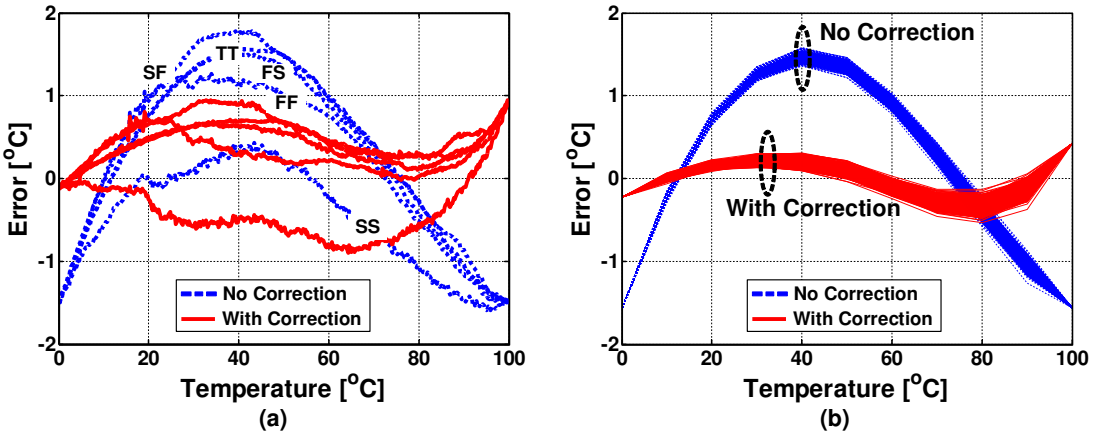


Figure 6.10: (a) Simulated nonlinearity across process corners at room temperature. (b) Simulated nonlinearity with 1000 mismatched simulations at TT corner.

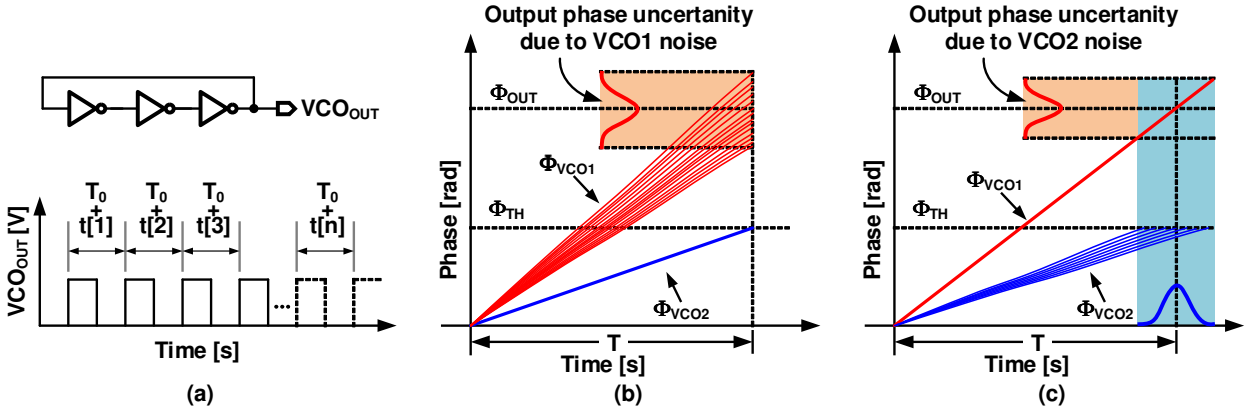


Figure 6.11: Effect of VCO phase noise on sensor resolution. (a) Period uncertainty in a VCO due phase noise. (b) Effect of VCO2 phase noise on the sampled output phase Φ_{OUT}. (c) Effect of VCO1 phase noise on the sampled output phase Φ_{OUT}.

6.4 Effect of Phase Noise on Sensor Resolution

Phase noise in a VCO manifests itself as jitter or uncertainty in the VCO time period, which eventually reduces the temperature sensor resolution. A graphical representation of the effect of VCO phase noise on the VCO time period is shown in Fig. 6.11(a). In this example, T_0 is the VCO time period, t denotes the random process representing VCO period jitter and t[n] denotes error in the n^{th} VCO period.

In the proposed sensor, phase noise of VCO1 introduces uncertainty in sampled phase Φ_{OUT} (see Fig. 6.11(b)). On the other hand, phase noise in VCO2 independently introduces

uncertainty in the time taken to reach Φ_{TH} (see Fig. 6.11(c)). Consequently, it results in the uncertainty in Φ_{OUT}. Phase noise of VCO1 and VCO2 are uncorrelated, and therefore, the effect of phase noise on sensor resolution is independently analyzed in this section.

6.4.1 Effect of VCO1 Phase Noise

Let us assume that the random variable P, which denotes period jitter of VCO1, is wide-sense stationary with zero mean, white PSD, and P[n] denotes error in the n^{th} VCO period. Let K denote the random process representing uncertainty in the sampled phase Φ_{OUT} and K_i denote the random variable representing uncertainty in the i^{th} temperature measurement period. Because the Accumulator-1 accumulates for M cycles and then resets, the output jitter sequence of this accumulator is of the form {(P[1] + P[2] + P[3] + ... + P[M]),(P[M+1] + P[M+2] + P[M+3] + ... +P [2M]),...}. Assuming VCO2 is noiseless, i.e. the sampling time T is constant, the variance of sampled output phase due to noise in VCO1 ($\Phi_{OUT\text{-}VCO1}$) is equal to the variance of K_i, which can be expressed as

$$\sigma^2_{Ki} = E[(P[1] + P[2] + ... + P[M])^2] \tag{6.11}$$

$$\sigma^2_{OUT\text{-}VCO1}[cycle^2] = \sigma^2_{Ki} = M\sigma^2_P \tag{6.12}$$

where σ^2_P is the variance of the period jitter of VCO1. σ^2_P can be estimated from the phase noise of VCO1 using the following expression

$$\sigma^2_P[cycle^2] = 2\left(\frac{1}{\pi}\right)^2 \int_0^\infty S\phi_1(f)\sin^2(\pi f T_1)df \tag{6.13}$$

where T_1 is the VCO1 time period, $S\phi_1(f)$ denotes the phase noise of VCO1, $\sin^2(\pi f\ T_1)$ is the mask to estimate period jitter from phase noise [74,75], as shown in Fig. 6.12. In (6.13), units of σ^2_P is $cycles^2$. In Section 6.4.2, σ_P will be multiplied by the quantization error to obtain σ_P in ^oC.

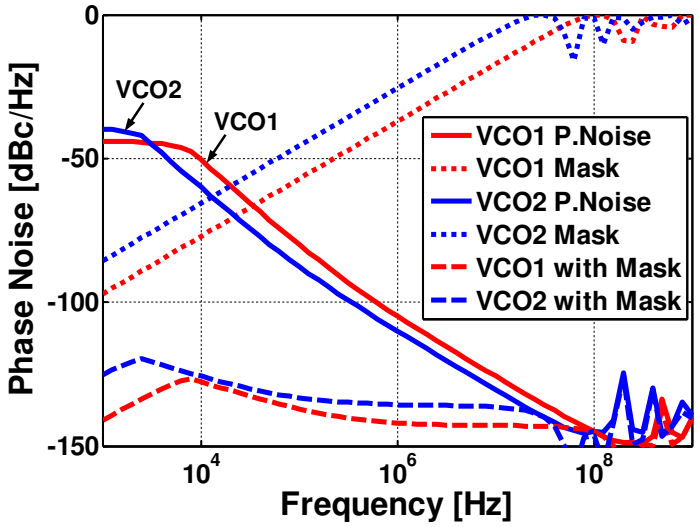


Figure 6.12: Simulated phase noise of VCO1 and VCO2 along with the filter mask to obtain period jitter.

6.4.2 Effect of VCO2 Phase Noise

Let us assume that the random variable L, which denotes period jitter of VCO2, is wide-sense stationary with zero mean and white PSD, and L[n] denotes error in the n^{th} VCO period. Let J denote the random process representing uncertainty in measurement time T and J_i denote the random variable representing uncertainty in the i^{th} measurement time. Because Accumulator-2 accumulates for N cycles and then resets, the output jitter sequence of this accumulator is of the form {(L[1] + L[2] + L[3] +...+ L[N]),(L[N+1] + L[N+2] + L[N+3] +...+ L[2N]),...}. Similar to (6.11), variance of J_i can be written as

$$\sigma^2_{Ji}[sec^2] = N\sigma^2_L \tag{6.14}$$

where σ^2_L is the standard deviation of the period jitter of VCO2. Here σ^2_L can be estimated from the phase noise of VCO2 using the following expression

$$\sigma^2_L[sec^2] = 2\left(\frac{T_2}{\pi}\right)^2 \int_0^\infty S\phi_2(f)\sin^2(\pi f T_2)df \tag{6.15}$$

where T_2 is the VCO2 time period, $S\phi_2(f)$ denotes the phase noise of VCO2, and $\sin^2(\pi f\ T_2)$ is the mask to estimate period jitter from phase noise, (see Fig. 6.12). Assuming VCO1 is

noiseless, using (6.15), variance of Φ_{OUT} due to VCO2 can be written as

$$\sigma^2_{\text{OUT-VCO2}}[\text{cycle}^2] = \mathrm{F}^2_{\text{VCO1}}\sigma^2_{\mathrm{Ji}} \tag{6.16}$$

Using (6.12) and (6.16), σ_{OUT} can be calculated as

$$\sigma_{\mathrm{OUT}}[\text{cycle}] = \sqrt{\sigma^2_{\text{OUT-VCO1}} + \sigma^2_{\text{OUT-VCO2}}} \tag{6.17}$$

The units of σ_{OUT} are converted to ^{o}C by multiplying (6.17) with the quantization step size [^{o}C/cycle].

$$\sigma_{\mathrm{OUT}}[^o\mathrm{C}] = \sigma_{\mathrm{OUT}}[\text{cycle}]\text{xQuantization}[^o\mathrm{C}/\text{cycle}] \tag{6.18}$$

Standard deviation of the measurement error due to phase noise is calculated to be approximately 0.06^{o}C and 0.17^{o}C for the case when the sensor is configured for a quantization error setting of 0.1^{o}C and 1^{o}C, respectively. In the present design, both VCOs consume approximately 60μW of power. A small value of σ_{OUT} (0.17^{o}C) compared to large quantization error (1^{o}C) indicates that there is an opportunity to reduce VCO power and bring σ_{OUT} close to the quantization error value.

6.5 Measurement Results

The proposed temperature sensor is fabricated in a 65nm CMOS process and operates with a supply voltage range of 0.85V to 1.1V (250mV). All measured results are reported with a supply voltage of 1.0V unless otherwise stated. The total area of this sensor is 0.004mm^2, as shown in the die micrograph in Fig. 6.13(a). The die was packaged in a 10mm x 10mm, QFN package.

A photograph of the lab test setup is shown in Fig. 6.13(b). The sensor package is mounted on an FR4 board and placed in a temperature chamber manufactured by Test Equity (model#107). Temperature inside the chamber was accurately measured using a calibrated sensor, manufactured by Analog Devices (part# ADT7420).

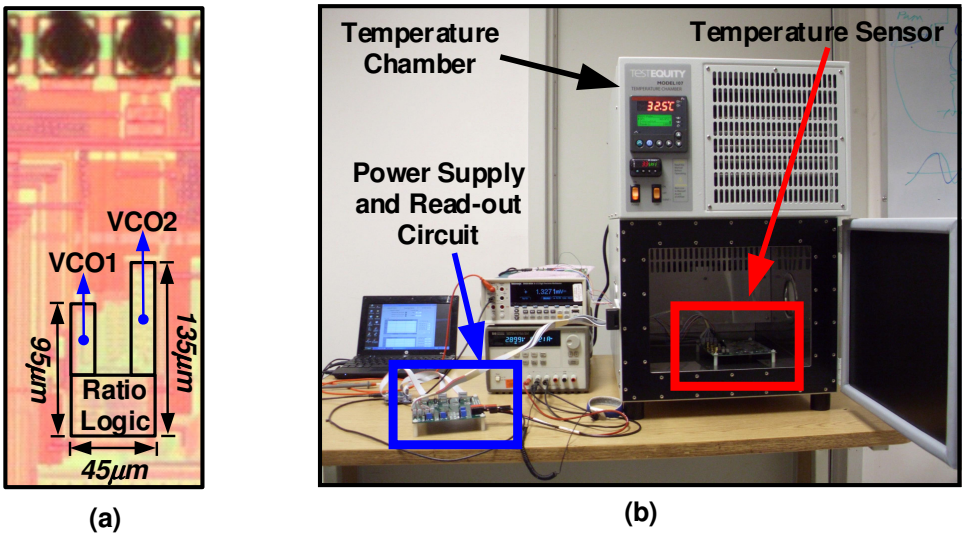


Figure 6.13: (a) Die micrograph of the proposed temperature sensor. (b) Test setup for the proposed temperature sensor.

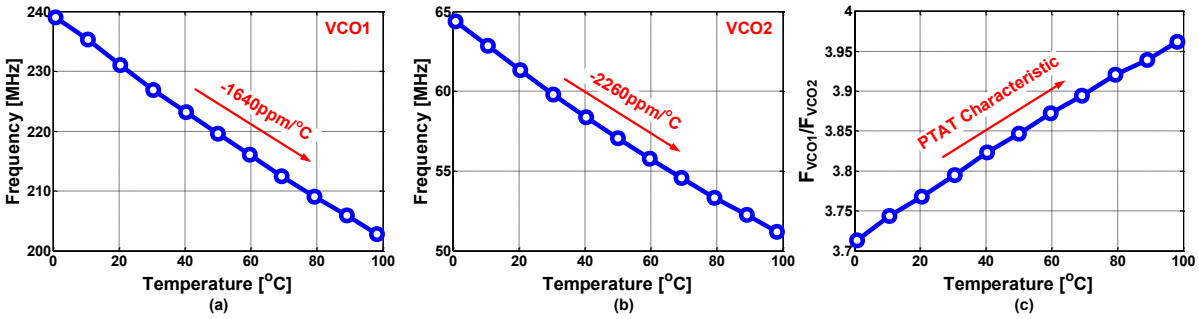


Figure 6.14: (a) Measured VCO1 frequency (F_{VCO1}) versus temperature. (b) Measured VCO2 frequency (F_{VCO2}) versus temperature. (c) Measured frequency ratio of VCO1 frequency over VCO2 frequency (F_{VCO1}/F_{VCO2}) versus temperature.

The sensitivity of VCO1 and VCO2 frequency to temperature is measured, and the results are plotted in Fig. 6.14(a) and Fig. 6.14(b), respectively. VCO1 frequency varies from 239MHz to 202.8MHz with a slope of approximately -1640ppm/°C for a temperature change from approximately 0°C to 100°C. VCO2 frequency varies from 64.37MHz to 51.2MHz with a slope of approximately -2260ppm/°C for a temperature change from approximately 0°C to 100°C. As designed, the negative slope of VCO2 is steeper compared to the negative slope of VCO1 because the threshold voltage of transistors in VCO2 is smaller. The ratio of frequencies of two VCOs shows the desired PTAT characteristics, as shown in Fig. 6.14(c).

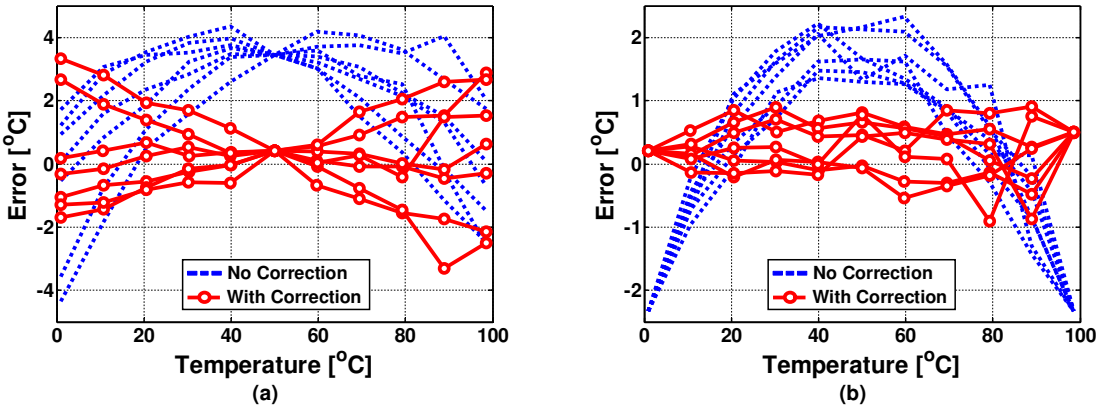


Figure 6.15: Measured linearity of seven test chips for (a) one-point calibration at 50°C with and without polynomial correction. (b) Two-point calibration at 0°C and 100°C with and without polynomial correction.

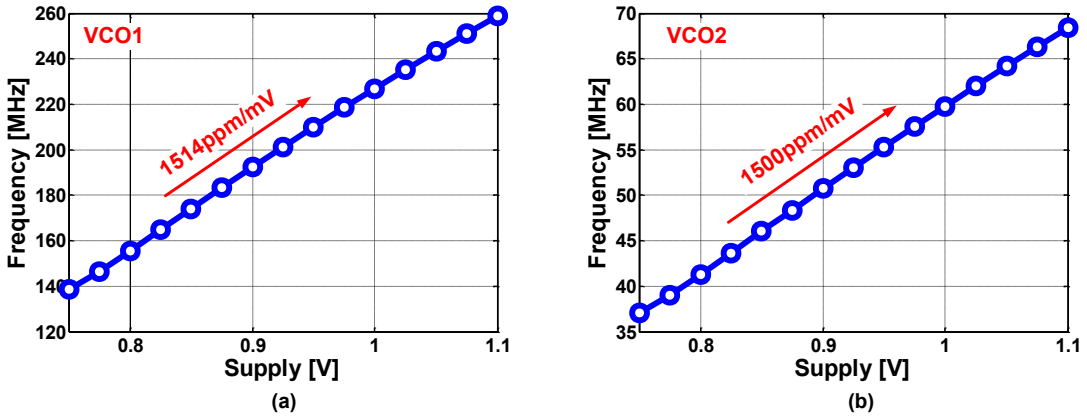


Figure 6.16: (a) Measured VCO1 frequency (F_{VCO1}) versus supply. (b) Measured VCO2 frequency (F_{VCO2}) versus supply.

The linearity of the proposed temperature sensor with one-point, and two-point calibration is shown in Fig. 6.15(a) and Fig. 6.15(b), respectively. With one-point calibration, at 50°C, measured peak-to-peak non-linearity with and without polynomial correction is ±3.3°C and ±4.3°C, respectively, over a temperature range of 0°C to 100°C. In the case of a two-point calibration, the calibration temperatures are 0°C and 100°C, and measured peak-to-peak non-linearity with and without polynomial correction is ±0.9°C and ±2.3°C, respectively.

The sensitivity of VCO1 and VCO2 frequency to supply voltage variation is measured, and the results are plotted in Fig. 6.16(a) and Fig. 6.16(b). VCO1 frequency varies from

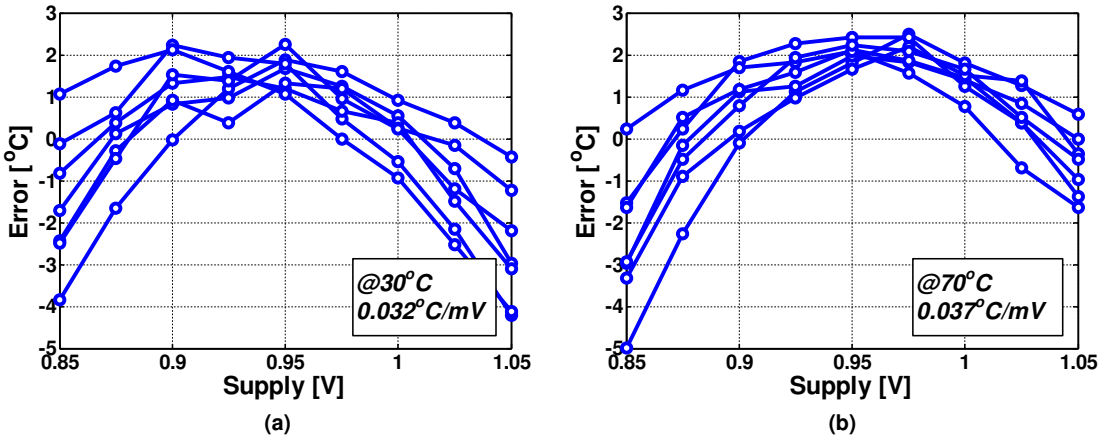


Figure 6.17: (a) Measured temperature sensor error versus supply voltage for seven test chips operating at 30°C. (b) Measured temperature sensor error versus supply voltage for seven test chips operating at 30°C.

138.5MHz to 258.8MHz with a slope of 1514ppm/mV for a supply voltage variation of 0.75V to 1.1V. VCO2 frequency varies from 37.04MHz to 68.38MHz with a slope of 1500ppm/mV for a supply voltage variation of 0.75V to 1.1V. It can be observed that both VCO1 and VCO2 have approximately the same sensitivity to the supply. The sensitivity of load capacitance (C_{DB}) of VCO2 to supply voltage helps to match the supply sensitivity of the two oscillators. Temperature sensor error due to supply voltage variation was measured for seven test chips at 30°C and 70°C, and the results are shown in Fig. 6.17(a) and Fig. 6.17(b). For these measurements, the supply voltage was varied by 200mV, ranging from 0.85V to 1.05V. At 30°C, the measured peak-to-peak supply sensitivity is 0.032°C/mV. At 70°C, the measured peak-to-peak supply sensitivity is 0.037°C/mV

Power consumption of the proposed sensor is measured across temperature, and the results are shown Fig. 6.18(a). Operating at 1V, the proposed temperature sensor consumes 154μW at room temperature. Power in the synthesized logic blocks is approximately 94μW while the VCOs consume approximately 60μW. In fine process nodes, logic power is expected to reduce and consequently, the sensor is expected to become more energy efficient. In case of end-of-the-road-map technologies, the sensor power will be dominated by the VCO power, which can be easily traded off with the desired resolution.

Leakage and active power component of the sensor are measured versus temperature, and

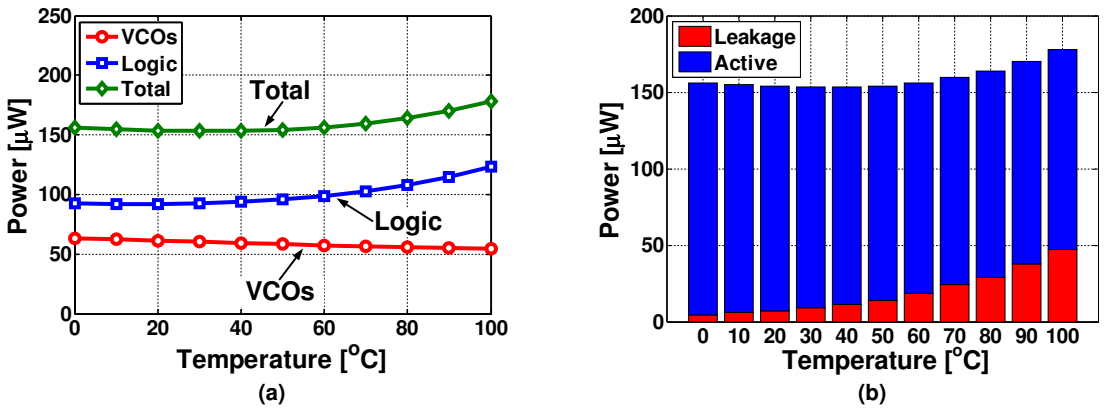


Figure 6.18: (a) Measured power break down versus temperature. (b) Measured power components versus temperature.

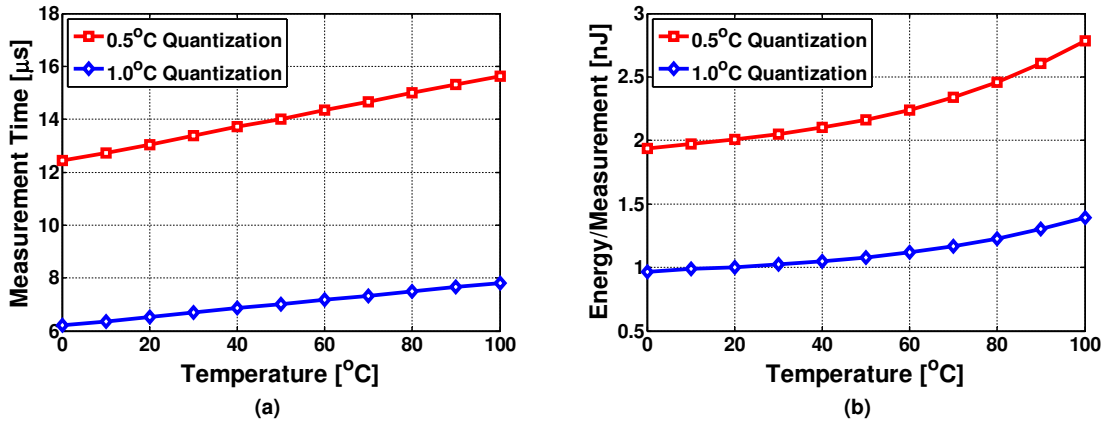


Figure 6.19: (a) Measurement time versus temperature for two different quantization error settings. (b) Energy/measurement versus temperature for two different quantization error settings.

the plot is shown in Fig. 6.18(b). At high temperatures, VCO frequency reduces, which reduces the active power. However, leakage in logic and VCO increase at high temperature and as a result total power consumption of the sensor increases.

Measurement time, also known as conversion time of the proposed sensor, is measured across temperature for two quantization error settings, and the results are shown in Fig. 6.19(a). The amount of quantization error can be altered by changing the threshold count (Φ_{TH}). At 20°C, the sensor takes approximately 6.5μs and 13μs to complete the measurement for a quantization error of 1°C and 0.5°C, respectively. Energy-per-measurement versus temperature for two quantization error settings is shown in Fig. 6.19(b). At 20°C, the sensor takes

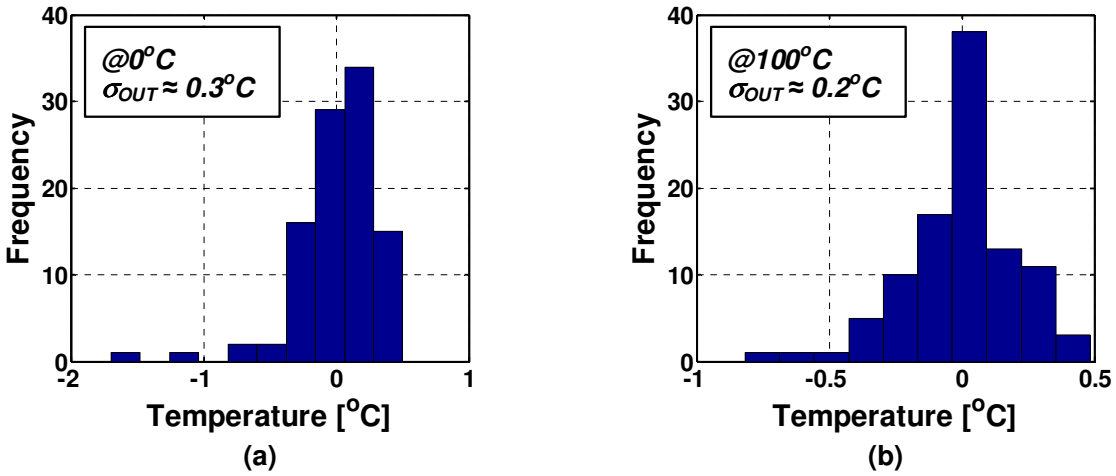


Figure 6.20: (a) Measured histogram of 100 sensor readings at 0°C. (b) Measured histogram of 100 sensor readings at 100°C.

approximately 1pJ and 2pJ to complete the measurement for a quantization error of 1°C and 0.5°C, respectively.

A lower bound on the measured sensor resolution is obtained by measuring the spread of sensor error at 0°C and 100°C, as shown in Fig. 6.20(a) and Fig. 6.20(b), respectively. At 0°C and 100°C the standard deviation of the measurement is 0.3°C and 0.2°C, respectively. The spread in the measured error is due to phase noise of VCOs and temperature fluctuations inside the chamber. Based on the phase noise simulation and calculations in Section 6.4, we think that the minimum achievable resolution is primarily limited by the thermal stability of the temperature chamber.

Table 6.1 compares the proposed sensor with the state-of-the-art temperature sensors. A graphical comparison of the proposed sensor with all previously published temperature sensors is shown in Fig. 6.21 [76]. The proposed sensor does not use any external clock reference or voltage regulators. It is designed with digital logic gates, and it achieves a competitive supply sensitivity of 0.034°C/mV and a resolution FoM of 0.3(nJ/conv)res^2, within a compact area of 0.004mm^2.

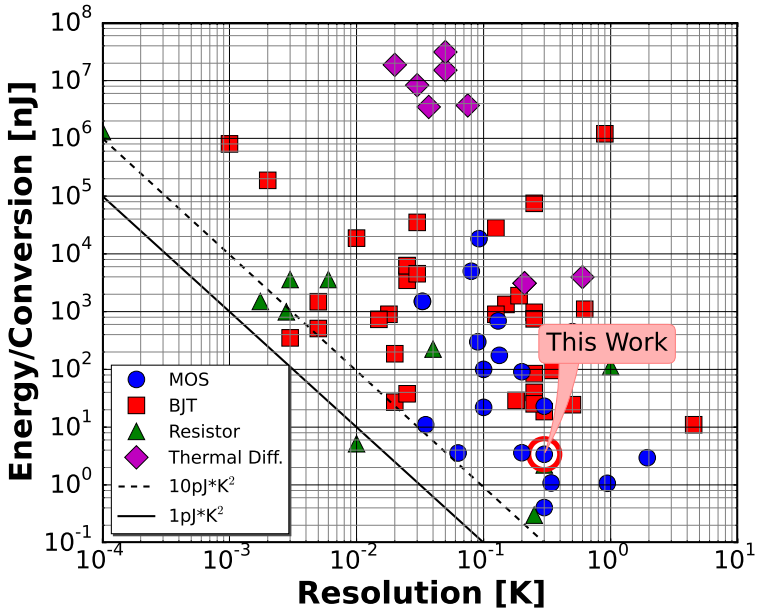


Figure 6.21: Graphical comparison of the proposed sensor in the energy-per-measurement versus resolution plot [76].

6.6 Conclusion

A self-referenced temperature sensor designed with logic gates was presented. The sensor works on the principle of converting temperature to frequency information to digital bits. A novel temperature measurement technique by creating threshold voltage difference between the transistors used in oscillators was proposed. Reverse short channel effect of planar transistors was leveraged to create threshold voltage difference. Supply sensitivity of the sensor is reduced by employing junction capacitance. Therefore, the overhead of voltage regulators and an external ideal reference frequency were avoided. The effect of phase noise on achievable sensor resolution was evaluated. The prototype temperature sensor was fabricated in 65nm CMOS technology and occupies an active die area of 0.004mm^2. It achieves a supply sensitivity of 0.034°C/mV, a resolution FoM of 0.3(nJ/conv)res^2, and its peak-to-peak non-linearity with and without polynomial correction is ±0.9°C and ±2.3°C, respectively, with two-point calibration over a temperature range from 0°C to 100°C.

Table 6.1: Performance Comparison of the Proposed Temperature Sensor with State-of-the-Art Designs

	This Work	[68]	[61]	[69]	[77]	[56]
Technology	**65nm**	180nm	160nm	65nm	65nm	14nm
Type	**MOSFET**	MOSFET	DTMOST	MOSFET	MOSFET	BJT
Area [mm²]	**0.004mm²**	0.09mm²	0.085mm²	0.008mm²	0.0012mm²	0.0087mm²
Supply[V]	**0.85-1.05**	1.2	0.85-1.2	1	1.1	1.35
Ext. Clk. Ref.	**NO**	NO	NO	NO	YES	NO
Supply Regulator	**NO**	NO	NO	YES	NO	YES*
Temp. Range[°C]	**0-100°C**	0-100°C	-40-125°C	0-110°C	40-100°C	0-100°C
Resolution[°C]	**0.3°C**	0.3°C	0.063°C	0.18°C	1°C	0.5°C
Measurement Time[s]	**22μs (0.3°C Qt.)** / **6.5μs (1°C Qt.)**	30ms	6ms	2.1μs	1ms	20μs
Calibration or Trim	**2-point**	2-point	1-point	1-point	N/A	2-point
Inaccuracy[°C] (w/ and w/o corr.)	**±0.9°C (w/)** / **±2.3°C (w/o)**	+1.5°C/-1.4°C	+0.4°C/-0.4°C	±1.5°C	3.1°C	3.3°C
Power	**154μW@1V**	71nW	600nW	500μW	N/A	1.1112mW
Energy/Meas.[nJ]	**3.4nJ (0.3°C Qt.)** / **1nJ (1°C Qt.)**	2.2nJ	3.6nJ	1.1nJ	N/A	22.8
FoM [nJK²]	**0.3**	0.198	0.0141	0.97	N/A	5.7
Supply Sens.[°C/mV]	**0.034°C/mV**	0.014°C/mV	0.00045°C/mV	(regulated)	0.018°C/mV	N/A

* Linear voltage regulator used for sigma delta ADC

CHAPTER 7

CONCLUSION

The universal growth of smartphones, social networking, and streaming sites have propelled the demand for high serial link bandwidths. The problem lies in the fact that energy involved in moving data on/off-chip through serial links is not scaling fast enough to meet the application demands. As a result, the available serial link bandwidth is getting limited by the battery life and thermal constraints of the package.

In the case of servers, serial links are utilized only 15% of the time, and a majority of the time they are idle and continue to consume peak power in order to maintain synchronization. Rapid-on/off transceiver, transmitter, and clock multiplier architectures, which were developed during the course of this dissertation, demonstrate that non-traditional architectural techniques, coupled with innovative algorithms, have the ability to minimize idle power. As a proof of this concept, design details and measurement results of a 7Gb/s embedded clock rapid-on/off transceiver and a 5Gb/s rapid-on/off transmitter were presented. Temperature sensor architecture, which is used to make PLL temperature insensitive during off periods has also been presented. We hope that serial link architectures, building blocks and algorithms presented in this dissertation would provide the system architect with necessary tools and information to make a power-scalable and energy-proportional communication system.

APPENDIX A

LIST OF SERIAL LINK PAPERS SURVEYED

Table A.1: Details of Surveyed Off-Chip Serial Links

Ref.	Year	Conf.	Node[nm]	Loss[dB]	Speed[Gb/s]	Pwr.[mW]	E/Bit[pJ]
[78]	2015	CICC	40	-	4	5.4	1.35
[79]	2015	CICC	40	-	10	41.6	4.16
[80]	2015	CICC	32	10	16	30.4	1.9
[81]	2015	CICC	65	15	40	190	4.75
[82]	2015	VLSI	22	12	8	6.32	0.79
[83]	2015	VLSI	28	35	13	49	3.8
[84]	2015	VLSI	22	-	5	10	2
[85]	2015	VLSI	65	12	14	39.2	2.8
[86]	2015	VLSI	40	-	25	98	3.92
[87]	2015	VLSI	40	-	9	9	1
[88]	2015	VLSI	40	-	56	670	11.96
[88]	2015	VLSI	40	-	56	710	12.6
[89]	2015	ISSCC	65	-	6	3.48	0.58
[90]	2015	ISSCC	65	-	10	49	4.9
[91]	2015	ISSCC	65	-	7	63.7	9.1
[92]	2015	ISSCC	20	10.4	32.75	785	23.96
[93]	2015	ISSCC	28	40	28	702.8	25.1
[94]	2015	ISSCC	28	40	28	295	10.53
[95]	2014	VLSI	28	20	40	927	23.17
[96]	2014	VLSI	20	20	36	609.9	16.9

Continued on next page

Table A.1 cont.

Ref.	Year	Conf.	Node[nm]	Loss[dB]	Speed[Gb/s]	Pwr.[mW]	E/Bit[pJ]
[97]	2014	ISSCC	40	15	12	51.5	4.29
[98]	2014	ISSCC	22	26	32	205	6.4
[99]	2014	ISSCC	28	20	20	130	6.5
[100]	2014	ISSCC	40	20	28	780	27.85
[101]	2014	ISSCC	28	34	28	560	20
[102]	2013	VLSI	28	21	11.4	32.2	2.82
[103]	2013	ISSCC	40	20.4	44.6	1920	43.04
[104]	2013	ISSCC	32	18	16	41.28	2.58
[105]	2013	ISSCC	28	-	6.4	58.24	9.1
[106]	2012	VLSI	28	33	12.5	335	26.8
[107]	2012	ISSCC	32	29	28	393	14.03
[108]	2012	ISSCC	90	-	8	257	32.12
[109]	2012	CICC	65	-	11.5	141	12.26
[110]	2012	CICC	28	31	13.1	282	21.5
[111]	2012	CICC	90	18.2	4	50	12.5
[112]	2011	VLSI	40	-	5.6	13.4	2.4
[113]	2011	VLSI	45	16.3	9	54.9	6.1
[114]	2011	ISSCC	65	-	8.4	21	2.5
[115]	2011	ISSCC	65	18	40	457	11.4
[116]	2011	ISSCC	90	34.9	12.5	348	27.84
[117]	2011	ISSCC	90	-	4	7.2	1.8
[118]	2011	ISSCC	65	-	11.3	214	18.9
[119]	2011	ISSCC	40	22	8	73	9.125
[120]	2011	ISSCC	130	-	4.8	68.35	14.24
[121]	2011	ISSCC	40	-	3.125	19	6.08
[122]	2011	ISSCC	45	32	16	385	24.06

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Table A.1 cont.

Ref.	Year	Conf.	Node[nm]	Loss[dB]	Speed[Gb/s]	Pwr.[mW]	E/Bit[pJ]
[123]	2011	ASSCC	32	-	8	94.4	11.8
[124]	2010	VLSI	40	-	7	27.58	3.94
[125]	2010	ISSCC	45	-	10	38	3.8
[126]	2010	ISSCC	65	12	12.5	12.3	0.98
[127]	2010	ISSCC	40	-	5.184	32.2	6.2
[128]	2010	ISSCC	40	8	10	14	1.4
[129]	2010	ISSCC	32	25	11.8	78	6.6
[130]	2010	ISSCC	65	15	5	280	56
[131]	2010	CICC	40	-	8	223.25	27.9
[132]	2010	CICC	90	5	16	384	24
[133]	2009	VLSI	65	21.2	20	87	4.35
[134]	2009	VLSI	32	10	12	37.8	3.15
[135]	2009	VLSI	60	-	1.6	17.58	10.9
[136]	2009	VLSI	40	10	4.3	14.19	3.3
[137]	2009	ISSCC	65	19	8.9	17	1.9
[138]	2009	ISSCC	90	35.8	10.3125	260	25.2
[139]	2009	ISSCC	65	-	40	5600	140
[140]	2009	ISSCC	65	26	10	1200	120
[141]	2009	CICC	90	10	11.4	307.8	27
[142]	2009	ASSCC	40	-	5	125	25
[143]	2009	ASSCC	65	-	3	91	30.3
[144]	2008	VLSI	90	-	8	160	20
[145]	2008	VLSI	130	-	39.5	3600	91.13
[146]	2008	ISSCC	90	36.8	8	232	29
[147]	2008	ISSCC	90	-	20	195	9.75
[148]	2008	ISSCC	130	-	10	10500	1050
[149]	2008	CICC	180	-	5	102	20.4

Continued on next page

Table A.1 cont.

Ref.	Year	Conf.	Node[nm]	Loss[dB]	Speed[Gb/s]	Pwr.[mW]	E/Bit[pJ]
[150]	2008	ASSCC	90	-	6.25	230	36.8
[151]	2008	ASSCC	180	-	3.2	225	70.3
[152]	2008	ASSCC	180	-	8	920.52	115.06
[153]	2007	VLSI	65	-	15	75	5
[154]	2007	ISSCC	90	-	10	250	25
[155]	2007	ISSCC	90	15	6.25	14	2.24
[156]	2007	ASSCC	90	-	10	980	98
[157]	2007	ASSCC	80	20	5	116.5	23.3
[158]	2006	VLSI	180	-	4.2	71.82	17.1
[159]	2006	VLSI	90	9.4	9.6	169.7	17.6
[160]	2006	ISSCC	90	24	10	300	30
[161]	2006	ISSCC	130	22	6	386	64.3
[162]	2006	ISSCC	130	-	12.5	3800	304
[163]	2006	ISSCC	90	-	9.6	100	10.41
[164]	2006	ISSCC	90	16	20	237	11.85
[165]	2006	ISSCC	130	-	11.1	793	71.4
[166]	2006	ISSCC	90	15	20	318	15.9
[167]	2006	ISSCC	110	5	20	263	13.15
[168]	2006	CICC	90	-	3.125	48.7	15.58
[169]	2006	ESSCIRC	80	-	6	25.2	4.2
[170]	2006	ESSCIRC	130	-	2	250	125
[171]	2005	VLSI	130	-	3.125	49	15.68
[172]	2005	ISSCC	130	9.9	5.15	2100	407.76
[173]	2005	ISSCC	130	-	6.25	150	24
[174]	2005	ISSCC	90	-	12	230	19.16
[175]	2005	ISSCC	250	-	3	152.25	50.75
[176]	2005	ISSCC	130	32	6.25	290	46.4

Continued on next page

Table A.1 cont.

Ref.	Year	Conf.	Node[nm]	Loss[dB]	Speed[Gb/s]	Pwr.[mW]	E/Bit[pJ]
[177]	2005	CICC	90	10	2.5	23	9.2
[178]	2005	ASSCC	130	-	2.5	70	28
[179]	2004	VLSI	110	-	6.4	247.5	38.6
[180]	2004	VLSI	90	-	3.125	73	23.36
[181]	2004	VLSI	110	30	3.125	250	80
[182]	2004	ISSCC	130	-	22.5	898	39.91
[183]	2004	ISSCC	130	-	22.8	800	35.08
[184]	2004	ISSCC	130	-	10.7	980	91.58
[185]	2004	ISSCC	180	-	3.125	180	57.6
[186]	2004	ISSCC	130	-	8	280	35
[187]	2004	CICC	150	-	3.125	65	20.8
[188]	2004	ESSCIRC	130	-	3.125	140	44.8
[189]	2003	VLSI	130	-	8	150	18.75
[190]	2003	VLSI	180	-	3.6	27	7.5
[191]	2003	ISSCC	110	-	10	415	41.5
[192]	2003	ISSCC	180	-	10	540	54
[193]	2003	ISSCC	180	-	8	120	15
[194]	2003	ISSCC	180	-	2.7	74	27.4
[195]	2003	ISSCC	130	-	3.125	160	51.2
[196]	2003	ISSCC	130	-	10.88	1000	91.91
[197]	2003	ESSCIRC	130	-	22.5	1500	66.66
[198]	2002	VLSI	130	9	5	300	60
[199]	2002	VLSI	130	-	4	128	32
[200]	2002	CICC	180	-	22.5	2900	128.88
[201]	2002	ISSCC	180	-	3.125	85	27.2
[202]	2002	ISSCC	130	-	5	378	75.6
[203]	2001	ISSCC	130	-	2	157.5	78.75

Continued on next page

Table A.1 cont.

Ref.	Year	Conf.	Node[nm]	Loss[dB]	Speed[Gb/s]	Pwr.[mW]	E/Bit[pJ]
[204]	2001	ISSCC	180	-	2.66	500	187.54
[205]	2001	ISSCC	250	-	2.5	269	107.6

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