UNDERSTANDING, MODELING, AND MITIGATING SYSTEM-LEVEL ESD IN INTEGRATED CIRCUITS

BY

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DISSERTATION

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Abstract

This dissertation describes several studies regarding the effects of system-level electrostatic discharge (ESD) and how to model and mitigate them. The topics in this dissertation fall into two broad categories: modeling pieces of a system-level ESD test setup and phenomenological studies.

Simulation is an important tool for achieving quality designs quickly. However, modeling methodologies for system-level ESD are not yet mature. This dissertation aims to improve (i) simulation models of ESD protection elements, (ii) simulation models of ESD guns, and (iii) analytic models of rail-clamp circuits used for power-on ESD protection. Simulation models for two common ESD protection elements, diodes and silicon controlled rectifiers (SCR) are presented and evaluated, specifically with regard to the origins of poor voltage clamping. These models can be used for ESD network design and simulation; their applicability is not limited only to system-level ESD. Next, a circuit simulation model for an ESD gun (used to produce system-level ESD stresses) is presented. This model can be used for trouble-shooting and design. Lastly, an analytic model of rail-clamp circuits during system-level ESD is presented. These circuits can produce unstable oscillations or ringing on the supply; such problems must be eliminated during design. Analytic models help the designer understand how circuit parameters will impact the circuit's performance.

System-level ESD is a relatively new requirement being imposed on IC manufacturers; as such, current understanding of how system-level ESD affects ICs is not yet mature. This dissertation includes two studies that expand upon this knowledge. The first demonstrates that ground bounce due system-level ESD stress can lead to severe problems, including latch-up and power integrity problems. The second reports observations regarding input noise signals at an IC pin during system-level ESD stress.

Lastly, this dissertation discusses experimental design of a test chip that will be manufactured shortly after this dissertation is completed. These experiments focus on observing and suppressing various errors that can occur during system-level ESD, arising from both noise at the inputs and power fluctuations. Additionally, this test chip includes standalone test structures that are used to reproduce power supply problems predicted in other sections of this dissertation.

Acknowledgments

I would like to that my advisor, Professor Elyse Rosenbaum for helping me improve as a scientist and communicator.

I would like to thank several current and former students in my research group for their teaching, helpful discussion, and advice that helped me to prepare this dissertation. Nathan Jack, Kuo-Hsuan Meng, Vrashank Shukla, Nick Thomson, Min-Sun Keel, Yang Xiu, Zaichen Chen, and Collin Reiman, thank you for your help.

I would like to thank my friends and family for all their support.

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Chapter 1 – Introduction

1.1 – Motivation

Electrostatic discharge (ESD) is a very common physical phenomenon that can disrupt electronic systems. Prior to an ESD event, a static charge is stored on some insulated object which can elevate its potential to several kilovolts; if the insulated object is subsequently grounded, the accumulated charge will rapidly discharge (which is the ESD event, itself). ESD events typically last between 1 ns and 1 μs and have a peak current on the order of several amperes; however particularly severe ESD events may approach tens of amperes. Because ESD events involve large, rapidly varying voltages and currents, they can cause a considerable amount of electromagnetic noise.

Some examples of electronic systems that could be disturbed by ESD include cell phones, laptops, electronics in automobiles, and electronics used in industrial control. Such systems usually consist of several integrated circuit (IC) components connected together on one or more printed circuit boards (PCBs) that are housed in an insulating or conductive enclosure. Some systems may also include antennas, cables, and electronic sub-assemblies (such as a display). ESD poses several main threats to electronic systems. First, the large currents and voltages associated with ESD can directly damage sensitive electronic components. Second, the large injected current can cause latchup. Third, the large current and voltage derivatives can induce large noise signals virtually anywhere within the system, which can cause individual components to malfunction. Lastly, the ESD current may disrupt the power supply integrity of an IC (ESD current injected at any IC pin is usually shunted to a power rail).

System manufacturers are often required to comply with at least one of several standards in order to sell their product. The most common standard for immunity to ESD based disruption

is IEC 61000-4-2 [1], which governs consumer electronics. Compliance to IEC 61000-4-2 is required to obtain the “CE” sticker that is seen on many electronic products. A similar standard, ISO 10605 [2] governs electronics used in automobiles.

In the past several years, system manufacturers have increasingly pushed IC manufacturers to produce designs that more easily help them meet the system level ESD specifications without the addition of external components, such as transient voltage suppressor diodes. ICs usually include some ESD protection, though it is not designed to handle the larger system-level ESD current stresses. Furthermore, some ESD protection elements (primarily the protection between supply rails) are designed to remain off when the chip is powered on; these designs must be altered to operate with the chip powered without disrupting normal operation. Even if the on-chip ESD protection devices are appropriately designed, the large ESD currents can introduce several problems, such as substrate current injection leading to external latchup [3], [4] and circuit node disruption [5], high amplitude coupled noise [6], and ground bounce due to package inductance and package/chip resistances. Understanding and mitigating these problems are an active area of research.

One of the issues complicating research in system-level ESD is measurement methodology. Some systems are intended to be used without connections to earth ground, such as a cell phone. Thus, when these devices are tested for system-level ESD resilience, they are also floating. Because most instruments, such as oscilloscopes, introduce a connection to earth ground, they cannot be used without strongly influencing the test. Thus, in studying system-level ESD, the most reliable investigative tools will be in-situ monitoring solutions and simulation. Both of these methods will be discussed in this dissertation.

1.2 – Overview

This dissertation focuses on addressing many current topics in system-level ESD. Chapter 2 presents the experimental setups used in this dissertation, including pulsed I-V measurement methods, system-level ESD testing, and test chips/boards used for studies later in this dissertation. The clamping performance of ESD protection devices may impact the resilience of a chip to system-level ESD stress. Chapter 3 demonstrates key factors that influence the clamping performance of silicon controlled rectifiers (SCRs) which are commonly used ESD protection devices. Chapter 4 introduces a circuit simulation model for the ESD guns that are used to perform system-level ESD testing. The model presented here is designed so that it can be used to simulate both IEC 61000-4-2 and ISO 10605 waveforms. Chapter 5 presents an analysis of MOSFET ESD clamps used between supply rails in many ICs. This chapter focuses on design tradeoffs for these circuits, especially regarding stability. Appropriate design is important because the transient response of the protection circuit will appear directly on the supply. Chapter 6 demonstrates how system-level ESD can result in severe ground bounce in ICs, leading to power integrity problems. Chapter 7 presents experimental results about coupled noise during system-level ESD testing using on-chip noise monitors. Chapter 8 presents a variety of experiments designed to expand upon the studies in Chapter 5, Chapter 6, and Chapter 7. Chapter 9 concludes this dissertation and suggests future work.

Chapter 2 – Measurement Techniques and First Test Vehicles

2.1 – Overview

This chapter documents the various experimental setups used in this dissertation. First, the pulsed I-V measurement methods for standalone test structures are described briefly, then methods of applying similar techniques to assembled chips mounted on a PCB are discussed. Second, various aspects IEC 61000-4-2 testing are discussed, including measurement considerations and a high-level description of the failures observed during the test. Lastly, this chapter describes the various test vehicles used in this dissertation, include a test chip and the test board that houses the test chip.

2.2 – Pulsed I-V Measurement Methodology

During ESD stress, devices on integrated circuits are briefly exposed to currents and voltages that would destroy them if they were applied for a longer duration. Thus, performing typical I-V characterization (e.g. a slow voltage or current sweep) over the operating range would destroy the device and not give a reliable I-V measurement. This problem is solved by using a pulsed I-V technique. A pulse is applied to the device under test (DUT), and its current and voltage are measured during each pulse. The voltage and current measurements during a pulse provide one data point in the I-V curve, so many pulses are used to construct the I-V curve. Often, low current I-V measurements can be performed between each pulse; a significant change in the I-V curve would indicate a failed device. In general, the failure behavior of a device is highly dependent on the duration of the applied pulse [7], so pulsed I-V characterization may use many different pulse widths.

One specific implementation of pulsed I-V measurements is transmission line pulsing (TLP) [8]. A simplified schematic of a TLP tester is shown in Figure 2.1. An actual TLP tester

may include other components, such as rise time filters, attenuators, and relays to connect the load to e.g. an instrument for performing DC measurements. Typical transient voltage and current waveforms are shown in Figure 2.2; to produce a point on the I-V curve, the voltage and current are averaged over a time window near the end of the pulse, e.g. 70 ns to 90 ns for a 100 ns pulse. One limitation of TLP is demonstrated in Figure 2.3. In general, the current probe (and possibly the voltage probe) cannot be placed directly at the DUT, so the reflections caused by the DUT are clearly visible in the measured waveform. For longer pulse widths, such as 100 ns, this reflection does not present a problem; however, as the pulse width is reduced, the effect of the reflections will become more and more pronounced. At a sufficiently short pulse width, measurement accuracy will suffer.

Because TLP ceases to be reliable at very short pulse widths, another measurement technique called very fast TLP (VFTLP) was developed [9]. Both VFTLP and TLP can use the measurement apparatus shown in Figure 2.1 with very minor modifications, e.g. the voltage pickoff resistor might be replaced with a short to minimize system reflections. In VFTLP, the cable between the current probe and the DUT is made sufficiently long so that the incident and reflected pulses do not overlap. A typical measured VFTLP current waveform is shown in Figure 2.4. To calculate the steady-state current, the incident and reflected pulses are aligned in time and added together. Conceptually, both the voltage and current and can be calculated from the incident and reflected pulses (which may be measured either as a voltage or current); however, this is seldom done in practice. The voltage is measured directly at the DUT to provide a more reliable transient measurement. Getting accurate transient voltage measurements is non-trivial and will be discussed shortly. VFTLP relies on the incident and reflected pulses being clear and

distinct; the entire measurement system must be reflection free (constant characteristic impedance) except for the DUT.

In order to get accurate voltage transient waveforms, some post-processing of the measured waveform may be required. Two types of voltage probes are commonly used for TLP testing: 50 Ω RF probes with very high bandwidth (40 GHz) and high impedance RF probes with moderate bandwidth (~3 GHz). The former are desirable because of their frequency response. The latter are desirable because (i) less current flows through the probe's contact resistance, which leads to smaller measurement error, and (ii) they do not add a load low impedance load in parallel with the DUT, which allows for higher source impedance. High source impedance is desirable because it allows for more complete characterization of devices that show negative differential resistance (e.g. SCR, bipolar transistors with high levels of impact ionization). To get accurate transient measurements with a high impedance probe, the measured waveform must be passed through a software filter that negates the high-pass filtering effect of the probe, as shown in Figure 2.5. The high-impedance RF probes have a high-pass transfer function due to their equivalent circuit, shown in Figure 2.6. Peak voltage determination requires some additional post-processing of the voltage transients. The peak occurs for a very brief time, and the two samples surrounding the peak may not be close to its actual value; this can manifest as a significant amount of measurement noise. A better estimate of the true peak voltage can be obtained using sinc interpolation to up-sample the measured transient. The effects of applying a corrective filter and sinc interpolation are demonstrated in Figure 2.7.

Both TLP and VFTLP are staple techniques for characterizing ESD devices and are primarily used on standalone test structures which allow voltage probes to be placed directly at the DUT. However, for system-level ESD, it is highly desirable to characterize the I-V and

failure characteristics of an IO on a chip in a fully assembled circuit board. Performing such a measurement introduces additional complications. In general, the connector and signal lines between the connector and IO will not form a matched transmission line or be electrically small; the possibility of additional reflections prevents VFTLP from being a reliable measurement method for shorter pulses. Figure 2.8(a) shows this problem; the TLP pulses applied to the test board do not have an appreciable flat portion until about 10 ns into the pulse, which makes pulses less than 10 ns impossible to use. As will be demonstrated in Section 2.3, some features of the waveforms used for system-level ESD testing have durations below 10 ns. The I-V curve show in Figure 2.8(b) demonstrates another problem with using TLP on a board. Significant voltage drops occur on the board, package and chip; it is non-trivial to separate each voltage drop and produce a meaningful I-V curve.

2.3 – Discussion on IEC 61000-4-2 Testing

A sample test setup for IEC 61000-4-2 testing is shown and described in Figure 2.9. Nominally, the discharge from the ESD gun is caused by a 150 pF capacitor discharging through a 330 Ω resistor; however, the discharge current does not resemble a basic RC discharge; the discharge is fast enough so that the electromagnetics of the gun are important. The nominal waveform into a broadband "Pellegrini" 2 Ω calibration target is shown in Figure 2.10. This waveform is given by an analytic expression in the standard [1]. A current peak is produced in the first few nanoseconds as charge is coupled from the 150 pF capacitor to nearby metal. Though the standard provides a reference waveform, it only specifies certain features about the waveform when the gun zaps the Pellegrini target. It should have (a) 10%-90% rise time of 0.8 ns ±25%, (b) first peak current of 3.75 A ±15%, (c) current at 30 ns of 2 A ±30%, and (d) current

at 60 ns of 1 A ±15%. The current values listed above are at 1 kV precharge on the capacitor; they should scale linearly with the precharge voltage.

When interpreting test results, it is helpful to understand the spectral content of the IEC 61000-4-2 waveform. Measured waveforms of the discharge into the Pellegrini target are shown in Figure 2.11. The Pellegrini target has a voltage pickoff that can be directly connected to an oscilloscope. The current is also measured directly using a Tektronix CT-6 current probe. To obtain the spectrum, the measured voltage waveform is Fourier transformed; the results are shown in Figure 2.12. The spectrum has two main sections: the first peak which has energy from DC to 300 MHz, and the slower second peak, which has energy from DC to 50 MHz.

During system-level ESD testing, several failure mechanisms can occur. First, the energy provided by the ESD gun (or the voltages it induces) may be large enough to damage the IO circuits of an IC. This may include damaging the ESD protection circuits, the output drivers, and input gate oxide. This is termed a hard failure. Second, if large currents are injected into an IC, the ESD protection diodes may inject majority/minority carriers into the substrate; as these carriers are collected, they may cause latchup. Third, the large currents induced on the board in which the IC is housed may couple onto signal lines, thereby corrupting the input signals to an IC. This is called a soft failure. Depending on the typical use of the system, it may be floating or grounded during IEC 61000-4-2 testing. If the system is floating, in general, less energy can be transferred to it because the capacitive return to earth ground will block a large amount of current. However, the capacitive return to earth ground may not be high enough impedance to block the first peak; this peak has a large current derivative, which may cause soft errors through inductive coupling.

Most instruments, e.g. oscilloscopes, introduce a ground connection which makes obtaining reliable measurements of system-level ESD waveforms very difficult or impossible. This is especially true for floating systems, where no DC connection to earth ground exists without the instrumentation. However, even in grounded systems, the presence of an additional ground connections and wires may alter the inductance of the ground path or provide additional capacitive return paths. Because of these difficulties, a test chip has been designed with monitors that can store information about, for example, coupled noise that the chip experiences.

2.4 – Test Chip

A custom test chip was designed and fabricated in 130 nm CMOS for the investigation of failures due to system level ESD. Not all of the experiments will be presented in this dissertation, but all sections that connect to off-chip components will be described for completeness. Figure 2.13 shows the chip layout. The test chip has two main power domains. The core circuitry and the SSTL IO test circuits lie within the 1.5 V domain, V_{DD}. The 3.3 V supply, V_{DDIO}, provides power to all the CMOS IO circuits.

Schematics showing all of the devices that appear in the CMOS IO cells and supply cells are shown in Figure 2.14. The basic dual-diode protected IO cells are shown in Figure 2.14(a). Devices D_{Top} and D_{Bot} conduct most of the ESD current; they can survive 100 ns TLP currents of about 9 A. Resistors are added to reduce the ESD current going to the output driver, which is comprised of N_0 and P_0. Devices Q_0 and D_0 provide voltage clamping for the gate oxide of the input buffer. Q_0 is fabricated as an NMOS with a grounded gate; it operates as an NPN transistor that is activated by impact ionization at the base-collector junction. That is, it operates in snapback mode. For SCR protected IOs, D_{Top} is removed from the dual-diode protected IO, and a DTSCR (e.g. Figure 2.14(b)) is added in parallel with D_{Bot}. The SCR circuit on the test chip uses

a string of six diodes instead of three. The SCR circuit can survive a 100 ns TLP current of roughly 5 A. The schematic of supplies is shown in Figure 2.14(c). Each V_{DD} cell contains a 2 mm active clamp (M_1), and it corresponding diode. Each V_{DDIO} cell contains a 5.5 mm active clamp (M_0) and its corresponding diode. Each V_{SSIO} cell contains anti-parallel diodes to V_{SS}. The rail clamp trigger circuits are optimized for power-on ESD. The design for the V_{DDIO} trigger circuit is described in Chapter 5; the V_{DD} rail clamp is very similar in design. The V_{DDIO} bus was subjected to 100 ns power-on TLP (w.r.t. V_{SSIO}); leakage current measurements indicate that at least one of the several V_{DDIO} clamps distributed around the pad ring suffers hard failure when 18 A is injected onto the pad ring. In an analogous measurement, one of the several V_{DD} clamps fails when 8 A is injected between the V_{DD} and V_{SS} buses.

In Figure 2.13, the pad cells labeled IO1 through IO6 are CMOS IOs that connect to external pins which will undergo ESD zapping; the pads with dual-diode protection are labeled "DD" and the pads protected by SCRs are labeled "SCR" (see Figure 2.14). All six of these pad cells contain the bi-directional transceiver ("TRX"); however, by selective exclusion of key interconnects, IO3 and IO4 were configured as transmitters ("TX"), and IO5 and IO6 were configured as ESD-protected dummy cells. All of the functional IOs, e.g. mux addressing and strobe, use a DD-TRX architecture. The latch-up zap points use either DD or SCR ESD-protected dummy cells.

A variety of soft-failure monitoring circuits were placed on the chip. The first is a "glitch detector," included because coupled noise at an input pin can produce logic errors. The glitch detector circuit is shown in Figure 2.15. This circuit was placed inside the IO1 pad cell and will detect a logic level change at the IO1 pin due to ESD discharges elsewhere in the system. The glitch detector is active when the OE control signal is low. When the logic level at the input

changes, GD switches from low to high, maintaining this value until the latches are reset. The rightmost multiplexer allows the IO to output either GD or D_{OUT}. The leftmost multiplexer keeps the signal at the input of the glitch detector constant when OE is high (activating the output driver); without it, the signal output by the glitch detector would be fed back into the glitch detector. This could cause the output of the glitch detector to be erroneously interpreted as a glitch. For most test chip designs, this implementation would be unnecessarily complicated, because GD need not necessarily be read out from the same IO the glitch detector is connected to. However, this circuit was added to the test chip as it was nearing completion. Using this complicated implementation was preferred over a simpler design that would require modifying the chip's architecture. Specifically, the output multiplexer shown in Figure 2.13 already had each input bit assigned. Passing GD through the mux would require an additional address pin, which was not available. Experiments using this circuit are reported in Chapter 7.

A "latchup monitor circuit" was designed to detect a significantly elevated substrate potential, which is one of the significant root causes of latchup (LU). The LU monitor circuit is shown in Figure 2.16(a); node IN is connected to a substrate tap. If the local substrate potential reaches 0.5 V, indicating conditions are almost right for latchup, the LU monitor output changes. In the physical implementation, R1, R2, M1, M2, and M3 are placed in an isolated P-well near the victim circuits. This portion of the circuit cannot latch up because the only P-type silicon is the isolated P-well, which is tied to VSS. There are no PMOS devices, so there is no P-anode to form an SCR structure. M4 and M5 are placed far away from the victim circuits and are connected to a different supply than the victims. A separate supply is required because the victim circuits' supply voltage will be pulled down when they latch up, which could alter the behavior of the circuit. Figure 2.16(b) shows the circuit's voltage transfer characteristic, obtained from a

standalone test structure. As is, this circuit can only detect sustained latch-up because it does not have any elements with memory. However, the output could be stored on, e.g., an SR latch, which would allow it to be used to detect unsustained latchup and brief elevations in substrate potential.

The IO and core logic were laid out following best practices for latchup prevention, i.e. all MOS devices have a well-ties directly adjacent to them, and thus latchup was not expected to occur. The substrate resistivity for the process ranges from 1 Ω-cm to 2 Ω-cm. Therefore, the LU monitors were placed in a relatively small region of the chip that is run off a separate 1.5 V supply, V_{DDLU}. The circuits within the V_{DDLU} domain have sparser well ties, making latchup more likely. Specifically, the design kit provides a maximum spacing between each MOS device and the nearest well-tie that will allow the chip to pass JEDEC latch-up testing [10]. The maximum well-tie spacing increases with the distance between the MOS device and the nearest aggressor device (any device connected to an IO pad). Next to each IO pad adjacent to the V_{DDLU} domain, there is a sea-of-gates powered by V_{DDLU} that contains victim circuits at various distances from the aggressor devices. These victim circuits have the maximum allowable well-tie spacing and are connected to a LU monitor. The LU monitor output stage is located far from the LU monitor front-end and is powered by V_{DD}. The output of an on-chip LU monitor circuit gets connected to a chip output pin for read-out by means of the MUX. Unfortunately, no sustained latchup was observed in this test chip. Because the LU monitor is a static circuit, this meant that there are no experimental data to report regarding it. However, unsustained latchup is observed and reported in Chapter 6.

Two USB transmitters are included on-chip; each outputs a differential square-wave near the 480 Mbps operating speed of USB 2.0. Each USB transmitter is driven by an independent on-

chip ring oscillator. The output pins of USB transmitter #1 have dual-diode ESD protection, while the output pins of transmitter #2 have DTSCR protection. The experiments using these circuits are beyond the scope of this dissertation; they are presented in [6].

Fourteen of the pad cells contain bidirectional SSTL IO test circuits [11]. As indicated on the bottom-right side of Figure 2.13, the SSTL IOs lie in two groups, labeled bank A and bank B. Each side contains six working SSTL transceivers; additionally, two non-functional SSTL transceivers were included on bank B for a component-level ESD study. The operating state of the SSTL block is programmable, allowing for selection between TX and RX modes and for adjustment of the on-die termination resistance. The SSTL block is programmed by an on-chip shift register via a 3-wire interface (serial data, serial clock and latch enable). Though these IOs are for an unrelated project, they experience soft errors during system-level ESD testing as reported in [6].

Banks of logic gates are included on the test chip. They are labeled as "Dyn. Logic" and "Static Latches" in Figure 2.13. The stored data may be read-out before and after an ESD zap, in order to detect ESD-induced logic errors. The experiments using these circuits are beyond the scope of this dissertation; they are presented in [5], which demonstrates that the dynamic logic circuits can be disrupted by minority carrier currents in the substrate, and both sets of circuits can be disrupted by noise coupling to the pins used to clock in data.

2.5 – Test Board

The system-under-test is a four-layer FR4 circuit board, shown in Figure 2.17. The test system can be powered by a DC supply or by a battery pack (pictured). Four independent linear low-dropout (LDO) regulators supply each of the power domains: V_{DDIO} (3.3 V), V_{DD} (1.5 V), V_{DDLU} (1.5 V) and V_{DDLED} (3.3 V), the last of which provides power for the LEDs described

below. Adequate decoupling capacitance is included on each of the power nets, including large tantalum capacitors and smaller ceramic capacitors. SMD decoupling capacitors were placed near the chip, following best practices.

An on-board LED provides a visual readout of logic high signals from the multiplexer output and a second LED enables data readout from IO1, the glitch detector circuit's output.

Some of the chip IO pins are intended to undergo ESD zapping; test points are placed at the board-edge ends of traces that terminate at these pins. A zap is initiated by a contact discharge to a test point. Test points provide direct access to IO1-IO6 and to a bank of IO cells located near the V_{DDLU} domain (the latter are labeled as "Latch-up Monitor Aggressor Pins" in Figure 2.17). An additional test point is connected to a trace that is adjacent to the signal trace that goes to IO1. This neighbor line is referred to as the "aggressor line;" the aggressor line is terminated near the test chip by a short circuit to ground. Zaps are applied to the aggressor line in experiments that utilize the glitch detector inside IO1; in these experiments, IO1 is set to receive mode and its input is set to either logic low or logic high. The logic input for IO1 is supplied by an on-board buffer IC. IO1 can also be directly connected to a test-point on the board's edge. The desired input source for IO1 is selected by soldering a 0 Ω resistor to one of two pads on the board.

The control signal switches drive the multiplexer address pins and the on-chip control lines, and are used to input data to the latches and dynamic logic. Address and control pins are not intended to be zapped; robust signal filters are placed on board near these pins of the test chip to minimize ESD-induced disturbances.

A 0.1 Ω precision resistor is inserted in series with the V_{DD} on-board voltage regulator. A multimeter can be used to measure the voltage across this resistor. This allows the quiescent current draw (I_{DDQ}) to be measured before and after an ESD gun discharge.

A comparator circuit is placed at the output of the LDO which provides V_{DDIO}. It compares the voltage level of V_{DDIO} against a 3 V reference. The reference voltage is generated by sinking current from V_{DDLED} (3.3 V) through a Schottky diode. If the maximum current limit of the V_{DDIO} LDO is exceeded due to latchup, V_{DDIO} will decrease and the comparator will light an LED. Neither V_{DDIO} nor V_{DD} showed any signs of latchup during system-level ESD testing.

By design, V_{DDLU} was more likely to undergo latchup. Each of the LU monitor circuits had a logic-low output after system-level ESD zaps, suggesting that latchup did not occur. A more careful conclusion is that sustained latchup did not occur, since there is a few second delay between when the experimenter initiates an ESD gun discharge and when he reads out the LU monitors. The test board was designed to limit the current into V_{DDLU} to 1mA to prevent catastrophic damage to the IC. An unintended consequence was that insufficient current was sourced from the supply to maintain latchup. In Chapter 6, it is shown that latchup on V_{DDLU} can be triggered during system-level ESD testing.

2.6 – Figures

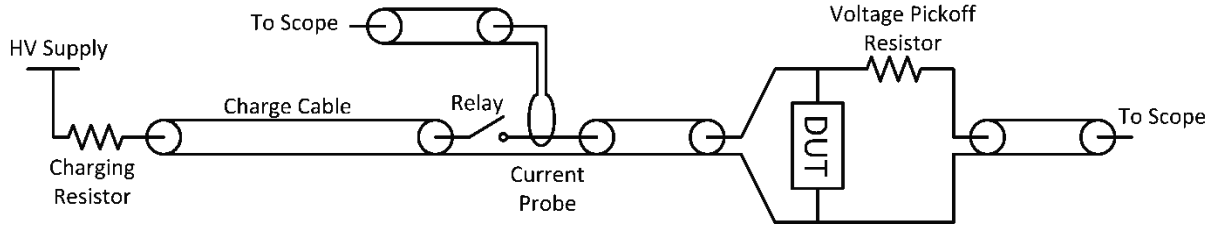


Figure 2.1: Simplified schematic of a TLP tester. The charging resistor will typically be 10 to 50 MΩ so that its current will not damage the DUT after a pulse. The voltage pickoff resistor is typically 1 to 5 kΩ to allow sufficient bandwidth for the pickoff while minimizing its effect on the measurement. For devices fabricated as standalone silicon test structures, the voltage pickoff can be placed directly at the DUT; however, this is not the case in general.

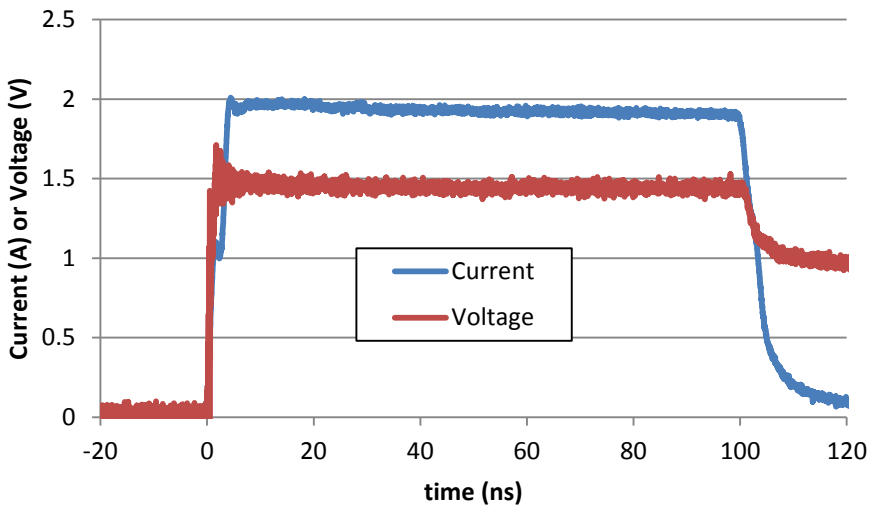


Figure 2.2: Typical measured voltage and current waveforms during TLP measurements.

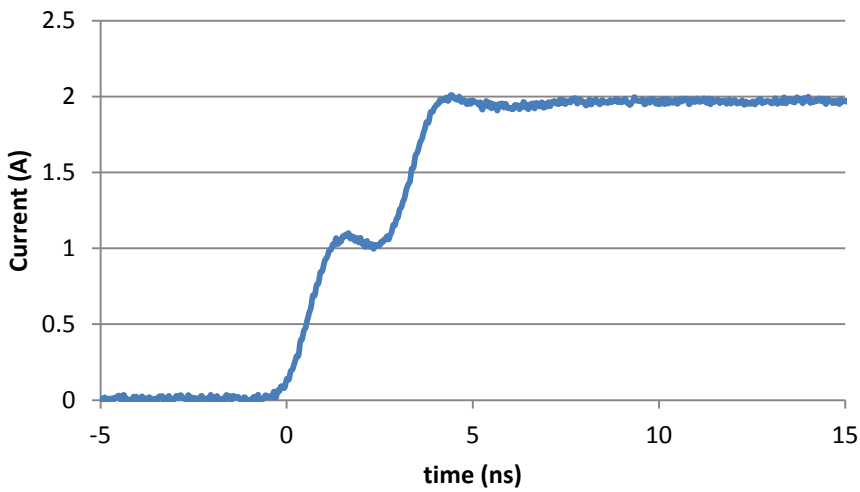


Figure 2.3: Zoomed-in view of current waveform plotted in Figure 2.2. The delay between the (overlapping) incident and reflected pulses of the DUT is clearly visible.

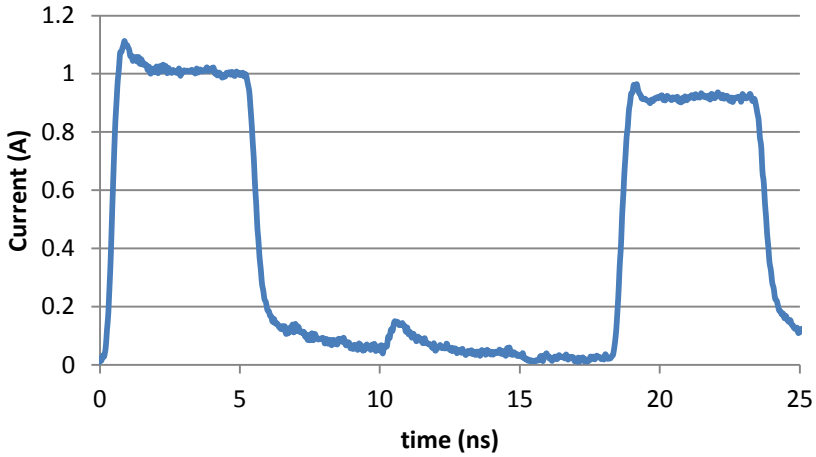


Figure 2.4: Typical VFTLP current waveforms. The incident and reflected pulses do not overlap.

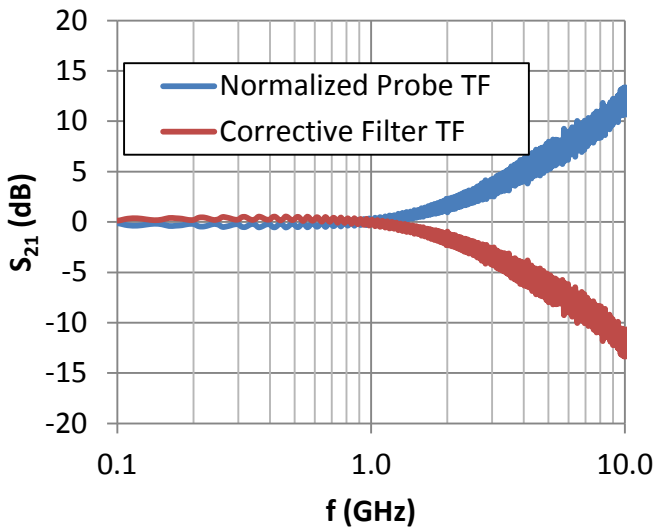


Figure 2.5: Transfer function of a typical high-impedance RF probe and corrective filter to undo the filtering from the probe. The high-pass characteristic of the probe arises due to the probe's equivalent circuit shown in Figure 2.6.

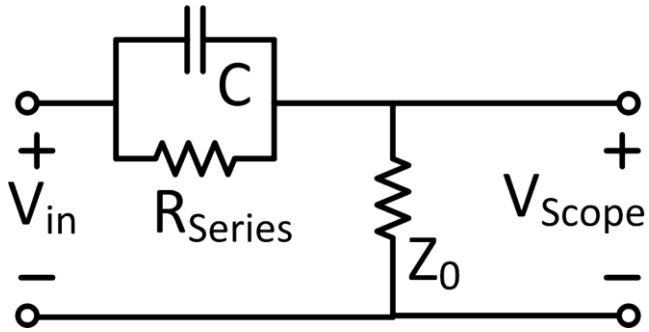


Figure 2.6: Equivalent circuit of high-impedance RF probes.

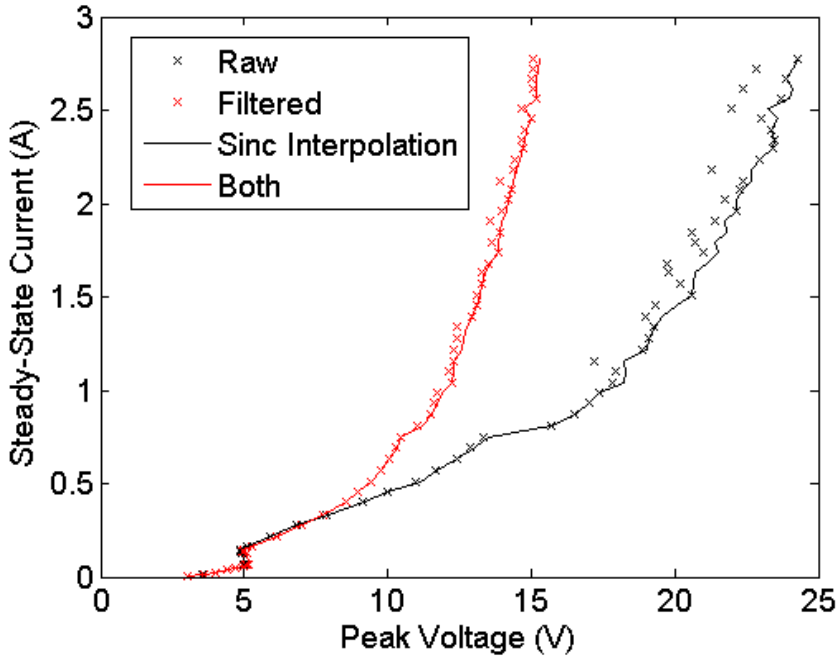
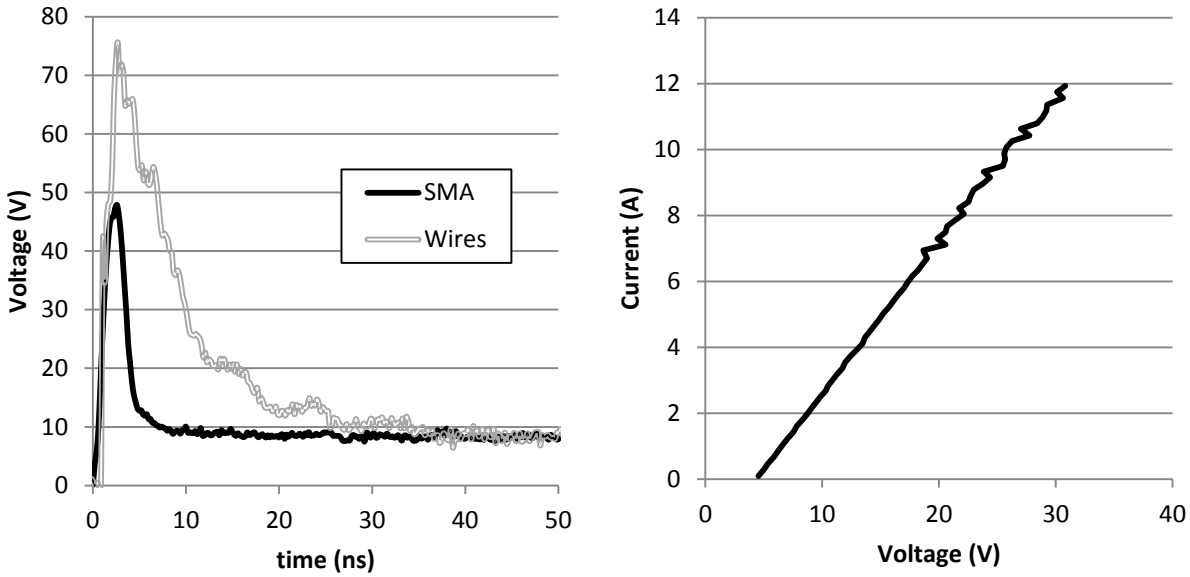


Figure 2.7: Peak voltage vs. steady-state current for a DTSCR in 130 nm CMOS during TLP with a 100 ps rise time and high-impedance RF probes. Without applying filtering, the (inaccurately) measured overshoot is extremely high. Applying a sinc interpolation filter significantly reduces noise in the measured overshoot. A discontinuity in overshoot is observed at ~0.8 A. This occurs due to a charge in attenuator settings in the TLP source.



(a) (b)

Figure 2.8: (a) TLP pulses (1.7A, 100 ns) applied to an IO through a test board. Connection to the board is made using either wire clips or an SMA connector. Voltage is measured through a pickoff tee between the TLP system and the board. (b) TLP I-V curve obtained using SMA connector. Measured TLP voltage drop is unusually high (30 V at failure) in comparison to measurements on standalone test structures of on-chip devices (10 V at failure), suggesting significant voltage drops on the board and package.

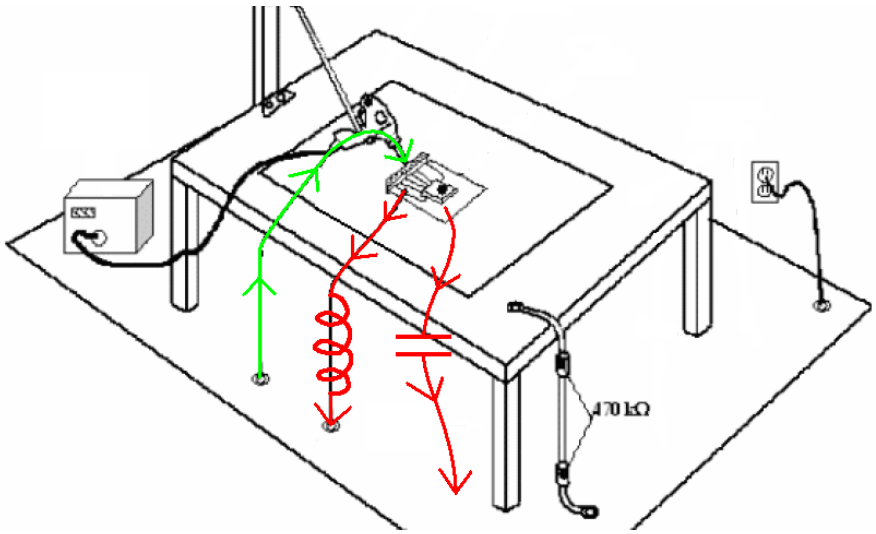


Figure 2.9: Typical IEC 61000-4-2 test setup, including large metal ground plane on floor and metal horizontal coupling plane on table. Capacitor in ESD gun is charged up through high valued resistor using the cable going to the source on the left. The ESD gun is grounded through the cable with arrows pointing to the ESD gun. During a test, the ESD gun is discharged into the system under test (SUT), which is typically an assembled electronic product. The current will return through any grounds connected to the DUT. If no ground is explicitly provided, the current will return through capacitive paths between the DUT and ground.

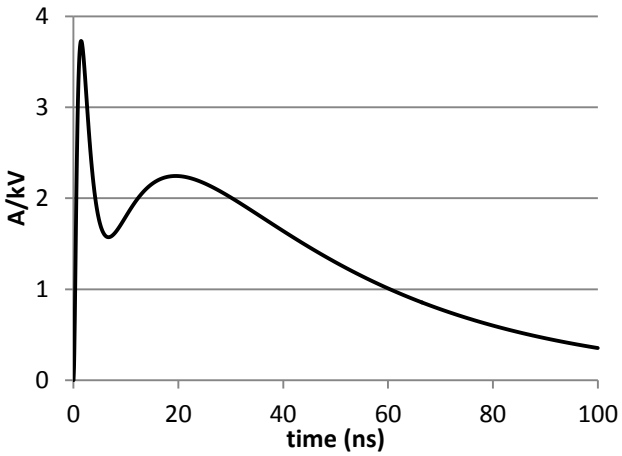


Figure 2.10: Nominal current waveform of IEC 61000-4-2 standard into a broadband 2 Ω load.

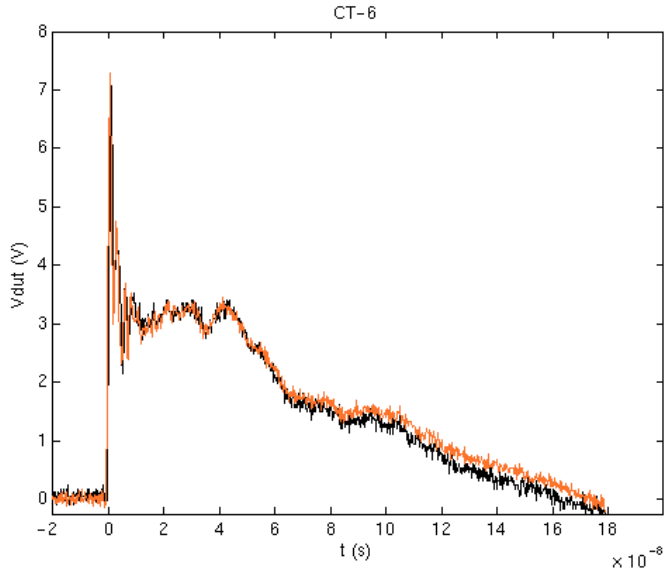


Figure 2.11: Measured IEC 61000-4-2 voltage waveform across 2 Ω load using an oscilloscope (orange) and a CT-6 current probe (black). Precharge voltage is 1 kV. Horizontal axis units are tens of nanoseconds.

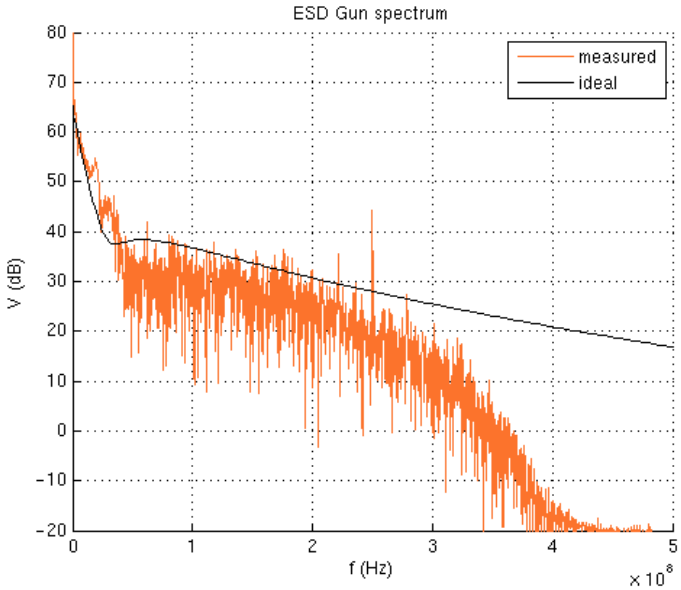


Figure 2.12: Spectrum of measured IEC 61000-4-2 waveform in Figure 2.11. The spectrum of the reference waveform shown in Figure 2.10 is plotted for comparison. Horizontal axis units are hundreds of megahertz.

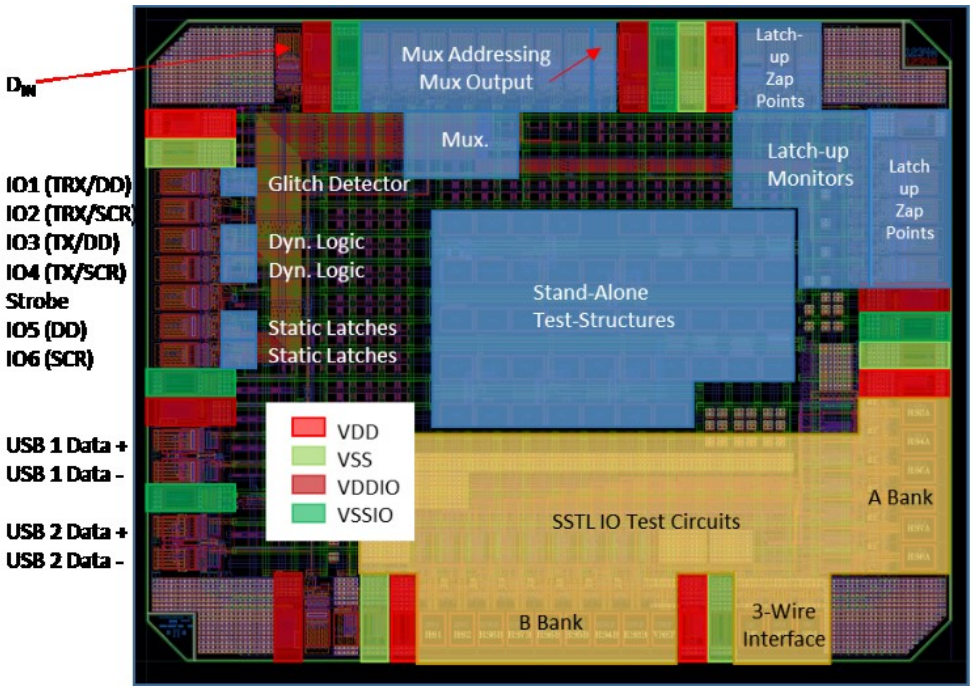


Figure 2.13: Chip layout view.

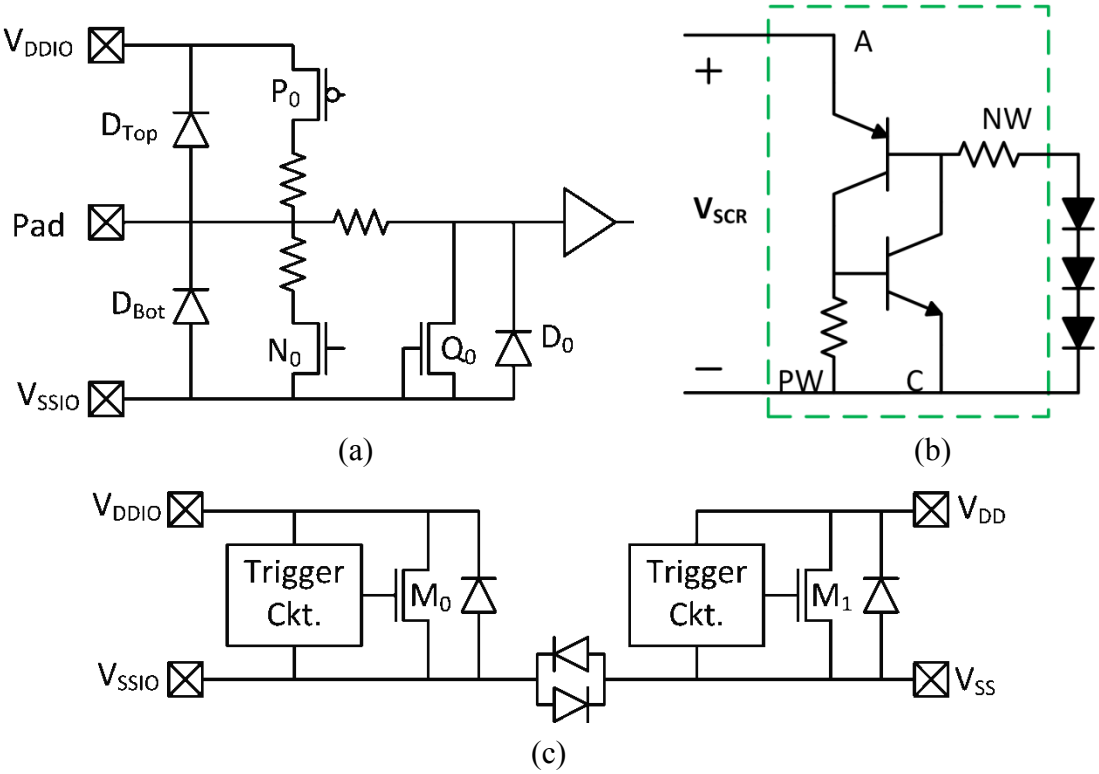


Figure 2.14: Schematics of devices present in the pad ring. (a) Basic bi-directional dual-diode protected IO. In SCR protected IOs, D_{Top} is removed and the circuit shown in (b) is connected between the pad and V_{SSIO}. The devices in supply cells are shown in (c).

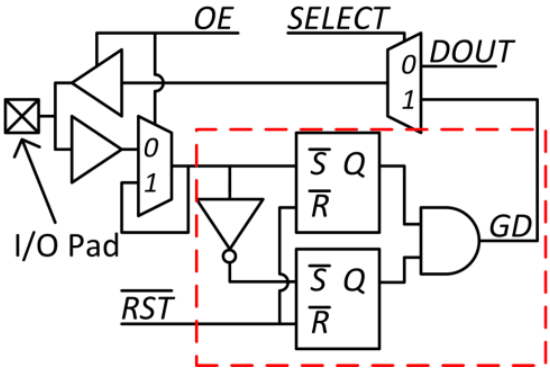
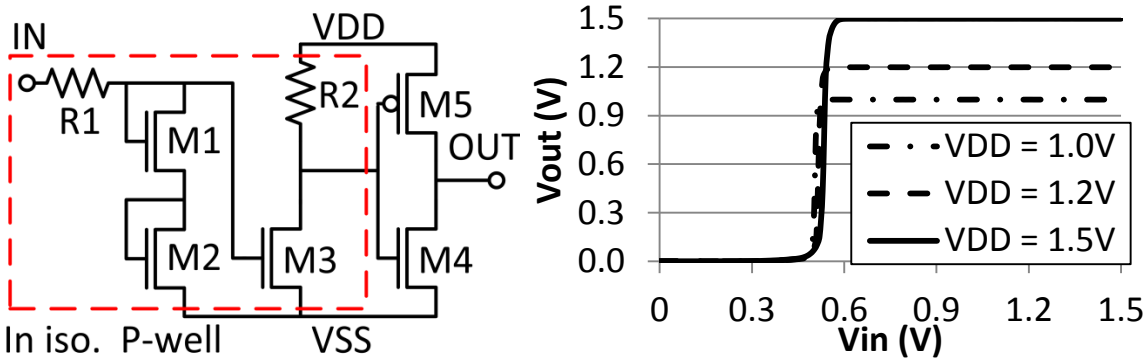


Figure 2.15: Glitch detector schematic.



(a) (b)

Figure 2.16: (a) Latchup monitor schematic. The input is connected to the substrate. Components R1, M1 and M2 provide 3.3 V tolerance for this circuit which uses 1.5 V transistors. An NMOS inverter is used inside the isolated P-well to prevent it from latching up. (b) Latchup monitor voltage transfer characteristics. When the input is raised to around 0.5 V, the output is driven high. Components M4 and M5 are placed far away from latchup susceptible circuits so that they do not latch up.

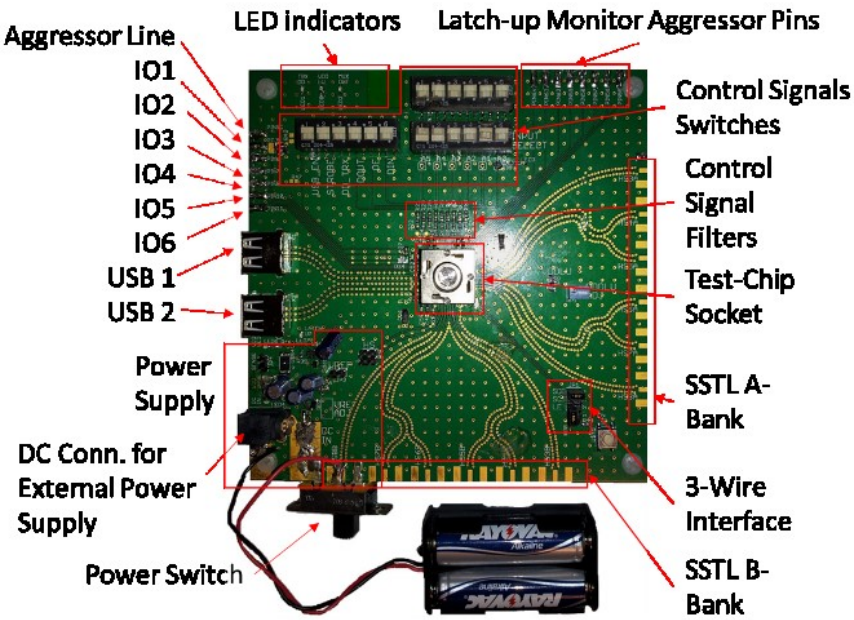


Figure 2.17: Board photograph.

Chapter 3 – Modeling and Optimizing Switching Speed of ESD Protection Devices

3.1 – Introduction

The ability of silicon controlled rectifiers (SCRs) to handle high current densities makes them an attractive ESD protection device. Unfortunately, SCRs do not turn on instantly, temporarily allowing large voltages to appear across their terminals and significantly compromising their ability to provide protection against very fast ESD transients, such as CDM or the first peak of a system-level ESD waveform. However, a well-designed trigger circuit may help limit the peak voltage seen across an SCR.

In order to design an optimized SCR-based protection circuit, the designer must understand how an SCR and its trigger circuit interact to determine voltage overshoot. The manner in which the trigger circuit is connected to the SCR determines what are the primary sources of overshoot; for example, for the case of a diode-triggered SCR, the data presented in [12] indicate that the STI-bound diode formed between the SCR anode and the N-well tap, which constitutes the first element in the trigger circuit, is responsible for the majority of the overshoot. Regardless of the SCR trigger circuit design, avalanche breakdown at the P-well/N-well junction provides an upper limit to the voltage overshoot [13], [14].

Circuit simulation may be used to aid in the design of an SCR-based protection circuit if the device compact models are known to accurately predict overshoot. Confidence in the predictive ability of an SCR model can be obtained only by comparing measurement and simulation over a wide range of conditions. Specifically, one should measure the transient response of an SCR in combination with a variety of trigger circuits and at a wide range of current levels. Next, one should simulate the response of the SCR when combined with each of

the trigger circuits, using a single set of parameters to describe the SCR in each of its configurations. If the measurement data and simulation results agree, the model has been validated and may be used subsequently for design optimization purposes. Such a broad validation of SCR compact model behavior was first done in the work presented in this chapter.

The SCR model validation procedure outline above is carried out in this chapter and circuit simulation is then used to identify possible design modifications for voltage overshoot reduction.

3.2 – Experiment

3.2.1 – Test Structures

The test structures used in this experiment include diode strings, diode-triggered SCRs (DTSCR) [15], resistively-triggered SCRs (RTSCR) [16], and grounded-gate NMOS triggered SCRs (GGSCR) [17], all fabricated in a 130 nm CMOS process.

The layout used for each of the three N-well diodes in the diode string is shown in Figure 3.1(a). Each diode has a separate guard ring that suppresses SCR effects within the diode string and allows each diode to be treated as a PNP transistor in which the emitter, base, and collector terminals correspond to the P+ diffusion, N+ diffusion, and P-guard ring, respectively. The diode string is connected as shown in Figure 3.1(b).

The layout for the DTSCRs and RTSCRs used in this experiment is shown in Figure 3.2(a). The RTSCR is formed by connecting a 50 Ω resistor between the N-well contact and ground, as shown in Figure 3.2(b). The resistor is fabricated using silicide-blocked P+ polysilicon. The RTSCR is not a practical protection circuit due to its high leakage; however, the resistive trigger will not show overshoot even on the CDM timescale, allowing the transient

response of the SCR to be studied separately from its trigger circuit. RTSCRs are generally more useful for parameter extraction than are avalanche-triggered SCRs. The currents inside an RTSCR are more similar to those present in a triggered SCR, and they provide for clear observation of the limiting effect that avalanche multiplication of the trigger current has on overshoot voltage. The DTSCRs used in this experiment are identical to the RTSCR of Figure 3.2, except that the resistor is replaced with the diode string illustrated in Figure 3.1.

The layout for the GGSCRs used in this experiment is fashioned after that in [17] and is illustrated in Figure 3.3(a). A schematic for the entire device is shown in Figure 3.3(b). A second GGSCR was also tested, in which the anode (A) to N-well tap (NW) spacing was 13 times larger.

3.2.2 – Measurement Apparatus

VFTLP data were obtained using a TLP-8010A from High Power Pulse Instruments (HPPI), which allows for variable pulse width and rise time. Measurement procedures follow the best practices outlined in Section 2.2, including post-processing for accurate peak voltage measurement. The voltage waveform at the device under test (DUT) is measured using a high impedance (2.5 kΩ) probe.

3.2.3 – Compact Models

The device compact models are implemented in Verilog-A. The compact model used for the N-well diodes is shown in Figure 3.4 and the equations used to represent each element are listed in Table 3.1. The diode model is closely related to the SPICE Gummel-Poon model. It has been expanded to include carrier multiplication due to impact ionization at the base-collector (N-well to P-well) junction, the formula for which is linearized near the breakdown voltage to promote convergence [18]. The expression for base resistance is also modified to reproduce

voltage overshoots that occur due to forward recovery [19]. The representation used here differs from [19] in that it neglects the effect of velocity saturation on the voltage drop in the base resistance; this simplification is acceptable, as long as the current density (and thus E-field) does not become extremely high. For simplicity, this model uses constant transit times, i.e. the diffusion charge stored at each junction is linearly proportional to the diode current across that junction. This simplification has been shown to not greatly affect simulation accuracy in [19].

The compact model used to represent the SCR is presented in [18]. It represents the SCR as a pair of cross-coupled bipolar transistors using modified Ebers-Moll equations. In contrast to previous SCR models [20], [21], the collector resistances are oriented in a way that allows them to contribute to the voltage drop between the anode and cathode, resulting in a continuous model that accurately represents conduction in an SCR's on-state. This model uses a base resistance model similar to that used in the N-well diode model presented in Table 3.1, which is essential for representing overshoot due to the SCR's resistance in series with the trigger circuit. Impact ionization induced multiplication of both the trigger current and the leakage current at the N-Well/P-well junction is also modeled.

The Verilog-A models described above are used together to simulate the DTSCR's behavior.

3.2.4 – Simulation Setup

Circuit simulations of the schematic shown in Figure 3.5 are performed using Spectre. The block marked Rise time Filter contains the five section low-pass filter [22] shown in Figure 3.6. This circuit may not provide a precise representation of the rise time filter incorporated in a specific commercial TLP tester, but its behavior closely resembles that of the rise time filters used in high-quality TLP systems. This filter has uniform group delay in the pass band, which

gives a clean rising edge, and very low reflections from both ports at all frequencies, which prevents ringing in the voltage and current waveforms due to mismatch at the device under test (DUT). The filter component values are listed in Table 3.2. The component values have been parameterized in terms of rise time by using the relationship between low-pass filter cutoff frequency and rise time:

$$f_c = \frac{0.34}{t_r}. \tag{3.1}$$

Figure 3.7 shows the pulse shape obtained when simulating the schematic in Figure 3.5 for the case of a 1 Ω load; despite the large mismatch, a clean pulse is produced.

3.3 – Results and Discussion

3.3.1 – Non-Uniform Conduction

Before presenting the main results of this experiment, it is worthwhile to discuss the effect of non-uniform conduction on the validity of simulation results. Compact models provide a description of the device terminal currents and thus generally assume that conduction across the device width is uniform. However, SCRs and snapback devices in general may exhibit non-uniform conduction as a consequence of having a region of negative differential resistance (NDR) [23]. Non-uniform layout across the device width will promote non-uniform conduction. Non-uniform conduction may lead to differences between simulation and measurement.

The GGSCR layout shown in Figure 3.3 is not uniform across the device width. This device's TLP I-V curve is shown in Figure 3.8; following snapback, there is a region in which $R_{on} \approx 0$, indicative of non-uniform conduction across the device width [23], which cannot be captured by conventional compact models.

Increasing the series resistance between the anode and N-well diffusions should lead to more uniform conduction [24]; however, evidence of non-uniform conduction occurs even in the GGSCR with increased A-NW spacing. This device's pulsed I-V curve, shown in Figure 3.9, shows significant variation with pulse rise time and duration. For a fixed rise time of 1 ns, the I-V curves obtained using 10 ns and 25 ns long pulses differ because a larger portion of the device width is conducting current at 25 ns than at 10 ns [23]; at high current densities, the on-resistance is further modified by pulse width dependent self-heating. For a fixed pulse width of 10 ns, the I-V curve varies as a function of the pulse rise time; this is caused by the action of two different triggering mechanisms. For slow rise times, the trigger circuit injects current at the center of the device; however, for fast rise times, the N-well/P-well junction's displacement current is an additional triggering current and it is injected uniformly across the device width. The improved triggering due to displacement current accounts for the more complete turn-on observed at fast rise times. The time-dependent spatially non-uniform current distribution prevents accurate circuit simulation of the GGSCR on short timescales. However, circuit simulation may be used to reproduce or predict this GGSCR's quasi-steady state behavior, as demonstrated by the 100 ns TLP I-V curves shown in Figure 3.10. The good fit of the simulated I-V curve to that obtained from measurements suggests that if conduction were uniform across the device width, the modeling approach used in this chapter could be applied to these GGSCRs, or P-well triggered SCRs in general.

In contrast, the DTSCR and RTSCR shown in Figure 3.2 will show uniform conduction prior to the onset of and after the completion of snapback because these SCRs have uniform layout. This allows the peak voltage, which occurs at the immediately at the onset of snapback,

to be simulated, even if non-uniform conduction during the snapback process leads to simulation inaccuracies as the voltage across the device collapses.

3.3.2 – RTSCR and DTSCR Model Validation

Figure 3.11(a)-(c) present the peak voltage for the diode string, RTSCR, and DTSCR, derived from both measurement and simulation. The peak voltage is obtained for three different values of pulse rise time (300 ps, 600 ps, and 1 ns) and a wide range of pulse amplitudes. For comparison, the quasi-static pulsed I-V curve (10 ns pulse width and 1 ns rise time) is also plotted. Simulation and measurement agree within 15% for all data points and the dominant trends are correctly replicated for each device. It is very difficult to pinpoint the cause of the discrepancy. One possible cause is parameter extraction error. A second possible cause is modeling simplifications, such as neglecting how base transit times vary with base current or base/collector bias and neglecting velocity saturation in the base resistance. A third possible cause is in the model of how the current gain of each transistor in the SCR changes based on the collector current of the other transistor. (This behavior only occurs in an unstable state, so it is not directly measureable; an arbitrary functional form is used that demonstrates the correct theoretical trend.) Lastly, some error could be caused because the 3-D structure is being represented by a 1-D model; effects like time-varying non-uniform conduction across the device width cannot be modeled using the approach used in this chapter [23]. The parameter values used in the diode and SCR models are consistent between all simulations (including the GGSCR simulation shown in Figure 3.10). Sample transient waveforms from measurement and simulation are plotted in Figure 3.12(a)-(c) to provide further validation of the models. The measurement data in Figure 3.11 and Figure 3.12 yield two key observations: (1) the diode string's overshoot is significant and must be taken into account when designing a DTSCR, (2)

even though the diode string has a much lower impedance than the resistive trigger, the DTSCR has only marginally lower overshoot during worst-case (fast rise time, high current) events than does the RTSCR.

Figure 3.13 shows the simulated peak voltage drop between the emitter and base contacts of each diode in the DTSCR's diode string, including the diode formed by the SCR anode and its N-well, denoted as D0. It is immediately apparent that every diode in the string contributes to overshoot; however, the diode intrinsic to the SCR provides the dominant contribution. In all cases, the overshoot occurs primarily in the series resistance of the N-well prior to conductivity modulation. Diode D0 has the dominant contribution to the overshoot for two main reasons. First, D0 has twice the current density in its resistive base region as do D1-D3; as seen in layout, D1-D3 have an additional N+ contact stripe. Second, the Darlington effect reduces the current in each subsequent diode in the string [25]. Note that impact ionization at the SCR's N-well/P-well junction provides a significant alternate current path to ground that bypasses part of the resistance between the emitter and base of D0, thereby limiting overshoot [13].

3.3.3 – DTSCR Design Optimization

Identifying the sources of overshoot permits one to propose ways to reduce it. The most direct way is to reduce the resistance of the SCR well regions that lie in series with the trigger circuit and, to a lesser extent, the resistance of the trigger circuit itself. This can be done by either increasing the width of the SCR and the trigger diodes, which was explored in [26], or by using poly-bound diodes to minimize the distance between the diodes' anode and cathode, which was explored in [1]. The latter approach further reduces overshoot by reducing the volume of silicon, allowing conductivity modulation to reduce this path's resistance more quickly. Alternatively,

the overshoot could be limited by reducing the breakdown voltage of the N-well/P-well junction, a concept used in low voltage triggered SCRs (LVTSCRs) [27].

Each of these options may be evaluated using the simulation models. Circuit simulation is used to compare the effects of (1) doubling the size of the trigger diodes D1-D3, (2) effecting a 2/3 reduction in the base resistance of D0-D3 by adopting a poly-bound diode structure rather than STI-bound and, (3) reducing the N-well to P-well breakdown voltage. There are numerous techniques that could be used to reduce the well breakdown voltage, for example, by including a heavily doped N-buried layer. The results of this comparison are shown in Figure 3.14. All three modifications are helpful; however, reducing the breakdown voltage and using poly-bound diodes give a dramatic improvement, whereas increasing the trigger diode size provides only a modest improvement.

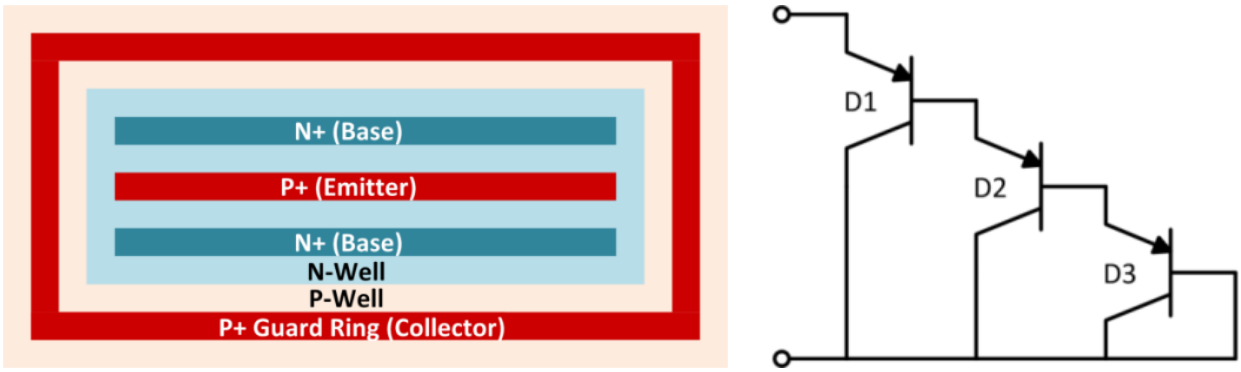
Though decreasing the well breakdown voltage is generally not an option for users of a LVCMOS process, switching to poly-bound diodes is feasible. Simulation may be used to demonstrate whether or not switching to poly-bound diodes is beneficial when other considerations such as area and capacitance are included in the analysis. In this 130 nm process, the oxide breakdown voltage is about 7 V. The poly-bound DTSCR's overshoot reaches 7 V at a current density of 34 mA/µm (1.7 A), whereas the original SCR circuit's measured overshoot reaches 7 V at 13.2 mA/µm (0.66 A). Thus, to protect against a fixed current stress without secondary protection, a poly-bound DTSCR would require less than 40% of the area of an STI-bound DTSCR. Defining I_{Fail} as the current corresponding to a V_{peak} of 7 V, both devices have similar I_{Fail}/C, which are 16.5 mA/fF and 16.2 mA/fF, respectively. The capacitance values used in these calculations are those of D0, which sets the upper bound on the SCR circuit's capacitance, and are estimated based on information in the PDK. This analysis suggests that

using a poly-bound DTSCR rather an STI-bound DTSCR will save area without degrading bandwidth.

3.4 – Conclusions

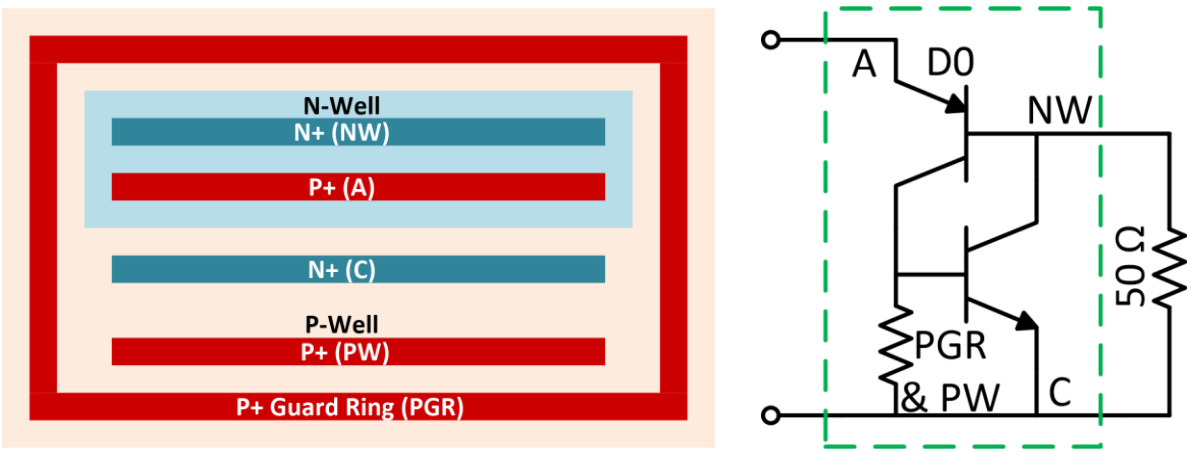
Circuit simulation has been used successfully to reproduce many observations about SCR overshoot that are found in the literature [12], [13], [24]. This establishes the feasibility of using circuit-level simulation to optimize the design of SCR trigger circuits. The overshoot voltage is determined by the fastest responding current paths: the path through the trigger circuit and impact ionization at the N-well/P-well junction. Circuit simulation suggests that the two most effective ways of reducing DTSCR overshoot involve the use of poly-bound diodes within the SCR and reducing the N-well/P-well breakdown voltage. Of course, increasing the SCR width would achieve the same goal, but at the expense of area and capacitance.

3.5 – Figures and Tables



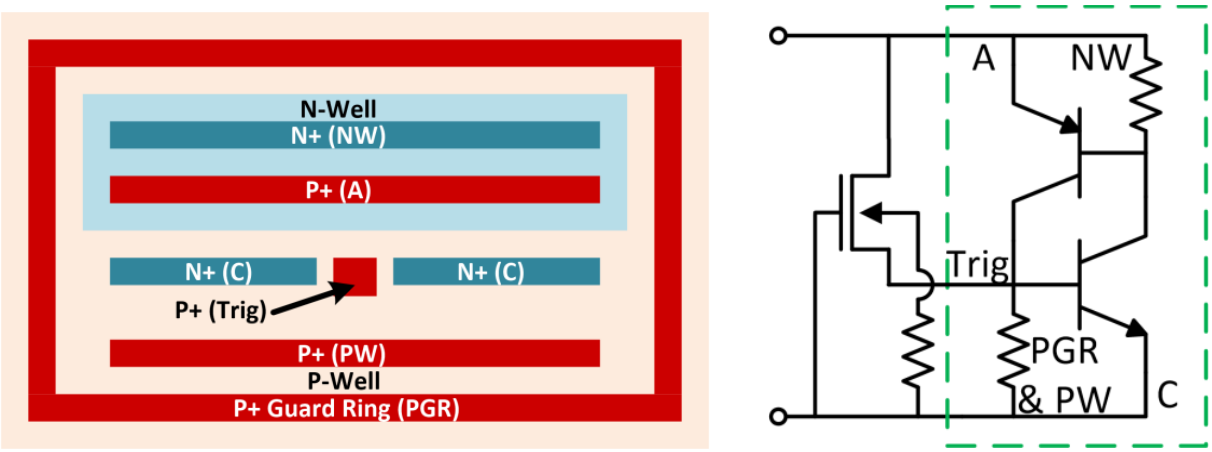
(a) (b)

Figure 3.1: (a) Layout (not drawn to scale) of each diode in the diode string. Each diffusion stripe is 50 μm wide; all other dimensions are minimum allowed by the design rules. (b) Diode string schematic.



(a) (b)

Figure 3.2: (a) Layout (not to scale) of the DTSCRs and RTSCRs. All layout dimensions are the minimum allowed by design rules, except for the N+ cathode to PW spacing. Each stripe is 50 µm wide. (b) RTSCR schematic. A dashed box divides the SCR-related components from the external trigger circuit components. The terminals PW and PGR are connected on-chip with metal. In the DTSCR, the trigger resistor is replaced with the diode string of Figure 3.1(b).



(a) (b)

Figure 3.3: (a) Layout (not to scale) of the GGSCR. With the exception of the addition of the P+ triggering diffusion (Trig), the layout is identical to that of the DTSCR and RTSCR. This modification reduces the total cathode (C) width from 50 µm to 47 µm. (b) GGSCR schematic. The GGNMOS is a silicide-blocked low-voltage transistor.

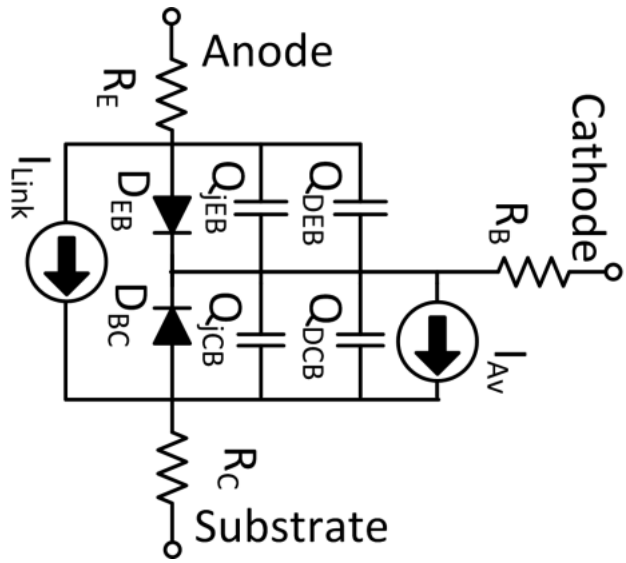


Figure 3.4: Schematic of N-well diode compact model.

Table 3.1: Model equations for N-well diode compact model. Departures from the SPICE Gummel-Poon model are highlighted in yellow. R_E and R_C are constant values, whereas R_B is variable.

$I_F = \boldsymbol{I_S}\left[exp\left(\frac{V_{EB}}{V_T}\right) - 1\right]$	$I_R = \boldsymbol{I_S}\left[exp\left(\frac{V_{CB}}{V_T}\right) - 1\right]$
$q_1 = \frac{1}{1 - \frac{V_{BC}}{\boldsymbol{V_A}} - \frac{V_{BE}}{\boldsymbol{V_B}}}$	$q_2 = \frac{I_F}{\boldsymbol{I_{KF}}} + \frac{I_R}{\boldsymbol{I_{KR}}}$
$q_B = \frac{q_1}{2}\left(1 + \sqrt{1 + 4q_2}\right)$	$I_{Link} = \frac{I_F - I_R}{q_B}$
$I_{DEB} = \frac{I_F}{\boldsymbol{\beta_F}}$	$I_{DCB} = \frac{I_R}{\boldsymbol{\beta_R}}$
$Q_{EB} = \boldsymbol{\tau_F} I_F + Q_j(V_{EB})$	$Q_{CB} = \boldsymbol{\tau_R} I_R + Q_j(V_{CB})$
$R_B = \boldsymbol{R_{contact}} + \frac{\boldsymbol{R_{B,Si}}}{1 + \frac{\boldsymbol{\tau_F} I_F}{\boldsymbol{Q_{B0}}}}$	
$I_{Av} = (I_{DCB} + I_{Link})\left(\frac{1}{1 - \left(\frac{V_{Av}}{\boldsymbol{BV}}\right)^{\boldsymbol{m}}} - 1\right)$	

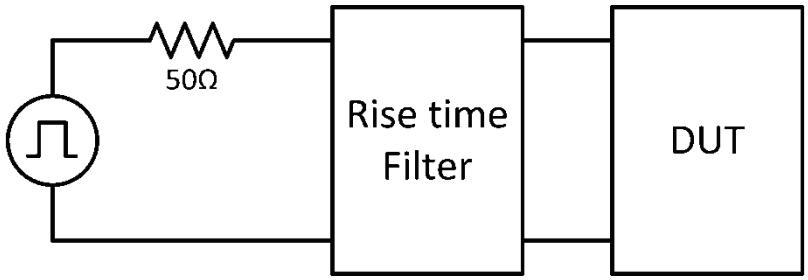


Figure 3.5: Schematic used for simulations. The pulse source provides an ideal trapezoidal voltage pulse with 1 ps rise time. The device under test (DUT) is a diode string, RTSCR, or DTSCR.

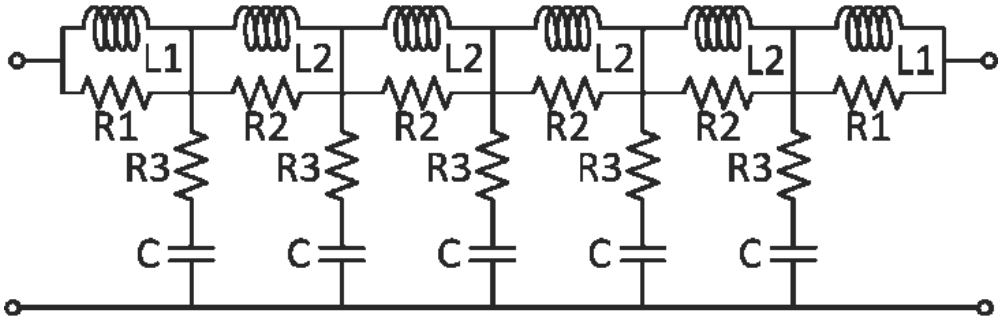


Figure 3.6: Rise time filter schematic. Component values are listed in Table 3.2.

Table 3.2: Component values for rise time filter shown in Figure 3.6. The inductors and capacitors are described as a function of rise time, allowing the filter to have an adjustable bandwidth.

R1	50 Ω
R2	390.625 Ω
R3	6.4 Ω
L1	$7.62 \cdot t_r$ H
L2	$15.24 \cdot t_r$ H
C	$6.096 \cdot 10^{-3} \cdot t_r$ F

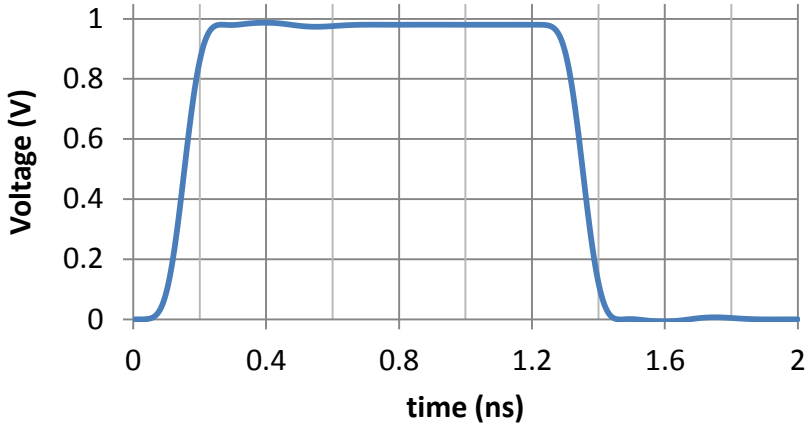


Figure 3.7: Simulated voltage across a poorly matched DUT (a 1 Ω resistor) using the schematic from Figure 3.5. The rise time filter is configured to produce a 100 ps 10%-90% rise time. The 50 V input pulse has a 1.2 ns pulse width and 1 ps rise and fall times.

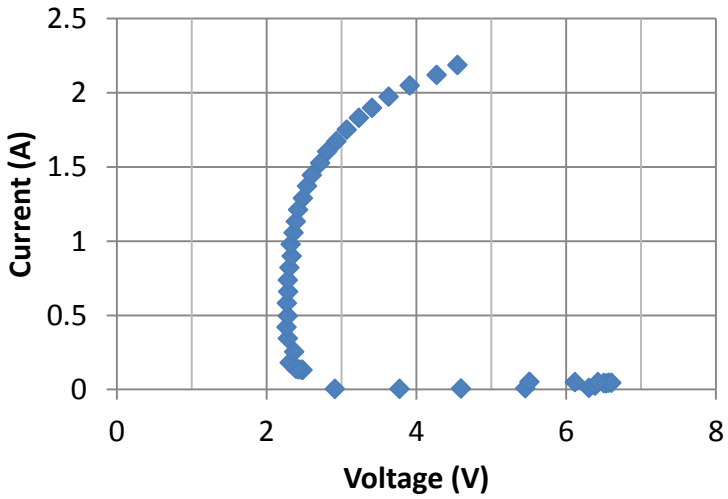


Figure 3.8: TLP I-V curve of the GGSCR shown in Figure 3.3. The vertical section in the I-V curve indicates non-uniform conduction across the device width. The pulse duration and rise time are 100 ns and 10 ns, respectively.

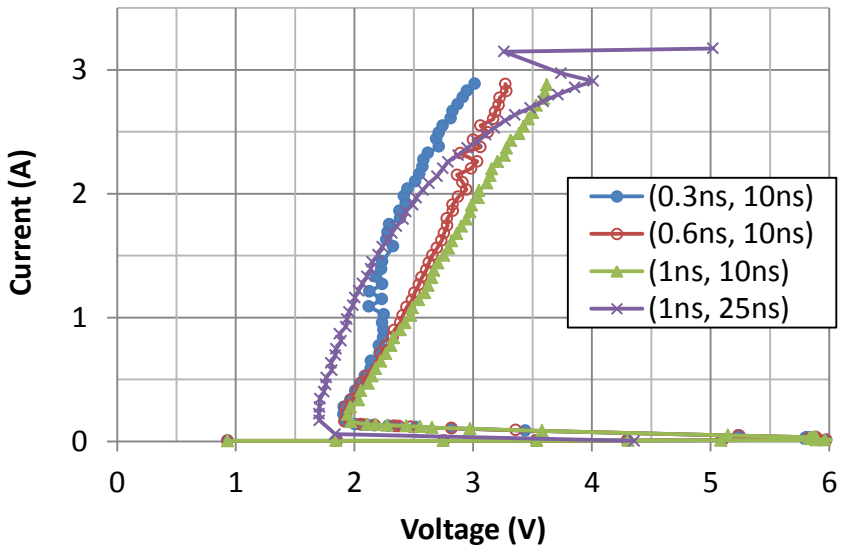


Figure 3.9: TLP I-V curves of the GGSCR with increased A-NW spacing. Legend entries are of the form (rise time, pulse width).

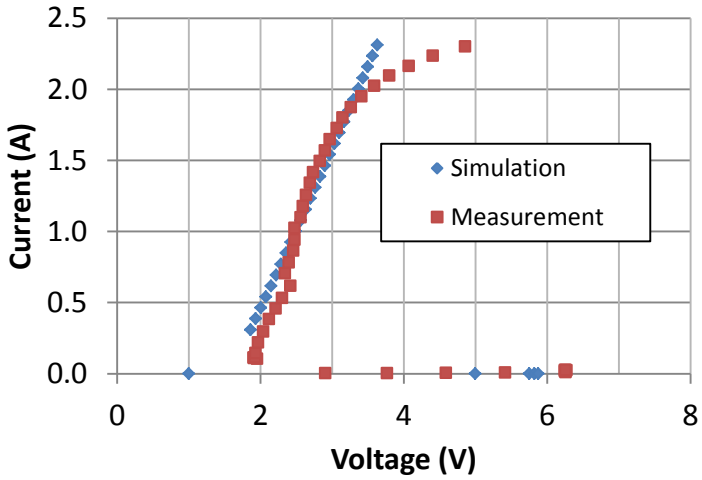


Figure 3.10: TLP I-V curve for the GGSCR with increased A-NW spacing. The pulse width and rise time are 100 ns and 10 ns, respectively. Self-heating in the SCR was not simulated, leading to an under-predicted R_{on} at high currents; however, self-heating can be included in the SCR model [20]. The GGNMOS is represented by a piece-wise linear Verilog-A model.

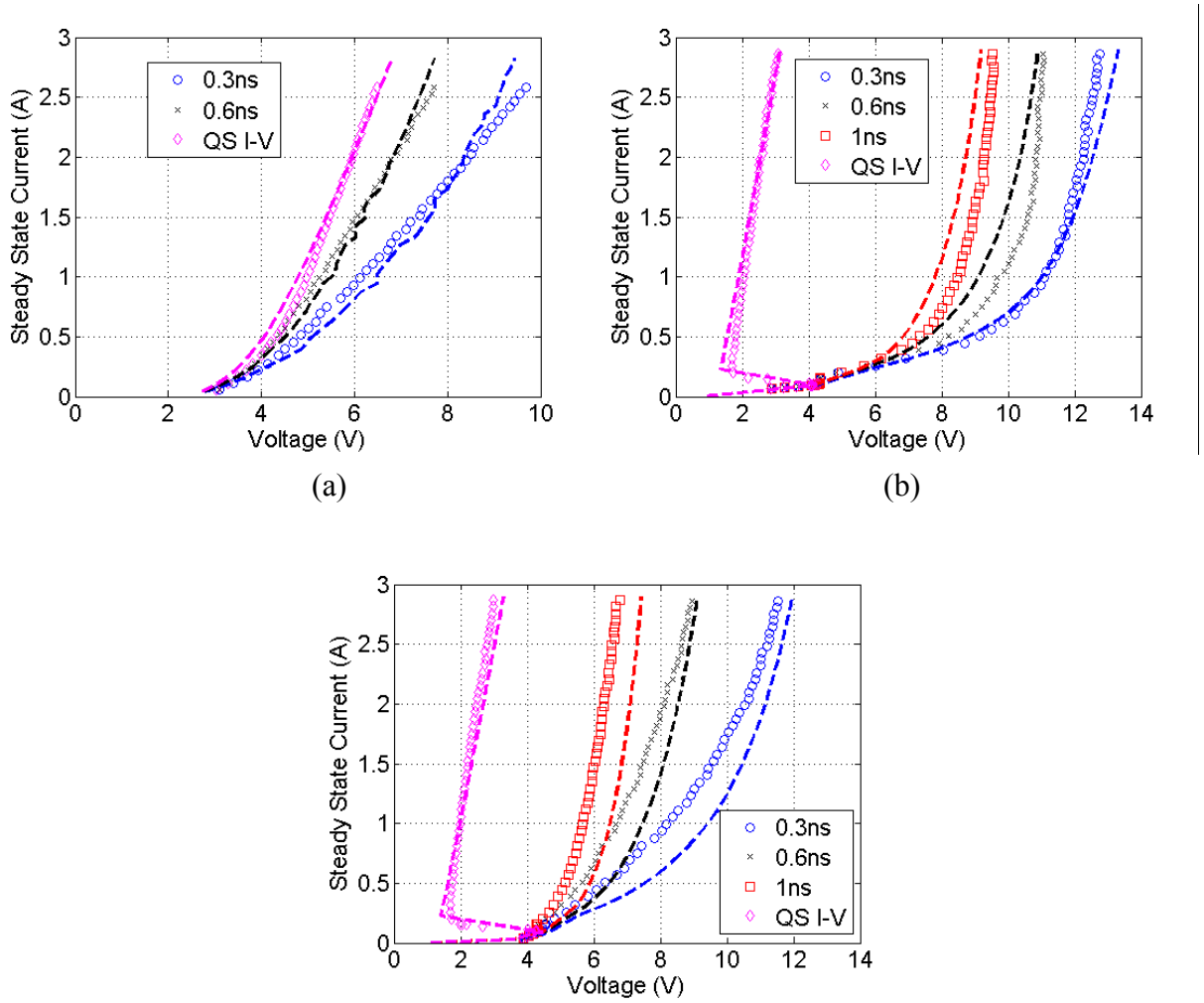
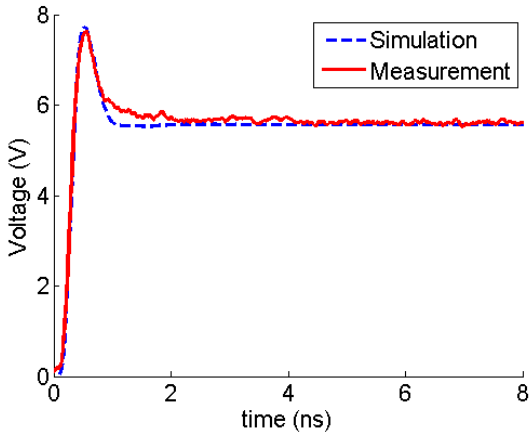
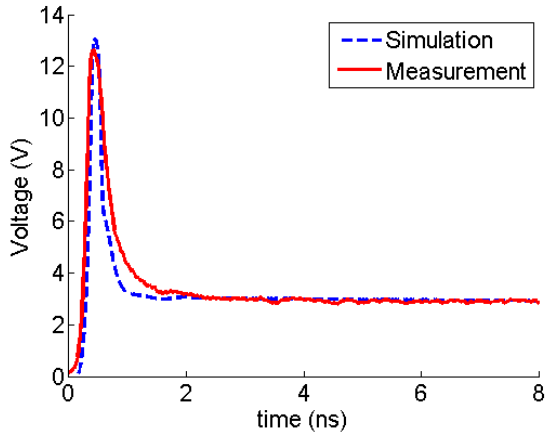


Figure 3.11: Plot of peak voltage and steady-state voltage as a function of steady-state current for (a) diode string, (b) RTSCR, and (c) DTSCR. TLP rise time ranges from 300 ps to 1 ns. Symbols are measurement data; dashed lines are the corresponding simulation results.



(a)



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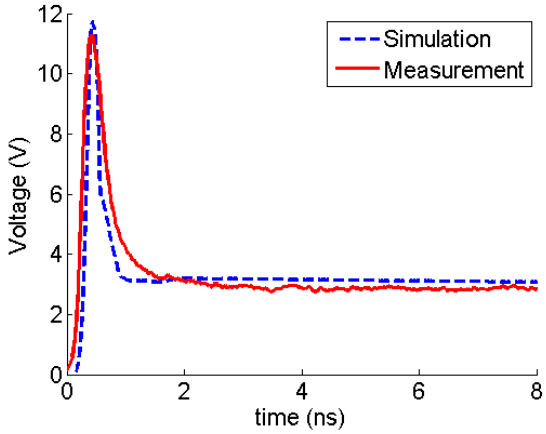


(c)

Figure 3.12: Sample transient voltage waveforms from both measurement and simulation for the (a) diode string at 1.65 A, (b) RTSCR at 2.60 A, and (c) DTSCR at 2.60 A. The rise time filter is configured for 300 ps rise time.

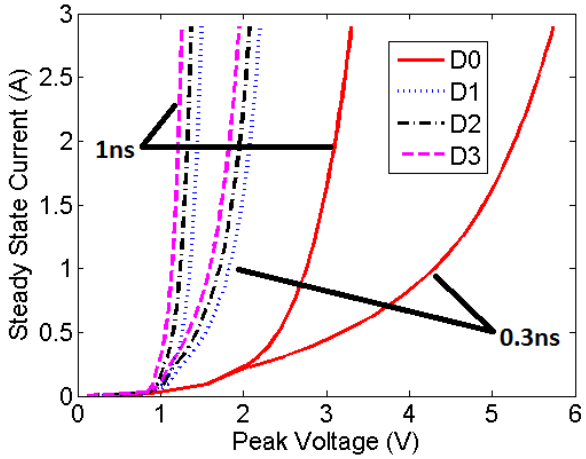


Figure 3.13: Simulated, peak voltage across each component of the DTSCR trigger circuit as a function of steady-state current for 1 ns and 0.3 ns rise times. Overshoot is most severe in D0, and progressively less severe in D1, D2, and D3.

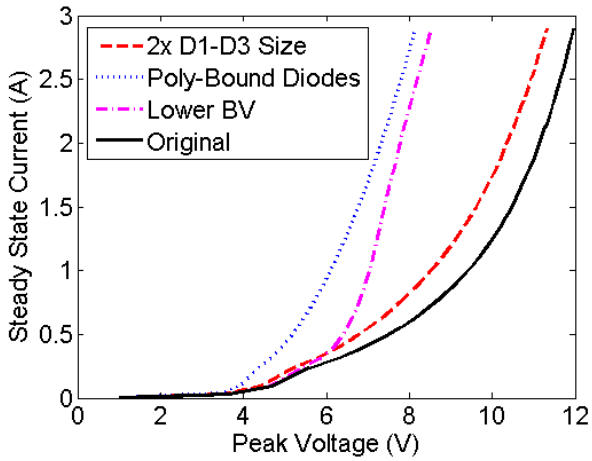


Figure 3.14: Several modifications to the DTSCR are evaluated using simulation. Peak voltage is plotted vs. steady-state current for a 0.3 ns rise time.

Chapter 4 – ESD Gun Circuit Model

4.1 – Introduction

As discussed in Chapter 1, it is often required that electronic equipment is qualified for immunity to system-level ESD according to the IEC standard [1]. A recent trend in the electronics industry is to push system-level ESD requirements onto individual components (usually an IC), rather than including dedicated ESD protection devices on a PCB. Because of the high up-front costs of fabricating an IC, it is highly desirable that the component pass ESD qualification testing on the first silicon spin, making accurate simulation of stresses caused by ESD guns increasingly important.

Techniques used to obtain the output waveform of an ESD gun include full-wave simulation, S-parameter characterization [28], and circuit simulation [29], [30]. Full wave simulation is useful because it provides a complete description of the system, including currents and E/H fields; however, it is generally not practical because it requires detailed knowledge of the testing environment and significant computational time. An S-parameter based approach, while accurate, provides no insight into the behavior of the system because it is purely measurement based. In contrast, a circuit model is very simple to implement and simulate and can provide insight into the behavior of the system.

Existing circuit-level models [29], [30] are not developed with an IC designer's needs in mind. Both works represent the discharge as an electromagnetic interference (EMI) phenomenon, whereas for IC designers, ESD is typically a current injection problem. The two different perspectives impose different requirements on the model. From an EMI point of view, accurate modeling of the current spectrum is important as stress is often caused by inductive coupling; however, for most IC applications accurate prediction of the ESD current into a small

impedance is much more important. Highly filtered pins are one important exception. For example, in RF pin applications, system level highpass/bandpass filters may shunt most of the ESD current (which contains most of its energy below 100 MHz) away from the IC pin. Unlike the attenuated low-frequency content, the high-frequency current components will reach the DUT; however, the high-frequency content varies greatly from ESD gun to ESD gun [31]. In filtered pin applications, an S-parameter based approach may be more useful because it can reproduce the high-frequency content from a specific ESD gun more accurately. Due to these considerations, an alternative circuit model, which can accurately simulate the transient current from an ESD gun, would be more useful for IC designers. Ideally, this model would be sufficiently flexible such that it can be easily adapted to model discharges from ESD guns other than those targeted for IEC 61000-4-2, such as those used for ISO 10605 testing [2].

This chapter presents a circuit model that produces current waveforms similar to that specified in [1] with more precision and flexibility than currently available models. The model is intended to simulate contact discharge into an IC, and focuses on low impedance loads.

4.2 – Model Development

The model proposed in this chapter is intended to replicate the output waveform from an ESD gun into a low impedance ESD protection device, without specific knowledge of what is inside the gun; nevertheless, the model corresponds reasonably well to the physical circuit of an ESD gun. A 2 Ω load is used to represent the DUT because the test load for ESD guns in the IEC 61000-4-2 standard is 2 Ω, which is much lower than the source impedance of the gun. The impedance of the DUT will likely be close to or slightly less than 2Ω, the current waveform will not significantly change with moderate variations in impedance because the ESD gun is acting like an ideal current source. The model development procedure is as follows. First, as indicated

in [1], the IEC 61000-4-2 current waveform may be represented as the sum of two transients: one with a short duration of about 5 ns, and one with a larger duration of about 100 ns. The two transients are assumed to be the response of two separate series-RLC circuits discharging into the test load. The initial conditions for each RLC circuit are $V_C = V_{precharge}$ and $I_L = 0$, where V_C is the voltage across the capacitor and I_L is the current through the inductor. To complete the model, the two series RLC circuits are connected as shown in Figure 4.1. The circuit element values are such that the two RLC circuits interact only weakly. The fast RLC circuit generates a transient with high-frequency spectral content to which L_{slow} presents a high impedance, thus the fast RLC circuit will primarily discharge through the low impedance load. Analogously, the slow RLC circuit will discharge through the low impedance load because C_{fast} presents a high impedance due to the low-frequency spectral content of the slow transient. The various R, L, C values are tuned to produce the desired current waveform.

The starting values of the R, L, C parameters, prior to fine-tuning, are found as follows. The fast current transient has a shape similar to that produced by a critically damped RLC circuit with zero initial current, namely

$$i(t) = i_{peak} \cdot \left(\frac{t}{\tau}\right) exp\left(1 - \frac{t}{\tau}\right). \tag{4.1}$$

The peak current i_{peak} appears explicitly in (4.1). From (4.1), the 10%-90% rise time of the fast transient is 0.57τ. Due to subtle interactions between the fast and slow RLC circuits, in practice, setting τ to be 1.625 times the desired 10%-90% rise time enables the circuit model to best reproduce the IEC 61000-4-2 reference waveform. Next, the values of R_{fast}, L_{fast}, and C_{fast} are obtained in terms of ($i_{peak}/V_{precharge}$) and τ.

For a critically damped RLC circuit, the following equations apply:

$$\tau = \frac{2L_{fast}}{R_{fast}}, \tag{4.2}$$

$$R_{fast}\sqrt{C_{fast}} = 2\sqrt{L_{fast}}, \tag{4.3}$$

$$\frac{i_{peak} \cdot e}{\tau} = \frac{V_{precharge}}{L_{fast}}. \tag{4.4}$$

Solving (4.2)-(4.4) for R_{fast}, L_{fast} and C_{fast}, the resulting design equations are:

$$R_{fast} = \frac{2}{e} \cdot \frac{V_{precharge}}{i_{peak}} \tag{4.5}$$

$$L_{fast} = \frac{\tau}{e} \cdot \frac{V_{precharge}}{i_{peak}} \tag{4.6}$$

$$C_{fast} = \tau \cdot e \cdot \frac{i_{peak}}{V_{precharge}}. \tag{4.7}$$

The characteristics of the slow current transient are dominated by the nominal 330 Ω, 150 pF RC time constant specified in [1], and thus R_{slow} and C_{slow} are initially set to 330 Ω and 150 pF, respectively. An initial value of 3 μH for L_{slow} was empirically found to give a good fit in simulation.

Finally, the component values are finely tuned to match the IEC 61000-4-2 reference waveform. Throughout this process, the fast RLC circuit's i_{peak} parameter is varied (resulting in new R_{fast}, L_{fast}, and C_{fast} values) to correct for interactions between the RLC subcircuits. R_{slow} was adjusted to control the current amplitude but the slow RLC circuit's RC product was kept constant. Adjustments to L_{slow} were not necessary, but in principle could be used to vary the shape of the second peak.

The IEC 61000-4-2 test standard not only describes a nominal waveform; it also describes the acceptable excursions. The various parameters in the circuit model may be adjusted

to produce waveforms closer to the limits. Component values for each optimization are listed in Table 4.1.

4.3 – Physical Interpretation of the Model

It is worthwhile to consider the physical origins of the various components in the circuit-level model of the ESD gun.

As noted previously, when the two RLC circuits are merged as shown in Figure 4.1, the independent operation of each is roughly preserved. Furthermore, this topology provides a physical mapping to the effective inductances of the ESD gun. The smaller inductor, L_{fast}, is associated with the tip of the ESD gun and the larger inductor, L_{slow}, is associated with the return cable. Similar inductances are used in other ESD gun models [29], [30].

In Table 4.1, the nominal values of R_{slow} and C_{slow} differ slightly from the 330 Ω and 150 pF values given in [1]. This is attributed to the action of the ESD gun's internal relay. As the internal relay closes, some of the initial charge on the (physical) 150 pF capacitor will be shared with parasitic capacitances of the ESD gun and the test environment. The charge on the main capacitor will be reduced by this transfer. The coupling paths are not included in the circuit model, but their impact is captured by reducing the value of C_{slow} below 150 pF. Similarly, because the charge (and therefore voltage) on the 150 pF capacitor has been reduced, the value of R_{slow} must be made larger than 330 Ω so that the simulated current will well match that produced by the real gun.

R_{fast} and C_{fast} do not have the clear physical analogs that the other components in the circuit model have. Instead, they represent displacement current paths that bypass the ESD gun's return cable [29]. The initial charge stored on C_{fast} can be thought of as charge shared from the main 150 pF capacitor to the surrounding environment when the relay in the ESD gun closes.

This charge will be shared primarily with conductors closest to the ESD gun, which is typically either the ground plane or the metal table top.

4.4 – Simulation Results

Figure 4.2 provides a comparison between the IEC-61000-4-2 reference waveform and the waveforms obtained from circuit simulation of the model presented in Section 4.2. The simulations were performed using each set of component values in Table 4.1. The markers at 30 ns and 60 ns represent the nominal current value at each of these times and the maximum acceptable excursions, as specified in [1]. The shapes of the simulated waveforms are very similar to that of the IEC-61000-4-2 reference waveform. Notably, the simulated current is very close to the target value at 30 ns and 60 ns.

Figure 4.3 shows the same simulation results plotted on a shorter timescale. In this plot, the markers denote the nominal peak current values and maximum acceptable excursions. The 10%-90% rise time for each of the three simulated waveforms closely conforms to the corresponding maximum, minimum, or nominal value given in the IEC standard. The rising edge of the reference waveform and that of the simulated waveform for the nominal case are slightly different in appearance; however, the important characteristics are accurately represented in simulation, e.g., both waveforms have very similar 10%-90% rise time. The main differences between the two are that the reference waveform is slightly delayed and that the current derivatives are different at the beginning of the stress. In most IC applications, the stress is caused primarily by the injected current, so these differences do not affect the utility of simulation results; however, if inductive coupling causes significant stress, the differences in the current derivatives (di/dt) could lead to simulation errors. The testing environment will significantly affect the initial part of the waveform, so attempting to reproduce the exact details

of the initial pulse in calibration does not guarantee that it will match the waveform during testing; thus a simple, general model is preferred.

4.5 – Application

Circuit simulation using the model presented in this chapter was used to diagnose unexpected failures in a general purpose I/O, and to evaluate possible corrective actions. The I/O in question was designed to tolerate high voltages and to survive a discharge from an ISO 10605 gun [2] at a 15 kV precharge voltage. Additionally, the pin was designed to tolerate an external capacitive rise time filter of up to 22 nF to limit radiated emissions. This I/O was protected by an on-chip SCR with V_{t1} of 47 V and I_{t2} of 5 A. The SCR parameters were extracted from TLP with a 500 ns pulse width.

When the design was fabricated and tested with the application specific capacitive filter connected to the pin, it failed during ten sequential 0.5 kV discharges (the minimum test voltage) or one 2 kV discharge, instead of the designed-for 15 kV. To determine the cause of the failure, the pin's response was simulated using a modified version of the model presented in Section 4.2. Specifically, the values of R_{slow} and C_{slow} were changed to 2 kΩ and 330 pF to produce an ISO 10605 waveform. Additionally, a circuit was added to re-establish the initial conditions in the ESD gun, which allowed the repeated strikes required for ISO 10605 testing to be simulated. This circuit is shown in Figure 4.4. While both ISO 10605 and IEC 61000-4-2 allow the DUT to return to its original condition between strikes, they do not explicitly require it. In practice, returning the DUT to a normal state would require either operator intervention or a modification of the test setup. Simulating multiple strikes is useful because it emulates a common test setup in which the DUT does not return to a normal state.

Simulation results, shown in Figure 4.5, indicate that the failure is caused by the filter capacitor discharging into the DUT during snapback. Initially, the current from the ESD gun charges the (large) filter capacitor. Once the voltage across the capacitor reaches V_{t1} of the SCR, the device snaps back and enters its low impedance state, causing the capacitor to rapidly discharge into the I/O. For single strikes, this discharge occurs at precharge voltages of 2 kV in measurement and 3.5 kV in simulation. The discrepancy is believed to come from the capacitor model, which does not include changes in capacitance at high voltages. During this discharge, the peak current into the I/O exceeds I_{t2} of the SCR, producing failure. The DUT voltage and current from simulation with precharge voltages of 3.5 kV and 15 kV are shown in Figure 4.5. The peak current is the same in both cases. When repeated strikes are simulated, a similar discharge waveform is observed after several strikes have charged up the capacitor. This can be observed at precharge voltages as low as 0.5 kV. Failures at low precharge voltage could not be predicted without simulating repeated strikes; a single low voltage strike does not contain sufficient charge to allow the filter capacitor to charge to V_{t1}.

Simulation shows that by replacing the capacitive filter with a series RC filter, the peak discharge current can be reduced to a manageable level. A 10 Ω resistor in series with the 22 nF capacitor was sufficient to limit the current into the I/O during snapback to below the SCR's I_{t2}. Simulated I_{DUT} for the original and modified circuits are shown in Figure 4.6. In the lab, when the series resistor is added to the test setup, the DUT survives up to a 15 kV discharge.

4.6– Influence of System-Level Test Environment on Floating DUT

In this section, the simulation model will be used to examine the influence of changes in the system-level test environment on the stress level observed by a DUT not connected to earth

ground, such as a cell phone. In such a case, the (capacitive) return path is defined primarily by the testing environment, rather than connections to the DUT.

To determine the effect of changes in the capacitive return path between the metal table top and ground plane below the table, the current through a 2 Ω load is simulated for different capacitances between the table and ground. A circuit schematic for these simulations is shown in Figure 4.7. The fast RLC circuit's return path is connected to the metal table top rather than the ground plane for the reasons discussed in Section 4.3. The slow RLC circuit's return path is through the ground plane below the table because the ESD gun's cable is physically connected there. The simulated DUT current is shown in Figure 4.8 for C_{table} values ranging from 50 pF to 1 nF. The current with the table top shorted to ground is also plotted for comparison. The simulation results suggest that for capacitances on the order of 100 pF, the DUT current is highly sensitive to changes in the test environment. This effect can be explained by the fact that the stress will be determined by charge sharing between C_{slow} and C_{table}. For large values of C_{table}, the voltage on the table will never reach an appreciable value, so the stress current will be similar to the case where the DUT is well grounded. However, if C_{table} is close in value to C_{slow}, charge sharing will cause a significant voltage to build up between the table and the ground plane. This voltage would have otherwise been dropped across the resistor inside the ESD gun, thus adding C_{table} in series with the DUT will reduce the DUT current relative to the case when the DUT is well grounded.

To interpret the preceding analysis in the context of a typical test setup, the capacitance between the table top and ground plane was measured using an LCR meter for several variations in test setup. The table on which these measurements were conducted was far from any walls and had a power strip built into the table parallel to the edge. When the power strip is left floating,

the capacitance between the table and ground were measured at 80 pF. When the power strip is connected to the building's electrical system, the table capacitance was measured at 136 pF. The large change is due to the fact that the ground in the power strip is much closer to the table top than the ground plane below the table. These capacitances are in the range where the simulated current injected from the ESD gun is highly sensitive to changes in C_{table}. Additionally, the fact that the table capacitance changed so much when a closer ground was provided suggests that the presence of any ground connected device on the test table, such as an oscilloscope or power supply, could significantly change test results on a floating DUT.

4.7 – Conclusion

Circuit-level modeling of contact discharge stress from an ESD gun allows one to simulate the response of a component to system-level stress, permitting pre-Si design verification. The model presented in this chapter has very good agreement with the IEC 61000-4-2 waveform. In contrast to the prior art, the model accurately predicts injected currents to facilitate IC design and includes the ability to simulate strong, nominal, and weak IEC-61000-4-2 compliant waveforms. The various elements in the circuit model have been mapped to the physical components of an ESD gun, facilitating its modification to reproduce other gun stresses, such as ISO 10605 stress. The model has successfully been used to analyze unexpected effects during ISO 10605 testing, and to predict changes in stress current caused by changes in the IEC testing environment.

4.8 – Figures and Tables

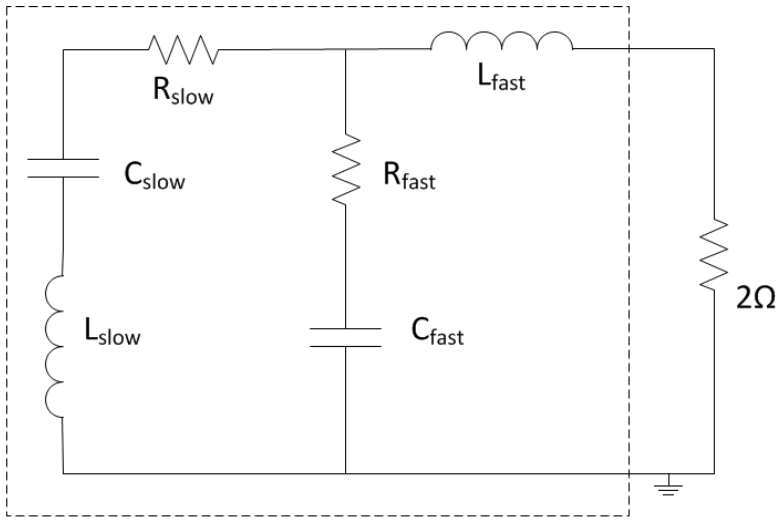


Figure 4.1: Circuit-level model of an ESD gun discharging into a 2 Ω test load.

Table 4.1: Component values to simulate an IEC 61000-4-2 waveform representing the nominal behavior and the upper and lower limits of the specification.

	Nominal	**Upper Limit**	**Lower Limit**
$\mathbf{R_{fast}}$	202.81 Ω	174.1 Ω	242.28 Ω
$\mathbf{L_{fast}}$	131.83 nH	84.88 nH	190.19 nH
$\mathbf{C_{fast}}$	12.82 pF	11.2 pF	12.96 pF
$\mathbf{R_{slow}}$	363.97 Ω	264.6 Ω	485 Ω
$\mathbf{L_{slow}}$	3 μH	3 μH	3 μH
$\mathbf{C_{slow}}$	136 pF	156.8 pF	102.06 pF

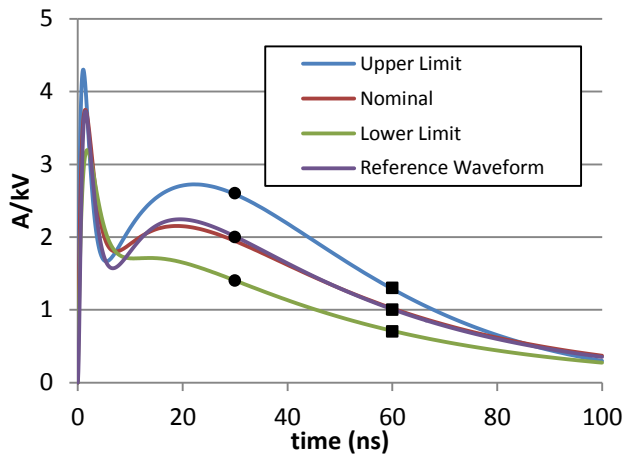


Figure 4.2: Simulated I_{DUT}, long timescale.

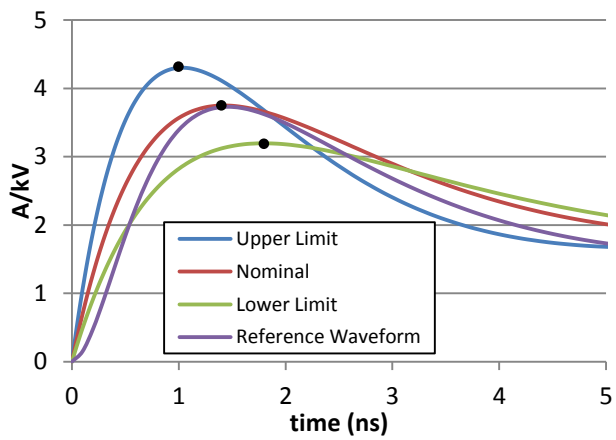


Figure 4.3: Simulated I_{DUT}, short timescale.

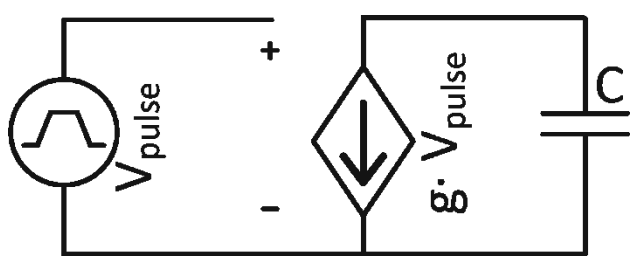


Figure 4.4: Circuit used to set initial conditions in ESD gun for repeated strikes. The shape of the pulse and g are set so that the capacitor is charged to the precharge voltage after the pulse. For example, V_{pulse} may be set to a trapezoidal pulse with 500 fs rise/fall times and 500 fs duration, and setting g = -C · 1S/pF. In this case, the capacitor will be charged to the amplitude of V_{pulse} after the pulse subsides.

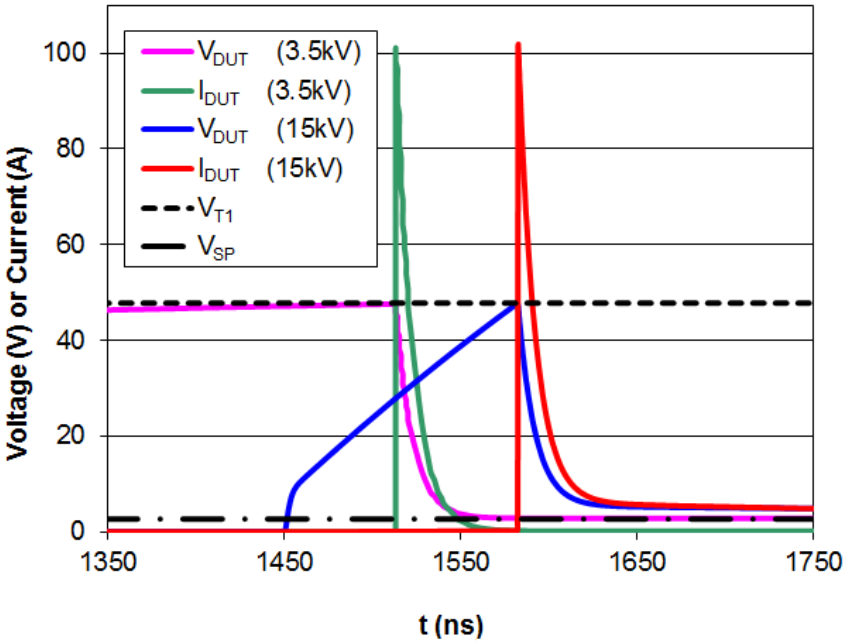


Figure 4.5: Simulated DUT behavior under 3.5 kV and 15 kV ISO 10605 stress. The 15 kV stress is delayed to begin at 1450 ns so snapback occurs at a similar time in both simulations.

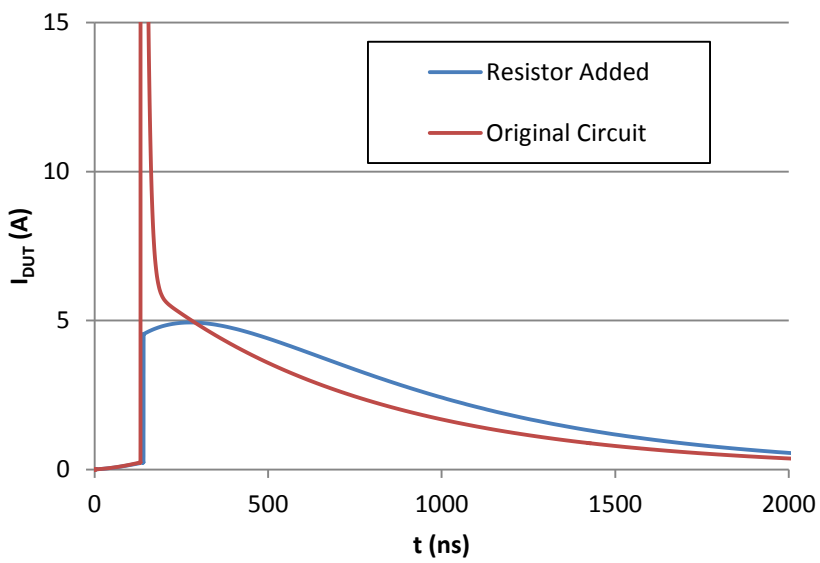


Figure 4.6: Simulated I_{DUT} for the original circuit and with a 10 Ω resistor added in series with the filter capacitor. The original circuit has a peak current of 100 A.

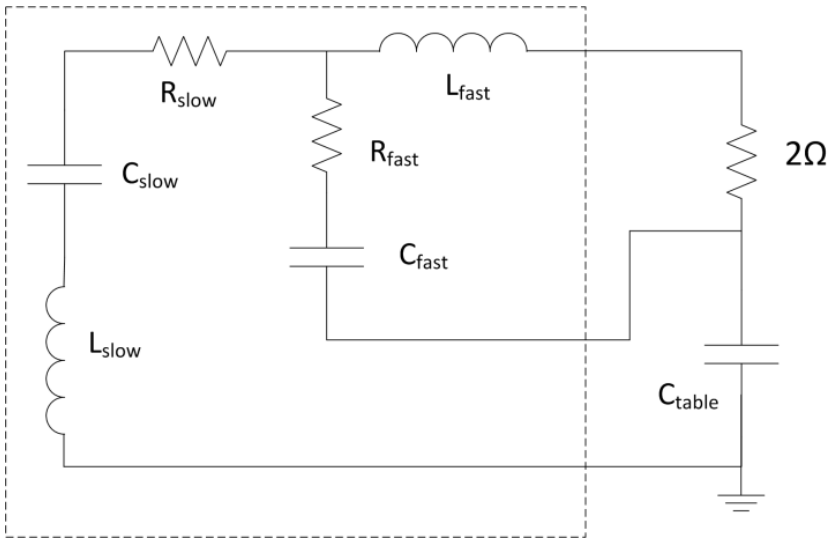


Figure 4.7: Simulation model for determining effect of C_{table} on I_{DUT}. Component values for the ESD gun model are taken from Table 4.1's Nominal column.

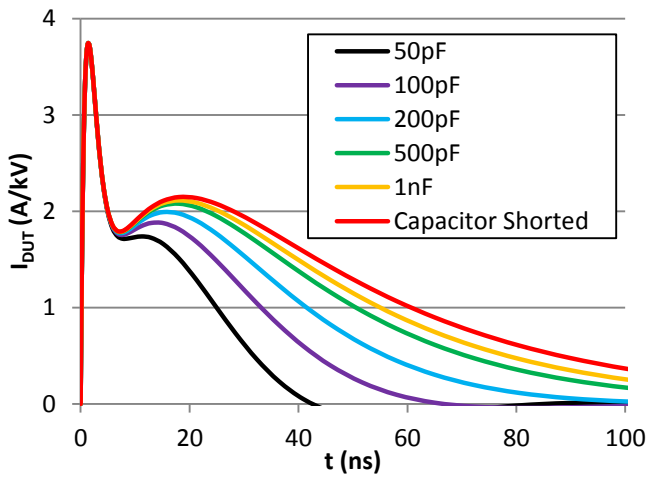


Figure 4.8: Simulation current through the DUT from the circuit in Figure 4.7. Legend values correspond to the values of C_{table} for each waveform.

Chapter 5 – Rail Clamp Analysis and Design

5.1 – Introduction

Active rail clamp based ESD protection [32], illustrated in Figure 5.1, is a common protection scheme. However, designing an active rail clamp circuit for power-on ESD (e.g., system-level ESD) protection is significantly more challenging than designing for component-level ESD. A clamp used for power-on ESD typically must pass all the requirements for component-level ESD but, furthermore, a clamp used for power-on ESD must also be able to shunt current between the supply rails without disturbing the supply. The meet this requirement, power-on ESD capable rail clamp designs operate as voltage regulators of last resort [33]. As with any voltage regulator, a feedback loop is used to control the output supply voltage; however, careful design is required to ensure that the circuit is both fast enough to regulate the supply during an ESD event and stable enough so that it does not interfere with functional circuitry on the chip.

This chapter provides a theoretical analysis of rail clamp circuits. Section 5.2 presents a small signal model of each amplifier stage in a trigger circuit. Section 5.3 shows how to combine the models for each stage, giving a model of the entire rail clamp circuit. Section 5.4 leverages the model to explore how the stability of rail clamp circuits is affected by on-chip and on-board components. Section 5.5 presents simulation and measurement data that support the preceding analysis. Section 5.6 derives how the amplifier stages in the trigger circuit affect the quasi-DC I-V characteristics of entire clamp circuit. The goal of this chapter is to provide a comprehensive guide as to how the rail clamp circuit design affects both its clamping performance and the stability of the power supply.

5.2 – Model of a Single Trigger Stage

Figure 5.2 shows the small-signal model of I1 and M0 from Figure 5.1. During power-on ESD, time-varying signals appear at nodes V_1, V_0 and V_{DD}. If V_{DD} is treated as an AC ground, the NMOS and PMOS in I1 each forms a common-source amplifier with its input at V_1 and output at V_0. Conversely, if V_1 is taken to be an AC ground, the PMOS forms a common-gate amplifier with its input at V_{DD} and output at V_0. C_{DG1} bridges from the input (V_1) to the output (V_0) of the common-source amplifier and complicates the analysis of the circuit. Furthermore, Miller's theorem [34] cannot be utilized to construct an equivalent schematic without the bridging impedance, because V_{DD} cannot be treated as an AC ground, even when the V_{DD}-V_{SS} decoupling capacitance is considered. An alternate method of decoupling the input and output must be derived.

Figure 5.3(a) is a generic representation of the circuit we wish to simplify by isolating the input, node 2, from the output, node 3. If one assumes that the load applied at node 3 is either included in Y_P and Y_N or is negligible ($i_3 = 0$), the desired transformation can be effected by removing Y_M and placing admittances at the input and output to emulate its effects. The specific modifications needed are determined by the KCL equations at the input and output nodes. At the output, node 3, application of KCL yields:

$$0 = g_{mp}(V_1 - V_2) - g_{mn}V_2 + Y_P(V_1 - V_3) - Y_N V_3 + Y_M(V_2 - V_3). \tag{5.1}$$

Nodal analysis of the transformed circuit must yield the exact same KCL equation at its output node. This is achieved through the following transformations. Y_M is removed, g_{mn} is replaced with g'_{mn} and Y_N is replaced with Y'_N such that

$$g'_{mn} = g_{mn} - Y_M \tag{5.2}$$

$$Y_N' = Y_N + Y_M. \tag{5.3}$$

To solve the KCL equation at the input, node 2, the current through Y_M must first be calculated, i.e. V_3 must be known. Using the earlier stated assumption that $i_3 = 0$, the voltage V_3 can solved for in terms of V_1 and V_2 using (5.1):

$$V_3 = \frac{V_1(g_{mp}+Y_P)+V_2(-g_{mn}-g_{mp}+Y_M)}{Y_N+Y_P+Y_M}. \tag{5.4}$$

Thus, when $i_3 = 0$, KCL at node 2 can be written as

$$i_2 = Y_B V_2 + Y_T(V_2 - V_1), \tag{5.5}$$

where

$$Y_B = Y_M\left(\frac{g_{mn} + Y_N}{Y_N + Y_P + Y_M}\right) \tag{5.6}$$

and

$$Y_T = Y_M\left(\frac{g_{mp} + Y_P}{Y_N + Y_P + Y_M}\right). \tag{5.7}$$

This indicates that the transformed input network should have an admittance Y_B from node 2 to ground and an admittance Y_T from node 2 to node 1. Finally, to cancel the effect of Y_T on the current flow into node 1, two elements of absolute value Y_T are also added between node 1 and ground, as shown in Figure 5.3(b). The circuits in Figure 5.3(a) and Figure 5.3(b) are equivalent; they have identical KCL equations at all nodes, as long as the assumption $i_3 = 0$ holds. But, the circuit shown in Figure 5.3(b) is easier to analyze, because the input node is isolated from the output node.

When the elements of Figure 5.3(a) are associated with specific circuit elements from the schematic of Figure 5.2, it is found that some of the terms in (5.2), (5.6), and (5.7) complicate

hand analysis by adding high-frequency zeroes. This motivates the use of the following approximations:

$$g'_{mn} \approx g_{mn} \tag{5.8}$$

$$Y_B \approx Y_M g_{mn}(r_{ON}||r_{OP}) \tag{5.9}$$

$$Y_T \approx Y_M g_{mp}(r_{ON}||r_{OP}). \tag{5.10}$$

Each of these approximations results from neglecting the zero, which occurs at a high frequency because g_m is large. When the high-frequency zeroes in (5.6) and (5.7) are neglected, their admittances reduce to that of a series RC circuit, e.g. evaluating and simplifying (5.6) gives

$$Y_B = \frac{sC_M\left(g_{mn} + \frac{1}{r_{on}}\right)(r_{on}||r_{op})}{1 + s(r_{on}||r_{op})(C_{on} + C_{op} + C_M)} = \frac{sC}{1 + sRC}. \tag{5.11}$$

The expressions in (5.9) and (5.10) neglect the effect of R in (5.11); in this case, the dominant pole at the input node is unchanged when combined with the parallel RC output impedance of the previous stage [35].

Each stage of the trigger circuit can now be represented by the simplified schematic shown in Figure 5.4. The elements corresponding to Y_T and Y_B are not drawn; they are folded into the output impedance of the previous stage to ensure the assumptions required for the transformation remain valid. The Y_T admittances between node 1 and ground are also neglected, since the current sunk by the trigger circuit is much smaller than the current sunk by the clamp. For the first stage, Y_T, Y_B and the input capacitances may be combined with the RC timer components; these components will act as a capacitive voltage divider over the frequency range to which the clamp is intended to respond. C_{ON} and C_{OP} represent the total capacitive load between V_O and V_{SS} or V_{DD}, respectively. C_{ON} and C_{OP} each consist of two components: (i) the

driver's output capacitance (i.e., Y'_N and Y_P from Figure 5.3(b)), (ii) the load capacitance of the next stage or the clamp (i.e. C_{GN}, C_{GP}, Y_T, and Y_B, as applicable). Applying KCL at the output yields

$$V_o = \frac{-(g_{mN} + g_{mP})V_i + \left(g_{mP} + \frac{1}{r_{OP}} + sC_{OP}\right)V_{DD}}{\frac{1}{r_{ON}} + \frac{1}{r_{OP}} + s(C_{ON} + C_{OP})}. \tag{5.12}$$

The zero due to C_{OP} may be neglected because it typically occurs at a frequency much higher than the pole, resulting in

$$V_o = \frac{-AV_i + A_G V_{DD}}{1 - \frac{s}{p}}, \tag{5.13}$$

$$A = (g_{mN} + g_{mP})(r_{ON}||r_{OP}), \tag{5.14}$$

$$A_G = \left(g_{mP} + \frac{1}{r_{OP}}\right)(r_{ON}||r_{OP}), \tag{5.15}$$

$$p = -\frac{1}{(r_{ON}||r_{OP})(C_{ON} + C_{OP})}. \tag{5.16}$$

5.3 – Rail Clamp Circuit Model

Making use of (5.13)-(5.16), a schematic representation of an active clamp containing a 3-stage trigger circuit is constructed as shown in Figure 5.5(a), and the 1-stage version is shown in Figure 5.5(b). The trigger circuit is represented by a signal flow graph and the active clamp is represented by g_{m0}. On the time scale of interest, the input of the first stage is tied to AC ground by the timing capacitor and is thus not shown in the figure. Figure 5.5(a) can adapted to the case of a 2-stage trigger circuit by replacing the A_{G3} block with a short to V_{DD}.

These signal flow graphs neglect the effect of the capacitive voltage divider at the input of the first stage (which will have only a small effect on stability). If desired, the signal flow graphs can be modified to account for this. The output of each stage is modeled as the sum of two linear amplifiers: A (input tied to the output of the previous stage), and A_G (input tied to V_{DD}). For the first stage, the input is $k \cdot V_{DD}$, where k is a constant between 0 and 1 to account for the capacitive voltage divider.

Applying KCL at node V_{DD} for either circuit of Figure 5.5 yields

$$I_{ESD} = g_{m0} H(s) \cdot V_{DD}, \quad H(s) = \frac{V_0(s)}{V_{DD}(s)}. \tag{5.17}$$

The terms in (5.17) may be rearranged to obtain an expression for the input impedance of the clamp:

$$Z_{in} = \frac{V_{DD}}{I_{ESD}} = \frac{1}{g_{m0} H(s)}. \tag{5.18}$$

Evaluating Z_{in} for the case of the clamp with a 1-stage trigger circuit gives

$$Z_{in1} = \frac{1}{G_1}\left(1 + \frac{s}{(-p)}\right), \quad G_1 = g_{m0} A_{G1}. \tag{5.19}$$

The DC value of (5.19) represents the on-conductance of the clamp during power-on stress; it is the conductance of the clamp during power-off ESD multiplied by the gain of the trigger circuit; thus the on-resistance of the clamp during power-on stress should be smaller than during power-off stress, until the ouput of a trigger circuit stage saturates, thereby reducing the gain (this behavior is discussed more in depth in Section 5.5). Rail clamp circuits with multi-stage trigger circuits similarly show a reduced on-resistance during power-on ESD, although the expression for gain is more complicated, as will be shown below.

When the number of trigger circuit stages is increased, the number of terms in the input impedance expression also increases. For example, the input impedance of a clamp with a 2-stage trigger circuit is

$$Z_{in2} = Z_{in1} || \left(\frac{1}{G_2} \left(1 - \left(\frac{1}{p_1} + \frac{1}{p_2} \right) s + \frac{s^2}{p_1 p_2} \right) \right), \quad G_2 = g_{m0} A_1 (A_2 - A_{G2}). \tag{5.20}$$

Z_{in2} has a negative resistance component that is proportional to ω^2; this allows for the possibility of unstable oscillation. Even a clamp with a 1-stage trigger circuit can show significant ringing when the chip is integrated into a larger system.

5.4 – Design for Power Integrity

The active clamp small-signal model may be combined with a board-level model of a power distribution network [36] to ascertain the overall stability of the system during power-on ESD. The resulting schematic is shown in Figure 5.6, for the case that the ESD current is injected through the top diode. Figure 5.7 shows a plot of the total admittance from chip-level V_{DD} to V_{SS}, Y_{DD}, under both normal operating conditions and when a 2-stage rail clamp circuit is triggered on. Y_{clamp} (i.e, $1/Z_{in}$ of the clamp, given by (5.20)) is also plotted in the figure for comparison purposes. To ensure that the results are realistic, a small parasitic resistance was included in each element.

To maintain a well-regulated supply, the total admittance at V_{DD} must be large and have a positive real part. Resonant frequencies, identifiable by $\mathrm{Im}\{Y_{DD}=0\}$, are designed to occur where there is little spectral content, e.g., away from f_{CLK} and its harmonics. Figure 5.7(b) clearly demonstrates that activation of the clamp will shift the resonant frequency of the supply away from its designed-for value. When the clamp is on, the resonance occurs between Y_{clamp} and C_{chip}, instead of L_{system} and C_{chip} as in normal operation. Given the broadband nature of ESD, it is

important that $Re\{Y_{DD}\}$ be above zero at the new resonant frequency so as to provide damping. Figure 5.7(a) shows that this requirement is met for the example under consideration; the series resistance of C_{chip} adds a large positive conductance to the system which cancels the negative value of $Re\{Y_{clamp}\}$, improving the stability of the circuit.

Rail clamp instability due to a negative $Re\{Y_{DD}\}$ or to an insufficiently damped resonance between Y_{clamp} and C_{chip} would result in the active clamp switching on and off repeatedly, producing large power/ground bounce. These hazards can be mitigated by careful trigger circuit design. The most common criterion for ensuring stability is that the loop gain of a circuit falls below 1 before the phase shift through the circuit exceeds 180°. Practically, this means that the ratio of the second and dominant (first) poles should be larger than the (linear scale) gain. In a rail clamp circuit, the loop gain is

$$A_{loop}(s) = H(s) \cdot g_{m0}(r_{o0}||Z_{DD}), \tag{5.21}$$

where r_{o0} represents the output resistance of the rail clamp and Z_{DD} represents that supply impedance seen by the clamp. Generally, r_{o0} and the supply decoupling capacitance will form a pole associated with the V_{DD} node. In Figure 5.7, this pole is the dominant pole. The dominant pole is not immediately visible in Figure 5.7; however, it can be determined from Figure 5.7 and (5.21). Y_{clamp} corresponds to $H(s) \cdot g_{m0}$ and Y_{DD} under normal operation corresponds to Z_{DD}. The zero in $Im\{Y_{DD}\}$ at about 150 MHz indicates a pole in Z_{DD}, which is the dominant pole in the loop transfer function. One method of improving stability is to increase the ratio of the second and dominant poles. If the dominant pole is on V_{DD}, this means using a faster (larger) trigger circuit or adding more decoupling capacitance. In contrast, if the dominant pole occurs in the trigger circuit, possible remedies include reducing the supply decoupling capacitance, speeding up stages with non-dominant output poles, or slowing down the stage with the dominant output

pole (thus slowing down the whole circuit). Alternatively, stability can be improved by decreasing the loop gain by reducing the gain through the trigger circuit. Gain can be reduced by using fewer stages and by decreasing the output resistance of each stage with a non-dominant output pole. (If the output resistance associated with the dominant pole is decreased, the dominant pole moves closer to the non-dominant poles, and stability is unchanged.) However, as will be addressed later, reducing the gain too much can negatively affect the DC behavior of the clamp.

5.5 – Clamp Analysis Application

Three 3.3 V rail clamp circuits are compared; all are designed in 130 nm CMOS technology. The trigger circuit is varied between the three circuits, while the active clamp is a fixed 4000 μm wide. Design 1 uses the topology shown in Figure 5.1. The trigger circuit transistors all have the minimum gate length, and the channel widths are given by [W_{N1}, W_{P1}, W_{N2}, W_{P2}, W_{N3}, W_{P3}] = [100, 200, 24, 48, 2, 12] μm. The first inverter, I3, uses a relatively large PMOS to tune the inverter's switching threshold so that the clamp activates before V_{DD} becomes too large. Design 2 is shown in Figure 5.8. The diode connected PMOS of the first stage limits the gain of the circuit, and also reduces the switching threshold of the first stage so that the clamp triggers with a smaller increase in supply voltage above its nominal value V_{nom}. Using two stages instead of three limits the gain and reduces the phase shift through the trigger circuit. Both changes improve stability. Design 3 is identical to the Design 2 except that all the transistors have double the width, reducing the delay. Because the dominant pole for this circuit is on V_{DD}, this speed-up improves stability. Simulated I-V curves for the three clamps are shown in Figure 5.9.

For power integrity analysis, it is desired to extract the impedance of the clamp (such as shown in Figure 5.7) using AC analysis. However, the clamp's operating point cannot be obtained using conventional DC analysis since the clamp will be turned off at DC, due to the timing capacitor. Instead, the clamp operating point is obtained by replacing the capacitor with a voltage source whose output is equivalent to that of the capacitor on the timescale of interest, given by

$$V_{cap} = V_{nom} + k(V_{DD} - V_{nom}), \tag{5.22}$$

where V_{nom} is the nominal supply voltage, V_{DD} is the instantaneous supply voltage, and k is a positive number less than 1 that is used to account for the fact that there may be a capacitive voltage divider between the timing capacitor and the input capacitance of the first inverter. The bias point of the clamp is then determined by forcing DC current equal to I_{ESD} onto V_{DD}. Once the bias point is determined, AC analysis can be performed.

When the active clamp circuits are biased at a quasi-static current of 2.5 A (about half of I_{t2}), they have admittances as shown in Figure 5.10. It is evident that Design 1 has much higher gain and much lower bandwidth than the other designs. Furthermore, it has a larger peak negative admittance than the other designs, due to the additional phase shift caused by the extra stage, and is thus expected to have poor stability. Of the other two designs, Design 3 should perform slightly better due to the increased bandwidth of the trigger circuit.

Figure 5.11 shows the simulated voltage across each of the active clamps when it is combined with the power distribution network of Figure 5.7 and subjected to a long 2.5 A square current pulse with 1 ns rise time. As predicted, Design 3 shows the best transient response, followed by Design 2 and Design 1. After about 15 ns, L_{system} and C_{system} constitute the preferred current path and each rail clamp turns off. Design 2 is used on the test chip introduced in Chapter

2, and none of the logic failures observed during power-on TLP testing were attributed to power supply instability, suggesting that the small amount of ringing shown in Figure 5.11 is acceptable.

The pad ring of a chip design will typically contain several instances of the rail clamp. In such cases, the performance of the clamp may be slightly different than predicted by a single-clamp simulation, such as the preceding one. The previously described test chip has five instances of Design 2 in its pad ring, and the composite I-V curve is obtained through wafer-level TLP measurement; results are shown in Figure 5.12 for both the power on and off cases. For the power-on measurement, a DC bias is applied by the pulse source; unlike in Figure 5.11, L_{system} is not present so the clamps sink the entire current pulse for its full duration. As predicted in Section 5.3, the clamp on-resistance is lower when the chip is powered. During power-on ESD, clamps may show different behavior based on their distance from the zap point. The gate voltage of clamps near the zap point may reach V_{DD} (saturating the clamp circuit) and the clamp will shunt as much current as possible. Clamp circuits far away from the zap point act as voltage regulators [33] and do not fully turn on; if they did, the local supply voltage would fall below the nominal supply voltage. This behavior can be observed in Figure 5.12; at about 9 A, the two clamp circuits nearest to the zap point saturate and the powered-on I-V curve's slope changes.

The fact that each clamp may operate at a different point on its I-V curve suggests that a simulation model of the clamp(s) must include the power bus resistances. Moreover, to reproduce the measured I-V, the model must also capture the effect of the capacitive voltage divider between the timing capacitor and the input capacitance of the first inverter. In Figure 5.13, simulated and measured I-V curves under power-on conditions are compared. Two sets of pad ring simulation results are shown; in one simulation, only the bus resistance is included, and

in the other, bus resistance and the capacitive voltage divider are both modeled. The second simulation matches very well to the measurement results. This indicates that the capacitive voltage divider between the timing capacitor and the input of the first inverter increases the cut-in voltage of the clamp; not accounting for this effect will result in an overly optimistic simulation of the supply voltage clamping. This effect is especially pronounced for the design measured in Figure 5.13, because of the implementation of the timing capacitor. The capacitor is implemented as a PMOS with gate connected to VDDIO and the source/body/drain connected to the input of the first stage; thus, the input capacitance of the first stage is augmented by the N-well/substrate capacitance of the timing capacitor. This parasitic capacitance can be removed by swapping the two terminals of the timing capacitor. For comparison purposes, the idealized I-V of a single clamp (Design 2) is also plotted in the figure. Because the on-resistance of the clamp is near zero, it is evident that the actual R_{on} is determined by the metal resistance, not the trigger circuit.

5.6 – Clamp DC Analysis

The cut-in voltage of a rail clamp circuit, i.e. the voltage at which it begins to conduct, is one of the key metrics of an active clamp circuit's performance; if the cut-in voltage is too high, the circuit will not be able to limit the supply voltage to a safe level, and thus prevent damage to the chip.

To calculate the cut-in voltage of a rail clamp circuit, each inverter stage is represented as a linear amplifier that saturates when its output hits either supply rail. In the clamp's off-state, the inverter will have an input voltage of V_{in0} and an output voltage of V_{out0}; the inverter's output will begin to change once the input changes by a circuit-dependent voltage, V_X. This behavior can be represented as

$$(V_{out} - V_{out0}) = A_v[(V_{in} - V_{in0}) - V_X], \tag{5.23}$$

or more simply,

$$V'_{out} = A_v(V'_{in} - V_X). \tag{5.24}$$

Inverting (5.24) gives

$$V'_{in} = V_X + \frac{V'_{out}}{A_v}. \tag{5.25}$$

This generic representation of each stage can be used calculate the input voltage of a given stage required to cause the next stage to switch. For example, the clamp in Figure 5.1, M0 will begin to switch when the output of I1 is equal to M0's threshold voltage, V_{T0}. Thus, using (5.25), the rail clamp circuit will begin to turn on when

$$V_{in1} = V_{X1} + \frac{V_{T0}}{A_{v1}}. \tag{5.26}$$

By using (5.25) to refer the output of each stage to the input of the previous stage, the input at I3 required to turn on M0 can be written as

$$V'_{in3} = V_{X3} + \frac{V_{X2}}{A_{v3}} + \frac{V_{X1}}{A_{v3}A_{v2}} + \frac{V_{T0}}{A_{v3}A_{v2}A_{v1}}. \tag{5.27}$$

The capacitor connected to the first stage is made large enough so that its voltage will remain fixed during a typical ESD event, e.g. HBM and shorter duration ESD stresses; its voltage will be roughly equal to the nominal supply voltage. Thus, V_{in3} (the voltage drop across the resistor in Figure 5.1) represents the increase in supply voltage required to trigger the rail clamp circuit. Equation (5.27) can be generalized to provide an estimate for the cut-in voltage of a given clamp circuit; it is the sum of the switching thresholds of each inverter divided by the gain of all preceding stages. Because the gain in each stage is usually significantly larger than 1, the

switching threshold of the whole circuit is dominated by the first stage; for the circuit of Figure 5.1, this is I3.

In [37], it was observed that traditional active clamp circuits, i.e. those that use only CMOS inverters in the trigger circuit, trigger at significantly higher voltages when the part is powered on (approximately double the supply voltage) than when it is powered off (approximately two threshold voltages), and thus provide poor clamping during power-on ESD. The preceding analysis can be used to explain why this is so. A CMOS inverter will typically have a switching threshold near half the supply voltage ($V_X \approx ½V_{DD}$). To estimate the switching threshold of the rail clamp circuit in Figure 5.1, this value of the switching threshold is plugged into (5.27), yielding

$$V'_{in3} = V_{DD} - V_{DD0} = V_{X3} \approx \frac{V_{DD}}{2}, \tag{5.28}$$

where V_{DD0} indicates the supply voltage prior to the clamp firing. V_{in3}' is the effective input to the first stage, I3, and is equal to the increase in supply voltage over its nominal value. Solving (5.28) for V_{DD} indicates the clamp will fire at approximately $2 \cdot V_{DD0}$. In many cases, the clamp will be triggered into snapback at a lower voltage than is required for the trigger circuit to fire. To address this problem, active clamp designs incorporating non-CMOS inverters have been used to achieve a lower switching threshold, such as designs in [33] and Section 5.5.

Based on the above discussion, a designer may wish to use low gain in the later stages of the trigger circuit; high gain negatively impacts stability and has little effect on the cut-in voltage. However, lowering the gain of the later stages in a trigger circuit can negatively impact other aspects of the circuit performance. Specifically, low gain circuits usually have reduced output swing. Consider a PMOS common-source amplifier with resistive load used as the last stage of a trigger circuit. The gain can be reduced by shrinking the PMOS relative to the resistive

load; however, doing so means that the PMOS cannot pull its drain as close to V_{DD}. In the context of a trigger circuit, this means a reduced gate voltage is applied to the clamp, potentially requiring the clamp area to be increased. Thus, in some designs, a tradeoff will exist between achieving high gate bias (requiring high gain) and stability (requiring low gain).

5.7 – Conclusion

The analysis presented in this chapter demonstrates the tradeoffs inherent in trigger circuit design for power-on ESD protection. Specifically: (a) higher gain at the first trigger circuit stage reduces the cut-in voltage, thereby providing improved voltage clamping, (b) higher gain at later trigger circuit stages increases the maximum gate voltage that can be applied to the clamp, favorably increasing the clamp current per unit area, and (c) high gain can lead to instability. To improve stability, a dominant pole must be created; in some cases, this may increase the clamp response time. A long response time will reduce clamping during fast transients.

5.8 – Figures

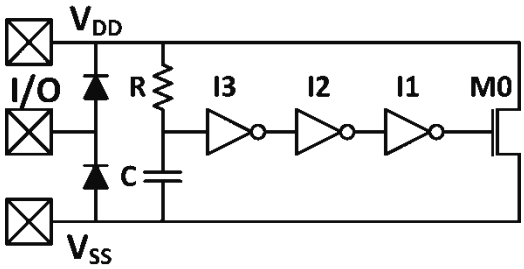


Figure 5.1: Dual-diode/active clamp ESD protection scheme [32]. Trigger circuit may contain 1, 2 or 3 inverters. If the number is 2, the R and C are swapped.

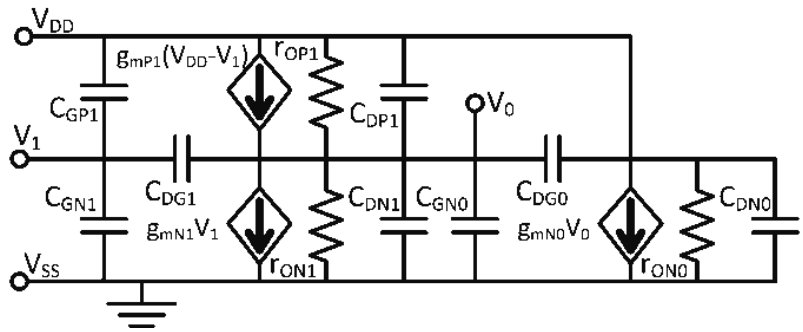
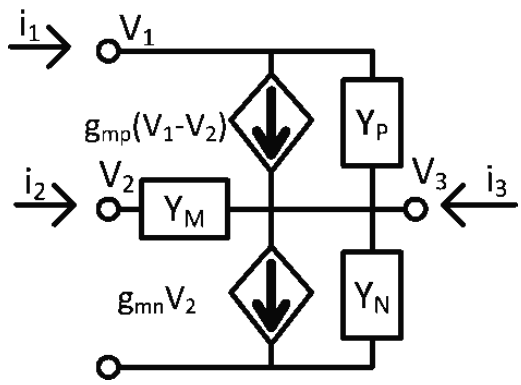
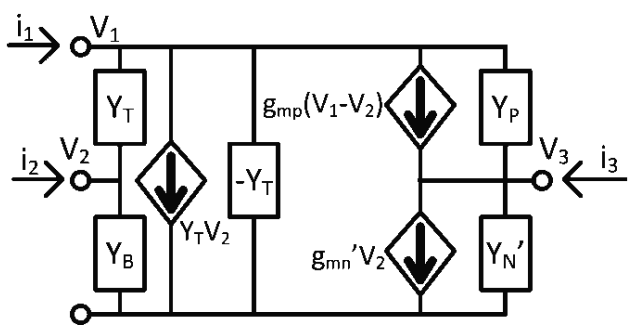


Figure 5.2: Small-signal model of M0 and I1.



(a)



(b)

Figure 5.3: Two equivalent networks. Transforming from (a) to (b) is roughly analogous to applying Miller's theorem to this three-port network.

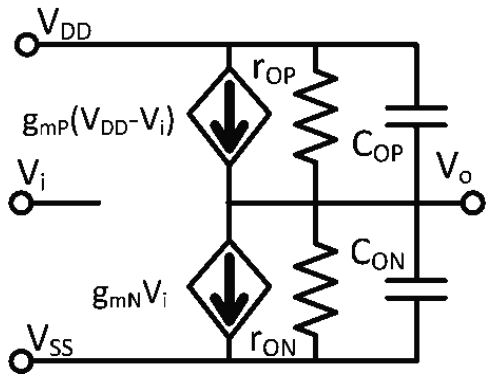
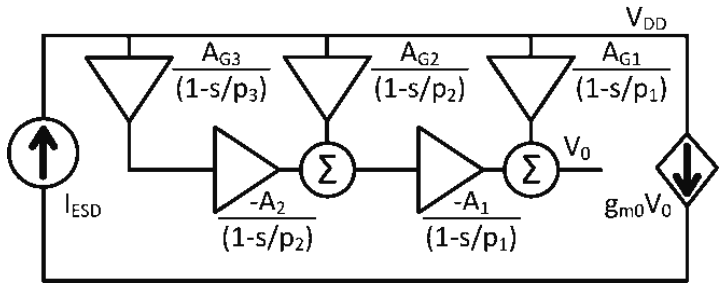
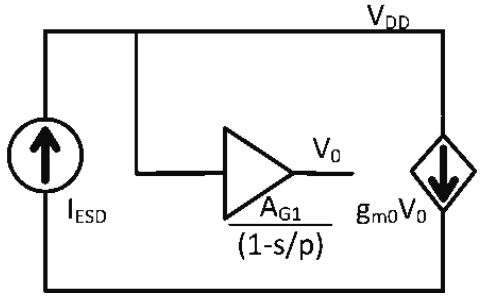


Figure 5.4: Simplified schematic of one stage in a trigger circuit.



(a)



(b)

Figure 5.5: Simplified models of (a) 3-stage and (b) 1-stage rail clamp circuits.

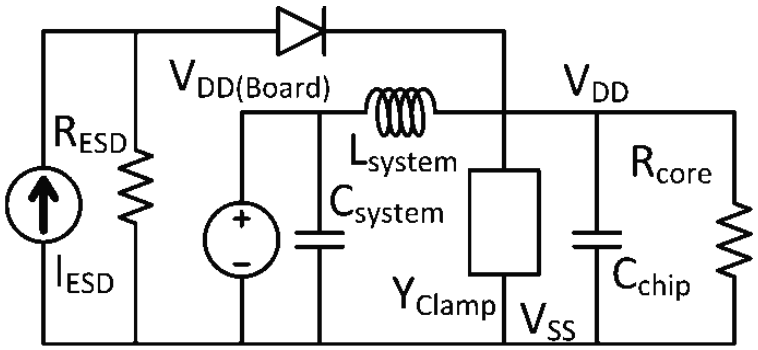
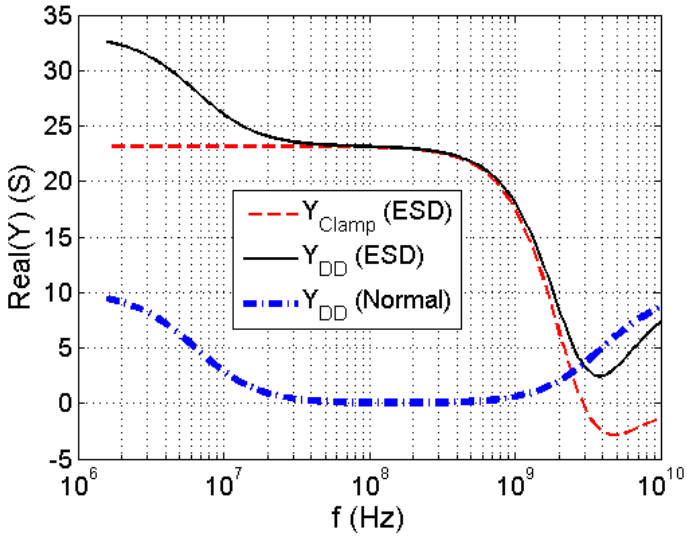
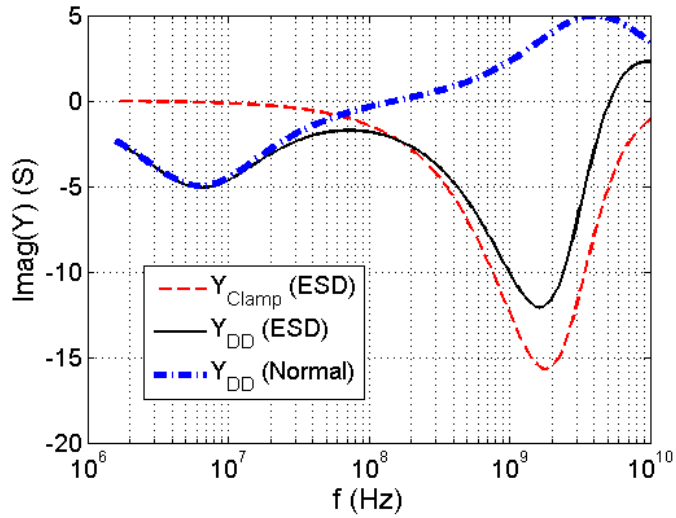


Figure 5.6: Schematic representation of important components during a positive ESD zap to an I/O pin protected by dual diodes. On- and off-chip decoupling capacitors are represented by C_{chip} and C_{system}, respectively. L_{system} represents trace and package inductance. For simplicity, the trace from the ESD source to the I/O pin is ignored, and the ESD source is assumed to have a pure real output impedance. The core circuitry is represented as a resistance to account for variations in supply current with supply voltage. The forward biased diode is treated as a short for stability analysis, so R_{ESD} and R_{Core} are in parallel.



(a)



(b)

Figure 5.7: Admittances between V_{DD} and V_{SS} for the circuit in Figure 5.6 with [L_{system}, C_{chip}, C_{system}, $R_{core}||R_{ESD}$] = [2.5 nH, 400 pF, ∞, 200 Ω]. Y_{clamp} is evaluated using (5.20) with [g_0, A_1, A_{G1}, p_1, A_2, A_{G2}, p_2] set to [1 S, 10, 5, 2π800 MHz, 5, 0.01, 2π4 GHz]. Series resistances are added to L_{system}, C_{chip}, and Y_{clamp} (100 mΩ, 100 mΩ, and 25 mΩ respectively). (a) Real and (b) imaginary admittances, under ESD and normal operating conditions.

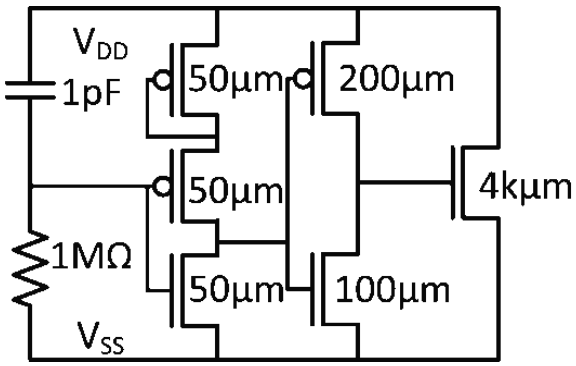


Figure 5.8: New trigger circuit design. The diode-connected PMOS limits the gain of the first stage and adjusts the switching threshold.

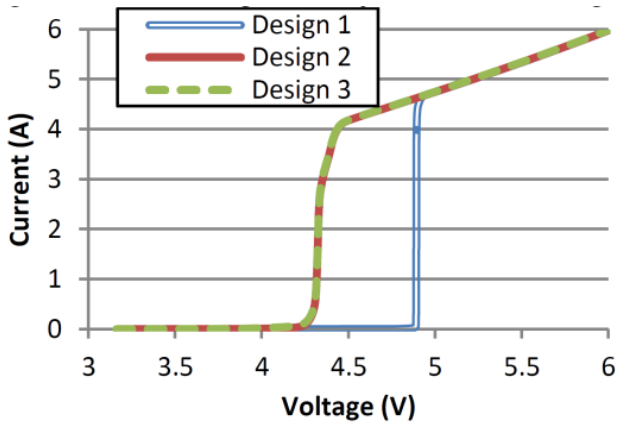


Figure 5.9: Simulated, 100 ns TLP I-V of the three rail clamp designs with the power on (V_{DD} = 3.3 V). Results are shown for R_{bus} = 0 Ω. I-V curves for Designs 2 and 3 are coincident, and all three designs have identical I-V above ~4.5 A).

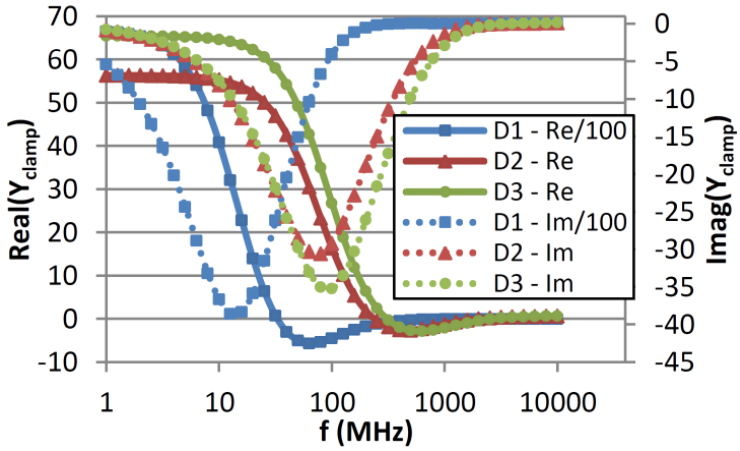


Figure 5.10: Simulated Y_{clamp} at 2.5 A for rail clamp Designs 1 through 3. For Design 1, Y/100 is plotted instead of Y.

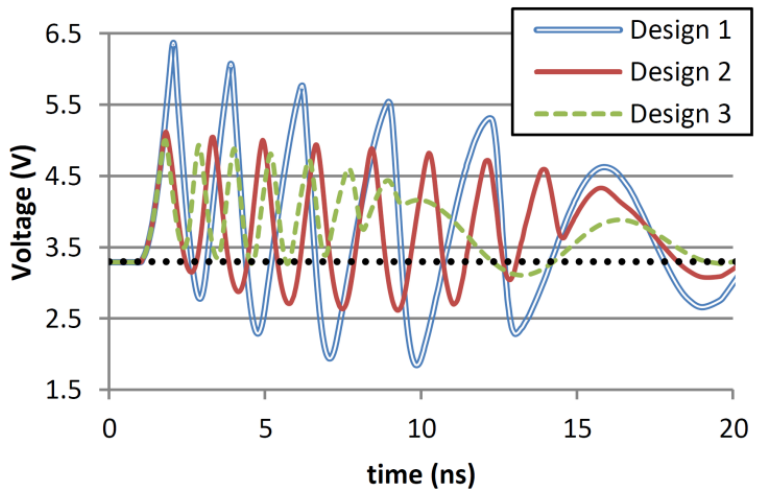


Figure 5.11: Transient response of each rail clamp to a 2.5 A pulse with 1 ns rise time and 50 ns width. The nominal supply voltage is also shown. The ringing on the supply occurs between the clamp (which appears inductive) and C_{chip}. After about 15 ns, each rail clamp turns off, and L_{system} and C_{system} sink the current pulse and ringing will occur between C_{chip} and L_{system}. Because L_{system} is larger than the inductance of the clamp, the ringing frequency on the supply will decrease after this transition occurs. This shift is visible in each of the waveforms above.

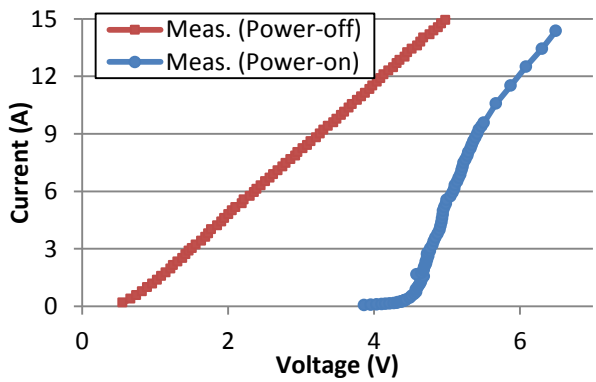


Figure 5.12: TLP curves of the pad ring during power-off and power-on TLP. On-resistance is lower the latter measurement.

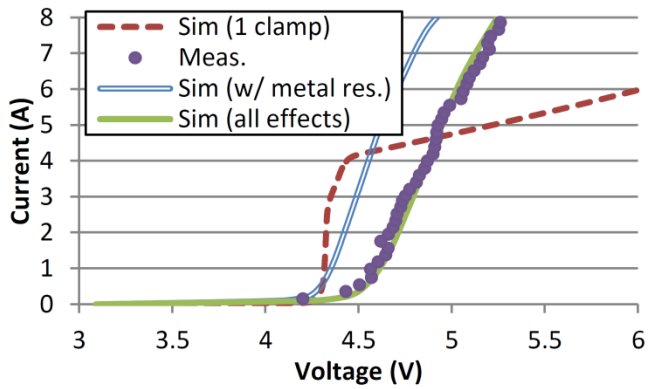


Figure 5.13: Measured and simulated TLP I-V curves of pad ring containing several instances of the rail clamp show in Figure 5.8. Simulations that include bus resistance, and bus resistance and capacitive coupling (using (5.22)) are shown. For reference, the I-V of one clamp circuit without either effect is also plotted.

Chapter 6 – ESD-Induced Ground Bounce and Related Problems

6.1 – Introduction

This chapter describes a newly identified threat to power integrity during power-on ESD. During an ESD event (which has a very high di/dt), there can be unusually large ground bounce in the board/package inductances. One consequence is that the ESD current may not return directly to the board ground through the expected current path. If this occurs, power domains may be briefly powered down, disrupting logic functionality. Another consequence is the forward biasing of parasitic diodes that lie between the P-substrate and various N-wells. The minority carrier injection from the P-substrate/N-well diode poses a global latch-up risk. It will also be shown that activation of a parasitic diode can discharge the capacitor inside an active clamp's RC timer circuit, leading to inadvertent triggering of the active ESD clamp and perturbation of the power distribution network. This chapter focuses on inductive ground bounce; however, conceptually, resistive ground bounce could cause similar problems.

This chapter explores two ways that ground bounce can affect the on-chip supply. The first is presented as a case study in Section 6.2. In this case study, an IO zap on one supply powered down an adjacent supply; this effect has been replicated in both simulation and measurement. Section 6.3 presents a theoretical analysis of a similar phenomenon where an IO zap powers down the zapped supply. Both of these effects could cause an IC to malfunction.

6.2 – Powering Down a Supply Domain Adjacent to the Zapped Domain – A Case Study

6.2.1 – Mechanism

The time-derivative of the on-chip ESD current can be very large, and gives very large ground bounce due to parasitic inductance in the power distribution network, e.g. bond wires or

an off-chip decoupling capacitor's equivalent series inductance. For the case of a chip that has multiple power supply domains, the large impedance presented by the inductive elements will cause the fast rise time ESD current to seek a large number of parallel paths to ground. An example is shown in Figure 6.1; a positive ESD current injected into an IO pin can leave the chip on any supply domain. First, the current will elevate V_{DDIO} and the active clamp will shunt current to V_{SSIO}. Significant ground bounce will occur on V_{SSIO}; consider that a 10 A/ns rising edge would cause a 20 V drop across a 2 nH inductance. The bounce on V_{SSIO} will force current onto V_{SS} through the anti-parallel diodes, resulting in ground bounce on V_{SS}. If the ground bounce on V_{SS} is severe enough, V_{SS} can rise above V_{DD} [38], [39]. Although such an event will only last for about one nanosecond (i.e. the time during which the current waveform has a large amplitude time derivative), it may still cause on-chip circuits to malfunction.

If V_{SS} rises above V_{DD} as outlined above, the active clamp may be triggered on once the supply returns to its normal polarity; this depends on the trigger circuit implementation. Figure 6.2 illustrates an active clamp with a 2-stage trigger circuit; often, the timing capacitor is an accumulation-mode MOS capacitor implemented as an NMOS in an N-well. A large parasitic diode is associated with the accumulation-mode capacitor and this diode will discharge the timing capacitor if V_{SS} exceeds V_{DD}. Before the ESD event, the voltage drop across the timing capacitor is V_{nom} (the nominal supply voltage), i.e., the node labeled V_{RC} is at a potential that is lower than that on the V_{DD} line by an amount equal to V_{nom}. During the ESD event, V_{SS} will not exceed V_{DD} by much more than a diode on-voltage, due to the action of the forward-biased ESD diode in the rail clamp circuit. This is sufficient to strongly forward-bias the parasitic diode and it will start to charge up the node V_{RC}. Once the voltage difference between V_{SS} and V_{RC} is reduced below the diode on-voltage, the rate of change slows. Thus, V_{RC} will be charged to

roughly the same potential as V_{DD} during the brief supply disruption. The timing capacitor will have been significantly discharged and, therefore, the active clamp will be turned on after V_{SS} falls back below V_{DD}.

6.2.2 – Demonstration in Simulation

The scenario outlined above is further investigated using circuit simulation. The simulation netlist describes the pad ring of the 130 nm CMOS test chip presented in Chapter 2. The test chip contains a 3.3 V IO supply domain, a 1.5 V core supply domain, and a small, 1.2 V domain ("V_{DDLU}") that is used to power some test circuits for a latchup study. Both V_{DD} and V_{DDIO} include approximately 400 pF of explicit decoupling capacitance. The chip-level ESD discharge network is designed as shown in Figure 6.1. The active rail clamps' trigger circuit designs are identical to that shown in Figure 5.8; the timing capacitor implementation is such that the parasitic diode shown in Figure 6.2 is present. The ESD protection devices at external pins were sized to survive 8 kV HBM to provide some protection against system-level ESD induced hard failure. The chips are assembled in a QFN80 package, with an estimated bond wire inductance of 5 nH. Each primary supply (V_{DDIO}, V_{SSIO}, V_{DD}, and V_{SS}) connects to five package pins. V_{DDLU}, which is referenced to V_{SS}, is connected to two package pins.

Circuit simulation is performed for the case that an ESD gun is discharged into one of the test chip's dual-diode protected IO pins; the ESD gun is represented by the model given in Chapter 4 and its ground is connected to the board ground. The other IOs are left floating. Each supply pin is set to its nominal voltage by an ideal voltage source, which represents the large board-level decoupling capacitance. PDK models are used for the MOS devices in the trigger circuits and for the active clamps; the PDK models for the output driver devices are augmented with a piecewise linear snapback model, implemented in Verilog-A and based on TLP data. The

diodes are represented using the model presented in Section 3.2.3; parameter extraction was performed using VFTLP data. Package resistance, self-inductance (i.e. inductance created by the loop formed between the bond wire and board ground), and self-capacitance (i.e. between the bond wire and board ground) are included in the netlist, based on data provided by the vendor; mutual inductances and capacitances are neglected.

The results of a simulated +4 kV zap are shown in Figure 6.3. In Figure 6.3(a), the voltage at each on-chip supply and the zapped pad are plotted with respect to board ground; a large ground bounce is observed. In Figure 6.3(b), the potential difference between each positive supply and its on-chip ground reference is plotted; similarly, the potential difference between the zapped pin and its ground is plotted. These results show that the V_{DDIO} domain supply is maintained at an elevated, but safe, voltage throughout the event. However, the V_{DD} supply domain swings negative. The node voltages for the V_{DD} rail clamp circuit are plotted in Figure 6.3(c). When V_{DD} is forced below V_{SS} due to ground bounce, the parasitic NW diode is observed to charge V_{RC} up to about the same potential as V_{DD}. After the ground bounce subsides and ESD current is no longer shunted to V_{SS} (it goes to board ground via V_{SSIO}), the quantity V_{DD}-V_{SS} is restored to its normal positive polarity. V_{RC} will track V_{DD}, but with a coupling ratio of less than one because a capacitive voltage divider is formed between the timing capacitor and the capacitors that lie between nodes V_{RC} and V_{SS}; the latter includes the parasitic capacitance of the timing resistor and the input capacitance of the first inverter. V_{RC} is coupled sufficiently high so that the active clamp is fully turned on, as evidenced by V_{Trig} tracking V_{DD}. The supply voltage for the V_{DD} domain does not get fully restored to its nominal 1.5 V until after the active clamp times out at about 1 μs; earlier, it is at 1 V, as shown in Figure 6.3(c).

6.2.3 – Demonstration in Measurement

It is desirable to confirm the preceding analysis with measurement data. However, the large board-level decoupling capacitance may prevent the rail clamp current from producing a significant voltage drop on the board power plane (most board regulators respond too slowly to mask the effects of current drawn by ICs, which is why decoupling capacitors are needed in the first place). The lack of a noticeable power supply disturbance on the board-level does not preclude such a disturbance from existing on the chip, since the bond-wire impedance partly decouples the board and chip level supply voltages. Here, droop on the test chip's V_{DDLU} supply was rendered visible by reducing the board-level decoupling capacitance on V_{DDLU} to 1 nF and then zapping an IO in the V_{DDIO} domain using an ESD gun with the board grounded. The voltage on V_{DDLU} is measured using an oscilloscope. A 2.4 kΩ probe is used to minimize the loading on the supply. The signal attenuation caused by the probe is corrected for during data post processing.

The waveform measured at V_{DDLU} during a +2 kV zap is shown in Figure 6.4(a). After the initial noise spike dissipates, the supply voltage has fallen to 0.5 V and then it recovers on a microsecond time scale. ESD zaps were also applied when the normal decoupling capacitance was used; results for a +2 kV zap are shown in Figure 6.4(b). In this case, the supply voltage falls to 0.75 V and then very slowly recovers on a time scale exceeding 1 ms. The disturbances on V_{DDLU} occur regardless of the polarity of the zap or the zapped pin, once the zap voltage exceeds about +/- 2 kV.

To understand the measurement results of Figure 6.4, the dynamic response of the on-board voltage regulator must be considered. V_{DDLU} is powered by a regulator configured as shown in Figure 6.5(a). By design, the on-chip circuits connected to V_{DDLU} have reduced latchup

resilience, and thus the resistor R_S is used to limit the current flowing into the chip and prevent latchup-induced hard failure. The op-amp sinks current through R_S to produce the desired voltage; a diode is placed at the op-amp output to prevent it from supplying current if the chip latches up. Figure 6.5(b) shows a simulation model that can be used to reproduce the behavior of this voltage regulator; R_P and C_P are used to model the frequency response of the op-amp regulator. The model for the dependent source includes parameters for the maximum and minimum output current; the effect of the diode in Figure 6.5(a) is emulated by restricting the dependent source to positive current.

Using the model of Figure 6.5(b) to represent the board-level V_{DDLU} supply, the full-chip response to an ESD zap is obtained from circuit simulation. The case simulated is a +2 kV discharge to an IO; the board-level decoupling capacitance on V_{DDLU} is set to 1 nF, as in the experiment of Figure 6.4(a). The simulated transient on V_{DDLU} is shown in Figure 6.6. The simulated gate voltage of the active clamp, V_{trig}, is also plotted, clearly showing that the active clamp is turned on. The simulation results support the interpretation of the data shown in Figure 6.4(a): *the active clamp protecting V_{DDLU} has been turned on, despite the ESD zap not having been applied to a pin within the V_{DDLU} domain*. In both measurement (Figure 6.4(a)) and simulation (Figure 6.6), the V_{DDLU} undergoes a slow, almost linear increase toward V_{nom} once the rail clamp times out. However, in measurement, the supply voltage slightly overshoots V_{nom} before finally settling to its final value, a behavior that is not replicated in simulation. This small discrepancy is attributed to the simple model of the voltage regulator, which does not exactly replicate the frequency response of the op-amp.

The simulation is repeated with the board-level decoupling capacitance increased to 47 μF. No disturbance of the board-level supply voltage is observed, inconsistent with the

measurements shown in Figure 6.4(b). The fact that the measured V_{DDLU} falls to about 0.75 V suggests that latch-up has occurred. The supply recovers slowly due to the large decoupling capacitance and the limited supply current. Latch-up is not observed on the other supply domains, which have a very high well-tie density. The simulation netlist does not include parasitic SCRs and thus latchup is not expected to be replicated in simulation. It is likely that latchup is triggered by the on-chip V_{DDLU} falling below V_{SS}, in a situation comparable to that shown in Figure 6.3. This would forward-bias all the P-substrate/N-well junctions in the domain, flooding a region of the substrate with minority carriers, which would then be "swept back" into the N-wells when the supply polarity recovers, triggering latchup [40]. Because the voltage regulator for V_{DDLU} can only source a few milliamps of current, latchup is not sustained, allowing the regulator to restore the supply voltage, albeit very slowly due to the current limiting resistor and the large decoupling capacitance.

As a final observation, it's worth noting that the V_{DDIO} plotted in Figure 6.3(b) (with respect to V_{SSIO}) does not show oscillations, in contrast to the simulated supply voltage waveforms shown in Figure 5.11. This is the result of using a simpler, and more idealized, representation of the power distribution network when generating Figure 5.11. This demonstrates that a full description of the supply network may be required to validate the stability of an active clamp circuit.

6.3 – Powering Down the Zapped Domain – Theoretical Analysis

Section 6.2 has shown that the supply inductance, e.g. due to bond wires and on-board decoupling capacitor parasitics, can strongly affect the path the ESD current takes through an IC. Specifically, it was shown that a zap on an IO domain briefly powered down an adjacent power domain due to large ground bounce in the package parasitics. However, it is also possible for a

zapped power domain to be temporarily powered down by the slow transient response of the clamp, or due to the supply inductance. The former case is relatively simple to understand; if the ESD current decreases rapidly and the clamp is not designed to respond quickly enough, it will discharge the on-die supply capacitance. The latter is more complicated; relevant elements along the discharge path are shown in Figure 6.7, and a simplified, equivalent circuit is shown in Figure 6.8. The ESD clamp is represented as an ideal voltage source, which is a good approximation as long as it is conducting positive current that is small enough such that all the transistors in the trigger circuit are in the saturation region (e.g. below 4 A in Figure 5.9).

During the fast rising edge of an ESD current pulse, the voltage drop in the inductors will be large relative to the difference between V_{clamp} and $V_{DD,nom}$. (A slew rate of 15 A/ns, which is typical of system-level ESD, would induce a 15 V drop in 1 nH of supply inductance, which is significantly larger than the several hundred of millivolts difference between the clamp's cut-in voltage and the nominal supply voltage.) Since the voltage difference between the clamp and the board decoupling capacitor is small, the supply inductances L_{DD} and L_{SS} are approximately in parallel during the fast rising edge. The portion of ESD current going to each will be determined primarily by the inductive current divider between L_{DD} and L_{SS}.

However, after the initial large di/dt subsides, the voltages across the supply inductances will be determined by the rail clamp's cut-in voltage (V_{Clamp}) and the voltage of the large on-board supply decoupling capacitance ($V_{DD,nom}$). Because V_{Clamp} is larger than $V_{DD,nom}$, the voltage across L_{DD} is positive and the voltage across L_{SS} is negative; thus, the current to the on-board decoupling capacitance will increase and the current to the rail clamp will decrease (and eventually reach zero). If the ESD current has a large, negative di/dt (such as seen in the IEC-61000-4-2 waveform after the initial peak), the incremental negative current, i.e. the total change

in current during a falling edge, will be split between L_{DD} and L_{SS}, as it was during the initial rising edge. This incremental negative current can cause the total current sunk by the rail clamp and on-die decoupling capacitance to become negative and discharge the on-die supply decoupling capacitance.

The above analysis was validated by circuit simulation. For these simulations, C_{Board} is set to 10 μF and charged to the nominal supply voltage by a 1 kΩ resistor, and both L_{DD} and L_{SS} are set to 3 nH with 100 mΩ series resistance. In some simulations, a second 1 kΩ resistor is added in series with the V_{DD} bond wire so that it conducts very little ESD current. The clamp is implemented using a circuit similar to that shown in Figure 5.8, designed in 65 nm CMOS with a 2.5 V IO supply voltage. The ESD current is made by passing a rectangular current pulse through a rise time filter [41]; a slowly decaying tail is added to ensure the ESD current is always positive, even if the filter has overshoot that would give negative current during the falling edge. This pulse is formed by combining the effects of two current sources, i.e. placing either two voltage sources in series or two trapezoidal current sources in parallel (the choice does not matter, as a source impedance is added that makes the two methods equivalent); the first creates an approximately rectangular current pulse by using very fast rise/fall times relative to the pulse width; the second pulse's rising edge is overlapped with the first pulse's rising edge with a rise time equal to the first pulse's fall time, a pulse width of zero, and a slow fall time, resulting in a smooth transition from the rectangular current pulse into a decaying current in the shape of a right triangle. In Figure 6.9(a), a 100 ps rise time filter was used, giving a clean rectangular current pulse. When current through the V_{DD} bond wire is limited by a large valued resistor, I_{ESD} flows primarily through the clamp; during the falling edge of the pulse, the clamp cannot turn off quickly enough, and the supply voltage drops. However, when the V_{DD} bond wire is configured

normally, the current is evenly split between the V_{DD} and V_{SS} bond wires. After the rising edge, the current through the V_{SS} bond wire decreases while the current through the V_{DD} bond wire increases, as predicted. During the current's falling edge, the V_{SS} current briefly becomes negative, powering down the supply. This simulation was repeated using an 800 ps rise time filter, resulting in an I_{ESD} that more closely resembles typical system-level ESD stress. The results of this simulation are plotted in Figure 6.9(b). In this case, when the bond wire is disabled, the clamp responds quickly enough so that the supply is well-regulated. However, when the bond wire is enabled, a negative current is forced through the V_{SS} bond wire during the current's falling edge. Even though the clamp can respond quickly enough to the incident current, the power supply still turns off because of supply inductance. It is also worth noting that because the supply can be powered down even if the clamp responds very quickly, it can affect power supplies that use other types of ESD protection, such as snapback clamps.

6.4 – Conclusion

This chapter has demonstrated that, during an ESD event, ground bounce resulting from parasitic inductance in the system or package can cause the ESD current to take unexpected paths through an IC. The ground bounce may be large enough to briefly power down power domains on the chip and cause the active clamp to fire. In addition to disrupting normal operation, the former effect poses a latch-up risk if the N-well/P-substrate junction becomes forward-biased; the latter effect may prevent the on-chip supply from quickly recovering. *These effects can affect all power domains on a chip, not just domains associated with pins that may be exposed to ESD current.* Both failure mechanisms presented in this chapter have been demonstrated in measurement and the latter has been demonstrated in simulation.

6.5 – Figures

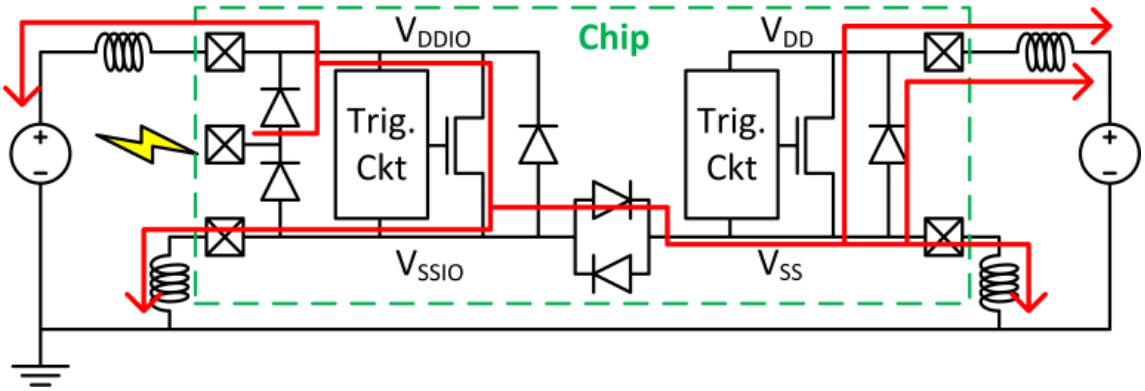


Figure 6.1: Current path during positive I/O zap.

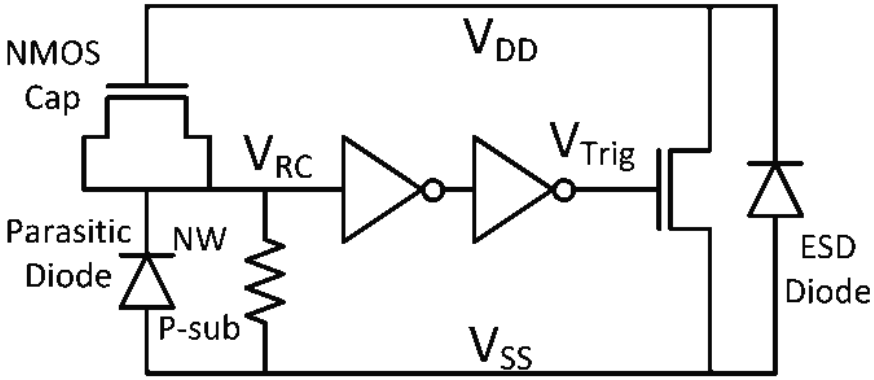
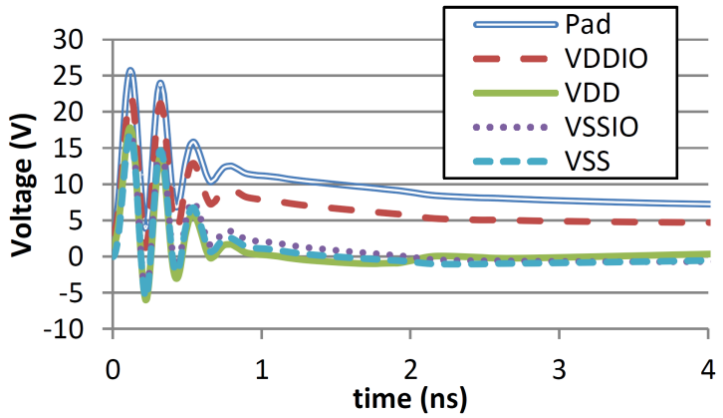


Figure 6.2: Implementation of RC timing elements in the 2-stage trigger circuit, with the parasitic P-sub/NW diode shown explicitly. This diode will discharge the timing capacitor if V_{SS} rises above V_{DD}. In a more common configuration, the terminals of the capacitor are flipped, connecting the parasitic diode to V_{DD}, instead of the timing node.



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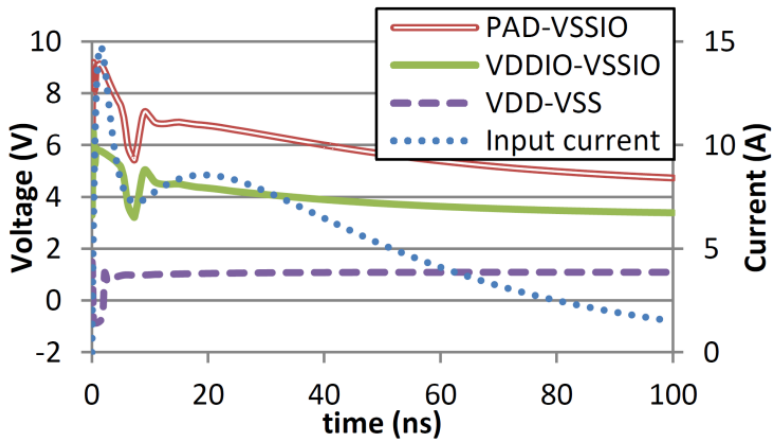

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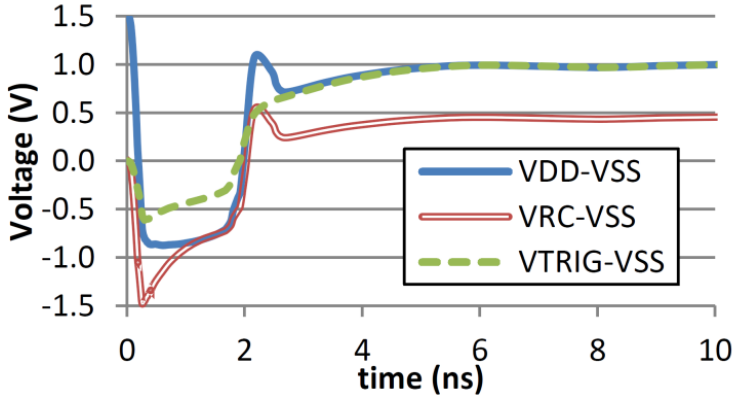
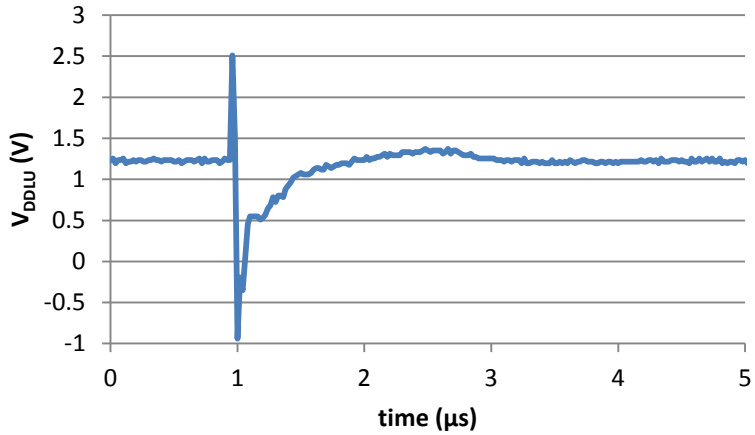
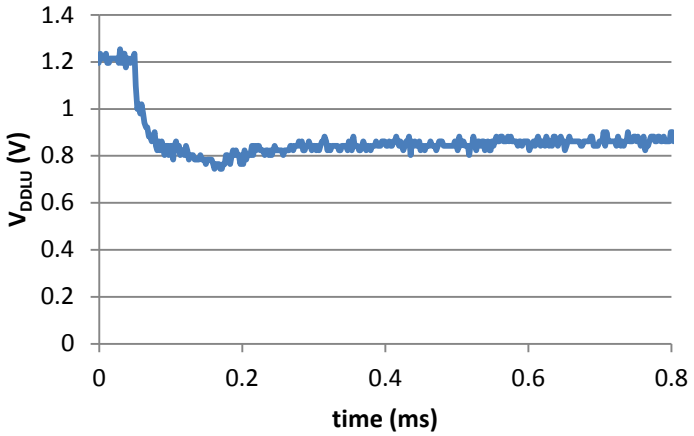


(c)

Figure 6.3: Simulated response to a +4 kV zap at an IO in the V_{DDIO} domain. (a) On-chip voltages at the zapped pad and supply busses referenced to board ground, (b) the same voltages referenced to local ground, and (c) internal voltages of the active clamp circuit protecting V_{DD}.

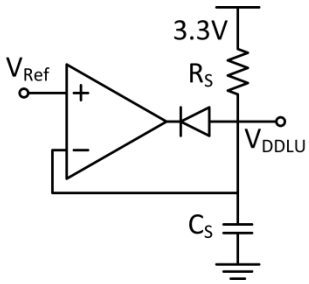


(a)

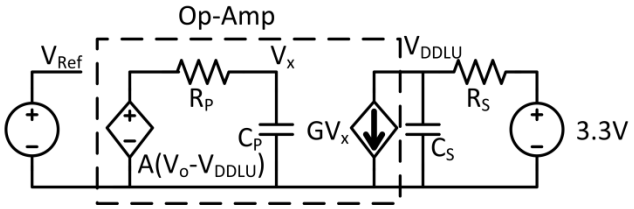


(b)

Figure 6.4: Measured transient on V_{DDLU} during a +2 kV zap to an IO on the V_{DDIO} domain, with (a) 1 nF and (b) 47 µF decoupling capacitance on V_{DDLU}. In (b), V_{DDLU} increases roughly linearly until 10 ms, when it reaches the nominal supply voltage.



(a)



(b)

Figure 6.5: The (a) implementation and (b) simulation model of the op-amp based voltage regulator used to power V_{DDLU}.

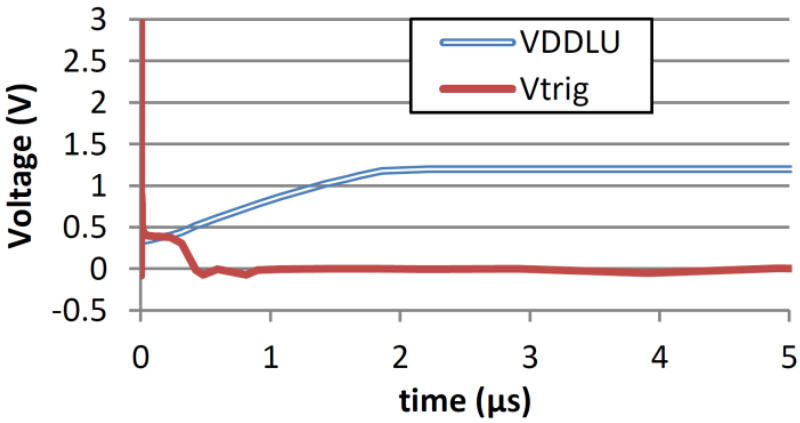


Figure 6.6: Simulated response on V_{DDLU} during a +2 kV zap to an IO. V_{DDLU} is powered using a regulator like that shown in Figure 6.5. R_S and C_S are 1 kΩ and 1 nF. R_P and C_P are set to produce a pole at 200 kHz. The initial voltage on V_{DDLU}, not visible in the plot, is 1.2 V.

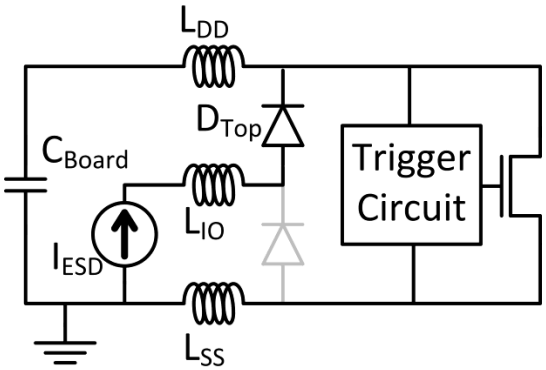


Figure 6.7: Schematic of a positive ESD zap to an IC.

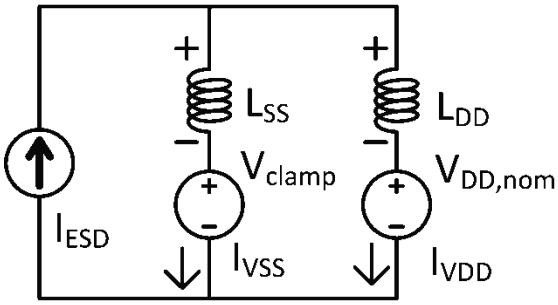
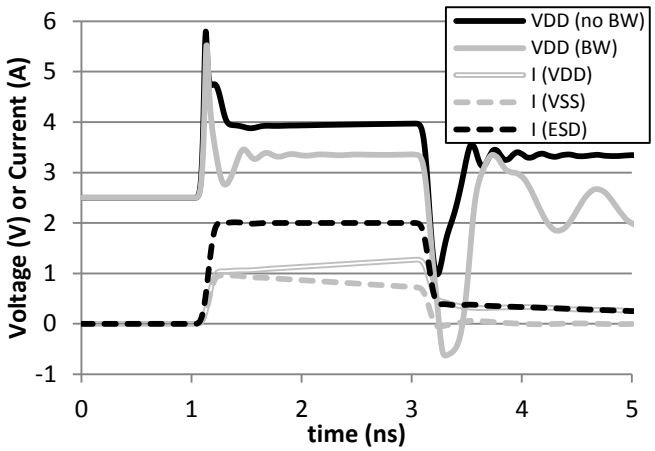
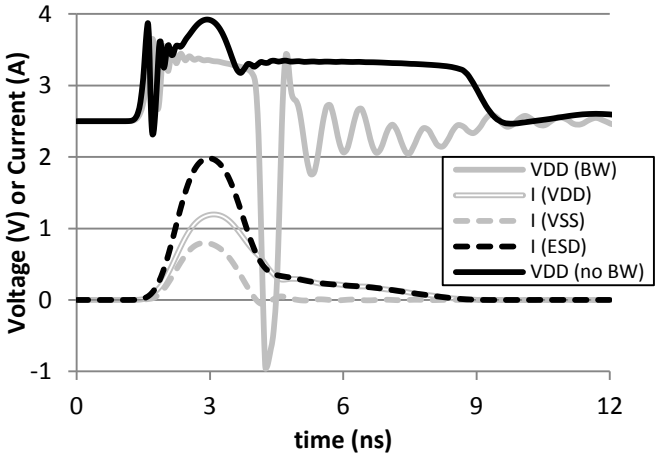


Figure 6.8: Simplified equivalent circuit of Fig. 14. Both L_{IO} and D_{Top} have been neglected because they are in series with the high impedance ESD current source. The decoupling capacitance, C_{Board} is represented by an ideal voltage source, $V_{DD,nom}$. The power clamp is represented by an ideal voltage source, V_{clamp}. V_{clamp} and L_{SS} are in series; their ordering has been switched to better illustrate the circuit's behavior.



(a)



(b)

Figure 6.9: Simulated on-die supply voltage given $I_{ESD}(t)$ consisting of (a) a rectangular current pulse with 100 ps rise and fall times and a slowly decaying tail after the main pulse, and (b) a pulse resembling the first current peak of a system-level ESD waveform. In each plot, the on-die V_{DD} is plotted for the case that the V_{DD} bond wire is configured normally ("BW") and for the case where its current is limited by a 1 kΩ series resistance ("no BW"). In the first case, the currents leaving the chip through the V_{DD} and V_{SS} bond wires are also plotted.

Chapter 7 – Glitches Produced by Coupled Noise During System-Level ESD Stress

7.1 – Introduction

Because ESD events have such high current derivatives, they can generate a substantial amount of electromagnetic noise. During system-level ESD, this high amplitude noise can couple to the input pins of an IC and produce a logic glitch at the input. This chapter describes experiments using the glitch detector circuit. These experiments indicate the ESD gun precharge voltage levels at which this coupled noise can produce a glitch on a digital input. For more information on the glitch detector circuit and the system into which it is integrated, see Sections 2.4 and 2.5, respectively.

7.2 – Experimental Results

Experimental results are presented for two configurations of the system presented in Section 2.5. In the first, the system is floating and powered by a battery pack. No connection to earth ground is explicitly provided; the stress current returns to earth ground through capacitive coupling. In the second configuration, the system is powered by a DC power supply. The connection to the DC power supply provides a connection to earth ground. Unless otherwise noted, the input to IO1 (the IO containing the glitch detector circuit) is driven by separate buffer IC.

7.2.1 – Battery Powered

Several experiments were performed with the system in the battery powered configuration. First, the aggressor line is zapped. The aggressor line is a trace that runs parallel to the line connected to IO1 before terminating at ground. This experiment determines the ESD

stress amplitude at which trace-to-trace coupling can become large enough to lead to signal disruption. These zaps are performed with input to IO1 set to “0” and “1” for both positive and negative polarity zaps. After each zap, the output of the glitch detector is read out and then reset. The test is performed at each precharge voltage is repeated several times. The second experiment is similar to the first, except the grounded USB1 shield (see Figure 2.17) is zapped instead of the aggressor line. In these experiments, the input data to IO1 are only set to “0”; that is, both input data polarities are not tested. The USB1 shield is not near IO1; this experiment indicates the ESD stress level at which system-wide noise becomes large enough to induce errors throughout the system.

These results for the two experiments described above are reported in Table 7.1. When zapping the aggressor line, glitches large enough to cause input logic errors occur more frequently in the following instances: (i) negative zap to aggressor when input to IO1 is low, (ii) positive zap to aggressor when input to IO1 is high. These results suggest that the glitch induced on the victim line has opposite polarity to the ESD zap. This observation indicates that the coupled noise is primarily inductive in nature. During a positive zap, the aggressor line’s potential will be elevated. Displacement current from the aggressor line would elevate the potential of nearby lines. This mechanism would suggest that a positive zap would be most likely to cause an error when the input is already low, which contradicts the observed errors. Conceptually, errors could also be caused by ground potential differences between the transmitter and receiver ICs due to resistive drops; however, the resistance of the ground plane should be very small. Similarly, radiation should not be strongly coupled to the board. The current waveform’s spectral content is relatively small above 300 MHz (see Figure 2.12); at

these frequencies, features on the board should all be electrically small and not act as good antennas.

Zaps on the USB shield are also seen to cause error-inducing glitches, but at much higher precharge voltages. During these tests, it was observed that the orientation of the ESD gun can significantly alter the precharge voltage required to induce a glitch without altering the injected current. The causes of these glitches cannot be determined as cleanly as the glitches caused by zapping the aggressor line. Positive zaps to the USB1 shield are more likely to create a false "1" than are negative zaps; this trend could be caused by either capacitive or inductive coupling. It is also more difficult to rule out ground plane potential differences between the driver and receiver because the stress current required to produce a glitch is significantly larger than when zapping the aggressor line.

A third experiment was performed with the system in the battery powered/floating configuration. In this experiment, the input signal was driven low with either the buffer IC used in the other experiments or with a resistive pull-down. This experiment was performed to rule out the possibility of the buffer IC being the source of the input glitches. The testing procedure is similar to the previous two experiments. Both the aggressor line and USB1 shield are zapped. The results of this experiment are shown in Table 7.2. In both cases, the trends are not substantially different, which indicates that coupled noise is the dominant factor in producing the glitches.

7.2.2 – Grounded System

Another experiment involving the glitch detector was performed to determine the effect of system grounding on the amplitude of the induced noise signal. Three points on the board were zapped: the aggressor line, the USB shield, and the board ground to the left of the control

signal filters shown in Figure 2.17. In all of the tests, the input to IO1 is held low and positive ESD zaps are applied to the system. In the tests which required the board to be grounded, a cable was attached between the ground on the lower right portion of the board and the ground plane below the table. The results of this experiment are reported in Table 7.3. The measurement results indicate that when the aggressor line adjacent to IO1 is zapped, the noise coupled on to IO1 is not sensitive to the system grounding configuration. However, when the board ground is zapped, the results suggest that the connection to earth-ground reduces the amplitude of the coupled noise. Interestingly, in this experiment, when zaps were made to the USB shield the results obtained were different from those presented in Table 7.1. A possible explanation for this discrepancy is that the ambient humidity was different on the two different days, or slight differences in experimental setup. In the second experiment (Table 7.3), zaps to the USB shield did not cause any glitches, but the ESD discharge was audible for precharge voltages above 6 or 7 kV. This may indicate the presence of a conducting path from the USB connector's mounting pin on the bottom of the board to the table top through the air; this would shunt current away from the board thereby reducing the displacement current that elevates the board potential relative to the table top. In the earlier experiment (Table 7.1), glitches were detected and there were no audible discharges.

7.3 – Conclusion

Taken together, the experimental results in this section provide several interesting pieces of information. Trace-to-trace inductive coupling can produce an input glitch that is capable of affecting logic circuits at relatively low precharge voltages, regardless of grounding configuration. It is also worth noting that the fact that this measurement can be reliably repeated suggests that the glitch detector circuit does work. The susceptibility of a circuit seems to be

independent of the driver strength, as shown in Table 7.2, though it may be affected by the polarity of the zap and the signal level of the driver. Lastly, ESD zaps to ground can still disrupt signal lines; however, these disruptions occur and significantly higher stress levels. In general, they are less reproducible than trace-to-trace coupling, which suggests some dependence on the measurement setup and possibly testing environment (e.g. humidity may affect spark formation).

7.4 – Tables

Table 7.1: Glitch detection results when zapping the aggressor line and USB1 shield. Aggressor line is a signal trace placed near the IO1 input. The USB1 shield is connected to board ground and is far away from IO1. Each entry represents the number of glitches detected per the number of repeated zaps. Incidences of glitches due to USB shield zaps are strongly affected by the orientation of the ESD gun.

	Zap on Aggressor Line				Zap on USB Shield	
V_{pre} (kV)	Data Input Low		Data Input High		Data Input Low	
	+ Zap	- Zap	+ Zap	- Zap	+ Zap	- Zap
0.25	-	2/5	2/3	-	-	-
0.5	0/1	4/4	2/3	0/3	0/3	0/3
1	0/1	2/3	1/5	1/3	0/3	0/3
1.5	0/1	3/3	3/3	1/3	0/3	0/3
2	1/3	3/3	3/3	3/3	0/3	0/3
2.5-5	3/3	3/3	3/3	3/3	0/3	0/3
6	3/3	3/3	3/3	3/3	1/3	0/3
7	3/3	3/3	3/3	3/3	2/3	0/3
8	3/3	3/3	3/3	3/3	3/3	1/3

Table 7.2: Glitch detection results with different signal trace drivers. IO1 is being driven low by either a buffer or a resistive pull-down. Each entry represents the number of glitches detected out of the total number of zaps.

V_{PRE} (kV)	Zaps to Aggressor Line	
	Buffer IC	Resistive Pull-Down
0.2	0/3	0/3
0.5	0/3	0/3
1	0/3	1/3
1.5	2/3	3/3
2	3/3	3/3
V_{PRE} (kV)	Zaps to USB Shield	
	Buffer IC	Resistive Pull-Down
4	0/3	0/3
5	0/3	0/3
6	0/3	0/3
7	1/3	0/3
8	1/3	0/3
9	0/3	0/3
10	0/3	1/3
11	0/3	2/3
12	2/3	3/3

Table 7.3: Glitch detection results for battery powered and grounded systems. Each entry represents the number of glitches detected per the number of repeated zaps.

V_{pre} (kV)	Aggressor Line		USB Shield		Board Ground	
	Battery	Grounded	Battery	Grounded	Battery	Grounded
0.5-1	0/3	0/3	0/3	0/3	-	-
1.5	2/3	2/3	0/3	0/3	-	-
2-4	3/3	3/3	0/3	0/3	-	-
5-7	-	-	0/3	0/3	0/3	0/3
8	-	-	0/3	0/3	2/3	0/3
9	-	-	0/3	0/3	2/3	0/3
10	-	-	0/3	0/3	3/3	0/3
11	-	-	0/3	0/3	-	3/3
12	-	-	0/3	0/3	-	3/3

Chapter 8 – Experiments and Circuits on Second Test Vehicle

The original test vehicle (see Chapter 2) used for this research provided many informative results about system-level ESD; however, research into this topic is still relatively incomplete. Thus, a new test vehicle has been designed to perform further research on the topic. This chapter describes the experiments included on this test vehicle.

8.1 – Test Vehicle Overview

A layout of the test vehicle is shown in Figure 8.1. The 65 nm CMOS chip has a 2.5 V IO domain and a 1.2 V core domain; both domains share a single V_{SS} rail. Two primary groups of experiments are included on the chip: system-level ESD related experiments, which are on the upper section of the chip, and high-speed IO experiments [42] which are on the lower section of the chip. The IO domain is used to power all of the IO circuits on the upper half of the chip, including ADDR0, ADDR1, GD1, GD2, GD3, GD4, GDF, OSC, and ORED. The remaining IOs, SDO, RST, LE, SCK, SDI, and RX_EN use only the core domain. (There are several additional unlabeled pins associated only with the high-speed IO experiments.) Of these pins, ADDR0, ADDR1, SDO, RST, LE, SCK, SDI, and RX_EN are control signals used control the state of the chip, or to read experimental results off the chip. The remaining pins, GD1, GD2, GD3, GD4, GDF, OSC, and ORED are associated with specific experiments.

The system-level ESD experiments fall into four categories: (i) errors due to input glitches, (ii) errors in long internal signal lines due to supply voltage gradients, (iii) errors in latches due to power supply fluctuations, and (iv) demonstration of rail clamp instability. Each of these experiments are detailed in the subsequent sections.

8.2 – Errors Due to Input Glitches

The experiments presented in this section are intended to expand upon the results presented in Chapter 7, which were informative but limited by the hardware available on the first test vehicle. The second test vehicle has a variety of hardware to allow for both a qualitative studies of the coupled noise that the chip experiences and design techniques for mitigating the impact of noise.

For the first experiment, glitch detector circuits (Figure 2.15) were placed on several IOs (GD1-GD4, GDF, and ORED) to determine differences in glitch prevalence with various spatial factors, such as relative distance to rail clamp circuits and distance from the zapped pin. A simplified version of the glitch detector circuit was used because these IOs did not need to be bidirectional. The simplified version removes both the output driver and the multiplexors; the multiplexors were required to disable glitch detection when the IO functions as an output driver.

All of the other glitch detection experiments introduce new circuits and are summarized here; they are presented in depth in their own subsections. The first is the out-of-range error detector, which is at the ORED pin. It is designed to be a circuit that can (unlike the glitch detector) detect signal glitches during normal operation, i.e. when the signal can switch either to perform some function or because of noise. The second is the glitch counter, which is connected to the GDF pin. It is intended to provide more information than a basic glitch detector; it counts edge transitions, thereby providing information about the number of glitches that occur on a constant signal line. The third experiment tests the effectiveness of various filters for suppressing glitches. These filters are connected to the buffered input of GDF.

8.2.1 – Out-of-Range Error Detector

The out-of-range error detector (ORED) is a circuit developed to provide a means of detecting large amplitude electromagnetic noise at digital IOs during normal operation i.e. when the signal can switch either to perform some function or because of noise. Such information could be used, for example, by software to provide some means of recovering from any induced errors. Alternatively, it could be used to aid in system-level ESD debugging by indicating the victims of the coupling. The glitch detector cannot fill this role because it requires a constant input level; it cannot distinguish between signal and noise during normal operation.

To discriminate between signal and large amplitude noise, some characteristic of the signals must be different. When developing the ORED, it was assumed that any input signal will remain between the supply rails (in-range), while large amplitude noise will likely produce a voltage that is not between the supply rails (out-of-range). Hypothetically, a noise pulse could exist strictly between the supply rails; however, such noise would be substantially more difficult to differentiate from signal.

The original concept for the ORED was to modify the primary ESD diodes to include a collector diffusion that is pulled high or low by a resistor. This forms two common-base amplifiers with inputs at the IO pad. The resulting schematic is shown in Figure 8.2. When the IO pin goes significantly above VDD, D_{Top} turns on and OREH (out-of-range error high) is pulled high. When the IO pin goes significantly below VSS, D_{Bot} turns on and ORELb (out-of-range error low bar) is pulled low. The signals OREH and ORELb are both stored on SR latches. The circuit design shown in Figure 8.2 has one major drawback: the lateral bipolar structure formed in the ESD diodes is not a device typically supported by design kits, so no accurate circuit model will be readily available.

The lack of simulation models for the bipolar structure can be remedied by using a common-gate amplifier instead of a common-base amplifier. A design based on this idea is shown in Figure 8.3. Unlike the design in Figure 8.2, this design is built into the CDM protection; the secondary ESD diodes are the source-body junctions of the MOSFETs. This modification is required to limit the gate voltage on each common-gate amplifier to a safe level. In this circuit, the bodies are tied to the supply, rather than the IO. In addition to being the normal configuration for secondary ESD diodes, this applies a forward body bias as the circuit is about to turn on, further improving the sensitivity of the circuit, i.e. the minimum excursion beyond the supply rails required to detect an out-of-range error.

The circuit in Figure 8.3 was designed using thick gate oxide devices in 65 nm CMOS. The component values are listed in Table 8.1. The circuit was simulated in Spectre with a 2.5 V supply voltage; a brief positive and negative excursion beyond the supply is applied to the pin. Figure 8.4(a) shows the result of this simulation when these excursions are 0.6 V, which is near the minimum excursion required to trigger the SR latches connected to OREH and ORELb. The level shifted outputs of these latches are labeled OREH_digital and OREL_digital. The digital outputs switch within about 300 ps of the pad voltage exceeding the power rails by 0.6 V. Figure 8.4(b) shows the same simulation with a significantly larger excursion. The node connected to the sources of the NMOS and PMOS is clamped near each supply rail instead of following the pad voltage; transistor inputs connected to this node will not be damaged during CDM, including the NMOS and PMOS transistors used in this circuit.

To further investigate sensitivity of this circuit to pulse duration, pulses of varying amplitude are applied to the ORED's input in simulation. To test the OREH/OREL behavior, the input voltage is initially VDDIO/VSS, and a positive/negative pulse with 100 ps rise time is

superimposed on the initial voltage. The minimum pulse amplitude that triggers the ORED circuit is reported in Figure 8.5 as a function of the pulse duration. At very short durations, the ORED become less responsive; however, even for pulses with 100 ps duration, the sensitivity is only slightly degraded.

8.2.2 – Glitch Counter

The glitch counter is designed to count the number of rising edge transitions at an IO pin, and thus count the number of noise-induced glitches that occur. Much like the glitch detector, it is not designed to be used on a functional IO pin, as it cannot differentiate between a signal and noise. The glitch counter is intended to be used as a research tool. It is impossible to probe on-die nodes with an oscilloscope, so it is very difficult to determine the nature of the noise waveforms induced at an IO pin. Whereas the glitch detector only indicates the presence of noise, the glitch counter will provide some additional information about the shape. For example, a damped sinusoid on the chip would produce many rising edge transitions, whereas a single pulse will only produce one.

The implementation of the glitch counter is shown in Figure 8.6; it consists of a 7-bit shift register clocked by a buffered input signal. The D signal to the first shift register is a fixed "1" and the shift register resets to "0". After each rising edge, one additional register will have a high output. The output of the entire shift register is then connected to a thermometer-to-binary converter for read out. This counter implementation was chosen for speed. As long as the counter is faster than ESD induced noise, it will provide an accurate count of the number of glitches that occur; a slower counter architecture requires more design effort to ensure a reliable output. The schematic for one of the registers in the shift register is shown in Figure 8.7. The buffered IO signal (which drives the register's CK) experiences at most four gate delays, so the circuit can

operate very quickly. The worst-case delay path is (i) generating CKb from CK, (ii) the rightmost AOI22, (iii) the NAND2, and (iv) the inverter.

The glitch counter circuit was simulated in Spectre to ensure it operates quickly enough to respond to the input signal caused by ESD noise. The simulation results are shown in Figure 8.8. Pre-layout simulation indicates that the circuit operates correctly with a 6.25 GHz square wave at the input. This is 20 times faster than a typical system-level ESD current waveform, which is limited to below roughly 300 MHz. Thus, the glitch counter will likely provide reliable output as long as the supply is not greatly disrupted.

8.2.3 – Filtered Input Lines

The purpose of these experiments is to determine how effective various filters are at suppressing signal glitches at an IO pin. Ideally, if the duration of the signal glitch at the filter's input is significantly less than the response time of the filter, no digital glitch will show up at the filter's output. If this method can effectively suppress glitches, it provides a straightforward way of mitigating the effects of ESD induced noise on low speed inputs.

Each of the filters in this experiment are implemented in the 1.2 V core power domain. All of the filters have their inputs connected to the buffered signal input at the pad GDF. Their outputs are connected to glitch detectors. The majority of the input filters are first-order passive RC filters, as shown in Figure 8.9. Multiple copies of this filter are instantiated on the test vehicle with varying time constants. The filter circuit was instantiated four times with various time constants. The time constants are selected so that the outputs will switch 3.3 ns, 10 ns, 33 ns, and 100 ns after the input. Additionally, a control case and a digital filter were instantiated. In the control case, the buffered input signal is connected directly to a glitch detector.

The digital filter is shown in Figure 8.10. This circuit stores the digital input for the last three clock cycles. The stored inputs "vote" to determine the output. That is, if there are two or more stored "1"s, the output will be "1"; if there are two or more "0"s stored, the output will be "0". Thus, a glitch must occur on two consecutive clock edges for it to appear at the output. This functionality can be produced using the carry generation circuitry that would be used in a full adder. The specific implementation is shown in Figure 8.11. The oscillator signal (Osc) is provided by the on-chip relaxation oscillator shown in Figure 8.12. The relaxation oscillator has a period/frequency of about 100 ns/10 MHz. If the glitch occurs immediately before a clock edge, the second rising edge will occur in 100 ns; if the glitch occurs immediately after a clock edge, it will take nearly two clock periods for two clock edges to occur. A glitch must last between 100 ns and 200 ns for it to be observable at the output, depending on when it begins, relative to the clock phase.

The digital filter is not especially layout efficient; it is slightly larger than the largest passive filter implemented, which has a 100 ns time constant. However, it is still an interesting case to study for a few reasons. First, it is possible to implement similar functionality to this digital filter using any generic processor. If this filter works at the hardware level, it may also work at the software level, so it may be able to be implemented on existing processor designs without any hardware modification. Second, it can likely be shrunk significantly, both by layout optimization and by process scaling; with proper optimization, it may be more layout efficient than passive filters. Third, the digital filter would be easier to reconfigure than passive filters. For example, the response time could be controlled by clock division, instead of a large number of switches and passive components.

8.3 – Errors in Long Internal Signal Lines Due to Supply Voltage Gradients

The goal of this experiment is to determine whether or not errors in long on-die signal lines are likely to occur. Section 8.3.1 will describe the theoretical reason why errors in long lines can occur due to ESD current when they would not occur with shorter line. Section 8.3.2 discusses experimental design on the test chip in attempt to reproduce these errors.

8.3.1 – Analysis of Errors in Long Lines

Figure 8.13 shows a basic schematic for a driver/receiver pair; because the driver and receiver are far apart, there is significant supply resistance between the two. By assuming (i) that the receiver switches at half its local supply voltage and (ii) that the input voltage of the receiver is equal to one of the supply voltages at the driver, it is possible to determine the conditions for an error based on the supplies at the driver, VDD1 and VSS1, and the supplies at the receiver, VDDRX and VSSRX (which is taken as a reference). If the driver outputs a "1" the receiver will erroneously detect a "0" if

$$VDDTX < V_{M,RX} \approx \frac{VDDRX}{2}. \tag{8.1}$$

Thus, a false "0" can occur if the driver's VDD is depressed and/or the receiver's VDD is elevated. Analogously, if the driver outputs a "0" the receiver will erroneously detect a "1" if

$$VSSTX > V_{M,RX} \approx \frac{VDDTX}{2}. \tag{8.2}$$

Thus, a false "1" can occur if the driver's VSS is elevated and/or the receiver's VDD is depressed.

Figure 8.14(a) and (b) show how current would flow during a negative IO zap depending on the positions of the driver and receiver relative to the zapped pin and VSS pin. In Figure

8.14(a), the driver is closer to the zapped pin than the receiver. The current flows along VSS from the receiver to the driver, which decreases VSSTX; based on (8.2), a false “1” is unlikely to occur. However, if VSS falls low enough below VDD, a rail clamp may turn on, causing VDD to track VSS. Thus, if VSSTX becomes low enough, VDDTX may also be pulled low, potentially causing a false “0”. It is worth noting that this depends on the position of the rail clamp; a specific layout may make this unlikely to occur. In Figure 8.14(b), the receiver is closer to the zapped pin than the driver. The current flows along VSS from the driver to the receiver, which increases VSSTX. This scenario could cause a false “1”.

Figure 8.15(a) and (b) show how current would flow during a positive IO zap depending on the positions of the driver and receiver relative to the zapped pin and VDD pin. In Figure 8.15 (a), the driver is closer to the zapped pin than the receiver. The current flows along VDD from the driver to the receiver, which increases VDDTX; a false “0” is unlikely to occur. However, the elevated VDDTX may cause a local rail clamp to turn on, pulling VSSTX up. This could lead to a false “1”. As with the discussion pertaining to Figure 8.14, this mechanism is dependent on clamp placement. In Figure 8.14(b), the receiver is closer to the zapped pin than the driver. The current flows along VDD from the receiver to the driver, which increases VDDRX. This scenario could cause a false “0” if VDDRX becomes much larger than VDDTX.

The results of the preceding discussion are summarized in Table 8.2. Notably, the error mechanisms presented in this section closely resemble the mechanisms that lead to damage in power domain crossing circuits during CDM testing [43].

8.3.2 – Experimental Design for Reproducing Errors in Long Signal Lines

In an attempt to demonstrate the possibility of resistive drops in supply buses causing errors in long signal lines, an experiment was designed and placed on the test vehicle. It is

located in the box “Long Lines” in Figure 8.1. When an IO pin, e.g. OSC, is zapped, there will be resistive drops on VSS between the zapped pin and the VSS pins near each corner of the chip. The experiment is oriented such that these resistive drops occur in the same direction as the signal lines, which could cause an error.

The victim signal lines in this experiment use VDD12 and VSS as positive and negative supply rails. The IO circuits have ESD protection diodes that go to VDD25 and VSS. Because a positive IO zap will inject current on VDD25, but the victim signal lines are referenced to VDD12, it is unlikely that positive zaps will cause errors. However, a negative zap will inject current on VSS, which the victims are referenced to. Thus, an error during a negative IO zap is significantly more likely.

Figure 8.16 shows a diagram of the experiment. There are two pairs of drivers that output complementary signals. That is, one driver in a pair outputs “0” and the other outputs “1”. One driver pair drives a line that travels to the left; the other driver pair drives a line that travels to the right. Glitch detectors are placed at 50 μm intervals along each line. Since driver has a constant input, any change in the output indicates that a logic level error has occurred; the glitch detector circuit is ideal for detecting such an event. Each glitch detector taps into the local power buses, which are drawn as a grid with 40 μm square tiles. This experiment allows for testing each case given in Table 8.2, namely: positive/negative zap, TX/RX near the supply pin, and false “0”/false “1”.

8.4 – Errors in Latches Due to Power Supply Fluctuations

In [6], it was observed that an on-chip shift register was disrupted when a distant IO was subjected to system-level ESD. The shift register was controlled by external clock, data, and latch-enable signals. The root cause of this disruption could not be determined from circuits on

the test chip. One hypothesis was that chip-wide power noise was disrupting the latches. Another hypothesis was that large ground bounce would cause a difference in the board/chip VSS potential, which could be erroneously interpreted as a signal. This section includes experiments to help determine whether or not the first effect (chip-wide power noise) can modify the data stored on latches.

In this experiment, three different core power domains are created, and several latches are placed on each of these power domains. The first, Domain 1, is connected to VDD12, i.e. it is driven by a voltage source external to the IC, as was done in [6]. The second and third supplies (Domains 2 and 3) are both sourced by on-chip voltage regulators powered by VDD25; a filtered version of VDD12 is used as a reference. The schematic of these regulators is shown in Figure 8.17, and a summary of key performance metrics of the regulator are given in Table 8.3. For Domain 2, the diode in Figure 8.17 is removed; for Domain 3, the diode is present.

The three supplies domains are used to isolate the effects of specific phenomena described in Chapter 6. In Section 6.2, it was shown that an external supply can be discharged during an IO zap on an adjacent external power domain; Domain 1 is susceptible to this type of power disruption when VDD25 is zapped; however, Domain 2 and Domain 3 are immune to it because they are referenced to VDD25. As demonstrated in Section 6.3, the zapped domain can be discharged by bondwire inductance. If VDD25 is discharged, Domain 2 will likely be affected, whereas Domain 3 should be immune because the series diode will block current flow from VDD_{int} to VDD25.

To determine the effectiveness of the series diode at preventing noise on VDD25 from appearing on VDD_{int}, the regulator is simulated with and without the diode during a brief dip on the supply. The dip is a trapezoidal pulse that goes from the nominal 2.5 V down to V_{min}; it has a

2 ns duration and 100 ps rise/fall times. No decoupling capacitance as added, beyond that provided in the voltage regulator. The results of this simulation are plotted in Figure 8.18(a) and (b) for V_{min} = -1 V and V_{min} = 0 V. The output of both regulators is disturbed because the 10 kΩ resistor pulls down the output and node V_G is discharged by the drain-body diode of the PMOS connected to the node. However, the disturbance on the supply with the diode is significantly less severe because the diode prevents the large NMOS from rapidly discharging the supply decoupling capacitance to the temporarily reduced VDD25. With the diode present, the performance could be improved by increasing the resistance or supply decoupling capacitance. Without the diode present, the NMOS will likely discharge the supply, regardless of the decoupling capacitance. As will be demonstrated later, it is unlikely that any latches connected to the supply with the series diode will be disturbed.

Each of the power domains described above contains eight latches. Any change in latch state not caused by asserting the RST signal indicates a large supply voltage drop (though such a drop could occur without a latch changing state). The latches include cross-coupled inverters (shown in Figure 8.19), D-latches (experiment schematic shown in Figure 8.20, latch schematic shown in Figure 8.21), and $\overline{SR}$ latches (shown in Figure 8.22). All gates for which no transistor level schematic is shown are implemented as static complementary CMOS. The leftmost latch in Figure 8.19, Q0, is intended to be more sensitive to brief interruptions on the power supply. The capacitors in the circuit cause the output to be “1” after power up, while the circuit resets to “0”. The other latches included in this experiment are intended to represent the most common types of latches found in CMOS processes. Each latch has an inverter placed directly at the output to minimize variations in capacitive loading due to routing. Furthermore, the state of the RST signal

may be poorly defined with large amplitude power noise; for this reason, each type of latch has one circuit where the RST signal is locally hard-tied so that the circuit never resets.

To verify latch Q0's ability to detect drops in supply voltage, in simulation, it was set to state "0" and a negative trapezoidal pulse was superimposed on the 1.2 V supply. The amplitude of the pulse is adjusted until the output switches to a "1" after power is restored. In addition, the rise time, fall time, and pulse width are varied. A sample transient from these simulations is shown in Figure 8.23. Notably, the state is preserved after power is removed; however, the coupling capacitors can erase the state during a rapid power up. Figure 8.24 shows the pulse amplitude required to flip the latch for several different pulse shapes. The figure shows the amplitude is determined predominantly by the rise time of the supply after the disturbance; however, both fall time and pulse width can play a role. If the rise time is fast enough, capacitive coupling currents will overwhelm the channel current of the transistors; the capacitors determine the final state of the latch. If the pulse width and fall time are too short, the nodes in the latch will not have discharged before power is restored, thus it will maintain its previous state more strongly. The discharging behavior can be seen in Figure 8.23. After about 5 ns, the discharge is limited to subthreshold current, and the discharging slows down dramatically. Notably, identical simulations were performed on the other latches in this experiment, and no data erasure could be reproduced; these latches will likely not experience upsets during experiments. The lack of data erasure is caused by the fact that the capacitive coupling is symmetric, whereas the channel currents are asymmetric and restore the previous state.

The simulation results in Figure 8.23 and Figure 8.24 suggest that only asymmetrically loaded latches like Q0 will be disrupted if their power is briefly removed. Further, the supply waveforms shown in Figure 8.18 suggest that no upsets will occur in the supply domain sourced

by the regulator with a series diode; because the supply recovers slowly enough, capacitive coupling currents will not be large enough to disrupt the instance of Q0 in this domain. The simulation results presented in this section indicate that latches might retain their stored data during a brief interruption in the supply.

This section has focused on bit flips in latches when the supply voltage rapidly increases after having fallen below its nominal value. Hypothetically, a similar error could occur in an asymmetric latch if the supply voltage rapidly increases from its nominal value to a higher value. This effect can be replicated in simulation using latch Q0, though the required stimulus is unrealistic. Using the same simulation setup as was used in Figure 8.23, Q0 can be upset with a 1.2 V to 3.1 V pulse with 1 ps rise time. Such a pulse is more than two orders of magnitude faster than is typical of ESD events, and thus highly unlikely to occur in the real world. This result passes a basic sanity check; if the pulse were slower than the logic circuit, the logic circuit would continuously restore its state. When the latch is powered on, it operates on a timescale of tens of picoseconds, so the pulse must operate on the scale of picoseconds. In contrast, when the power supply voltage is first significantly reduced, the latch enters the subthreshold region, and responds much more slowly. As demonstrated earlier, Q0 is much more susceptible under these conditions.

8.5 – Demonstration of Rail Clamp Behaviors

The goal of the experiments presented in this section is to demonstrate some of the behaviors presented in previous chapters using standalone test structures. Specifically, the first of these experiments attempts to demonstrate that the analytic rail clamp model presented in Chapter 5 predicts how circuit modifications will impact stability. The second experiment

attempts to demonstrate the mechanism presented in Section 6.3: when a power domain is zapped, that power domain can be discharged by the supply inductance.

8.5.1 – Demonstration of Factors Affecting Clamp Stability

To show how certain circuit modifications will affect stability, three 2.5 V rail clamps circuits were designed as standalone test structures and placed on the 65 nm test chip. Their designs are shown in Figure 8.25 and Figure 8.26. The 2-stage design shown in Figure 8.25 is fabricated with and without the 20 pF decoupling capacitor. For the 2-stage designs, the dominant pole occurs at the clamp's gate, as this node is the only node with appreciable capacitance. When the 20 pF capacitor is added, the pole on the supply node moves to a lower frequency, which may destabilize the circuit. As described in Chapter 5, 3-stage designs are very difficult to make stable because they have very high loop gain; the 3-stage circuit in Figure 8.26 will likely be unstable.

Before these designs were fabricated, various aspects of their performance were simulated. The quasi-static I-Vs were simulated by replacing the 1 pF timing capacitor with a 2.5 V DC voltage source (when the circuit responds to an ESD event, the voltage across the capacitance should barely change) and performing a DC sweep of the supply voltage. The quasi-static I-Vs are shown in Figure 8.27. The I-V of the clamp used in Section 8.5.2, labeled "Fast," is also plotted.

The loop gain of each design was also simulated at a quasi-static current of 0.6 A; the magnitude is plotted in Figure 8.28(a) and the phase is plotted in Figure 8.28(b). To perform this simulation, the timing capacitor is replaced with an ideal voltage source, as done in the DC simulation. A DC current source injects the bias current onto the VDD node. To break the feedback loop, a large valued inductor is used to separate the VDD nets of the trigger circuit and

the clamp. The AC input voltage is connected to the trigger circuit's VDD node through a large DC-blocking capacitor; the output is measured at the clamp's VDD node. As with the quasi-static I-V characterization, the clamp labeled "Fast" is also plotted. Figure 8.28 shows that adding the 20 pF capacitor did result in a negative phase margin for the 2-stage clamp, indicating the circuit will only be stable without the capacitor. The frequency response of the 3-stage design has a very high loop gain and negative phase margin. It should be unstable, as predicted.

The transient response of each clamp circuit to a 0.6 A TLP pulse was also simulated using the schematic shown in Figure 8.29. This schematic is intended to reproduce the setup that will be used to measure the transient response of these circuits, shown in Figure 8.30. The inductor and capacitor allow a TLP pulse to be superimposed on the DC bias (which represents the supply voltage). The simulated responses are plotted in Figure 8.31. As predicted by the AC simulation results, the 2-stage clamp circuit is only stable without the 20 pF capacitance, and the 3-stage clamp circuit is not stable. Because the 3-stage design has such poor stability, it undergoes very large oscillations. It is worth noting that the rail clamp circuit's designer may not know what decoupling capacitance will be present on the supply; when the rail clamp circuit is used on a given chip, it must be verified that the clamp design will be stable in the environment in which it is placed.

8.5.2 – Demonstration of Undershoot on a Zapped Power Domain

This experiment attempts to use standalone test structures to demonstrate the mechanism presented in Section 6.3: when a power domain is zapped, that power domain can be discharged by the supply inductance. As shown in Section 6.3, a power domain can also be discharged if the clamp circuit cannot respond quickly enough to changes in the input current. To prove that

inductance discharges the supply (as opposed to the clamp causing this problem), the clamp must be able to respond very quickly.

A fast-responding clamp was designed; it is shown in Figure 8.32. The simulated quasi-static I-V and frequency response of this clamp are plotted in Figure 8.27 and Figure 8.28, respectively. As shown in Figure 8.28, it has a unity gain frequency higher than any of the other standalone clamp circuits. This improvement is achieved by two modifications. The pull-down of the last stage is changed to an NMOS with its gate connected to VDD through an RC filter. This filter applies a delayed version of the supply voltage at the pull-down NMOS's gate. When the supply voltage decreases, the gate voltage on the pull-down is higher than the supply, so the NMOS turns off the clamp faster than would otherwise be possible. The second modification is the modified pull-up network of the first stage. The modification allows for a weak pull-up when the PMOS is off and a strong pull-up when the PMOS is on, while maintaining the average gain of the stage. These changes uniquely benefit system-level ESD designs. In designs that only require component-level ESD protection, the clamp only needs to turn on quickly; if a fast turn-off time is not required, it is more effective to use CMOS inverters sized so that the turn-on path is faster and the turn-off path is slower.

To verify the speed of this clamp, it was simulated during a 0.6 A pulse using the schematic shown in Figure 8.29. The TLP source's rise time filter was varied to determine the minimum fall-time for which the clamp would not cause a serious undershoot. The results of these simulations, shown in Figure 8.33, demonstrate that the clamp will cause undershoot during a 100 ps falling edge, but not a 200 ps falling edge. When attempting to reproduce undershoot caused by supply inductance in measurement or simulation, rise time filters slower than 200 ps should be used with this circuit.

In fact, such undershoot can be reproduced in simulation using the schematic shown in Figure 8.34. This schematic represents the measurement setup that will later be used to reproduce undershoot due to the supply, shown in Figure 8.35. In the measurement setup, a capacitor is connected between the clamp circuit's terminals by connecting one of its (the capacitor) terminals to VDD with a DC needle and the other terminal to one of the RF probe's shields. This method of connection creates some parasitic inductance, which is required to allow undershoot to happen. When the schematic shown in Figure 8.34 is simulated, a large voltage undershoot is observed, as shown in Figure 8.36. This simulation uses a current pulse with 10 ns width, 1 ns rise time, and 0.6 A amplitude. In this simulation, the current initially flows exclusively through the clamp. Because the clamp (when activated) and the decoupling capacitor are both low impedance, the voltage drop across the parasitic inductance is constant; the current to the decoupling capacitor (through the parasitic inductance) increases linearly with time, and the current through the clamp decreases. Once the input current flows only to the decoupling capacitor, the clamp turns off and measured voltage is clamped to the 2.5 V stored on the decoupling capacitor. When the pulse ends, the parasitic inductance pulls the voltage across the clamp negative.

8.6 – Summary and Conclusion

This chapter details a variety of experiments implemented on a 65 nm CMOS test chip. One group of experiments on this test chip includes circuits and experiments on input glitches. This group includes an out-of-range error detector, a glitch counter, various filters to suppress glitches, and glitch detectors at inputs around the chip to study spatial variations in glitches. A second experiment examines the possibility of voltage drops in supply resistance causing errors in transmitter/receiver pairs that are separated by long distances. A third experiment examines

the possibility of latches being disrupted by power supply fluctuations. The last experiment reproduces many of the behaviors described in Chapter 5 and Chapter 6 using standalone rail clamp test structures.

All of the experiments will be performed after the completion of this dissertation; however, the design process of this test chip revealed several interesting results. First, power disruptions on the external supply can propagate to internally regulated supplies by disrupting internal nodes of the regulator and by directly discharging the regulated supply through the regulator's large output transistor. Second, power fluctuations seem unlikely to affect typical latches. A latch's stored data could only be disrupted for large power fluctuations where power is rapidly restored; for such a disruption to occur, the latch also must have an asymmetric capacitive load.

8.7 – Figures and Tables

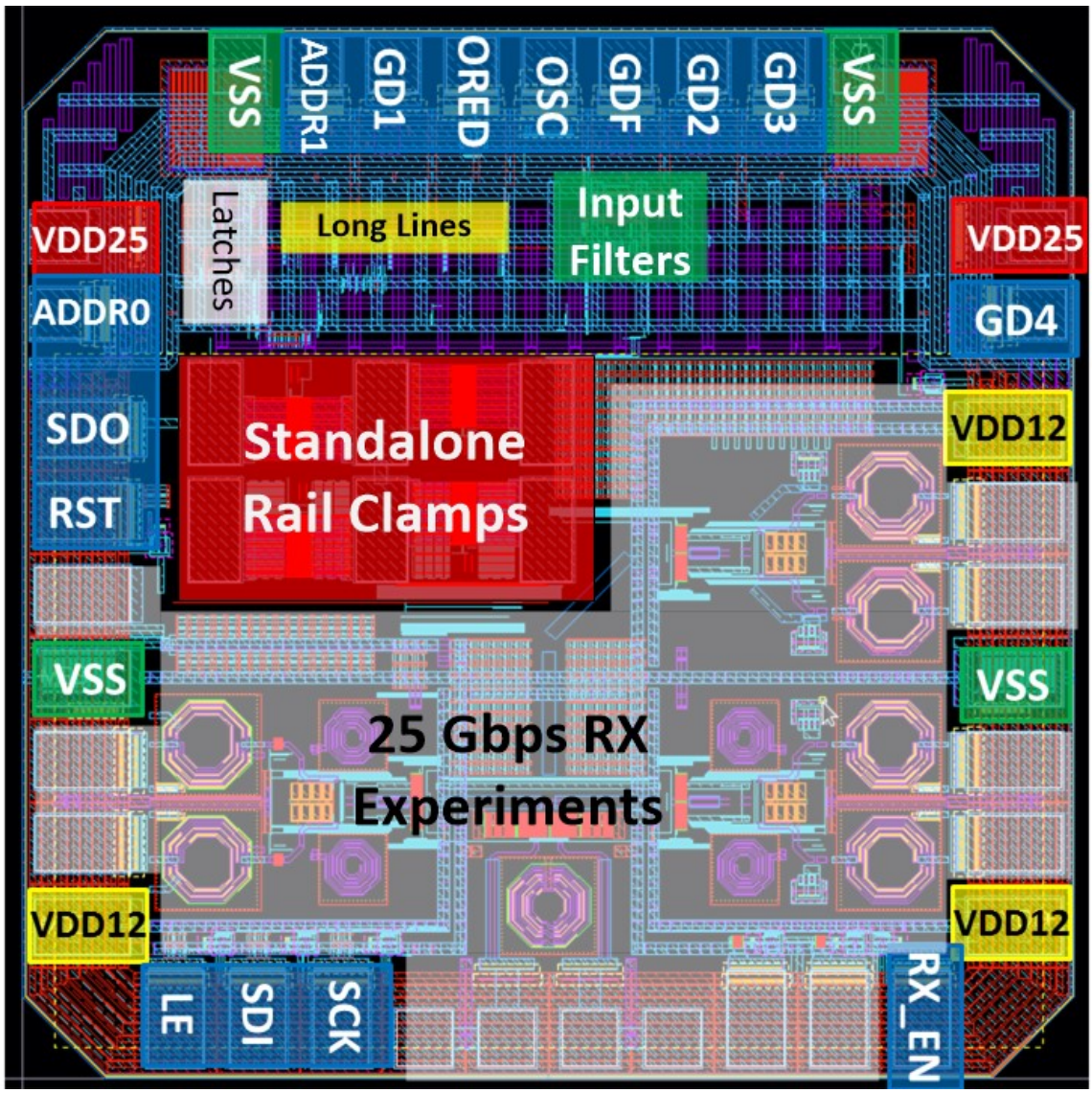


Figure 8.1: Layout of new test vehicle.

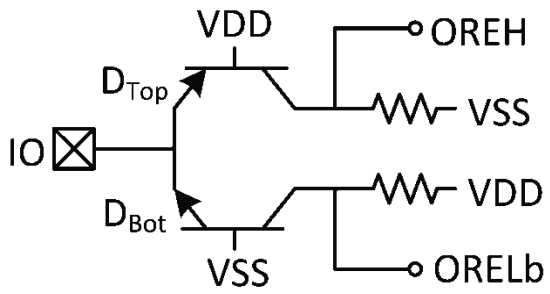


Figure 8.2: Original concept for ORED circuit. Collector diffusions are added to DTop and DBot, allowing the ESD diodes to be used as a common-base amplifier that activates when the IO voltage rises above VDD or falls below VSS.

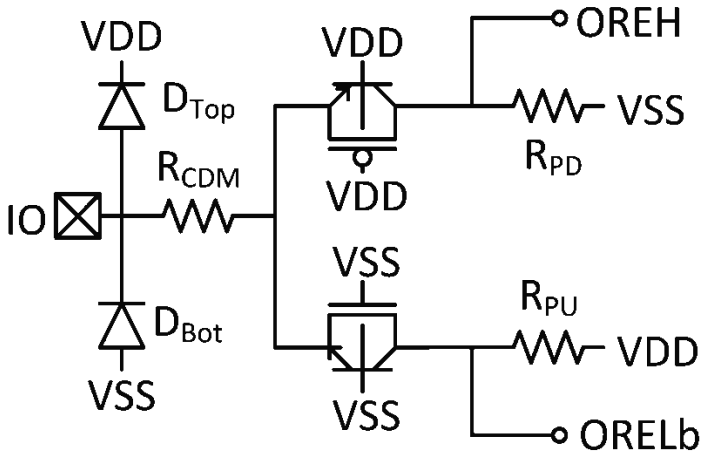
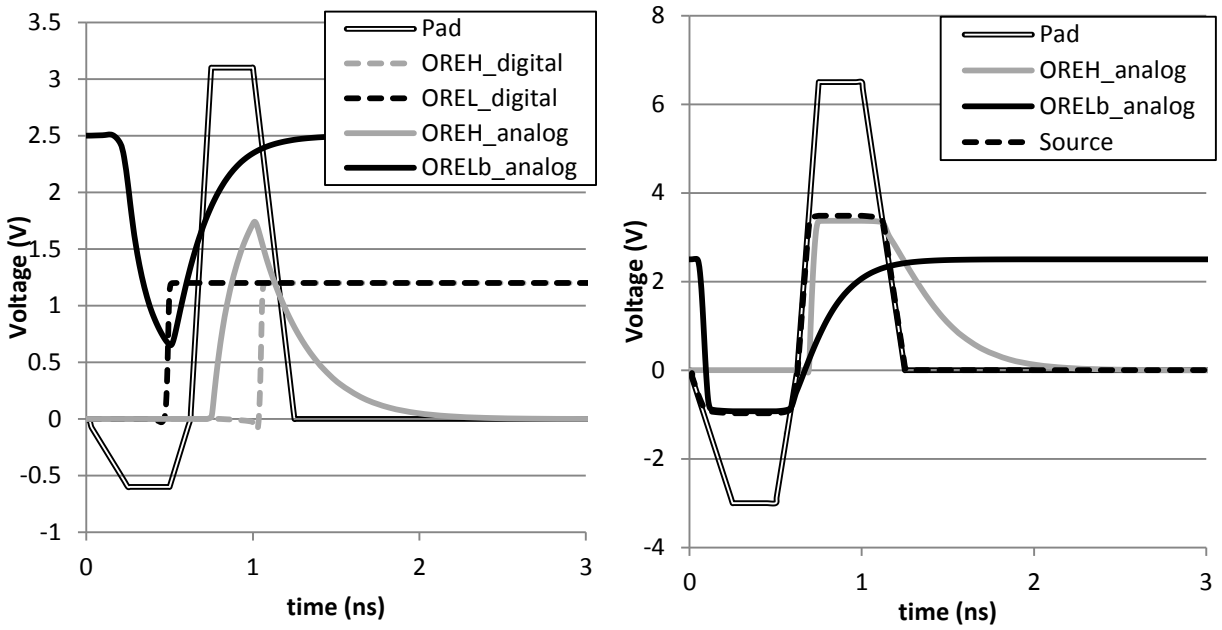


Figure 8.3: Modified ORED circuit using common-gate amplifier. The common-gate amplifier is built into the secondary ESD protection (the secondary ESD diodes are the source-body junctions) so that the gate voltage on the common-gate amplifier (and input buffer) does not become dangerously high.

Table 8.1: Component values used in ORED circuit.

Component	NMOS W/L	PMOS W/L	R_{CDM}	R_{PD}	R_{PU}
Value	6 µm/0.28 µm	12 µm/0.28 µm	182 Ω	33.4 kΩ	33.4 kΩ



(a) (b)

Figure 8.4: Simulated response of the ORED circuit to negative and positive pulses appearing at the pad. (a) Input pulse exceeds each supply by 0.6 V. The ORELb and OREH analog signals do not achieve full swing; however, their swing is sufficient to trigger the SR latches connected each output, producing the OREH and OREL digital signals (which are level-shifted to the core domain). (b) Input pulse goes significantly beyond each supply rail. The OREH and ORELb analog signals achieve full swing. With high input voltages, the node connected to the source of the NMOS and PMOS does not greatly exceed the supply voltage, providing effect CDM protection.

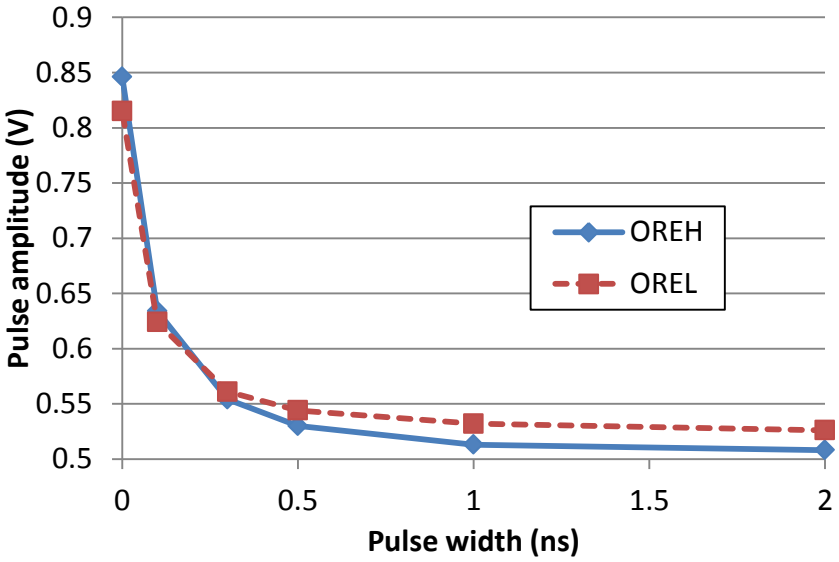


Figure 8.5: ORED sensitivity vs. pulse width. The trapezoidal pulse is at its peak amplitude for the duration listed on the x-axis; the pulses have a fixed 100 ps rise/fall time. The values on the y-axis represent the minimum pulse amplitude that would cause one latch in the ORED to switch. At very narrow pulse widths, the circuit requires a larger amplitude pulse to detect an out-of-range error.

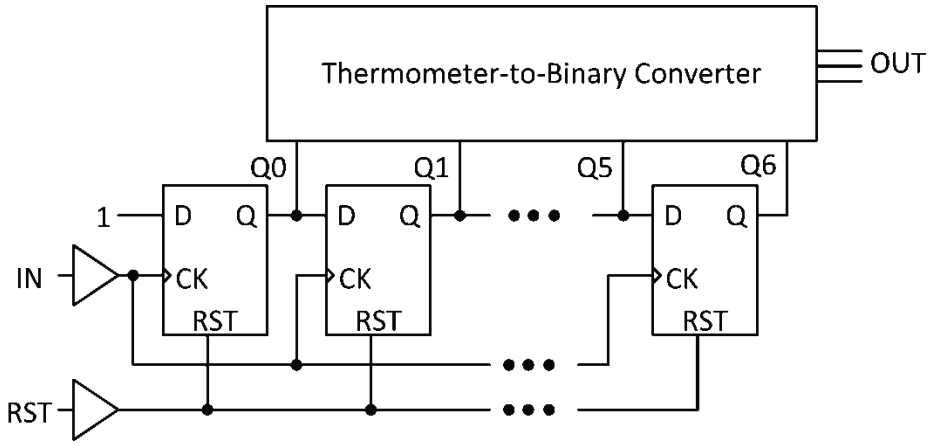


Figure 8.6: Glitch counter schematic. Each of the D-registers uses the schematic shown in Figure 8.7. When reset is high, the output of each latch resets to "0". This circuit is implemented in the core power domain. IN represents the output of the IO circuit after having been passed through a level-shifter between the IO and core supplies.

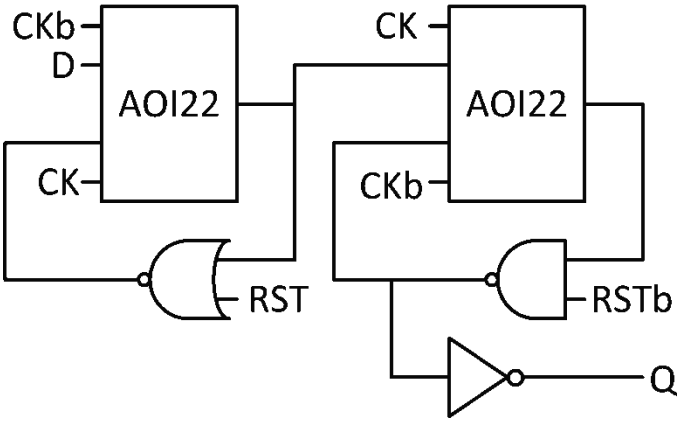


Figure 8.7: Register used in the glitch counter's shift register. In the AOI22 gates, the top two signals are ANDed together, as are the bottom two. The signals CK and RST are provided externally, while CKb and RSTb are generated using inverters. The rightmost AOI22's output should not be used as Q; during edge transitions of CK, clock skew causes a low amplitude (~0.4·VDD) signal glitch at this node that is suppressed by the NAND gate and inverter.

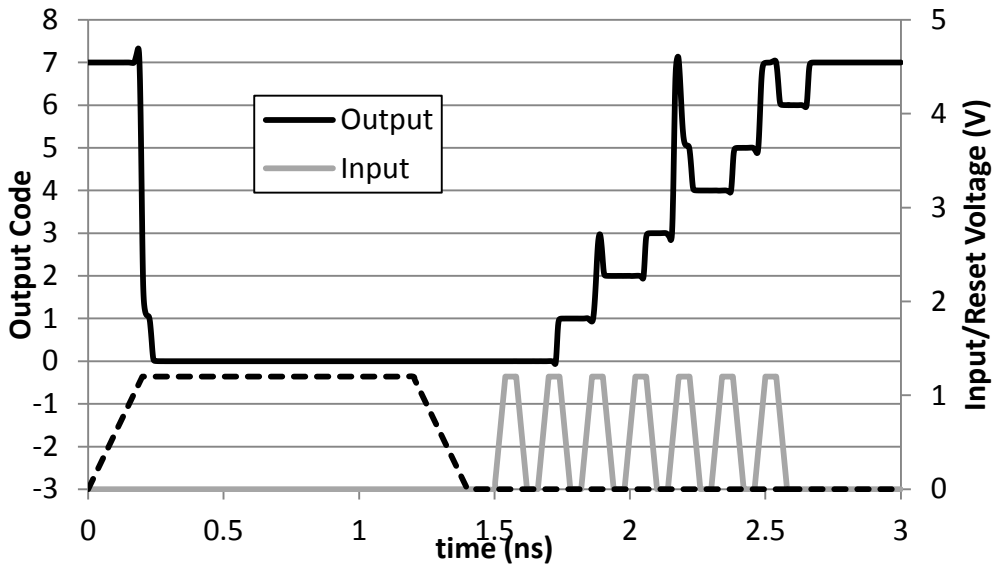


Figure 8.8: Simulated response of the glitch counter circuit. The input signal clocks the shift register at 6.25 GHz with 40 ps rise and fall times. The spikes in the output code are caused by the thermometer-to-binary converter; the more significant bits have a lower propagation delay than the less significant bits. For example, on the transition from 3 to 4, the binary output code goes 011 → 111 → 101 → 100.

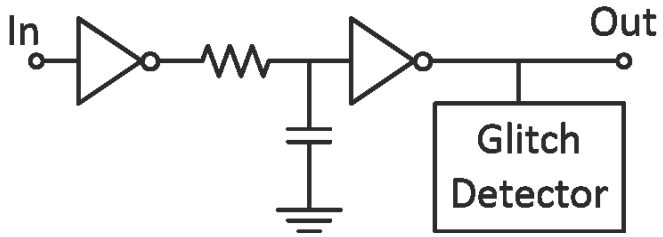


Figure 8.9: Schematic of passive RC filter for glitch suppression. The RC is driven by the buffered input signal. The output of the RC filter is connected to another inverter to restore the output of the RC filter to a clean digital signal. Functionally, the output of this circuit is "Out". On this test vehicle, the output is connected to a glitch detector to determine if the time constant is effective at suppressing glitches.

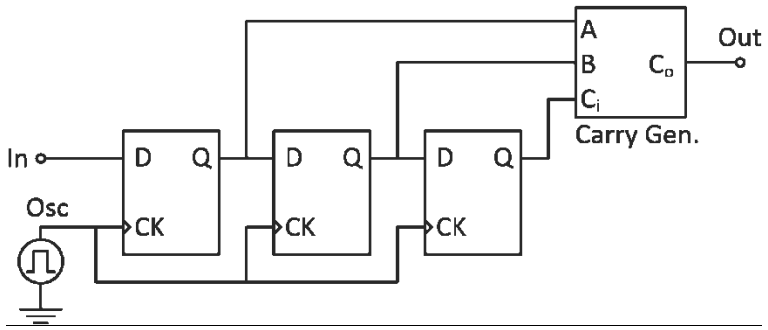


Figure 8.10: Block-level schematic of digital filter. The latches use the schematic shown in Figure 8.7, except the NAND and NOR gates are replaced with inverters, since no reset functionality is needed. The block labeled "Carry Gen." is the circuit shown in Figure 8.11. The clock is provided by an on-chip RC relaxation oscillator shown in Figure 8.12. On the test vehicle, a glitch detector is connected to the output.

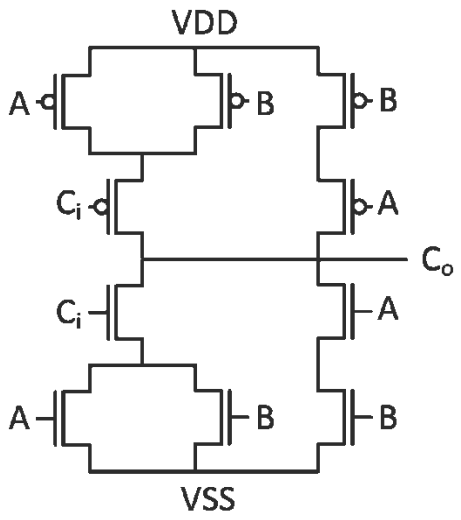


Figure 8.11: Carry generation circuit used in Figure 8.10. This design is the carry generation circuit from a mirror-adder [44].

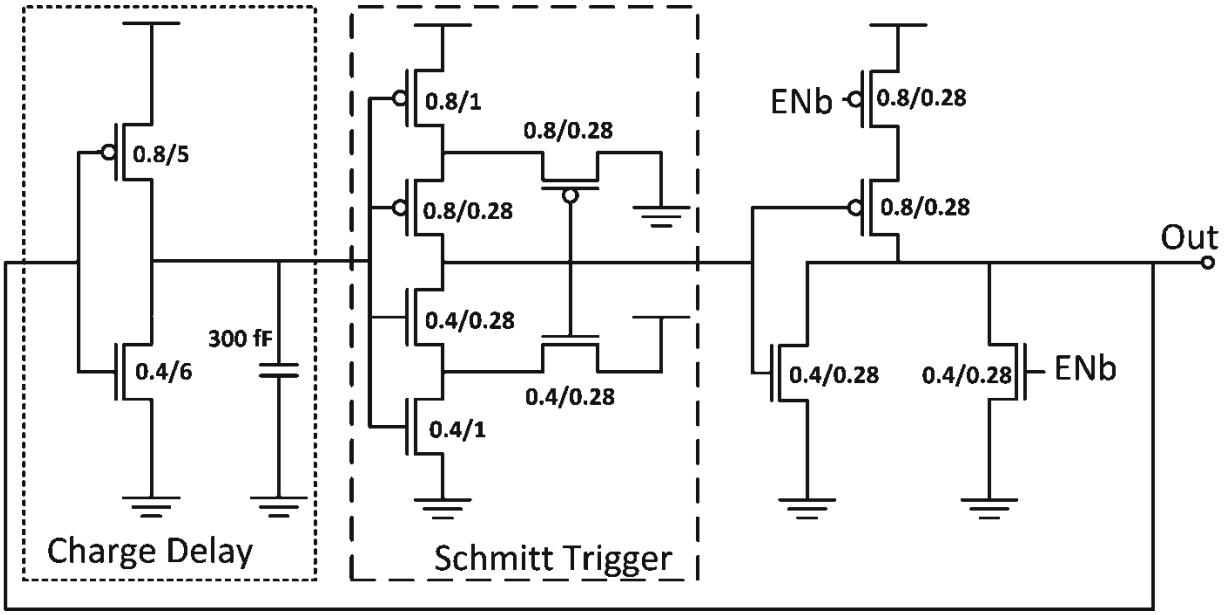


Figure 8.12: On-chip 10 MHz relaxation oscillator used to clock the digital filter shown in Figure 8.10. This circuit runs on the 2.5 V IO supply; the output is level shifted to the 1.2 V domain before being connected to the digital filter. The first stage ("Charge Delay") uses a large capacitive load and long channel MOSFETs to produce a large charging delay. The second stage is a CMOS Schmitt trigger with large hysteresis. The last stage is a NAND gate that provides a means of shutting the oscillator off. Each stage inverts the output of the previous stage; an odd number of stages cause the circuit to oscillate.

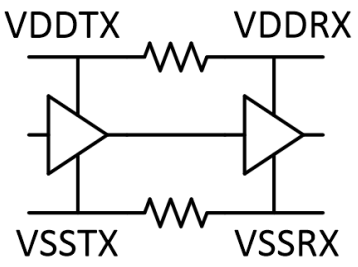
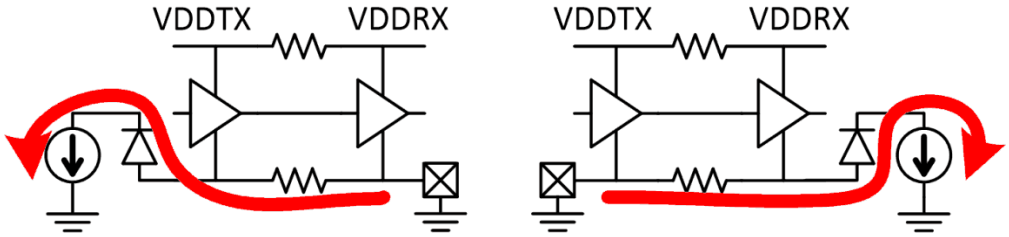
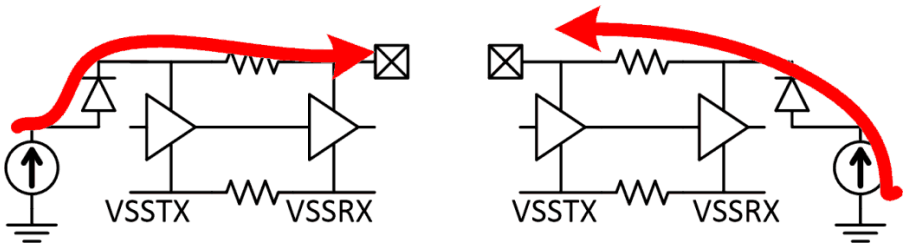


Figure 8.13: Schematic of a driver and receiver where local VDD and VSS are separated by effective bus resistances.



(a) (b)

Figure 8.14: Schematics of current flows during negative IO zaps. (a) Driver near the zap pin and the receiver near the VSS pin. (b) Receiver near the zap pin and the driver the VSS pin.



(a) (b)

Figure 8.15: Schematics of current flows during positive IO zaps. (a) Driver near the zap pin and the receiver near the VDD pin. (b) Receiver near the zap pin and the driver near the VDD pin.

Table 8.2: Summary of possible errors in long lines due to resistive drops in supply buses due to ESD current. Configuration describes the positions of the transmitter and receiver relative to the relevant supply pins. Errors marked with an (*) require the VDD to VSS ESD clamp to turn on, and thus depend on the position of the clamp, as well. Unlikely errors are errors that would require a mechanism other than the one described in this section to occur.

Zap Polarity	Configuration	Possible Errors	Unlikely Errors
Negative	TX near IO, RX near VSS	False “0”*	False “1”
Negative	RX near IO, TX near VSS	False “1”	False “0”
Positive	TX near IO, RX near VDD	False “1”*	False “0”
Positive	RX near IO, TX near VDD	False “0”	False “1”

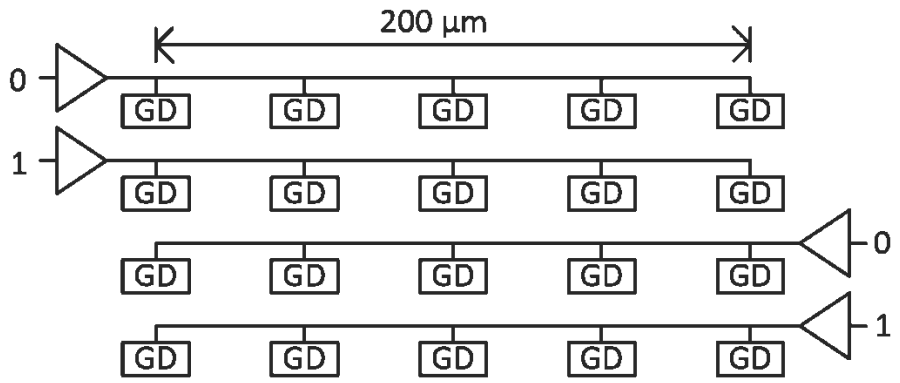


Figure 8.16: Diagram of long line experiment. Each driver has its input tied high or low and drives a 200 µm long line. Glitch detectors are placed periodically along the lines to detect if voltage drops in the supply buses cause logic errors. Each glitch detector taps into the local power grid.

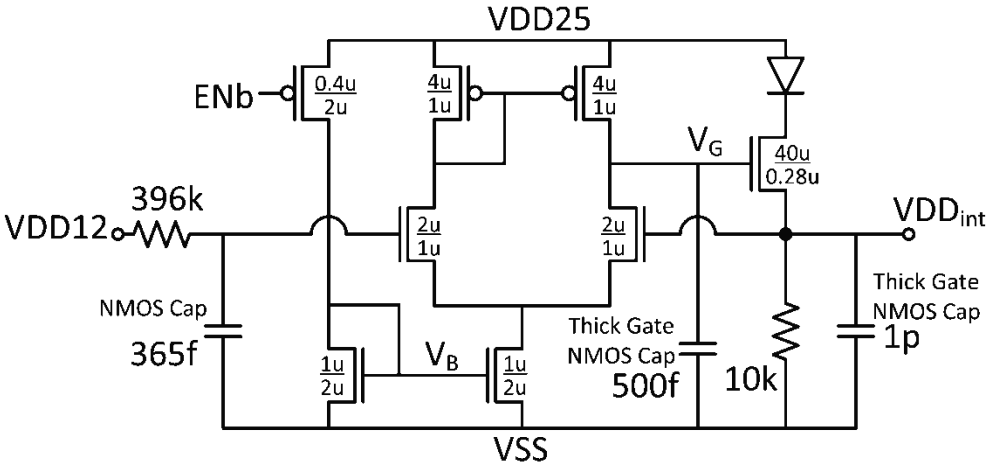
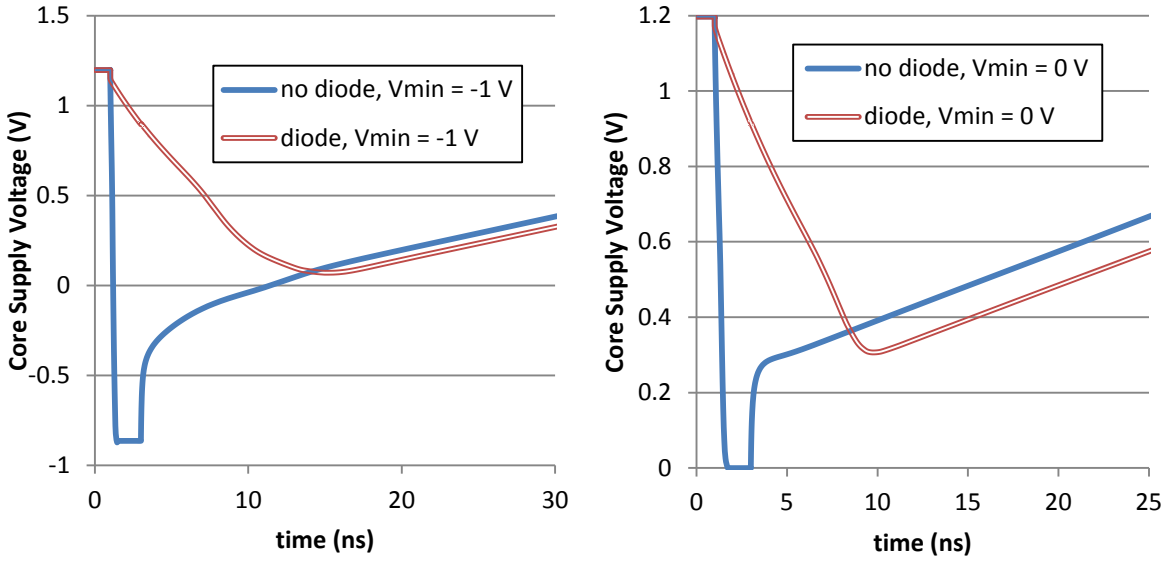


Figure 8.17: On-chip voltage regulator used to power the second and third core power domains. In the regulator for Domain 2, the diode is not present, while in the regulator for Domain 3 includes the diode. The external 1.2 V supply, VDD12, is filtered and used as a reference voltage. The 500 fF capacitor is used to create a dominant pole at V_G, and the 1 pF capacitor is decoupling capacitance for the regulated supply (and the only explicit decoupling capacitor on the supply). The 10 kΩ resistor ensures some current flows through the NMOS output driver so that the output impedance ($1/g_m$) does not become too large. If the output impedance became too large, the output pole would move toward the dominant pole, degrading phase margin.

Table 8.3: Performance metrics of the voltage regulator shown in Figure 8.17 with VDD12 set to 1.2 V.

Loop Gain	40.3 dB
Gain Error @ I_L = 2.5 mA	2%
Gain Error @ I_L = 5 mA	10%
Unity Gain Frequency	16 MHz
Phase Margin (C_L = 0 pF, I_L = 0 mA)	86°
Phase Margin (C_L = 30 pF, I_L = 0 mA)	45°



(a) (b)

Figure 8.18: Simulated output voltages of the regulators with and without the series diode. In these simulations, VDD25 drops from 2.5 V to V_{min} for 2 ns. (a) V_{min} = -1 V, (b) V_{min} = 0 V. Without the diode, the output voltage is rapidly pulled down; with the diode, the 10 kΩ resistor gradually pulls the output down by discharging the decoupling capacitor. When VDD25 drops, node V_G in the regulator is discharged through the drain-body diode of the PMOS connected to that node. Thus, the driver NMOS stays off until the amplifier can recharge the node V_G. Once V_G is recharged, the regulator resumes normal operation and the output voltage begins to return to its nominal value.

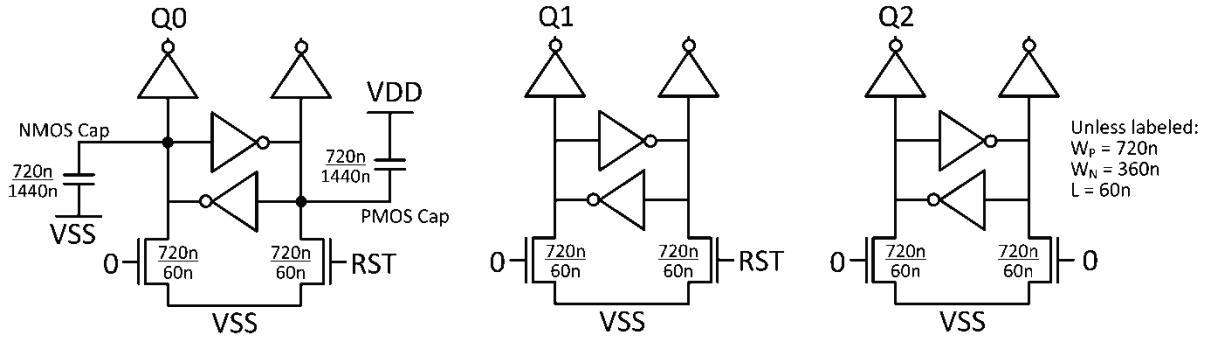


Figure 8.19: Cross-coupled inverter latches. The capacitors in the leftmost latch cause its output to be "1" after power-up. The two left latches output "0" after RST is "1". The rightmost latch has its reset signal hard-tied low, so a control case is available to determine if the RST line is the cause of any observed disturbances.

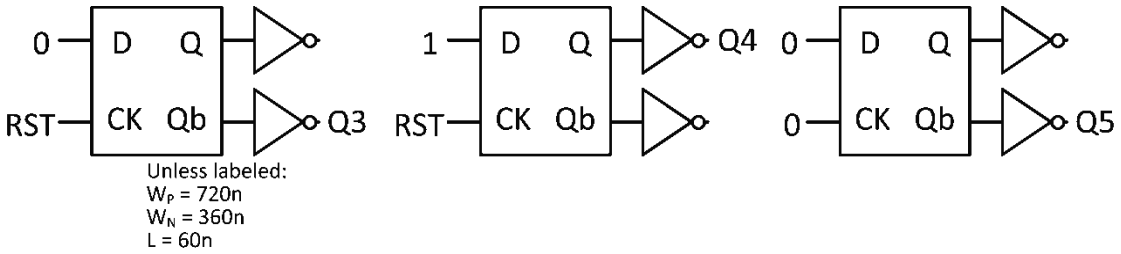


Figure 8.20: D-latch experiments. The schematic of each latch is shown in Figure 8.21. All three latch will power up to unknown states. The two leftmost latches will either be set to a "0" or a "1" after being reset. In either case, the output will be read as "0" after being reset, since the output is taken from a different node in the two circuits. The rightmost latch is a control case to help determine if the reset line is a source of disturbance.

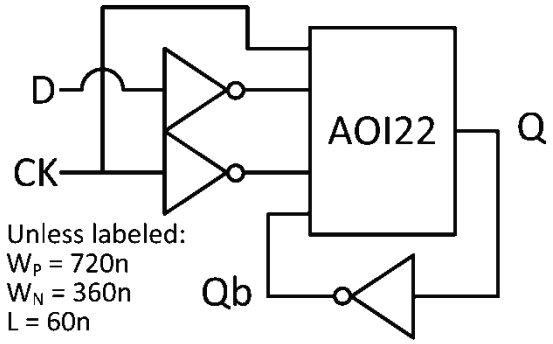


Figure 8.21: Circuit for each D-latch shown in Figure 8.20. The two pairs of inputs that are drawn closer together in the AOI22 gate are ANDed together.

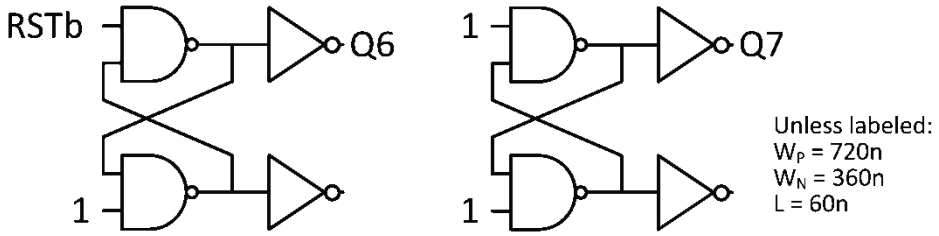


Figure 8.22: SR latch experiments. Both latches power up to unknown states. The left latch outputs "0" after being reset. The right latch is a control case to determine if the reset line is a source of disturbances.

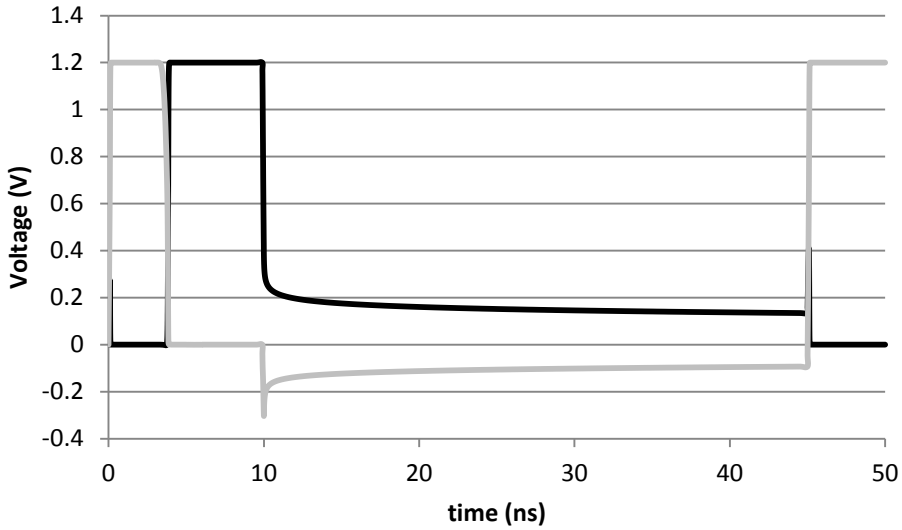


Figure 8.23: Transient showing both internal nodes of latch Q0. The latch is reset at 4 ns, the supply is set to 0 V at 10 ns, and then restored at 45 ns. After the power supply is turned off, the internal nodes of the latch rapidly discharge. After the initial discharge, the previous state is still apparent. When the supply is restored, the coupling capacitors cause the latch to enter the state opposite to its value before the supply was turned off. However, in a symmetric latch, the initial state would likely be preserved during power up.

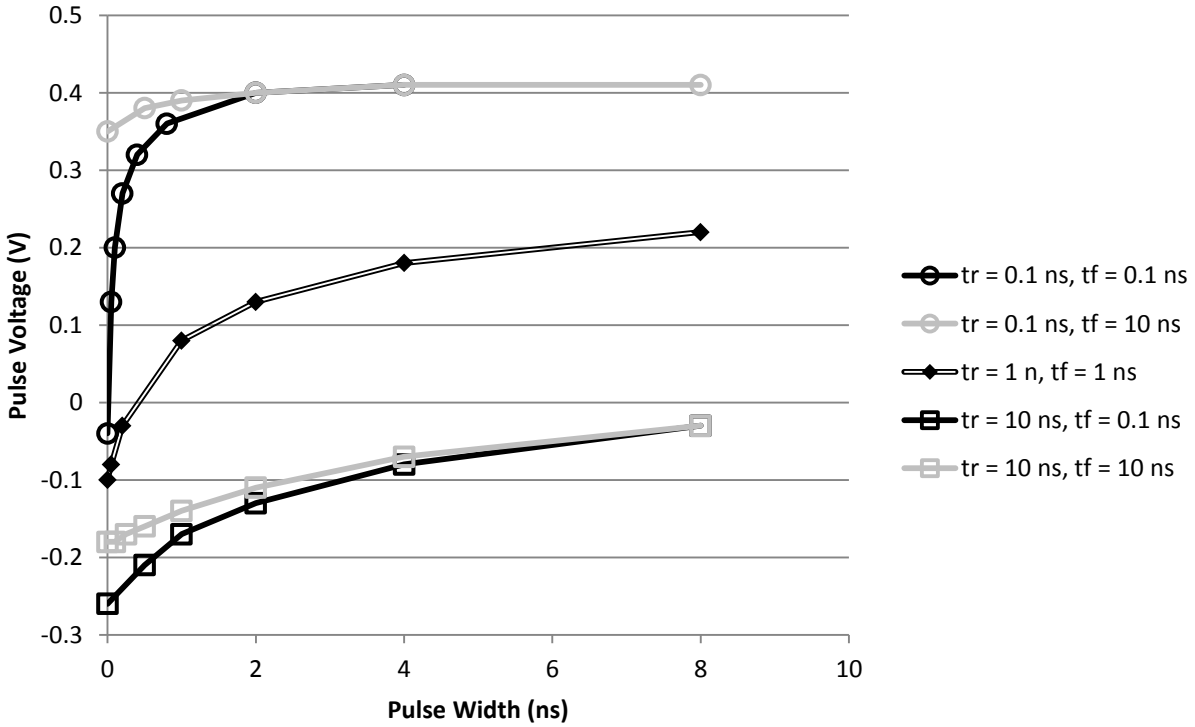


Figure 8.24: Minimum temporary drop in supply voltage required to change the data stored on latch Q0.

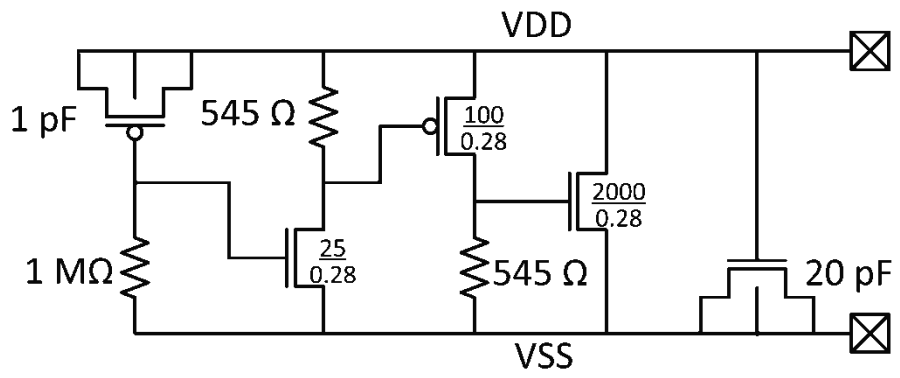


Figure 8.25: Schematic of 2-stage rail clamp circuit in 65 nm CMOS technology using 2.5 V transistors. This circuit was fabricated with and without the 20 pF capacitor as a standalone test structure.

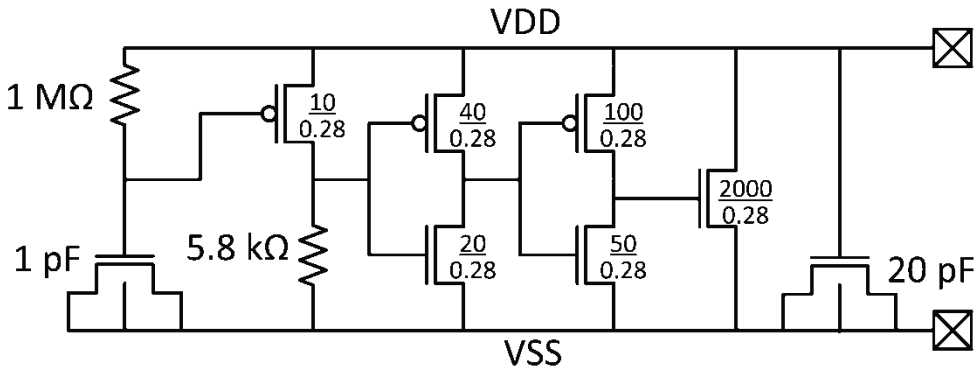


Figure 8.26: Schematic of 3-stage rail clamp circuit in 65 nm CMOS technology using 2.5 V transistors.

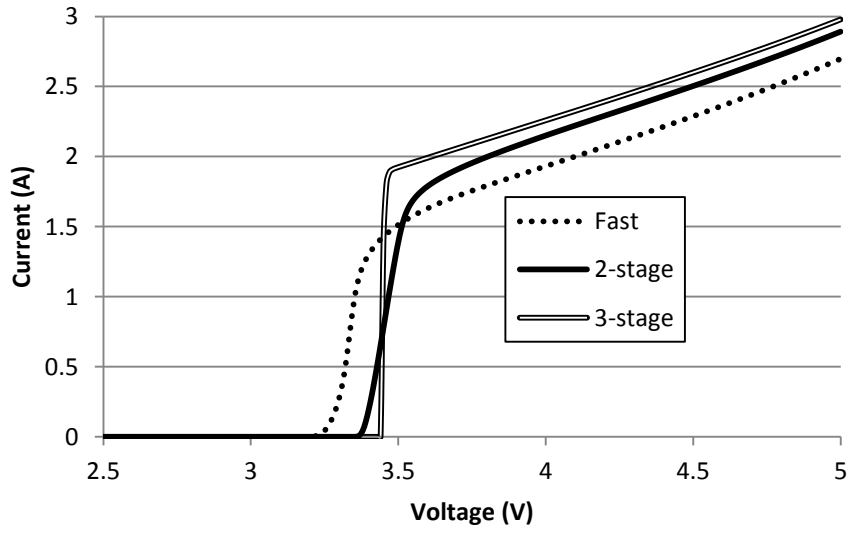
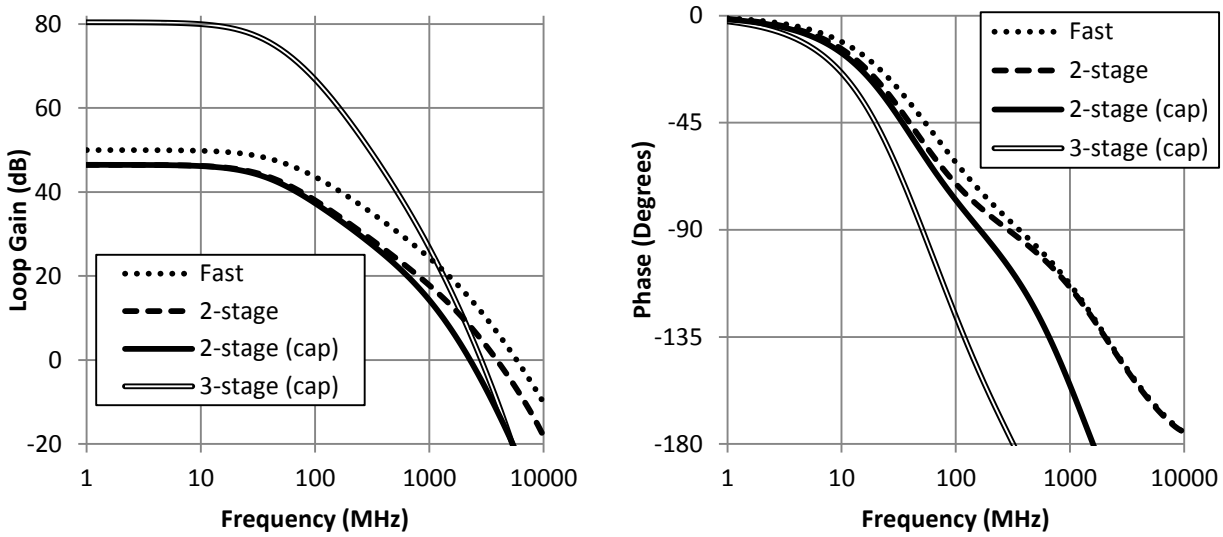


Figure 8.27: Simulated quasi-static I-V of each standalone rail clamp test structure. This simulation is done by replacing the 1 pF timing capacitor with a 2.5 V source and sweeping the supply voltage.



(a) (b)

Figure 8.28: Frequency response of each rail clamp circuit. Adding the capacitor to the 2-stage rail clamp circuit reduces the phase margin to a negative number. The 3-stage rail clamp circuit's gain is too high to make designing a stable circuit practical; this circuit is unstable.

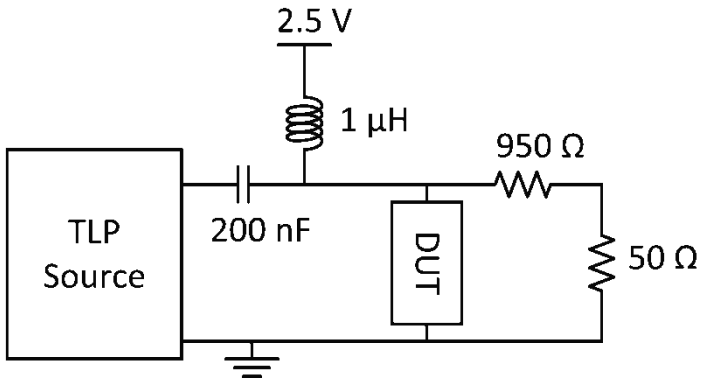


Figure 8.29: Schematic used to simulate the transient response of each rail clamp circuit. This schematic is used to duplicate the measurement setup shown in Figure 8.30. The TLP source is represented similarly to the schematic shown in Figure 3.5 with a 1 ns rise time filter. The device under test (DUT) represents one of the rail clamp circuits. The resistors represent a high-impedance probe and oscilloscope input. The inductor and capacitor allow the TLP pulse to be superimposed on a DC bias.

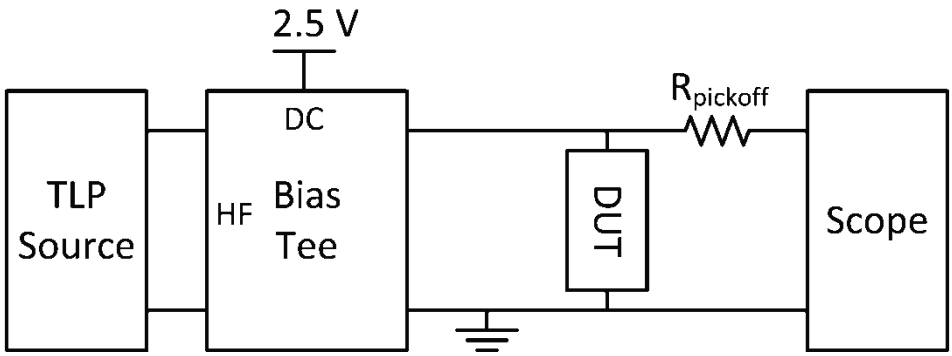


Figure 8.30: Test setup used to measure the transient response of each rail clamp circuit. The device under test (DUT) represents one of rail clamp circuits. A 50 Ω probe connects the DUT to the bias tee and a high impedance probe ($R_{pickoff}$) is connected between the DUT and the oscilloscope (Scope).

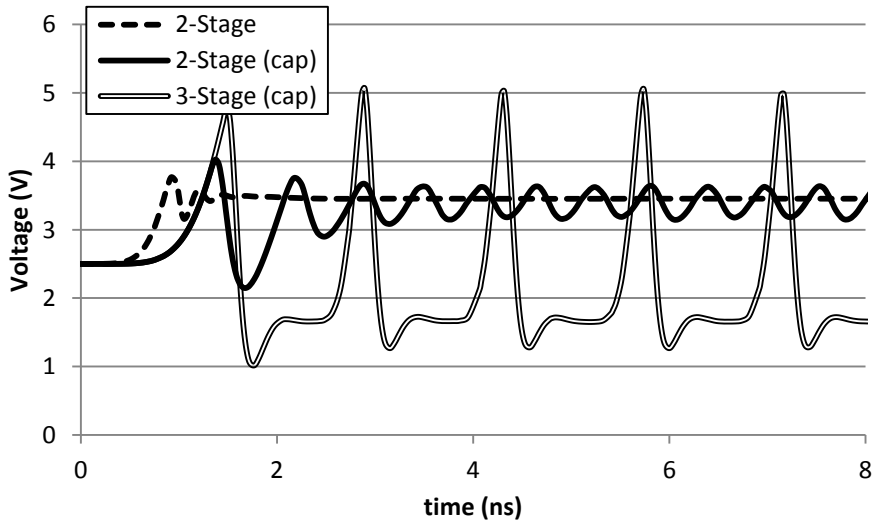


Figure 8.31: Simulated transient response of the 2-stage (with and without the 20 pF capacitor) and the 3-stage rail clamp circuits to a 0.6 A, 1 ns rise time TLP pulse superimposed on a 2.5 V DC bias. These simulations use the schematic shown in Figure 8.29. The 2-stage clamp with the capacitor and the 3-stage clamp are both unstable.

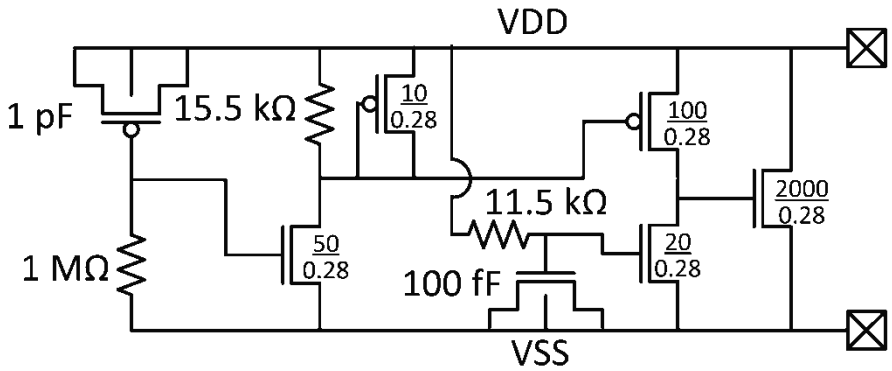


Figure 8.32: Schematic of a 2.5 V rail clamp circuit designed to have very fast transient response. The fast transient response ensures that the circuit will not pull the supply voltage too low during the falling edge of a current pulse.

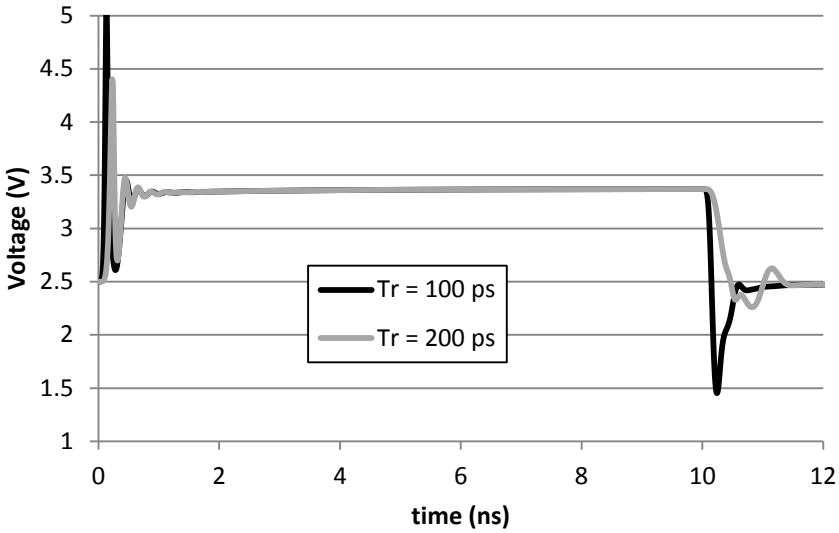


Figure 8.33: Simulated transient response of the clamp shown in Figure 8.32 using the test setup shown in Figure 8.29. The pulse has an amplitude of 0.6 A and a duration of 10 ns. The rise time of the pulse is set to either 100 ps or 200 ps. With a 200 ps rise time, the clamp causes only a small voltage undershoot during the pulse's falling edge.

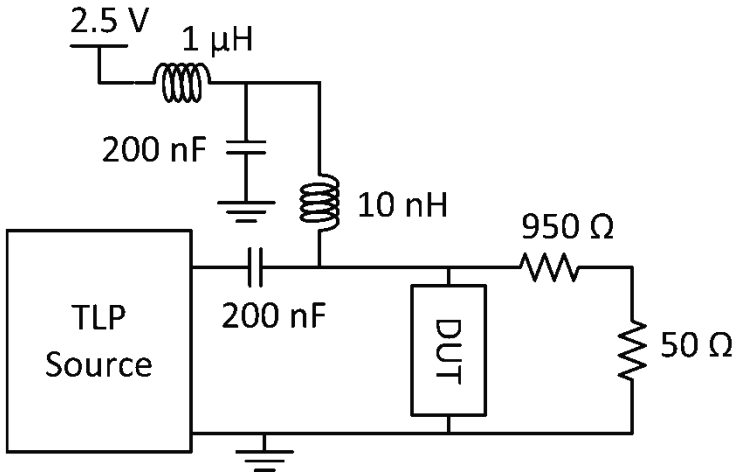


Figure 8.34: Schematic used to predict undershoot due to supply inductance when testing the clamp circuit shown in Figure 8.32 (DUT). The 200 nF capacitor in series with the TLP source represents a DC blocking capacitor. The other capacitor represents a decoupling capacitor connected between the positive terminal of the DUT and the shield of one of the probes. This decoupling capacitor is assumed to have 10 nH of parasitic inductance. The 1 µH inductor is used to separate the DC supply from the capacitor. The TLP source uses a 1 ns rise time filter.

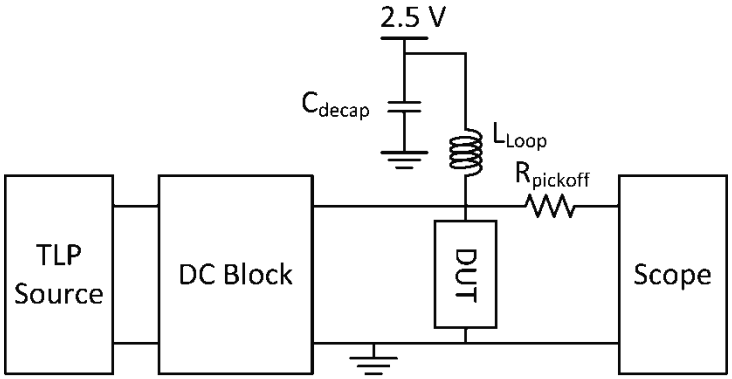


Figure 8.35: Test setup used to demonstrate undershoot cause by supply inductance. The device under test (DUT) represents the rail clamp circuit shown in Figure 8.32. A 50 Ω probe connects the DUT to the DC block and a high impedance probe ($R_{pickoff}$) is connected between the DUT and the oscilloscope (Scope). A decoupling capacitor is connected between one probe's shield and the positive terminal of the DUT, producing a parasitic inductance, L_{loop}. The decoupling capacitor is powered by a DC power supply.

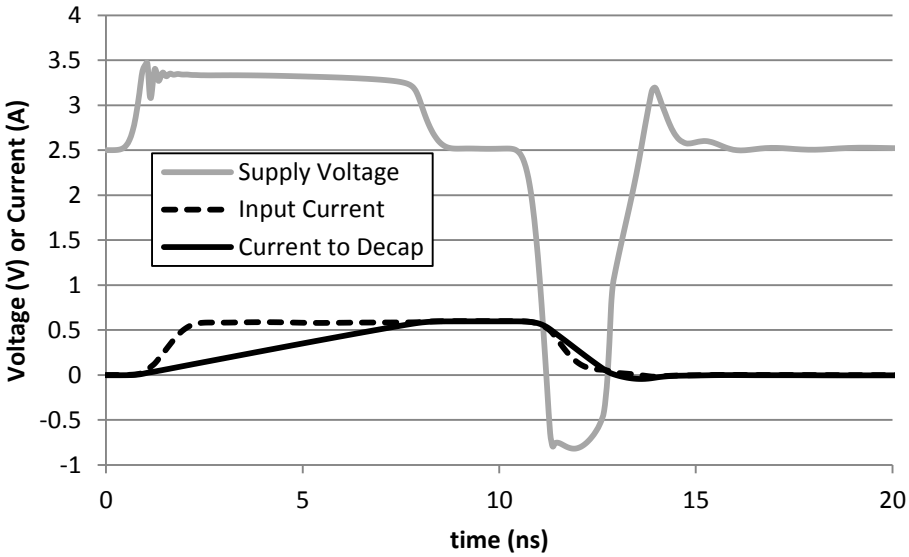


Figure 8.36: Simulation results of the schematic shown in Figure 8.34. The supply voltage across the clamp (DUT) decreases when all of the input current flows to the decoupling capacitor. When the pulse ends, the parasitic inductance to the decoupling capacitor pulls down the voltage measured across the clamp.

Chapter 9 – Summary, Conclusions, and Future Work

9.1 – Summary and Conclusions

This dissertation focuses on modeling and designing for system-level ESD robustness. Chapters 1 and 2 present background relevant to the subject.

Chapter 3 addresses various aspects of the behavior of and modeling of ESD protection devices in silicon. In particular, it presents a simulation model for ESD protection diodes and demonstrates key factors that influence the clamping performance of silicon controlled rectifiers (SCRs). In both diodes and SCRs, the performance is dictated largely by the series resistance in the N-/P-wells in which the devices are formed. This resistance varies with the forward bias on nearby PN junctions; the gradual change in this resistance leads to a non-instantaneous switching process which can increase stress on protected devices. Impact ionization in the N-well/P-well junction was also found to influence the clamping performance of SCR based ESD protection.

Chapter 4 introduces a circuit simulation model for the ESD guns that are used to perform system-level ESD testing. Variants of this model can produce current stress waveforms at the upper and lower limits of the IEC 61000-4-2 specification [1], in addition to replicating the reference waveform. The model is also designed so that it can be used to simulate ISO 10605 waveforms. Additionally, the model was used to demonstrate that small changes in testing environment can dramatically affect the stress waveform applied to a floating device.

Chapter 5 presents an analysis of MOSFET ESD clamps used between supply rails in many ICs. It was found that increasing the gain of these circuits negatively impacts stability, but can improve clamping performance *of the rail clamp circuit*. However, the total clamping performance is usually determined by supply bus resistances, so very high gain is usually

detrimental. In general, there exists a tradeoff between DC clamping voltage, area, response time, and stability.

Chapter 6 demonstrates how system-level ESD can result in severe ground bounce in ICs, leading to power integrity problems. Specifically, large voltage drops the package inductance can cause the chip's supply voltages to vary greatly from the supply voltages on the board that powers the chip. Because of this, a host of problems may arise, such as powering down a domain (which in some cases may cause the ESD protection clamp to stay on after the pulse subsides) or latchup. These effects are not strictly limited to the stressed power domain; they can affect other power domains as well.

Chapter 7 presents experimental results about coupled noise during system-level ESD testing using on-chip noise monitors. It was found that trace-to-trace inductive coupling can produce an input glitch at relatively low precharge voltages, regardless of grounding configuration. The susceptibility of a circuit seems to be independent of the driver strength, though it can be affected by the polarity of the zap and signal level of the driver. ESD zaps to ground can still disrupt signal lines; however, these disruptions occur at significantly higher stress levels. In general, they are less reproducible than trace-to-trace coupling, which suggests some dependence on the measurement setup and possibly testing environment (e.g. humidity may affect spark formation).

Chapter 8 describes experiments designed for a second test vehicle that have mostly not been performed as of the writing of this dissertation. As such, most of the interesting results are not yet available. However, the design process of this test chip revealed several interesting results. First, power disruptions on the external supply can propagate to internally regulated supplies by disrupting internal nodes of the regulator and by directly discharging the regulated

supply through the regulator's large driver transistor. Second, in simulation, brief power fluctuations can affect latches only under extreme circumstances.

9.2 – Future Work

The test chip described in Chapter 8 has not been tested as of the writing of this dissertation; it will provide an excellent starting point for future work on the topic of system-level ESD. The out-of-range error detector circuit and the filter experiment may provide useful tools for detecting or suppressing input signal errors; the glitch counter and glitch detectors placed around the pad ring may provide useful phenomenological studies of how input glitches can affect an IC. The other experiments, including the voltage regulator/latch experiment and long signal line experiment, may demonstrate specific circuits on an IC that are vulnerable to on-chip power supply problems caused by system-level ESD. The standalone rail clamp test structures may provide experimental validation of the analysis presented in Chapter 5 and Chapter 6.

One topic that may provide interesting results is in-situ supply monitors. One significant limitation of this dissertation has been that the on-die supply voltage cannot be measured using conventional measurement techniques. Thus, supply problems have only been demonstrated in simulation, direct measurement in standalone test structures, and indirect evidence from measurement (e.g. the on-board supply disruption shown in Figure 6.4). Direct measurement on a packaged IC would help support many of the findings of this dissertation.

Another topic that could be explored in much greater detail is design practices for preventing malfunction during system-level ESD; this design could be addressed at a circuit, architecture, and even software level. For example, the out-of-range error detector circuit could provide a useful tool for detecting input glitches; however, either it must be integrated into the

architecture to seamlessly suppress errors, or software must be designed to effectively use the information it provides. Similarly, digital filters might be implemented in software to suppress errors without hardware modification, though this approach is completely untested. Additionally, though this dissertation hypothesizes that latches are typically unaffected by power fluctuations, it is unknown whether this result can be generalized to more complicated circuits, e.g. sequential logic circuits. Lastly, this dissertation demonstrates that supply disruption appears inevitable, and can propagate through voltage regulators. However, an appropriate design may be able to minimize the effect on on-die supplies.

One topic that this dissertation has largely neglected is external latchup caused by the large system-level ESD currents. Modern ICs do not necessarily short the wells to the supplies. Instead, they may use more complicated biasing schemes; well resistances, routing resistances, and the resistance of the bias generator could all affect latchup resilience. It is not yet clear what design practices can ensure that a given design will not latch up during system-level ESD testing.

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