SELECTIVE LATERAL NANO-EPITAXY FOR MANUFACTURABLE NANOWIRE ELECTRONICS

BY

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DISSERTATION

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ABSTRACT

This dissertation provides a comprehensive study on vapor-liquid-solid (VLS) growth of III-V planar nanowires and their electronic device applications. III-V materials, especially high-In-content InGaAs, are considered as a very promising n-channel material candidate for post-Si complementary metal-oxide-semiconductor (CMOS) technology due to their excellent electron mobility. Semiconductor nanowires are of interest for electronic device applications primarily due to their 3D nature which facilitates realization of multi-gate field effect transistors (FETs). VLS growth, where a metallic seed nanoparticle is used to gather materials and guide nanowire growth, is a unique bottom-up method suitable for synthesizing extremely thin nanowires with high aspect ratios and axially uniform diameters.

Unlike conventional VLS nanowires which grow along out-of-plane directions with respect to the substrate surface, the recently emerged planar VLS growth produces III-V nanowires self-aligned along certain in-plane crystal directions and epitaxially attached to substrates. This particular type of VLS growth is called Selective Lateral nano-Epitaxy (SLE), where the selectivity is provided by seed nanoparticles. Those planar nanowires are compatible with the well-established planar processing technology and are therefore a potential solution to realizing manufacturable nanowire-based integrated circuits.

In this dissertation, homogeneous GaAs planar nanowire arrays with perfect yield of planar growth, which are ready for practical device and circuit applications, are developed. The array-based GaAs planar nanowire growth also enables systematic growth studies, based on which the underlying mechanism responsible for the planar type of growth is proposed. In addition to homogeneous growth, heterogeneous SLE of high-quality planar InAs nanowires on GaAs is demonstrated. On the application side, GaAs planar nanowire tri-gate MOSFETs and a

current-source loaded amplifier circuit based on nanowire MESFETs are presented. Gate-all-around (GAA) InAs planar nanowire MOSFETs are developed and analyzed.

Chapter 1 discusses the motivation behind researching III-V materials and semiconductor nanowires for future low-power and high-performance nano-electronics.

Chapter 2 introduces the planar type of VLS growth—Selective Lateral nano-Epitaxy—and compares it with the top-down nanowire fabrication technology.

Chapter 3 presents the array-based GaAs planar nanowire growth and detailed growth mechanism studies intended to reveal the underlying reasons leading to the planar version of VLS growth.

Chapter 4 demonstrates GaAs planar nanowire tri-gate n-MOSFETs with Al_2O_3 as gate dielectric material and a high voltage-gain amplifier circuit based on GaAs planar nanowire MESFETs.

Chapter 5 presents the growth and material characterizations of heterogeneous InAs planar nanowires on GaAs substrate. InAs nanowire GAA MOSFETs are then presented with detailed device analysis.

Chapter 6 outlines several future research directions including InAs nanowire MOSFET performance improvement, heterogeneous InAs planar nanowire growth yield improvement, and heterogeneous integration of different types of nanowires.

To my mother, father, and my wife

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CHAPTER 1 – III-V NANOWIRES FOR FUTURE NANO-ELECTRONICS

III-V compound semiconductor materials, especially InGaAs, have very high electron mobility (μ_n) compared to Si. They have historically been used in high-speed field-effect transistors (FETs) for radio-frequency (RF) applications. Recently there has been a growing interest in applying III-V channels in metal-oxide-semiconductor (MOS) logic devices. This chapter reviews the potential of III-V materials, particularly in the form of nanowires, for future logic and RF applications, serving as the underlying motivation for the research on various aspects of III-V nanowires in the present dissertation.

1.1 Benefit of a high mobility channel

InGaAs, with very light electron effective mass (m^*), is the most widely used high-electron-mobility III-V material for RF applications. The low-field electron mobility, μ_n, generally increases with In content. A remarkably high μ_n of ~30,000 $cm^2/V{\cdot}s$ can be routinely measured from planar AlSb/InAs heterostructures at room temperature [1], which is to be compared with 1,300 $cm^2/V{\cdot}s$ in a lightly doped n-type bulk silicon or several hundred in $cm^2/V{\cdot}s$ in the inversion layer at a SiO_2/Si interface [2]. In a short channel device, high electron mobility translates to a high electron carrier injection velocity (v_{inj}) [3]. The ballistic velocity, which serves as the upper limit of v_{inj}, of a non-degenerate 2D channel can be written as $\sqrt{2k_BT/\pi m^*}$ where T is the temperature [4]. The ballistic velocity in III-Vs is much higher than that in Si due to their light m^*. In addition, devices with high-mobility III-V channels generally operate closer to the ballistic limit than Si devices for a given gate length [3]. Therefore, III-V devices usually exhibit significantly higher v_{inj} than Si. A v_{inj} approaching 4×10^7 cm/s has been

extracted from planar InAs high electron mobility transistors (HEMTs) [5], which is to be compared with ~1.0×10^7–1.5×10^7 cm/s in a silicon n-MOSFET [3]. The high v_{inj} ensures the superb frequency performance of those III-V FETs since the intrinsic current-gain cutoff frequency (f_T) can be written as [6]

$$f_T = \frac{v_{inj}}{2\pi L_g} \tag{1.1}$$

where L_g is the gate length.

Table 1.1: Parameter and performance comparison between Si and III-V FETs

	III-V	Si
Supply voltage V_{dd} (V)	0.5	1.0
Intrinsic gate delay τ (ps)	0.5*	0.8*
Gate capacitance C_g (μF/cm^2)	1.5†	3.4†

* both numbers are taken from Ref. [7] with gate length L_g = 40 nm.

† both numbers are calculated based on SOI-like structures with 10 nm $In_{0.53}Ga_{0.47}As$ and 10 nm Si, respectively. The equivalent oxide thicknesses (EOT) are both 0.6 nm.

In terms of logic device applications, III-Vs are currently receiving intensive interest as a promising n-channel material candidate for post-Si CMOS technology. The continuous performance improvement of Si CMOS technology over the past thirty years has been enabled by the aggressive down-scaling of transistor size and increase of operating frequency, with the growth of power density as a side effect. However, as the device packing density has increased drastically, the power dissipation has now become a major obstacle that prevents further down-scaling and performance improvement [8], [9]. The average active power dissipation on a CMOS chip can be approximately written as [2]

$$P = C\,V_{dd}^{2}\,f \tag{1.2}$$

where C is the total equivalent capacitance on a chip, V_{dd} is the supply voltage and f is the clock frequency. As can be seen, the power dissipation is closely related to V_{dd}. It was shown that if V_{dd} could be scaled down in proportion with the scaling of device physical dimensions, the average power density would be unchanged. However, the down-scaling of V_{dd} has been much slower than the size scaling, and stopped at ~1.0 V for high-performance logic processors [8]. This is because for a given off-state leakage current, the supply voltage needs to be large enough to maintain sufficient drain current which ensures good speed performance. The width-normalized drain current, I_d, of a planar MOSFET can be written as

$$I_d = v_{inj}\,Q \approx v_{inj}\,C_g\,(V_{gs} - V_{th}) \tag{1.3}$$

where Q (C/cm^2) is the channel charge density, C_g (F/cm^2) is the gate capacitance per unit area, V_{gs} is the gate voltage, and V_{th} is the threshold voltage. Therefore with high v_{inj}, III-V materials can potentially deliver similar or even better performance than Si at lower supply voltages. One complication is related to the gate capacitance, C_g, which equals the oxide capacitance (C_{ox}) connected in series with the semiconductor capacitance (C_s). C_s of a III-V material is generally smaller than that of Si due to the small electron effective mass, leading to a reduced total gate capacitance. A numerical comparison of C_g between III-V and Si devices is shown in Table 1.1. Despite a reduced C_g, experimental results have shown that III-V materials could deliver higher on-state current when both are operated at a low supply voltage, V_{dd} = 0.5 V [7]. Another important figure of merit for logic MOSFETs is the intrinsic gate delay, τ, which can be estimated as

$$\tau = C_g V_{dd}/I_{dsat} \tag{1.4}$$

where I_{dsat} is the drain current at $V_{gs} = V_{ds} = V_{dd}$. Given the smaller C_g and larger I_{dsat}, a faster intrinsic gate delay is expected for III-Vs. A comparison of τ between the state-of-the-art planar III-V device and commercial Si n-MOSFETs at L_g = 40 nm is shown in Table 1.1. Because of all those facts mentioned above, lots of attention has recently turned to III-V materials for their potential in future low-power and high-performance logic applications [10], which have been the territory of Si for decades.

1.2 Multi-gate transistors

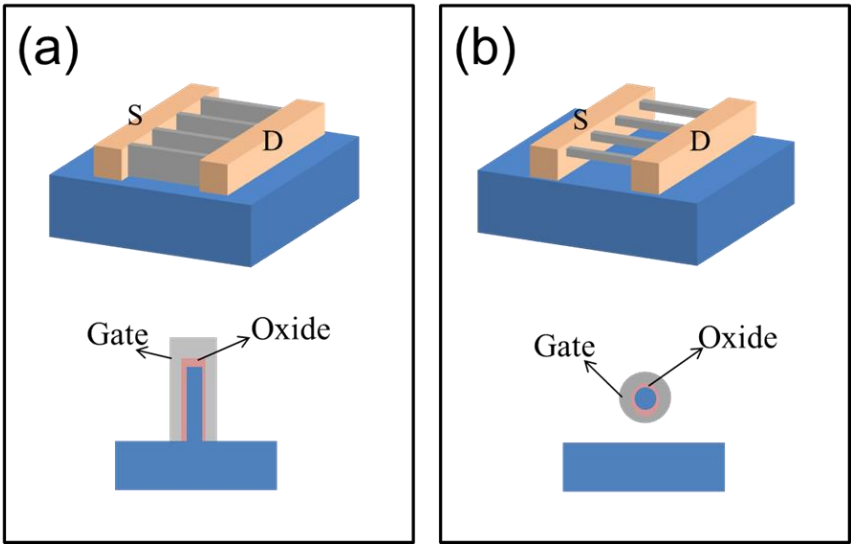

Figure 1.1 (a) Schematic diagram of a FinFet (top) and its cross section (bottom) and (b) schematic diagram of a cylindrical nanowire gate-all-around MOSFET (top) and its cross section (bottom). A FinFET is essentially a double-gated device if the width is much smaller than the height.

The evolution of device geometrical structure has been another important aspect in the CMOS scaling. Traditional CMOS transistors have a planar channel structure with a single top gate. Devices with multi-gate structures, such as double-gate, tri-gate and gate-all-around (GAA) MOSFETs (shown in Figure 1.1), have improved gate electrostatics, *i.e.*, better immunity to

short-channel effects, compared to planar devices and therefore are more attractive for device scaling for the sub-20 nm technology nodes. A geometry-related parameter called natural length, λ, can be defined to characterize the scaling property [11]. The short-channel subthreshold slope (SS) and drain-induced barrier lowering (DIBL) are largely determined by the ratio between L_g and λ. If the gate length, L_g, is no less than six times as much as λ, the device is nearly free of short-channel effects [11]. For a single-gate thin-body device, λ can be expressed as [11]

$$\lambda_1 = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} t_s} \tag{1.5}$$

where ε_s, ε_{ox} are the dielectric constants of the semiconductor and the oxide, respectively. And t_{ox} and t_s are the thicknesses of the oxide and the semiconductor thin body, respectively. For a double-gate device [11] (a FinFET is essentially a double-gated device if the width is much smaller than the height),

$$\lambda_2 = \sqrt{\frac{\varepsilon_s}{2\varepsilon_{ox}} t_{ox} t_s} \tag{1.6}$$

where t_s now refers to the width of the fin. For the nanowire GAA structure with a square-shape cross section [11],

$$\lambda_3 \approx \sqrt{\frac{\varepsilon_s}{4\varepsilon_{ox}} t_{ox} d} \tag{1.7}$$

where d is the width of the nanowire. The natural length of a tri-gate device is between λ_2 and λ_3. It can be seen that given the same t_{ox} and the same channel lateral dimensions, *i.e.*, the width of a nanowire, the width of a fin, and the thickness of a thin body, the natural length decreases as the number of gates increases. A smaller natural length means a better scaling property. In other words, for fixed lateral dimensions, a multi-gate structure allows devices to be scaled to shorter L_g while maintaining an acceptable short channel effect.

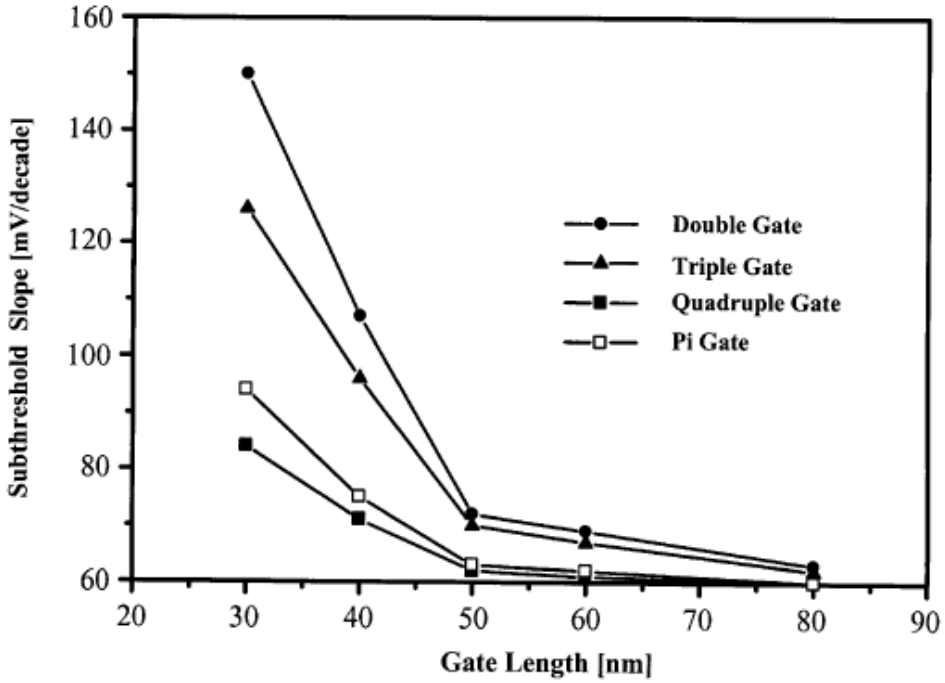

Figure 1.2 Subthreshold slopes as a function of gate length in Si MOSFETs with various multi-gate structures. The lateral dimensions are all 50 nm and t_{ox} = 3 nm. The quadruple gate is here is essentially GAA. Reprinted from Ref [12], Copyright (2004), with permission from Elsevier.

Figure 1.2 shows the simulation results done by J.-P Colinge [12] on Si MOSFETs to illustrate the benefit of multi-gate structures. As the gate length scales down, the subthreshold slope of all structures increases from the ideal room-temperature number (~60 mV/dec). SS increases slower for devices with more gates, which allows the implementation of a shorter L_g. The nanowire GAA structure (referred to as Quadruple Gate in Figure 1.2) has the best scaling property among all.

In terms of RF transistors, the improvement of gate electrostatics enabled by multi-gate structures is also beneficial in the way that the output resistance (R_{ds}) of a device can be enhanced. This could eventually lead to the increase of the maximum oscillating frequency, f_{max} [13], which can be related to f_T as [14]

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}\left(R_G + R_i + R_S\right) + 2\pi f_T R_G C_{gd}}} \tag{1.8}$$

where g_{ds}, R_G, R_i, R_s and C_{gd} are the output conductance, gate resistance, channel resistance, source series resistance and gate-drain capacitance, respectively. As seen from (1.8), given similar f_T and other parameters, a reduced g_{ds} (enhanced R_{ds}) leads to an increase of f_{max}.

CHAPTER 2 – SELECTIVE LATERAL NANO-EPITAXY

2.1 Introduction to VLS nanowire growth

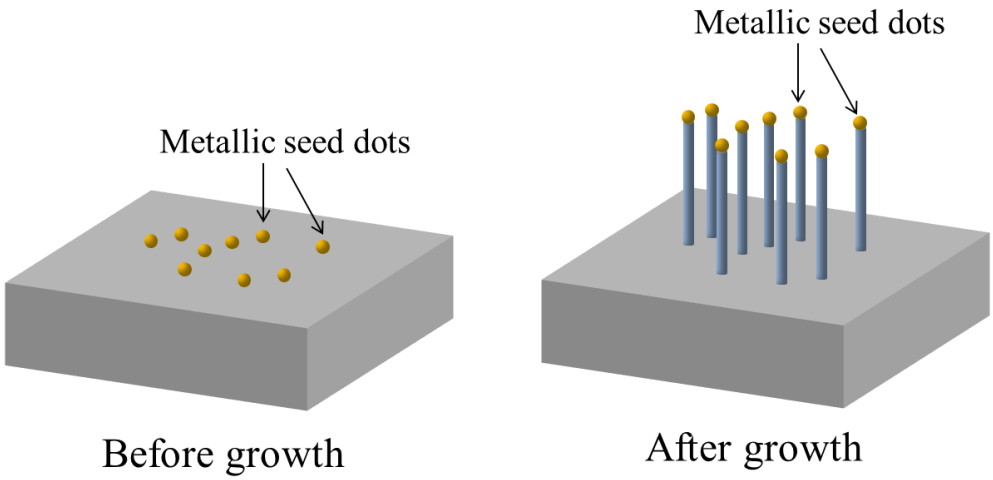

Figure 2.1 Schematic diagrams illustrating the VLS growth mechanism on a (111) substrate. The metal seed nanoparticles (usually made of Au) are first dispersed on the substrate (left). As the nanowires grow, the seed particles are elevated from the substrate surface (right).

Vapor-liquid-solid (VLS) growth, first introduced by Wagner and Ellis [15], is a bottom-up approach for semiconductor nanowire synthesis. As illustrated by Figure 2.1, metal seed particles, usually made of Au, are used to catalyze and direct the nanowire growth usually in a metal-organic chemical vapor deposition (MOCVD) reactor or molecular beam epitaxy (MBE) system. The seed nanoparticles can be either colloidal metals or patterned on the substrate surface by lithography. At a certain temperature, the growth species of the target semiconductor, which come from the **vapor**-phase precursors, enter the metal seed particle and a supersaturated eutectic droplet (**liquid** phase) can be formed. Trimethylgallium (TMGa), Trimethylindium (TMIn), AsH_3, and PH_3 are the most commonly used precursors for III-V VLS growth in a MOCVD system. As the growth species are continuously supplied, they precipitate from the

supersaturated droplet in the form of a **solid**, single-crystal semiconductor nanowire. The VLS growth temperature is usually substantially lower than that of conventional thin-film growth. Therefore, the thin-film deposition rate during VLS growth is heavily suppressed due to reduced pyrolysis efficiency. But thanks to the enhancement effect of seed nanoparticles (either catalytically or kinetically), the nanowire growth can reach a very high growth rate (in terms of length per unit time).

III-V nanowires tend to grow along <111>B directions for energetic reasons [16]. Therefore, vertically aligned nanowires can be observed if a (111)B substrate is used, which is the case shown in Figure 2.1. Slanted, out-of-plane nanowires normally occur on substrates with other orientations.

2.2 Planar VLS growth: Selective lateral nano-epitaxy

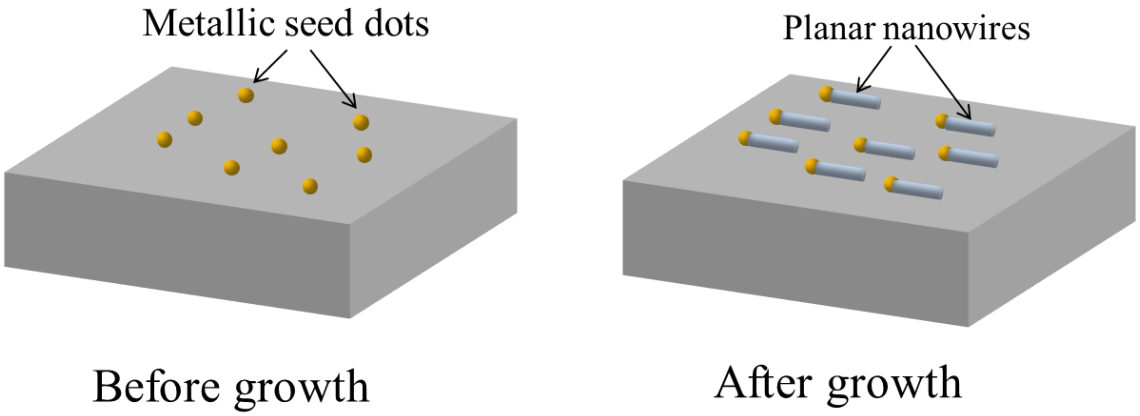

Figure 2.2 Schematic diagrams for the illustration of planar VLS growth, which is called selective lateral nano-epitaxy. The unidirectional III-V nanowires can be achieved by growing on a (110) substrate.

In direct comparison to the conventional out-of-plane VLS nanowires, our group has discovered that under particular growth conditions in a MOCVD system, the VLS growth can

occur in a planar manner when a non-(111) substrate is used [17]. This is illustrated by Figure 2.2, where the nanowires grow in a self-aligned fashion along certain crystalline directions that are in-plane with the substrate surface. The nanowires are epitaxially attached to the substrate, shown by the TEM analysis of GaAs planar nanowires grown on GaAs (100) [17]. We call this particular kind of VLS growth **Selective Lateral nano-Epitaxy** (SLE), which will be used hereinafter interchangeably with "planar VLS growth". Unlike the conventional selective-area growth where an amorphous growth mask is used to partially cover the crystalline substrate surface [18], the selectivity in SLE is provided by the seed nano-particles, which move laterally on the surface as the nanowire growth proceeds.

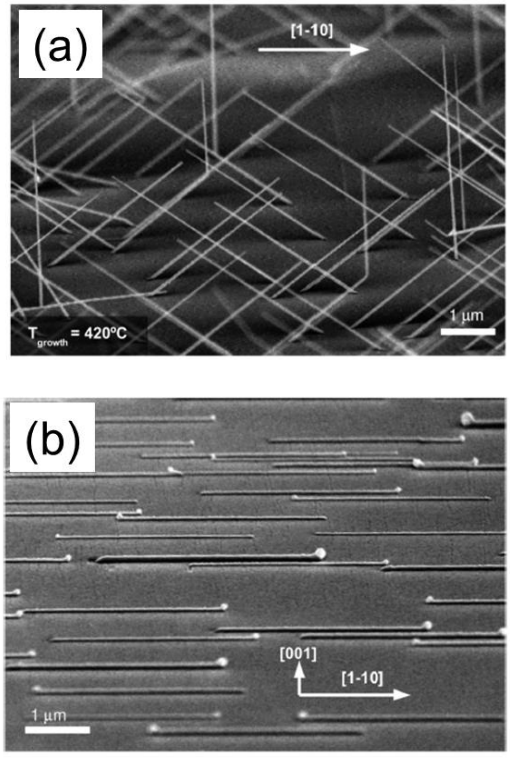

Figure 2.3 SEM images of VLS-grown GaAs nanowires on GaAs (100) substrates. (a) Out-of-plane nanowires and (b) planar nanowires. The Au seeds are visible on the tips of the planar nanowires. Adapted with permission from Ref [17]. Copyright (2008) American Chemical Society.

Figure 2.3 shows representative SEM images of the out-of-plane and planar GaAs nanowires grown on GaAs (100) substrates [17]. The growth was seeded by colloidal Au nanoparticles which were randomly dispersed on the substrate surface. Figure 2.3(a) shows out-of-plane nanowires observed at the growth temperature T_g = 420 ºC. Most out-of-plane nanowires point at an angle of 35.3º with the substrate surface, which corresponds to <111>B direction. When the growth temperature is increased to 460 ^{o}C (Figure 2.3(b)), planar growth can be achieved.

Detailed studies on the growth directions of planar nanowires have been presented in Refs. [19] and [20]. It is found for GaAs planar nanowires, the growth directions are along the projections of out-of-plane <111>B directions on the substrate surface. Therefore, for the growth on (100) substrate, GaAs planar nanowires randomly pick either [0-11] or [0-1-1] direction because they are the projections of the two equivalent <111>B directions on a (100) surface. This is seen from Figure 2.3(b). Uni-directionally aligned nanowires (along [001]) can be achieved if GaAs (110) substrates are used [19].

2.3 Comparison with the top-down approach

VLS growth, as a bottom-up approach, is to be directly compared with the top-down etching method for III-V nanowire fabrication [21], [22], [23], [24]. As illustrated by Figure 2.4, the top-down approach usually starts with a thin-film heterostructure that is epitaxially grown with a sacrificial layer in the middle. Then, fin-like structures are defined by lithography and dry etching. Finally, the sacrificial layer is selectively etched in order to suspend the nanowires. Many selective etchants are known for the well-studied III-V material system. For example, HF etches high-Al-content AlGaAs against most other III-Vs. HCL etches InP but not III-arsenide.

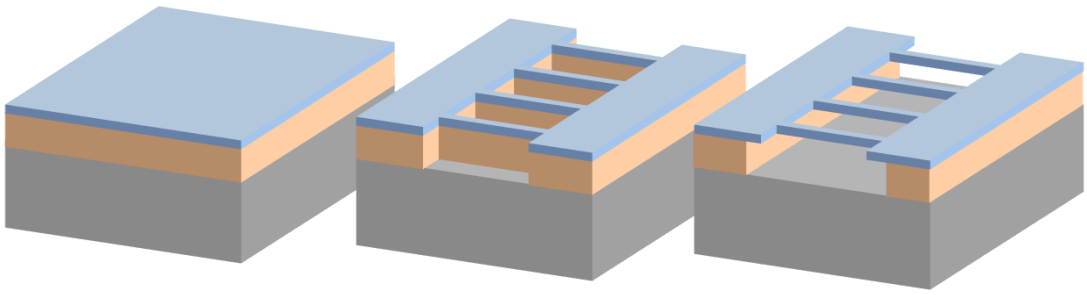

Figure 2.4 Schematic diagrams illustrating the top-down etching method for III-V nanowire fabrication. The middle material serves as the sacrificial layer, which is selectively removed for releasing the nanowires from the substrate.

The top-down approach is prevailing in the industrial manufacturing of semiconductor devices; however, the bottom-up direct growth of nanowires by the VLS method has some distinct advantages. First, as the diameter (or width), *d*, of a VLS nanowire is primarily determined by the size of the seed particle, the diameter downscaling is convenient. With commercial colloidal Au particles of various sizes readily available, sub-20-nm VLS III-V nanowires can be easily obtained [25], [26], [27], [28]. InAs nanowires with $d < 10$ nm have been achieved [29]. VLS growth of nanowires with patterned seed particles can relax the lithographical constraint on achieving ultra-thin wires. The VLS growth starts with the formation of a eutectic seed droplet with approximately semispherical shape, from the solid seed particle. Therefore, the diameter of the nanowire is determined not by the diameter of the original patterned seed dot but by its volume. When the diameter of the seed dots is limited by the lithography method used, it is still possible to scale down the nanowire diameter by reducing the height of the seed dots through, for example, controlling the metal deposition thickness.

Secondly, semiconductor heterostructures, which are routinely applied in planar III-V devices, can be directly incorporated to VLS nanowires in a monolithic growth run to improve the electron transport property [30] and the subthreshold characteristics [31], [32] in a nanowire transistor. For axial heterostructures, they can be done by switching precursors during VLS

growth. For radial heterostructures, they can be realized by switching to the thin-film (vapor-solid) growth mode, usually associated with a temperature ramp-up, after finishing the VLS growth. Such heterostructures cannot be easily implemented on the nanowires fabricated by the top-down etching approach unless a second growth (re-growth) is carried out after the formation of nanowires. However, besides adding processing complexity, this comes at the price of a degraded heterointerface due to the etching damage induced in forming the nanowires.

Lastly and perhaps most importantly, the VLS method offers an attractive solution for the integration of III-Vs on a lattice-mismatched substrate. The top-down approach starts with thin-film growth, which could limit the kind of material one can obtain because of the lattice-matching constraint for growing thin-films. For example, InAs, with very high electron mobility, has a huge lattice mismatch with the commonly available III-V substrates—GaAs and InP. The mismatches are 6.7% and 3%, respectively. The critical thickness for InAs thin-film growth on GaAs is less than 1 nm [33], [34], [35] and it is ~2 nm for its growth on InP [36]. In contrast, more lattice mismatch can be accommodated by a nanowire/substrate heterointerface [37], [38]. Below certain critical diameter [38], high-quality and long nanowires can be grown on highly mismatched substrates without generating axial dislocations. 20-nm-thick vertical VLS InAs nanowires have been realized on Si (11.6% lattice mismatch) [38]. This is particularly attractive when considering integration of different channel materials (for example, InAs for n-channel and GaSb for p-channel) on one single substrate.

One complication with the conventional vertical VLS nanowire is the difficulty in fabricating nanowire transistor devices. Early device demonstrations were done by first breaking nanowires off the growth substrate and then randomly dispersing them onto an insulating substrate such as SiO_2/Si [30], [39]. A non-traditional fabrication scheme, with polymer spacers

to isolate the source (drain) from gate, has been successfully developed to realize vertical nanowire transistors [40], [41]. Nonetheless, its effectiveness still remains to be demonstrated on ultra-thin nanowires ($d \approx 10$ nm) because thin wires might easily collapse during the fabrication process [42]. In addition, the speed performance of those vertical nanowire transistors were heavily affected by the parasitic capacitances because of contact pad overlaps [41], [43].

The planar nanowires by SLE, while offering the same advantages of the VLS method stated above, are completely compatible with the well-established planar processing technology. High-performance metal-semiconductor FETs (MESFETs) and modulation-doped heterojunction high electron mobility FETs (HEMTs) have been demonstrated on GaAs planar nanowires homogeneously grown on GaAs (100) [44], [45]. Those devices have an inherent tri-gate structure that consists of the top and two sidewall facets of the planar nanowire. In this dissertation, in addition to homogeneous SLE, heterogeneous SLE of InAs planar nanowires, as well as the gate-all-around (GAA) MOSFET devices based on them, is presented.

CHAPTER 3 – ARRAY-BASED HOMOGENEOUS SLE AND MECHANISM STUDY[†]

3.1 Array-based GaAs planar nanowire growth

Previous growth studies on planar nanowires have all used randomly dispersed colloidal Au nanoparticles as the growth seeds [17], [20], [45]. This method is effective for initial growth study and proof-of-concept device demonstration but cannot be used for any practical applications because the positions of the nanowires cannot be controlled.

In this section, array-based GaAs planar nanowire growth with lithographically defined Au seed dots is demonstrated. Au dot arrays are fabricated by electron beam lithography (EBL) in a Raith eLine system with PMMA 950k A2 resist and the standard lift-off process. As the planar nanowires are epitaxially attached to the substrate, a pristine substrate surface free of polymer contamination is necessary for obtaining reproducible results. A two-step cleaning procedure has been developed. The samples were first soaked in solvent (Remover PG from MicroChem) with sonication for prolonged time (over one hour). Then, the native oxide on GaAs surface was removed by 1:1 HCl:H_2O solution right before the samples were loaded into the MOCVD reactor. This is to ensure any remaining polymer residues are washed away during oxide etching. Both the prolonged solvent cleaning and oxide-removal etching are critically important because, otherwise, non-reproducible results with dominantly out-of-plane nanowires are observed. All the growth runs in this dissertation are done in an Aixtron MOCVD 200/4 reactor. The standard GaAs planar nanowire growth process starts with an oxide-desorption

[†]Some content in this chapter is adapted with permission from Chen Zhang, Xin Miao, Parsian Mohseni, Wonsik Choi, and Xiuling Li, "Site-controlled VLS growth of planar nanowires: yield and mechanism," *Nano Lett.*, vol. 14, no. 12, pp. 6836–6841, Dec. 2014. Copyright (2014) American Chemical Society.

annealing at 625 ºC for 10 min with AsH_3 overpressure. The temperature is then ramped down to the nanowire growth temperature, T_g, which is normally from 450 ºC to 480 ºC. TMGa is then introduced to the reactor to start nanowire growth. After the growth is done, the samples are then cooled down to room temperature usually with continuous AsH_3 overpressure.

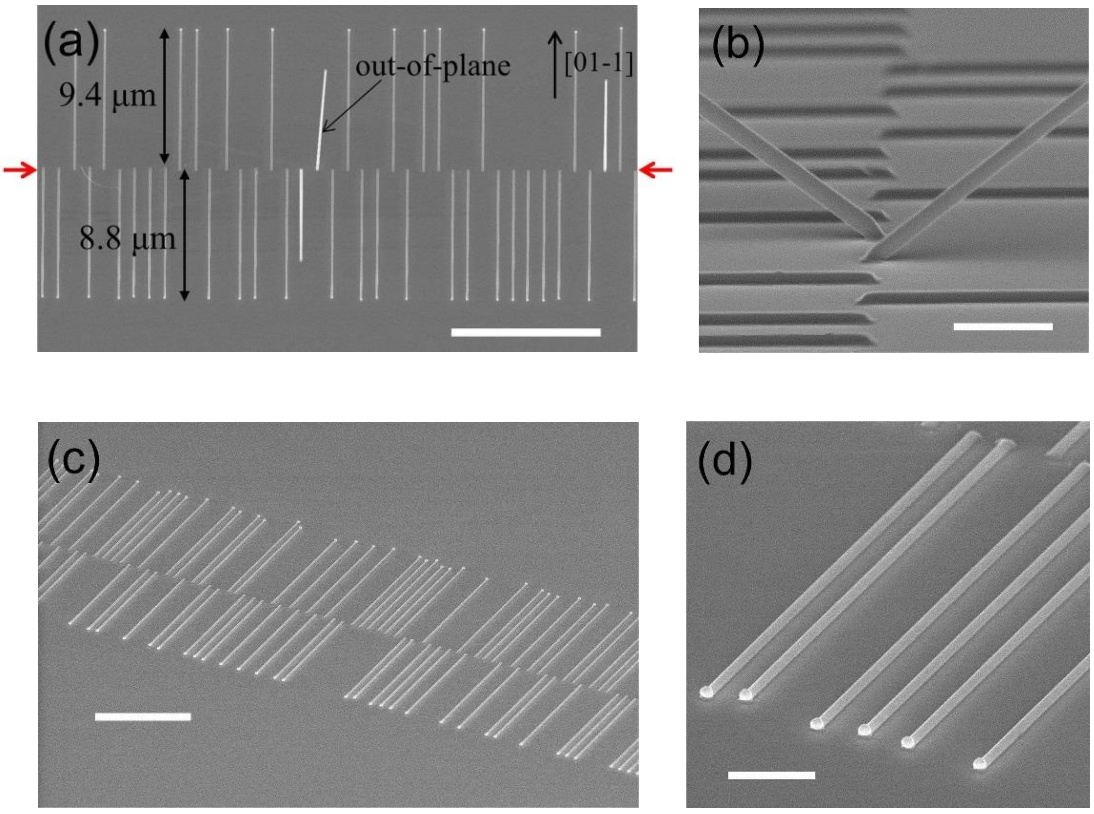

Figure 3.1 SEM images of GaAs planar nanowire arrays grown on GaAs (100) substrates. (a) Top-view SEM image of a representative GaAs planar nanowire array on a (100) substrate. The three brighter nanowires are out-of-plane as indicated. The nanowire bottom width (trapezoidal cross-section) of this particular array is 145 nm. (b) 80º tilted-view SEM image of the same sample in (a) clearly showing two out-of-plane nanowires. (c) 60º tilted view of a planar nanowire array with perfect yield of planar nanowires achieved by optimizing the growth. (d) Higher magnification view of the same array in (c). The scale bars are 10, 1, 5, and 1 μm for (a) – (d), respectively.

Figure 3.1(a) and 3.1(b) show representative scanning electron microscope (SEM) images of a GaAs planar nanowire array grown on GaAs (100) substrate. The patterned Au dot array

was placed at a horizontal line as indicated by red arrows in Figure 3.1(a). The center-to-center spacing between the nanowires is 1 μm. The sample shown here was grown under 950 mbar at temperature T_g = 460 ^{o}C for 80 sec. The bi-directional growth can be clearly seen in Figure 3.1(a). Interestingly, we observe a noticeable difference in the planar nanowire lengths and thus in the growth rates between the two presumably crystallographically equivalent directions, with the nanowires propagating along [01-1] and the anti-parallel [0-11] direction being 9.4 μm and 8.8 μm in length, respectively. Such growth rate difference (typically < 20%) is only observed on large diameter nanowires and disappears when the nanowire widths are smaller than ~ 80 nm. This phenomenon needs further investigation. It is speculated that the preference could be induced by substrate orientation miscut (manufacture specification was ±0.5°) which makes the two directions no longer perfectly equivalent. On this particular sample, a few out-of-plane nanowires are observed and can be identified as those brighter (and shorter) nanowires in Figure 3.1(a). The out-of-plane nanowires grow along <111>B directions and therefore are aligned at 35.3° with respect to the substrate surface [17]. Figure 3.1(b) is a tilted-view SEM image where two out-of-plane nanowires can be clearly seen. Remarkably, the yield of the planar nanowires can be improved by tuning the growth conditions (details will be discussed later). Figure 3.1(c) and 3.1(d) show exemplary SEM images of the planar nanowire array with unity yield.

The realization of array-based SLE is not only important for practical device and circuit applications but also paves a way for doing systematic study of the growth mechanism as the spacing between nanowires, which could greatly affect the VLS nanowire growth rate [46], can now be precisely controlled.

3.2 Size-dependent growth rate of SLE GaAs nanowires

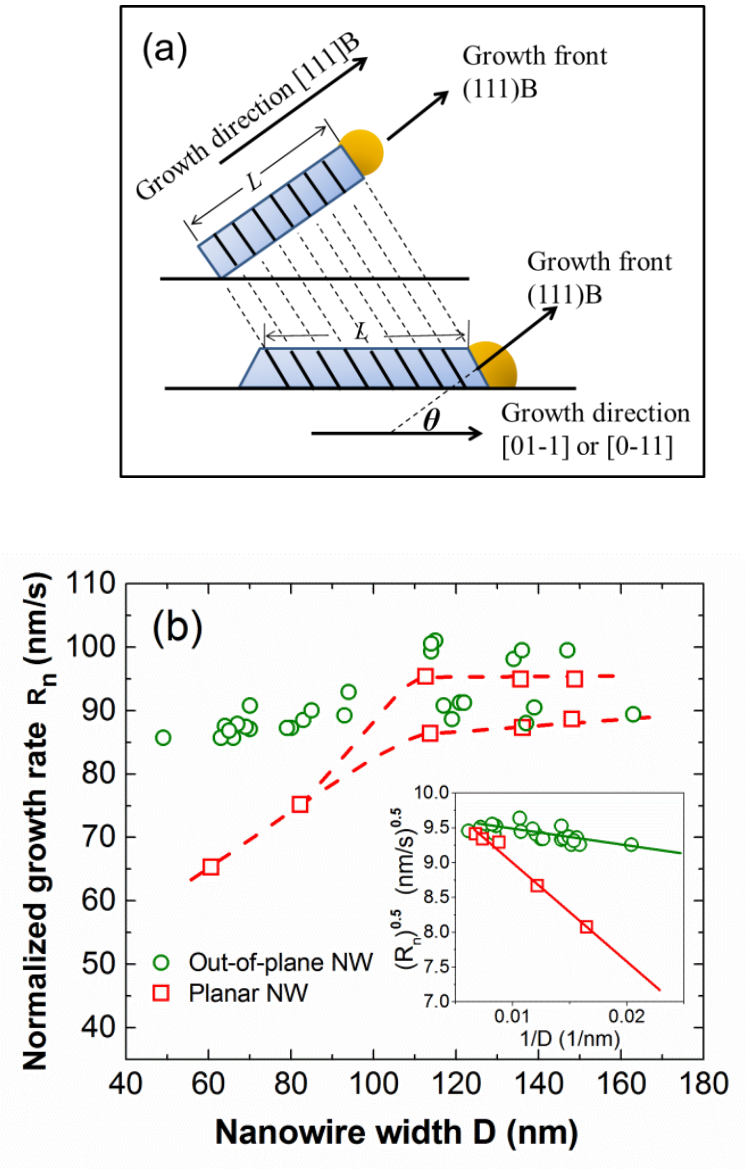

Figure 3.2 Comparison between growth rates of planar and out-of-plane GaAs nanowires. (a) Schematic diagrams of out-of-plane and planar nanowires grown on (100) substrate. A normalized growth rate is introduced in the main text for a fair comparison of the two growth modes. (b) Comparison between normalized growth rates of planar nanowires and non-planar nanowires. The growth was done at 460 ^{o}C with a V/III ratio of 30 under 950 mbar. The dashed lines are only for eye guidance. The Inset of (b) shows a linear fit to the square root of growth rate versus the inverse of nanowire width for both growth modes.

A comparison between the growth rates of planar and out-of-plane nanowires is shown in Figure 3.2. For out-of-plane nanowires, the growth direction (direction of facet advancing) and the normal direction of growth front are the same (both [111]B) [16], as illustrated by the top schematic in Figure 3.2(a). However, the two directions are different for the planar nanowire growth. As shown in Figure 3.2(a) (bottom schematic), the angle θ between the two directions is 35.3º for planar nanowire growth on GaAs (100) substrates because the growth direction is either [01-1] or [0-11] while the growth front is still (111)B, according to our previous studies [17], [19]. Let R_m be the measured nanowire growth rate, which can be obtained by directly dividing the measured nanowire length by the growth time. The volume of material deposited per unit area per unit time is $R_m\cos\theta$, where θ is 0º for out-of-plane nanowires and 35.3º for planar ones. So the number of atoms deposited per unit time per unit area is proportional to $R_m\cos\theta$. In Figure 3.2(a), the planar nanowire shown there appears to be longer than the out-of-plane one in terms of physical length. However, as indicated by the dashed lines, the two wires have exactly the same number of (111) atomic layers. They should be considered to have the same growth rate. Therefore, we define a normalized growth rate as $R_n = R_m\cos\theta$ in order to compare the two different types of nanowires on an equal footing.

Figure 3.2(b) shows the normalized growth rates of planar nanowires and out-of-plane nanowires measured from the sample prepared under the same growth condition as in Figure 3.1(a). Each of the data points (red squares) for planar nanowires was measured and averaged from about 20 nanowires in an array with 10 μm spacing between adjacent nanowires. The large spacing was designed to minimize any synergetic effect of growth rate between neighboring nanowires [46]. Without spacing control in the growth rate study, the real trend can be hidden by density related variations. Five arrays of holes were first patterned on PMMA by EBL with

nominal diameters of 300 nm, 250 nm, 200 nm, 150 nm and 100 nm, respectively. Au dots were then produced by a lift-off process after 30 nm Au film was evaporated. The planar nanowires are very uniform in size and growth rate within each array. The standard deviations of growth rate and width are smaller than 3 nm/s and 3 nm, respectively. As seen from Figure 3.2(b), when the nanowire width is relatively large (> ~ 110 nm in bottom width), two different growth rates are associated with each planar nanowire size. The growth rate starts to roll off clearly when the width becomes smaller. This is consistent with the conventional VLS model proposed by Givargizov [47] where smaller nanowires are associated with slower growth rates because nanowire surface energy reduces supersaturation. The inset of Figure 3.2(b) plots the square root of growth rate versus the inverse of nanowire width (the data points with slower growth rate are adopted for the bimodal cases). A fairly good linear fit can be obtained for planar nanowires, supporting the interpretation by the conventional model [47], [48].

The lengths of out-of-plane nanowires were also measured from those arrays since the yield of planar nanowires was not perfect under that particular growth condition. Note that each of the data points (green circles) of out-of-plane nanowires only refers to the growth rate measured from an individual nanowire. The bimodal rate is also seen for the out-of-plane nanowires. The normalized growth rates of planar nanowires (slightly slower) match closely with that of out-of-plane nanowires, both of which remain a near constant value. This can be understood by the fact that the Gibbs-Thomson effect [47] (nanowire sidewall energy) is weak for thick nanowires and thus out-of-plane and planar nanowires should have very similar supersaturation, $\Delta\mu$, defined as the difference between chemical potentials of nanowire materials in the vapor phase and in the nanowire [47]. As the nanowire width shrinks, the growth rate of planar nanowires decreases faster than that of out-of-plane nanowires. Note that this trend, where

the two modes have close growth rates at large sizes but planar nanowire grows slower at smaller sizes, is true for all growth conditions we have tested. This implies that for smaller sizes, out-of-plane growth is associated with higher supersaturation. In the discussion above, we assume the kinetic parameters that connect supersaturation to growth rate are the same for both types of growth. While open for discussion, it is reasonable because both planar and out-of-plane nanowires are seeded by Au and have (111)B growth front. Since they are located on the same sample, they also had experienced identical growth conditions. Another factor that needs to be considered is the surface adatom diffusion, which can affect the nanowire growth rate and cannot be captured by the conventional model [25]. It is confirmed in the next section that the nanowire growth rate induced by surface diffusion is negligibly small in our experiment (below 1 nm/s). Note that the observation here is different from an insightful previous study on InAs planar nanowires [49], where it was shown that planar growth was associated with larger supersaturation (less suffered from Gibbs-Thomson effect) due to the removal of substrate surface by planar growth. The contradiction is worth further study and it is speculated that under our growth conditions, the top (100) and sidewall (111)A surface energy of the planar nanowire is large and makes the overall supersaturation of planar growth smaller despite the removal of the bottom surface.

3.3 Growth rate contributed from surface diffusion

As shown in the studies of vertical InAs nanowires [25], [50], the surface-diffusion contribution to the nanowire growth cannot be captured by the conventional growth model proposed by Givargizov [47]. To validate the interpretation of our experimental results by the conventional model, a quantitative analysis on the growth rate resulting from surface diffusion is

presented in this section. Following Fröberg *et al*. [25], the nanowire growth rate due to surface diffusion can be written as

$$\frac{dL}{dt} = R\lambda\left(1-\gamma\right)\frac{2\Omega}{r}\frac{K_1\left(r/\lambda\right)}{K_0\left(r/\lambda\right)} \tag{3.1}$$

where λ is the surface diffusion length, r is the radius of a seed particle, and K_0 and K_1 are modified Bessel functions of the second kind. Ω is the atomic volume in GaAs, which can be calculated by $a^3/4$ with a being the lattice constant of GaAs. R (nm^{-2} s^{-1}) is the arrival rate of surface adatoms which can be measured from substrate growth rate. Based on Ref. [45] from our group, the substrate growth rate R_{sub} (growth rate of the parasitic thin film deposited simultaneously during the VLS growth) was measured to be ~0.1 nm/s under similar growth conditions as used here. Such low thin-film growth rate is because the growth temperature is quite low (460 ^{o}C). R can then be calculated by $R=R_{sub}/\Omega$. The parameter γ is related to Gibbs-Thomson effect and is close to 1 when Gibbs-Thomson effect dominates [25]. It is set to zero here for estimating the upper limit of growth rate induced by surface diffusion. The diffusion length λ used here is on the order of 10 nm according to another study on VLS growth of GaAs nanowires by MOCVD where similar growth conditions were used [51]. The upper limit of growth rate (γ = 0) induced by surface diffusion is then calculated as a function of the seed particle diameter and is shown in Figure 3.3.

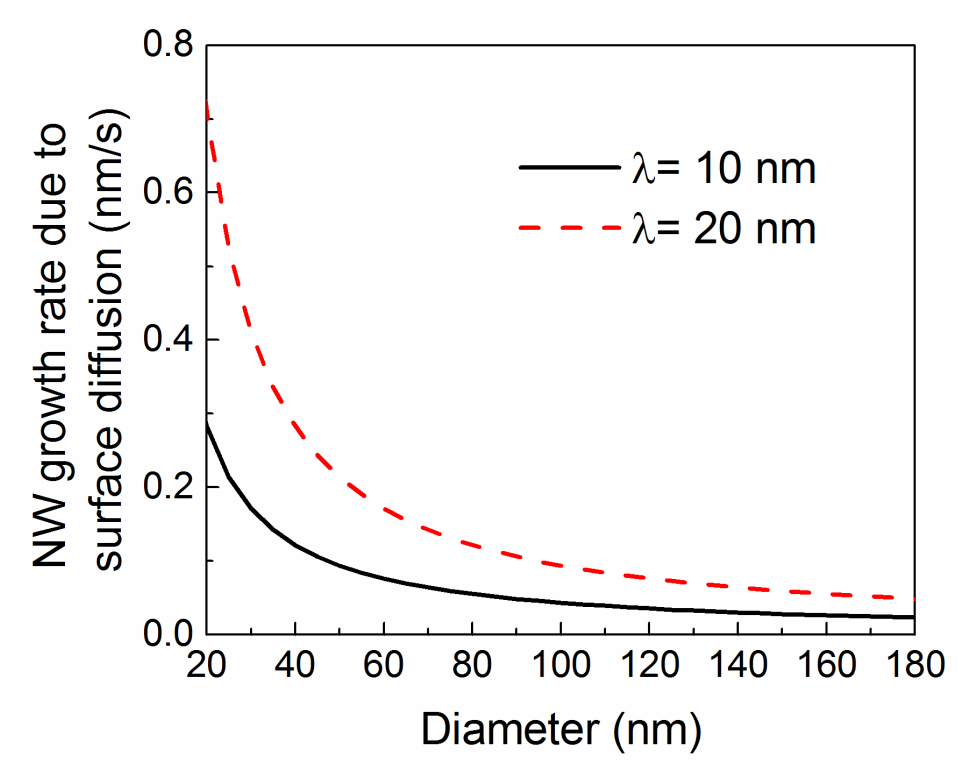

Figure 3.3 The calculated upper limit of nanowire growth rate induced by surface diffusion.

As seen from Figure 3.3, the growth rate contributed by surface diffusion is much smaller than the growth rate observed in our experiments so it can be safely neglected for the size range discussed in our experiment (> 50 nm). Even for λ=100 nm, the contribution is below 2 nm/s for diameters larger than 50 nm. This is still small compared to the nanowire growth rate observed in our experiment. Therefore the mechanism that is responsible for the nanowire growth here is dominantly the direct impingement from gas phase. The quantitative analysis above is also consistent with the fact that we did not observe the signature behavior of a diffusion-limited growth—smaller nanowires grow faster within certain diameter range. In our experiments, smaller nanowires always grow slower.

3.4 Yield of planar growth versus nanowire size

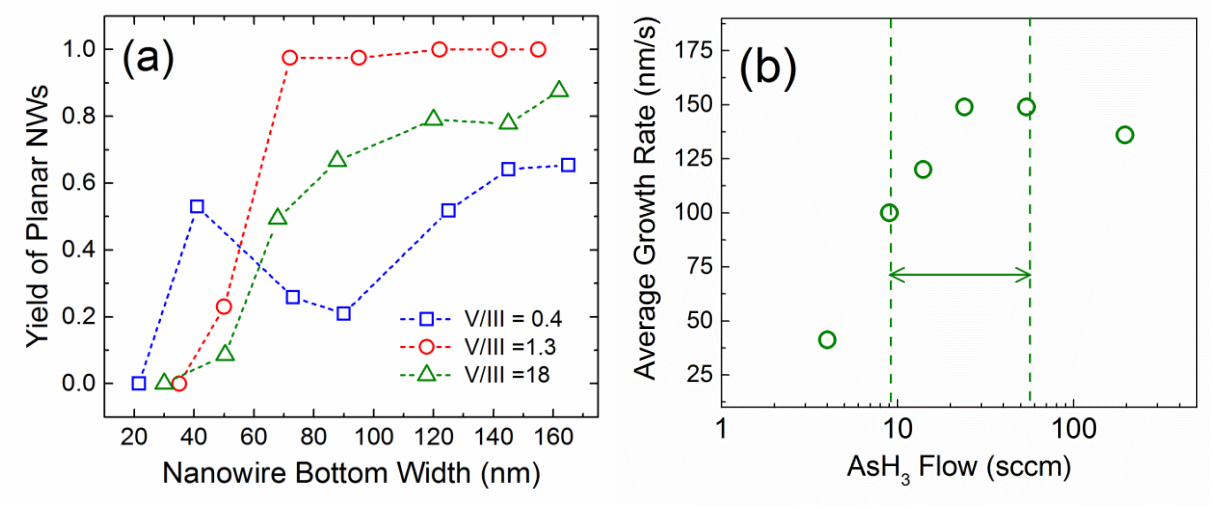

Figure 3.4 (a) Yield of planar nanowires as a function of bottom width. Three samples were prepared with V/III ratios of 0.4, 1.3 and 18, respectively. We fixed TMGa flow and only the AsH_3 flow was changed across the three samples. The growth temperature and reactor pressure were 460 $^{\circ}$C and 150 mbar, respectively. (b) Plot of nanowire growth rates versus AsH_3 flow rates. The green arrow indicates the regime where perfect yield can be obtained.

Figure 3.4(a) shows the yield of planar nanowires as a function of the nanowire size (bottom width). The yield here is defined as the ratio between the number of nanowires that remain planar throughout the entire growth period and the total number of nanowires (81) grown in the array. Three samples grown with different nominal V/III molar flow ratios (0.4, 1.3 and 18) are shown in Figure 3.4(a). To vary V/III ratios, the TMGa flow was fixed and only the AsH_3 flow was changed across the three samples. Other growth conditions were identical, with growth temperature and reactor pressure being 460 ^{o}C and 150 mbar, respectively. Multiple Au dot arrays with the same dot size within each array were patterned on each of those samples. The growth rates of large nanowires (> 120 nm in width) on the samples with V/III ratio of 18, 1.3 and 0.4 are 135 nm/s, 120 nm/s and 40 nm/s, respectively. The corresponding growth times are

50 s, 50 s, and 80 s, respectively. For smaller nanowires, the growth rate decreases following a trend similar to that in Figure 3.2(b). From Figure 3.4(a), it can be seen that for nanowires with bottom width larger than ~70 nm, the sample with V/III = 1.3 has unity yield of planar nanowires. The yields from the other two samples are noticeably lower. In this size range, unity yield can be reproducibly achieved when the V/III ratio ranges from ~0.8 to ~5. The optimized regime is indicated by the green arrow in Figure 3.4(b) where the growth rate is plotted as a function of AsH_3 flow. It is interesting to note that the regime is centered with the point where the growth rate starts to level off.

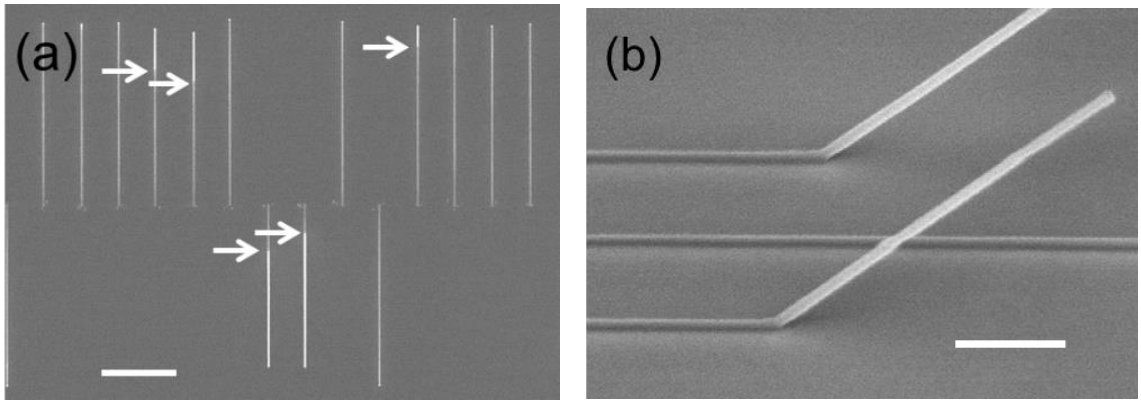

Figure 3.5 (a) A typical SEM image showing the transition regime where some of the planar nanowires start to take off from the substrate surface in the middle of the growth. The out-of-plane nanowires show brighter contrast in the image. The white arrows indicate the points where the nanowires start to take off. The scale bar is 2 μm. (b) 60 degree tilted view of the nanowires taking off in the middle of the growth. The scale bar is 500 nm.

As the nanowire width becomes smaller, the yield at the optimum V/III ratio of 1.3 drops below 100% and when the width becomes less than ~50 nm, no planar nanowires can be observed. The widths shown in Figure 3a for the zero yield case were measured on out-of-plane nanowires. Shown in Figure 3.5(a) is a typical SEM image of the transition regime where the planar nanowire yield has degraded. It is observed that many nanowires start the growth in the

planar mode but take off from the substrate surface at some point, as indicated by the white arrows in Figure 3.5(a), during the growth. This can be seen more clearly from Figure 3.5(b). The result suggests the presence of a delicate balance between planar and out-of-plane mode. The other two samples show similar trend in general where smaller nanowires have lower yield and no planar nanowires can be found when the size drops below certain points. A hump at 40 nm nanowire width is observed on the yield-size curve with V/III=0.4, which is not understood at this point and needs further study. It has to be mentioned that the cessation of planar nanowire growth at very small sizes is not because of a complete loss of supersaturation due to the Gibbs-Thomson effect. Extremely high growth rates (~100 nm/s) for planar nanowires are still observed from the very low-yield array of small-size nanowires. In other words, there still exists a large level of supersaturation to support fast planar nanowire growth. Other underlying reasons that control the preference between planar and non-planar growth need to be considered.

3.5 Proposed growth mechanism

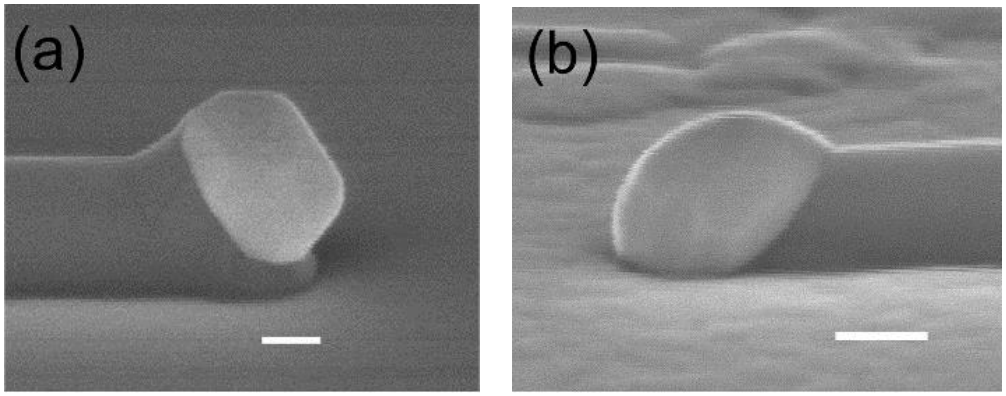

Figure 3.6 SEM images showing the shapes of seed particles after sample cooling. (a) Cooling with AsH_3 overpressure. (b) Cooling without AsH_3 overpressure. The sample is tilted by 80^o. The scale bars are both 100 nm.

Shown in Figure 3.6 are two SEM images of Au seeds after growth where (a) and (b) show the samples that were cooled down from the growth temperature with and without AsH_3 overpressure, respectively. It is observed that the Au particle in Figure 3.6(a) shows a non-spherical shape and a neck-like structure is formed and clearly visible below the Au nanoparticle. This is because with the supply of As precursor during sample cooling, the Ga atoms in the seed particle can continue to precipitate out to form an additional growth segment of GaAs, as is the case for out-of-plane nanowires [52]. However, the Au particle in Figure 3.6(b) exhibits a rounder profile and only negligible extraneous material is visible below the gold. In the absence of AsH_3 supply, only a very small amount of GaAs can be formed during the cooling process because of the extremely low solubility of As in Au so the shape of seed can be well preserved. Therefore, Figure 3.6(b) should more closely represent the actual growth-phase geometry of Au nanoparticle. Importantly, the base of the nanoparticle is in contact with the substrate, which suggests that it was in direct contact with the substrate, in addition to the nanowire growth front, during planar nanowire growth. Note that in the growth of in-plane InAs nanowires, such additional contact interface was also observed [49], [53].

Based on the experimental analysis above, we propose that the wetting nature of seed droplet on the substrate during growth is an important factor responsible for the planar type of VLS GaAs nanowire growth. Once the liquid-form seed particle contacts the substrate surface, it needs to overcome the adhesion energy between the seed and the substrate surface before the out-of-plane mode may proceed. Note that it was suggested, in the case of in-planar InAs traces growth on (111)B GaAs [53], that the Au seed stays on the substrate because Au/GaAs interfacial energy is lower than that of Au/InAs interface. We believe that in general, this energy difference is not necessary for the occurrence of planar VLS nanowire growth since in our case,

the Au/GaAs (111)B interface at the growth front should have lower interfacial energy [16]. It is speculated that the wetting was initiated during oxide desorption procedure at the very beginning of the growth—the gold dots collect materials from the substrate and become eutectic droplets. After the growth precursors are introduced, the planar growth proceeds with materials stacking in a layer-by-layer manner on (111)B facet while the droplet remains in contact with the (100) substrate since (100) is not the growth front. As discussed in refs [54] and [55], perturbations that occur during nanowire growth might strongly affect the choice of growth modes. Perturbations such as organic residue on the substrate or the occurrence of a stacking fault may interrupt the contact between the seed particle and the substrate and make the nanowires switch to the out-of-plane mode. Supporting evidence can be found in our previous study where the intentional introduction of twinning defects by dopant incorporation can cause the planar nanowire to switch to out-of-plane growth mode [56]. This explains the fact that even the yield for large planar nanowires is not always perfect except for under optimized V/III ratios. As reported in the recent research on *in-situ* TEM observation of III-V VLS nanowire growth [57], a growth condition with very high V/III ratio can induce twinning defects, which is likely to disturb the planar growth in our case. The factors discussed above also provide a natural explanation for the size-dependent yield study. Small-size seeds would have less contact area with the substrate so one would expect that it is easier to separate them from the substrate. In other words, the growth of narrower planar nanowires should be more vulnerable to perturbations and thus shows lower yield. The analysis here implies that the planar type of growth could be universally achievable in any material system if i) the growth front is not in parallel with the substrate surface and ii) the adhesion between the substrate and the seed can be engineered to be sufficient.

CHAPTER 4 – DEVICE AND CIRCUIT BY HOMOGENEOUS SLE

4.1 Planar GaAs nanowire MOSFETs[†]

This section describes MOSFET devices based on the n-type GaAs planar nanowires homogeneously grown on GaAs semi-insulating (S.I.) substrates. This is not only to show a new functionality in addition to planar nanowire MESFETs [44] and HEMTs [45], but also to demonstrate that those planar nanowires, although grown with entirely different conditions compared to conventional thin film epitaxy, can form a good dielectric/nanowire interface that allows decent MOSFET operations.

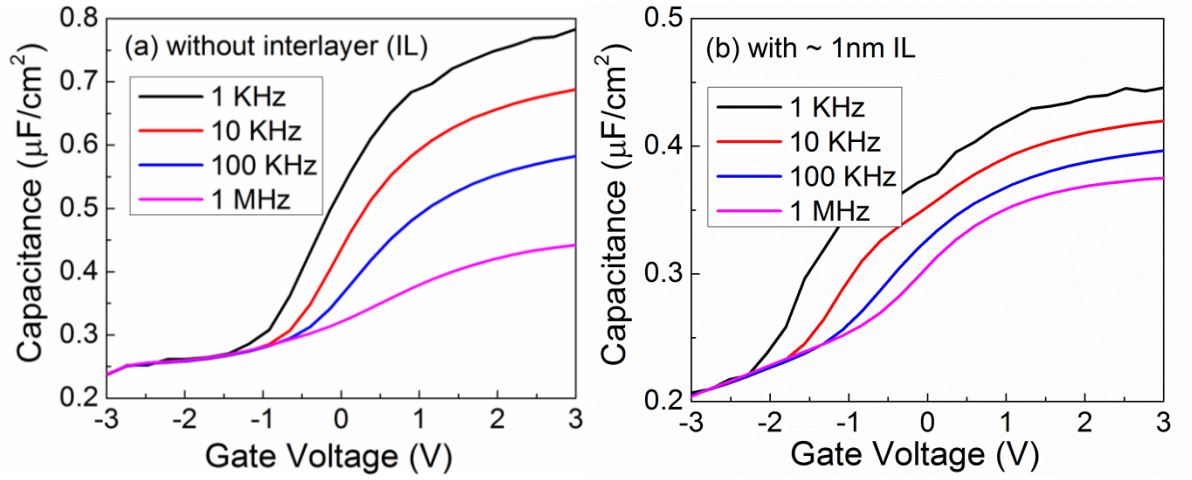

Figure 4.1 C-V characteristics of Al_2O_3/GaAs MOSCAPs. (a) Without interlayer (IL), (b) with ~1 nm IL. Both MOSCAPs were fabricated without annealing.

A study of oxide/GaAs interface was first carried out by capacitance-voltage (C-V) measurement of GaAs MOS capacitors (MOSCAPs). The MOSCAPs were fabricated on n-type

[†]Some of the content in this section is adapted with permission from Chen Zhang and Xiuling Li, "Planar GaAs nanowire tri-gate MOSFETs by vapor–liquid–solid growth," *Solid-State Electronics*, vol. 93, pp. 40–42, 2014. Copyright (2014) Elsevier.

doped ($1\sim3\times10^{18}$ cm^{-3}) GaAs (100) substrates. Figure 4.1(a) shows the C-V curves of a 10-nm-Al_2O_3/GaAs MOSCAP measured at different frequencies. Very large frequency dispersion (0.11 $\mu F \cdot cm^{-2}$/dec at V_g= 3 V) is observed, indicating poor interface quality [58]. We attempted to deposit amorphous Si by PECVD as an interlayer between ALD Al_2O_3 and GaAs to improve the interface quality, following Ref. [59]. However, the deposited material was actually SiO_2 because of the residual oxygen in the PECVD chamber. This is supported by the fact that the material cannot be etched by XeF_2 and the measured refractive index is 1.44. Nevertheless, substantial improvement of C-V characteristics can be achieved by using this SiO_2 layer. As shown in Figure 4.1(b), much less frequency dispersion is observed (0.024 $\mu F \cdot cm^{-2}$/dec at V_g= 3 V). It is likely that despite the presence of oxygen, the Si-rich environment in the PECVD chamber could still help remove the residual native oxide on GaAs surfaces, similarly as the mechanism discussed in Ref. [59].

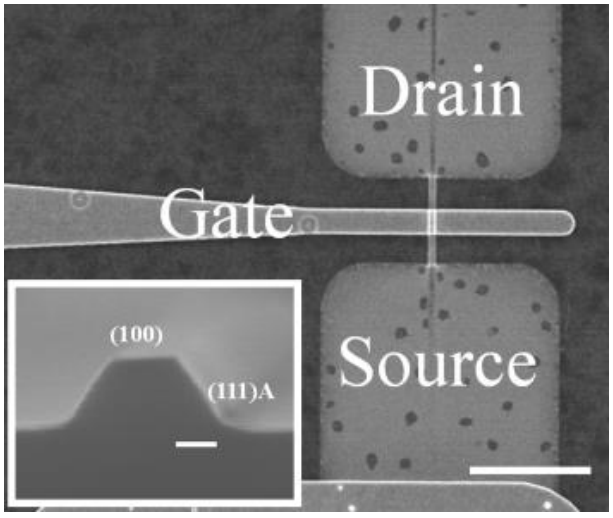

Figure 4.2 SEM image of a fabricated planar nanowire MOSFET device. Scale bar indicates 4 μm. The inset SEM image shows the cross section of an as-grown planar nanowire with a (100) top facet and two (111)A sidewalls. The scale bar in the inset represents 80 nm.

The GaAs planar nanowire growth used in this section was done under atmospheric pressure at 460 ^{o}C utilizing colloidal Au particles (250 nm in diameter) as growth seeds. Si_2H_6 was used as the n-type doping source. The entire nanowire is n-type doped so the MOSFET device operates in depletion mode. The as-grown nanowires have a bottom width of ~280 nm. For GaAs planar nanowire grown on (100) substrate, the top surface has been identified to be (100) whereas the two sidewalls are (111)A [19]. Standard Ge/Au/Ni/Au metal stack is used for S/D contact whereas Ni/Au is used for gate contact. The gate length (L_g) is measured to be ~ 850 nm. The nominal thickness for the MOSFET high-*k* Al_2O_3 layer is 7.2 nm. When an interfacial layer of ~1 nm was inserted between the multi-faceted GaAs nanowire and the high-*k* Al_2O_3 layer, the Al_2O_3 thickness was reduced to 6.3 nm. A SEM image of a fabricated GaAs nanowire MOSFET is shown in Figure 4.2. The inset shows the trapezoidal cross-section profile of the nanowire channel with a (100) top facet and two (111)A side facets, a tri-gate structure. In fact, it has been shown that Fermi level on GaAs (111)A surface is inherently unpinned [58].

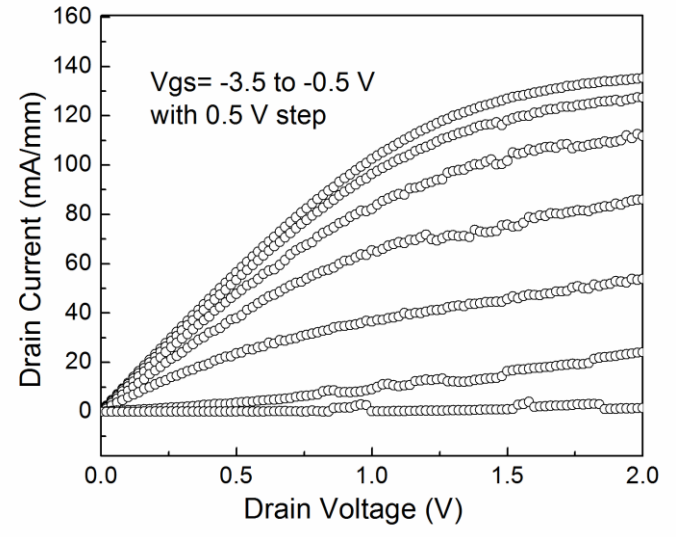

Figure 4.3 Output curves of the planar nanowire MOSFET device with SiO_2 interlayer.

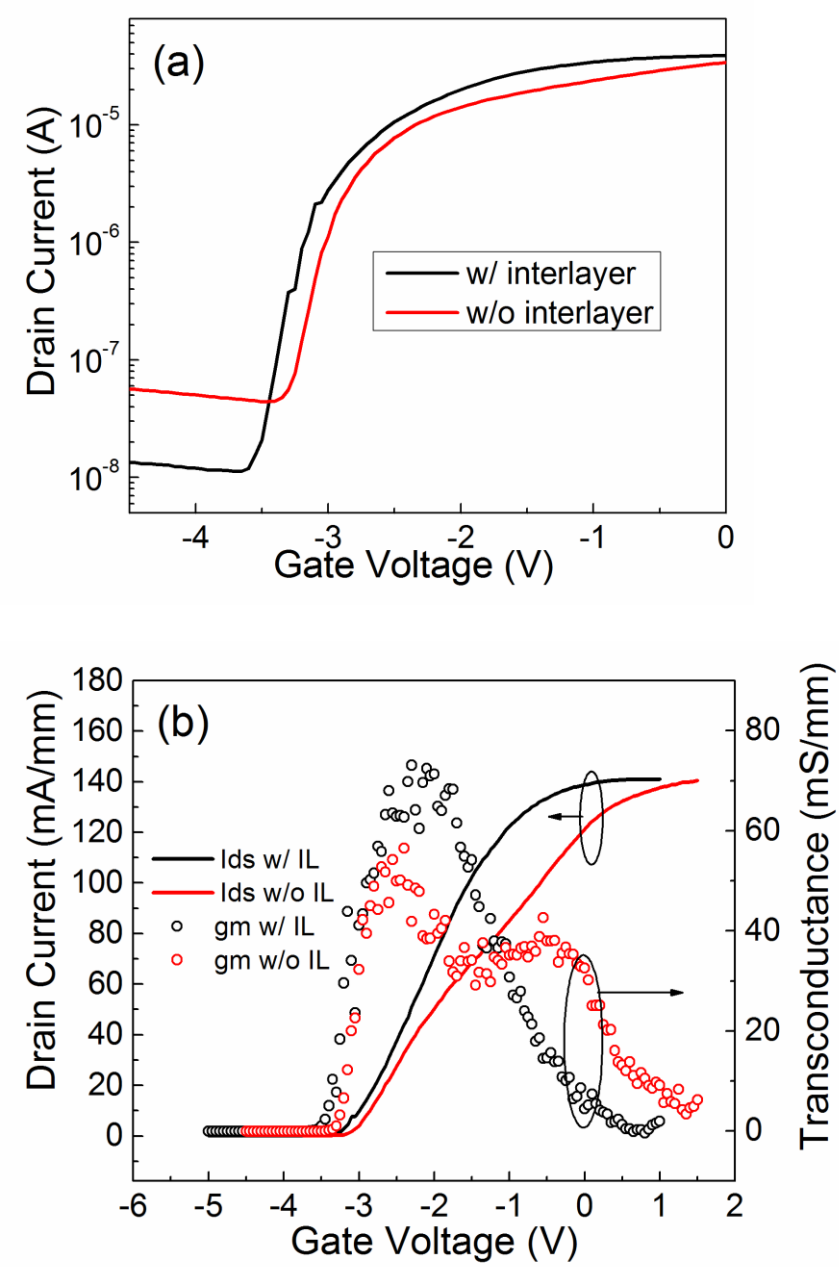

Figure 4.4 Comparison of transfer characteristics between devices with and without interlayer (V_{ds} = 2 V). (a) Semi-log scale showing sub-threshold and off-state characteristics. (b) Linear plot scale showing on-state characteristics.

The output characteristics of the device with interlayer are shown in Figure 4.3. Figure 4.4(a) compares the semi-log scale transfer curves of two typical devices with and without the

SiO_2 interlayer at V_{ds} = 2 V. The sub-threshold slope of the device without interlayer is calculated to be 190 mV/dec, whereas a better number of 160 mV/dec is obtained for the one with interlayer. We re-plot the transfer curves in linear scale and calculate the transconductances (g_m) in Figure 4.4(b), normalized with respect to the bottom width of the nanowire. The peak extrinsic g_m is about 73 mS/mm for the device with interlayer. The intrinsic g_m is estimated to be about 92 mS/mm by taking into account the source-side series resistance (2.8 kΩ·μm by estimation). For the device without interlayer, g_m is lower in general and quickly rolls off after the gate voltage reaches ~1 V beyond threshold. The comparison in Figure 4.4 indicates that the nanowire surface Fermi level can be more effectively moved in the device with the interlayer. In addition, we observe a double-hump feature in the g_m curve of the device without interlayer, which is presumably related to the presence of two kinds of facet in our planar nanowires. This feature is seen to be removed (Figure 4.4(b)) by applying the interlayer, which can improve the passivation quality of the top (100) facet.

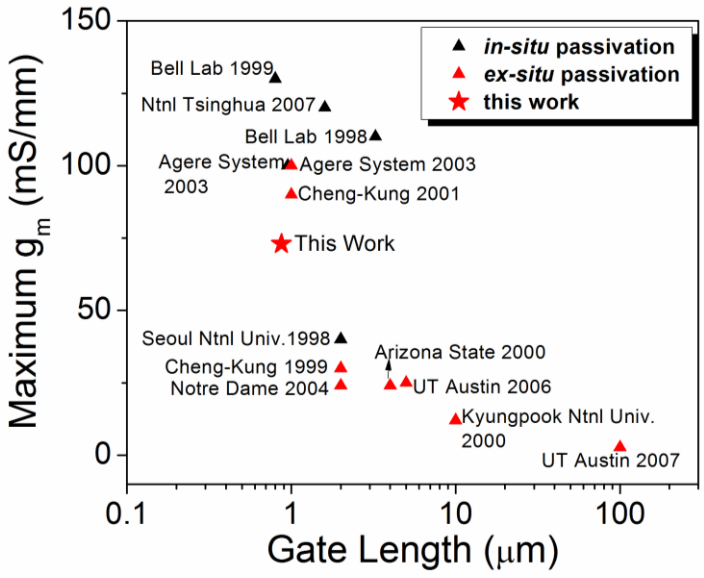

Figure 4.5 Benchmark of depletion-mode GaAs MOSFETs in literature.

Figure 4.5 summarizes the peak g_m of the conventional thin-film GaAs depletion-mode MOSFETs reported in the literature. We divide the data into two categories. The first one, which is indicated by the black triangles, refers to MOSFET devices with gate oxide grown by *in-situ* methods. In this case, the gate oxide was deposited *in situ* right after the growth of GaAs in the same chamber. In this case, no native oxides can be formed before the gate oxide growth, presumably resulting in good interface. The other category, indicated by the red triangles, corresponds to the MOSFETs with gate oxide fabricated by *ex-situ* methods, i.e. the GaAs surface has been exposed to air before the formation of gate oxide. Although native oxide and extra contaminations might be introduced to the interface, the *ex-situ* methods are more practical for IC fabrication. Our device shows a reasonably high transconductance compared with other *ex-situ* passivated devices, indicating a good dielectric/nanowire interface.

4.2 GaAs planar nanowire MESFET amplifier[†]

This section presents a current-source load amplifier fabricated by interconnecting GaAs planar nanowire MESFET devices. To our knowledge, so far it is one of very few works that demonstrate circuit applications, beyond discrete devices, of a particular nanotechnology. Traditional planar GaAs MESFET devices often show low output resistance, thus low voltage gain for the amplifiers resulting from the large channel length modulation effect [60]. This is because the thick depletion layer that exists between gate and the actual conducting channel degrades the gate control, which is similar to the case in MOSFETs. It is anticipated that a nanowire channel with the multi-gate structure can improve the gate electrostatics and reduce the

[†]Some of the content in this section is adapted with permission from Chen Zhang, Ryan Dowdy, and Xiuling Li, "High voltage gain MESFET amplifier using self-aligned MOCVD grown planar GaAs nanowires," in *Device Research Conference (DRC)*, 2013, pp. 63–64. Copyright © [2013] IEEE.

channel length modulation effect as a result.

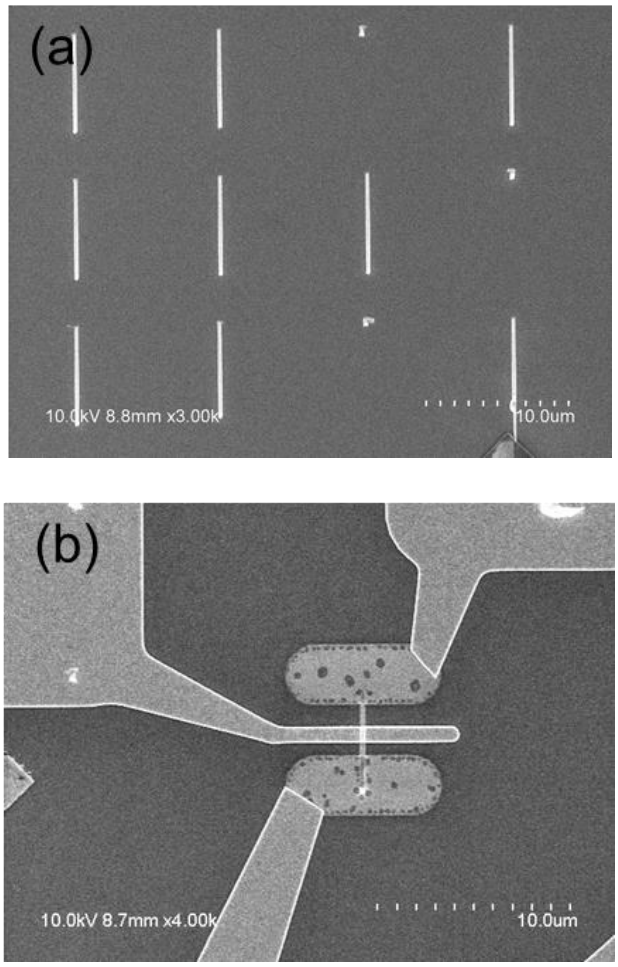

Figure 4.6 (a) SEM image showing a uni-directionally aligned GaAs planar nanowire array grown on a S.I. GaAs (110) substrate. The Au particles are on lower end of the nanowires. (b) SEM image of a planar nanowire MESFET.

The Au dot array (growth seeds) was patterned by EBL on S.I. GaAs (110) substrate. The growth on (110) was done at 480 ºC and Si_2H_6 was used as n-type dopant precursor. Figure 4.6(a) shows a top-view SEM image of the nanowire array. The yield of planar nanowire on (110) substrate is not perfect with current growth conditions but could certainly be further improved. The three missing wires in Figure 4.6(a) were originally out-of-plane and were broken

off by sonication. The nanowires used in this study have a trapezoidal cross section with bottom width of ~300 nm, top width of ~ 100 nm and bottom angle of 45 degree [20]. Figure 4.6(b) shows a SEM image of a fabricated planar nanowire MESFET device. Standard Ge/Au/Ni/Au metal stack was used for S/D drain contact. Ti/Au was used as gate metal.

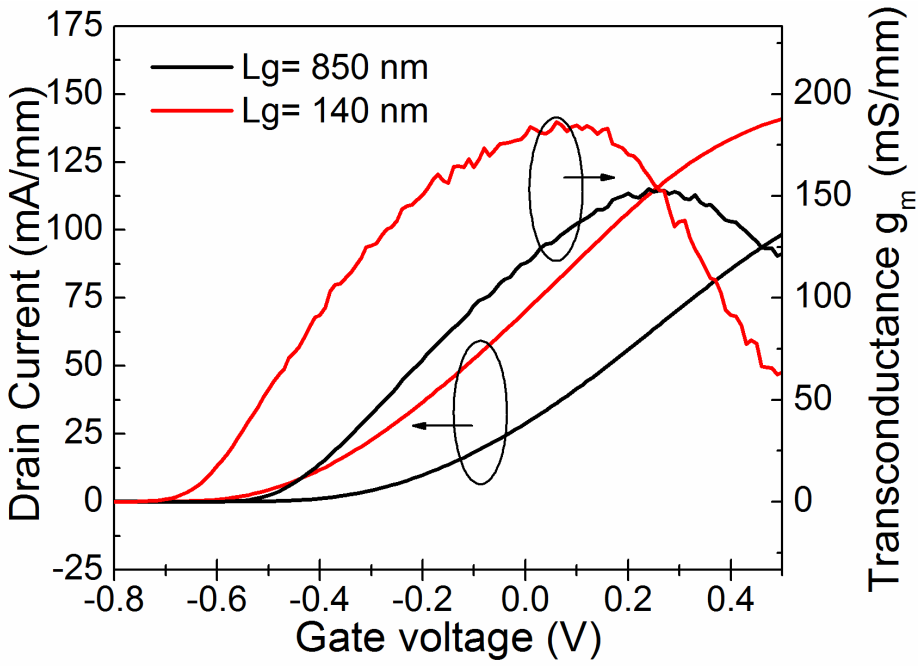

Figure 4.7 Transfer and g_m curves of nanowire MESFETs with gate length of 850 nm and 140 nm at V_{ds} = 2.0 V

The transfer and transconductance curves of single-nanowire MESFET devices with gate length of 850 nm and 140 nm are shown in Figure 4.7. The current and g_m are normalized with respect to the bottom width (300 nm) of the nanowire. The peak extrinsic g_m obtained on the short channel device is 180 mS/mm. The intrinsic transconductance estimated is about 260 mS/mm where the source-side series resistance R_s was calculated based on the two terminal *I-V* measurement. Shown in Figure 4.8 is the subthreshold performance of MESFET devices with different gate lengths. Owing to the multi-gate structure enabled by nanowire, DIBL still

maintains a low value (less than 40 mV/V) when the gate length shrinks down to 140 nm. The low on-off ratios shown in Figure 4.8(a), (b) and (c) are actually due to substrate leakage resulting from the parasitic thin film deposition during the growth of VLS nanowires. The leakage can be largely suppressed by etching several nanometers of the GaAs surface at the beginning of the fabrication.

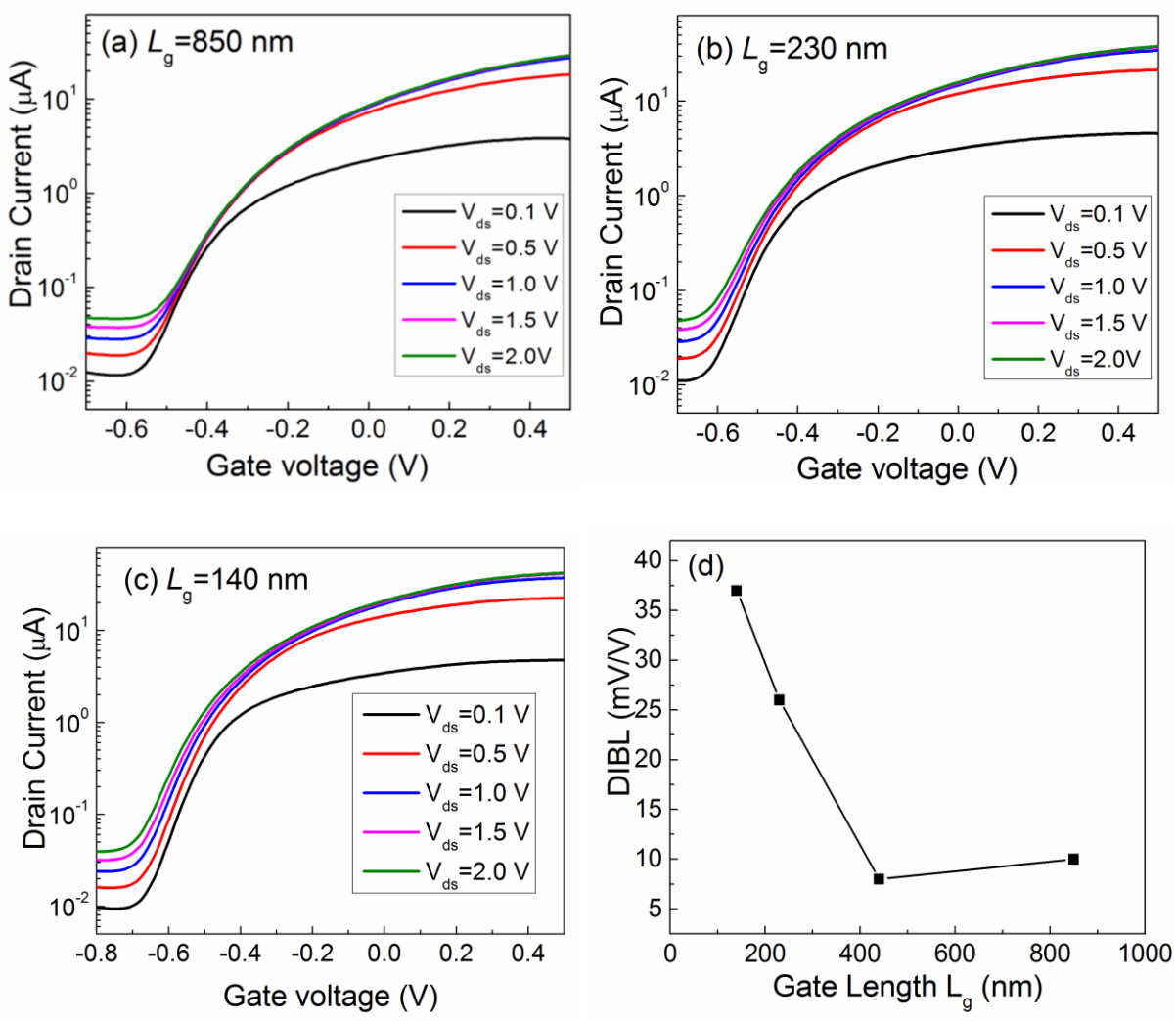

Figure 4.8 (a), (b) and (c) show the semi-log scale transfer curves of the of nanowire MESFET devices with gate length of 850 nm, 230 nm and 140 nm, respectively. Shown in (d) is DIBL as a function of gate length.

A long-channel output characteristic can be seen in Figure 4.9 for the device with 850 nm gate length whereas some channel length modulation effect shows up in the device with 230 nm gate length. To calculate the channel length modulation parameter λ, we first extracted the intrinsic drain conductance (g_{id}) from the output curves using the method in Ref. [61]. The drain current in saturation region can be expressed as:

$$I_{ds} = \beta(V_{gsi} - V_{th})^2(1 + \lambda V_{dsi}) \tag{4.1}$$

where V_{gsi} and V_{dsi} are intrinsic gate and drain voltage, respectively. Based on (4.1), we calculate λ by

$$\lambda = \frac{\partial I_{ds}}{\partial V_{dsi}} \Big/ \beta(V_{gsi} - V_{th})^2 = \frac{g_{di}}{\beta(V_{gsi} - V_{th})^2} \approx \frac{g_{di}}{I_{ds0}} \tag{4.2}$$

where I_{ds0} refers to the drain current at the beginning of the saturation region. The calculated λ is 0.02 V^{-1} for L_g = 440 nm and 0.04 V^{-1} for L_g = 850 nm. It is lower than the typical value of 0.1–0.3 V^{-1} for conventional GaAs MESFETs with L_g of ~1 μm [60]. We believe this improvement can be attributed to the multi-gate geometry of the nanowires.

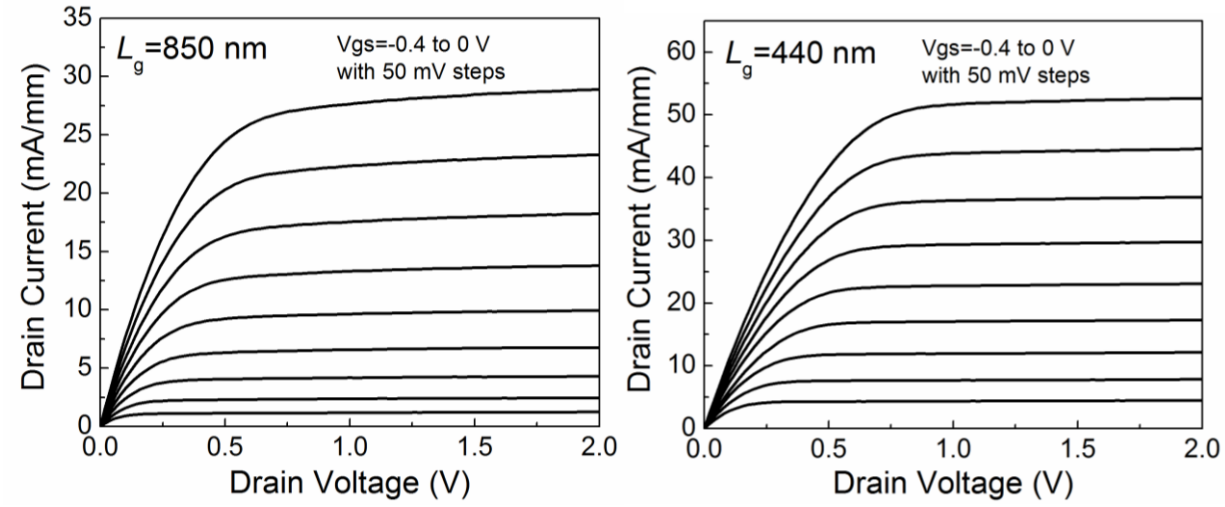

Figure 4.9 Output curves of nanowire MESFET devices with gate length of 850 nm and 440 nm.

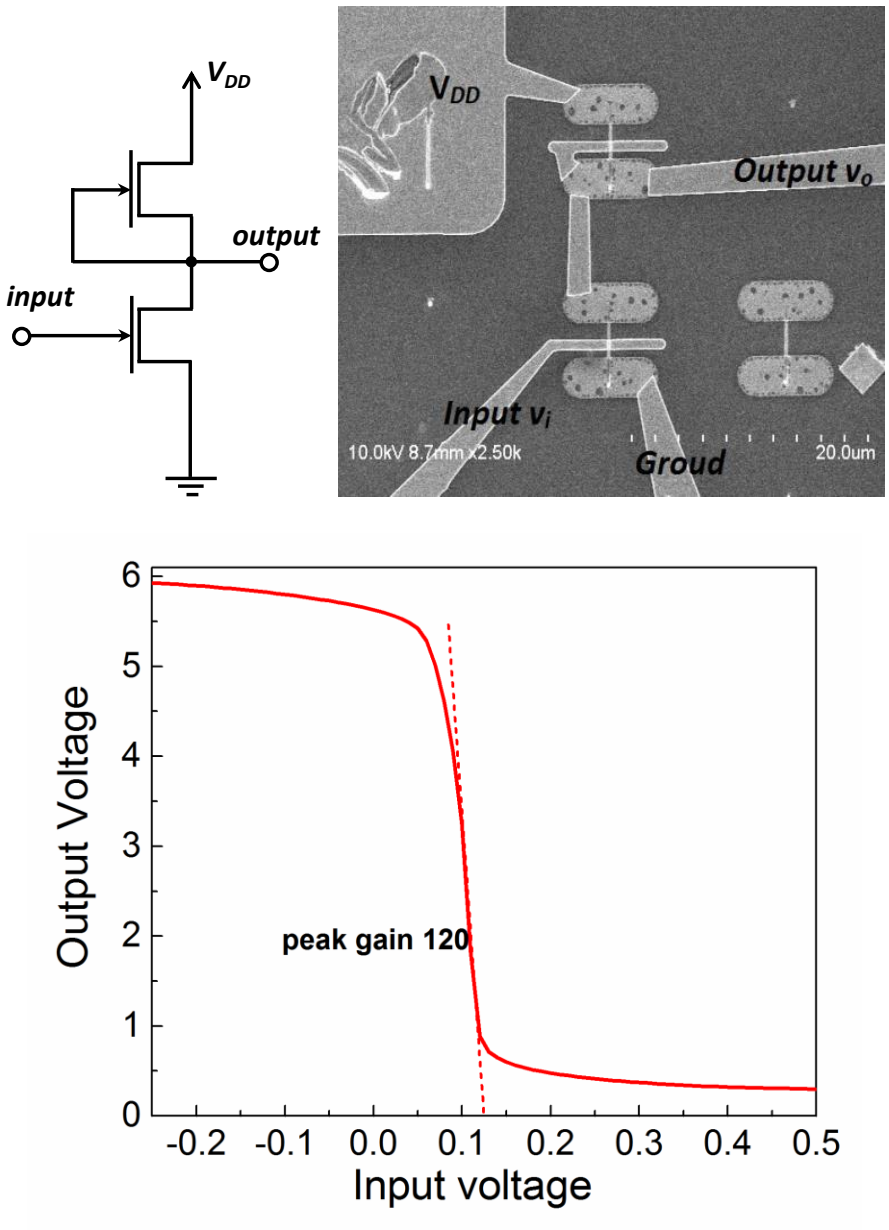

Figure 4.10 The top SEM image shows an amplifier made by two nanowire MESFETs. The bottom figure shows the output versus input of two different devices. V_{DD} = 6 V.

Based on the planar nanowire array, a simple version of amplifier has been successfully demonstrated as shown in Figure 4.10. The schematic circuit diagram is shown on top in Figure 4.10. The amplifier consists of two MESFETs, one of which is connected as a current source and

acting as the load. The bottom MESFET is the active device for voltage amplification. The SEM image in Figure 4.10 shows a fabricated amplifier with the input (V_i) and output (V_o) metal leads clearly labelled. The bottom figure shows the V_o-V_i transfer characteristics of an amplifier. An excellent peak voltage gain of ~120 is extracted, which is much higher than the traditional planar MESFET amplifiers [60], thanks to the improved output resistance enabled by the multi-gate structure. Even higher voltage gain should be able to be achieved by using more sophisticated amplifier design.

4.3 Array-based planar GaAs nanowire HEMT

It has to be mentioned that based on the array-based growth technology developed in Chapter 2, our group has demonstrated array-based GaAs planar nanowire HEMT devices [13]. Excellent frequency performance with f_T = 33 GHz and f_{max} = 75 GHz has been demonstrated. By further increasing the nanowire density, a f_{max} = 248 GHz at L_g = 150 nm is predicted [14].

CHAPTER 5 – HETEROGENEOUS SLE OF InAs PLANAR NANOWIRES AND THEIR MOSFET APPLICATION[†]

GaAs is a representative III-V material good for growth mechanism study and prototype device demonstration, partly because of the easy access to native GaAs substrates. On the other hand, the electron mobility of GaAs (6,000–8,000 $cm^2/V{\cdot}s$ at room temperature for very lightly doped GaAs thin film [62]) is not as high as other III-V materials, for example, high In-content (In%) InGaAs. In fact, the electron mobility generally increases with In%. A remarkably high electron mobility of ~30,000 $cm^2/V{\cdot}s$ can be routinely measured from planar AlSb/InAs quantum well structures [1]. However, the conventional thin-film growth of high-quality very high-In% InGaAs material is not straightforward because of the lack of lattice-matched substrate. As mentioned in Chapter 1, InAs is heavily lattice-mismatched with the common III-V substrates. The In% in those planar InGaAs nanowire GAA transistors fabricated by top-down etching of a thin film structure is typically 53% or slight higher since $In_{0.53}Ga_{0.47}As$ is lattice-matched to InP substrates [21]–[23], [63], [64].

The SLE method provides a potential way of solving the lattice-mismatch restriction since the direct growth of nanowire structure could accommodate more strain than standard thin film [38], [65]. This chapter is devoted to the discussion of direct growth of InAs planar nanowires on highly-mismatched GaAs (100) substrate as well as the GAA MOSFET devices based on them.

[†]Some of the content in this chapter is adapted with permission from Chen Zhang, Wonsik Choi, Parsian Mohseni, and Xiuling Li, "InAs Planar Nanowire Gate-All-Around MOSFETs on GaAs Substrates by Selective Lateral Epitaxy," *IEEE Electron Device Lett*., 2015.

5.1 Growth and TEM characterization of InAs planar nanowires on GaAs

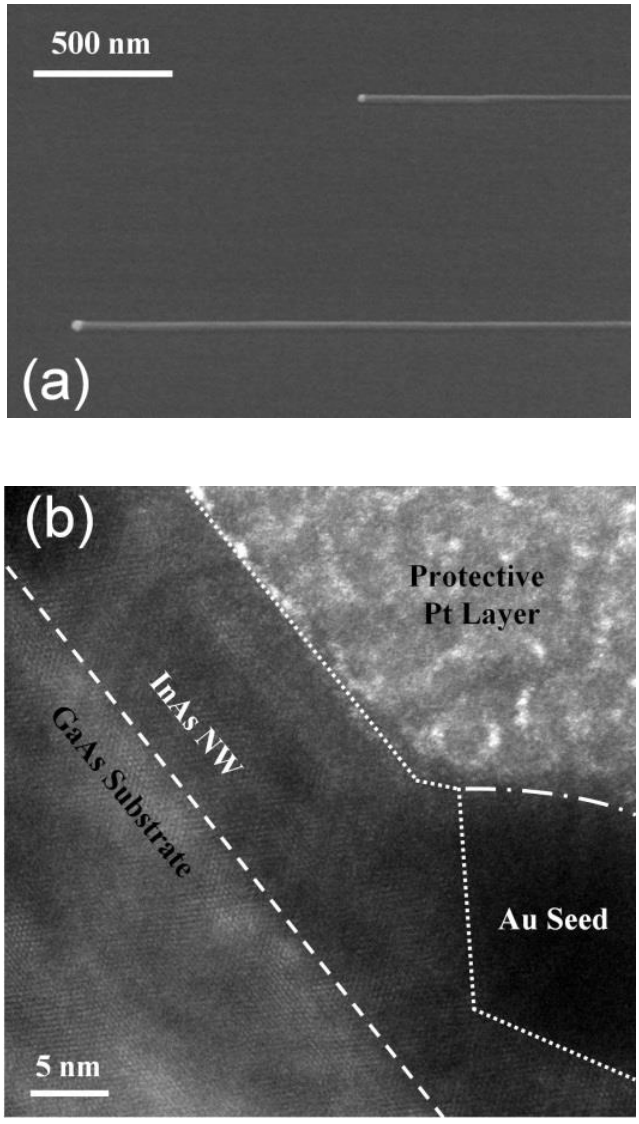

Figure 5.1 Hetero-epitaxial VLS InAs planar nanowires on semi-insulating GaAs (100). (a) Tilted-view SEM image showing parallel growth of two straight planar InAs nanowires on a GaAs substrate. (b) Cross-sectional HR-TEM image of a ~12 nm-thick planar InAs nanowire directly interfaced with the underlying GaAs substrate.

The planar InAs nanowire growth was carried out in the same reactor as GaAs on S.I. GaAs (100) substrates. Either randomly dispersed Au colloidal nanoparticles (5 nm or 10 nm in

diameter) or EBL patterned Au dots were used as growth seeds. The samples first went through an oxide desorption annealing step at 625 °C for 10 min with AsH_3 overpressure. The susceptor temperature was then ramped down to 340–360 °C, followed by InAs nanowire growth by using AsH_3 and TMIn as growth precursors. No dopant precursor was used in all growth runs.

Planar InAs nanowires were removed from the as-grown samples for scanning transmission electron microscopy (STEM) analysis using an FEI Helios NanoLab 600i focused ion-beam (FIB) system. All TEM characterization, including bright-field and high-angle annular dark-field (HAADF) imaging as well as energy dispersive X-ray spectrometry (EDXS), was performed using an energy-filtered, field-emission JEOL 2010F analytic STEM system. Prior to single nanowire liftout using the FIB, the nanowires of interest were coated with a conformal and protective, *in-situ* deposited Pt film.

Figure 5.1(a) shows a tilted-view SEM image of two as-grown InAs nanowires on GaAs (100). Note that Au-seed particles are clearly identified at the nanowire tips, characteristic of VLS-type growth, while the nanowire widths exhibit no structural variations (twinning or tapering) along their lengths. InAs planar nanowires are self-aligned along [011] or [0-1-1] direction on GaAs (100) substrates, which is the projection of <111>A direction. Figure 5.1(b) shows a cross-sectional view high-resolution transmission electron microscopy (HR-TEM) image of a laterally-grown InAs nanowire on GaAs. While the nanowire body and GaAs substrate share an atomically abrupt interfacial plane (dashed line, Figure 5.1(b)), the Au seed appears raised relative to the substrate surface, likely resulting from post-growth termination precipitation of growth species from the liquid-phase alloy in an AsH_3-rich environment.

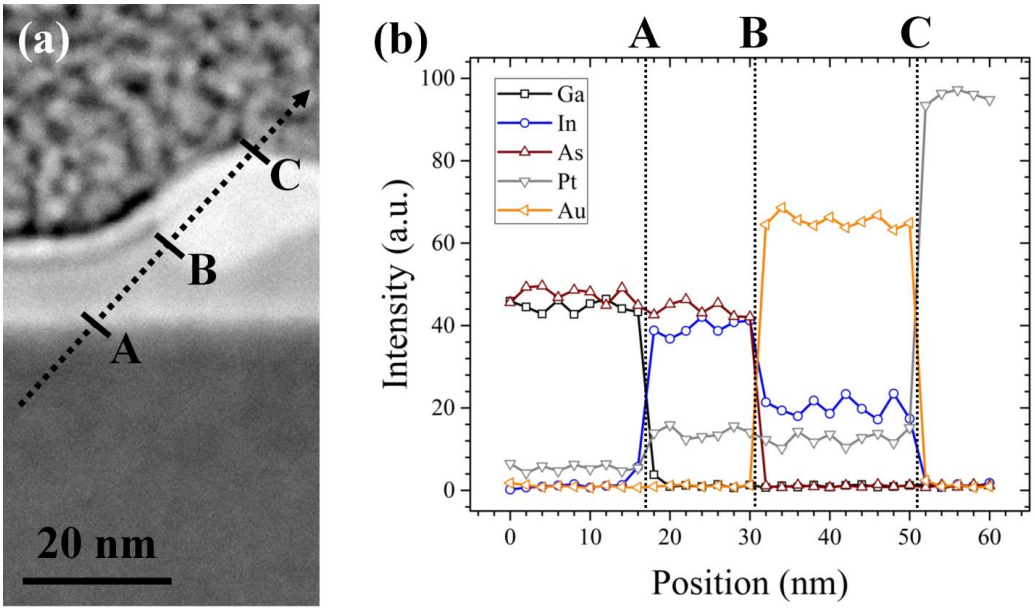

Figure 5.2 (a) HAADF-STEM image showing the tip of a hetero-epitaxial, planar InAs nanowire. (b) EDXS line-scan collected along the location of the black dotted line in (a), showing variations of Ga (black, squares), In (blue, circles), As (green, upward triangles), Pt (grey, downward triangles), and Au (orange, left-facing triangles) content. Interfacial markers ('A', 'B', and 'C') are shown in both panels for clarity.

Figure 5.2(a) shows an HAADF image of the InAs nanowire, GaAs substrate, and Au seed, while Figure 5.2(b) shows quantified elemental counts of In, Ga, As, Au, and Pt obtained through an EDXS line-scan along the location of black dotted line in (a). Coincident with the contrast variations in (a), the line-scan data in (b) confirm the presence of a GaAs substrate (region preceding marker 'A') beneath a nanowire of purely InAs composition (region between markers 'A' and 'B') with an In-Au alloyed seed at its tip (region between markers 'B' and 'C'). Note that similar to conventional non-planar InAs nanowire growth by the Au-seeded VLS mechanism, roughly 25 at.% In-content remains soluble in the seed particle post-growth. The detected background Pt signal arises from the TEM foil preparation procedure and incomplete milling of the protective Pt layer above and adjacent to the ultra-thin nanowire.

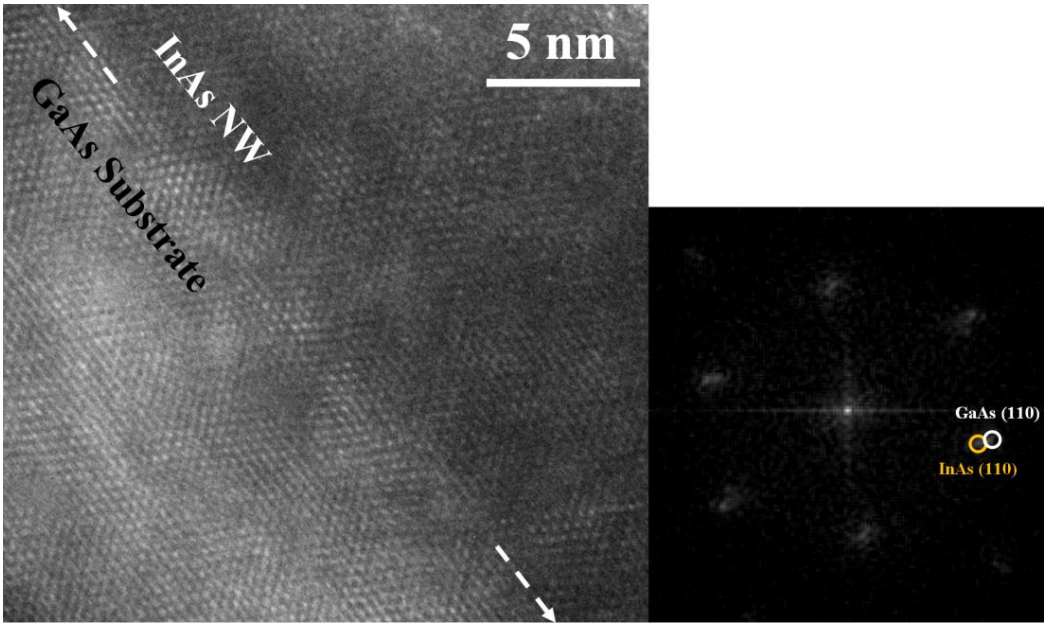

Figure 5.3 HR-TEM image obtained at the InAs nanowire/GaAs substrate interface and corresponding FFT pattern.

Figure 5.3 shows a high-magnification HR-TEM image obtained at the interface of the planar InAs nanowire and the underlying GaAs (100) substrate and corresponding indexed Fourier transform (FFT) pattern. The nanowire/substrate interface is depicted by the two dashed white arrows. From the HR-TEM image, we note that the cubic structure of the substrate is extended to the nanowire crystal. The FFT pattern shows coincident spot splitting, with negligible broadening and identical symmetry, indicative of single-crystalline nanowire growth. The inner (outer) spots are associated with the InAs nanowires (GaAs substrate), showing nanowire growth parallel to the [110] direction. The spot splitting indicates that the nanowire is indeed relaxed to some extent, likely through the free surfaces (top and sidewalls). Notable is the high crystalline quality, free of stacking faults and high density interfacial dislocations, attributed to the small diameter and minute height (~12 nm) of the nanowire.

5.2 Parasitic film growth and digital etching

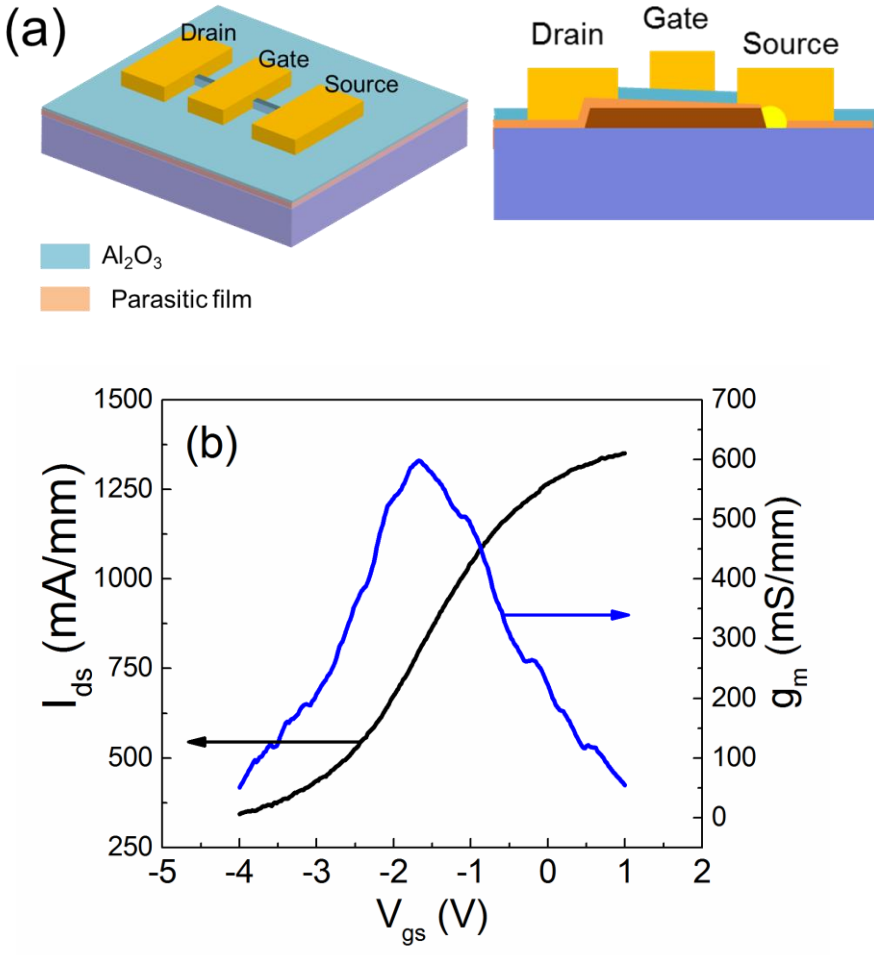

Figure 5.4 (a) Schematic diagram of the InAs planar nanowire MOSFET device directly fabricated by depositing 10 nm ALD Al_2O_3 and then metal contact for source, drain and gate. (b) Transfer and tranconductance curves of the device with ~300 nm gate length.

Figure 5.4(a) shows the schematic diagrams of the InAs planar nanowire MOSFET device directly fabricated on an as-grown nanowire. Both the tilted-view and side-view schematic diagrams are shown for a better illustration of the device structure. After MOCVD growth, the nanowire-on-GaAs sample was first treated with 10:1 buffered oxide etchant (BOE) for 40 sec to remove the native oxide, followed by sulfur passivation by soaking the sample in

$(NH_4)_2S:H_2O$ (1:2) solution for 10 min [66]. The sample was then immediately loaded into a Cambridge NanoTech Savannah atomic layer deposition (ALD) system to deposit 12-nm Al_2O_3 at 220 ºC with ten trimethylaluminum (TMA) half cycles performed at the beginning [67]. Ni/Au gate contact was then deposited by EB evaporation. After that, S/D contact was fabricated again by evaporating Ni/Au metal stack. All the patterning steps were done by EBL in a Raith eLine system.

Figure 5.4(b) shows the I_{ds}-V_{gs} transfer curve measured on the device directly fabricated on an as-grown nanowire. The nanowire width, d, and the gate length, L_g, are ~30 nm and ~300 nm, respectively. As seen from Figure 5.4(b), the device shows high on-state current and transconductance. However, it could not be turned off even when a very negative gate voltage (–4 V) was applied, showing a minimum current of ~350 mA/mm. The result above indicates that there are certain current leakage paths that cannot be well controlled by the gate. Note that the bulk substrate used is semi-insulating with resistivity, ρ, larger than 10^7 Ω·cm. So the current conducted by the bulk substrate should be much smaller than what is seen here, and thus cannot be responsible for the large leakage current observed here.

It is found that one leakage current path is on the substrate surface. During the InAs planar nanowire growth, a thin film of InAs (with its thickness in the nanometer range) is simultaneously deposited on the entire GaAs substrate surface via the vapor-solid (VS) growth mode. Given the lattice mismatch between InAs and GaAs, this parasitic thin film could be defective but it is actually quite conductive. It could potentially help reduce the S/D contact resistance like S/D re-growth (shown later in section 5.5) but needs to be removed on the channel region. The substrate surface leakage current was measured between S/D contact pads that are not connected by a planar nanowire. The leakage was measured to be 1–2 μA at 0.5 V bias,

much larger than what should be caused by a S.I. GaAs substrate. As seen from the tilted-view device structure shown in Figure 5.4(a), a large area of substrate surface is not gated. In order to remove the parasitic film, a controlled etching method needs to be employed and over-etch should be minimized in order to preserve the nanowire.

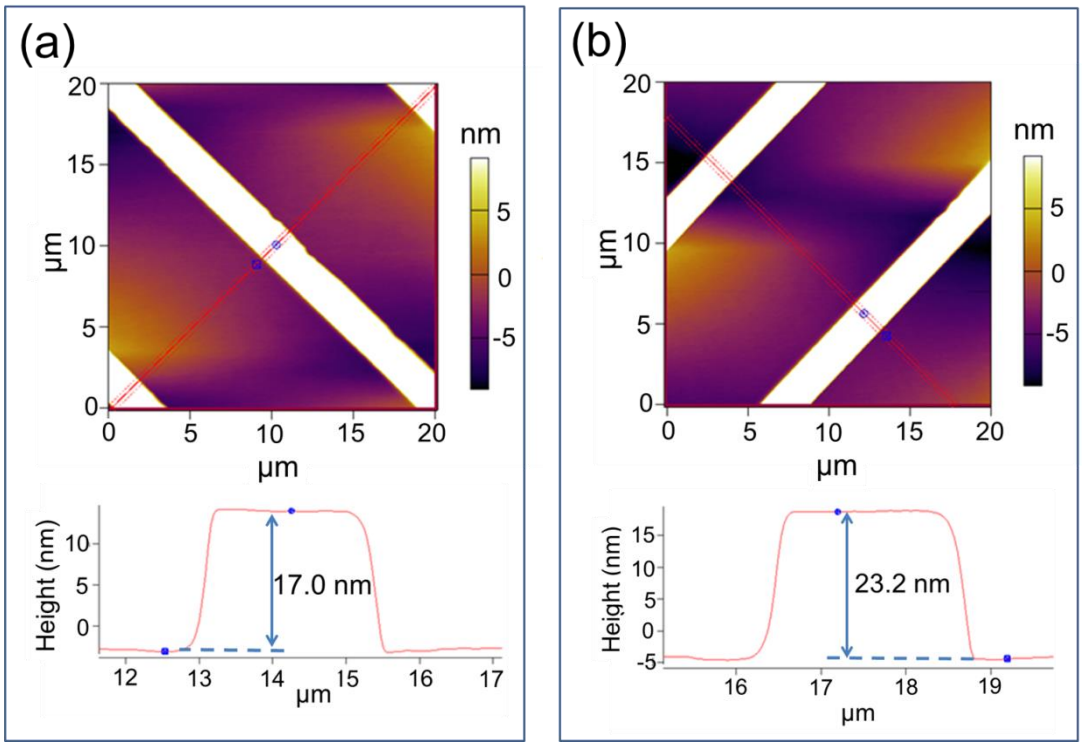

Figure 5.5 AFM images and line-scan profiles of GaAs samples with patterned Al_2O_3 stripes. (a) Before applying digital etching and (b) after applying 6 cycles of digital etching. The process details of the digital etching can be found in the text.

Digital etching is a very precise etching method with ~1 nm precision. Each cycle of digital etch consists of a room temperature oxidation process followed by an oxide removal wet etching. The oxidation, which can be done by using H_2O_2 solution [68] or a UV ozone tool [69] or an oxygen plasma asher [70], is a self-limiting process which stops at about 1–1.6 nm from

the surface depending on the material. Therefore each etching cycle can precisely remove a very thin layer of material.

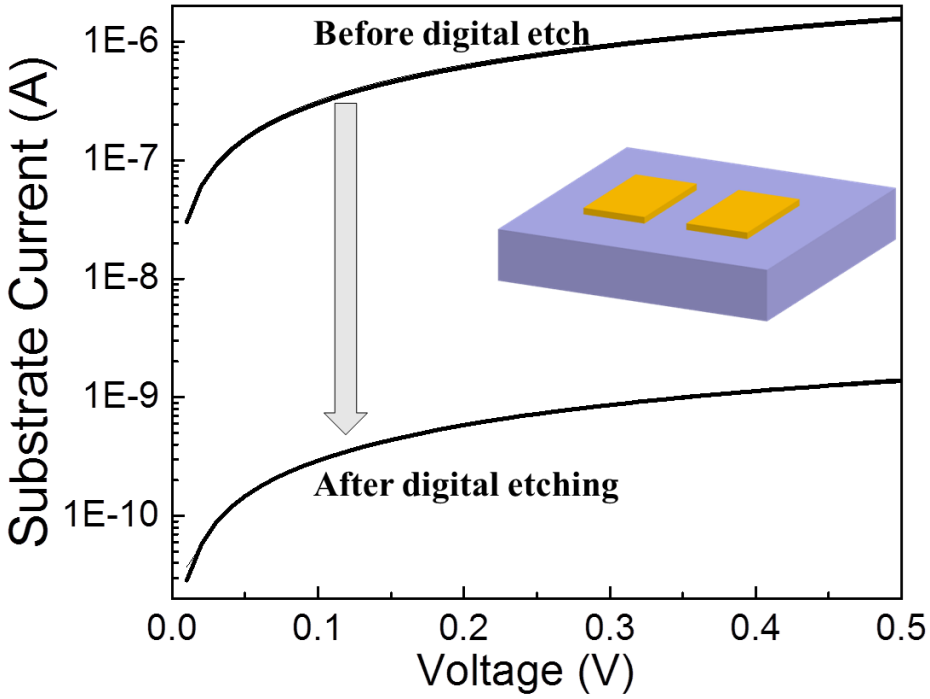

Figure 5.6 Substrate leakage current measured between two contact pads that are not connected by a planar nanowire (illustrated by the inset schematic device structure). The lower curve shows a significant reduction of surface leakage after applying digital etching for only one cycle.

GaAs (100) samples with patterned Al_2O_3 (deposited by ALD) stripes, which act as an etching mask on the surface, were used in order to calibrate the digital etching process. The oxidation half cycle of digital etching was done in a planar plasma asher system (Texas Instrument) at 320 W for 15 min. The resulting oxide was then removed by 1:1 HCl:H_2O etching for 30 sec to compete a full cycle of digital etching. Note that Al_2O_3 is not affected by either the oxidation or wet etching process. Figure 5.5(a) shows an atomic force microscope (AFM) area-scan image of a control sample with no digital etching applied. At the bottom of Figure 5.5(a) is a line-scan height profile along the red line on the top AFM image where the height of the Al_2O_3

stripe on GaAs is measured to be 17.0 nm. Figure 5.5(b) shows the AFM area-scan image and the line-scan height profile of a sample with 6 cycles of digital etching applied. The height of the stripes increases to ~23.2 nm due to the etching of GaAs. Therefore, the etching rate is ~1 nm/sec. Although the calibration here is done on GaAs since GaAs substrates are easily accessible, similar etching rate is expected on other III-V materials.

By applying one cycle of digital etching to the as-grown InAs nanowire sample, the substrate surface leakage current can be significantly reduced. This is shown in Figure 5.6 where current was measured between S/D contact pads that are not connected by a planar nanowire (illustrated by the inset schematic device structure). After digital etching, the current measured at 0.5 V bias is reduced by 3 orders of magnitude, from μA to nA range, which agrees with the current level carried by a S.I. GaAs substrate.

5.3 Nanowire release etching

This section considers how to reliably release the center portion of planar InAs nanowires from the GaAs substrate surface. This is a necessary step for realizing the GAA structure that provides the best gate electrostatics. A selective etchant, $NH_4OH:H_2O_2:H_2O$ (1:1:80), is used to selectively etch GaAs over InAs [71]–[73] with ALD Al_2O_3 as etching mask. The release etching process, illustrated by Figure 5.7, involves two pattern transfer steps. First a trench opening is transferred to Al_2O_3 coated on GaAs surface by BOE etching, and second, the opening is subsequently transferred on to GaAs. Note that it is difficult to preserve the width of the designed opening if the first transfer step is done by using a PMMA mask. PMMA is a commonly used resist for EBL but its adhesion on Al_2O_3 does not seem to be firm enough for it to behave as a good wet etching mask.

As shown schematically in Figure 5.7(a), extensive lateral over-etch can occur due to PMMA peeling off during etching. A SEM image of Al_2O_3 etched by BOE with PMMA mask is shown in Figure 5.8(a), where an opening on PMMA of 90 nm center width (original design, not shown in the image) ends up to be a 350-nm gap (center width) on Al_2O_3.

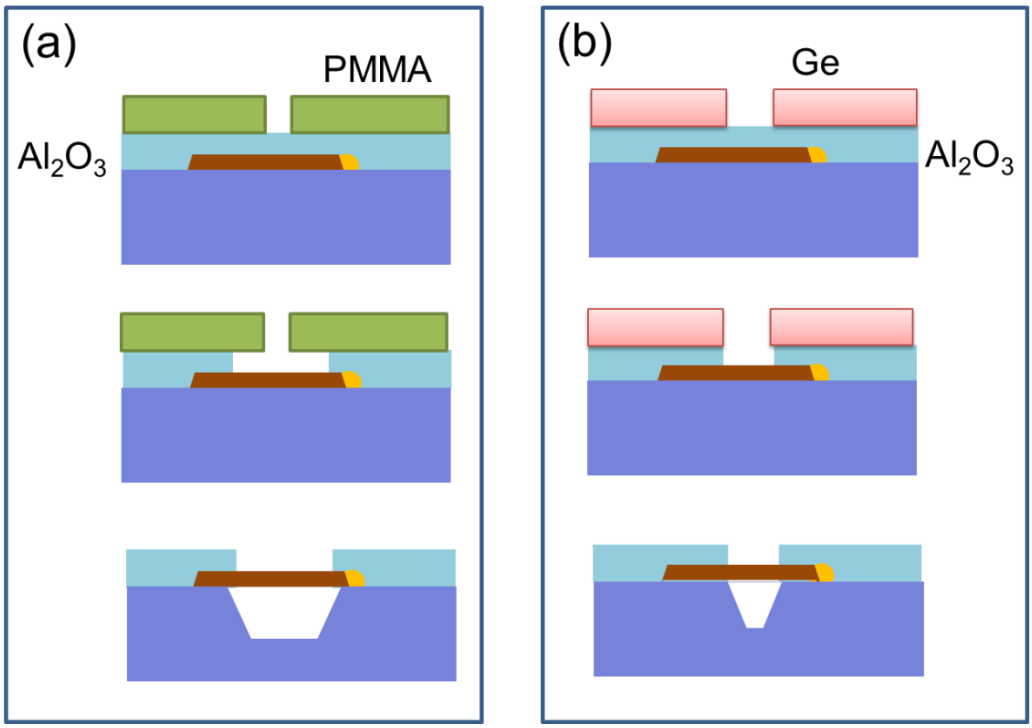

Figure 5.7 Schematic diagrams showing the nanowire release etching process. (a) With PMMA etching and (b) with Ge hard mask.

The observation above suggests using a hard mask instead of PMMA. Instead of using the traditional SiO_2 hard mask, a novel Ge hard mask fabricated by EBL, EB evaporation and lift-off is designed. There are two advantages of this method. The first is that since the gap width of the opening is directly determined by EBL, it can be well controlled. Secondly, Ge can be easily removed by H_2O_2 solution which does not attack common semiconductors such as III-Vs and Si and dielectrics such as Al_2O_3, SiO_2 and Si_3N_4. Figure 5.8(b) shows SEM images of a

sample etched with Ge hard mask. The opening, with a designed width of 100 nm, was nicely transferred to Al_2O_3 with a resulting opening width of ~110 nm (top SEM image in Figure 5.8(b)). After removing Ge by 5-min H_2O_2 (30%) etching, the opening was then transferred to GaAs by $NH_4OH:H_2O_2:H_2O$ (1:1:80) etching for 4 sec (the etching rate is ~8 nm/sec). As shown by the bottom SEM image of Figure 5.8(b), the opening was precisely transferred from Al_2O_3 to GaAs.

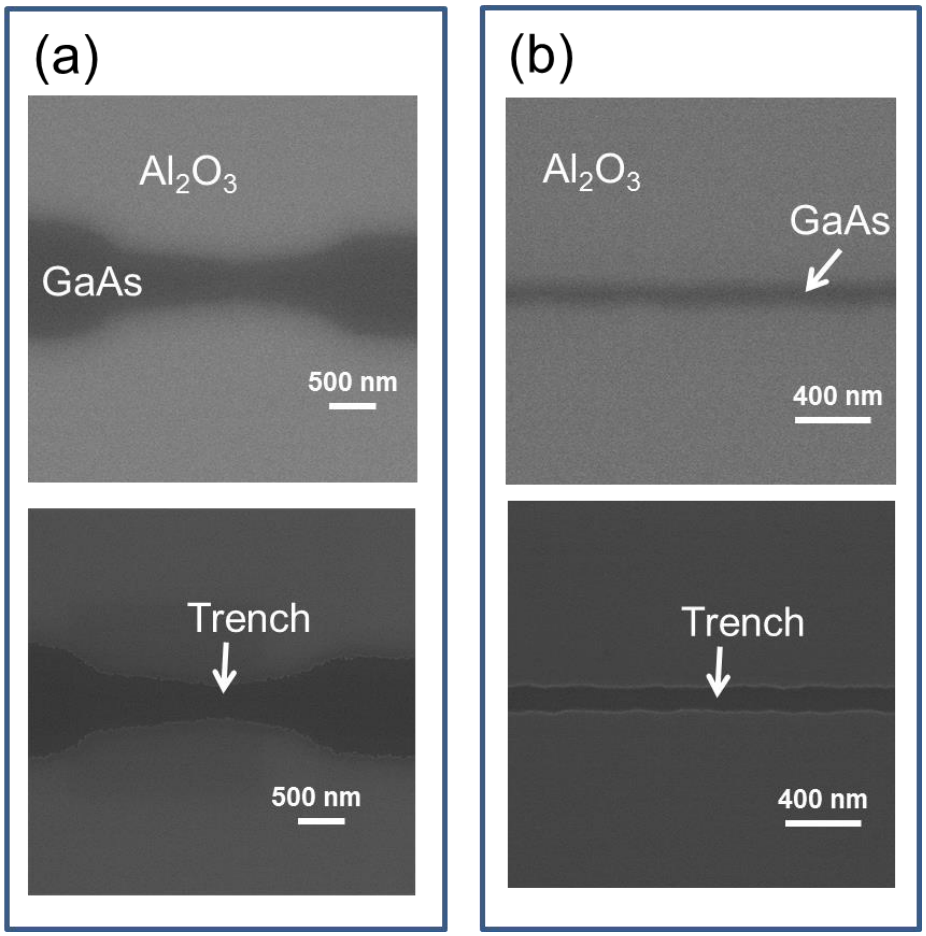

Figure 5.8 (a) SEM images of a trench opening on Al_2O_3 by BOE etching with PMMA mask (top) and the same trench subsequently transferred to the underlying GaAs (bottom) by $NH_4OH:H_2O_2:H_2O$ etching. (b) SEM images showing the pattern transfer results by using Ge hard mask.

5.4 Fabrication scheme for GAA devices

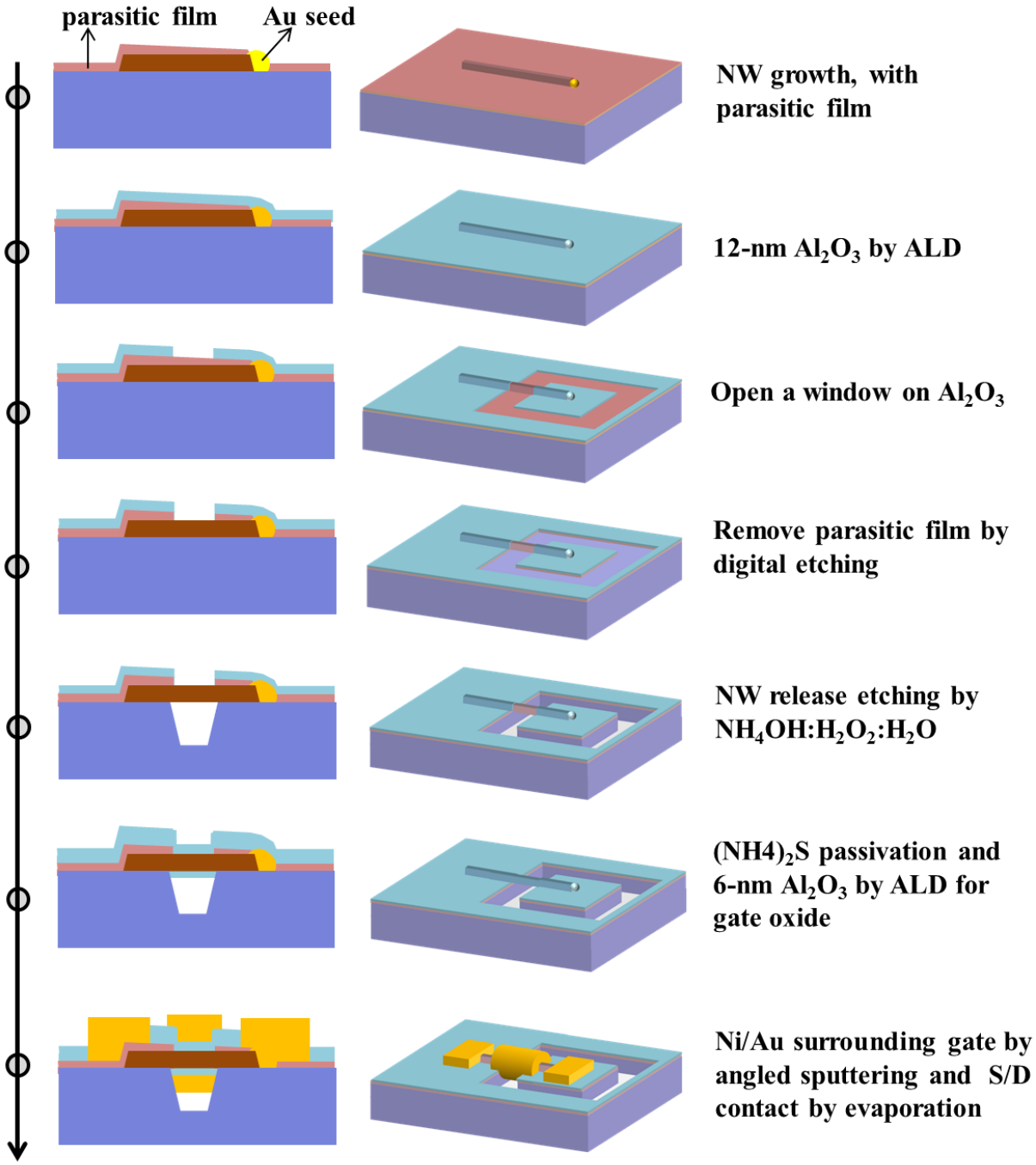

Figure 5.9 Step-by-step schematic diagrams illustrating the fabrication process for a GAA InAs planar nanowire MOSFET. Side-view cross-sectional device structures are shown on the left while the tilted view schematics are shown in the right column.

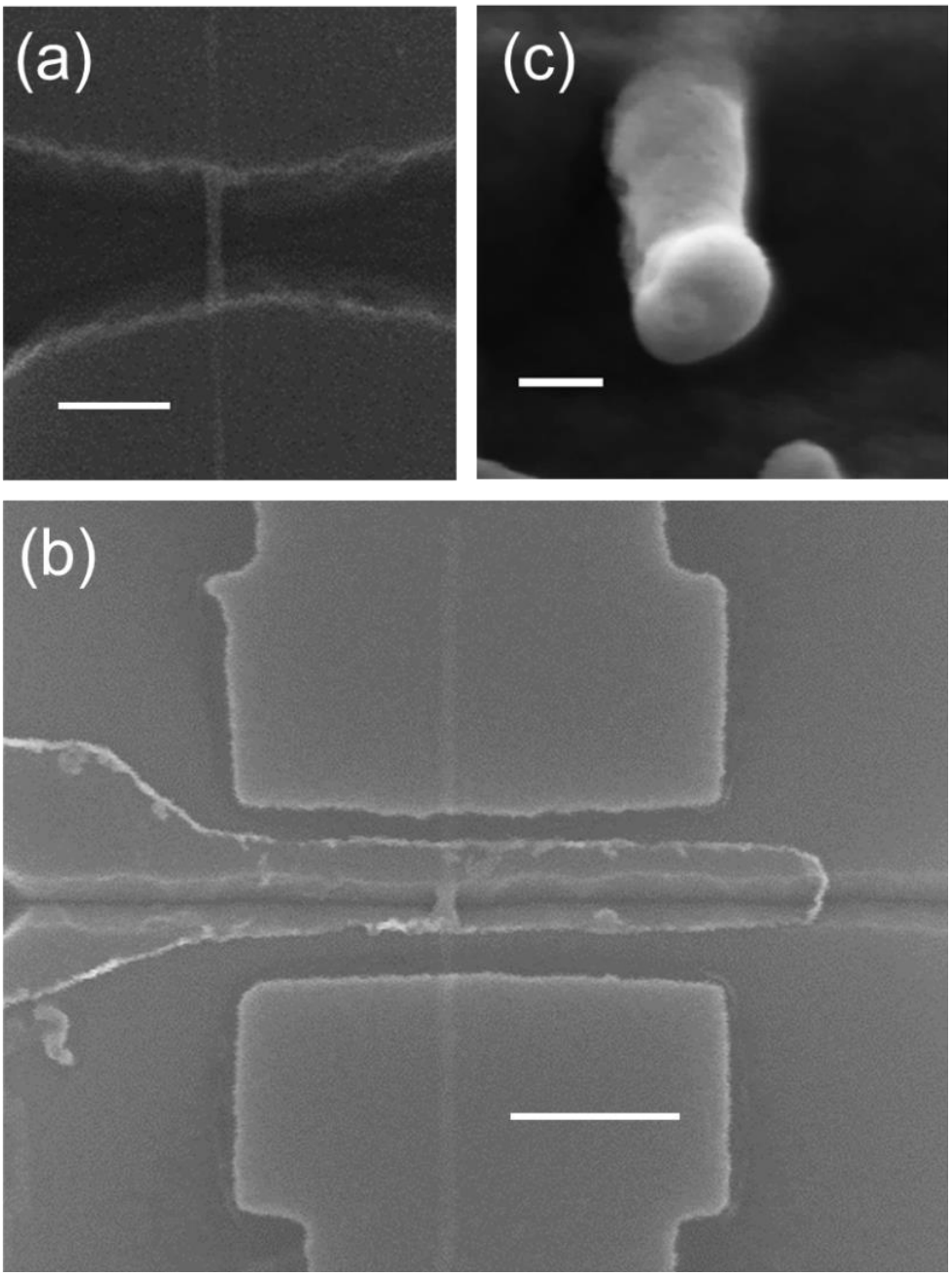

Figure 5.10 (a) SEM image showing a nanowire hanging over the trench after releasing. (b) Top-view SEM image of a fabricated planar nanowire MOSFET device. (c) Cross-sectional SEM image of a fabricated nanowire device with conformal gate metal coating. Scale bars are 300 nm, 400 nm and 50 nm for (a), (b) and (c), respectively.

After the digital etching and release etching processes have been developed, the InAs planar nanowire GAA MOSFET can be fabricated. The detailed fabrication process is

schematically shown in Figure 5.9. First, a 12-nm Al_2O_3 layer is deposited by ALD to be the etching mask for subsequent steps. A ring-shaped window is then opened on Al_2O_3 by either PMMA mask or Ge hard mask. In order to release the InAs nanowire from the underlying GaAs substrate, the exposed InAs parasitic film is removed by digital etching. This is to both remove the substrate surface leakage path and expose the GaAs beneath for trench etching. Here the oxidation half cycle is done at room temperature in a UV ozone cleaner (BioForce Nanoscience, Inc.) instead of the oxygen plasma asher to avoid any plasma induced damage to InAs planar nanowires. The oxide is then removed by 1:1 $HCl:H_2O$ etching for 30 sec. A trench is then formed on GaAs to release the center portion of the nanowire by selectively etching GaAs against InAs by $NH_4OH:H_2O_2:H_2O$ (1:1:80). Figure 5.10(a) shows a SEM image of a nanowire after releasing. Al_2O_3 is then deposited by ALD at 220 ^oC as the gate oxide, followed by the Ni/Au gate metal deposition by sputtering to provide conformal gate contact, as shown previously in our work [24]. Finally, Ni/Au is evaporated for source and drain contacts after Al_2O_3 is removed from the S/D region. No annealing is performed in the fabrication process. Although the current process leaves a large area of substrate covered by the parasitic film (bottom structures shown in Figure 5.9), which is undesired for circuit applications, in principle only the parasitic film in the S/D region can be kept by patterning. Figure 5.10(b) shows the SEM image of a completed device with ~100 nm trench width. Figure 5.10(c) shows the cross-section (after milling by focused ion beam (FIB)) of a fabricated device with the gate metal covering all around the nanowire.

Note that for all the nanowire devices fabricated by release etching, the gate length, L_g, is defined to be the trench width because the non-released gated portion cannot be well modulated (as shown in Figure 5.4(b)).

5.5 Device characterizations and analysis

Figure 5.11 shows the log-scale transfer curves (V_{ds} = 0.5 V) of InAs nanowire MOSFET devices with two different fabrication schemes. The nanowire width, *d*, of the devices is ~30 nm. The gate oxide (Al_2O_3) thicknesses, t_{ox}, are 12 nm and 6 nm for the non-released device and released GAA device, respectively. 6 nm of ALD Al_2O_3 corresponds to an equivalent oxide thickness (EOT) of ~3 nm. The black, dashed curve shows the result of a device fabricated with digital etching applied to the entire substrate. The device structure resembles that shown in Figure 5.4(a) except the parasitic InAs film is removed. Some reduction of leakage current is observed when compared to the device shown in Figure 5.5. However, the off-state current is still very large and a small I_{on}-I_{off} ratio of 10 is seen for V_{gs} = –2 V to 1 V.

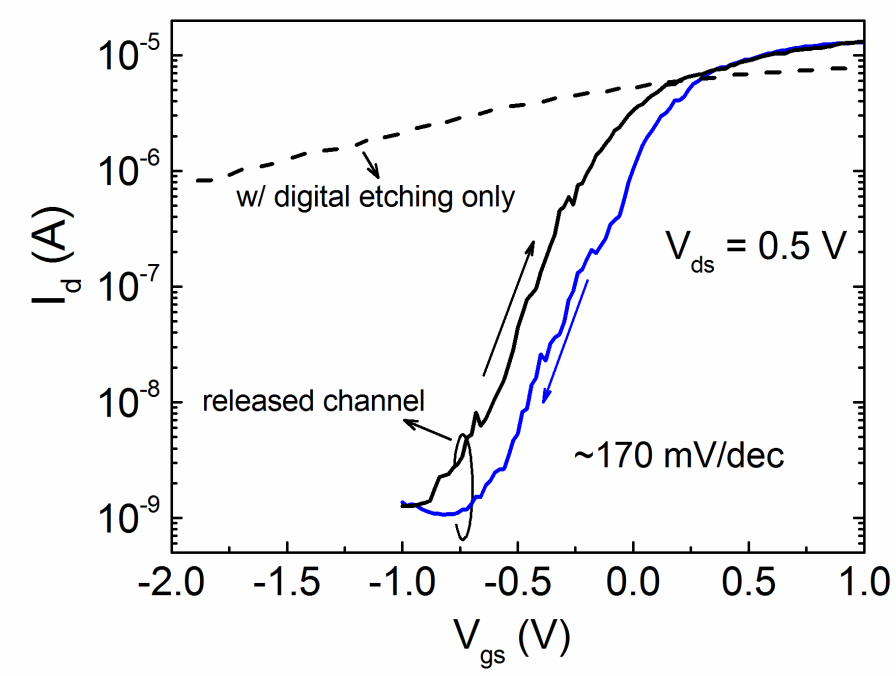

Figure 5.11 Log-scale transfer characteristics of the InAs planar nanowire MOSFETs with *d* = 30 nm and L_g = 350 nm. Hysteresis is seen between forward and backward sweeps, indicating the presence of mobile charges in the oxide. The gate oxide thicknesses are 12 nm and 6 nm for the non-released device and released GAA device, respectively.

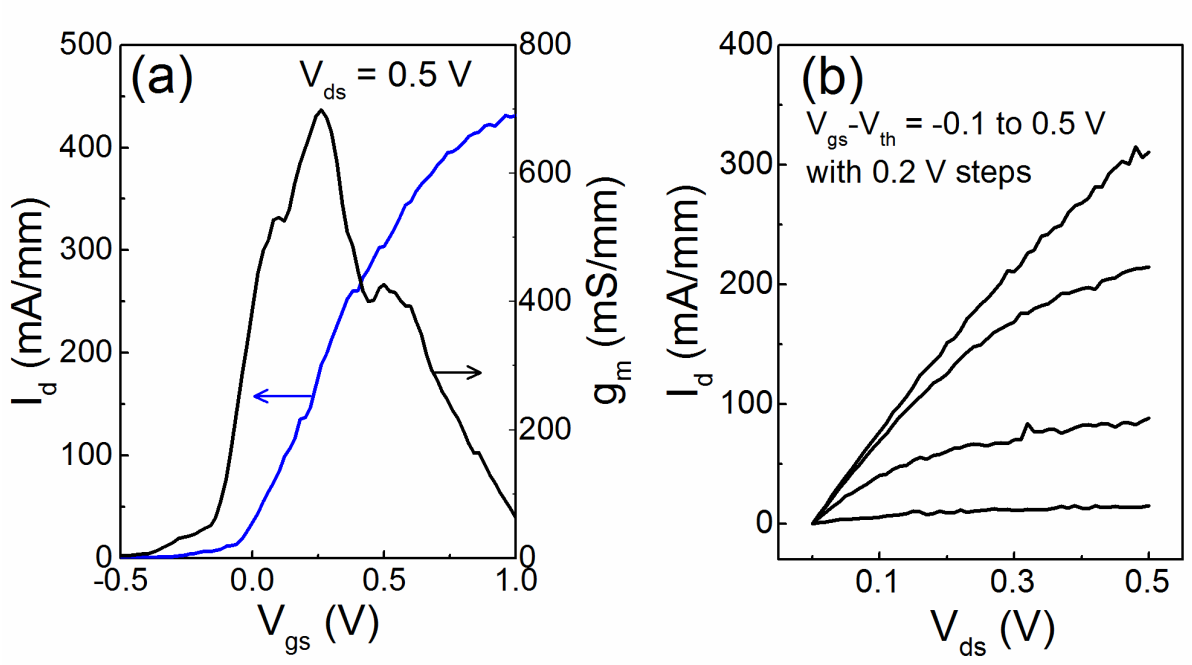

Figure 5.12 (a) Transfer and transconductance curves of the GAA device with t_{ox} = 6 nm, d = 30 nm and L_g = 350 nm. (b) Typical output curves of the device with the same dimensions. All the results are width-normalized.

Significant reduction of off-state leakage was observed only after fully releasing the nanowire channel from the substrate. Shown in Figure 5.11 by the solid curves, the I_{on}/I_{off} ratio is as high as 10^4 as V_{gs} varies from –1 V to 1 V. The subthreshold swing (*SS*) measured from the positive-sweep curve (V_{gs} = –0.6 V to –0.4 V) is ~170 mV/dec. This suggests that besides the parasitic thin film, the current leakage was also induced by the bottom interface between InAs and GaAs. It is speculated that certain interface defects pin the Fermi level of InAs close to its conduction band so that the device could not be turned off completely.

For the device with digital etching only, there was no patterned etching mask on the sample before digital etching. So the whole parasitic film including the portion on the S/D area is removed. Therefore the S/D contact is made directly on the nanowire. As seen from Figure 5.11

on the positive V_{gs} side, the on-state current of the device with digital etching only is lower than the device with both patterned digital etching (which preserves the parasitic film on the S/D area) and release etching. This observation supports the effect of parasitic film in reducing the contact resistance.

The on-state transfer curve and typical output characteristics of the GAA device are shown in Figure 5.12. The threshold voltage is ~0 V. The device shows a width-normalized drive current, I_{on}, of 300 mA/mm at V_{ds} = V_{ov} = 0.5 V and a peak width-normalized extrinsic transconductance, g_m, of 700 mS/mm. The R_{on} is measured to be 1.3 Ω·mm at V_{ov} = 0.5 V.

The *SS* and g_m reported here are decent compared to other III-V nanowire devices summarized in [74]. We can estimate the interface trap density D_{it} by

$$SS = (1+q\pi dD_{it}/C_{ox})\cdot 60 \text{ mV/dec} \tag{5.1}$$

where q is the electron charge and C_{ox} (F/cm) is the oxide capacitance per unit length along the nanowire, which can be calculated, for a cylindrical nanowire, by

$$C_{ox} = \frac{2\pi\varepsilon_{ox}}{\ln\left(1+2t_{ox}/d\right)} \tag{5.2}$$

where ε_{ox}, t_{ox} and d are the dielectric constant of the gate oxide, the thickness of the oxide and the diameter of the semiconductor nanowire, respectively. Thus, D_{it} is 1.6×10^{13} $cm^{-2}eV^{-1}$ in the device shown in Figure 5.11. For comparison, D_{it} is estimated to be 2.5×10^{13} $cm^{-2}eV^{-1}$ in [26] and 6×10^{13} $cm^{-2}eV^{-1}$ in the top-down etched in-plane InAs nanowire MOSFETs (grown on GaAs with an InGaAsSb metamorphic buffer layer) [75]. A better D_{it} of ~5×10^{12} $cm^{-2}eV^{-1}$ was reported on the best top-down InGaAs (In% is close to 53%) nanowire MOSFETs [22].

The effective electron mobility, μ_{eff}, can be extracted from the measured transfer curve at low drain bias, for example, V_{ds} = 0.05 V. The gate capacitance of a nanowire GAA structure can be computed by a 2D Poisson-Schrödinger coupled simulation at its cross section in Nextnano

[76], where a circular structure with an un-doped InAs core (d = 30 nm) an gate oxide shell (EOT = 3 nm) is considered. The gate metal work function is set to be 4.4 eV. After the charge-voltage (Q_n-V_{gs}) relation is obtained from the simulation, D_{it} can be manually added to the result. In doing this, first, the nanowire surface potential ψ_s at each V_{gs} point is calculated by

$$V_{gs} = V_{fb} + \psi_s - \frac{Q_n}{C_{ox}} \tag{5.3}$$

where V_{fb} is the flatband voltage, Q_n is the electron charge in the nanowire in C/cm, and C_{ox} can be calculated by (5.2). In an undoped nanowire structure, $q\psi_s$ can be defined to be the displacement between the mid-bandgap level E_i at the surface and the channel Fermi level, similarly as in a double-gate MOS structure [77]. The corresponding flatband voltage V_{fb} can be defined to be ($\phi_m - \chi_s - E_g/2$), where ϕ_m and χ_s are the gate metal work function and semiconductor electron affinity, respectively. Then, the new V_{gs} at each ψ_s point with the effect of D_{it} can be computed by

$$V_{gs} = V_{fb} + \psi_s - \frac{Q_n + Q_{it}}{C_{ox}} \tag{5.4}$$

where Q_{it} is the total interface charge density (C/cm) at the nanowire/dielectric interface, which can be written as

$$Q_{it} = q\int_{-\infty}^{E_{CNL}} \pi d D_{it}\left[1 - f(E, E_f)\right] \mathrm{d}E - q\int_{E_{CNL}}^{+\infty} \pi d D_{it} f(E, E_f)\, \mathrm{d}E \tag{5.5}$$

where $f(E, E_f)$ is the Fermi distribution and E_{CNL} is the surface state charge neutrality level, below which the interface states are donor-like and above which they are acceptor-like [78]. For InAs, E_{CNL} is well above the conduction band edge [79]. Assuming D_{it} is constant and E_f is well below E_{CNL}, a simple estimation of (5.5) can be

$$Q_{it} = q\pi d D_{it}(E_{CNL} - E_f) = q\pi d D_{it}(\psi_{s,CNL} - \psi_s) \tag{5.6}$$

where $\psi_{s,CNL}$ is the surface potential where E_f meets E_{CNL}. The exact value of $\psi_{s,CNL}$ is not important here since it can be lumped into V_{fb} after replacing Q_{it} in (5.4) with (5.6). The new V_{fb} will later become a fitting parameter when interpreting the measurement data. The drain current I_{ds} measured at low V_{ds} can be expressed as

$$I_{ds} = \mu_{eff} \frac{V_{ds}}{L_g} \left| Q_n \left(V_{gs} \right) \right| \tag{5.7}$$

So based on (5.3) and (5.7), the measured I_{ds}-V_{gs} transfer curve can be fitted by the simulated Q_n-V_{gs} relation of (5.4) with μ_{eff} and V_{fb} being the two fitting parameters. Figure 5.13 shows an excellent fitting result where a good agreement between the measured and simulated data is seen. The transfer curve is measured at V_{ds} = 0.05 V on an InAs planar nanowire MOSFET with the nanowire width, oxide thickness and gate length being 30 nm, 6 nm, and 350 nm, respectively. D_{it} (1.6×10^{13} $cm^{-2}eV^{-1}$ as extracted from Figure 5.11) was added to (5.4) to simulate the transfer-curve stretch-out.

The μ_{eff} obtained from the fitting is 2730 $cm^2/V\cdot s$, which is much higher compared to those in the inversion layer of a Si MOSFET (typically in the range of several hundred in $cm^2/V\cdot s$ [2]) and those measured from Si nanowire GAA MOSFETs [80], highlighting the benefit of a III-V channel. But it appears to be a little lower than the electron mobility in InAs nanowires with similar diameters extracted from long-channel devices (L_g ~ 10 μm) [27]. The reason could be related to the limit imposed by ballistic mobility [81] as a relatively short L_g (350 nm) is presented here. In addition, the pronounced effect of S/D series resistance in relatively short-channel devices could lead to an overestimation of electrical field and thus to underestimation of mobility.

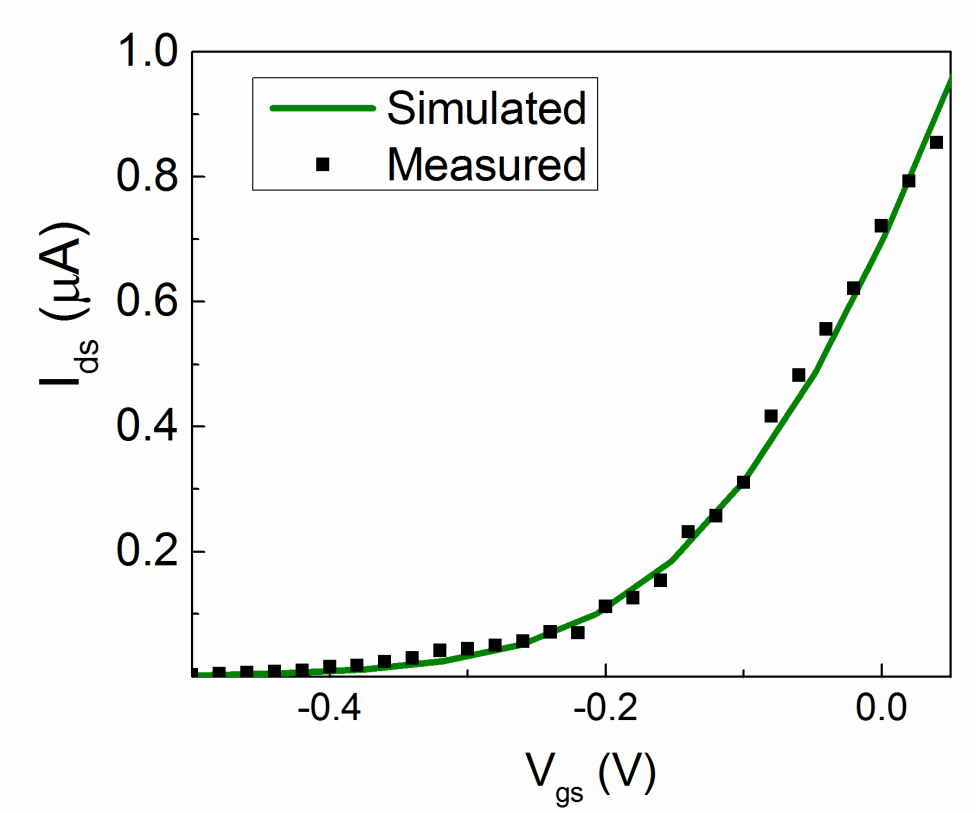

Figure 5.13 Fitting result for effective mobility estimation. A good agreement between the measured and simulated data is seen. The nanowire width, oxide thickness and gate length are 30 nm, 6 nm, and 350 nm, respectively. The transfer curve is measured at V_{ds} = 0.05 V.

Lastly, Figure 5.14 shows the transfer and tranconductance characteristics of a down-scaled InAs planar nanowire MOSFET with $d \approx 22$ nm and $L_g \approx 75$ nm. The thickness of Al_2O_3 gate dielectric is scaled down to 4 nm compared to 6 nm in the device shown in Figure 5.12. A clear improvement of device performance can be seen. The width-normalized drive current at V_{ov} = 0.5 V and V_{ds} = 0.5 V is ~400 mA/mm and the peak extrinsic transconductance is ~830 mS/mm.

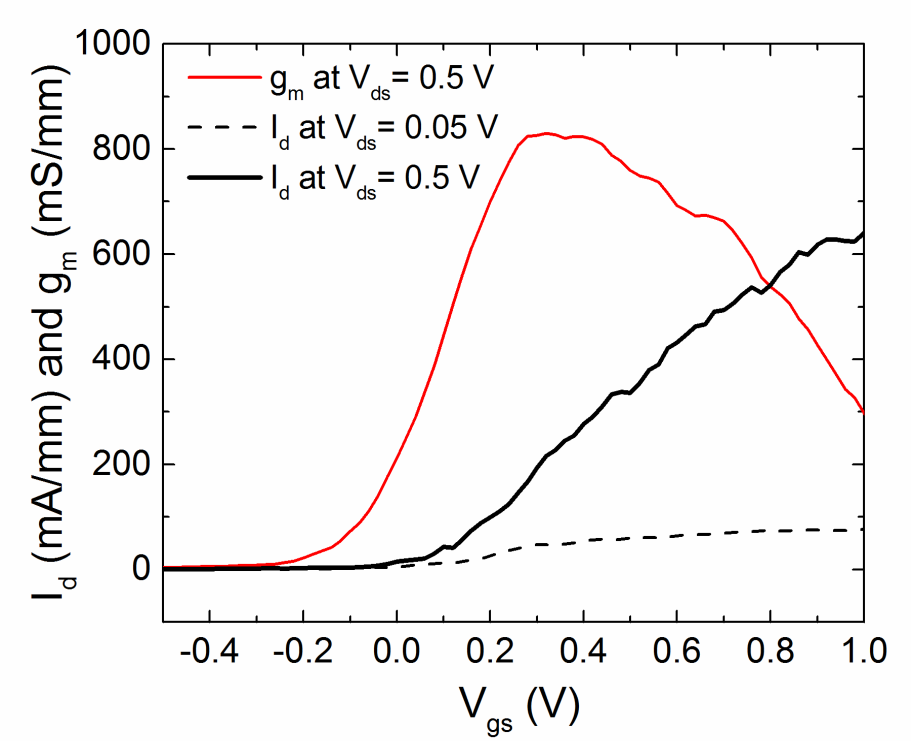

Figure 5.14 Transfer and tranconductance characteristics of a down-scaled InAs planar nanowire MOSFET with t_{ox} = 4 nm, d = 22 nm and L_g = 75 nm. The device shows a performance improvement in both drive current and peak transconductance, which are normalized by nanowire width.

CHAPTER 6 – FUTURE WORK

6.1 Further performance improvement of InAs nanowire MOSFETs

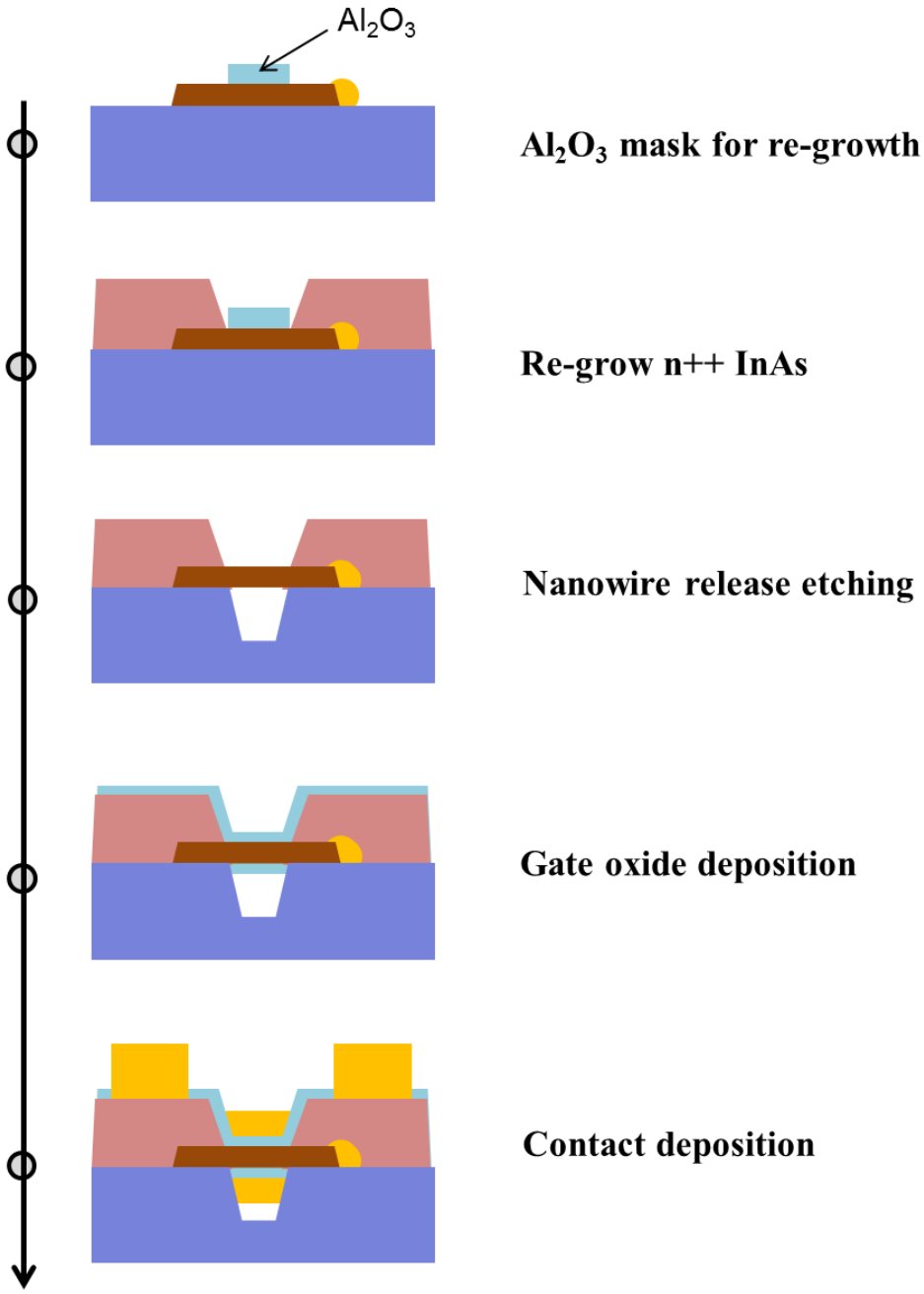

Figure 6.1 Schematic diagrams illustrating the process flow for fabrication of planar nanowire GAA MOSFET with S/D re-growth.

The oxide/semiconductor interface trap density (D_{it}) needs to be reduced in order to further improve both off-state and on-state performance of InAs planar nanowire MOSFET devices. As estimated in Chapter 5, D_{it} is on the order of 10^{13} $cm^{-2}eV^{-1}$, which is about three orders of magnitude larger than that of Si/SiO_2 interface. A post-oxide-deposition annealing in the forming gas environment, which has been reported to be effective in reducing D_{it} for InGaAs nanowires [82], may be employed.

In addition, S/D series resistance needs to be scaled down for short channel devices. The current fabrication scheme (shown in Figure 5.9) results in relatively long S/D extension regions (Figure 5.10(b)). This brings additional parasitic resistance, R_{ext}, which, together with the contact resistance (R_c) between metal and the undoped nanowire, adds to the total series resistance. The parasitic InAs thin film grown simultaneously during nanowire growth should help reduce both R_{ext} and R_c. However, due to its thin nature, the effect could be limited, especially for short-channel devices. Employing S/D re-growth technology should help further reduce R_c and R_{ext} and boost on-state performance [24]. Figure 6.1 shows a proposed process flow for fabricating an InAs planar nanowire MOSFET with re-grown S/D. Re-growth can be done before the nanowire release etching. First, SiO_2 or Al_2O_3 is deposited and patterned as growth mask. Then n++ InAs is selectively grown on S/D openings. The material re-grown is not necessarily of high crystalline quality but has to be highly doped in order to reduce both R_c and R_{ext}. Then, nanowires can be released from the substrate followed by deposition of gate oxide and metal contact layers, similarly as shown in Figure 5.9.

6.2 Yield improvement for heterogeneous InAs nanowires

The yield of high-quality InAs planar nanowires grown on GaAs is not perfect at this point. Some nanowires do not grow in a straight line. Instead, they form a random, zigzag

trajectory on the substrate surface. This is shown in Figure 6.2(a) where the growth was done at 340 °C under 950 mbar. The V/III flow ratio was optimized for the yield of straight nanowires. The TMIn and AsH_3 flows were 30 sccm and 7 sccm, respectively. The TMIn bubbler temperature and pressure were 17 °C and 1000 mbar. The reason why zigzag nanowires are present is presumably related to the heterogeneous nature as it has been shown in Chapter 2 that homogeneous GaAs planar nanowire growth can be perfect. In fact, InAs planar nanowires also grow very well on their native substrate [49].

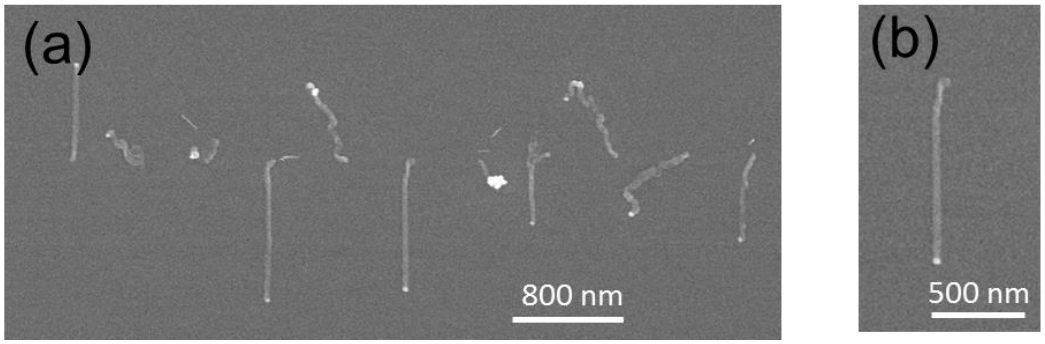

Figure 6.2 SEM images of InAs planar nanowires directly grown on the GaAs (100) substrate. The growth was done at 340 °C under 950 mbar. (a) An array of nanowires containing both straight and non-straight wires. (b) A magnified image showing a nanowire in (a) for highlighting the starting segment.

During the oxide desorption annealing step at the very beginning of the growth run, Au seed dots form eutectic droplets with Ga atoms from GaAs substrate. The droplet has a (111)B interface with the substrate. This would complicate the initial stage when TMIn is introduced for InAs growth because planar InAs nanowires grow along projections of <111>A and have a (111)A growth front interfaced with the seed. This is shown in Figure 6.2(b) where the nanowire struggles to change the growth direction at the beginning of the nanowire growth.

The initial oxide desorption step, therefore, may be skipped to avoid this complication. The native oxide on the substrate surface can be removed by wet etching right before samples are loaded into the reactor. Another possible way of preventing Ga from entering Au seed is to introduce In into Au by pulsing TMIn before raising the temperature for oxide desorption. According to K. Dick *et al*. [83], the presence of In in Au could greatly reduce the Ga solubility. Experiments based on the speculations above, however, did not show a very significant yield improvement of InAs planar nanowire growth on GaAs.

Other than surface chemistry, strain effect induced by the huge lattice match between InAs and GaAs may also affect the growth. A less-mismatched substrate such as InP, which has a 3% lattice mismatch to InAs, may be used. Figure 6.3 shows the primary result of InAs planar nanowire growth on an InP (100) substrate. The growth was done at 380 °C seeded by randomly dispersed 10-nm colloidal Au nanoparticles. The native oxide was removed by BOE before growth and no oxide desorption step was included.

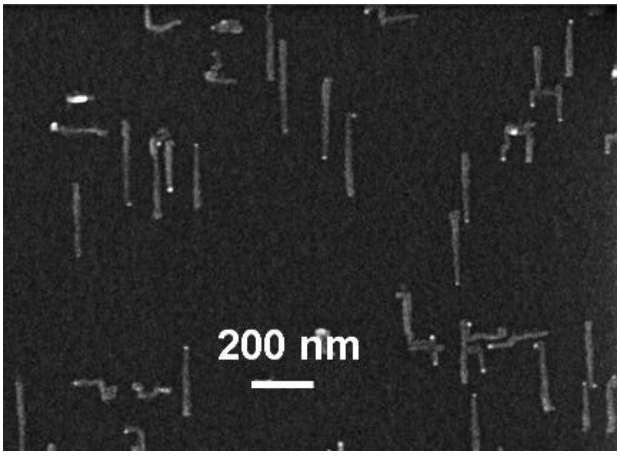

Figure 6.3 InAs planar nanowires grown on an InP (100) substrate. The growth, seeded by randomly dispersed 10-nm colloidal Au nanoparticles, was done at 380 °C without oxide desorption.

The yield of InAs planar nanowires on InP appears to be better than that on GaAs, highlighting the potential of achieving planar nanowire arrays on InP. Still, some nanowires grow along the wrong directions. Further growth studies including mapping the growth parameter space are needed.

6.3 Use a CMOS compatible seed nanoparticle

Using Au seed particles for growth is one of the major concerns when considering moving this technology to Si substrates because Au is a notorious deep-level impurity in Si. Actually it is possible to use CMOS compatible metals to seed VLS growth, such as Ni. Ni-catalyzed high-quality VLS InAs nanowires have been demonstrated [84]. Indium-seeded VLS growth of InAs nanowires can also be an option [85]. So far, neither Ni-seeded nor In-seeded growth has been studied as extensively as Au. The study in Chapter 2 suggests that the reason why nanowires stay in-plane is mainly due to the adhesion between the liquid-form seed particle and the substrate surface [86]. The adhesion alters the original growth direction by "pinning" nanowires on the surface, so it is plausible to grow planar nanowires using other seeds if the growth condition (pressure, temperature, V/III, etc.) for "pinning" can be found.

6.4 Growth of p-channel GaSb nanowires and their integration with InAs

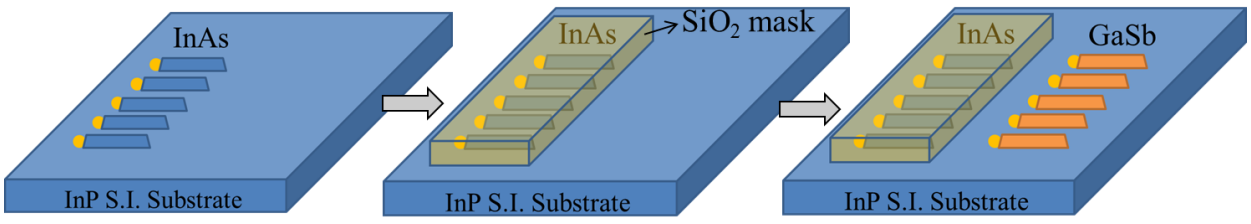

Figure 6.4 Vision for the future of the SLE technology. Both n-channel and p-channel nanowires are integrated on the same substrate.

While InAs is promising for n-MOSFET devices due to its ultra-high electron mobility, practical CMOS applications require comparable p-channel materials. Another type of III-V material, GaSb, has a room-temperature hole mobility of about 1000 cm^2/Vs, which is much higher than that in Si. Therefore, GaSb can be a good candidate for future p-MOSFETs [87], [88]. It is anticipated that the same SLE mechanism can be applied to GaSb growth. The ultimate goal is to integrate both InAs and GaSb planar nanowires on the same substrate such as InP (Figure 6.4). One possible way of integrating a second material (shown by Figure 6.4) is to first selectively cover the existing nanowires with a mask, such as SiO_2. Then the second growth will not affect the existing nanowires and no parasitic shell of the second material will cover the first nanowires.

APPENDIX A – MOCVD GROWTH OF GaAs THIN FILMS ON GaAs (110) SUBSTRATES

This appendix presents a study of MOCVD growth of GaAs thin films on GaAs (110) substrates. Unlike the GaAs (100) surface, the (110) surface, which is actually the natural cleavage facet, is free of As dimers and intrinsic surface defects [89], and therefore is promising for MOS device applications. Those facts lead to interest in the growth study on (110) surfaces. All the growth runs in this study were done under 100 mbar reactor pressure.

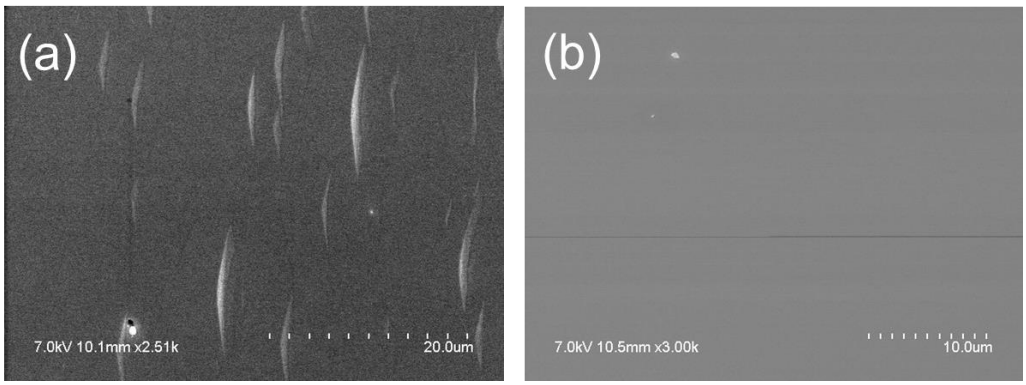

Figure A.1 Top-view SEM images of the GaAs (110) surface grown at (a) 680 °C and (b) 650 °C.

Figure A.1(a) shows a top-view SEM image of the GaAs (110) sample grown at 680 °C with a V/III molar flow ratio of 25. A rough surface with stripe-like structures is seen from the image. However, this kind of rough surface was not seen on the (100) sample grown in the same run. When the growth temperature was reduced to 650 °C, a smooth surface was achieved on the (110) substrate (Figure A.1(b)).

The growth rate on (110) surfaces was found to be slower than that on (100). For the growth done at the temperature of 650 °C with the TMGa molar flow rate of 2.15×10^{-4} mol/min, a growth rate of 1.49 nm/s was measured on the (110) surface whereas it was 1.61 nm/s on (100).

Another major difference between the growth on (110) and (100) substrates is the Si dopant incorporation efficiency. Si_2H_6 was used in our experiments as the n-type dopant precursor. As shown in Figure A.2, for the same Si_2H_6/TMGa flow ratio, the resulting dopant concentration on the (110) surface is considerably lower than that on (100). All the growth runs in the doping study were carried out at 650 °C.

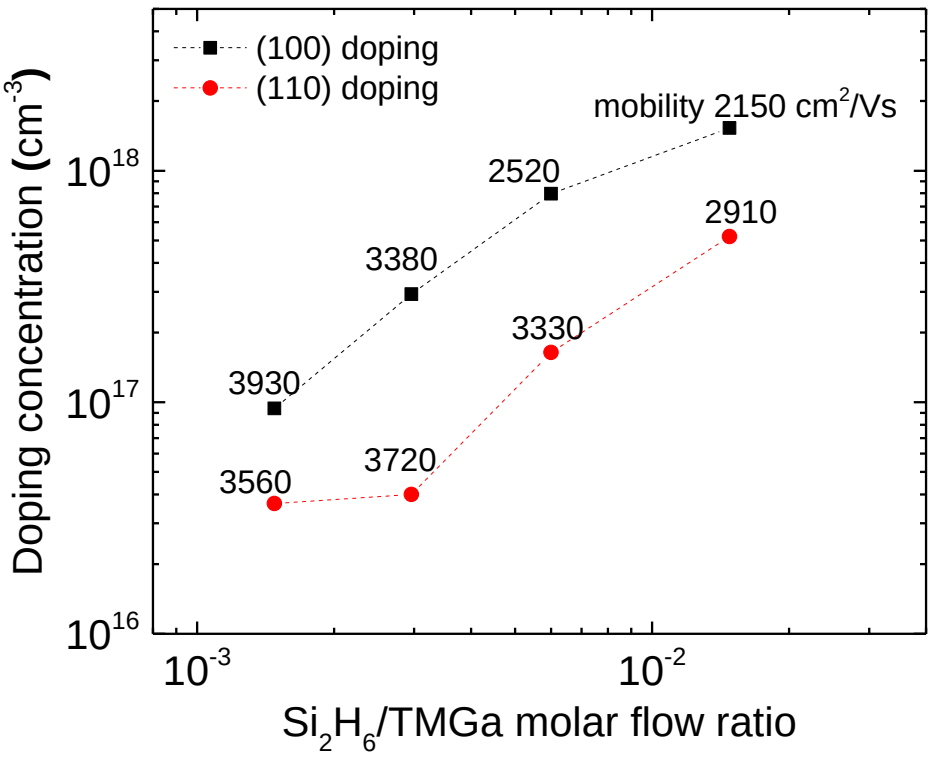

Figure A.2 Comparison of Si dopant incorporation efficiency between (110) growth and (100) growth. All growth runs were done at 650 °C. The doping concentration was obtained from Hall measurement. Hall electron mobilities are also labelled (adjacent to each data point) for each sample.

APPENDIX B – FABRICATION PROCESS FOR InAs PLANAR NANOWIRE GAA MOSFETS

This appendix describes a complete and detailed process flow for the fabrication of InAs planar nanowire GAA MOSFETs. The key steps have been outlined in Chapter 5. Here, detailed processing conditions are provided, which could serve as references for future device development.

1. Pattern Au dot arrays on a GaAs (100) S.I. substrate.

(1) PMMA preparation: pre-bake the sample at 200 °C for 2min, spin-coat PMMA (950K A2) at 2500 rpm for 60 s, then bake the sample at 200 °C for 2 min.

(2) EBL by Raith e-Line. Make sure the arrays have the correct orientation (example pattern file: common\GDS files Chen\E60\). Column conditions: voltage = 25 kV, aperture = 10 μm, WD = 7 mm.

(3) Develop for 60 s.

(4) Au evaporation by CHA evaporator: ~ 5 nm (make sure the crucible is clean).

(5) Lift off by Remover PG. This is usually done very quickly (several minutes) because Au film is very thin.

2. InAs planar nanowire growth (example recipe: G171).

(1) First make sure the beakers are clean. Clean them by piranha solution if needed and make sure they are dry before use.

(2) Perform the standard cleaning procedure for patterned VLS growth. First soak the sample in Remover PG heated by a hotplate (set to 120 °C) for 10 min and then do a 10-min sonication. Repeat the two steps above for at least 1 hr.

(3) Immediately before loading the sample into the reactor, remove the native oxide by HCL:H_2O (1:1) etching for 30 s.

(4) Grow InAs planar nanowires by Aixtron 200/4 MOCVD reactor.

3. Coat the as-grown sample with ~12 nm Al_2O_3.

(1) Remove the native oxide with HCL:H_2O (1:1) or BOE (10:1).

(2) Deposit Al_2O_3 in Savannah ALD at 220 °C for 125 cycles. Use the recipe "Al2O3_ChenTMAfirst".

4. Create markers for alignment use.

(1) PMMA preparation: pre-bake the sample at 180 °C for 2 min, spin-coat PMMA (950K A4) at 2500 rpm for 60 s, then bake the sample at 180 °C for 80 s.

(2) Maker pattern exposure by Raith. Column conditions: voltage = 10 kV, aperture = 30 μm, WD = 10 mm.

(3) Develop for 60 s.

(4) Evaporate 100 nm Au by CHA evaporator.

(5) Lift off.

5. Sample imaging for alignment use. In this step, SEM images are taken to determine the relative position of nanowires with respective to the markers. All the EBL steps below are based on this step.

This step has to be done in Raith (not Hitachi S-4800) because the EB current in Raith is very small so the induced damage can be minimized. Except for this step, avoid exposing nanowires under EB before the final electrical measurement. Use "image" command in Raith software (left computer). Use 1024×1024 resolution, and 20×20 μm^2 or 30×30 μm^2 (preferred) image size.

6. EBL patterning for Ge hard mask

(1) PMMA preparation: pre-bake the sample at 200 °C for 2 min, spin-coat PMMA (950K A2) at 3000 rpm for 60 s, then bake at 200 °C for 2 min.

(2) Example pattern file for exposure: common\GDS files Chen\ G171-B Ge mask exposed Exposure\. Column conditions: voltage = 10 kV, aperture = 20 μm and WD = 10 mm. Use x-step = y-step = 10 nm.

(3) Develop for 55 s.

(4) Immediately load the sample into CHA evaporator to deposit 20 nm Ge.

(5) Lift off.

7. Ring-shape patterning by EBL. (This is for later use in order to create a ring-shaped trench to isolate source and drain.)

(1) PMMA preparation: first pre-bake the sample at 180 °C for 2min, spin-coat PMMA (950K A4) at 3500 rpm for 60s, bake the sample at 180 °C for 25 min.

(2) Example pattern file for exposure: common\GDS files Chen\ G171-B ring shape pattern EXPOSED\. Column conditions: voltage = 10 kV, aperture = 20 μm, WD = 10 mm.

(3) Develop for 60 s.

8. Remove the exposed Al_2O_3 to expose the surface underneath (GaAs covered by a thin InAs layer) by BOE (10:1) etching for 27 s.

9. Remove PMMA by Remover PG and then etch away Ge by 30% H_2O_2 solution (5 min).

10. Use digital etching to remove the top InAs parasitic thin film.

(1) UV ozone oxidation for 15 min.

(2) HCL:H_2O (1:1) etching for 30 s to remove the oxidized top material.

(3) One cycle is usually enough.

11. Nanowire release etching.

(1) Release etching by NH_4OH:H_2O_2:H_2O (0.5 ML: 0.5 ML: 40 ML) for 24 s. The etching rate is roughly 7–8 nm/s but seems to become slower as the etching proceeds.

(2) Inspect the sample by optical microscope. A very tiny line (trench) should be visible across the nanowire. It could very unclear if the trench is very narrow.

12. Perform one more cycle of digital etching.

13. BOE (10:1) etching for 10 s. This etches about 6 nm of the Al_2O_3 initially deposited.

14. Passivate the nanowire surface by soaking in $(NH_4)_2S$:H_2O (1:3) solution for 10 min.

15. Deposit Al_2O_3 as gate oxide by ALD, by recipe "Al2O3_ChenTMAfirst".

16. Gate lithography

(1) PMMA preparation: first pre-bake the sample at 180 °C for 2 min, spin-coat PMMA (950K A4) at 3000 rpm for 60 s, then bake the sample at 180 °C for 80 s.

(2) Example pattern file for exposure: common\GDS files Chen\ G171-B gate\. Column conditions: voltage = 10 kV, aperture = 20 μm and WD = 10 mm. Use x-step = y-step = 10 nm.

(3) Develop for 70 s.

17. Gate metal deposition by sputtering

(1) Use AJA sputter in MRL. Use 3 mTorr pressure. First deposit Ni at 150 W for 3 min and then deposit Au at 50 W for 4 min and 10 s. In AJA sputter, the source target is facing the sample at an angle so it should help make the GAA structure.

(2) Lift off. It might take a while because the opening area on PMMA is so small.

18. S/D patterning by EBL

(1) PMMA preparation: first pre-bake the sample at 180 °C for 2 min, spin-coat PMMA (950K A4) at 2500 rpm for 60 s, then bake the sample at 180 °C for 25 min. The prolonged baking is to reduce the lateral over-etching.

(2) Example pattern file for exposure: common\GDS files Chen\ G171-B SD exposed\. Column conditions: voltage = 10 kV, aperture = 20 μm and WD = 10 mm.

(3) Develop for 60 s.

19. S/D metallization

(1) Treat the sample by BOE (10:1) for 25 s to remove Al_2O_3.

(2) Deposit Ni/Au (40 nm/10 nm) in CHA evaporator.

(3) Lift off.

20. Electrical measurement

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