ARRAYS OF LATERAL P-N JUNCTION GAAS PLANAR NANOWIRE DIODES GROWN BY SELECTIVE LATERAL EPITAXY

BY

WONSIK CHOI

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2015

Urbana, Illinois

Adviser:

Associate Professor Xiuling Li

ABSTRACT

Realizing lateral p-n junction is a critical technique to fabricate electronic and optic devices. Recently, lateral p-n junctions were achieved by *ex-situ* doping on thin film or *in-situ* doping of vertical nanowire (NW). However, fabricating lateral junctions on thin film are less effective due to the difficulties in defining abrupt junction geometry and escaping physical damages from the post-doping process. Utilizing monolithically grown lateral p-n junction vertical NW also has problem because the as-grown NWs are not compatible with conventional planar device processing.

In this thesis research, arrays of lateral p-n junction planar GaAs NW diodes grown by selective lateral epitaxy (SLE) mechanism was developed to overcome the limitations of current lateral p-n junctions in thin films and vertical NWs. Size and position controlled array of lateral p-n junction planar GaAs NWs were monolithically grown on semi-insulating GaAs (100) substrate using metal-organic chemical vapor deposition (MOCVD). The realization of lateral p-n junction diodes was confirmed by measuring two terminal I-V characteristics of the devices. The device was turned on at 1.2 V of diode voltage, and the 10^6 of rectification ratio and 2.18 of ideality factor were measured. The forward-biased current scales with the number of contacted NWs. Finally, the doping concentration modulation capability on SLE grown planar p-n NWs were verified.

To my mother, father, and sisters

ACKNOWLEDGMENTS

Firstly, I would like to thank my advisor, Professor Xiuling Li, for giving me a precious opportunity to join her group and conduct research. Professor Li vigilantly helped my research work by answering my questions and sharing her knowledge. Also, her diligence and great enthusiasm for the research has been an inspiration to me. It is a great honor for me to have such an excellent advisor in my life.

I would also like to express my thanks to a cherished group of past and present collaborators: Dr. Ryan Dowdy, Dr. Xin Miao, Dr. Chen Zhang, Dr. Kevin Bassett, Dr. Karthik Balasundaram, Kyooho Jung, Jeong Dong Kim, Seung Hyun Kim, Dr. Parsian K. Mohseni, Kelson Chabak, Paul Froeter, Moyang Li and Wen Huang. I would like to thank the Micro and Nanotechnology Laboratory staffs, including Clay Childers and Ken Tarman, for their sterling efforts to keep the cleanroom operating safely.

Finally, I would like to thank my family for their constant love and support. Thanks to their help and kindness, I was able to get through many difficulties and enjoy my studies and research without any fears or anxieties.

TABLE OF CONTENTS

CHAPTER 1 – INTRODUCTION

The p-n junction is a fundamental building-block for general semiconductor electrical and optical devices, such as transistors, laser diodes, light emitting diodes (LEDs), and solar cells. Generally, p-n junctions are created in a vertical structure through either by diffusing the gas, liquid or solid phase of each type of doping sources on the substrate sequentially in a thermal furnace or by implanting charged doping ions directly into the targeted substrate. Recently, the alternative p-n junction geometry – lateral p-n junction – has been widely investigated due to its geometric potentials, such as reducing junction capacitance by shrinking junction area and enhancing junction isolation by realizing co-planar metal contacts on the semi-insulating substrates [1]. In addition, the lateral junction geometry is necessarily desirable for specific devices such as surface acoustic wave (SAW) single photon emitters [2, 3], laterally defined optoelectronic devices on photonic integrated circuits [4–6] , and the circuit structure consists of the combination of field-effect and bipolar junction transistors (BiCMOS) [7].

However, fabricating lateral p-n junction is much more complicated and less economical than making vertical p-n junctions. Especially, conventional post-doping processes, such as thermal diffusion or ion implantation, are less affordable to the lateral junction because the inherent junction geometry easily causes a non-abrupt junction profile and gives physical damages on the targeted samples respectively. To overcome the undesired factors of *ex-situ* lateral p-n junction doping processes, techniques for in-*situ* growth of the lateral p-n junction, such as realizing lateral GaAs p-n junctions through molecular bean epitaxy (MBE) on a patterned GaAs (100) substrate using a surface facet dependent doping characteristic [8] and

fabricating a lateral p-n AlGaAs layer by *in-situ* focused ion molecular beam epitaxy (FIMBE) [9], have been proposed. However, the introduced methods still have limitations in applications to the conventional electronic and optic devices fabrication due to the difficulties in controlling the independent carrier (n and p) concentration and position, and the requirement of high-cost processing steps.

One alternative technique to achieve a semiconductor p-n junction is to utilize the semiconductor nanowires (SNWs) grown by the vapor-liquid-solid (VLS) mechanism [10]. During the VLS NW growth, doping sources can be easily introduced and switched to create p-n junctions along the axis and radius of the NW, and, recently, VLS grown GaAs lateral p-n junction NW diodes were introduced [11]. However, such VLS NWs are typically grown in the out-of-plane directions and share the common limitation as vertical p-n junctions. In order to utilize vertically grown NWs into conventional planar device fabrication platforms, researchers have given effort to transfer as grown vertical NWs on foreign substrate laterally, but the process is extremely complicated to control the position and orientation of NWs on a large scale [12–14]. Therefore, the investigation of a novel way to achieve size and position controlled epitaxially grown lateral p-n junction NW is required.

CHAPTER 2 – VLS GROWTH OF NW

2.1 VLS growth of vertical III-V NWs

SNWs have been widely researched as a novel one-dimensional (1D) material due to its unique electrical, optical and mechanical characteristics [15, 16]. Among the SNWs, particularly, the III-V compound semiconductor NWs have been garnering attentions because of their significant material properties such as, direct band gap, relative high carrier mobility than conventional group IV semiconductor materials, energy-band engineering capability, and realization of axial and radial heterostructures [17, 18]. Generally, SNWs can be synthesized by either a top-down method or a bottom-up process. Among the NW fabrication mechanisms, bottom-up grown NW has advantages of being free from the generating surface defects caused by chemical or mechanical etching steps in top-down nanowire fabrication steps. The most commonly researched bottom-up III-V NW growth is the vapor-liquid-solid (VLS) mechanism using metal-organic chemical vapor deposition (MOCVD) which can easily realize heterostructure NWs and control the doping concentration during NW growth [19, 20].

Typically, metal seed particles are used to provoke the VLS NW growth process [21]. The vapor phase of group III and V precursors are introduced into the MOCVD chamber under the certain NW growth conditions (chamber pressure and temperature), and then the seed particles form a liquid alloy. When the vapor phase sources are further introduced into the alloy, the particle reaches the supersaturation point, and the solid-phase source precipitates out to form a crystalline NW structure. In the VLS NW growth process, the diameter of NW is controlled by the size of the seed particles, while the length of NW is governed by modulating growth time.

Generally, the growth direction of NW is determined by the surface free energy at the interface between the seed particle and SNW, and the (111) and (111)B facets occupy the smallest surface energy with the group IV and III-V compound semiconductor, respectively [22, 23]. Therefore, group IV SNWs tend to be grown out-of-plane along the <111> crystal direction, while III-V SNWs are grown toward the <111>B direction on (100) or (110) substrate, and the typical VLS growth of <111>B GaAs NW growth on GaAs (100) substrate using an Au seed particle is illustrated in Figure 2.1. As already mentioned in Chapter 1, these vertically grown NWs cannot be directly applied to the electronic devices via conventional planar processes due to their inherent out-of-plane geometry. Therefore, the additional post NW growth processing, such as removing as-grown NWs from the substrate and transferring removed NW on the foreign substrate are required as described in Figure 2.2.

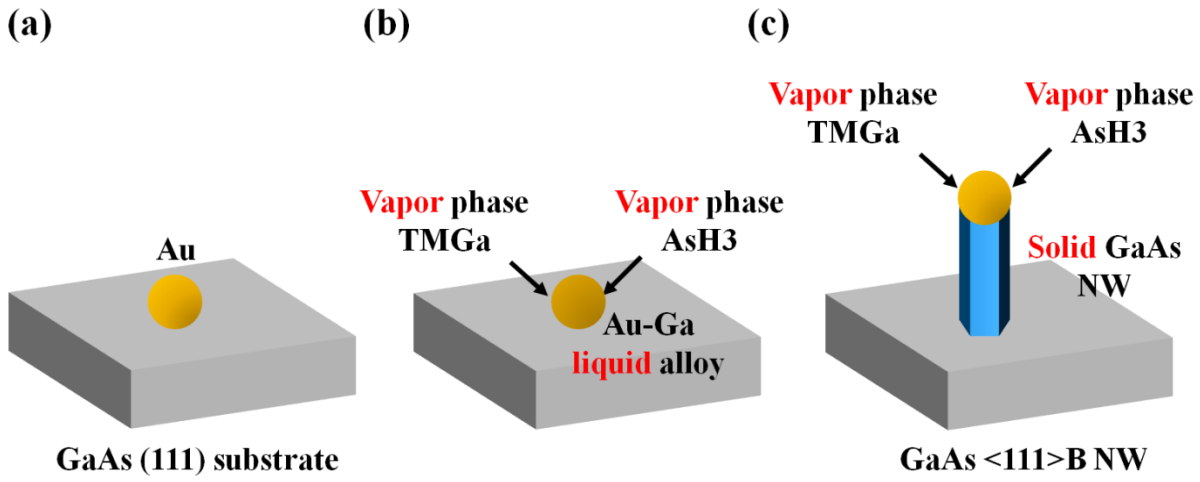

Figure 2.1: VLS growth of <111>B GaAs NW on GaAs (100) substrate. (a) Au particle is deposited on the GaAs (100) substrate. (b) The vapor-phase trimethyl-gallium (TMGa) and arsine (AsH_3) precursors are then introduced, and the gold particle forms a liquid eutectic alloy with indium at a certain growth temperature. (c) When the particle reaches the supersaturation point, the solid-phase GaAs NW is formed.

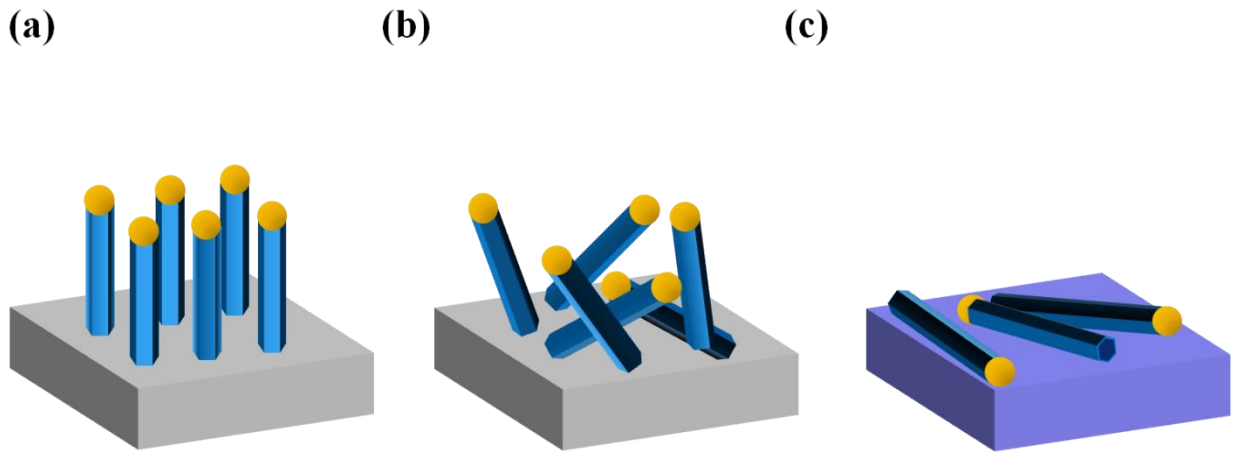

Figure 2.2: Vertical VLS grown NWs transferring process. (a) Vertical NWs are grown on the original host substrate. (b) As-grown NWs are detached from the substrate by sonication in solution. (c) Removed NWs are randomly dispersed on the foreign substrate.

2.2 VLS growth of selective lateral epitaxy (SLE) III-V NWs

2.2.1 SLE GaAs NWs on GaAs (100), GaAs (110)

To overcome the limitations in utilizing out-of-plane grown NWs to electrical and optical devices, our group has recently developed a condition for growing Au-assisted SLE planar GaAs NWs on GaAs (100) and GaAs (110) substrates using MOCVD [24, 25]. Here, we define the epitaxially grown planar NW as a SLE of NW because NW crystal growth occurs at a much faster rate at particular sites where gold seeds exist, and the in-plane NWs are grown epitaxially in a lateral direction on the substrate. Figure 2.3 shows the different directional growth of GaAs NWs under different growth temperatures on GaAs (100) and (110) substrates. When the growth temperature is lower than 430 °C, GaAs NWs are grown along the <111>B direction (Figure 2.3a), which is the traditional growth direction of III-V NWs. However, when the growth temperature is increased to 460 °C, the NWs epitaxially attached to the substrate and self-aligned

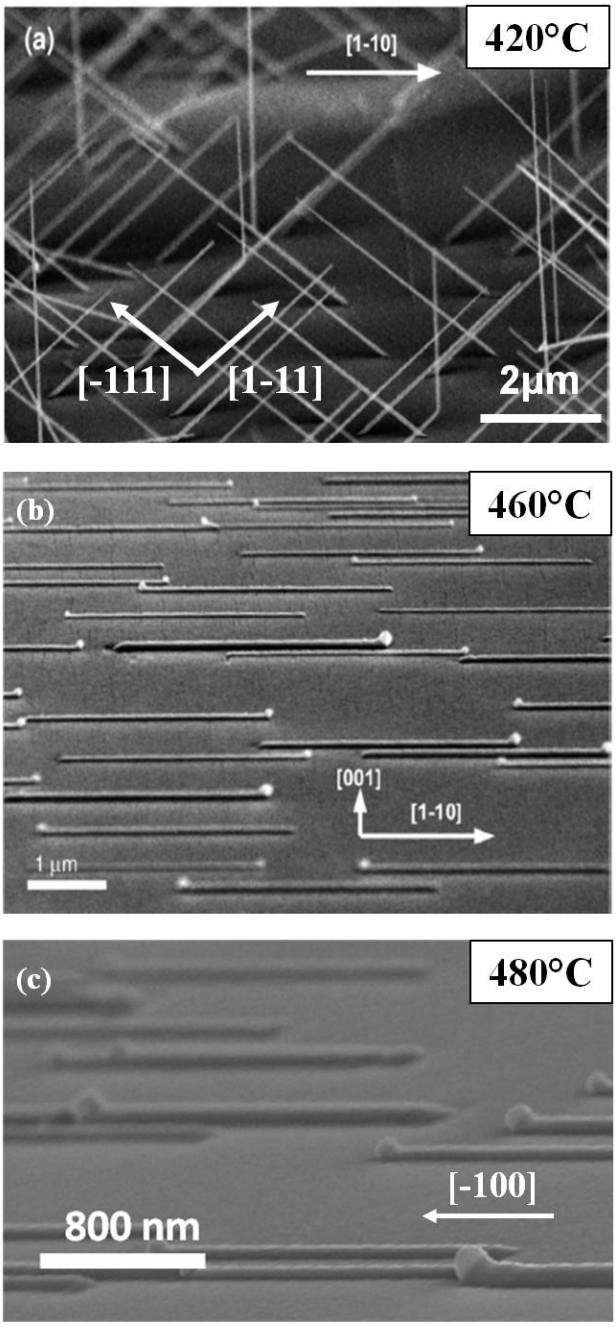

Figure 2.3: GaAs NWs grown on GaAs (100) and GaAs (110) substrates. (a) Most of GaAs NWs are grown along <111>B directions ([-111], [1-11]) on GaAs (100) substrate at 420 °C. (b) At 460 °C, GaAs NWs are epitaxially grown on the GaAs (100) substrate along <110> directions ([-110], [1-10]). (c) On the GaAs (110) substrate, planar GaAs NWs are grown along [-100] at 480 °C. Images were reproduced from Reference [24, 25].

SLE GaAs NWs grow along either the [-110] or [1-10] direction (Figure 2.3b) [24]. On the GaAs (110) substrate, planar NWs are grown unidirectional along the [-100] direction under optimized SLE growth conditions (Figure 2.3c) [25]. The low-magnification TEM image of a planar NW (Figure 2.4a) clearly shows that the entire NW is perfectly attached and grown along the [1-10] direction, and the high-resolution TEM (HR-TEM) image (Figure 2.4b) indicates that the SLE grown NW does not have misfit dislocations with only a small number of stacking faults defect density [24] . By observing self-aligned bidirectional NW growth on GaAs (100) substrate and on GaAs (110) substrates, the growth directions of SLE NWs were hypothesized to be the projection of the <111>B grown vertical NWs on the surface of the substrate [25], and the assumption is illustrated in Figure 2.5.

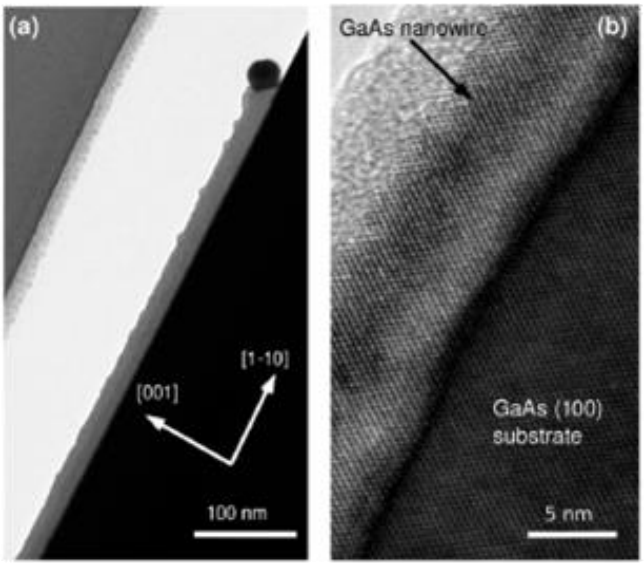

Figure 2.4: TEM images of SLE GaAs NW grown on GaAs (100) substrate. (a) Low-magnification TEM image of GaAs NW grown along [1-10] direction. Darker contrast of Au seed particle was depicted at the tip of NW. (b) HR-TEM image of SLE GaAs NW indicates that the NW is epitaxially attached on the GaAs (100) substrate without showing dislocations. Images were reproduced from Reference [24].

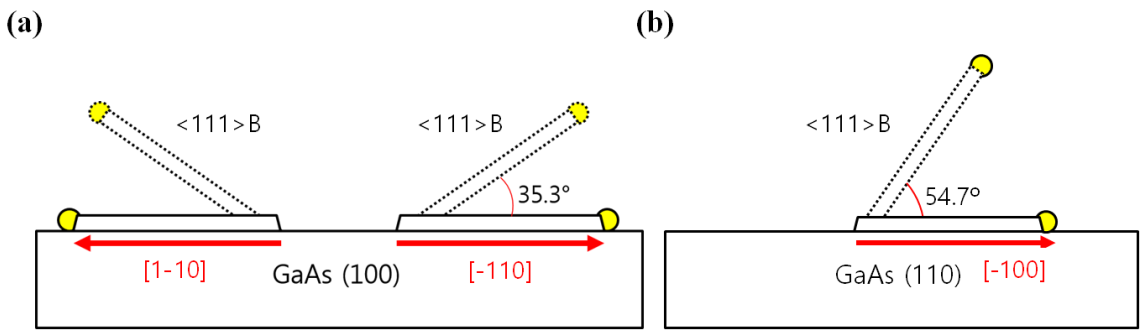

Figure 2.5: Illustration of the growth direction of SLE GaAs NWs on GaAs (100) and GaAs (110) substrates. (a) On the GaAs (100) substrate, planar NWs are grown bidirectional along the [1-10] and [-110] directions which are the vector projection of <111>B directions on the substrate. (b) On the GaAs (110) substrate, only one <111>B direction is available, so the planar NWs are grown unidirectional along surface projection of <111>B direction ([-100]).

2.2.2 SLE InAs NWs on InAs (100)

GaAs NWs have several limitations when utilizing them they in electric and photonic devices because of their inherent material characteristics, such as the existence of a relatively large number of surface-states density and mid-energy band gap Fermi-level pinning characteristic which hinders the realization of n-type Ohmic contacts [26]. InAs is one of the most desirable n-type channel materials which can substitute GaAs, because of its small effective mass, higher electron mobility [27] and its conduction band Fermi-level pinning ability with n-type metal contacts which offers advantages in realizing n-type Ohmic contacts [28].

Recently, our group found the growth conditions of SLE InAs NWs, and realized the growth of planar InAs NW on InAs (100) substrate. The growth of SLE InAs planar NWs was performed in the AIXTRON AIX 200/4 MOCVD reactor. The 50 nm diameter of Au colloids was randomly dispersed on the InAs (100) substrate after applying a poly-L-lysine (PLL) to give adhesion between metal particles and the wafer. The Au seeds-deposited samples were placed into the MOCVD chamber and the reactor temperature was ramped up to the NW growth

temperature (400-420 °C) under a constant AsH_3 flowing condition (3.71 x 10^{-3} mol/min). When the system reached the NW growth temperature, the AsH_3 molar flow rate was reduced to 3.13 x 10^{-4} mol/min and then trimethyl-Indium (TMIn) was introduced. Four different amounts of TMIn (50, 80, 110 and 170 sccm) were introduced to see the changes of NW morphology depending on the V/III molar ratios.

Figure 2.6 shows the scanning electron microscopy (SEM) images of InAs NWs grown under four different V/III ratios (39.1, 24.5, 17.8, and 11.5). At the lowest V/III ratio (Figure 2.6a), every NW is grown in-plane on the substrate along [-110] and [1-10] directions, and the growth trend is identical with previously researched SLE GaAs NWs on GaAs (100) substrates [29]. At the V/III ratio, NWs are grown with tapered structure due to prevalence of the vapor-solid-solid (VSS) growth on the side facets of the NW [30–32]. After increasing the V/III ratios to 17.8 and 24.5 (Figure 2.6b, Figure 2.6c), the VSS side-wall growth of NW disappears, while NWs start to grow along out-of-plane directions. When the V/III ratio is further increased to 39.1 (Figure 2.6d), planar NWs begin to grow again along the [-1-10] and [110] directions (<111>B projected directions), which are perpendicular to the GaAs SLE NWs on GaAs (100) and InAs NWs grown under lower V/III ratio. Particularly, at this V/III ratio, the NWs do not show any tapered side-wall morphology.

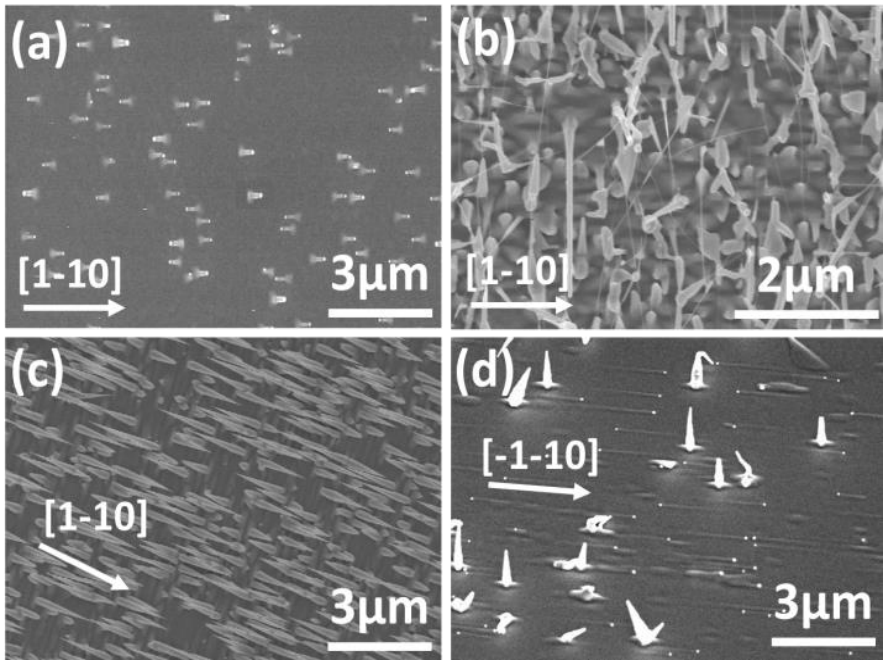

Figure 2.6: SEM images of InAs NWs grown on InAs (100) substrate under different V/III ratios. (a) At 11.5 of V/III ratio, 100% yield of tapered planar NWs are grown along [-110] and [1-10] directions. (b), (c) At higher V/III ratios (17.8, 24.5), NWs grow along out-of-plane directions. (d) When the V/III ratio reaches to 39.1, non-tapered planar NWs are synthesized along the [-1-10] and [110] directions.

2.2.3 Heterostructure SLE InAs NWs on GaAs (100)

To directly apply epitaxially grown InAs planar nanowires to electronic and photonic devices, the NWs have to be grown on semi-insulating substrates. However, a semi-insulating InAs wafers does not exist, so we need to grow planar InAs NWs on a lattice mismatched, foreign semi-insulating substrate such as GaAs, InP or Si. However, growing heteroepitaxy SLE NWs is challenging due to relatively large lattice mismatch that exists between InAs and semi-insulating foreign substrates [33]. Our group has been trying to grow SLE InAs NWs on foreign semi-insulating substrates, and recently, self-aligned SLE InAs NWs were successfully grown on semi-insulating GaAs (100) substrate beyond the presence of ~7% of lattice mismatch between two different materials.

To grow heterostructure planar SLE InAs NWs, Au seed particles (5 nm diameter) were randomly dispersed on the semi-insulating GaAs (100) substrate by evaporating Au colloid solution at 100 ºC. Au nanoparticles-distributed samples were loaded to the MOCVD chamber and heated at 625 °C for ten minutes under the presence of AsH_3 flow (50 sccm) to desorb the native oxide layer on the samples. After the annealing session, the chamber temperature was lowered to the growth temperature and TMIn was introduced under constant 7 sccm AsH_3 flow condition. To investigate the relationship between NW morphologies and NW growth conditions (growth temperature, V/III ratio), NWs growth temperatures and TMIn flow were engineered from 350 °C to 420 °C and 20 to 130 sccm (30 – 196 V/III molar ratios), respectively. The size of seed particles varies from 15 nm to 100 nm due to the random merging of neighboring Au colloids during the annealing process.

The yield, growth direction and morphology of InAs NWs are strongly dependent on the growth temperature and diameter of the NWs as shown in Figure 2.7. At 420 °C (Figure 2.7a), the InAs NWs cannot grow on the GaAs surface, but InAs parasitic thin film is grown on the entire surface of substrate regardless of the diameter of NWs. When the growth temperature is reduced to 380 °C (Figure 2.7b), planar NWs starts appear but most of NWs are wiggled without showing aligned growth directions, and lifted up from the substrate at the middle of growth. At the further decreased growth temperature (350 °C), self-aligned straight non-tapered planar InAs NWs, the diameters of which are smaller than 70 nm, grow along <111>B projected [-1-10] and [110] directions. The reason for the absence of in-plane NWs at higher temperatures can be assumed that the larger number of InAs parasitic islands – which are less observable at lower temperatures – on the surface hinder the growth of planar NWs. The size-dependent SLE NWs characteristic implies that critical limited width of SLE NW existed on the lattice mismatched

substrate like the existence of critical thin film growth thickness on lattice mismatched materials [34].

The growth rate study regarding the diameter of NW is illustrated at Figure 2.8. When the diameters of NW are 18 nm (Figure 2.8a) and 57 nm (Figure 2.8b), the corresponding length of NWs are 7.45 μm and 3.51 μm, respectively. Further investigation to find the relationship between the diameter of NW and the length of NW was performed, and it was verified that the length of the NWs increases with decreasing their diameter. Shown in Figure 2.9a are cross-sectional high-resolution transmission electron microscopy (HR-TEM) images of an SLE InAs NWs with 12 nm of thickness grown on a GaAs (100) substrate. The specific locations of GaAs substrate, InAs NW, Au seed and protective platinum (Pt) layer are separated by white dashes. Figure 2.9b shows an HR-TEM image obtained at the interface of the planar InAs NW and the underlying GaAs (100) substrate. The NW and substrate interface is depicted by the two dashed white arrows. The HR-TEM confirmed that the heteroepitaxially grown SLE planar NWs have high crystalline quality without any stacking faults. A high-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) is shown in Figure 2.9c while Figure 2.9d shows quantified elemental counts of In, Ga, As, Au, and Pt obtained through an energy-dispersive X-ray spectroscopy (EDXS) line-scan along the location of the black dotted line in Figure 2.9c. Coincident with the contrast variations in Figure 2.9c, the line-scan data in Figure 2.9d confirms the presence of an InAs NW at the region between markers A and B where A is the interface between GaAs substrate and InAs NW, and B is the interface between InAs NW and Au tip [35].

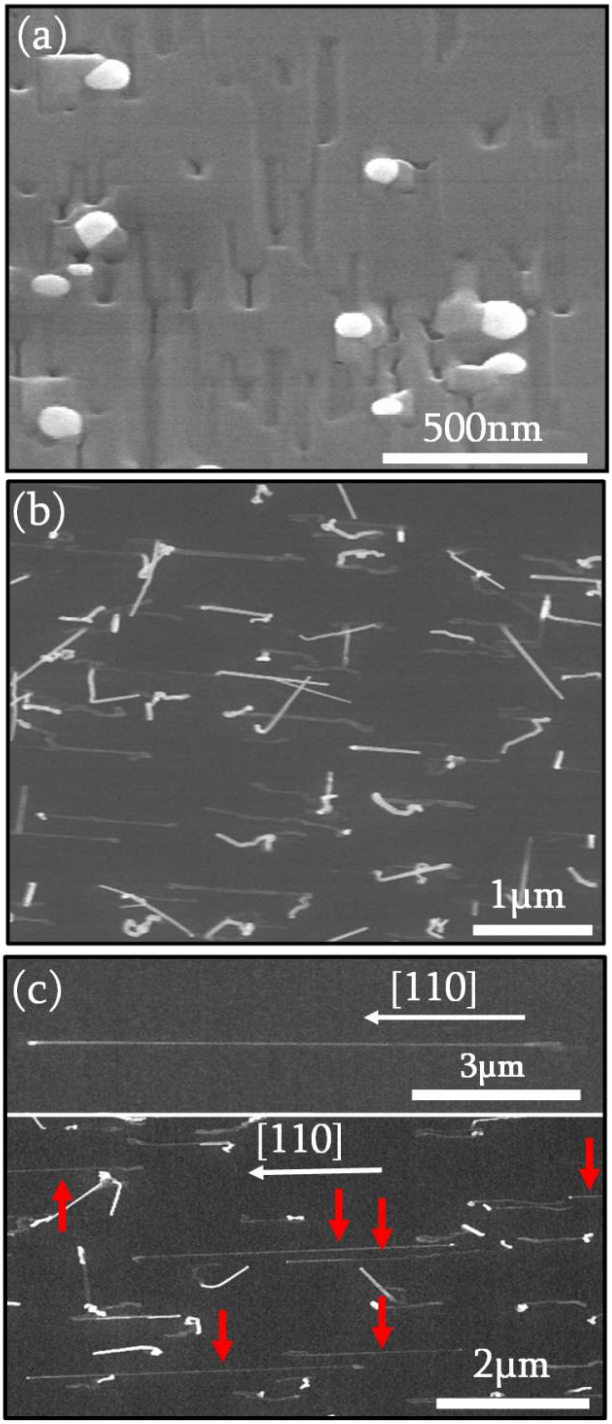

Figure 2.7: SEM images of heteroepitaxially grown SLE InAs NWs on semi-insulating GaAs (100) substrate. (a) Only parasitic thin film is grown all over the surface at 420 °C. (b) At 380 °C, partially planar NWs grow along random directions. (c) Planar NWs (indicated by red arrows) grow along [-1-10] and [110] directions. Inset shows magnified image of non-tapered planar SLE InAs NW.

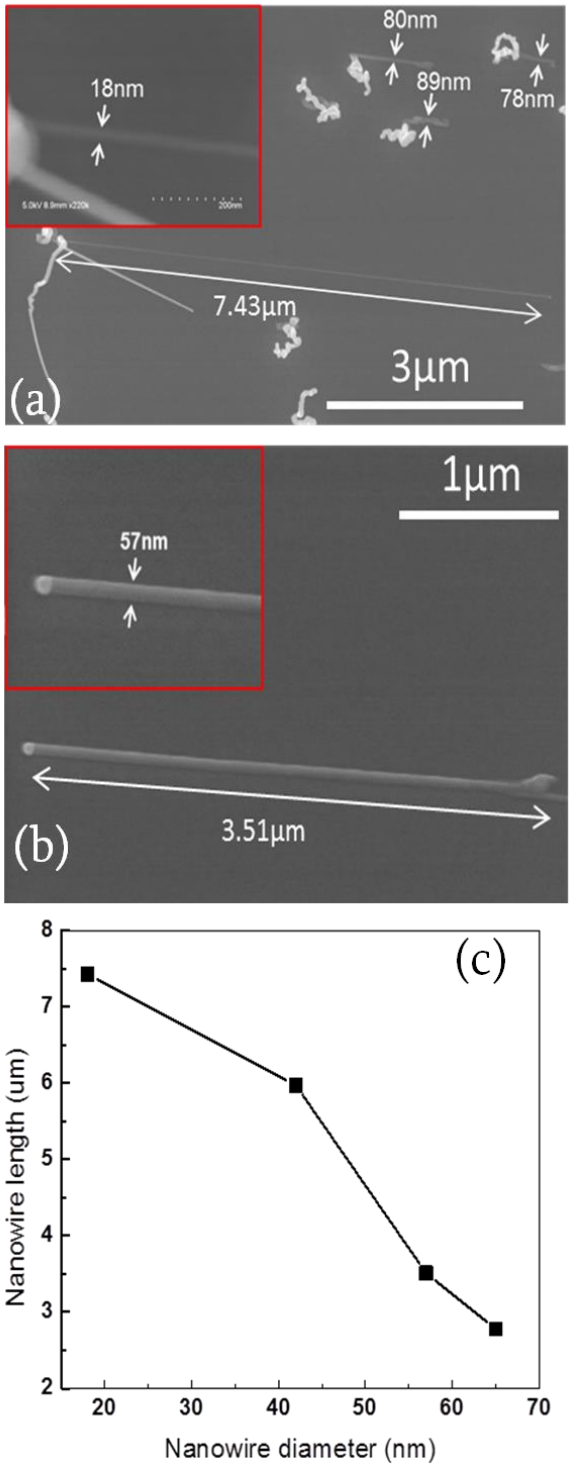

Figure 2.8: SEM images of planar InAs NWs with (a) 18 nm and (b) 57 nm diameter. The lengths of NW are measured to 7.43 µm (diameter of 18 nm) and 3.51 µm (diameter of 57 nm), respectively. (c) The plot of the NW diameter vs. NW length shows that the length of NW increases with decreasing diameter.

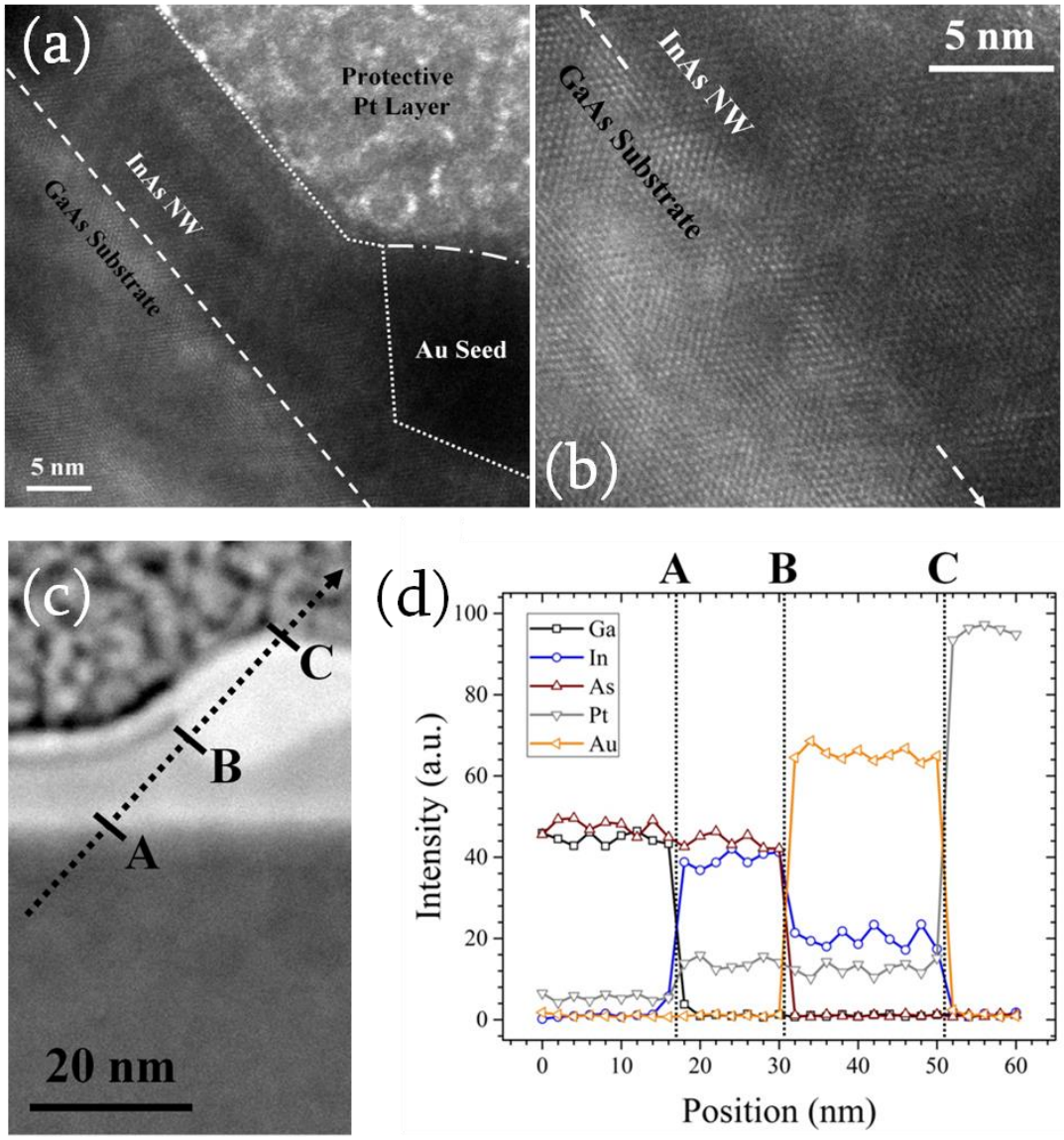

Figure 2.9: (a) HR-TEM image of SLE InAs planar NW. NW is epitaxially grown on GaAs (100) substrate. The Au seed is located at the tip of the NW. (b) High-magnified HR-TEM image at the interface between InAs NW and GaAs substrate. High crystal quality NW which is free from stacking faults is observed. (c) HAADF image of InAs NW. The black dot arrow indicates the EDXS line scan region at the GaAs substrate/InAs NW (A), InAs NW/Au seed (B), and the Au seed/Pt layer (C). (d) EDXS line-scan profile corresponding to the black arrow indicated at (c) confirms the existence of heteroepitaxially grown InAs NW. Reproduced from Reference [6].

CHAPTER 3 – DOPING OF NW

3.1 Doping of vertical NWs

Controlling the conductivity of NW is a critical issue for fabricating NW-based electrical or optical devices. Until now, variety of n- or p-type doped group IV NWs [36−38], III-V NWs [39, 40] and a related optical device [40] and electronic devices [41, 42] have been studied. To achieve n-type doped Si NWs, phosphine (PH_3) is introduced, while silane (SiH_4) or disilane (Si_2H_6) is supplied during the III-V NW growth process. For the p-type group IV and III-NWs, generally, diborane (B_2H_6) and diethylzinc (DEZn) are used respectively. However, most of generally researched doped NWs are grown vertically, so the NWs were not compatible with planar device fabrication steps.

In addition to the geometrical problem of conventional out-of-plane grown n-doped NWs, the incorporation tendency of dopant in the VLS NW growth system causes non-uniform doping distribution on the NWs. Figure 3.1a illustrates the two types of crystal growth (VLS and VS growth) which occur during the NW growth process [43]. Through the VLS mechanism, the precursors and doping sources are incorporated into the alloy droplets, and then dopants diffuse via liquid-solid interface to dope the NWs uniformly along their axial growth direction. Another doping pathway is through vapor-solid (VS) deposition: vapor phase dopants do not dissolve into the liquid alloy seed but are directly deposited on the side wall of NW, resulting in radial growth rather than axial growth of the doping profile on NW. This VS growth is undesirable because the side-wall deposition induces non-uniform doping distribution along the growth direction and degrades the device performances. Figure 3.1b, c shows the atom probe tomography (APT) results of phosphorus (P) – doped n-type Germanium (Ge) NW [43]. Figure 3.1b shows APT of

top-to-end cross-sectional distribution of dopant atoms while the side cut cross-sectional atomic distributions are illustrated at Figure 3.1c. The P and Ge atoms are depicted as gray dots and blue dots, respectively, and the APT results confirm that the VS deposition is prevalent during the NW growth process.

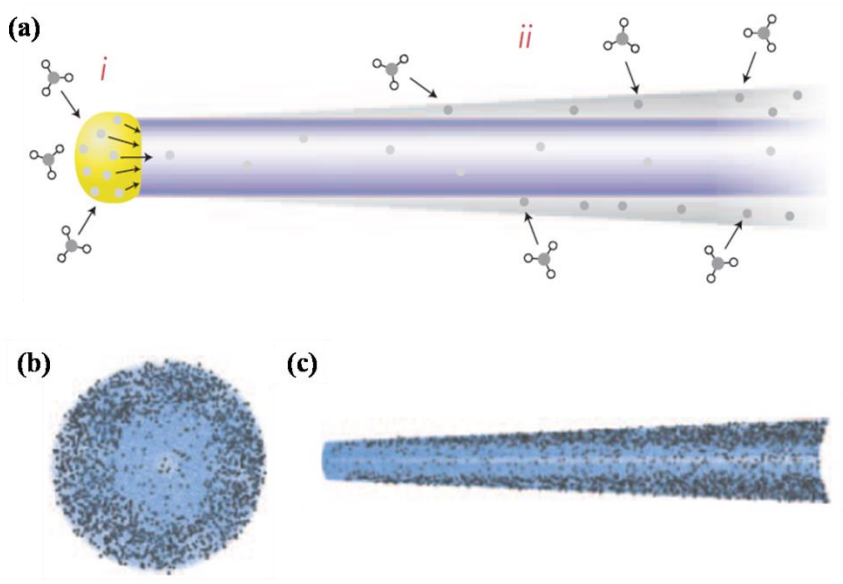

Figure 3.1: (a) Schematic of two kinds of dopant incorporation pathways. Through the VLS mechanism (i), dopants are dissolved into the liquid alloy and placed along the core of NW. (ii) Dopant directly deposited on the surface of NW by VS growth mechanism. (b) End-on view APT image of P doped Ge NW. P atoms (gray dots) are concentrated at the surface of NW due to the VS growth. (c) Side cross-section APT image of identical NW shown in Figure 3.1b. Significant VS radial growth doping profile is shown on tapered NW. Reproduced from Reference [14].

3.2 Doping of SLE grown planar GaAs NW

The one way to solve the geometrical limitation from using vertically grown doped NW is to grow doped SLE grown planar NWs, and Zn-doped SLE grown planar GaAs NW was

researched [44]. To grow Zn-doped planar GaAs NWs, 250-nm Au colloids were randomly scattered on the semi-insulating GaAs (100) substrate. The sample was loaded into the MOCVD chamber and TMGa and DEZn sources were introduced under the constant AsH3 flowing condition at 460 °C. Unlike previously studied un-doped GaAs planar NWs, at the Zn/Ga gas molar ratio of 5.9 x 10-4, the periodic corrugations are detected over the planar GaAs NW as shown in Figure 3.2a. After further increasing the Zn/Ga ratio, planar NWs start to grow in the out-of-plane direction without maintaining crystal structures. By inspecting a bright-field TEM image of Zn-doped NW (3.2b) and the selected-area electron diffraction pattern (3.2c), it is verified that the twinning planes which correspond to the corrugations exist along the [110] axis of NW. The conductivity of Zn-doped GaAs planar NW is tested by two-terminal electrical measurement (Figure 3.3) after depositing p-type contact metals on the NW, and the linear I-V curve confirms the electrical activity of p-type NW.

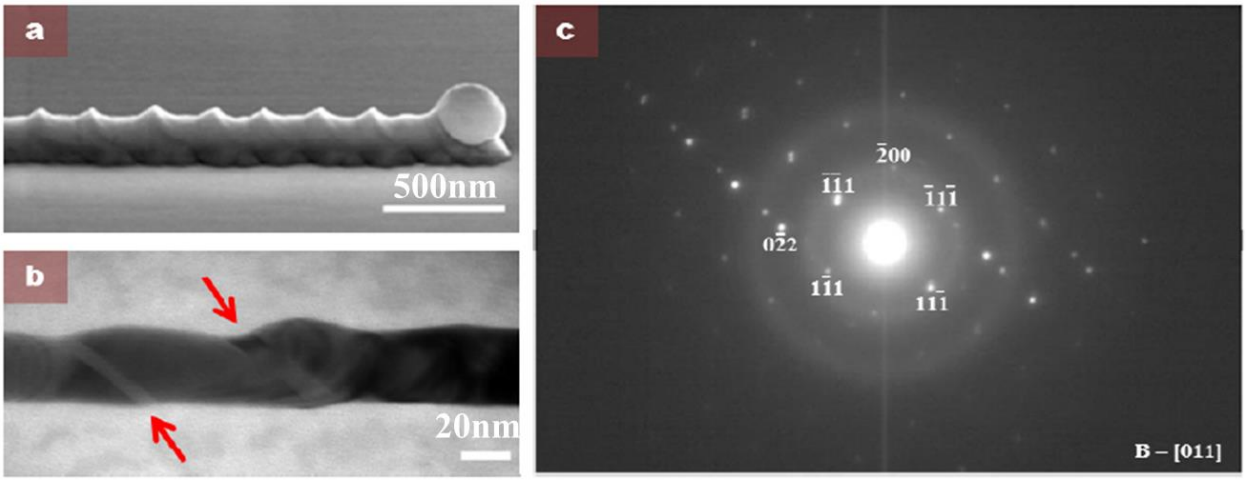

Figure 3.2: (a) Tilted-view SEM image of the same Zn-doped GaAs NW, highlighting the corrugated faceting structure. (b) TEM image of a p-type segment of a planar GaAs NW with red arrows pointing at the lateral twins. (c) Selected-area electron diffraction pattern indicates that the twin boundary exists along the [110] axis. Reproduced from Reference [44].

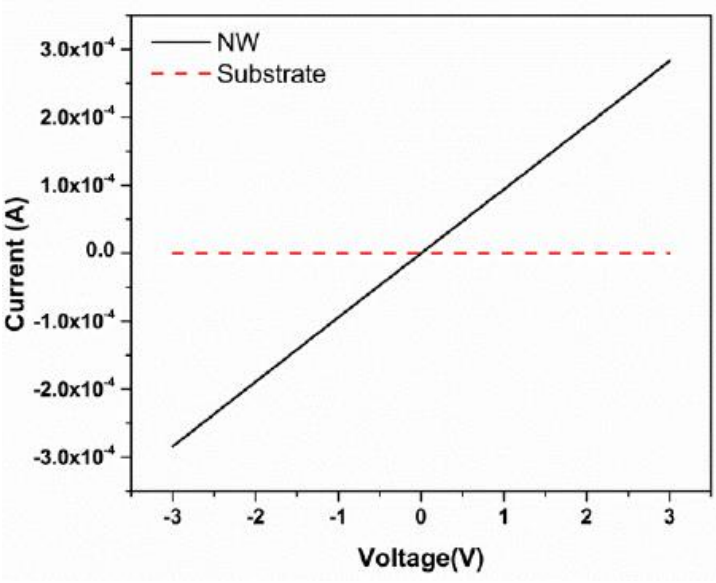

Figure 3.3: Two terminal I-V curves of Zn-doped planar NW. Linear Ohmic characteristic confirms that the NW can achieve conductivity from the *in-situ* doping process. Reproduced from Reference [44].

Multiple p-n junctions of GaAs NWs were also studied by using Si2H6 and DEZn as n-type and p-type doping sources, respectively. The general growth conditions of multi-junction planar GaAs NW, such as growth temperature, growth pressure and V/III gas molar flow ratio were identical to the previously studied Zn-doped NW process. To realize n-p-n-p-n-p lateral junctions, three different amounts of Si2H6 (8, 20 and 400 sccm) and DEZn (0.5, 1.0 and 1.6 sccm) were introduced by turns under a constant TMGa and AsH3 flowing condition. The Si/Ga molar flow ratios were 3.05 x 10^{-5}, 1.525 x 10^{-4} and 3.05 x 10^{-2}, while Zn/Ga ratios were 2.61 x 10^{-}3, 5.21 x 10^{-3} and 8.34 x 10^{-3}, respectively. Figure 3.4 shows plan-view SEM images of a multi p-n junction planar GaAs NWs with MOCVD precursor flow variations superimposed as red (TMGa, AsH3), green (Si2H6), and blue(DEZn) curves. Periodic corrugations are shown only at the Zn-doped (p-type) segments due to the formation of twin planes. In the same way as the Zn-doped

planar GaAs NW research, planar NW takes off at the middle of growth under a high Zn/Ga gas molar flow ratio (8.34×10^{-3}).

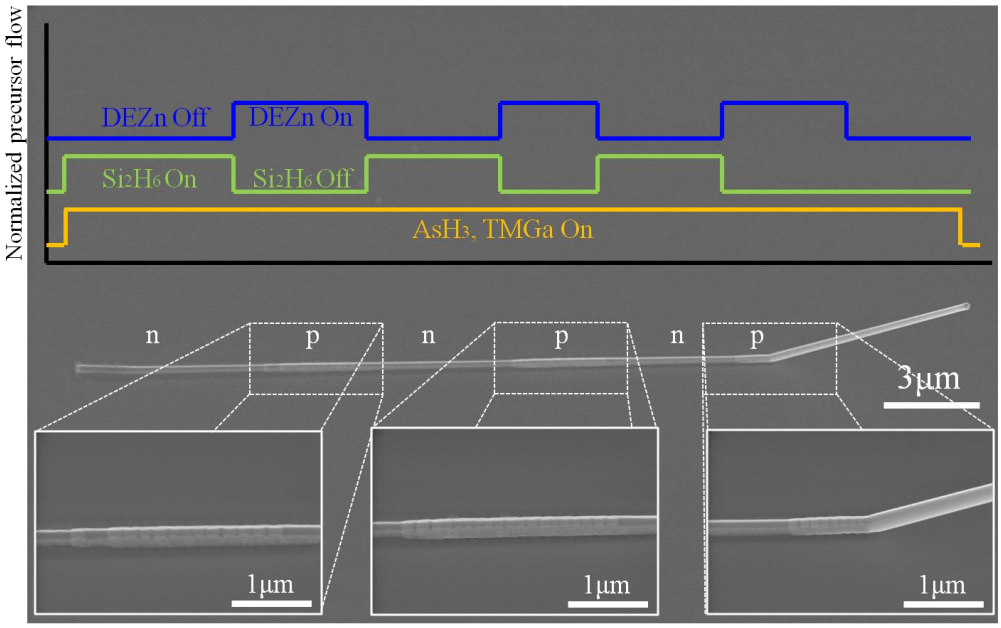

Figure 3.4: Tilted-view SEM image of n-p-n-p-n-p multi-junction GaAs NW grown on GaAs (100) substrate. Corresponding normalized precursor gas flow is plotted above the NW SEM image. Insets show the Zn-doped periodic corrugated p-type segments.

CHAPTER 4 – MONOLITHICALLY GROWN ARRAYS OF LATERAL P-N JUNCTION GAAS NW DIODES

4.1 Device fabrication

To overcome the limitations in using conventional vertical geometry p-n junctions and lateral p-n junction of vertically grown NWs (detailed in Chapter 1), for the first time, monolithically grown arrays of lateral p-n junction GaAs NW diodes was realized. Owing to the self-aligned growth characteristic of SLE GaAs NW, the positon of NW can be easily engineered by controlling the location of Au seed nanoparticles [24]. To grow an array of p-n junction GaAs NWs, an array of Au nanoparticles was deposited on the semi-insulating GaAs (100) substrate by electron-beam lithography (EBL) patterning. Au was deposited on the EBL dot patterns using an electron-beam evaporation system. The diameter of NW can be controlled by engineering the diameter of the EBL circular pattern and height of Au thin film which determines the volume of Au pillar, because, during the annealing session of NW growth step, the pillar becomes a sphere and its diameter determines the diameter of VLS grown NW.

The entire device fabrication steps are illustrated at Figure 4.1. In the study, 65 nm thickness of Au metal deposited on 400 nm diameter EBL patterned circular opening to grow ~250 nm diameter of NWs. The Au EBL patterned sample was loaded into the AIXTRON AIX 200/4 MOCVD reactor and the chamber was heated to 625 °C, stayed at that temperature for 10 min under a 50 sccm of AsH_3 (2.23×10^{-3} mol/min) flowing condition to desorb a native oxide layer on the substrate. After finishing the annealing session, the reactor temperature dropped to NW growth temperature (460 °C) and the AsH_3 flow was reduced to 15 sccm (6.71×10^{-4} mol/min). To grow an n-type segment of GaAs NW, 10 sccm of TMGa (1.17×10^{-4} mol/min) and 400 sccm

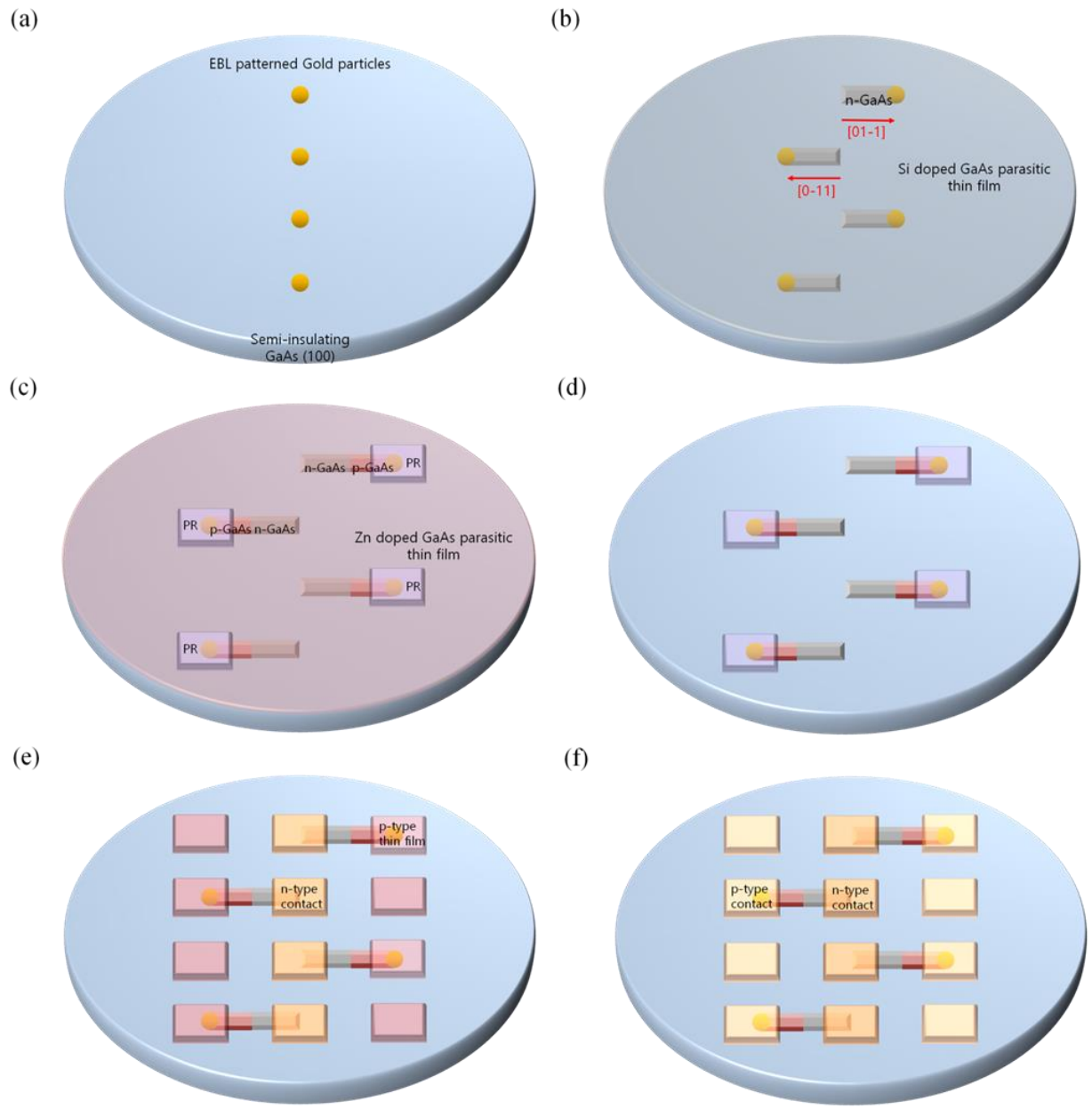

Figure 4.1: Array of lateral p-n junction GaAs NW diodes fabrications. (a) Deposit Au on EBL patterned semi-insulating GaAs (100). (b) Si-doped n-type segment of NW was grown. (c) Zn-doped p-type portion of GaAs NW was grown. P-type regions of NW were covered by PR patterns. (d) Parasitic thin film was etched by $H_2SO_4 : H_2O_2 : H_2O$ (1 : 8: 340) solution. (e) PR pads on p-type region were removed, and n-type contacts (Ge/Au/Ni/Au) were deposited. (f) After annealing n-type contacts, p-type contacts (Ti/Au) were evaporated.

of Si_2H_6 (3.57 x 10^{-6} mol/min) sources were simultaneously introduced for 17 s. After finishing the growth of n-type NW, Si_2H_6 was abruptly switched off and 1.6 sccm of DEZn (9.78 x 10^{-7} mol/min) immediately introduced for 17 s under the constant AsH_3, TMGa flowing circumstance to grow a p-type segment of NW. The corresponding Si/Ga and Zn/Ga molar flow ratios were 3.05 x 10^{-2} and 8.34 x 10^{-3}, respectively. To remove possibly grown parasitic thin film on the substrate, the grown sample was etched with a 1:8:340 (H_2SO_4:H_2O_2:H_2O) solution for 8 s. Before removing the parasitic thin film, p-type NW regions were protected by AZ5214 photo-resist (PR) patterns in order to achieve better Ohmic contact by preserving a highly Zn-doped region from the wet etching process. The PR patterns which cover p-type regions were removed by acetone washing, and then 20 x 20 μm^2 patterns were opened on the n-type contact regions by an optical lithography process. Next, 1 minute oxygen (O_2) plasma treatment and 30 s of 1:1 (HCl:H_2O) solution wet etching were performed to remove the PR residue and native oxide layer on the opened areas. A stack of n-type metal contacts (Ge/Au/Ni/Au) were deposited by electron beam evaporator, and the metal stacks were alloyed by 15 s of annealing step at 400 °C. The third optical lithography was performed to open p-type contact regions, and then the stack of p-type metal (Ti/Au) contacts were evaporated on the opened area to complete the device fabrication.

4.2 Results and discussion

4.2.1 Two terminal I-V characteristic of p-n diodes

Figure 4.2a shows the SEM image of the array of lateral p-n junction SLE grown GaAs planar NW diodes. Individual diodes are highlighted by the white dashed boxes. The locations of NW were well controlled by the EBL process, and p-n GaAs NWs were grown along the same

direction in the particular region. The high-magnified SEM image of a single p-n diode is illustrated in Figure 4.2b. Then 20 x 20 μm^2 of n-type and p-type metal contacts were deposited at a distance of ~4.8 μm. Two terminal I-V characteristics of diodes were measured by a Keithley 4200 semiconductor parameter analyzer, and the results are shown in Figure 4.3. The diode voltage (V_D) was sweeped from -2 V to 2 V to measure the diode current (I_D). The diode was turned on 1.2 V of forward bias, and the 10^6 of relatively high rectification ratio was detected (Figure 4.3a). The semi-log I-V plot measured at ± 2 V of V_D range is shown in Figure 4.3b. By measuring the slope of the I-V curve at the forward biased linear region, a relatively high ideality factor (2.18) was extracted due to the large number of surface states which generate an amount of recombination current [45]. The high ideality factor of GaAs NW diodes can be improved by applying surface passivation on the NWs to reduce surface states [45].

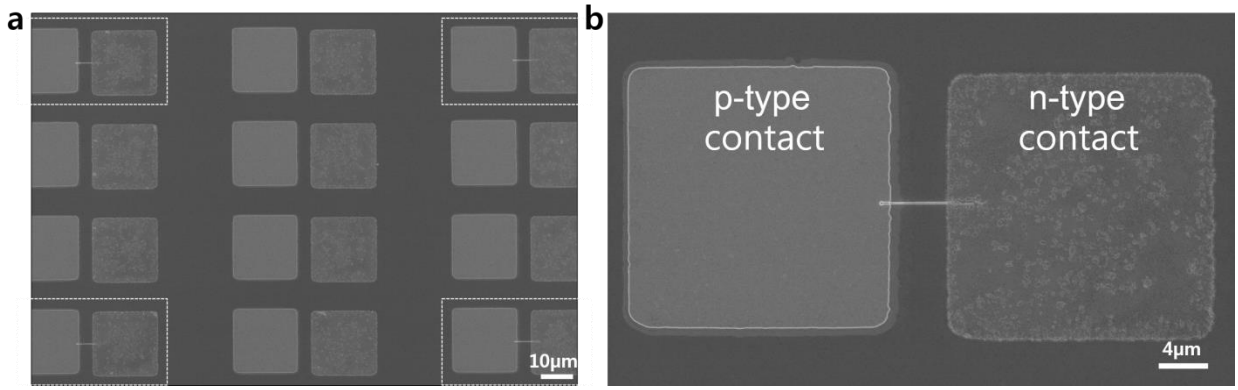

Figure 4.2: (a) SEM image of SLE grown single p-n junction planar GaAs NW diode arrays. Single diodes are marked in the white boxes. (b) High-magnified single p-n diode.

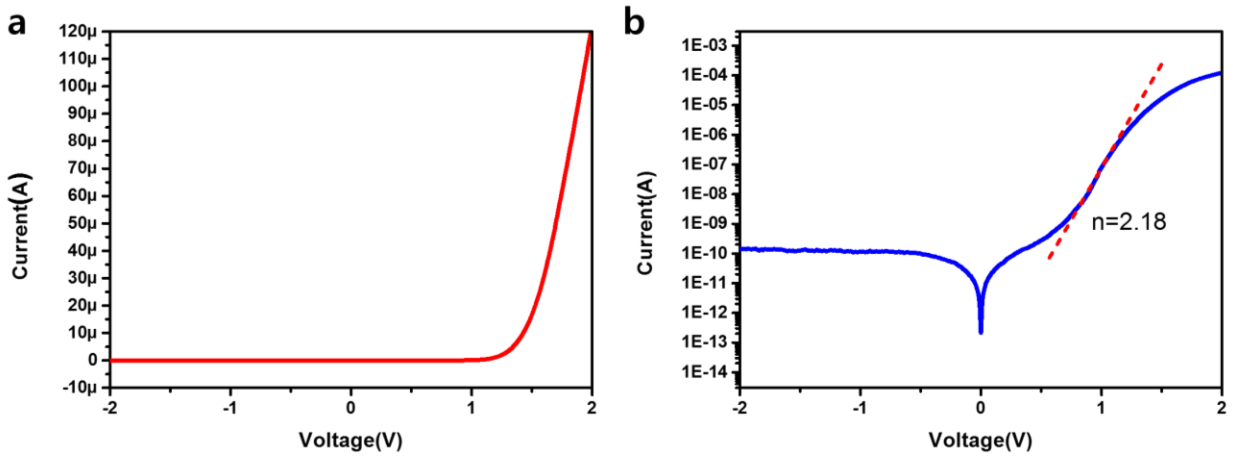

Figure 4.3: (a) Two terminal I-V characteristic of a p-n diode. I_D was measured from -2 V to 2 V, and the diode turned on at 1.2 V. (b) Semi-log I-V curve of the diode. Ideality factor of 2.18 was extracted by measuring the linear slope of the I-V curve at ~ 1 V.

4.2.2 I-V characteristics depend on the doping concentration

Table 4.1: Doping conditions of three different p-n GaAs NW diodes

	Si_2H_6	DEZn
Device 1	40 sccm (Si/Ga=3.05 x 10^{-3})	1.6 sccm (Zn/Ga=8.34 x 10^{-3})
Device 2	400 sccm (Si/Ga=3.05 x 10^{-2})	1.6 sccm (Zn/Ga=8.34 x 10^{-3})
Device 3	400 sccm (Si/Ga=3.05 x 10^{-2})	1.0 sccm (Zn/Ga=5.21 x 10^{-3})

To see the doping concentration modulation capability of monolithically grown lateral p-n junction planar GaAs, I-V characteristics of three differently doped (Table 4.1) diodes were comparatively studied (Figure 4.4). When the n-type dopant gas flow rate was reduced from 400 sccm (Device 2) to 40 sccm (Device 1) while keeping the DEZn flow at 1.6 sccm constantly, the forward current magnitude at 2 V was reduced by 17 times (85 μA to 15 μA). However, the

diode did not show any rectifying performance after reducing the Zn/Ga molar flow ratio from 8.34×10^{-3} (Device 2) to 5.21×10^{-3} (Device 3).

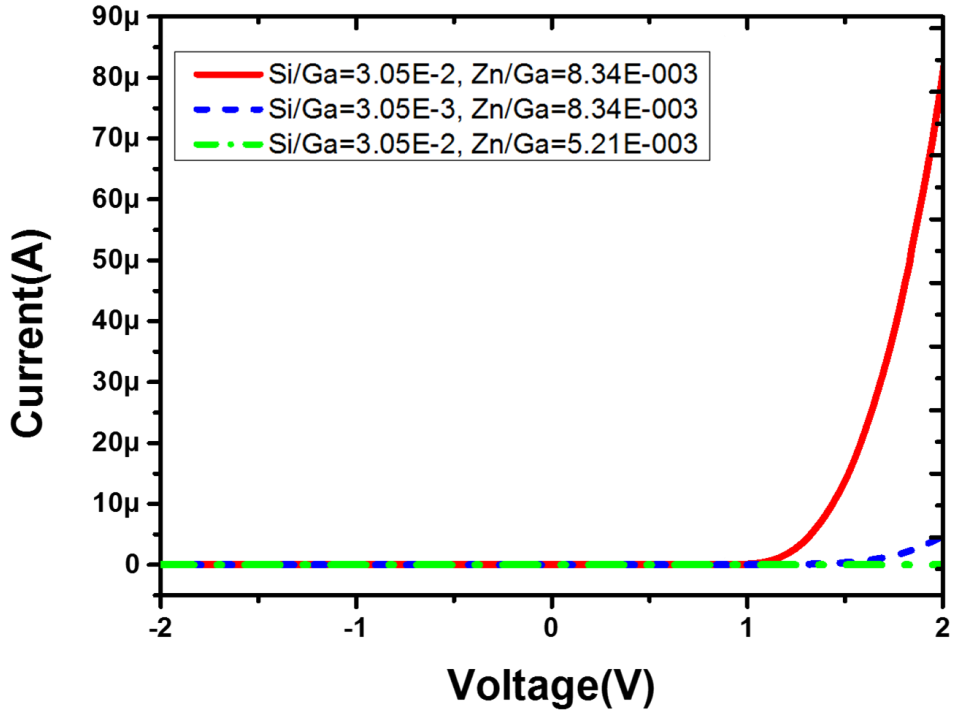

Figure 4.4: Two terminal I-V characteristics of p-n GaAs NW diodes under different doping conditions. By reducing the Si/Ga ratio from 3.05×10^{-2} (red line) to 3.05×10^{-3} (blue dashed line), the forward I_D was also reduced at the same value of V_D. When the Zn/Ga was reduced from 8.34×10^{-3} (red line) to 5.21×10^{-3}, the diode was not turned on until V_D of 2 V.

4.2.3 I-V characteristics depend on the number of NWs between contacts

The linearity regarding the number of NWs is a critical requirement to utilize NW-based electric and optical devices. Linearity of I-V characteristics depends on the number of GaAs nanowires

between two terminal contacts is shown in Figure 4.5. The magnitude of I_D at forward bias linearly increases by increasing the number of NWs. This indicates that the parasitic thin film on the substrate was successfully removed by acid solution etching process, so the diode behavior is realized only through NWs.

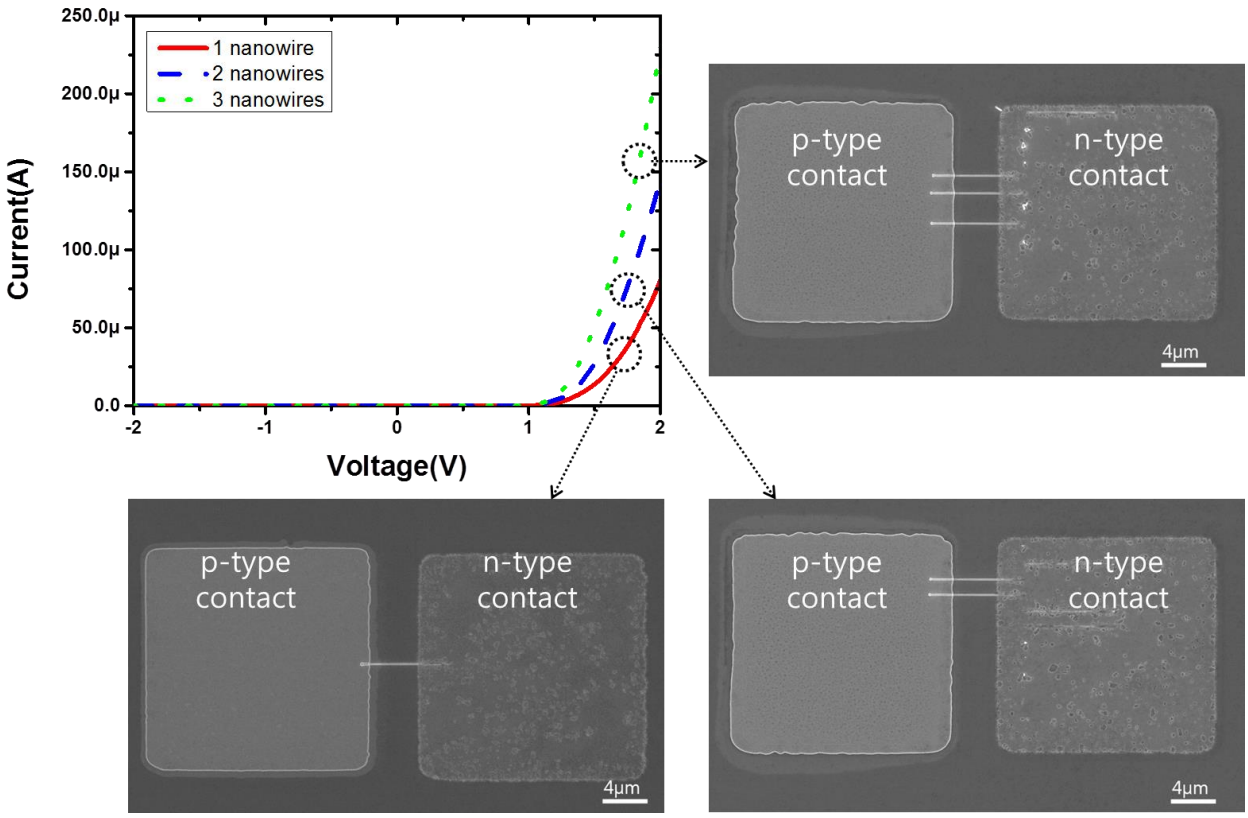

Figure 4.5: I-V characteristics of SLE-grown p-n junction GaAs NWs depend on the number of NWs connected between two metal contacts. The forward-biased current scales with the number of contacted NWs, as seen for 1 (red), 2 (blue dash), and 3 (green dash) NWs. Correlated SEM images of single p-n diodes are indicated.

CHAPTER 5 – FUTURE WORK

5.1 SLE grown planar III-V NW based tunnel field-effect transistors (TFETs)

TFET is one of the most promising novel field-effect transistor FETs which can overcome the limitations in scaling down the conventional transistors' subthreshold swing (SS) and can provide improved short channel effect (SCE) as well as high I_{ON}/I_{OFF} ratio by using a band-to-band-tunneling (BTBT) mechanism [46]. Among the device structures of TFET, NW-based TFET is desirable due to its capability of realizing multi-gate geometry and heterostructure band-line up interface which increase the tunneling possibility and tunneling current [47, 48], and recently, the simulation [49] as well as the experimental research [50] of vertical NW TFETs were introduced.

The monolithically p-n doped SLE planar GaAs NWs growth technique can be directly applied to the fabrication of planar NW TFETs, and we are proposing 2D fabrication-platform array-based NW tri-gate TFET as a future research area. The suggested array-based SLE grown planar GaAs NW TFET fabrication steps are showing in Figure 5.1. First, the array of Au seed particles will be deposited on the semi-insulating GaAs (100) substrate through EBL patterning. After loading the sample into the MOCVD chamber the lateral p+-i-n+ junction NW will be grown. During the growth of the NW, AsH_3, TMGa and Si_2H_6 will be introduced simultaneously to grow an n-type segment of NW. After finishing growth of the n-type NW, Si_2H_6 is abruptly switched off to grow the intrinsic part of the NW. Finally, DEZn will be supplied for growing a p-type segment of NW. After the growth of p-i-n GaAs NW, the parasitic thin film on the sample will be removed by the digital etching process (HCL wet etching process after 1 min of O_2 plasma treatment). Next, a high-k dielectric atomic layer deposition (ALD) will be performed on

the entire substrate, and the three individual lithography and metal deposition processes will be performed to form source, drain and gate metal contacts.

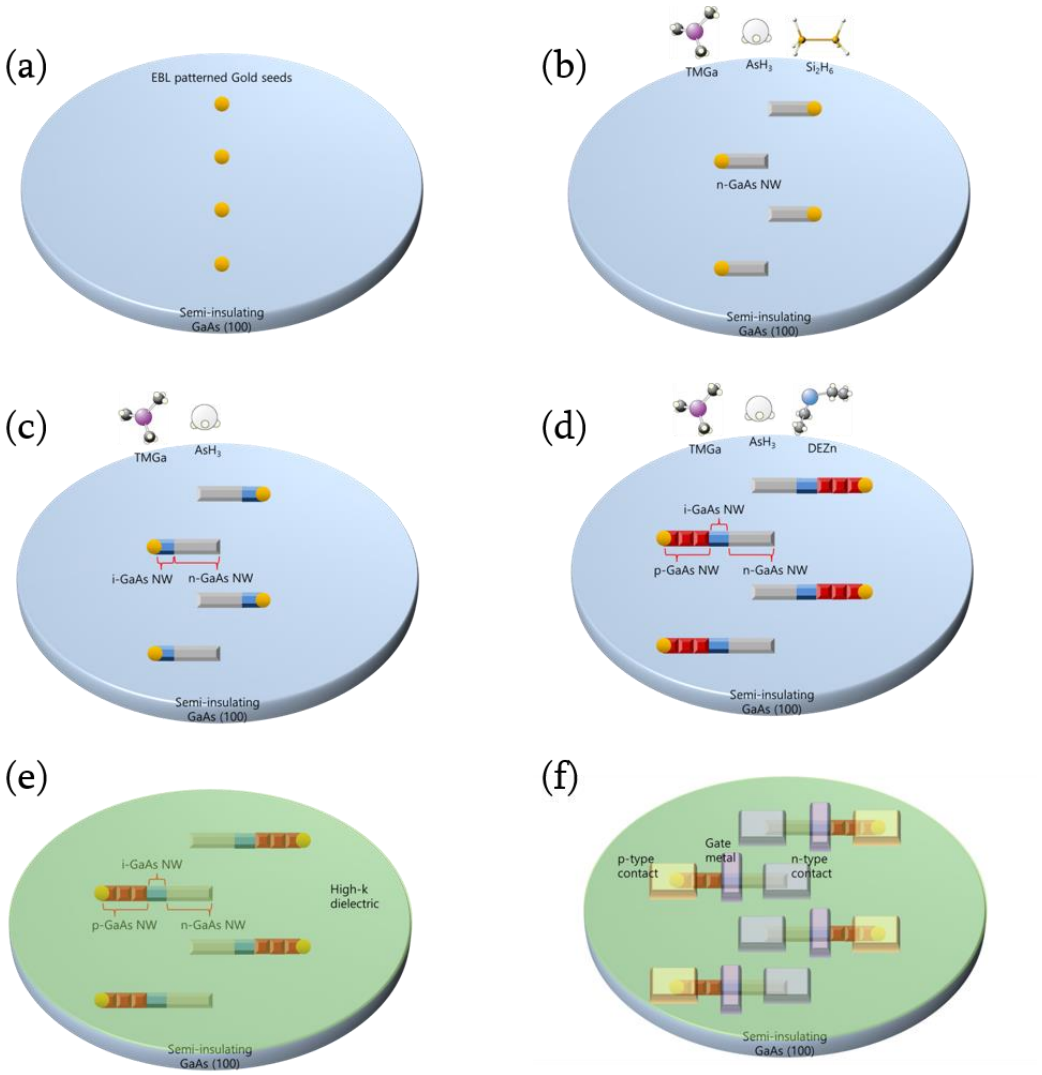

Figure 5.1: Fabrication steps of a suggested array of planar GaAs NW TFET. (a) Array of Au dots is deposited on the GaAs (100) substrate by EBL patterning. (b) Si_2H_6 will be supplied to grow an n-type segment of NW. (c) AsH_3 and TMGa are introduced without flowing any dopant sources to grow intrinsic GaAs NW. (d) After growing intrinsic NW, DEZn will be introduced to grow p-type segment of NW. (e) High-k dielectric is deposited on the surface using ALD. (f) Source, drain and gate metal contacts will be deposited.

The expected band diagrams of TFET in each gate biasing conditions are shown in Figure 5.2. In the 0 V gate biasing condition (Figure 5.2a), an electrical channel cannot be formed due to the energy barriers formed between n-type/intrinsic and p-type/intrinsic interfaces. Under the positive gate biasing condition (Figure 5.2b), electrons can tunnel from the p+ segment of NW to the intrinsic channel. With negative gate voltage bias (Figure 5.2c), carriers in the n+ region can tunnel into the intrinsic channel region.

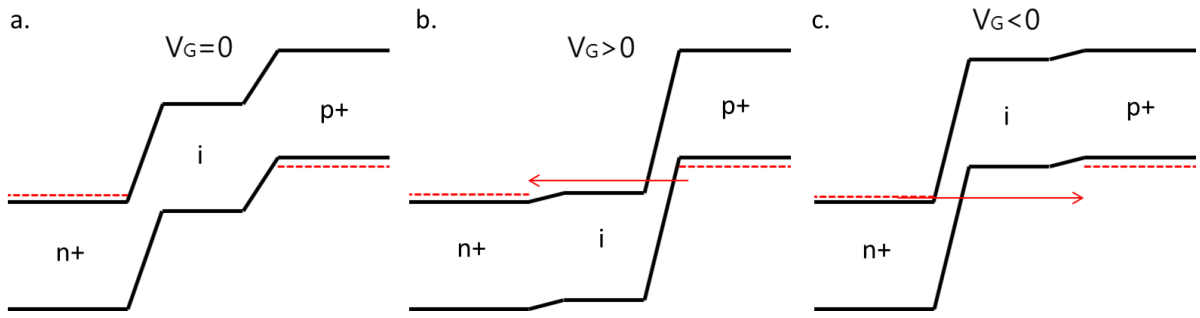

Figure 5.2: Band diagram of planar NW TFET under three different gate bias conditions. (a) At the 0 V gate bias condition, carriers located at the n+ or p+ regions cannot tunnel into the intrinsic channel region. (b) Under the positive gate bias, carriers at the p+ region can tunnel into the empty states in the n+ region. (c) At the negative gate bias condition, carriers located at the n+ region can tunnel into the p+ region.

REFERENCES

[1] P. O. Vaccaro, A. Vorobev, N. Dharmarasu, T. Fleischmann, J. M. Zanardi Ocampo, S. Saravanan*, et al.*, "Lateral p–n junctions for high-density LED arrays," *Microelectronics Journal,* vol. 34, pp. 355-357, 2003.

[2] J. R. Gell, P. Atkinson, S. P. Bremner, F. Sfigakis, M. Kataoka, D. Anderson*, et al.*, "Surface-acoustic-wave-driven luminescence from a lateral p-n junction," *Applied Physics Letters,* vol. 89, p. 243505, 2006.

[3] C. L. Foden, V. I. Talyanskii, G. J. Milburn, M. L. Leadbeater, and M. Pepper, "High-frequency acousto-electric single-photon source," *Physical Review A,* vol. 62, p. 011803, 2000.

[4] B. Kaestner, J. Wunderlich, J. Sinova, and T. Jungwirth, "Co-planar spin-polarized light-emitting diodes," *Applied Physics Letters,* vol. 88, p. 091106, 2006.

[5] M. Cecchini, V. Piazza, F. Beltram, M. Lazzarino, M. B. Ward, A. J. Shields*, et al.*, "High-performance planar light-emitting diodes," *Applied Physics Letters,* vol. 82, pp. 636-638, 2003.

[6] G. De Simoni, L. Mahler, V. Piazza, A. Tredicucci, C. A. Nicoll, H. E. Beere*, et al.*, "Lasing in planar semiconductor diodes," *Applied Physics Letters,* vol. 99, p. 261110, 2011.

[7] C. A. King, M. R. Frei, M. Mastrapasqua, K. K. Ng, Y. O. Kim, R. W. Johnson*, et al.*, "Very low cost graded SiGe base bipolar transistors for a high performance modular BiCMOS process," in *Electron Devices Meeting, 1999. IEDM '99. Technical Digest. International*, 1999, pp. 565-568.

[8] P. O. Vaccaro and K. Fujita, "Optoelectronic devices based on lateral p-n junctions fabricated by molecular-beam epitaxy growth of silicon-doped GaAs on patterned (311)A-oriented substrates," *Quantum Electronics, IEEE Journal of,* vol. 36, pp. 849-857, 2000.

[9] T. Hosey, V. Talyanskii, S. Vijendran, G. A. C. Jones, M. B. Ward, D. C. Unitt*, et al.*, "Lateral n–p junction for acoustoelectric nanocircuits," *Applied Physics Letters,* vol. 85, pp. 491-493, 2004.

[10] M. Borgström, J. Wallentin, J. Trägårdh, P. Ramvall, M. Ek, L. R. Wallenberg*, et al.*, "In situ etching for total control over axial and radial nanowire growth," *Nano Research,* vol. 3, pp. 264-270, 2010.

[11] I. Regolin, C. Gutsche, A. Lysov, K. Blekker, Z.-A. Li, M. Spasova*, et al.*, "Axial pn-

junctions formed by MOVPE using DEZn and TESn in vapor–liquid–solid grown GaAs nanowires," *Journal of Crystal Growth,* vol. 315, pp. 143-147, 2011.

[12] A. Pevzner, Y. Engel, R. Elnathan, T. Ducobni, M. Ben-Ishai, K. Reddy*, et al.*, "Knocking down highly-ordered large-scale nanowire arrays," *Nano Letters,* vol. 10, pp. 1202-1208, 2010.

[13] S. Raychaudhuri, S. A. Dayeh, D. Wang, and E. T. Yu, "Precise semiconductor nanowire placement through dielectrophoresis," *Nano Letters,* vol. 9, pp. 2260-2266, 2009.

[14] A. R. Tao, J. Huang, and P. Yang, "Langmuir−Blodgettry of nanocrystals and nanowires," *Accounts of Chemical Research,* vol. 41, pp. 1662-1673, 2008.

[15] J. Appenzeller, J. Knoch, M. T. Bjork, H. Riel, H. Schmid, and W. Riess, "Toward nanowire electronics," *Electron Devices, IEEE Transactions on,* vol. 55, pp. 2827-2845, 2008.

[16] P. J. Pauzauskie and P. Yang, "Nanowire photonics," *Materials Today,* vol. 9, pp. 36-45, 2006.

[17] Y. Li, F. Qian, J. Xiang, and C. M. Lieber, "Nanowire electronic and optoelectronic devices," *Materials Today,* vol. 9, pp. 18-27, 2006.

[18] H. J. Joyce, Q. Gao, H. Hoe Tan, C. Jagadish, Y. Kim, J. Zou*, et al.*, "III–V semiconductor nanowires for optoelectronic device applications," *Progress in Quantum Electronics,* vol. 35, pp. 23-75, 2011.

[19] R. S. Wagner and W. C. Ellis, "Vapor-liquid-solid mechanism of single crystal growth," *Applied Physics Letters,* vol. 4, pp. 89-90, 1964.

[20] A. F. Seth and L. Xiuling, "Metal-catalyzed semiconductor nanowires: A review on the control of growth directions," *Semiconductor Science and Technology,* vol. 25, p. 024005, 2010.

[21] K. A. Dick, K. Deppert, T. Mårtensson, B. Mandl, L. Samuelson, and W. Seifert, "Failure of the vapor−liquid−solid mechanism in Au-assisted MOVPE growth of InAs nanowires," *Nano Letters,* vol. 5, pp. 761-764, 2005.

[22] V. A. Nebol'sin and A. A. Shchetinin, "Role of surface energy in the vapor–liquid–solid growth of silicon," *Inorganic Materials,* vol. 39, pp. 899-903, 2003.

[23] W. Braun, V. M. Kaganer, A. Trampert, H.-P. Schönherr, Q. Gong, R. Nötzel*, et al.*, "Diffusion and incorporation: Shape evolution during overgrowth on structured substrates," *Journal of Crystal Growth,* vol. 227–228, pp. 51-55, 2001.

[24] S. A. Fortuna, J. Wen, I. S. Chun, and X. Li, "Planar GaAs nanowires on GaAs (100)

substrates: Self-aligned, nearly twin-defect free, and transfer-printable," *Nano Letters,* vol. 8, pp. 4421-4427, 2008.

[25] S. D. Ryan, A. W. Donald, and L. Xiuling, "Relationship between planar GaAs nanowire growth direction and substrate orientation," *Nanotechnology,* vol. 24, p. 035304, 2013.

[26] M. D. Pashley, K. W. Haberern, R. M. Feenstra, and P. D. Kirchner, "Different Fermi-level pinning behavior on n- and p-type GaAs(001)," *Physical Review B,* vol. 48, pp. 4612-4615, 1993.

[27] S. M. Sze, *Physics of Semiconductor Devices* (2nd ed.) Wiley Interscience, 1981.

[28] C. A. Mead and W. G. Spitzer, "Fermi level position at metal-semiconductor interfaces," *Physical Review,* vol. 134, pp. A713-A716, 1964.

[29] S. A. Fortuna and L. Xiuling, "GaAs MESFET with a high-mobility self-assembled planar nanowire channel," *Electron Device Letters, IEEE,* vol. 30, pp. 593-595, 2009.

[30] M. Kolíbal, R. Kalousek, T. Vystavěl, L. Novák, and T. Šikola, "Controlled faceting in 〈110〉 germanium nanowire growth by switching between vapor-liquid-solid and vapor-solid-solid growth," *Applied Physics Letters,* vol. 100, p. 203102, 2012.

[31] S. Heun, B. Radha, D. Ercolani, G. U. Kulkarni, F. Rossi, V. Grillo*, et al.*, "Coexistence of vapor–liquid–solid and vapor–solid–solid growth modes in Pd-assisted InAs nanowires," *Small,* vol. 6, pp. 1935-1941, 2010.

[32] H. Cui, Y. Y. Lü, G. W. Yang, Y. M. Chen, and C. X. Wang, "Step-flow kinetics model for the vapor–solid–solid Si nanowires growth," *Nano Letters,* vol. 15, pp. 3640-3645, 2015.

[33] J. Narayan and B. C. Larson, "Domain epitaxy: A unified paradigm for thin film growth," *Journal of Applied Physics,* vol. 93, pp. 278-285, 2003.

[34] K. Jagannadham and J. Narayan, "Critical thickness during two-dimensional and three-dimensional epitaxial growth in semiconductor heterostructures," *Materials Science and Engineering: B,* vol. 8, pp. 107-124, 1991.

[35] C. Zhang, X. Miao, P. K. Mohseni, W. Choi, and X. Li, "Site-controlled VLS growth of planar nanowires: Yield and mechanism," *Nano Letters,* vol. 14, pp. 6836-6841, 2014.

[36] Y. Cui, X. Duan, J. Hu, and C. M. Lieber, "Doping and electrical transport in silicon nanowires," *The Journal of Physical Chemistry B,* vol. 104, pp. 5213-5216, 2000.

[37] Y. Wang, K.-K. Lew, T.-T. Ho, L. Pan, S. W. Novak, E. C. Dickey*, et al.*, "Use of phosphine as an n-type dopant source for vapor−liquid−solid growth of silicon nanowires," *Nano Letters,* vol. 5, pp. 2139-2143, 2005.

[38] C. Celle, C. Mouchet, E. Rouvière, J.-P. Simonato, D. Mariolle, N. Chevalier*, et al.*, "Controlled in situ n-doping of silicon nanowires during VLS growth and their characterization by scanning spreading resistance microscopy," *The Journal of Physical Chemistry C,* vol. 114, pp. 760-765, 2010.

[39] M. Hilse, M. Ramsteiner, S. Breuer, L. Geelhaar, and H. Riechert, "Incorporation of the dopants Si and Be into GaAs nanowires," *Applied Physics Letters,* vol. 96, p. 193104, 2010.

[40] K. Tomioka, J. Motohisa, S. Hara, K. Hiruma, and T. Fukui, "GaAs/AlGaAs core multishell nanowire-based light-emitting diodes on Si," *Nano Letters,* vol. 10, pp. 1639-1644, 2010.

[41] G. Zheng, W. Lu, S. Jin, and C. M. Lieber, "Synthesis and fabrication of high-performance n-type silicon nanowire transistors," *Advanced Materials,* vol. 16, pp. 1890-1893, 2004.

[42] M. T. Björk, J. Knoch, H. Schmid, H. Riel, and W. Riess, "Silicon nanowire tunneling field-effect transistors," *Applied Physics Letters,* vol. 92, p. 193504, 2008.

[43] D. E. Perea, E. R. Hemesath, E. J. Schwalbach, J. L. Lensch-Falk, P. W. Voorhees, and L. J. Lauhon, "Direct measurement of dopant distribution in an individual vapour-liquid-solid nanowire," *Nat Nano,* vol. 4, pp. 315-319, 2009.

[44] R. S. Dowdy, C. Zhang, P. K. Mohseni, S. A. Fortuna, J.-G. Wen, J. J. Coleman*, et al.*, "Perturbation of Au-assisted planar GaAs nanowire growth by p-type dopant impurities," *Optical Materials Express,* vol. 3, pp. 1687-1697, 2013.

[45] C. Zhang and X. Li, "Planar GaAs nanowire tri-gate MOSFETs by vapor–liquid–solid growth," *Solid-State Electronics,* vol. 93, pp. 40-42, 2014.

[46] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature,* vol. 479, pp. 329-337, 2011.

[47] A. L. Vallett, S. Minassian, P. Kaszuba, S. Datta, J. M. Redwing, and T. S. Mayer, "Fabrication and characterization of axially doped silicon nanowire tunnel field-effect transistors," *Nano Letters,* vol. 10, pp. 4813-4818, 2010.

[48] J. Knoch, "Optimizing tunnel FET performance-impact of device structure, transistor dimensions and choice of material," in *VLSI Technology, Systems, and Applications, 2009. VLSI-TSA'09. International Symposium on*, 2009, pp. 45-46.

[49] J. Knoch and J. Appenzeller, "Modeling of high-performance p-type III–V heterojunction tunnel FETs," *Electron Device Letters, IEEE,* vol. 31, pp. 305-307, 2010.

[50] K. Moselund, H. Schmid, C. Bessire, M. Björk, H. Ghoneim, and H. Riel, "InAs–Si

nanowire heterojunction tunnel FETs," *Electron Device Letters, IEEE,* vol. 33, pp. 1453-1455, 2012.