GATE CURRENT MODELING OF TUNNELING REAL-SPACE TRANSFER TRANSISTOR WITH NEGATIVE DIFFERENTIAL RESISTANCE

BY

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THESIS

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ABSTRACT

In this project, the modeling of gate current is introduced to obtain a negative differential resistance (NDR) on a dual-channel tunneling real-space transfer transistor (TRSTT). The device was fabricated on a GaAs (100) substrate with a GaAs/InGaAs/GaAs straddling heterostructure. According to the experimental data reported by Yu et al. in 2010 [1], they demonstrate an InGaAs and δ-doped GaAs dual-channel TRSTT device with an λ-type NDR in a low drain-source voltage (V_{DS}), which reaches a peak-to-valley current ratio of 3.3. Meanwhile, the gate-source current sharply increases at the same applied V_{DS}. The thesis aims to build current models to reproduce these I-V characteristics, and to investigate the mechanism of current-controllable NDR effects. The drain-source I-V relation without leakage has been first derived and simulated to fit the experimental data and set down constants for later modeling processes. Then an analytic model of the gate current I_G is introduced. The simulated results obtained a sharp drop similar to experimental data. The gate current model involves intermediate modeling processes such as tunnel probability (θ_y), velocity of charges (υ_y) approach to quantum well (QW), charge distribution function ($f(E)$), and potential difference along the channel ($V(x)$). These models are discussed in a progressive path step by step, which includes numerical derivation and simulations. The current flow direction will be analyzed as a core point. The complementary drain-source I-V characteristic relation is produced by considering the gate current derived before and generating a family of curves in a λ-shaped NDR in the same V_{DS} region with a sharp drop of I_G. All the simulations are done by mathematical iterating in Matlab with the Illinois Taub Cluster as simulator source. The simulated results will be compared with experimental data to verify the high reliability of the model. In the last section of the project, the limitation of the uncomplementary derivation of $V(x)$ after device saturation will be discussed, accompanied by suggestions for future improvements.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my adviser, Prof. Jean-Pierre Leburton, for his inspirational guidance over the past three years. I thank him for introducing me to the topic as well as for his support along the way. Furthermore, I am indebted to the Illinois Campus Cluster Program for providing the Taub Cluster simulation resource.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

As the miniaturization of complementary metal-oxide-semiconductor technology continues beyond 20nm, it becomes more and more difficult to make transistors smaller and pack more into unit area, without increasing the power consumption and cost, to maintain speed. New computer technologies require the chip to work more efficiently and enable more functions per unit space and time, pushing the semiconductor industry towards groundbreaking revolution. Many proposals have been carried out with novel fabrication technologies, new materials or superior structure, etc. Among them, the inventions of the gate controllable negative differential resistance (NDR) resonant tunneling diodes and real space transfer (RST) transistors have attracted much research interest in making next-generation devices, especially high frequency oscillators and high speed memories [2].

The mechanism of the NDR through RST in heterojunctions was first proposed by Hess in 1979 [3]. Later the mechanism was developed and adopted in new devices. The conventional NDR effect was based on the thermionic emission of charge carrier transfer from the high-mobility quantum well (channel) region to the low mobility barrier region. On the other hand, the AlGaAs/InGaAs/GaAs pseudomorphic modulated doped tunneling real-space transfer transistor (TRSTT), which was proposed by Bigelow and Leburton in 1990 [4], was considered the first to integrate gate voltage controlled NDR effects. It was believed that the TRSTT endowed with NDR characteristics would make it available as a terahertz oscillator source [5] with a fast switching speed and a lower subthreshold swing. This application was considered incredibly useful in high frequency circuits, such as weighted sum threshold logic circuits [6], static frequency dividers or flexible logic circuits

[7]. Hence, many experiments have been done in the past few decades on the performance of typical devices, such as negative resistance field-effect transistors [8], charge injection transistors [9] and tunneling field-effect transistors [6], etc. Apparently, theoretical research on I-V characteristic modeling is needed to help investigate and further develop the mechanisms of gate current controlled NDR effects.

1.2 Previous Research

Gate current controlled NDR effects became evident in a wide range of experiments with different device structures [8-12]. Group III-V materials were used to make heterostructures, which let electron charges flow from high mobility area to lower and cause an NDR phenomenon. Through analyzing those research results, much information about the NDR effects in dual channel devices can be gathered. This section briefly reviews, chronologically, examples that are relevant to this thesis.

"Enhanced resonant tunneling real-space transfer in δ-doped GaAs/InGaAs gated dual-channel transistors grown by MOCVD" (1996) [10]

A δ-doped GaAs/InGaAs gated dual-channel transistor (DCT) was studied to observe a pronounced N-shaped NDR and negative transconductance by tunneling real-space transfer. A family of I_{DS} versus V_{DS} curves were made by changing the sheet density of the δ-doped channel layer and the thickness of the barrier layer. The authors found that decreased sheet charge density and barrier thickness led to an increased current flow along the gate direction, which resulted in an increase of peak-to-valley current ratio (PVR) at NDR. The study announced the achievement of higher PVR values than any other proposed TRST devices.

The basic concept of DCT device study to observe NDR by taking the TRST was also used in this thesis project. And the PVR values are discussed in the NDR region as well. The tunneling occurred from the δ-doped channel to the metal gate, which increased the gate current and caused the NDR. However, in our modeling process, the gate current varies mainly by gate bias and applied V_{DS} with fixed $4 \times 10^{12}/\text{cm}^2$ sheet charge density in the δ-doped channel and 30nm barrier layer.

"Enhancement-mode $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ as tunneling real space

transfer high electron mobility transistor" (2004) [11]

The device made in this case was a single channel, high electron mobility transistor (HEMT) fabricated with $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$. It operated at a low gate bias of 0V to 0.5V. Since the electric field increased between the channel and gate layer with increasing applied gate bias, the electrons in the channel became "hot". Tunneling happened because of the continued increase of the e-field, which made electrons accumulate enough energy to overcome the barrier layer (QW). Hence the increasing leakage from the gate decreased I_{DS}, which led to a pronounced N-shape of the NDR phenomenon.

This HEMT device study is similar to the experimental device study presented in this thesis. The main difference is that the HEMT they used was a single channel device in which hot electrons tunneled directly to the gate, instead of a dual channel device in which charges tunnel from high mobility channel to lower and finally reach the gate. The idea behind [11] was adopted to help simplify the TRSTT device structure and make it easier to analyze.

"Fabrication and dc current−voltage characteristics of real space transfer transistor with dual-quantum-well channel" (2008) [12]

The device studied in this case is similar to the device presented in this thesis project. Both devices have a GaAs/InGaAs/GaAs dual-channel heterojunction structure and the NDR effects happen with a real space transfer. And both devices exhibit increased gate current due to the "hot" electrons tunneling through the cap layer and reaching the gate with a NDR.

However, [12] focused on discussing the advantages of using the gate to control NDR effects, with an eye towards replacing the combination of resonant tunneling diodes and high electron mobility transistors in NDR circuits. The thesis project gathered ideas about applications of NDR effects in different circuits, but put more effort into using analytical models to understand the mechanism of gate controllable NDR effects.

1.3 Research Project Outline

The research aims to investigate the analytic models of gate current controlled NDR effects in a GaAS/InGaAs/GaAs heterostructure dual-channel TRSTT device. Experimental data used was provided by [1] and [13] through

fabricating the real device followed by bench tests. Simulations are carried out according to the built up device circuit to fit the experimental data, in order to reproduce the NDR phenomenon and verify the reliability of the research.

The models are divided mainly into two parts: drain-source I-V characteristic I_{DS} models and gate current I_G models. The modeling process begins with a simple MOSFET structure, then derives an I_{DS} versus V_{DS} model without considering the leakage, followed by the gate current modeling. There are four intermediate steps involved. The tunnel probability θ_y is the first to be introduced. Its derivation starts from the simple time-independent Schrödinger equation [14] and then applies Wentzel-Kramers-Brillouin approximation (WKB) [15] to get a general solution. Then the solution is simplified by analyzing the band moving under gate bias with a single triangular QW. After getting θ_y, the velocity of charges approach to quantum well (υ_y) and charge distribution function $f(E)$ is investigated. $V(x)$ is derived by a method similar to that used previously to derive V_{DS}. Then the project focuses on explaining the mechanism of gate current direction change after reaching V_{NDR}, which is considered the main cause of NDR. The simulation data of I_G are then used to carry out the I_{DS} including tunneling effects. A λ-shaped NDR exists right at the region of sharply drooped I_G, indicating that the NDR effects of the particular TRSTT are controllable by gate current. All calculations and simulations were done in Matlab, and results fit well with the experimental data provided, except for the limitation of $V(x)$, which is discussed in Chapter 6 along with ideas for future improvement.

CHAPTER 2

TRSTT DEVICE STRUCTURE

2.1 Simple Structure and Band Diagram

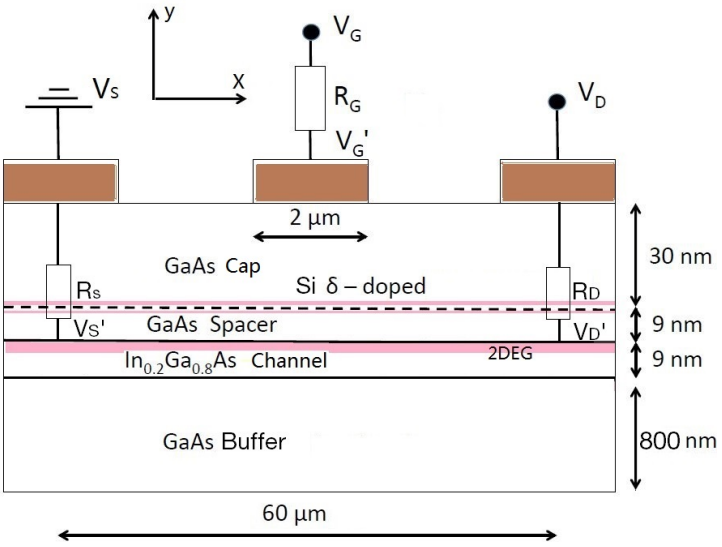

Figure 2.1: Cross-section view of device structure along x-y plane.

The device structure is retrieved from that in Refs. [1], [13], and the cross−section view is shown in Fig. 2.1. It is a GaAs/InGaAs/GaAs dual-channel heterostructure device [10], which consists of a 0.8-m intrinsic GaAs buffer layer at the bottom with a 90Å undoped $In_{0.2}Ga_{0.8}As$ channel layer on the top. Then a 90Å undoped GaAs spacer layer was placed, followed by a silicon δ-doped thin layer with a $4 * 10^{12}$ cm^{-2} sheet density. Finally, a 300Å undoped GaAs formed the cap layer. The channel length is 2μm, and the width is 60μm. A layer of 2-dimensional electron gas (2DEG) [16] was created between the channel layer and spacer layer by the InGaAs/GaAs straddling heterostructure [17]. The 2DEG and δ-doped layers, colored in

pink, will form two channels when the device is turned on. The electron mobility in the 2DEG channel was measured to be 5604 cm^2/Vs by Hall test [18], and the sheet density of carrier in InGaAs channel was $9.02 * 10^{11}$ cm^{-2}. The device source and body were connected to ground. However, since the electron mobility along the δ-doped channel was thousands of times smaller than that in the 2DEG channel, we neglected the current contribution made by the charges flow in the δ-doped channel. This made the device structure much simpler to analyze. The resistance of R_G was known as 10kΩ. And the other two resistors R_S and R_D were both set to 180Ω, though they were not included in the real experimental test. The reason for having them is to simplify device structure and help derive the analytical model. This will be explained in detail when we introduce the device band diagram.

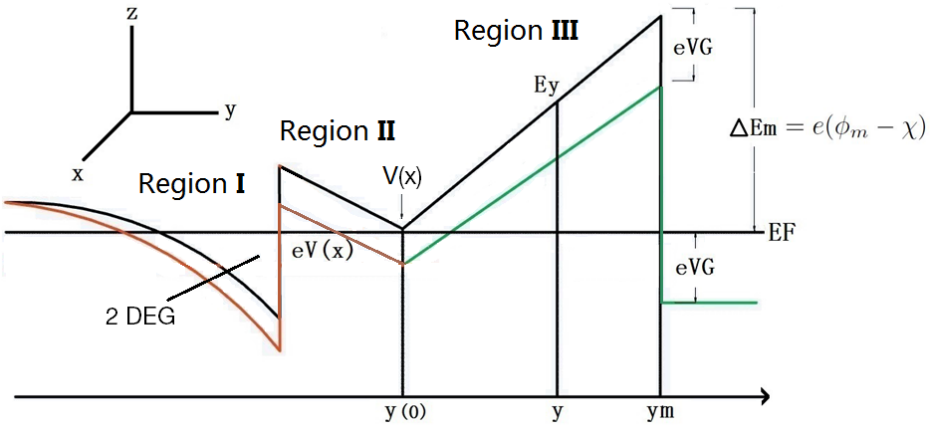

Figure 2.2: Band diagram in cross section view along vertical direction (y-z plane) from gate to substrate along the channel.

The band diagram in Fig. 2.2 shows the cross section in the y-z plane of the device. Region I represents the 2DEG channel, Region II is the δ-doped channel and Region III is the metal gate side. The purpose of the band diagram is to illustrate how the band movement is controlled by gate bias under different drain-source voltage supplies, as well as the charges tunneling through the barriers all the way from Region I to Region III or in reverse. The black lines show the device at equilibrium with the line $E_F = 0$ as the reference. The green line shows a forward gate bias applied on the device. The whole barrier between Regions II and III moves downward by an order of magnitude of eV_G without changing the barrier height ΔE_m, where $\Delta E_m = 0.95eV$ [1], ϕ_m is metal gate work function, and χ is vacuum work

function. The variable $V(x)$ represents the potential difference from the position x to source along the channel direction. The brown lines show that the barrier between Regions II and I moves downward by assuming the $V(x)$ increases along the x-axis (channel direction). The distance from $y(0)$ to y_m is 30nm, which is the GaAs cap layer, and below $y(0)$ to Region I is the 9nm InGaAs channel layer.

2.2 Experimental Test Results

The DC I-V characteristics were measured in a Keithley 4200 characterization system at room temperature [1]. The TRSTT device was fabricated by conventional MOSFET processes consisting of photolithography, wet etching and liftoff techniques. AuGeNi and Au were sputtered as source and drain electrodes on the GaAs substrate, and sintered at 375°C for 25s for the ohmic contacts. Then Au was evaporated on the GaAs cap layer as a Schottky gate in the middle of the source and drain. The partial experimental results are presented in Fig. 2.3 [1].

From the data curve of drain-source current I_{DS}, a λ-shaped NDR is observed via a family of curves made by different gate biases from 0V to 0.8V. When the drain-source voltage approaches a value V_{NDR}, the I_{DS} dramatically drops. Meanwhile the gate current I_{GS} increases sharply at the same point where I_{DS} drops, indicating that the NDR was formed because of the sudden change of the gate current. However, the previous researcher made a mistake here: after reaching the V_{NDR}, the gate current should drop sharply instead of quickly increase. From Fig. 2.1, every increase of I_{GS} will result in a larger gate bias $V_{G'}$, which will open the channel further; therefore, a more open channel should have a bigger current flow, which conflicts with the data result in Fig. 2.3 in which I_{DS} drops to form an NDR. Therefore, the answer is that I_{GS} should reduce to get negative (opposite direction) after approaching V_{NDR}. Detailed reasoning and current model will be presented in the next chapter.

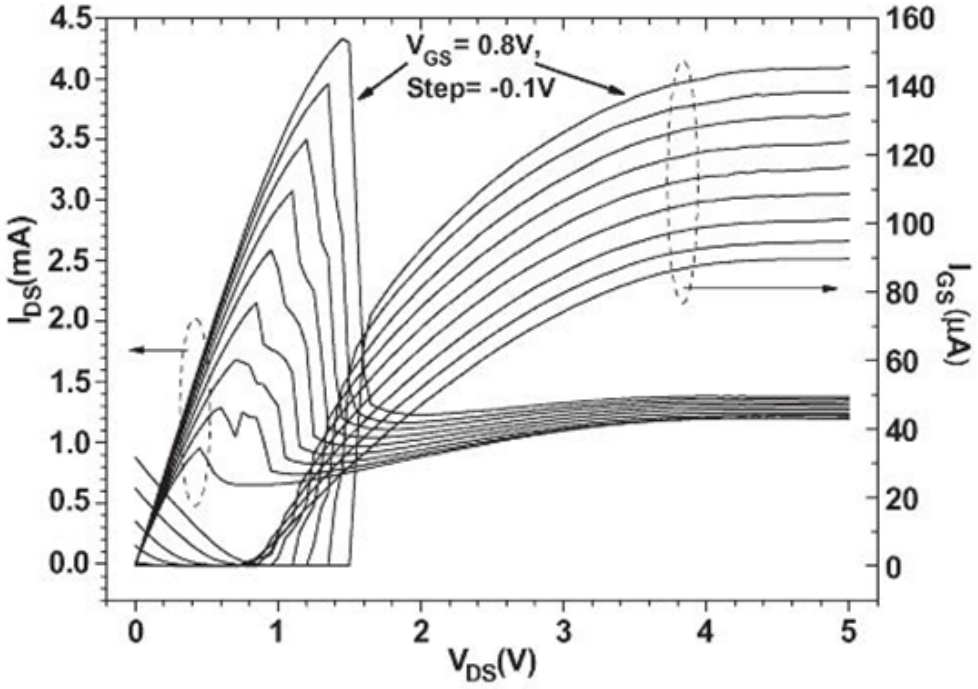

Figure 2.3: Experimental result. Drain-source current (left axis) and gate current (right axis) versus drain-source voltage with step gate voltage characteristics of TRSTT at room temperature. Gate voltage change from 0V to 0.8V with a 0.1 V step.

CHAPTER 3

ANALYTIC MODEL OF GATE CURRENT

3.1 I-V Characteristic without Tunneling

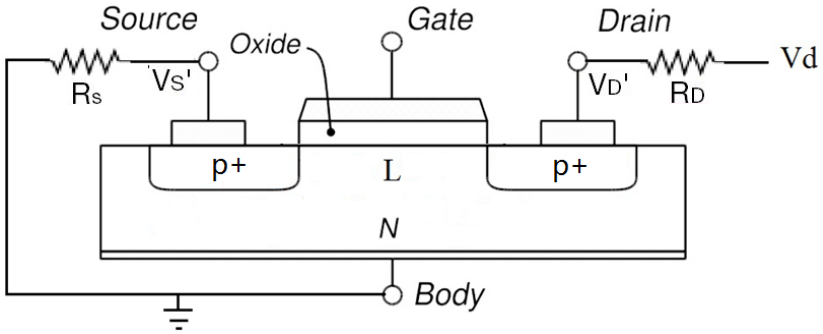

Figure 3.1: Simple MOSFET circuit model, with two resistors connected in series at drain and source side.

The gate current derivation is the core of this thesis, since it will directly control the current flow in the channel from source to drain. The gate current can be treated as a leakage by which the electron charges tunnel through the barrier from the 2DEG all the way to the metal gate. But before we address the gate current, there are still some constants that are very important in derivation but are unknown from the experimental result; these include, for example, $R_{S/D}$ and electric field strength. So we need to finalize those constants through deriving the I-V relations and simulate the characteristics of a simple 2-D MOSFET circuit structure without gate tunneling to fit the experimental data in [1], [13]. The circuit consists of two resistors attached in series at drain and source side. The general circuit was already shown in Fig. 2.1, but in order to make it clear and easy to read, another simplified circuit diagram is given in Fig. 3.1. The device is under gate control in different drain biases with source and body grounded. Kirchhoff's current law (KCL) solves the circuit with the I-V relations defined in Eq. 1(a,b) and Eq. 2. As

we mentioned before, the reason for connecting two identical series resistors along source and drain is because this helped to make the band diagram easier to analyze. The electron charges go from source and drain into the 2DEG channel; they have to pass through the GaAs cap and spacer layers. Since the two layers will not change under the drain and source regions, we recognize the loss of the charges along the path to be two identical resistors connected in series under drain and source.

$$V_{S'} = (I_{DS} - I_{GS}) * R_S \approx I_{DS} * R_S \tag{1.a}$$

$$V_{D'} = V_D - I_{DS}R_D \tag{1.b}$$

$$V_{G'} = V_G - I_{GS}R_G \tag{2}$$

From the experimental data in Fig. 2.3, the gate current I_{GS} was about 1/30 of the I_{DS}. Especially before the drain-source voltage reached the V_{NDR}, the difference was even larger. So $I_{DS} - I_{GS} \approx I_{DS}$ in Eq. 1.a was established. On the other hand, since the gate current direction flow from the metal gate to the semiconductor was considered as positive, the potential at $V_{G'}$ is larger than V_G shown in Eq. 2.

Now we substitute the assumptions above into the integration of the simple drain-source current equation. Considering the hot electron mobility degradation [11] of the mobility along the channel, we get the general equation of the device I-V relations. Using Eq. 4, the electron mobility was measured to be $\mu_{n0} = 5406$ cm^2/Vs

$$\int_0^L I_D dx + \frac{I_D}{\epsilon_c}\int_{V_{S'}}^{V_{D'}} dV_x = \mu_{n0}C_i Z \int_{V_{S'}}^{V_{D'}} (V_{G'} - V_T + V_{S'} - V_x)\, dV_x \tag{3}$$

$$I_D = \frac{\mu_{n0}}{1 + \frac{V_{D'S'}}{\epsilon_c L}} C_i \frac{Z}{L}\left(V'_{GT}V_{D'S'} - \frac{V_{D'S'}^2}{2}\right) \tag{4}$$

However, as the $V_{D'S'}$ depends on I_{DS}, it is needed to expand the whole equation and simplify it via representing constant terms with a single character. Substituting $\epsilon_c L = V_C$ and $(R_D + R_S)C_i\frac{Z}{L}\mu_{n0} = \frac{1}{V_\mu}$, then rearranging into a quadratic form of $V_{D'S'}$, yields

$$V_{D'S'}^2(\frac{1}{2V_\mu} - \frac{1}{V_C}) + V_{D'S'}(\frac{V_{DS}}{V_C} - \frac{V_{G'T}}{V_\mu} - 1) + V_{DS} = 0$$

Here only the '-' sign was adopted after solving the quadratic function; since there is no voltage supply along the drain-source when $V_{DS} = 0V$, the term $V_{D'S'}$ should be omitted as well.

$$V_{D'S'} = \frac{-(\frac{V_{DS}}{V_C} - \frac{V_{G'T}}{V_\mu} - 1) - \sqrt{(\frac{V_{DS}}{V_C} - \frac{V_{G'T}}{V_\mu} - 1)^2 - 4V_{DS}(\frac{1}{2V_\mu} - \frac{1}{V_C})}}{\frac{1}{V_\mu} - \frac{2}{V_C}} \quad (5)$$

Finally, by substituting $I_D = \frac{V_{DS} - V_{D'S'}}{R_D + R_S}$, the general relation I_{DS} versus V_{DS} is found in the linear region of the simple MOSFET model.

$$I_D = \frac{V_{DS}}{R_D + R_S} - \frac{(\frac{V_{G'T}}{V_\mu} + 1 - \frac{V_{DS}}{V_C}) - \sqrt{(\frac{V_{DS}}{V_C} - \frac{V_{G'T}}{V_\mu} - 1)^2 - 4V_{DS}(\frac{1}{2V_\mu} - \frac{1}{V_C})}}{(R_D + R_S)(\frac{1}{V_\mu} - \frac{2}{V_C})} \quad (6)$$

The next step is to make the complementary I-V relations. The saturation (pinch-off) can be calculated by taking the conductance G_d equal to zero.

$$G_d = \frac{dI_D}{dV_{DS}} = \frac{1}{V_\mu} - \frac{1}{V_C} - \frac{\frac{1}{V_C}(\frac{V_{G'T}}{V_\mu} + 1 - \frac{V_{DS}}{V_C}) + 2(\frac{1}{2V_\mu} - \frac{1}{V_C})}{\sqrt{(\frac{V_{DS}}{V_C} - \frac{V_{G'T}}{V_\mu} - 1)^2 - 4V_{DS}(\frac{1}{2V_\mu} - \frac{1}{V_C})}} = 0$$

The solved drain-source voltage point was set to be V_{DS}^{SAT}. Plugging the saturation voltage back into the current general formula Eq. 6, we can get saturation current as well. However, the conductance equation was very complicated to rearrange and calculate V_{DS}^{SAT}. We have to multiply the dominant and square both sides. The substitutions were used again to make the equation easier to solve, namely, $\alpha = \frac{V_C}{V_\mu} - 1$ and $\beta = \frac{V_{G'T}}{V_\mu} + 1$ respectively. Then we rearrange the equation again to form a quadratic function and solve V_{DS}^{SAT} in Eq. 7.

$$\begin{aligned}
&(\frac{1}{V_\mu} - \frac{1}{V_C})^2[(\frac{V_{DS}}{V_C} - \frac{V_{G'T}}{V_\mu} - 1)^2 - 4V_{DS}(\frac{1}{2V_\mu} - \frac{1}{V_C})] \\
&= [\frac{1}{V_C}(\frac{V_{G'T}}{V_\mu} + 1 - \frac{V_{DS}}{V_C}) + 2(\frac{1}{2V_\mu} - \frac{1}{V_C})]^2 \\
&\Rightarrow V_{DS}^{SAT} = V_C[\beta + \alpha - 1 + \sqrt{\frac{2\beta\alpha^2 + (\alpha - 1)(\alpha - 2)^2}{\alpha + 1}}] \quad (7)
\end{aligned}$$

After we solved Eq. 6 and Eq. 7, the simulation of drain-source current versus drain-source voltage was carried out by changing the gate voltage from

0V to 0.8V with a 0.1V step. However, this time the tunneling current along the gate direction was not included, which means $V_G' \approx V_G$.

The simulation was performed by Matlab using Illinois Taub Cluster. Through continuously modifying simulation constants, a family of I-V curves has been established to fit perfectly with the testing data. Since the NDR existed before the saturation of the device, the saturation points of the simulated curves in Fig. 3.2 were bigger than V_{NDR} in the experimental data. The constants were finalized to be $R_D = R_S = 180\Omega$ and the electric field strength along the channel $\epsilon_C = 500\text{V/cm}$.

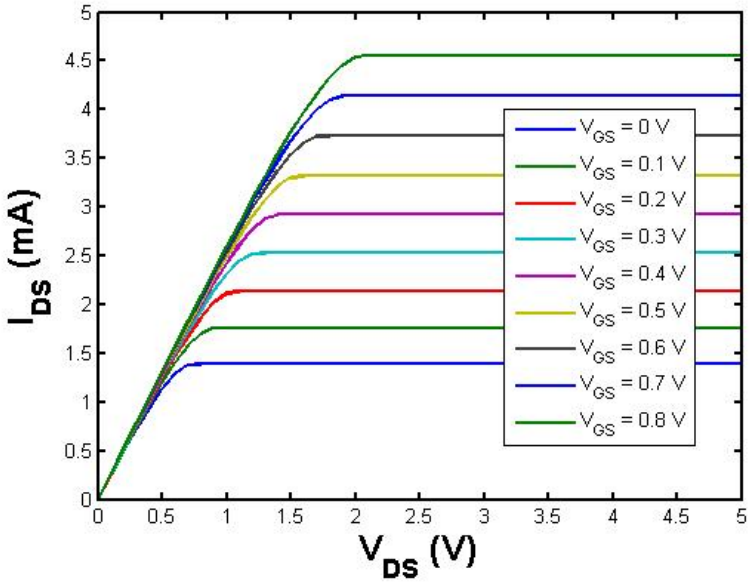

Figure 3.2: Matlab simulated result. Drain-source current versus drain-source voltage without considering tunneling in gate voltage change from 0V to 0.8V with a 0.1V step. Constants are $Rs = Rd = 180\Omega$, $Ci = 0.0038\text{F/m}^2$, $\epsilon_c = 500\text{V/cm}$, $Z = 60\mu\text{m}$, $L = 2\mu\text{m}$ and $V_{th} = -0.47\text{V}$, at room temperature.

3.2 Potential Difference Along the Channel

Before we introduce the tunneling probability, the $V(x)$ needs to be discussed because it is one of the most important intermediate expressions, with a considerable effect on both tunneling probability and charge distribution. The $V(x)$ was the potential difference from position x to source (grounded).

The derivation is based on the same idea as deriving the drain-source voltage of a simple MOSFET circuit device, since at position $x = 0$, $V(x) = V_{S'}$ and when $x = 2\mu$m which was the maximum, $V(x) = V'_D$. This relation was already shown in Fig. 2.1; hence, we use the same integral in Eq. 3 which solved V_{DS}, but change the upper limit from $V_{D'}$ to $V(x)$, and follow all the same steps that we did before from Eq. 3 to Eq. 5. Finally the expression of $V(x)$ should be as follows in which the $V_{G'T} = V'_G - V_T$:

$$V(x) = I_D R_S + (V_{GT} - \frac{I_D}{\mu_{n0} C_i Z \epsilon_c}) - \sqrt{(V_{GT} - \frac{I_D}{\mu_{n0} C_i Z \epsilon_c})^2 - \frac{2 I_D x}{\mu_{n0} C_i Z}} \quad (8)$$

The $V(x)$ actually depends on the drain-source voltage (as it depends on I_{DS}), gate bias, and the position inside the channel. In order to simulate the expression, which has two variables, we decided to fix gate bias and plot $V(x)$ versus x with different V_{DS}. The simulation was done with Matlab using the Illinois Taub Cluster simulator source. The gate bias was set to vary from 0V to 0.8V with 0.1V step, and V_{DS} was set to change from 0.2V to 3V with 0.2V step. Figure 3.3 only shows 2 out of 8 graphs, since it is enough to observe the trend. In order to check whether the simulations are reasonable, we look at the values of $V(x)$ at $x = 0$ and $x = L$ under a specific gate bias. The potential difference at the two points should just be $V_{S'}$ and $V_{D'}$, which can be observed from the circuit in Fig. 2.1. Then take the corresponding I_{DS} value from Fig. 3.2 with same gate bias, and put into Eq. 1.a to get values of $V_{S'}$. For getting $V_{D'}$, choose the one $V(x)$ curve with specific V_{DS} and use Eq. 1.b to get $V_{D'}$. It is found that they fit perfectly with the simulated $V_{D'}$ and $V_{S'}$ under all the gate biases applied from 0V to 0.8V with the corresponding applied V_{DS}. This verifies that the simulated results we have for $V(x)$ are accurate and reasonable.

From the two graphs, it was found that not all the curves corresponding to different V_{DS} were observed. The reason was that once the device reached V_{DS}^{SAT}, the I_{DS} never increased further because of the saturation. On further inspection of Eq. 8, one can see that if I_{DS} is saturated, the trend of the curve will not change any more as the other variables are all constants or changing in the fixed trends. So the curves with V_{DS} higher than the saturation point were overlapped together with the highest value that $V(x)$ can reach under this particular gate bias. The $V(x)$ has a limitation at this point, which will

be discussed in detail in Chapter 5.

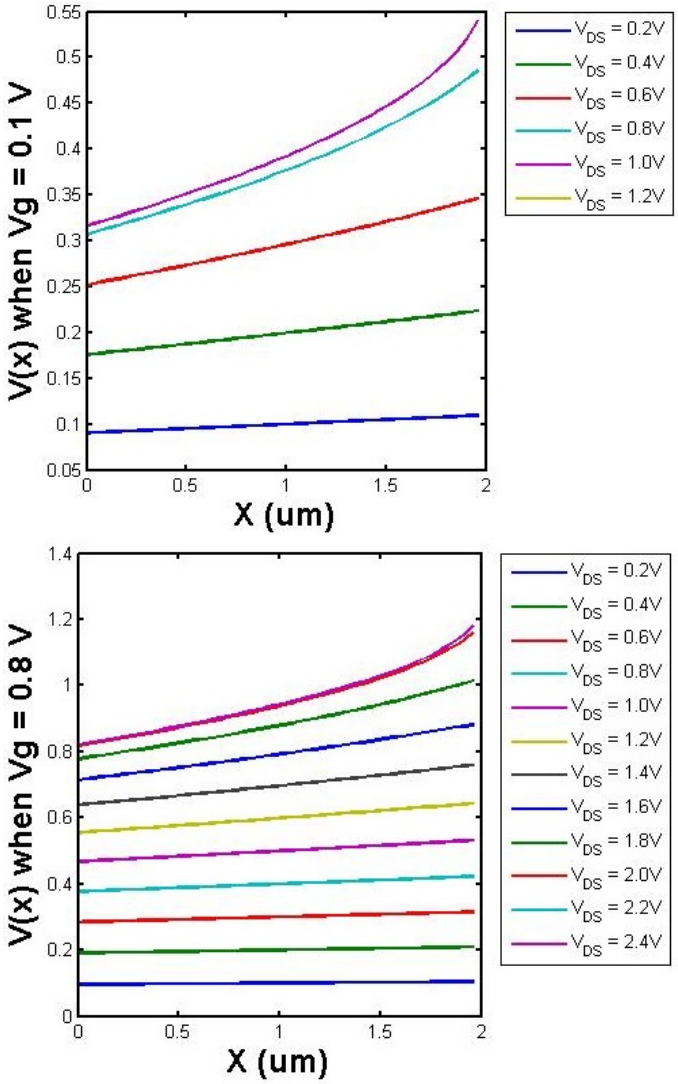

Figure 3.3: Matlab simulated result. $V(x)$ versus x without considering leakage with $V(x) = 0.1$V and $V(x) = 0.8$V, drain-source applied voltage range from 0V to 0.8V with a 0.2V step. Constants are $\mu_{n0} = 5406$ cm^2/Vs, Ci =0.0038F/m^2, $\epsilon_c = 500$V/cm, $L = 2\mu$m, $V_{th} = -0.47$V and $R_S = 180\Omega$ at room temperature.

3.3 Tunneling Probability

After all the constants and intermediate expressions were derived, the tunneling current along the gate was taken into consideration to observe the NDR in the I-V characteristics of the TRSTT, which means $V_{G'} = V_G - I_{GS}R_G$. Above all, the tunnel probability $\theta_y(E_y, x)$ would be the first to introduce. The tunneling probability varies at different position x in the channel, because $V(x)$ changes with position. According to the band diagram in Fig. 2.2, the tunnel probability should be the integration over all energy levels inside the quantum well corresponding with different tunnel length y. The tunneling happened over both of the two barriers between Region I and II, and in Region III. It was difficult to solve, since it needs to consider the motion change of the two barriers at the same time under the applied voltage bias. However, as Fig. 2.2 shows, the barrier height between Region I and II is much lower than that between Region II and III. Because of InGaAs/GaAs straddling the heterostructure, the band gap difference [19], [20] formed the barrier between Region I and II.

For GaAs at 300K,

$$Eg = 1.519 - 5.405 * 10^{-4} * \frac{T^2}{T + 204}(eV)$$

For $In_{1-x}Ga_xAs$ at 300K,

$$Eg = 0.324 + 0.75x + 0.45x^2(eV)$$

From the experimental data for $x = 0.8$, $\Delta E_g = 0.21$eV existed at room temperature. Meanwhile since the discontinuity of the conduction band $Q_c = \frac{\Delta E_c}{\Delta E_g} \approx 0.76$ [10], the barrier between the 2DEG and δ-doped channel was just 0.16eV, about one sixth of the other barrier $\Delta E_m = 0.95$eV. The lower barrier made the tunneling probability much larger than that of tunneling through the gate barrier. In addition, the availability of tunneling charges is much higher in the 2DEG channel than in the upper δ-doped channel, with a shorter tunneling length of 9nm instead of 30nm. All of these factors contributed to our assumption that the tunneling effect of the barrier between Region I and II can be ignored, since the influences on the current are smaller than those

of the larger barrier in Region III. So after all assumptions were applied, it became a single triangular quantum well (QW) tunneling problem, which was much easier to solve. The derivation of tunneling probability starts with the simple time-independent Schrödinger equation [14].

$$-\frac{\hbar^2}{2m^*}\frac{d^2\psi}{dx^2} + V(y)\psi = E_y\psi$$

which can be written as

$$\frac{d^2\psi}{dx^2} = \frac{2m^*(V(y) - E_y)}{\hbar^2}\psi$$

In the device band diagram, the y-axis was considered as the positive direction from left to right (semiconductor to gate), which is the way charge flows (opposite to current flow). Since the barriers between Region I and II were ignored, the y-axis started at $y(0)$ – the δ-doped channel, which was also the overlap of the GaAs spacer and cap layer. Its maximum length reached the metal gate y_m. The energy corresponding to the position y was called E_y and the potential at the point was $V(y)$. The Wentzel-Kramers-Brillouin approximation (WKB) [15] was used to help solve the tunneling probability in a finite QW. It gave us the following general formula:

$$\theta_y(E_y) = e^{-\int_y^{ym} \frac{2\sqrt{2m^*[V(y)-E_y]}}{\hbar}dy} \tag{9}$$

Since the line $E_F = 0$ at equilibrium was set as the reference, the potential difference related to position y along the triangular QW was solved by defining $V(y_m) = \Delta E_m - eV_G + E_F$, and $V(y_0) = -eV(x) + E_F$, where $\Delta E_m = e(\phi_m - \chi)$.

$$V(y) = [V(y_m) - V(y_0)]\frac{y}{ym} + V(y_0) \tag{10}$$

Substituting the line expression $V(y)$ back into the general formula of tunneling probability, Eq. 9, we should get

$$\theta_y(E_y) = e^{-\frac{2}{\hbar}\int_y^{ym} \sqrt{2m^*[V(y_m)-V(y_0)]\frac{y}{ym}+V(y_0)-E_y}dy}$$

Now we rewrite the Eq. 10 to get the relation between the position y and corresponding energy $y = \frac{E_y - V(y_0)}{V(y_m) - V(y_0)} y_m$, and plug it back into the new general formula above to get the final tunneling probability.

$$\theta_y(E_y) = e^{-\frac{4\sqrt{2qm^*}}{3\hbar} \frac{y_m}{V(y_m)-V(y_0)} (V(y_m)-E_y)^{\frac{3}{2}} - [(V(y_m)-V(y_0))\frac{y}{ym} + V(y_0) - E_y]^{\frac{3}{2}}}$$

However, since we already know $V(y_m)$ and $V(y_0)$, substituting them with the terms inside the equation gives us a much simpler expression. However, in the final expression, the variable $V(x)$ played a decisive role which can be observed through the following simulation:

$$\theta_y(E_y, x) = e^{-\frac{4\sqrt{2qm^*}}{3\hbar} \frac{[e(\phi_m - \chi) - eV_G - E_y]^{\frac{3}{2}}}{e(\phi_m - \chi) - eV_G + eV(x)} y_m} \tag{11}$$

The simulation of tunnel probability was also done with Matlab and the results are plotted in Fig. 3.4, which shows a family of curves of probability ranging [0,1] under the gate control from 0V to 0.8V with 0.1V step. The value of potential difference from position x along the channel was set to be a constant varying from 0.2V to 0.7V with 0.1V step. Totally there will be eight simulated graphs, but only the $V(x) = 0$V and $V(x) = 0.8$V are shown below, since it is enough to observe the difference due to the quantity change. The graphs are divided into two sets: the first set consists of two regular plots, and the rest are log plots. The change of tunnel probability can be observed more clearly in log plots. They change uniformly with the uniform change of gate bias, but the increase of $V(x)$ will slow down the tunneling, especially at energy level close to the ground.

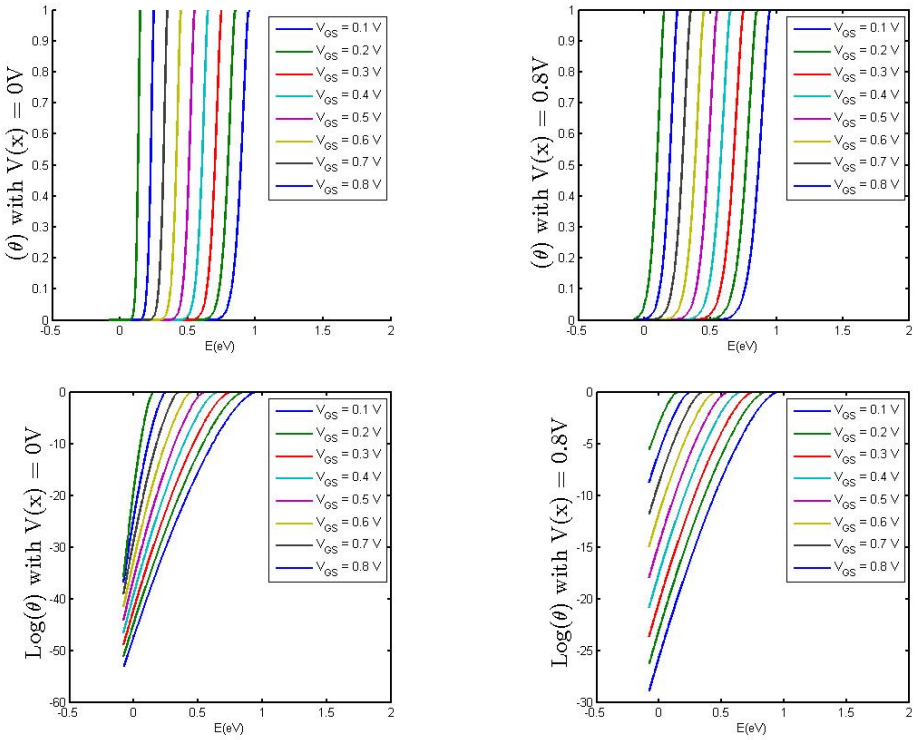

Figure 3.4: Matlab simulated result. Regular/log plots of tunnel probability with $V(x) = 0$V and $V(x) = 0.8$V, gate voltage range from 0V to 0.8V with a 0.1V step. Constants are $\mu_{n0} = 5406$ cm^2/Vs, $R_S = R_D = 180\Omega$, $Ci = 0.0038$F/m^2, $\epsilon_c = 500$V/cm, $Z = 60\mu$m, $L = 2\mu$m, $y_m = 30$nm, $m^* = 1.1m_0$, $\Delta E_m = 0.95$eV, $R_G = 10k\Omega$ and $V_{th} = -0.47$V, at room temperature.

3.4 Speed of Charges Approaching to the Barrier

In addition to the tunnel probability and $V(x)$, another category involved is the speed of charges approaching to the barrier (a triangular QW) of Region III in the band diagram, which shows in Fig. 2.2. By considering quantum mechanics, the semi-classical equation of motion states that velocity with an particular wave vector k will be

$$\upsilon_y(E) = \frac{1}{\hbar}\nabla_{k_y} E_n(k)$$

where $E_n(k)$ is the n-th energy level. And according to the band diagram near the triangular QW, it should be $E_n(k) = E + E(k_y)$. Taking the divergence of the energy level $\upsilon_y(E) = \frac{1}{\hbar}\frac{dE(K_y)}{dk_y}$, then we can have the expression related to energy and the k vector along the y-axis. This will be used later to simplify the gate current equation.

$$\frac{dE}{\hbar} = \upsilon_y(E_y(k)) * dk_y \tag{12}$$

3.5 Gate Current Derivation

The gate current we have is actually a leakage flow from channel to gate. It can be derived from a 2-D leakage current density function and integrated with the whole area along the x-z plane.

$$I_G = \int_0^Z \int_0^L dxdz * J_{leak} = \int_0^Z \int_0^L dxdz * \frac{2}{V_{ol}} \sum_k^{k_y>0} \upsilon_y(E_y(k))\theta_y(E,x)f(E)$$

The sum of the flux in the whole volume of current could be transformed as $\sum_k^{k_y>0} \rightarrow \frac{V_{ol}}{(2\pi)^3}\int d\ \vec{k}$. Then the current density was written to be

$$J_{leak} = \frac{1}{4\pi^3}\int d\ \vec{k_{\|}} * \int_{k_{(y=0)}}^{+\infty} dk_y \upsilon_y(E_y(k))\theta_y(E,x)f(E) \tag{13}$$

In the equation, the charge distribution function $f(E)$ was the only term that was not yet defined. Since the experiment took place at room temperature, and the electron charges are already accumulated in the 2DEG channel at

equilibrium, we set the $f(E)$ to be the Fermi-Dirac distribution [21], [22].

$$\int d\vec{k}_{\parallel}\, f(E) = \int_0^{2\pi} d\rho \int_0^{+\infty} dk_{\parallel} * k_{\parallel} * \frac{1}{1 + e^{\frac{E - E_F + eV(x)}{k_B T}}}$$

The distribution takes the integration over all the energy levels in the QW. To simplify it, we substitute the energy level in the QW to $E = E_y + \frac{\hbar^2 k_{\parallel}^2}{2m^*}$, and use ζ to represent $\zeta = \frac{\hbar^2 k_{\parallel}^2}{2m^* k_B T}$. After yielding them into the distribution function, then we get a term with natural logarithm.

$$\frac{2\pi m^* k_B T}{\hbar^2} \int_0^{+\infty} d\zeta * \frac{e^{-\zeta}}{e^{-\zeta} + e^{\frac{E - E_F + eV(x)}{k_B T}}} \quad \Rightarrow \quad \frac{2\pi m^* k_B T}{\hbar^2} * ln(1 + e^{-\frac{E - E_F + eV_{(x)}}{k_B T}}) \tag{14}$$

The expression of the leakage current density was formed by plugging tunneling probability Eq. 11, the velocity of charges Eq. 12 and charge distribution function Eq. 14 together into Eq. 13. The J_G was the leakage current density at a particular position x along the channel. It is needed to integrate it over all energy levels in QW and the positions on the x-axis to get the final gate current. The E_F in Eq. 15 represents the Fermi-energy level at equilibrium.

$$J_G = J_{leak} = \frac{Z * m^* k_B T}{2\pi^2 \hbar^3} \int_{(E_F - eV(x))}^{+\infty} dE_y * \theta_y(E_y) * ln(1 + e^{-\frac{E - E_F + eV(x)}{k_B T}}) \tag{15}$$

CHAPTER 4

GATE CURRENT DIRECTION

4.1 Before Approaching NDR within $V_{DS} \leq V_{NDR}$

The gate current did not always flow in one direction. As discussed in Chapter 2, the researcher made a mistake in the experiment by confusing the direction of the gate current before and after getting the NDR. From Fig. 2.2, the NDR occurs right at the sudden change of I_G. According to the theory of this thesis, current flowing from metal gate to semiconductor was defined as positive; the NDR happened because of the sharp reverse of current direction. Before the V_{NDR} was reached, the electron charges came equally from both the drain and source sides, then traveled to the middle of the 2DEG channel and tunneled through the GaAs cap layer to the metal gate. The model of charge flow is shown in Fig. 4.1. Since the current flows opposite to the charge flow, the gate current was in the positive direction at this time.

From Figure 4.1, the increase of V_{DS} will reduce the voltage potential difference between gate bias $V_{G'}$ and $V_{D'}$. This will reduce the electron charges that flow from drain to gate, which will result in a drop of gate current. Since $V_{G'} = V_G - I_{GS}R_G$, the decrease of gate current will cause an increase of $V_{G'}$; thus, the channel, and the device as well, will be more opened. The experimental data result in Fig. 2.3 provides evidence to support the conclusion. I_{DS} increases in the linear region with the decrease of the gate current before reaching V_{NDR}.

There is another essential part that needs to be pointed out here. The potential $V_{D'}$ is the value when $V(x)$ reached the maximum of the channel length. Though the V_{DS} was small at this period, we cannot just consider the difference between the gate bias and voltage applied at drain, but we also have to consider the difference in $V(x)$ along the channel. If $V_{G'}$ became smaller

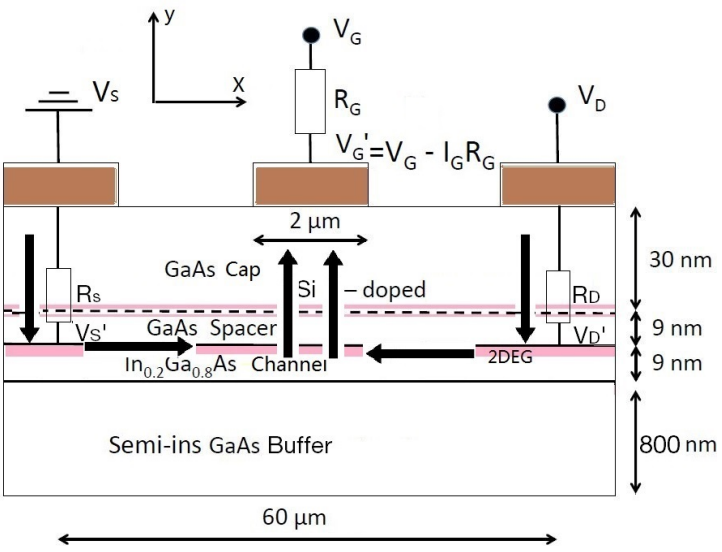

Figure 4.1: When $V_{DS} \leq V_{NDR}$, electrons flow from drain and source to the gate, the gate current drops along with the increase of V_{DS}. The NDR occurs once the V_{NDR} has been reached.

than $V(x)$ at a particular position x^*, then from source to this position, the electrons will flow right from source side to gate, and the current I_1 will go from metal to semiconductor. On the other side, electrons go from gate to drain with a current I_2 flowing in an opposite direction. Hence the total gate current would be the difference between the two portions of the current. Since the I_1 went the same positive direction as the gate current, then $I_G = I_1 - I_2$. The structure is shown in Fig. 4.2.

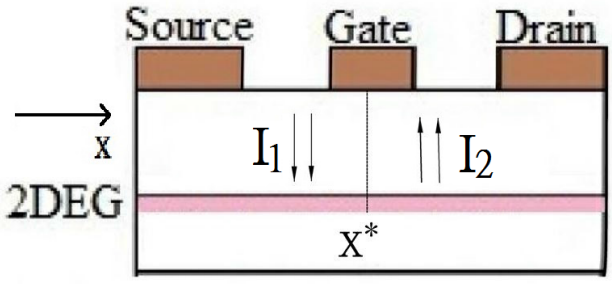

Figure 4.2: Tunnel effective length x^* is the position value when $V(x) = V_{G'}$.

I_1 can be obtained by integrating the current density from source $x = 0$ to $x = x^*$ along the x-axis. And I_2 of course will be the current integrated from x^* to maximum gate length $L = 2\mu$m. Gate current will be the difference between the two portions of current, which is shown in Eq. 16. The

simulation of the gate current in period $V_{DS} \leq V_{NDR}$ will be shown together with the whole period to be discussed next.

$$I_G = I_1 - I_2 = \int_0^{x^*} J_G dx - \int_{x^*}^{2\mu m} J_G dx \tag{16}$$

4.2 After Getting NDR in $V_{DS} > V_{NDR}$

Once V_{DS} exceeds V_{NDR}, the story will be different. NDR happens as the gate current suddenly drops to negative, and its magnitude increases with that of V_{DS}. The mechanism behind this relation is similar to that explained in Section 4.1. However, in this period, since V_{DS} keeps increasing, $V_{G'}$ drops. This causes V_{DS} to be much larger than $V_{G'}$, and even the voltage at the $x = 0$, $V_{S'}$, is larger than $V_{G'}$. Then the electrons flow from source and gate all the way through the channel to the drain in Fig. 4.3. Hence, the gate current will go from semiconductor to metal gate across the whole channel length, which is in the negative direction according to the definition.

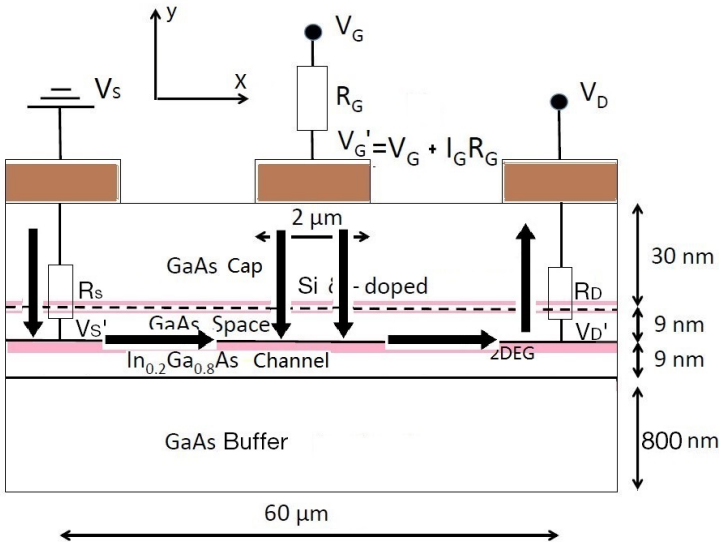

Figure 4.3: When $V_{DS} > V_{NDR}$, electrons flow from gate and source to drain; the gate current goes in the negative direction and increases in magnitude with increasing V_{DS}.

At this time, the current density integration takes the range of the whole

gate length from 0 to L to obtain the gate current with a negative sign.

$$I_G = -\frac{Z * m^* k_B T}{2\pi^2 \hbar^3} \int_{(-eV(x))}^{+\infty} dE_y \int_0^{2\mu m} dx * \theta_y(E_y, x) * ln(1 + e^{-\frac{E - E_F + eV(x)}{k_B T}}) \tag{17}$$

CHAPTER 5

SIMULATION RESULTS AND CONCLUSION

5.1 Gate Current Simulation Results

The purpose of this simulation is to verify that the model of the gate current (leakage current) we built fit the experimental data, and accordingly to observe a λ-shaped NDR on the drain-source I-V characteristic of the TRSTT device. After simulating the theoretical models, we can deeply investigate the control categories of the NDR in a TRSTT device. Eq. 16 and Eq. 17, which are the two portions of the gate current, will constitute the majority of the simulation work. And the gate current values will be put back into Eq. 6 and Eq. 7 to observe the NDR of drain-source current curves.

The whole simulation contains multiple variables mainly in two sections. One is the voltage control, which consists of gate bias V_G and drain-source voltage supply V_{DS}. The other is position variables along the x,y,z axes, with an exception – the energy levels in QW. Since the voltage potential $V(x)$ in Eq. 8 depends on gate bias $V_{G'}$, it contains a variable of I_G, which is the dependent variable that will be simulated. Hence, iterations were used to finalize the answers. The gate current calculated in the previous stage was put back into the equation $V_{G'} = V_G - I_{GS}R_G$ as a variable, and the rest of the calculation steps were followed. When the simulation converged, the answer was within 0.1% of the previously calculated gate current. Then this value was accepted to the final results. All the calculations and intermediate steps were accomplished with Matlab, using the Illinois Taub Cluster as the simulator.

The result is shown in Fig. 5.1 with V_G and V_{DS} varying from 0V to 0.8V and 0V to 5V respectively. Both of the two variables have 0.1V step. The family of curves under different gate biases is exactly within the theoretical

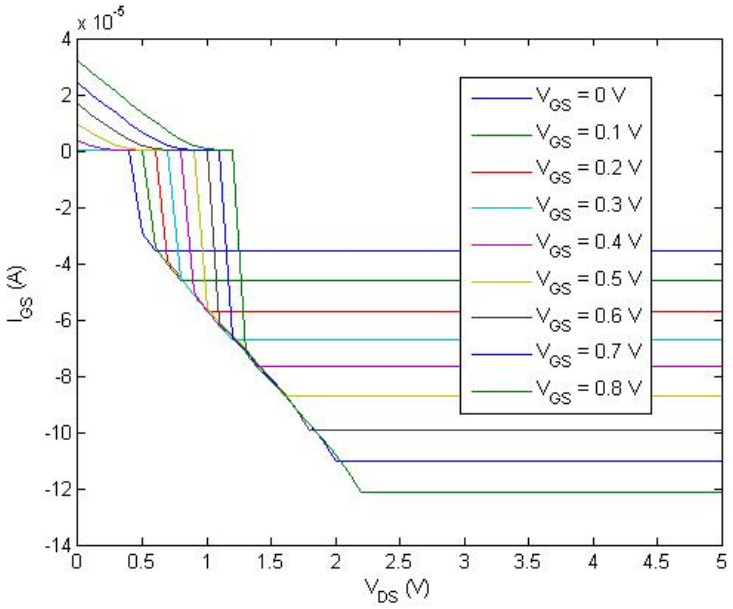

Figure 5.1: Gate current versus drain-source bias with gate current increasing from 0V to 0.8V in 0.1V step. Constants are $\mu_{n0} = 5604$ cm^2/Vs, $R_S = R_D = 180\Omega$, $C_i = 0.0038$F/m^2, $\epsilon_c = 500$V/cm, $Z = 60\mu$m, $L = 2\mu$m, $V_{th} = -0.47$V, $m^* = 1.1m_0$, $\Delta Em = 0.95$eV at room temperature.

model expectation in the period $V_{DS} \leq V_{NDR}$. The current value drops sharply from positive to negative right at $V_{DS} = V_{NDR}$. Referring back to Fig. 2.3, the experimental data at $V_{DS} \leq V_{NDR}$, it is found out that the highest gate current occurs at $V_{DS} = 0V$ with the value around 32μA. And the separations between the start points of the other curves look uniform, which is just the case we have in our simulation as well. The values after the sudden drop also fit with the experimental data, which vary within $40-70\mu$A. The only exception is the current magnitude, which stays constant instead of increasing with V_{DS} from the experimental data. The main reason is that the solution we have for $V(x)$ is not complementary.

5.2 Drain-Source Current Simulation Results

Before discussing the limitation of $V(x)$, the drain-source current I-V simulation should be analyzed in detail. We put the I_G values in Fig. 5.1 into $V_{G'}$ in Eq. 6 and Eq. 7 to have the current curves as shown in Fig. 5.2. The λ-shaped NDR manifests as expected. Comparing with the

experimental data in Fig. 2.3, the gate current is similar, and the simulated results fit perfectly at $V_{DS} \leq V_{NDR}$. However, when the drain-source voltage approaches V_{NDR}, the sudden drop in current magnitudes is less than that in the experimental data, especially under higher gate bias, and it holds constant later on. This makes the peak-to-valley current ratio (PVR) smaller than that of the experimental data. It is not surprising that the reason for this problem is the same as that in the gate current simulation. When the device starts to get saturated after the NDR, the derived $V(x)$ is a general solution which works very well in the linear region, but less so when approaching saturation. Though the PVR drops, it is still in an increasing trend from 2 to around 3 with the gate bias going from 0V to 0.8V, which verifies that the gate bias depends on the gate current which can be used to control the NDR effects, especially by increasing it. This conclusion was also reached by [23] in 2006 by testing an InGaAs dual channel transistor.

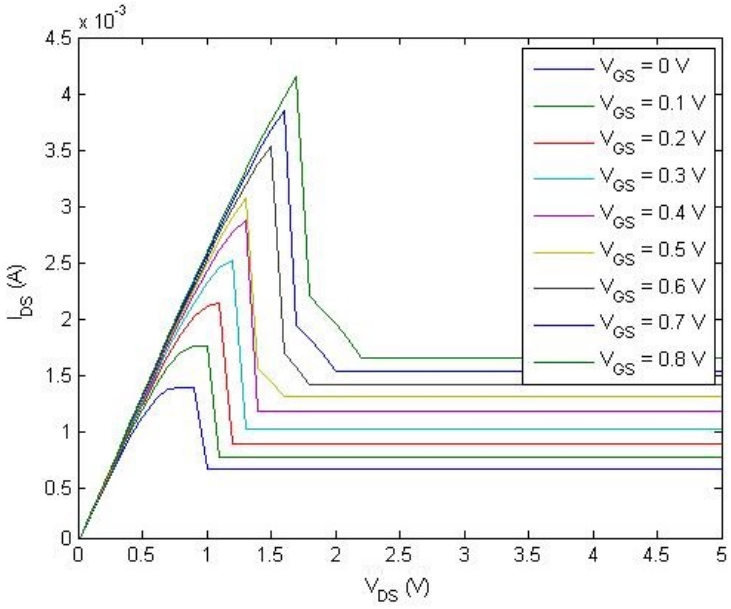

Figure 5.2: Drain-source current versus drain-source voltage considering gate tunneling with gate current increasing from 0V to 0.8V in 0.1V step. Constants are $\mu_{n0} = 5604$ cm^2/Vs, $R_S = R_D = 180\Omega$, $C_i = 0.0038$F/m^2, $\epsilon_c = 500$V/cm, $Z = 60\mu$m, $L = 2\mu$m and $V_{th} = -0.47$V at room temperature.

Refer back to Fig. 3.3, which reports a simulation of $V(x)$ without considering the gate current $V_{G'} \approx V_G$. Another set of $V(x)$ simulations which including the leakage current is shown in Fig. 5.3, which help us

to observe the limitation of $V(x)$ under more complementary conditions. The sudden drop of the $V(x)$ values at $x = 0$ under larger applied V_{DS} is reasonable because of the effects from the NDR. Amazingly, both the sets of curves in Fig. 3.3 and Fig. 5.3 exhibit the same problem, namely that $V(x)$ stays the same after device saturation.

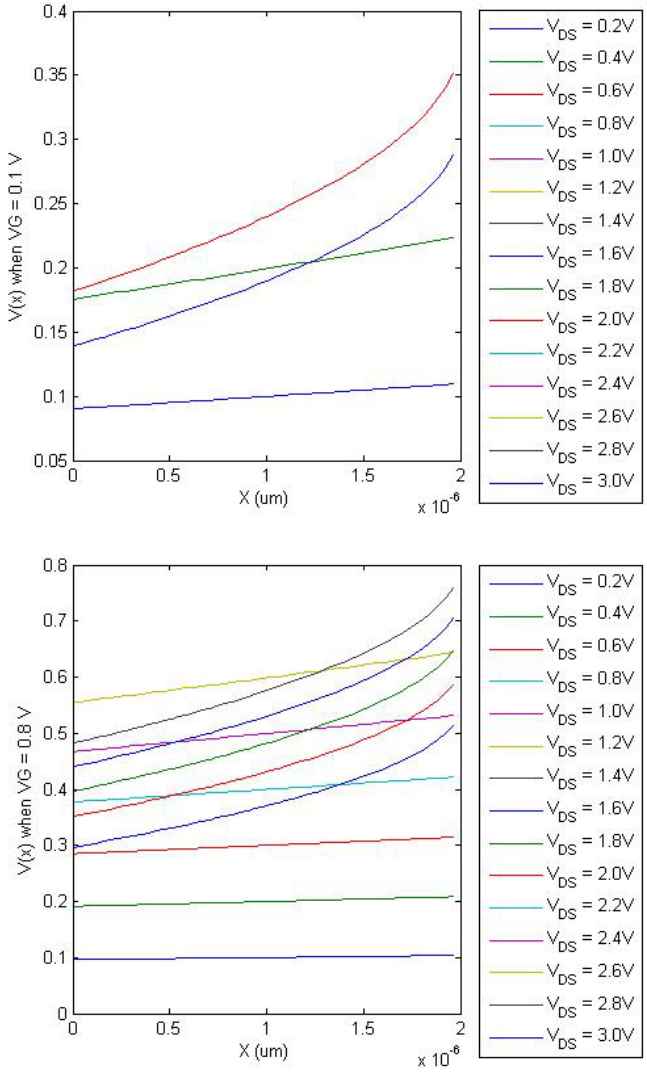

Figure 5.3: Matlab simulated result, $V(x)$ versus x including leakage with $V(x) = 0.1$V and $V(x) = 0.8$V, drain-source applied voltage range from 0V to 0.8V with a 0.2V step. Constants are $\mu_{n0} = 5406$ cm^2/Vs, $Ci = 0.0038$F/m^2, $\epsilon_c = 500$V/cm, $L = 2\mu$m and $V_{th} = -0.47$V and $R_S = 180\Omega$ at room temperature.

According to device physics, after pinch-off of the channel, the continued increase of V_{DS} should cause a "snap back" of the pinch-off point. Then the

electric field will reach maximum and electrons will drift from that point all the way to the drain side. The electric field strength should be incredibly large from the pinch-off point to the end of the channel. However, the $V(x)$ derived before stays constant after exceeding saturation without having the "snap back" effect. Considering the $V(x)$ equation and analyzing numerically, one finds that the main problem lies in the square root term of Eq. 8. According to expectation, this term should approach maximum faster with increasing V_{DS}. To be more precise, it is the inside term $\frac{2I_D x}{\mu_{n0} C_i Z}$ becoming less dominant that makes $V(x)$ never increase faster when V_{DS} increases. Thus, another expression after V_{DS}^{SAT} is needed to make a complementary model of $V(x)$. It will definitely be the most essential improvement to be done in future work.

CHAPTER 6

FURTHER RESEARCH DEVELOPMENT

6.1 Expectation Model of $V(x)$ in Future Work

An idea from [24] can be adopted to build the new $V(x)$ model. The model comes from a conventional silicon MOSFET structure. It mainly describes the Δx that "snaps back" along the channel from the maximum channel length to the pinch-off point, which is controlled by gate bias under different drain-source voltages. The l in Eq. 18 is calculated by $\sqrt{\frac{\epsilon_{GaAs}}{\epsilon_{ox}} * T_{ox} * x}$, where ϵ_{GaAs} and ϵ_{ox} are both permittivity, T_{ox} is the thickness of the gate oxide, and ϵ_{SAT} is the field strength in the channel after saturation.

$$\Delta x = l * sinh^{-1}[\frac{V_{DS} - \frac{V_{G'T}\epsilon_{sat}(L-\Delta X_0)}{V_{G'T}+m\epsilon_{sat}(L-\Delta X_0)}}{l * \epsilon_{sat}}] \tag{18}$$

To solve the equation above, iteration is needed, in which ΔX_0 is a value we defined to be the initial value of Δx in the first stage. After calculating the "snap back" distance, we let the $V(x)$ increase to maximum at the point $x = L - \Delta x$, and hold it constant from the point to drain in the channel. Simulating the idea until it converges, Fig. 6.1 is the expectation curve model of $V(x)$ without considering leakage. The new expectation model has $V(x)$ reaching maximum faster with larger applied V_{DS}. Looking back at the band diagram in Fig. 2.2, the earlier the $V(x)$ gets to its maximum along the channel, the deeper the δ-doped channel will be, which makes the barrier thinner (shorter tunnel length). And this causes the tunneling probability to increase as well as the charge distribution. Hence, the magnitude of the gate current at $V_{DS} > V_{NDR}$ will increase (more leakage happen), which will make a slow increment of $V_{G'}$. Then the I_{DS} will increase as well. All of

these expectations fit with the experimental data in Fig. 2.3.

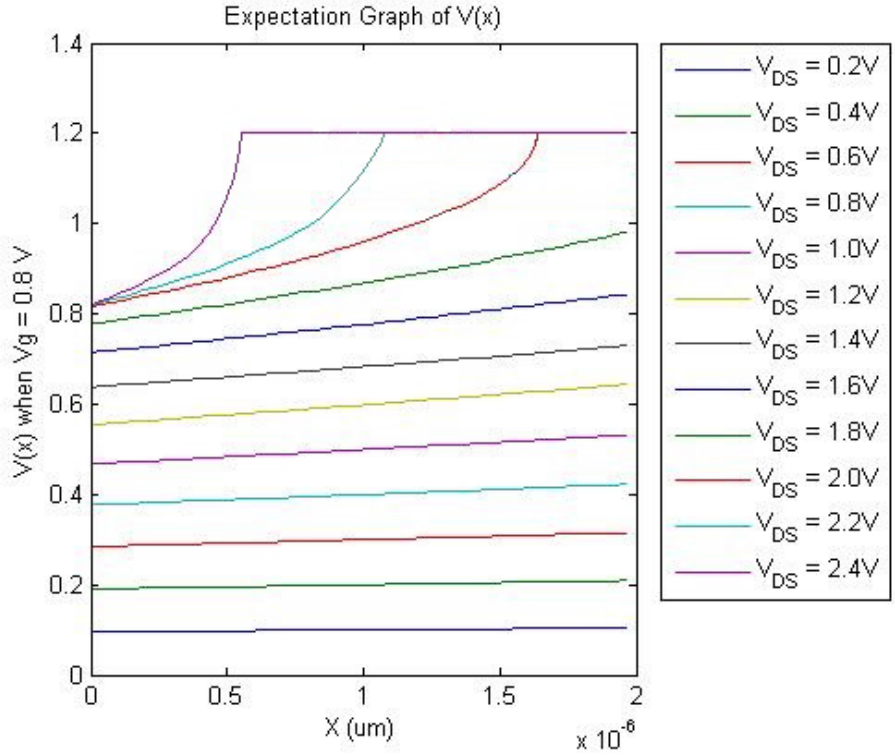

Figure 6.1: Expectation curve of $V(x)$ versus x without leakage under $V(x) = 0.8$V, drain-source applied voltage range from 0V to 0.8V with a 0.2V step. Constants are $\mu_{n0} = 5406\text{cm}^2/\text{VS}$, $Ci = 0.0038\text{F/m}^2$, $\epsilon_c = 500\text{V/cm}$, $L = 2\mu\text{m}$, $Z = 60\mu\text{m}$, $V_{th} = -0.47\text{V}$ and $R_S = 180\Omega$ at room temperature.

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