Development of low power readout electronics for micro channel plate detectors with cross strip anodes for UV space observatories

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Zusammenfassung

Der wissenschaftliche Fortschritt in der Astrophysik wird maßgeblich unterstützt durch Beobachtungen im ultravioletten (UV) Wellenlängenbereich des elektromagnetischen Spektrums. Die Erkenntnis über spezielle Eigenschaften astrophysikalischer Objekte ist allein durch Beobachtungen im UV möglich. Am Institut für Astronomie und Astrophysik in Tübingen (IAAT) werden neuartige, photonenzählende Mikrokanalplatten (MCP)-Detektoren entwickelt, um die wissenschaftliche Arbeit im ultravioletten Spektralbereich deutlich zu verbessern. Zusätzlich sind diese Detektoren unempfindlich im optischen Spektralbereich. Für den Einsatz der Detektoren in wissenschaftlichen Satelliten sind eine höhere Empfindlichkeit, eine längere Lebensdauer und eine geringe Leistungsaufnahme entscheidende Eigenschaften. Diese sind im Fokus der Arbeit am IAAT.

Im Rahmen dieser Dissertation wurde ein neuartiges Konzept für eine Elektronik zur Auslese der MCP-Detektoren untersucht und realisiert. Das Konzept ermöglicht die Erhöhung der Lebensdauer bei gleichzeitig geringer elektrischer Leistungsaufnahme. Die Schlüsselkomponente zur Realisierung des Konzeptes ist der `Beetle` Vorverstärker-Chip, welcher am Max-Planck-Institut für Kernphysik in Heidelberg für das LHCb-Experiment am CERN entwickelt wurde. Zur Steuerung und Auslese des `Beetle` Chip und weiterer elektronischer Komponenten wurde eine entsprechende Einheit in einem field-programmable gate array (FPGA) umgesetzt. Des weiteren wurde Steuer- und Analysesoftware implementiert. Für Tests der Ausleseelektronik wurden ein Gerät zur Ladungseinkopplung und ein Laboraufbau realisiert.

Die akkurate Verarbeitung von Signalen ähnlich denjenigen eines MCP-Detektors wurde durchgeführt. Komponenten, welche eine weitere Verbesserung der Ausleseelektronik hinsichtlich ihrer wissenschaftlichen Zielsetzung ermöglichen, wurden in Betrieb genommen.

Die korrekte Funktion einer weltraumtauglich realisierbaren Ausleseelektronik mit geringer Leistungsaufnahme wurde in dieser Arbeit gezeigt. Damit können MCP-Detektoren für zukünftige UV-Missionen gebaut werden, die einen bisher unerreichte Lebensdauer und Dynamik besitzen.

Abstract

Scientific progress in astrophysics is strongly supported by observations in the ultraviolet (UV) wavelength regime of the electromagnetic spectrum. Insight into unique features of astrophysical objects is only possible in the UV. At the Institute for Astronomy and Astrophysics in Tübingen (IAAT), novel solar blind and photon counting micro channel plate (MCP) UV detectors are developed to improve scientific work in the UV significantly. For the application of the detectors in satellite observatories, enhanced sensitivity, longer lifetime and low power dissipation are crucial properties. These are at the focus of the work at IAAT.

In this thesis, a novel concept of low power readout electronics for the MCP detectors has been investigated and realized. The concept furthermore allows for an enhanced lifetime of the detectors. The `Beetle` pre-amplifier chip which was developed at Max-Planck-Institute for Nuclear Physics in Heidelberg for LHCb at CERN is the key component to realize the concept. To control and readout the `Beetle` chip and further electronic components, a corresponding unit was implemented in a field-programmable gate array (FPGA). Control and analysis software was furthermore implemented. For tests of the readout electronics, a charge injector device and a readout electronics laboratory setup were manufactured.

The accurate readout of signals that are comparable to signals from an actual MCP detector was performed. The commissioning of components to further improve the electronics setup in terms of the scientific constraints was carried out.

The proper function of a low power readout front-end electronics for MCP detectors that can be implemented space-qualified was shown in this work. It allows to build MCP detectors for future UV missions that have a so far unrivaled lifetime and performance.

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Introduction

Astronomy is one of the oldest natural sciences. Ancient civilizations studied the motion of celestial objects and, despite the fact that the motivations were essentially religious or mythological, astronomical observations already have been used to establish calendars and to improve navigation. Astronomy as a mathematical science was established among the Babylonians however and was advanced in ancient Greece by the motivation to find physical explanations for celestial phenomena.

Astronomy today is the quantitative science of celestial observations and the underlying physical laws. The origin, physical properties, and the evolution of celestial objects in the Cosmos is at the focus of it.

The probes of astronomy are the particles and the radiation that stem from inside or the environment of celestial objects. Telescopes equipped with instruments like spectrographs, photometers, and imaging cameras are the experimental tools. Simulation of the physical conditions that are observed is the theoretical approach.

Astronomical observations of electromagnetic radiation from the Universe is possible in a wide energy range from below 10^{-4} eV in the radio band to above 10^{9} eV in the gamma regime. The ultraviolet (UV) spans the energy range from 5 eV to 100 eV which is usually expressed as a wavelength range of 91.2 nm to 300 nm.

UV astronomy covers a wide range of topics like the evolution of the Universe and its baryonic content, the physics of accretion and outflow in celestial objects, and the astrochemistry in the presence of strong radiation fields. UV observations are the only way to explore specific features of astronomical objects as resonance lines of the most important atoms and ions are located in the UV.

UV observations started in the late 1940s when unstabilized sounding rockets have been used to escape the atmosphere of Earth which blocks the UV radiation from the Universe. Spin-stabilization of the rockets and cold-gas reaction systems allowed for the observation of specific targets. However, the observation time was limited to a few hundred seconds. Satellites are used nowadays as platforms to observe the Universe in UV

light. They enable a longer observation time per target and a large number of targets that can be observed by the same instrument.

A variety of technologies were used on board of recent satellite observatory missions to acquire UV data. Progress was made during the last decades in the fields of detector efficiency, throughput, and lifetime of UV instruments. The progress was enabled by new gratings and coatings, novel detector configurations, and efficient readout electronics. Improved detector technology for UV observations is mandatory to expand the frontiers of scientific perception. For an application of detectors on future UV observatories, enhanced sensitivity, longer lifetime, and low power dissipation are crucial properties.

The development of novel photon counting, solar blind, and photon noise limited micro channel plate (MCP) detectors at the Institute for Astronomy and Astrophysics in Tübingen (IAAT) is a contribution to future astronomical UV space missions. The investigation of improved photocathode materials and a novel readout anode geometry are at the focus of research. The low power MCP detector readout electronics concept which was realized and tested in this work is a part of this development project at IAAT. It will allow to build MCP detectors for future UV missions that have a so far unmatched lifetime.

This doctoral thesis is organized as follows:

An overview of the questions that are addressed by observations in the ultraviolet spectral band is given in Chapter 1. Past and future instruments which are engaged by astronomers to answer these questions are described as well.

Chapter 2 gives an overview of technology that is available for UV observations with a focus on the micro channel plate detector concept and the components that have been applied in past and present realizations of MCP detectors. In Chapter 3, an MCP detector design that is investigated at the IAAT is described and its individual components are introduced. Details on an ultra-high vacuum facility for the production of photocathodes and the sealing of detector tubes are given.

The general readout electronics concept for this work is described in Chapter 4. The realized laboratory readout electronics and its components are introduced. Details on the specific function of the components are given. The `Beetle` chip and its architecture and function are discussed as

well as details on the control and readout unit in the field-programmable gate array (FPGA). At the end of Chapter 4, the control and first-level analysis software is introduced.

Chapter 5 shows details on setups to test the readout electronics. In particular, a charge injector device and a setup in a vacuum chamber are introduced. Selected measurement runs and analyzed data to prove the proper function of the laboratory readout electronics are presented.

After a conclusion, the thesis ends with the Appendix where technical details in the form of schematics and pin tables of the readout electronics setup are given.

1. Astronomy in the ultraviolet spectral band

The motivation to perform astronomy in the ultraviolet (UV) wavelength band of the electromagnetic spectrum, is the fact that UV radiation interacts with matter in many physical conditions. Most of the resonance lines of atoms are excited in this energy domain. Simple ions have fluorescent transitions in this wavelength domain as well. Most molecules and atoms are photo-ionized or even photo-dissociated by ultraviolet radiation. Hence, as the UV radiation can be observed by astronomers, its interaction with the matter in the Universe and by this the properties of the matter itself can be investigated (Brosch et al., 2006).

Here we follow a convention stated by Werner (2010) for the limits of the ultraviolet spectral band: The UV band spans the wavelength range from 91.2 nm to 300 nm. The lower limit is the hydrogen Lyman absorption edge that shows up in observed spectra at 91.2 nm. Below this edge, the extreme ultraviolet (EUV) reaches down to 10 nm. Radiation that has wavelengths above 300 nm is accessible by ground-based telescopes while observations below 300 nm have to be performed outside the atmosphere of the Earth. This is the case because UV radiation is blocked by the ozone layer in Earth's atmosphere and hence a natural upper limit for the UV band is given. The UV band can be further divided into the far-UV (FUV) that spans from 90 nm to 200 nm, and the near-UV (NUV) between 200 nm and 300 nm. The wavelength range of the FUV and EUV below 200 nm down to 10 nm is often referred to as the vacuum-UV (VUV).

The work on the development of novel micro channel plate UV detectors at the Institute for Astronomy and Astrophysics in Tübingen is intended as a contribution to the improvement of the observation technology that will be used in the future to expand the scientific frontiers of UV astronomy. The development has been started with the aim to deliver detectors for the WSO-UV satellite observatory project which is discussed below.

This chapter gives an overview of the questions that are addressed by UV astronomy. The instruments utilized to answer these questions are described as well.

The following sections start with an introduction to the scientific topics

that modern UV astronomy is faced with and the methods that are used to deal with specific problems. In the second part of this chapter, an overview of the history and current status of UV missions and their instruments is given. The chapter ends with an outlook on the future of observational astronomy in the ultraviolet wavelength regime.

1.1. Scientific topics and methods

This section gives an overview of the scientific topics that modern UV astronomy deals with. Methods to answer the physical questions are introduced. The section presents a concrete example of the UV spectroscopic investigation of the central star in the Stingray Planetary Nebula and the modeling of its physical properties at IAAT. As far as not stated specifically, general information in this section is taken from the articles in Dopita et al. (2006).

Due to the fact that UV radiation interacts with matter in nearly every state, a huge amount of objects from different classes (see Figure 1.1) can be observed in the UV and hence a lot of phenomena can be explored in this spectral band. Gómez de Castro et al. (2006a) present three key fields of modern astronomy which are also key scientific issues to be addressed by the upcoming WSO-UV satellite observatory (see Section 1.3) (Gómez de Castro et al., 2009):

- The chemical evolution of the Universe and the diffuse baryonic content in the Universe
- The physics of accretion and outflow in astronomical objects
- The atmospheres of extrasolar planets and the astrochemistry in the presence of strong UV radiation fields

Further fields and classes of objects are stated by Gómez de Castro et al. (2006a) in addition to the key fields that are listed above:

- The Solar System. Data that are acquired in the UV and data that are acquired in other bands as well as the combination of these data sets is essential to understand the nature of the celestial bodies in our neighborhood and hence the evolution of the overall Solar System.

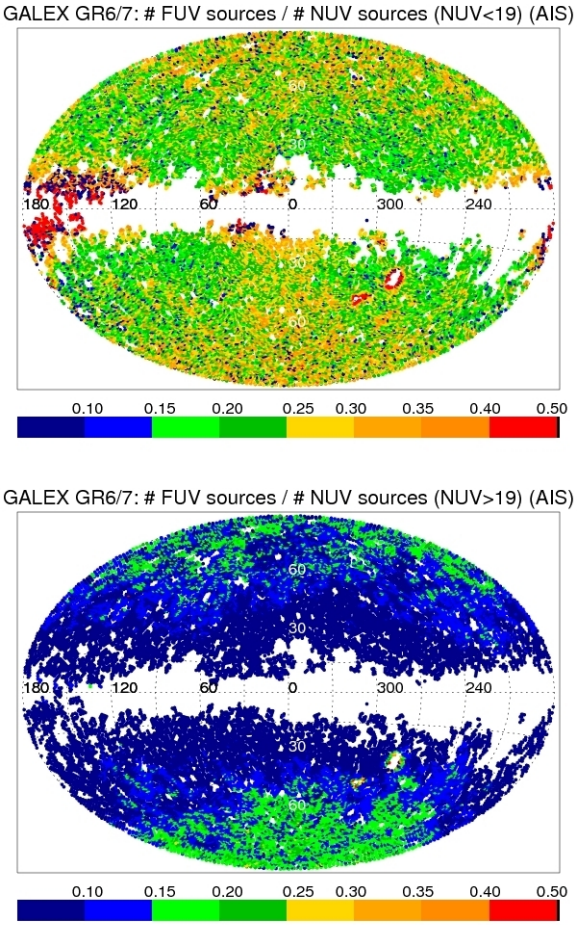

Figure 1.1.: Fraction of sources in the FUV (134.4 nm-178.6 nm) and NUV (177.1 nm-283.1 nm) bands from the all-sky imaging survey (AIS) by GALEX (Section 1.2). Top: sources brighter than $m_{\mathrm{AB}} = 19$ mag, bottom: sources fainter than 19 mag in the NUV band. Brighter sources are dominated by hot stars in the Milky Way, fainter ones are extragalactic. Taken from Bianchi (2014), see also Bianchi et al. (2014).

- Star and stellar system formation. Most (65%) of the volume of the interstellar medium (ISM) is filled with diffuse gas at temperatures between 3000 K and 300 000 K. This gas is best observed in the UV. Absorption spectroscopy is the best tool to study the properties of circumstellar gas and the atmospheres of planets close to the central star that transit the stellar disk.

- Cool stars. The UV is unique to study their atmospheres.

- Massive stars. As the maximum of their spectral energy distribution is in the UV, it is the optimal spectral window to explore massive stars.

- White dwarfs, their structure and evolution as well as their interaction with the ISM. Far-UV spectra in the wavelength region between 122 nm and 200 nm are essential to determine the composition of white dwarfs and the evolution of their atmospheres. Imaging of the sky yields complementary information and is an important way to discover binary systems (Barstow and Werner, 2006).

- Interacting binaries in general. A large part of the interaction energy is released by radiation in the UV regime.

- Active galaxies have their maximum flux in the UV.

- Starbursts. The existence of one ore more initial mass functions (IMF)[1] and the form of the IMF, the possible modes of the star formation, and the interaction between massive stars and the ISM and intergalactic matter (IGM) can be explored.

- Supernovae.

In the following, details on selected key fields are given. Though they are mentioned as separate fields of research, they are strongly related and insight is most promising when they are all taken into account.

[1] A function that describes the distribution of the initial masses in a population of stars.

The chemical evolution of the Universe. The chemical evolution of the Universe is driven by its enrichment of heavier elements that are produced in stars and released in supernova explosions at the end of their life time, distributed by stellar winds, or when planetary nebulae form at the end of the life of their solar-type progenitors. Hence, it is crucial to understand the life cycle of these stars to be able to comprehend the chemical evolution of the baryonic matter in the Universe. Simulations of the magneto-hydrodynamic turbulence in stellar atmospheres combined with data that are acquired in the UV are used to understand the thermal and dynamical evolution of the stars and diffuse gas in the Universe (Gómez de Castro et al., 2006a).

The interstellar matter is the raw material for star formation and the outcome of the star evolution process is the enrichment of the intergalactic matter with chemical elements heavier than those produced during the formation of the Universe. The warm gas of the ISM is best observed by the absorption of UV radiation in resonance lines of the elements in the gas. Many issues raise in this context that require attention. The structure of warm interstellar gas clouds and the consequences of the interaction of interstellar gas clouds are at the focus of discussion. Furthermore, it has to be determined in which way the ISM is influenced if star bursts occur in the proximity of the clouds. The theory of galaxy formation can be rechecked when one determines the portion of material in the local ISM that has its origin in a foreign region of the Galaxy (Linsky, 2009).

As the interstellar and intergalactic matter is the raw material for star formation, the mechanisms that cycle the gas from the ISM and IGM to feed the star and galaxy formation, respectively, have to be understood. The star formation rate is impacted by the efficiency of the gas transport mechanisms from and between the matter reservoirs. To track the overall evolution of the ISM and IGM, one has to establish a connection between the nearby and the early Universe. The early Universe can be observed in red-shifted UV wavelengths even via ground based telescopes. SNIa supernovae are consulted as standard candles to measure cosmic distances. The observation of more distant SNIa is necessary to determine distances in the even more early epochs of the Universe. It is only possible to identify Type I supernovae and distinguish them from Type II supernovae when taking their UV spectral distribution into account (Wamsteker et al., 2006).

The physics of accretion and outflow. Active Galactic Nuclei, white dwarfs that accrete matter, and T Tauri stars are examples for objects that transform energy of various form into corresponding other forms when they accrete matter from their surrounding. These energy forms can be potential energy, thermal energy, radiation, and magnetic energy for example. Furthermore, angular momentum has to be conserved and for example magnetic flux is built up during gravitational contraction (Gómez de Castro et al., 2006b, 2009).

The identification of the several possible interaction regions is the key to understand the phenomenon of accretion (Gómez de Castro et al., 2006a):

- In Active Galactic Nuclei and microquasars, FUV radiation is produced by an accretion disk.
- Where white dwarfs accrete matter, UV radiation is produced in the atmosphere of the accretion disk and the atmosphere of the white dwarf itself.
- In addition, UV radiation in T Tauri objects is produced in an extended magnetosphere.

Non-relativistic objects provide the best opportunity to study the accretion and outflow of matter in cosmic engines. To distinguish accretion and outflow in observations, the UV line profiles are the best footprint that is visible in the spectra.

For example, Figure 1.2 shows the time evolution of the UV spectrum of the central star of the so-called Stingray Planetary Nebula (SAO 244 567, Figure 1.3). The N V and C IV resonance lines display P Cygni profiles that are characteristic for a strong stellar wind. These lines almost vanished during one decade. By comparison with synthetic spectra which have been computed with appropriate stellar atmosphere models it could be shown that the mass-loss rate strongly decreased within this decade. This fact indicates an unusually fast evolutionary rate of the star that was probably caused by a re-ignition of helium-fusion in the white dwarf progenitor star (Reindl et al., 2014).

As the understanding of the underlying physics in accretion and outflow phenomena improves, new observations that employ instruments which are more sensitive and provide a better spatial and spectral resolution compared to current instruments are required (Gómez de Castro et al., 2006a,b).

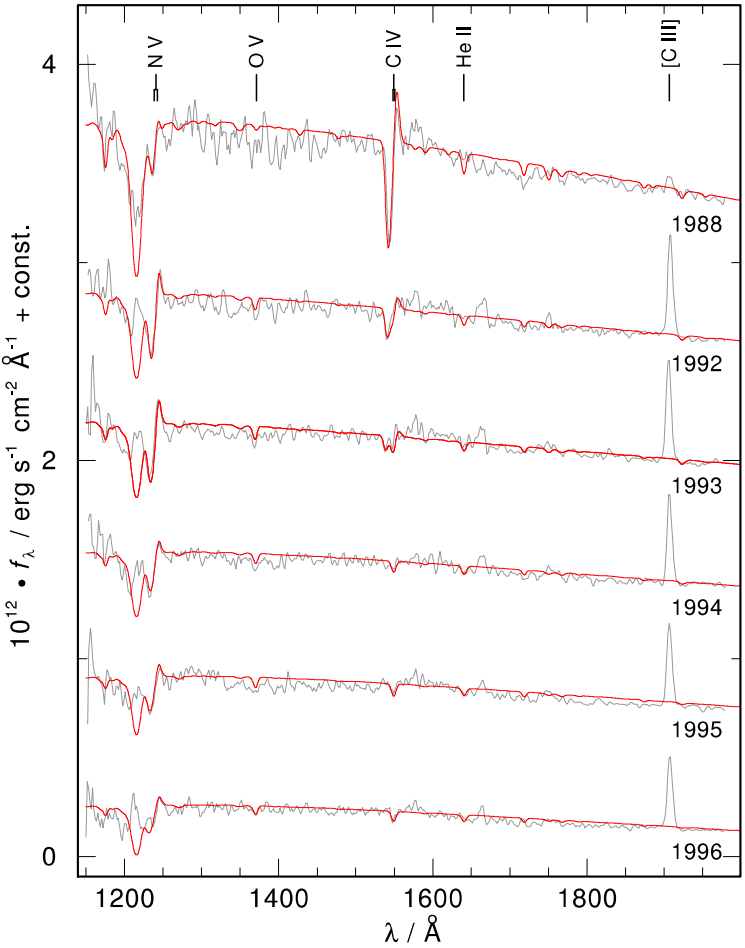

Figure 1.2.: Time series of UV spectra of the central star of the Stingray Nebula (black lines) compared to model atmosphere spectra (red lines). The decreasing strengths of the N V and C IV resonance lines indicate a decreasing stellar wind mass-loss rate. The observations were obtained with IUE (Section 1.2). Taken from Reindl et al. (2014).

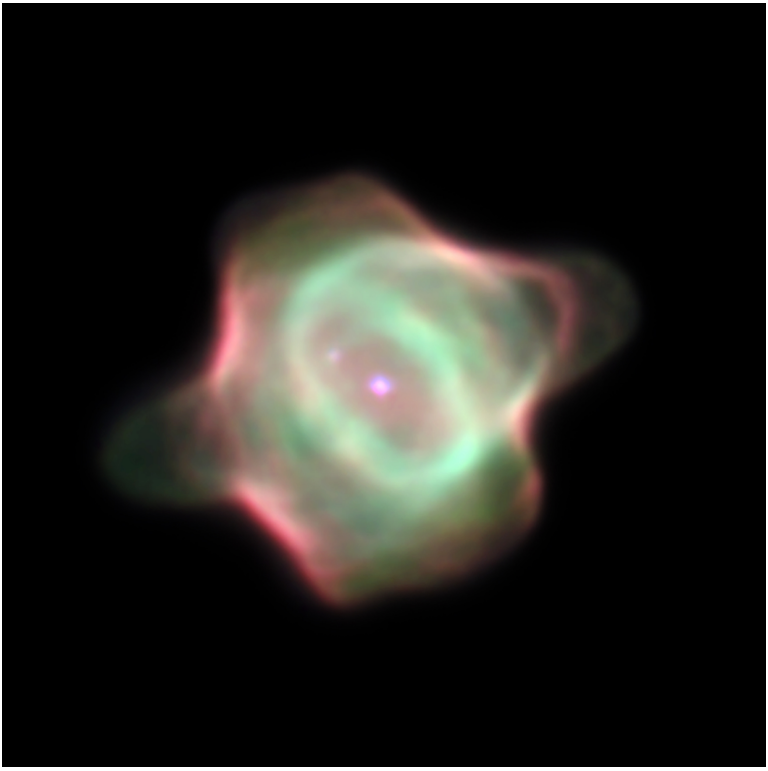

Figure 1.3.: Image of the Stingray Planetary Nebula (Hen-1357). The image was taken by the Wide Field and Planetary Camera 2 on board the Hubble Space Telescope. A bright central star (SAO 244 567) can be seen in the center of the image. The time evolution of its UV spectrum is shown in Figure 1.2. Gas bubbles expand to the lower left and upper right of the green ring. The red contours represent hot gas which is heated when the wind of the central star hits the walls of the bubbles. The colors indicate nitrogen (red), oxygen (green), and hydrogen (blue). The Stingray Nebula is the youngest known planetary nebula (Space Telescope Science Institute, 2014c).

Extrasolar planetary atmospheres and astrochemistry. In recent years, the field of exoplanetary research gained a large popularity among experts as well as the public. The reason for this is the fact that more and more planets in foreign star systems could be identified with increasingly powerful instruments. The research in this field revealed a large diversity in orbit-parameters, masses, atmospheric composition, and other planetary parameters. UV astronomy can contribute to this field of research as it provides powerful tools to astronomers. In particular, the footprint of absorption lines in the spectra of exoplanets that transit their host star are a powerful tool to explore the atmospheres of exoplanets and protoplanetary disks. In this context, insight into the shaping of planets and the impact of UV irradiation emitted by young stars onto the protoplanetary disks can be gained (Gómez de Castro et al., 2006a).

The process of planet formation in particular can not be investigated apart from other fields as for example the physics of the ISM and the physics of processes as accretion and outflow (Gómez de Castro et al., 2006b).

UV studies of the Solar System. The UV can also support the exploration of our cosmic vicinity. This field of science helped to understand the mechanisms that formed and still influence our home planet Earth. Studies of the atmospheres of Venus and Mars helped to understand the greenhouse effect and the consequences of the release of anthropogenic gases of which CO_2 is the most famous one. The strong greenhouse effect on Venus caused by CO_2 led to surface temperatures of up to 490 °C whereas a lack of a greenhouse effect on Mars has cooled its atmosphere to temperatures far below zero.

The composition of other planetary atmospheres in the Solar System besides the atmosphere of Earth indicates the origin of the planets, their unique evolution, and furthermore the evolution of the complete Solar System. The study of local atmospheric phenomena and the interaction of the atmospheres with the magnetic environment are further fields of interest.

Also the smaller bodies in the Solar System can be explored using UV radiation. In comets that originate from the outskirts of the Solar System, water dissociation products can be observed while the composition of the solid nucleus of comets is of further interest. In this context, the influx of

interstellar material into the Solar System may be important for planetary evolution in general.

Finally, planetary surfaces, the nuclei of the giant planets and the rings of planets can be explored by planetary mineralogy. This field can be expanded to the UV when it is supported by laboratory programs that characterize the possible minerals in the UV spectral region. As the transport of condensable gases is controlled by seasonable effects, a facility to monitor for example the rings of the giant planets in the UV could be installed (Brosch et al., 2006).

1.2. History and status of UV instruments and missions

This section shows the historic development of UV observations. An overview of past end present observatory missions is given and the instruments employed are introduced. As the UV radiation that is emitted from the various classes of sources in the Universe is blocked in the upper layers of Earth's atmosphere, UV observations were only possible as soon as technology to leave Earth's atmosphere was available (see Figure 1.4).

Rockets have been used as platforms that carried UV instruments to high altitudes in the beginning of observational UV astronomy in the late 1940s. A few hundred seconds of observational time were possible in this way. As the technology of satellites evolved afterward, longer observational periods per target were possible and far more targets could be observed with each instrument. Nowadays, satellites are the platforms that enable instruments to observe over years while rockets are used seldom and rather as a technology qualification platform.

At the time of this thesis, only a small number of UV instruments is in operation with limited observing capability or an only small remaining lifetime of the satellite that carries the instrument in the order of few years. New observatories and improved instruments are necessary to ensure that observational UV astronomy can contribute to deepen our understanding of the Universe in the future.

This section gives a brief overview of the history of scientific observations in the UV spectral band. An overview of the status of current instruments in orbit that are capable of UV observations is given. The last section of this chapter gives an outlook on candidates for future UV observatories.

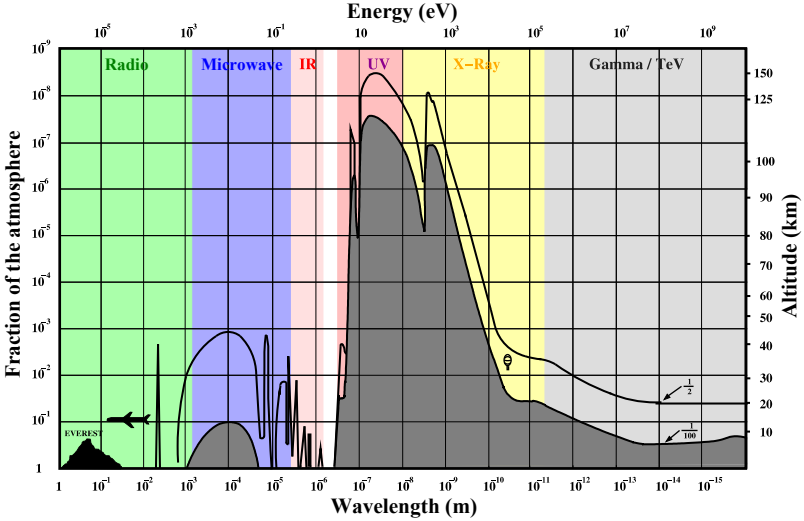

Figure 1.4.: Transmission of electromagnetic radiation of different wavelength bands in the atmosphere of the Earth. The Figure shows 50 % and 1 % transmission curves depending on the wavelength (energy) and the height above sea level (remaining fraction of Earth's atmosphere). More then 50 % of the original UV light from the Universe can be observed only at altitudes of more then 150 km above sea level. Reproduced by T. Schanz from Giacconi et al. (1968).

History of observational UV astronomy

Sounding rockets. In the late 1940s, first UV observations have been performed outside the atmosphere of Earth. The instruments had been installed on sounding rockets that did not have any guidance and stabilization and for this had a pure ballistic trajectory with a pointing that was arbitrary. The first UV instrument was flown by Hulburt und Tousey from the American Naval Research Laboratory on a German `V2` rocket. The observations that have been performed in the following years were UV photometric programs (Tousey, 1967; Wilson and Boksenberg, 1969).

The first spectrophotometric observations in the UV band have been performed by Stecher and Milligan (1962). They used a spectrometer that scanned the sky and was flown in a spin-stabilized but unguided `Aerobee` rocket. The peak altitude of the flight trajectory was 172 km. Scientific data was acquired in the wavelength range from 160 nm to 400 nm. The data suffered from an instrument anomaly during the first flight that was then absent in the following flights.

To be able to perform observations of specific regions of the sky and single objects, Morton and Spitzer (1966) used a cold-gas jet reaction system to orient the `Aerobee` rocket. Furthermore, they added a fine stabilization system which made an instrument stability of $\pm\ 20''$ and a spectral resolution of about 0.1 nm possible.

First satellites. To overcome the problem of a limited observation time and a small number of targets that could be observed per flight, the installation of UV instruments on satellites as soon as these were available was the logical consequence. The first UV instrument on board of a satellite was a photometer used by Smith (1967) in the unstabilized US satellite `1964 83C`.

The most important breakthrough in the technology to support scientific observations in the UV was a series of stabilized satellites of which Orbiting Astronomical Observatory-2 (OAO-2) `Stargazer` was the first successful one. Watts (1969) and Code et al. (1970) published first results from the experimental packages on board of OAO-2. First high-resolution UV-spectra were acquired on-board of OAO-3 `Copernicus` via the 80 cm primary mirror of the Princeton Experiment Package with a spectral resolution of 5×10^{-3} nm in the range between 95 nm and 145 nm (Rogerson et al., 1973; Snow, 1975).

IUE. The International Ultraviolet Explorer (IUE) was an astronomical satellite that was launched in 1978 and was a joint venture of ESA, NASA and UK. It provided the opportunity for guest observers to make real time observations which made IUE the first observatory type satellite in the current sense. IUE had an extraordinarily long operational time until 1996. During this 18 years of lifetime it returned more than 30 000 spectra of more than 9000 targets with a brightness range that spanned 10 orders of magnitudes. Two echelle spectrographs recorded spectra that have a resolution $R = \lambda/\Delta\lambda$ of up to 1.8×10^4 in the wavelength range between 115 nm and 320 nm. They were served by a 45 cm mirror (European Space Agency, 2014).

ORFEUS. Kappelmann et al. (1990) introduced the science that would be possible with the Orbiting Retrievable Far and Extreme Ultraviolet Spectrometers (ORFEUS) (Grewing et al., 1998; Space Telescope Science Institute, 2014d). This project was a follow-on project to a German/US collaboration where a 1 m telescope was flown on an American `ARIES` rocket (Grewing et al., 1981). Mandel et al. (1994) presented the first results of the ORFEUS instruments which have been a US Rowland and a German Echelle spectrograph. They were served by a 1 m telescope. The telescope and instruments were manufactured by Kayser-Threde GmbH (now: OHB System AG). The instruments were integrated into the retrievable free-flying platform ASTRO-SPAS. ASTRO-SPAS was built by Messerschmitt-Bölkow-Blohm (now a part of EADS) and was managed by the DARA (Deutsche Agentur für Raumfahrtangelegenheiten, today: DLR, German for: German Aerospace Center). It was launched into orbit four times, of which ORFEUS was on-board for two flights.

On each flight, ASTRO-SPAS was transported into its orbit by the Orbiter of the Space Shuttle Transport System (STS)[2] and then deployed into space via the robotic arm of the Orbiter. After a free flight mission phase of up to 14 days, it was retrieved by the shuttle crew and brought back to the Earth. The free-flight of ORFEUS mission I in the year 1993 (STS mission 51) lasted 6 days. During this flight, ORFEUS recorded more than 100 stellar spectra in the range 39 nm-120 nm via the US

[2] Also known as NASA's manned Space Shuttle Program. It lasted from 1981 to 2011. The Space Shuttle Orbiter could carry four to seven astronauts and launched vertically attached to an external tank and solid boosters. 135 missions have been flown of which two have been lost in 1986 and 2003.

spectrometers. The second flight of ORFEUS was part of Space Shuttle Orbiter `Columbia`'s mission STS-80 in 1996 and the free-flight phase of ORFEUS-SPAS II lasted 14 days (Figure 1.5). The spectral range of the German FUV Tübingen Echelle Spectrograph was 90 nm-140 nm with a resolution R of better than 10 000 during the second flight (Barnstedt et al., 1999). See Section 2.2.1 for details on the wedge and strip anode micro channel plate detectors that have been designed and built in Tübingen for the FUV channel of ORFEUS.

FUSE. Following ORFEUS, among others, Far Ultraviolet Spectroscopic Explorer (FUSE) was a further scientific satellite that was on a permanent orbit. FUSE acquired high-resolution ($R = 20\,000$) spectra in the far-UV band from 91 nm to 118 nm. It used four mirror segments instead of one where two mirrors each were coated to operate in a defined bandpass. Siegmund et al. (1994, 1997) at the Space Science Laboratory of the University of California in Berkeley developed the delay line micro channel plate detectors that had been used in the spectrographs on board of FUSE (see Section 2.2.2 for details on the detectors). After the launch of the satellite in 1999, FUSE performed more than 6000 observations. FUSE was decommissioned in 2007 after the failure of the pointing-system of the satellite bus (Moos et al., 2000; Kaiser and Kruk, 2009; Space Telescope Science Institute, 2014a).

GALEX. Launched in April 2003 on a `Pegasus` rocket, the Galaxy Evolution Explorer (GALEX) was a sky survey satellite that performed the first UV all-sky survey beyond our Galaxy in two bands (135 nm-175 nm and 175 nm-275 nm) with a primary mirror of 50 cm. The surveys of GALEX were different in the amount of sky coverage and exposure time for a single pointing. The latter one included also the focusing on single nearby galaxies. During the baseline mission as well as during the legacy surveys that have been performed after the extension of the mission lifetime in 2006, low-resolution ($R = 100$-200) spectroscopic surveys have been performed besides the imaging surveys as well. Figure 1.1 in the previous section shows the distribution of UV sources that have been identified by GALEX. GALEX was decommissioned in June 2013 (Martin et al., 2005; Morrissey et al., 2005; GALEX science team at California Institute of Technology, 2014).

Figure 1.5.: ORFEUS-SPAS II at the arm of the orbiter of STS-80. The Tübingen Echelle Spectrometer is attached to the 1 m ORFEUS telescope in the center of the platform ASTRO-SPAS. On the right side of the platform, the Interstellar Matter Absorption Profile Spectrograph (IMAPS) of the Princeton University is mounted. Photograph from IAAT archive.

Current instruments that perform observations in the UV

HST. The Hubble Space Telescope (HST) is a joint mission of ESA and NASA. Its primary mirror has a diameter of 2.4 m. In April 1990, HST was deployed by the crew of the Space Shuttle Mission STS-31. It was maintained by the crews of five further Space Shuttle servicing missions in the years from 1993 to 2003. Currently, HST carries six scientific instruments whose observation capability spans a wavelength range from the UV to the infrared. These instruments are three spectrographs, two imaging cameras and the fine guidance sensors that can be used for astrometry as well. The Space Telescope Imaging Spectrograph (STIS) is able to perform two-dimensional spectroscopy in the range from 105 nm to 1000 nm and has a camera mode furthermore. It was installed on the 10-day second servicing mission (STS-82) in 1997. In 2004, the power supply of STIS failed and there was no UV instrument available at all until a third servicing mission in 2009 when STIS was repaired. During this mission (STS-125), the Cosmic Origins Spectrograph (COS) was installed on HST as an additional instrument. Its purpose are spectrographic observations of faint objects that are possible due to the high sensitivity of COS. COS can perform moderate and low-resolution spectroscopy in the range from 115 to 320 nm (Space Telescope Science Institute, 2014b).

OM und UVOT. Besides the instruments on HST there are, at the moment, only two more, though very similar, space-based instruments in operation that have the capability to perform UV observations: the Optical and UV Monitor (OM) on-board the XMM-Newton X-ray observatory (Mason et al., 2001; Talavera, 2009) and the Ultra-Violet/Optical Telescope (UVOT) on-board the Swift Gamma-Ray Burst Mission (Roming et al., 2005; Roming et al., 2009). Both telescopes have a 30 cm aperture and a spectral response from 180 nm to 600 nm and 160 nm to 800 nm, respectively. However, OM has a higher spatial resolution while UVOT has a higher throughput. Due to the fact that these instruments are co-aligned to the main instruments of their host observatory, their purpose is in general to expand the wavelength coverage of the observations that are performed by the particular main instrument. Hence, they are no true alternative to the instruments that are installed on space observatories that are intended for observations in the UV range specifically. In addition, they have a small aperture and a missing capability to cover the FUV.

1.3. Observational UV astronomy in the next decade

After a shutdown of the HST around the year 2020 at the latest, new UV space astronomy missions are required urgently. In any case, the community of UV astronomers is facing years and possibly even decades where no adequate scientific instruments for observations in the UV wavelength band are available. In this section, an overview of the general requirements for future UV observatories that have been expressed by several members of the UV community is given. A brief look on the applicability of alternatives to UV satellite observatories is also taken. After that, a selection of proposed future UV observatories is illustrated. Finally, the World Space Observatory UltraViolet (WSO-UV) is described in more detail as one of the most promising candidates for a future access to observations in the UV with a launch scheduled for 2019 (Sachkov et al., 2014a, Talk at conference).

Requirements for future UV instruments and missions

Throughput is the most important technology driver for observational astronomy and for UV astronomy in particular to raise the signal statistics of observations. This implies improvements in the fields of detector area, optical components and and their coatings as well as in the development of big light-weight mirrors (Kappelmann and Barnstedt, 2006).

Solar blind detectors and solar blind imaging systems in general are required to reduce the huge background in the optical wavelengths that are emitted by many astronomical objects. See Section 2.1 for more details on UV sensors and photocathodes.

Requirements for the performance of future space-borne instruments depend on the specific science case. Kappelmann and Barnstedt (2006) summarize that most of the current science questions can be faced by a 3 m-4 m class telescope and two types of spectrographs with high throughput. These two spectrograph types are:

1. A spectrograph with high spectral resolution of $R = \lambda/\Delta\lambda$ between 50 000 and 100 000 in the wavelength range of 90 nm to 350 nm

2. A spectrograph with medium spectral resolution ($R \sim 1000$ to 5000) that is capable to perform integral field spectroscopy with a spatial resolution of $\sim 0.01''$ and a wavelength coverage of 90 nm to 450 nm

Alternative approaches to space UV observatories

Modern astronomy requires space-borne instruments to meet scientific requirements. These observatories are rather expensive and require long phases of design and planning. There are several suggestions of UV observational locations different than the low Earth orbit that is usual for UV satellite observatories. On this locations, observatories could possibly be realized significantly cheaper on the first glance. Brosch (2009) analyzed Antarctic astronomy, balloon-borne UV astronomy, and moon-based UV observations. He concluded that there is no true alternative to space observatories in the future.

UV space observatories announced for the near future

Only a small number of missions is proposed at the moment that will be capable to perform observations in the UV during the next decade. After a failure of HST, the community of UV astronomers might face an age of observational darkness if the international community will not be successful to initiate a further mission. Two selected proposals for future UV observatories are presented in the following as examples. Though, the only UV satellite that is in the implementation phase at all is the Russian-led WSO-UV mission. It is discussed in more detail in the next section.

`ASTROSAT` is the first satellite of India's Space Research Organization (ISRO) that is dedicated to astronomy. It will carry several payloads. The UltraViolet Imaging Telescope (UVIT) is one of them. It is a twin 38 cm-aperture UV instrument and will perform simultaneous imaging in the range from 130 nm to 300 nm in two ultraviolet channels and one optical channel in the wavelength range from 320 nm to 530 nm with an angular resolution of up to $1.8''$. The launch of `ASTROSAT` is scheduled for 2015 (Inter-University Centre for Astronomy and Astrophysics, 2012; Hindu, 2014).

The Canadian Space Agency (CSA) proposed a UV/optical space telescope that is called `CASTOR`. The 1 m primary mirror of `CASTOR` would provide nearly diffraction-limited imaging in a field of view that is a factor 200 larger than that of ACS or WFC3 on HST. The focal plane is divided into three sections for a broad UV band from 150 to 300 nm and two blue-optical bands (Côte et al., 2012; Côte and Scott, 2014).

The World Space Observatory-Ultraviolet (WSO-UV)

The World Space Observatory-Ultraviolet is the most promising candidate for a 2 m-class space UV telescope in the next decade (Sachkov et al., 2014b; INASAN, 2014)

WSO-UV is a cooperation of an international consortium that is led by the Federal Space Agency of Russia (ROSCOSMOS). The mission and scientific operations will be coordinated by Russia and Spain. The science program is planned to comprise a core scientific program, an open program for projects from the international community, and a funding bodies program for the partners in the project consortium. The nominal lifetime is planned to be 5 years with an optional extension to 10 years.

The satellite bus is the Russian NAVIGATOR platform that was used already for the radio satellite `Spektrum-R`[3] and will be used for `Spektrum-RG`[4], a high-energy astrophysics observatory satellite, as well. The satellite bus of WSO-UV will carry a 1.7 m-aperture telescope (see the model in Figure 1.6) and instruments to carry out high resolution and long-slit low resolution spectroscopy as well as imaging. WSO-UV will be launched from Baikonur (Kazakhstan) in 2019 (Sachkov et al., 2014a, Talk at conference).

WSO-UV will carry three scientific instruments:

- A far UV high resolution echelle spectrograph with a resolution of $R \sim 50\,000$ in the range between 115 nm and 176 nm
- A near UV high resolution echelle spectrograph with a resolution of $R \sim 50\,000$ in the range between 174 nm and 310 nm
- A long slit spectrograph to perform long slit spectroscopy with a low resolution of $R \sim 10\,000$ in the 115 nm-305 nm band and a spatial resolution of $0.5''$

The original design for the spectrographs was performed by Kappelmann et al. (1995, 2006); Kappelmann et al. (2009); Hermanutz et al. (2012). This design, called the High Resolution Double Echelle Spectrograph

[3] Also called `Radioastron`. Russian satellite observatory to perform observations for radio astronomy. It was launched in July 2011 (RadioAstron Science and Technical Operations Group, 2014).

[4] International high-energy astrophysics satellite under Russian leadership. The launch is scheduled currently for 2016.

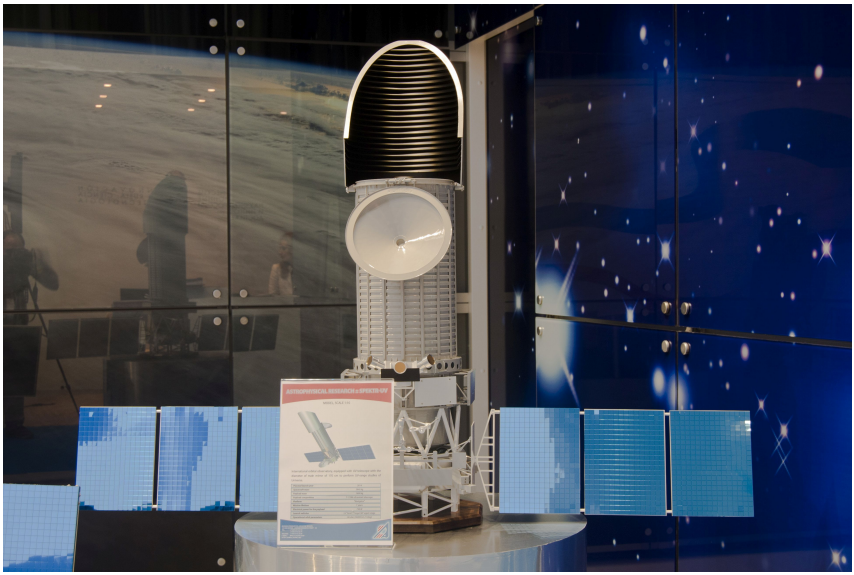

Figure 1.6.: A model of the WSO-UV telescope exhibited during "Space Week" in Madrid (Kolotilov, 2011).

(HIRDES), incorporated micro channel plate detectors (see next chapter) manufactured at IAAT in the instrument. Meanwhile, it is planned to equip the spectrographs on WSO-UV with cooled CCDs (Shugarov et al., 2014).

The imagers are a multi-purpose instrument to carry out imaging and slitless spectroscopy. This instrument will be equipped with two micro channel plate detectors that employ CsI and CsTe photocathodes (see 2.1).

2. Micro channel plate UV detectors

After a look onto UV astronomy in general as well as on the history and status of UV instruments, this chapter focuses on certain UV detector technologies that are applied in the scientific instruments.

In a scientific instrument, the detector determines the feasibility of certain astronomical research projects for a given aperture.The improvement of existing technologies and the establishment of new detector techniques is the main focus of hardware research in UV astronomy.

A variety of detector types and technology is available to detect UV radiation. It's goal is to convert the UV radiation into electrical signals that are processed, stored, and sent to ground for further scientific exploration. Each detector type consists of a specific combination of certain technologies. This chapter will give a brief overview of advantages and disadvantages of certain UV technologies.

At the Institute for Astronomy and Astrophysics Tübingen (IAAT), research on one detector type, called a micro channel plate (MCP) UV detector, in combination with a cross strip anode readout, is conducted. MCP UV detectors have a history of successful applications in several observatory programs in the past. The research on MCP detectors at the IAAT is based on the heritage from detector contributions to missions on `ARIES` rockets and in the German instrument of ORFEUS. Photocathodes are at the focus of research as a means to raise the efficiency of the photon detection process. A cross strip anode readout is an innovation to raise the spatial resolution and the lifetime of a micro channel plate detector.

An overview of the UV detection technology that is available is given in the first section of this chapter. Examples where MCP detectors have been applied successfully in the past as well as details on the development of a cross strip anode MCP detector which inspired the current development at IAAT are given in the second section of this chapter. The next chapter describes the current research on MCP detectors at the IAAT.

2.1. Overview of UV detection technology

As far as not stated otherwise, the general information in this section is taken from Joseph (1995, 2000).

General characteristics of UV detectors

A detector that is intended to be used in a UV instrument has to be composed carefully. Usually, a compromise between several properties is necessary in the context of the scientific requirements that are defined for the overall instrument configuration. In general, there are five properties that a UV detector should have (Joseph, 1995):

- The detector should be solar blind
- High detective quantum efficiency (DQE)
- High local dynamic range (LDR) or global dynamic range (GDR) depending on the specific scene that is recorded
- Low intrinsic background and an insensitivity to external background sources
- Large multiplexing capability (i.e. a large number of pixels) to realize a sufficient spatial resolution for imaging applications or a sufficient spectral resolution in spectroscopy

Solar blindness is the property that the detector should not be sensitive to photons at optical wavelengths that are emitted from many astronomical objects besides the UV radiation. Often, astronomical sources of interest for UV astronomy radiate more of their flux in the optical wavelength range than they do in the UV. Hence, if the detector would be sensitive in the optical, this would cause a huge background in the scientific data and bring the detector operational point closer to the limits of its dynamic range.

The **detective quantum efficiency** means the total photon detection efficiency of a detector system. This includes for example the losses due to absorption of the UV radiation in an entrance window or losses due to the dead-time of a readout electronics.

The **local dynamic range** is defined as the maximum flux level in a narrow area of a detector minus the faintest level that is three standard

deviations above the background in acceptable integration times (Joseph, 1995).

In most astronomical imaging applications the light is concentrated in a few pixels on a detector or the sources are generally faint. Hence, the **global dynamic range** is less important for these applications. The GDR which is the maximum flux rate spread over the whole detector area is of greater interest in the cases where for example echelle spectra of bright hot stars are observed.

Detector **background sources** create events in the detector besides the radiation from the object that is observed. The background sources include internal detector dark events (e.g. caused by radioactive contaminations) and external background sources (e.g. Cherenkov radiation produced by cosmic rays).

Classes of UV detection devices

The detection devices that are of interest for astronomical observations in the UV can be sorted into two classes:

- Photoemissive devices: a photon releases an electron from the device's material. Photoemissive devices are for this photon counting. Examples are micro channel plate detectors or electron-bombarded CCDs (see below). The energy to release an electron is a few eV. Hence, photoemissive devices are natural UV detectors and are inherently solar blind. They have negligible background rates at room temperatures below $0.1\,\mathrm{counts/cm^2/s}$. However, an amplification mechanism to multiply a single photoelectron to a charge amount that is sufficient for further processing is usually necessary.

- Photoconductive devices: a photon causes an electron to transit into the conduction band of the material of the device. Silicon-based CCDs are an example for these devices. In general, they are integrating photon events except for X-ray applications. The excitation energy is in the order of one eV. Photoconductive devices are for this natural detectors for optical and near-infrared radiation and are obviously not solar blind. Furthermore, usual photoconductive devices are sensitive to thermally induced backgrounds and require cooling.

2.1.1. Micro channel plate based photoemissive detectors

Micro channel plate (MCP) based detectors are the most successful type of UV detectors. A subtype that employs a cross strip anode (XSA) readout is of special interest here. This section presents details on the operation principle of MCP detectors. Micro channel plates, photocathodes, and readout schemes are introduced as well. Three examples for the realization of the MCP detector principle are described in Section 2.2 of this chapter. Chapter 3 shows the design of a cross strip anode MCP detector that is realized in Tübingen.

Operation principle. A micro channel plate detector consists of several components that act as a system to multiply an electron that is released by an incoming photon due to the photoelectric effect (see Figure 2.1).

The central element in the detector is the MCP that is a thin disk made in most cases of lead-oxide glass which contains hundreds of microscopic channels with a diameter and a distance of several micrometers (see Figure 3.2 for a photograph of the MCPs used at IAAT). The multiplication is performed in the channels of the micro channel plate where several electrons are released by each electron that hits one of the walls of the channels. Usually, a stack of two or more MCPs is used to realize a certain gain. A high voltage in the order of 1 kV for each MCP in the stack is applied from one face of the MCP stack to the rear side of the stack to accelerate the electrons in the channels. An electron avalanche leaves the MCPs.

The original electron usually is released by the incoming photon in a photocathode that is either deposited directly on top of the MCP stack or on the back side of a window in front of the MCPs. The photocathode is deposited to raise the probability of the photo effect but is not crucial for the operation of a MCP detector since electrons can be released off the surface of MCPs as well. The quantum efficiency for this process is small (2 % at 120 nm and 10^{-9} at 260 nm (Paresce, 1975)) nevertheless.

The electron cloud that leaves the MCP stack at its rear side can be deposited either onto an anode configuration or a solid state device to detect it. A readout electronics has to detect the charge information that is determined in this way.

A further digital processing in the electronics usually has the task to determine the center of mass of the charge distribution and hence the

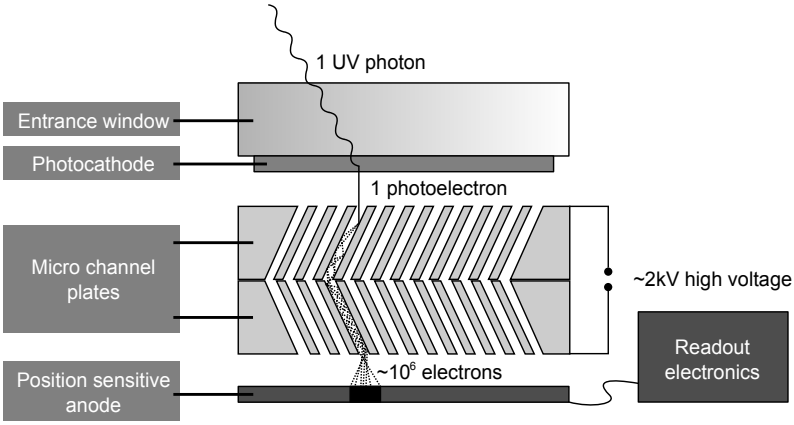

Figure 2.1.: The architecture and operational principle of a micro channel plate detector.

center of the cloud. The cloud center corresponds to the position where the original photon hit the detector's active area in certain limits which are given by the channel bias angle and spacing, or distortions of the electric field of the high voltage at the edges of the MCPs.

In the following, several possible realization examples for photocathodes, micro channel plates, and readout anodes as well as their properties are described briefly.

Photocathodes

Photocathodes are used to convert photons into electrons. Different materials are used depending on the specific application (HAMAMATSU, 1997, Chapter 4). The bandgap of the photocathode material is the key parameter that determines the spectral range where the cathode operates most efficient. Usually, the operating spectral range has a sharp sensitivity cutoff (see the Figures 2.2, 2.3, and 2.4 below). In addition to an appropriate bandgap of the material, it should allow for a good electron transport to the emission surface and furthermore have a low or negative electron affinity to allow the electron that is released in the conversion process to escape from the photocathode material (Tremsin and Siegmund, 2005).

For astronomical applications, the out-of-bandpass rejection is yet another important parameter of the photocathode material. This means that the quantum efficiency should be as low as possible in the region below and above the spectral band for which the photocathode is intended. Especially the rejection of visible light is very important for instruments on satellites. For the example of UV instrumentation, stray-light from the sun is not easy to suppress. In scenarios where the intensity of the incident radiation is quite high, e.g. when performing observations of the Sun, the stability of the photocathode under intense radiation is more important than a good conversion efficiency.

Most of the photocathode materials require an operation in high vacuum conditions since their efficiency degrades substantially even under short atmospheric exposure. This implies some issues on production of the cathodes and handling during their integration into the detector assembly when selecting the proper material for the photocathode. In some photon counting applications, thermionic electron emission may be a final parameter that requires active cooling of the cathode to reduce the dark noise contribution of the cathode.

Photon conversion process. The process that ejects an electron from the photocathode surface when a photon is absorbed can be described as follows. The photon is absorbed in the photocathode and excites an electron, referred to as photoelectron, into the conduction band. For this, the energy of the photon must be larger then the bandgap energy of the photocathode material. The photoelectron produced in the inner volume of the material must be able to travel to the emission surface without being reabsorbed. The electron transport properties depend on the specific material structure and on the presence of impurities and defects that act as absorption centers and should be reduced to a minimum during the manufacturing process. When the photoelectron finally reaches the surface of the material, it must have more energy than electrons in the vacuum have. This negative electron affinity has often to be established by a treatment of the surface of the photocathode material to activate it. Usually, a doping of the material via Cs on top of a photocathode lowers the escape energy for photoelectrons off the surface.

In addition to the photon absorption and electron transport properties as well as the surface states of the photocathode material, the thickness of

the cathode film on a carrier substrate is another important parameter that contributes to the conversion efficiency of a photocathode. The photon absorption probability increases with the photocathode film thickness while the probability of the transport of the electron to the emission surface decreases for a given wavelength of the photon to be converted. The optimum thickness for a given photocathode thus also has to be adjusted to the expected wavelength of the incoming photons.

The conversion efficiency of a photocathode usually is higher in the opaque mode where photons and electrons enter and leave at the same face of the photocathode than in the semitransparent mode where the electrons leave the photocathode at the opposite face of the cathode with respect to the incident photons. Despite this fact, when selecting a photocathode configuration, the semitransparent mode has to be favored for a given combination of a photocathode material and a carrier substrate. This is because since some cathode materials require high substrate temperature during their fabrication they can for example not been grown directly onto the surface of glass MCPs or other electron multiplying elements that are not rated for high temperatures.

Alkali halide photocathodes. Several alkali halide photocathodes have successfully been flown in space based instruments. The materials of this photocathode family are for example KBr, CsI, CsTe, and others. They are used due to their high efficiency that has its origin in good electron transport and surface emission properties, but also because their manufacturing is relatively easy. These photocathodes are typically manufactured by evaporation of high-purity powder under vacuum conditions. The result is a polycrystalline film that has sub-micrometer granular structure. The high bandgap of these materials makes them solar blind. KBr becomes sensitive to these wavelengths under prolonged exposure to high-intensity UV radiation which is restored after a short exposure to only visible light.

The quantum efficiency of alkali halide photocathodes (Figure 2.2) is different for example in the case of CsI and CsTe (Tremsin and Siegmund, 2005; Siegmund et al., 2008). The long-wavelength cut-off of CsI is at about 180 nm while it reaches an efficiency of about 40 % at 100 nm. For the case of CsTe, the peak quantum efficiency of below 20 % is located at 200 nm and drops to zero at $\approx$ 300 nm.

Alkali halide photocathodes are stable only under short air exposure.

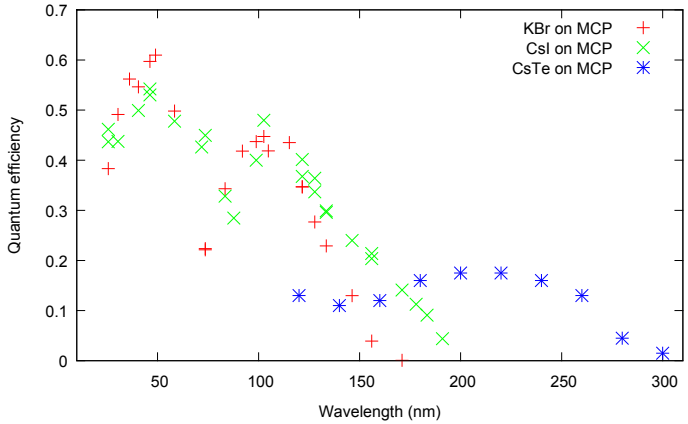

Figure 2.2.: Quantum efficiency of selected alkali halide photocathodes plotted against the wavelength of the incident photons. The photocathodes are deposited on MCPs. Data from Tremsin and Siegmund (2005).

The degradation of the performance under air conditions is caused by the sensitivity of the photocathodes to moisture. In the case of alkali halide photocathodes, the moisture is absorbed and forms a solution of the photocathode material. In extreme cases, when the water evaporates again, the film becomes completely discontinuous and leaves large crystal clusters on the surface of the substrate. CsI for example is, in contrary, not very hygroscopic and thus can sustain moderate exposures to air in the order of 10 minutes when it is transferred and installed into the final detection device. KBr can even withstand exposures up to 1 hour.

Diamond photocathodes. Despite the fact that diamond photocathodes are less efficient than other photocathode materials, diamond films have some features in favor of other cathode films. These features are radiation hardness, the chemical and mechanical stability under harsh environmental conditions and a very efficient heat dissipation. Diamond is thus attractive where efficiency can be sacrificed to stability. Diamond photocathodes are solar blind.

Chemical vapor deposition is applied to grow thin films of diamond. Other deposition techniques allow to grow diamond films on non-diamond substrates in a polycrystalline form and even on structured substrates as for example MCPs.

After the deposition of the diamond film, a surface treatment, often in form of a cesiation, is performed to achieve the smallest electron affinity and hence the best quantum efficiency. To avoid the necessity of the cathode processing under vacuum conditions for the case of surface activation by cesiation, other forms of surface treatment can be used. These are for example the activation by hydrogen in a hydrogen microwave plasma or the deposition of quasi monolithic layers of LiF. Hydrogenated diamond surfaces can withstand air exposures of several hours without much degradation (cf. Figure 2.3). Furthermore, the efficiency of these surfaces can be restored by moderate heating in vacuum after the exposition to water vapor.

The quantum efficiency of diamond in the opaque mode has its peak value in the order of 20 % at around 50 nm with a long wavelength drop at around 150 nm or at 200 nm when the surface is hydrogenated.

GaN photocathodes. The efficiency and bandwidth of the spectral sensitivity of GaN is better than that of the other materials mentioned above. The long wavelength cutoff furthermore can be tuned for GaN. GaN photocathodes are grown for example by molecular beam epitaxy on substrates that have a matching lattice as for example sapphire or silicon carbide. When the lattice of the substrate is not matching that of GaN, the quantum efficiency is typically reduced about a factor of 10 % though still significant and in particular higher than for CsI at wavelengths above 150 nm. GaN has to be processed and activated by Cs and oxygen under very high vacuum conditions. Nevertheless, after the exposure to air or nitrogen, the QE of GaN can be mostly recovered by vacuum bake out and fully restored by a subsequent cesiation of the cathode if necessary. The long term stability over several years in an evacuated sealed tube was shown (Siegmund et al., 2008).

In contrary to the other cathode materials, the spectral response of GaN is very broad expanding from the FUV up to a steep drop at around 380 nm. Opaque GaN photocathode configurations have shown quantum efficiencies of up to 70 % at 120 nm, though efficiencies of semitransparent

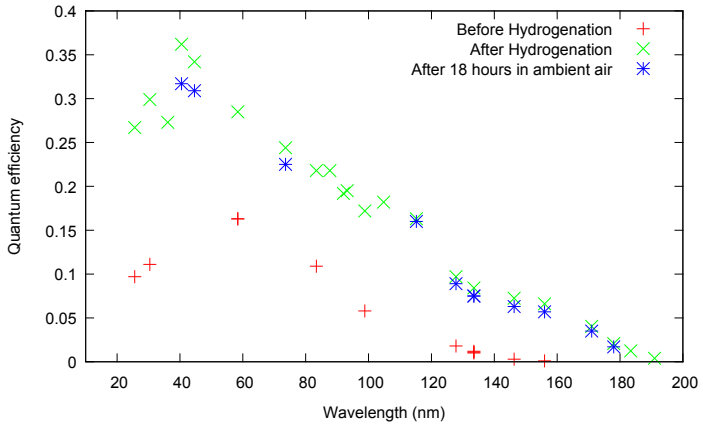

Figure 2.3.: Quantum efficiency of diamond photocathodes plotted against the wavelength of the incident photons, before and after the activation via hydrogen as well as after 18 hours exposed to air. Normal incidence on a planar Si substrate. Data from Tremsin and Siegmund (2005).

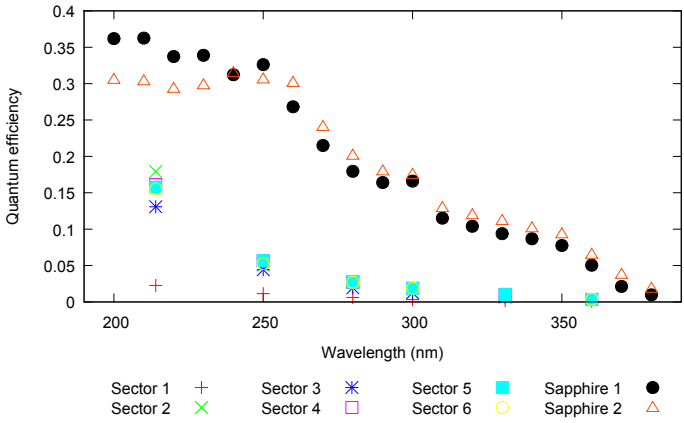

Figure 2.4.: Quantum efficiency of opaque GaN photocathodes plotted against the wavelength of the incident photons. Data from Tremsin et al. (2013). They deposited different layer configurations on six sectors of one MCP on top of a Al_2O_3 layer. The Al_2O_3 layer is intended as a reflection barrier for the photoelectrons that travel towards the MCP. Sector 1 carries only the Al_2O_3 layer. All sectors were backed as well as cesiated. For comparison, data of opaque GaN on planar Sapphire substrates is shown.

configurations are substantially reduced to typically 4 % but quantum efficiencies of up to 20 % have been reported for thinner layers. The efficiency in the semitransparent mode depends on the layer thickness of the photocathode on top of the substrate. A thinner layer performs less attenuation of light for the advantage of a higher escape probability for photoelectrons (Siegmund et al., 2008).

Tremsin et al. (2013) showed the production of opaque GaN on novel MCPs that can withstand higher processing temperatures (see Figure 2.4). The photocathodes have been baked and activated with cesium afterward. The quantum efficiency of opaque GaN on MCPs is reduced compared to opaque GaN on planar substrates due to the reduced area ratio.

Micro channel plates

The central component of a MCP detector is a stack of micro channel plates. These are plates typically made of a high resistive material as lead oxide glass into which small channels are etched. The channel diameter is typically between 4 µm and 25 µm while the centers of the pores are spaced a few µm more then the pore diameter itself. The channels are usually inclined around 10° with respect to the surface (HAMAMATSU, 2013).

One technique to manufacture lead oxide glass MCPs is the so called etchable core technique (Wiza (1979) and Fraser (1989, Chapter 3)). It is shown in Figure 2.5: the raw material for this technique are drawn fibers of hollow billets of lead oxide glass which are supported by a rod of core glass that can be etched away later. Many of these solid rods are stacked to a hexagonal structure and drawn again to a hexagonal multi-fiber. These are stacked subsequently and fused into a glass envelope to form a boule. The boule is then sliced at a small bias angle with respect to the channel axis. The slices are polished to thin plates and the solid core of the channels is then removed by means of chemical etching. After further processing, the plates are reduced in a hydrogen furnace to enhance the secondary electron emissivity. There, the lead oxide at the glass surface is converted into semiconducting lead. Electrodes are deposited onto the polished faces of the plate in the end of the manufacturing process.

An alternative to the standard lead glass MCPs are silicon based MCPs (Si MCPs). Siegmund et al. (2000, 2002) tested samples with either square or hexagonal pore shape. Si MCPs are manufactured using a Si photolithographic micro-machining process. The channel thickness and spacing are selected using a photolithographic mask, 7 µm and 8 µm have been realized resulting in open area ratios of more than 75 %. The major advantage of Si MCPs is that, since Si can withstand much higher temperatures than glass MCPs, materials with high resiliency and high photoelectron emission probability such as e.g. diamond and aluminum nitride can be deposited on the MCP. Tested samples achieved DQEs close to the values achieved for high DQE glass MCPs in the EUV range. The gain curves of Si MCPs are close to those measured with equivalent glass MCPs.

Franco et al. (2014) showed the production of amorphous-silicon-based microchannel plates that can be vertically integrated directly onto specialized readout chips or solid-state detectors.

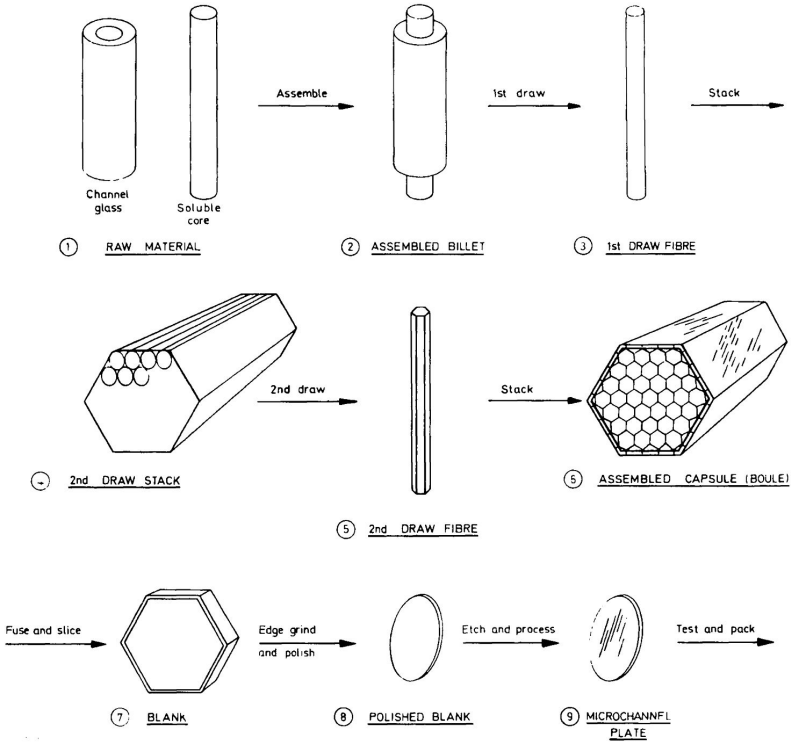

Figure 2.5.: The micro channel plate manufacturing process via the etchable core technique (Fraser, 1989, Chapter 3).

Anode readout layouts

The charge cloud that leaves the MCPs after the multiplication of the initial photoelectron that was released by the original photon must be detected and its position must be encoded. This is done by means of different possible anode readout schemes that encode the position of the charge cloud which leaves the MCP stack. In this way, the reconstruction of the position where the incident photon hit the detector surface is possible. Three general subtypes of MCP detector readout schemes have been used so far: continuous and discrete anodes as well as pixellated readouts.

Continuous anodes. The first concepts for MCP detector readouts have been continuous anodes due to their easy manufacturing and handling. Barstow et al. (1986) used a single resistive anode and the charge cloud position was encoded in the amount of charge that was divided between amplifiers that have been attached to the corners of the anode. Wedge and strip anodes (WSA) have been introduced by Martin et al. (1981) and used by Barnstedt et al. (1999) for example in ORFEUS. They allow to physically divide the charge of an electron cloud between four electrodes that are shaped in a pattern of wedges and strips (see Figure 2.6) (Barnstedt, 1985).

Crossed delay line and double delay line anodes are a further type of continuous anodes. The latter one uses the physical charge division for one coordinate as well as charge signal propagation timing for the second coordinate of the detector plane. Siegmund et al. (1997) and Sahnow et al. (2000) applied a helical double delay line anode in the MCP detectors on board of the FUSE satellite (see 2.2.2) and in ORFEUS (see Figure 2.7).

All of these continuous readouts have in common that they have only a small number of electrodes and for this need only a small number of amplifiers or timing analyzers. The spatial resolution is moderate in the order of 20 µm for a relatively high MCP gain of approximately 10^7 in case of the cross delay line anode (Vallerga et al., 2009).

Discrete anodes. As soon as low noise and lower power Application-Specific Integrated Circuits (ASICs) came available, the anode area could be divided into electrodes that are smaller and independent of each others. Each was attached to a single preamplifier and digitization chain. Due to this concept, the capacitance of the electrodes and hence also the noise is decreased. The sacrifice is a more complex and power consuming readout

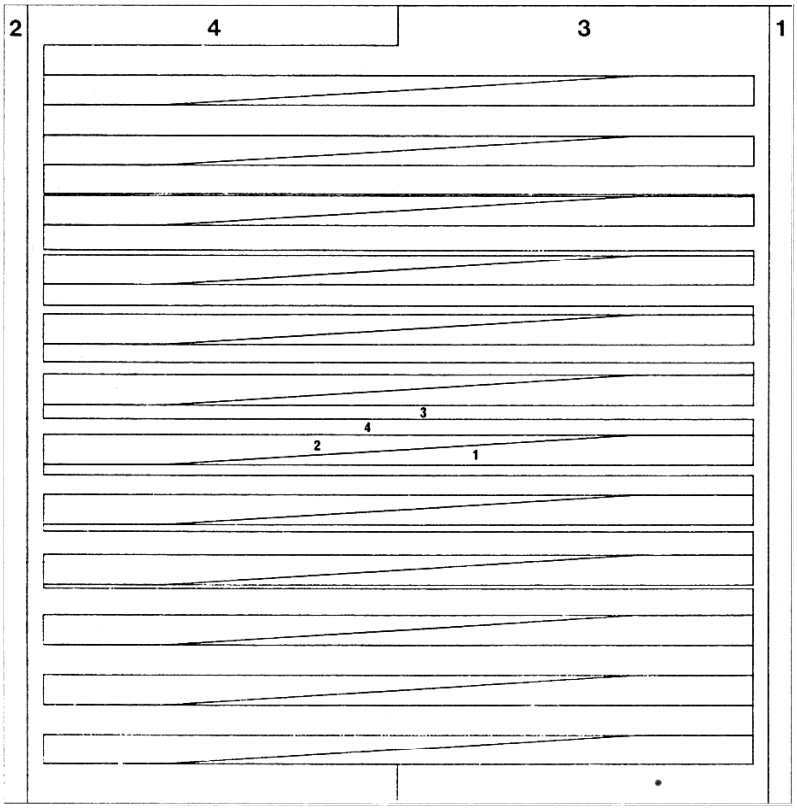

Figure 2.6.: Illustration of the geometry of a wedge and strip anode. The four electrodes are not to scale with respect to the anode total area (Barnstedt, 1985).

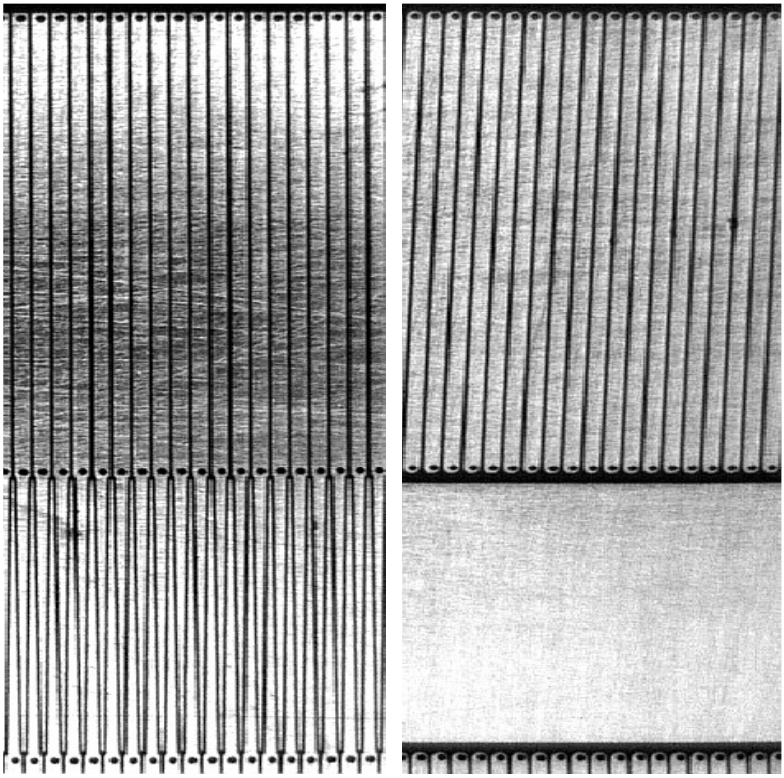

Figure 2.7.: Photograph of the top side (left) and bottom side (right) of a section of a helical double delay line anode. On top, one side of the delay line can be seen, the bottom shows the interleaved wedges in the active area of the anode. Taken from Siegmund et al. (1997).

due to an enhanced number of necessary ASICs. However, the operational gain of the MCPs can be lower and their lifetime is enhanced. The power dissipation of the readout is at the focus of investigation since it has to meet the limits that are given by instrument and satellite designs. The *coded anode converter*, the *multi-anode microchannel array* that is applied in STIS on HST (Timothy, 1991a,b, 1997), and the *vernier anode* (Lapington, 2004) are examples for the discrete anode type.

The most prominent example of a discrete anode is the cross strip anode (Figure 3.3) that has been used by Siegmund et al. (2009) in laboratory prototypes and is improved to larger formats and by means of a specialized readout ASIC by Vallerga et al. (2010, 2014). This development is shown in Section 2.2.3 and the concept is used for the design of the MCP detectors that are developed at IAAT at the time of writing. A cross strip anode readout was shown to allow for a spatial resolution of 5 µm at a moderate gain of 5×10^5 (Vallerga et al., 2009).

Pixellated readouts. Pixellated readouts can be particular ASICs or CCDs in general. The applicability of the latter ones for UV detection is discussed in the next section.

Pixellated anode ASICs consist of a pattern of pixels where each pixel contains a dedicated processing stage. The main advantage of this ASICs are huge input rates while their resolution is rather moderate.

The `Medipix2` ASIC is a detector chip that was developed at CERN for tracking applications in High Energy Physics and was used in other fields and for the readout of MCP detectors. It contains a 256 times 256 pattern of pixels with a pixel size of 55 µm. Each pixel contains an amplifier, a discriminator and a counter. As the events are integrated on the ASIC, the time tagging is only accurate to the period of the frame readout. Furthermore, the event amplitude information is not processed in `Medipix2`.

`Timepix` is a modification of `Medipix2` that allows furthermore to determine the pulse amplitude of each event. In this way, when the charge cloud that leaves the MCP is spread over several pixels, a sub-pixel event location can be determined that is resolved better than 16 µm at a lower threshold of the gain that is about 10^4 (Vallerga et al., 2009).

Strengths and disadvantages of MCP based detectors

MCP detectors are a mature technology with plenty of flight history (see Section 2.2 for examples of MCP detectors on past observatory missions). MCP detectors are solar blind and have good DQEs. MCP detectors are photon counting devices which makes it possible to acquire data without reaching an upper limit of the device capacity compared to integrating devices. MCPs are limited only by the statisctical photon noise and not by internal background contributions. The GDR is usually limited by the speed of the readout electronics because a certain conversion time is necessary for each event. The LDR is determined by the recharge timescale of the MCP while the LDR is general strongly depending on the scene that is recorded as well. MCP detectors are operable in a wide temperature range. They are radiation hard though the readout electronics has to be designed radiation hard as well.

The need for a high voltage supply that is usually complex is the major disadvantage of MCP detectors compared to alternative UV detection devices. The gain of the MCP decreases as a function of the total charge that is extracted over time. By preconditioning the MCPs, the gain sag is smaller and can be compensated by adjusting the high voltage. Hexagonal structures in flat field images when standard glass MCPs are applied are a further disadvantage. Finally, from a practical point of view, the large surface area of the MCPs due to the channels as well as the high sensitivity of common photocathodes to residual gases requires a careful handling and complex facilities during the fabrication process (Joseph, 2000).

2.1.2. CCDs: Photoconductive detectors for the UV?

CCDs are investigated as an alternative to photoemissive UV detectors and MCP detectors in particular.

In CCDs, incoming photons cause electrons of the semiconductor material to transit into the conduction band of the device's material. The charges are collected in an array of capacitors where the amount of charge in a capacitor corresponds to the light amount in the specific location of the capacitor. The total amount of charge is limited for each capacitive cell. The readout of the CCD is a transfer of the charges from one line of capacitors in the array to the next line. At the edge of the array, charge pre-amplifiers are located and their voltage output is digitized.

The most prominent problems that prevented CCDs from the broad application in UV observatories so far are (Joseph, 1995):

- The DQE of common CCDs below a UV wavelength of 200 nm is lower (15 % at 150 nm for the CCDs in WFPC2 on HST (Clampin, 2000)) compared to MCPs.
- As CCDs are operated in integrating mode, the read noise is present on a smaller sample of data compared to photon counting MCPs.
- CCDs require filters on top or in front to make them solar blind. But most filters have relatively low UV peak transmission.
- CCDs must be cooled to decrease the internal dark currents. In this way, residual gases in the instrument that condense onto the cold CCD surface might decrease the UV DQE even more.
- Cosmic ray hits degrade the charge transfer efficiency and increase the levels of dark current. This effect is more important in higher orbits than in the lower ones.

The advantages of CCDs compared to MCP detectors, if the technical difficulties could be overcome, would however be:

- The incident electromagnetic radiation is detected directly in the CCD material. There is no need for an intensification mechanism. This would make the detector assembly lighter, smaller and less complex. In particular, no complex high voltage supply is necessary as it is the case for MCP detectors.
- No lifetime limitation compared to MCPs.

Possible solution mechanisms to overcome the technical problems are to include phosphor in a CCD coating to shift the UV radiation to the visible band, the thinning and back-illumination of CCDs, and to apply anti-reflection coatings. Furthermore, as UV radiation is absorbed in the surface of the CCDs, attempts are made to move charge that is produced close to the surface into the gate structure. This can be done by means of an electric field that is established by ion implanting or by applying a bias gate on top of an insulating layer.

UV Detector systems that already used CCDs had mechanisms to convert the incident UV radiation to either electrons or optical light that can be detected by the CCD.

An Electron-bombarded CCD (EBCCD) comprises an opaque photocathode on a planar substrate where photoelectrons are released, an electromagnetic focusing and accelerating system, and a CCD. The focusing system is bulky and heavy however. An EBCCD was flown in the IMAPS spectrometer on ORFEUS-SPAS (Jenkins et al., 1996). This configuration has high DQEs and is radiation hard.

The MCP-intensified CCD (ICCD) consists of an MCP that is coated with a photocathode. At the back of the MCP, a phosphor coated fiber optic bundle images the charge cloud that leaves the MCP onto a CCD. The LDR in this configuration is constraint by the phosphor persistence and the CCD framing rate as the CCD is used in a photon counting mode. A typical charge gain is 2×10^5. An interpolation between CCD pixels is possible if the light spot is spread across a few pixels in each coordinate of the detector plane. A resolution of smaller then 10 µm is possible (Lapington, 2004).

Further alternative UV detection devices that are under investigation are AlGaN or GaN solid state detectors. They offer a natural sensitivity to UV due to their high band gap, they are solar blind and offer high DQEs. These detectors can be build compact and are radiation hard. The cutoffs of the sensitivity at the red side of the spectrum is tailorable between 195 nm and 365 nm. The problems that have to be overcome are high leakage background currents due to a bad material quality and a high read noise (Joseph, 2000).

Recently, silicon CMOS sensors have been introduced that are sensitive to the Far-UV range. They exceed 10 % DQE between 100 nm and 200 nm. These data are however shown only for single-pixel devices (Davis et al., 2012).

Obviously, MCP-based detectors with an anode readout are still the best choice for designs of future UV instruments. To conclude, Table 2.1 shows a comparison of selected UV detectors.

Table 2.1.: Performance comparison for different UV detectors (Joseph, 1995; Siegmund et al., 1997, 2009).

Parameter	ICCD	EBCCD	FUSE DDL	Berkeley CSA
DQE	15 %-20 % @121.6 nm	50 %-60 % @121.6 nm	40 % @115 nm	
Max. LDR	5 cts/pixel/s	45 cts/pixel/s		
Max. GDR	2.0×10^4 cts/s	1.5×10^6 cts/s	4×10^4 cts/s	$> 1 \times 10^6$ cts/s
Pixel Size	$7.5 \times 7.5\,\mu m^2$	$21 \times 21\,\mu m^2$	$15 \times 45\,\mu m^2$	$< 12 \times 12\,\mu m^2$
Maturity	Major program	Flight	Major program	Laboratory
Photon Counting	No	Yes	Yes	Yes

2.2. MCP detector realization examples

2.2.1. ORFEUS-SPAS II wedge and strip anode detectors

Instrument. On the German platform ORFEUS-SPAS, two instruments could be served by the ORFEUS telescope: the Rowland spectrograph developed at the University of California at Berkeley and the echelle spectrograph developed at the University of Tübingen and the Landessternwarte Heidelberg (Barnstedt et al., 1999). A tiltable mirror was used to switch between the two spectrographs. The echelle grating had a groove density of 316 lines mm^{-1} with a blaze angle of 62.5°. The spectrograph was operated in the diffraction orders of 40 to 61 and covered the wavelength range between 90 nm and 140 nm. To separate the orders, a spherical cross disperser grating with 1200 lines mm^{-1} was used.

Detector concept. The MCP detectors in the echelle spectrometer on board of the ORFEUS-SPAS II mission had a wedge and strip anode for photon position determination. The detectors, the readout electronics, and the on board processor had been developed at the Institute for Astronomy and Astrophysics, Department Astronomy of the University of Tübingen. In the detectors, a Z-stack of three MCPs provided a gain of 10^7 to 10^8 electrons per photon. During flight, the gain of the detector was controlled by variation of the high voltage of the last MCP in the stack. The photoelectrons that were released off the area between the channels were forced back into the channels by a repellent grid in front of the MCP stack that produced an electric field of 50 V mm^{-1}. This grid improved the quantum efficiency by around 30 % but decreased it at the same time by around 10 % due to shading of the detector active area. The anode was oversized to an active area of 44 mm × 44 mm to avoid distortions within the area of the detector. The readout provided a 1024 by 512 pixels image format.

Readout electronics and data handling. For each photon event, the readout electronics sent the coordinates for the dispersion as well as the cross-dispersion direction to the on board processor of the instrument. There, an image was integrated and stored on tape at the end of each observation. Furthermore, most event coordinates were stored on tape in parallel to the image integration. Hence, it was possible to keep track

of the event arrival time with a resolution of below 1 s. The maximum event rates have been 30 000 counts s^{-1} for the integrating data path and 3500 counts s^{-1} for the time tagging path, respectively. The electronic dead time was about 13 µs per event. For the functional check of the instrument after the integration into ASTRO-SPAS and to monitor the electronic performance of the detector during the mission, electronic test pulses were fed onto the anode at two corners with three different pulse heights.

Spectral performance. In the main dispersion direction of the echelle spectrum on the detector, one optical resolution element was 161 µm ($\Delta\lambda$=λ/10 000) and corresponded to 3 detector pixels. The electronic resolution was estimated to be about 1.5 detector pixels which was sufficient to maintain the optical resolution of the echelle spectrometer.

2.2.2. FUSE helical double delay line detectors

Instrument. The instrument of FUSE incorporated four mirrors and gratings for the band pass between 195 nm and 365 nm. Two detectors were used to record two of the spectra each. The active area of the detector was 184 mm in dispersion and 10 mm in cross dispersion direction and in particular they have been curved to match the Rowland circle[1] of the instrument which was 1652 mm.

Detector concept. The MCP detectors used on board of FUSE had been developed at the Space Science Laboratory (SSL) of the University of California in Berkeley (Siegmund et al. (1997) and Sahnow et al. (2000)). A Z-stack of MCPs was used in the detectors. The photocathode was opaque KBr. The charge clouds that left the MCP stack were several mm in size and contained $1 \times 10^7\, e$ to $2 \times 10^7\, e$. A helical double delay line anode with an active area of 94 nm × 20 mm was mounted behind the MCP stack.

[1] To minimize the amount of optical components and losses due to reflection and transmission in an instrument, curved gratings are used that perform dispersion as well as imaging of the separated orders of the incident radiation. The Rowland circle is a model that passes through the center of the grating surface and marks the location where the images of the spectral orders are focused opposite to the curved grating.

In front of the MCP stack, two Ni meshes have been mounted to force photoelectrons that were created on top of the first MCP back into the channels and to keep charged particles off the detector that could increase the background.

The voltage across the MCPs were adjusted individually and in particular the voltages were reduced when FUSE passed through the South Atlantic Anomaly to prevent damage to the detectors (Kaiser and Kruk, 2009).

To maintain low pressure during the integration, two ion pumps were installed on each detector and furthermore a shutter with a sapphire window was installed to be able to illuminate the detectors under ambient pressure.

Readout electronics and data handling. A timing circuit was employed to encode the dispersion direction with a resolution of 5.92 µm to 5.98 µm. In the cross-dispersion direction, charge division was used and the resolution was between 9.1 µm and 17.3 µm. Stimulation pulses could be fed into the inputs of the preamplifiers employed in the circuits for test purposes.

Detector data processing units processed and filtered the photon events. Five independent masks could be programmed to reject events. Events that were not rejected were packed and sent to the instrument data system.

It received the data and could process them either in a time tag or a histogram mode. The time tag mode allowed a rate of 8000 counts s^{-1}, the histogram mode allowed 32 000 counts s^{-1} from all segments.

2.2.3. Cross strip MCP detector development at SSL Berkeley

The work by Siegmund et al. (2009) and Vallerga et al. (2010) on cross strip anode MCP detectors at the SSL culminated in a laboratory prototype with Parallel XS (PXS) readout electronics. The XSA MCP detector development at IAAT is based on the work at SSL.

Detector concept. Due to the fact that only a reduced gain ($\approx 10^6\,e$) was necessary compared to previous readout configurations, a stack of two MCPs can be used. Among different cross strip anode configurations, a rectangular version that has 72 strips on the two layers was manufactured. It is 47 mm wide. The pattern period of the strips is 640 µm and the capacitance of the strips is approximately 17 pF. The anodes are connected through hermetical holes to the back side of the anode.

Readout electronics and data handling. Each strip is connected to an input of a `Preshape32` 32-channel amplifier chip that was developed at Rutherford Appleton Laboratory Harwell Oxford for CERN. The output of the chip is a unipolar pulse ($t_{\text{rise}} \approx 40\,\text{ns}$, $t_{\text{fall}} \approx 200\,\text{ns}$) and the noise is in the order of $500\,e + 50 \times C_{\text{load}}\,e\,\text{pF}^{-1}$.

The output signal of the `Preshape32` chips are amplified again and digitized by discrete 12 bit analog-to-digital converters (ADCs)[2] for each anode strip at 60 mega-samples per second. The samples are fed into a `Virtex 5` field-programmable gate array and digitally Finite Impulse Response Filtered to extract the peak information. Event rates of up to $10^6\,\text{counts}\,\text{s}^{-1}$ in single-event-driven mode are possible.

Performance. A 10 µm pinhole mask was attached directly on the surface of the top MCP. A resolution of $\approx 20\,\mu\text{m}$ FWHM at a gain of $10^6\,e$ was shown.

Current work. The laboratory prototype of the XS MCP detector was upgraded with a Xilinx `Virtex 6` FPGA and redesigned for a rocket flight with the Colorado High-Resolution Echelle Stellar Spectrograph (CHESS) (Vallerga et al., 2014). The average spatial resolution in the x and y coordinates is 17.5 µm and 22 µm FWHM, respectively. The dissipated power is 16 W and the weight of the detector and electronics box is around 3 kg.

A polyimide cross strip anode was manufactured due to a lower dielectric constant to minimize anode capacitance. This anode concept is not feasible for a sealed tube detector design due to the outgasing of the polyimide and glues.

Two ASICs are developed: The 16 channel charge sensitive preamplifier chip `CSAv2` and the buffering and digitizing chip `Half-graph_2`. `CSAv2` has shorter rise- and fall-time for the shaped output pulses (22 ns and ≈ 80 ns) compared to the `Preshape32` chip. `Half-graph_2` has 16 channels and 12 bit resolution. The expected power consumption is 10 mW per channel in quiescent state. It will be more for high event rates.

[2] An integrated electronic circuit that converts a continuous physical measure (e.g. a voltages) to discrete digital information that represents the amplitude of the measure.

The submission of the `Half-graph_2` design to the foundry is planned for the autumn of 2014.

Challenges for XS MCP detector readout electronics.

Among further challenges, Vallerga et al. (2010) stated the following tasks of cross strip anode readout electronics in general:

- Control and configuration of a preamplifier and digitization processing chain
- Remaping of the preamplifier channel numbers to match the proper anode locations
- Correction of each data point for pedestal and gain non-linearity
- Event identification by a settable threshold
- Determination of the spatial extend of the event and search for the approximate center channel
- Implementation of a pileup filter so that events are not contaminated by previous events
- Identification of N triggered channels and taking M samples into account
- Search for the peak amplitude for each strip
- Calculation of two coordinates and the total charge of an event
- Correction of the information for expected sub-strip distortions
- Combination of the event coordinates, the total charge, and an event time as a single event
- Buffering of the event packets and passing them to the back-end

The tasks above have to be taken into account when designing readout electronics for cross strip anode micro channel plate detectors.

3. IAAT cross strip anode MCP detector development

The current development of novel solar blind and photon counting MCP detectors at the Institute for Astronomy and Astrophysics of the University of Tübingen (IAAT) (Diebold et al., 2012) was continued based on its successful heritage. The activities associated to this development incorporate the design of the components of a novel cross strip anode MCP detector. In particular, the detector body, the photocathodes, a cross strip anode, and the readout electronics (Diebold et al., 2013) are investigated. The detectors have been offered as a part of the German HIRDES (Kappelmann et al., 1995) instrument to be installed onto the WSO-UV satellite (Hermanutz et al., 2012). In the following, an overview of these activities is given apart from the readout electronics development which will be discussed in detail in chapters 4 and 5 of this work. In the first section of this chapter, the IAAT detector concept is presented and the components that comprise the detector are shown. The second section presents details on the production and activation of photocathodes as well as on the vacuum tight sealing of the detectors. These activities are performed in an ultra-high vacuum (UHV) facility that is also described.

3.1. Detector concept

The IAAT sealed tube detector design is shown in Figure 3.1. The tube diameter is 80 mm with a diameter of the active area of 40 mm. The tube of the detector body consists of aluminum oxide ceramics (Al_2O_3) that also isolates the contact pads that are intended to apply a high voltage to the MCPs. The contacts are made of Kovar (Fe54Ni29Co17). This combination of materials is chosen to match the thermal expansion coefficients of the materials and hence to reduce the thermal stress on the welds. The leak tight welding of the detector bodies is performed at Swiss Federal Laboratories for Materials Science, Dübendorf, Switzerland. A smaller version of the detector body is also manufactured that does not

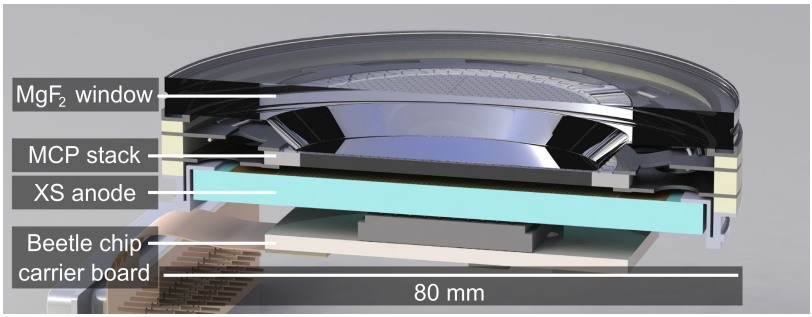

Figure 3.1.: Cross section of the CAD drawing of the IAAT sealed tube MCP detector design. Modified from Pfeifer et al. (2014a).

contain the inner parts of the MCP detector but is intended to test the window sealing process. Furthermore, the smaller tube works as a diode to measure the efficiency of a photocathode sample which is coated on the inside of a quartz window (see Figure 3.10).

The entrance window substrate consists of MgF_2 and is spaced apart from the MCPs by a few hundred micrometers in the center of the tube. On the inside of the window, a GaN or CsTe photocathode was coated to realize a semitransparent photocathode configuration. The detector tube and the window substrate have to be sealed leak tight in a vacuum environment to protect the photocathode from oxygen and moisture as well as to protect the MCPs from further residual gases. For this, and for the production of the photocathodes, an ultra-high vacuum (UHV) facility is used that creates a vacuum environment below 10^{-9} mbar (see Section 3.2).

Following the entrance window, in the center of the detector body, a stack of two MCPs in a chevron configuration is held by two electrodes. The distance of the upper MCP relative to the photocathode on the inner side of the window substrate is selected to realize a proximity focusing of the photoelectrons that leave the MCP stack. The relative orientation of the MCPs has to be adjusted to maximize gain and reduce Moiré patterns. The latter ones are created by the superposition of the images of the channel pattern of MCPs that are stacked.

At the back side of the detector body, following the MCPs, the cross

strip anode is located. It also is sealed leak tight to the detector body. The charge cloud that leaves the MCP stack at the back side is spread onto a few of the electrode strips. The width of the cloud extent on the anode area, and hence the fraction of the total charge that is placed on each of the strips, depends on the distance of the anode to the MCPs as well as on the high voltage across the stack of MCPs.

The charge that is spread on the electrodes of the cross strip anode is pre-amplified, digitized, and processed by the readout electronics (see Section 4.1 and in particular Figure 4.3 for details on the readout electronics configuration and the components that are used). The front end of the electronics which performs the pre-amplification is located on a multilayer ceramics hybrid carrier board that is directly attached to the rear of the cross strip anode. On this board, a `Beetle` pre-amplifier chip (see Section 4.2) is mounted. It pre-amplifies the charge signals, buffers them and provides them as a serial stream to the readout electronics FPGA board (Section 4.3). The connection to the FPGA board is realized as a polyamide flexible printed circuit board (PCB)[1] and two standard size connectors that are mounted to the flexible PCB. At the FPGA board, the information of the charge distribution is digitized and further processed in an FPGA in order to reconstruct the position where the original photon hit the detector.

Micro channel plates

In the detectors, a stack of two MCPs which are manufactured by Photonis USA, Inc. will be used (Figure 3.2). These are made of lead glass and one plate is 50 mm in diameter and 0.61 mm thick. The pore size and spacing are 10 mm and 12 mm, respectively. The micro channels are biased at an angle of 12° with respect to the normal of the MCP surface. The open area ratio is 55 %. NiCr electrodes are coated on both surfaces. The gain of one plate is stated by the manufacturer to be 10^4 at a high voltage of 1200 V (PHOTONIS, 2010).

[1] PCBs are used to mechanically support and electronically connect electronic components. The connections are done by means of pads and tracks that are etched off copper layers on non-conducting supporting substrates.

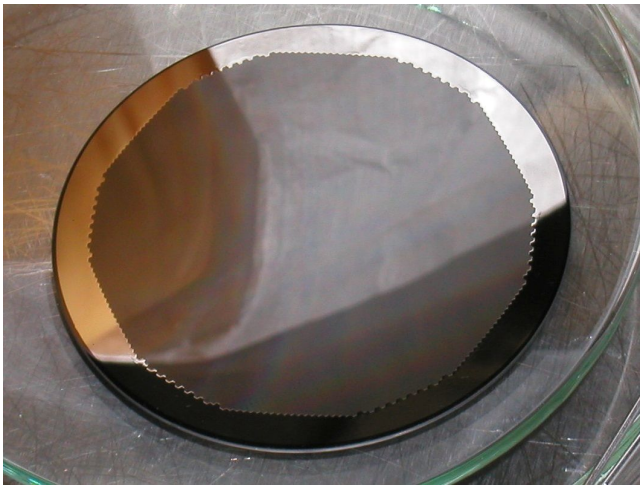

Figure 3.2.: An MCP manufactured by Photonis USA, Inc.. It will be used in the MCP detectors. Its diameter is 50 mm. Photograph by J. Barnstedt (IAAT).

Cross strip anode

The cross strip anode (see Figure 3.3) is assembled in a low temperature cofired ceramics (LTCC) process. The electrodes of the cross strip anode are placed on the top of a 70 mm supporting substrate, the anode total area is 44 mm by 33 mm. The cross strip anode is assembled as two perpendicular sensitive layers of electrodes that are separated by a layer of insulating strips. The sensitive layers are formed by 64 electrode strips each (Figure 3.4). The width of the strips on the top layer is 0.216 mm, the strip spacing is 0.699 mm. On the bottom sensitive layer, the strips are 0.4 mm wide and are spaced 0.524 mm. The strip spacing and the isolation layer parameters were optimized to realize a maximum sensitive area of about 61.8 % of the anode total area. The sensitive area splits up equally to the two active layers.

A version of the cross strip anode, where the electrode strips are buried below a ceramics cover layer is also available. It is coated with a highly resistive germanium layer. The layer is intended to keep the charge of the

charge cloud at their original position and couple it into the strips of the cross strip anode. Afterward, the charge can leave the layer slowly and does not concentrate on the surface area of the anode. This could cause a repulsion of charge clouds that leave the MCP stack.

The capacitance of the strips of the anode was measured to be around 7 pF for neighboring strips. The capacitance drops to around 4 pF when measured relative to more distant strips or relative to strips of the second layer. Measured to ground, the capacitance is in the order of 24 pF for the bottom layer and 22 pF for the top layer.

The electrodes of the cross strip anode are routed vacuum tight through the anode supporting substrate. On the back side of the substrate, they can be accessed by a 14 by 10 pattern of contact pads (Figure 3.5). In addition to the 128 electrode signals, pads for grounding and test purposes are included in the pattern of 140 contacts. Since the input capacitance is important for the performance of the `Beetle` pre-amplifier chip, the `Beetle` chip has to be placed as close as possible to the anode. For this, the ceramics hybrid carrier board that holds the `Beetle` chip has the same pattern of contact pads on its back side as the cross strip anode has. Hence, the anode and the `Beetle` chip ceramics hybrid carrier board can be directly attached by means of a double-sided spring-loaded contact connector (Figure 3.6). The cross strip anode was designed at IAAT and is manufactured by partners at VIA electronic GmbH[2].

3.2. UHV facility for photocathode production and detector tube sealing

For the production and activation of the photocathodes as well as for the sealing of the detector bodies, a UHV facility is operated. Figure 3.7 shows a cross section of the facility. It consists of two vessels that are separated by a valve and can be evacuated to a pressure of around 10^{-10} mbar individually. The evacuation of the vessels is performed by a three stage pumping system that includes an ion getter pump and a liquid nitrogen cooled titanium sublimation pump. The diameter of the vessels is 500 mm. A manipulator allows to transfer window substrates from the first to the second vessel.

[2] http://www.via-electronic.com/

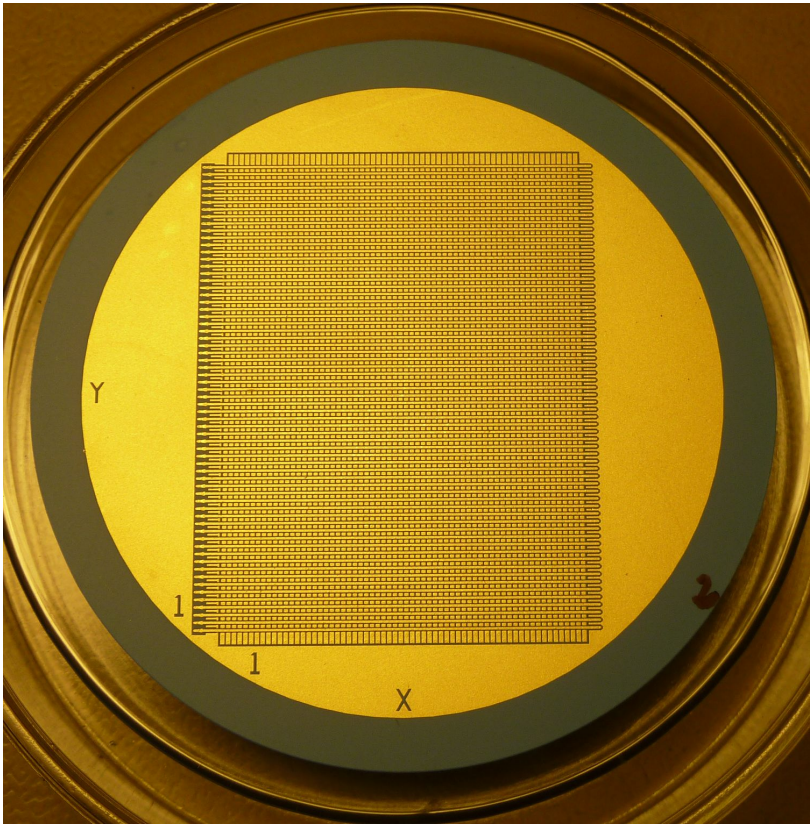

Figure 3.3.: The front of a cross strip anode to be used in the MCP detectors. The diameter of the LTCC carrier substrate is 70 mm, the size of the active area is 33 mm by 44 mm. See Figure 3.4 for a detailed view. Photograph by J. Barnstedt (IAAT).

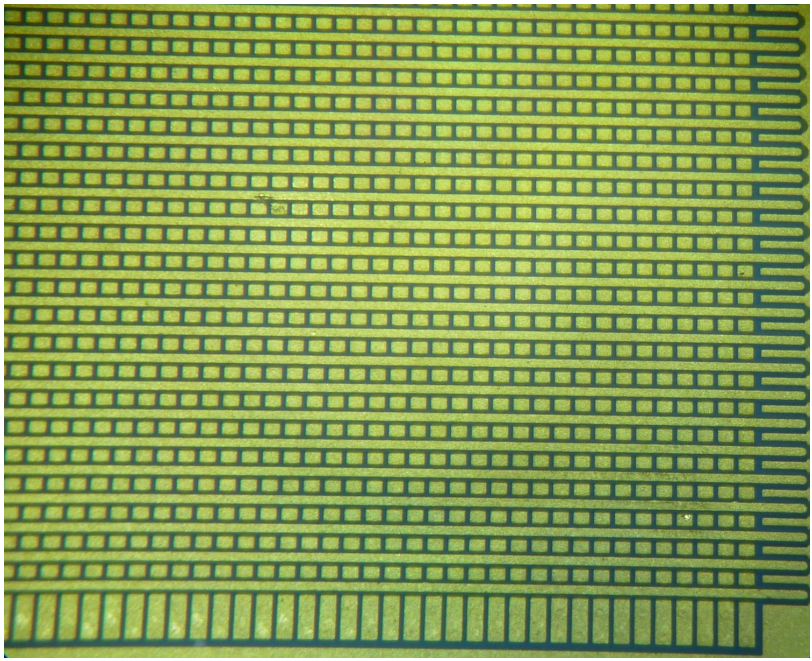

Figure 3.4.: Microscopic detail view of the front side of the cross strip anode that is shown in Figure 3.3. Photograph by J. Barnstedt (IAAT).

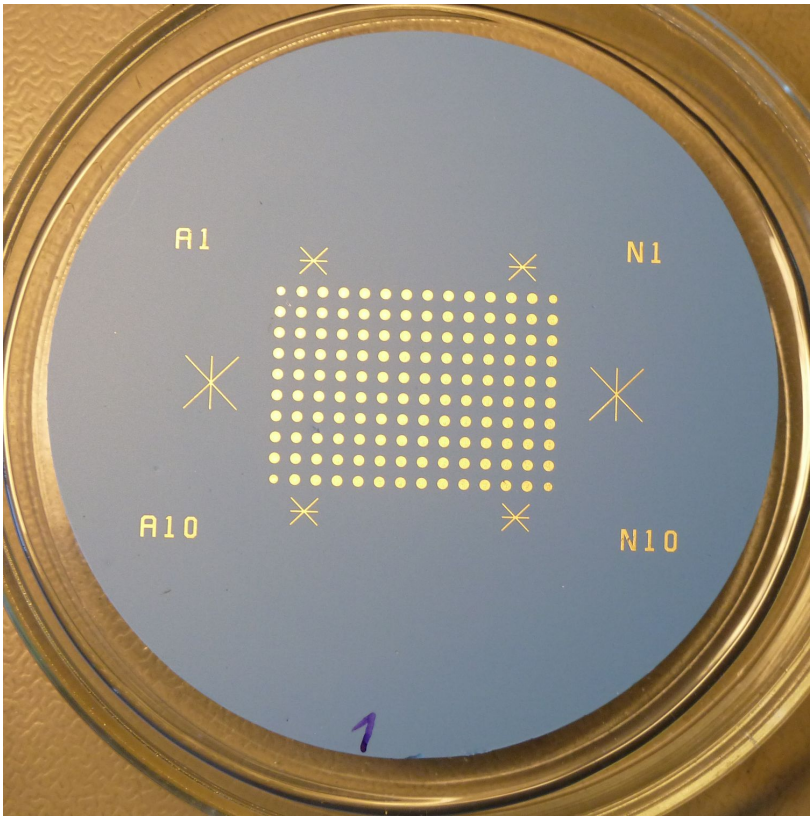

Figure 3.5.: The back of a cross strip anode to be used in the MCP detectors. The diameter of the carrier substrate is 70 mm. Photograph by J. Barnstedt (IAAT).

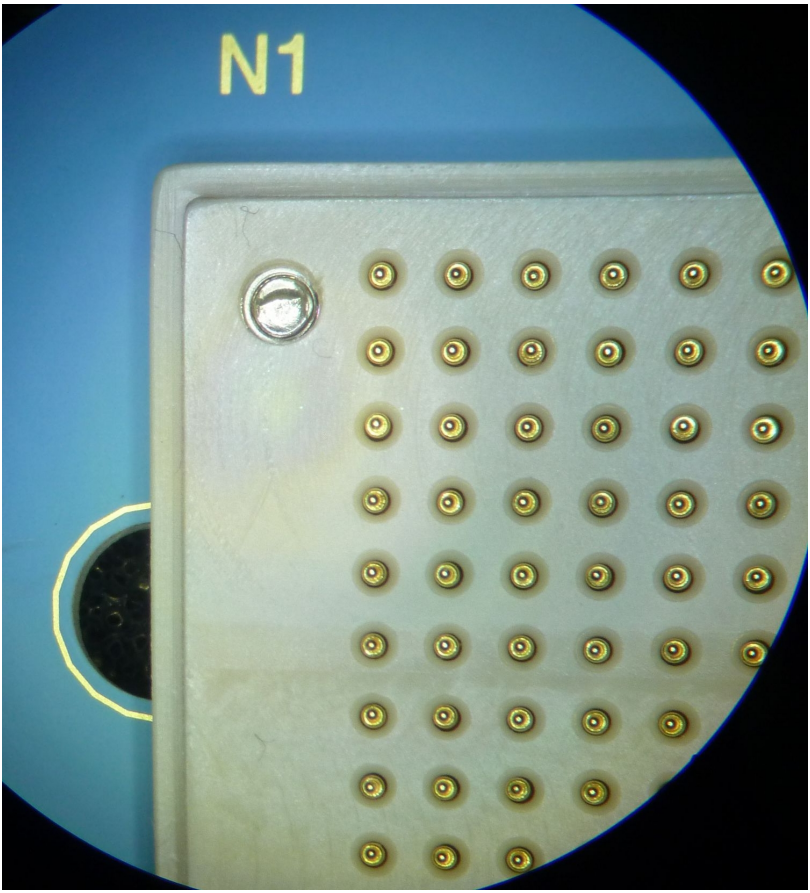

Figure 3.6.: Part of a 39 mm by 24 mm double-sided spring-loaded contact connector that is attached to the back side of the `Beetle` chip ceramics hybrid carrier board (Section 4.3.1). Photograph by J. Barnstedt (IAAT).

Figure 3.7.: Cross section of the CAD model of the IAAT UHV facility. The diameter of the vessels is 500 mm. Drawing by J. Barnstedt (IAAT), modified.

Photocathode production

In the coating vessel, the deposition and activation of photocathode layers on the bottom of window substrates is performed (see Figure 3.8). These substrates are made of quartz for test runs of the deposition and the diode sealing and made of MgF_2 when they will be used on top of the detector body. Quartz is much cheaper than MgF_2 which is used due to its UV transmission down to lower wavelengths compared to quartz. The deposition and activation of CsTe onto the window substrates is explored. The activation of GaN films that are grown by the working group "Energy Conversion" at the Clausthal Technical University is a further option. Up to six substrates can be stored on a rotating dish in the coating vessel. On one side of the vessel, the photocathode deposition and activation takes place. During the process, the substrate is heated from the top. An effusion cell is used for the evaporation of tellurium at temperatures between 250 °C and 300 °C. The rate of the tellurium deposition is between $0.1\,\text{Å}\,\text{s}^{-1}$ and $0.3\,\text{Å}\,\text{s}^{-1}$. A micro balance rate controller is used to monitor the deposition rate and layer thickness during the evaporation. The

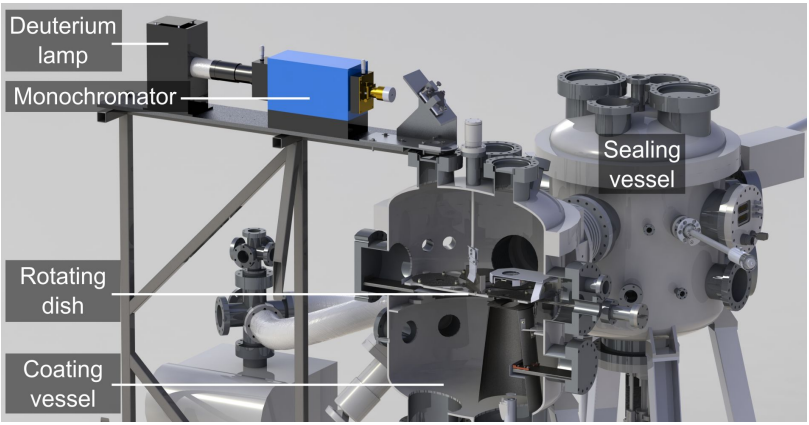

Figure 3.8.: Cross section of the CAD drawing of the IAAT UHV facility that shows the monochromator which is used for photocathode quantum efficiency measurements. Drawing by J. Barnstedt (IAAT), modified.

activation of deposited layers of Te and GaN is done by means of a high purity cesium dispenser. The optimum thickness of the CsTe film is in the order of 60 nm to 70 nm as estimated by simulations (Hermanutz et al., 2014, and references therein). The sample is illuminated by a UV LED that emits at a wavelength of 256 nm and the photo current is monitored by a low current amperemeter during the activation process.

To determine the quantum efficiency of the deposited photocathode film depending on the wavelength of the incident light, a deuterium lamp, a monochromator, and a calibrated photodiode are used. To do this, the sample has to be rotated to the other side of the coating vessel. The setup allows for a measurement of the quantum efficiency for wavelengths above around 190 nm up to 300 nm. The lower limit is due to absorption of the UV light of the monochromator in the surrounding atmosphere. Figure 3.9 shows the quantum efficiency versus wavelength of some CsTe photocathode samples that have been coated onto a quartz substrate in the UHV facility. The quantum efficiency shows a maximum at around 190 nm, decreases to a plateau for higher wavelengths and drops to zero at around 300 nm. As already stated, the character of the photocathode

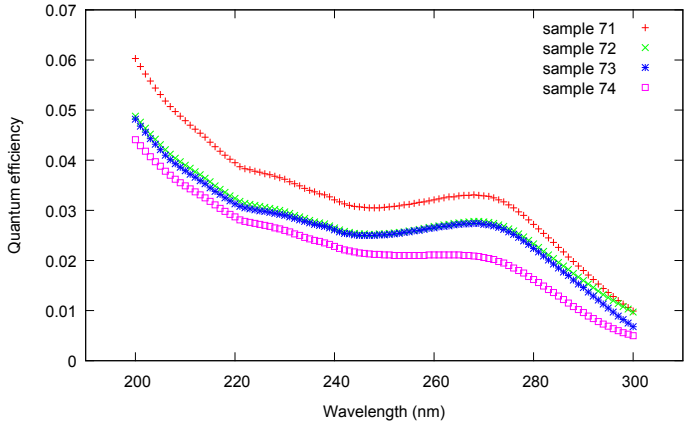

Figure 3.9.: Quantum efficiency of some CsTe photocathode deposition runs plotted against the wavelength of the incident UV light. They are coated onto a quartz substrate and have been characterized in semitransparent configuration in the IAAT UHV facility.

can not be investigated in the current setup below wavelengths of around 200 nm. The optimum CsTe photocathode configuration is investigated by the variation of pressure, temperature, material deposition rate, and layer thickness. See the dissertation thesis of S. Hermanutz (IAAT, in preparation) for further information.

Detector body sealing and test diodes

The sealing of the detector bodies is done in the sealing vessel of the UHV facility. Therefore, the detector body including the anode and MCP, but without the window on top, is placed in the center of the vessel. The detector window can then be transferred under high-vacuum conditions from the coating into the sealing vessel after a photocathode was deposited onto its inner side. The detector body and the entrance window are sealed in the sealing vessel by a molten indium alloy. The indium is placed on top of the weld seam as a solid ring at the beginning of this process. A heater is activated to heat the detector body to temperatures between 72 °C and

157 °C to melt the indium subsequently. The temperature depends on the indium alloy that is used. To heat residuals out of the detector body, it has to be heated to more than 200 °C in advance. After the indium is molten, the window is placed on top of the weld seam. The indium ring and the detector body and the window are pushed together subsequently. A mechanism to turn them with respect to each other in order to remove imperfections and bubbles in the weld is designed but not yet installed.

For the investigation of the details of the sealing procedure and in particular to determine the best heating cycle and indium alloy material, the production of photodiodes is performed (see Figure 3.10). The photodiodes are tubes that are made of the material which is also used for the detector bodies but reduced in size (25 mm diameter). The bottom face of the diode tube is realized as a contact plate that is made of Kovar. When a photocathode was deposited onto the window that is sealed on top of the diode, a measurement of the photo current under UV light illumination can be done and hence the quality of the cathode can be determined.

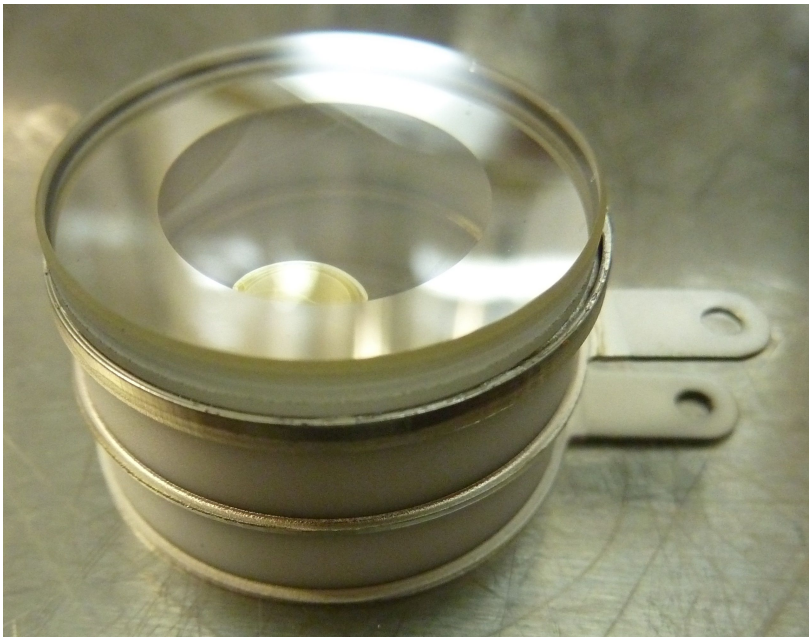

Figure 3.10.: Sealed diode body that is used for tests of the detector sealing procedure and to characterize photocathodes. The diameter of the diode tube is 25 mm. Photograph by J. Barnstedt (IAAT).

4. MCP detector readout electronics

As described in Chapter 3, the MCP detectors utilize a cross strip anode (XSA) to acquire the charge of the cloud that leaves the MCP stack on a pattern of 64 by 64 electrode strips. The readout electronics performs the digital position determination. The position of the incident photons can correspond to a certain photon wavelength if, e.g. a spectrograph is in front of the detector. The main task of the readout electronics therefore is to reconstruct the position of the photon by means of the charge information that is provided by the anode. Furthermore, a time stamp of the event and the total charge of the electron cloud that leaves the MCPs are important for observations of time variable sources and for MCP gain monitoring.

The readout of a cross strip anode was presented only as a laboratory prototype so far of which the power dissipation is to high for an application on a UV satellite (Vallerga et al., 2010).

The XSA readout electronics presented in this chapter employs the `Beetle` pre-amplifier chip to realize an XSA readout scheme with a low power dissipation (Pfeifer et al., 2012, 2014a,b). The work on the electronics included the development and simulation of a VHDL[1] firmware-design for a field-programmable gate array (FPGA)[2] that controls and communicates with the electrical building blocks that are necessary to readout the cross strip anode of an MCP detector. These building blocks are in particular the `Beetle` chip but also the ADCs to digitize the data for a further digital processing inside the FPGA. Other issues of this work have been the manufacturing and continuous improvement of the electronics prototype setups, the implementation of control and analysis software for the readout electronics, and tests of the single components as well as tests of the proper

[1] Very high speed integrated circuit (VHSIC) hardware description language. Parallel description language standard used in electronics design to describe digital or mixed-signal systems such as FPGAs. The standard is maintained and extended by the VHDL Analysis and Standardization Group (VHDL Analysis and Standardization Group, 2009).

[2] Integrated circuit which function is configured by a designer after its manufacturing. This can be done using a hardware description language (HDL) as for example VHDL.

function of the complete readout chain.

This chapter starts with a description of the readout electronics concept, followed by details of the realized readout electronics setup and its main components. A structural and functional overview of the FPGA VHDL firmware design is given. Finally, the readout and analysis software is described. A verification of the function of the readout electronics is done in Chapter 5.

4.1. Readout electronics concept

An MCP detector operates as a device to multiply a photoelectron that is released when an incoming photon enters the photocathode (as described in Section 3.1). The cloud of electrons that is produced in the channels of the MCPs and leaves the stack at its back side hits the cross strip anode and spreads the charge on a few electrodes of the anode.

Figure 4.1 shows the graphical output of a software that was written in this work to estimate the distribution of the charge on the anode's electrodes for certain cross strip anode and charge cloud geometries. The distribution of the electrons in the cloud is Gaussian with a FWHM of 0.8 mm. The charge distribution is divided into an array of 100 discrete cells along each axis for the calculations. The top plot in Figure 4.2 shows the charge in the cells through the center along the axis of the top layer electrodes. The bottom plot in Figure 4.2 shows the charge amount that is spread on each of the electrodes in the area where the charge cloud hits the anode.

One task of the readout electronics is to determine the center of gravity of the charge distribution from the discrete charge distribution on the anode. The center of gravity of the charge distribution corresponds in certain limits to the location where the original photon hit the photocathode of the detector. Discrepancies of the two positions are for example caused by the MCP channel bias angle and channel spacing as well as by perturbations in the electric field of the high voltage at the edges of the MCPs.

An illustration of the readout electronics concept is shown in Figure 4.3. It consists of the anode of the MCP detector, the `Beetle` pre-amplifier chip on a ceramics hybrid carrier board, and the front-end electronics FPGA board for the digital charge centroid processing. The 128 electrode strips of the cross strip anode are fed through the carrier substrate of the anode

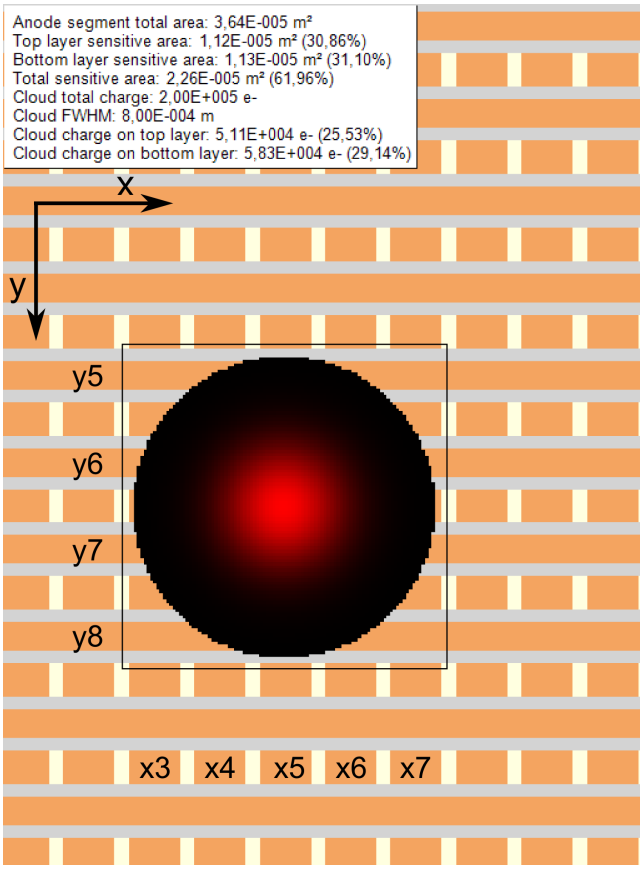

Figure 4.1.: Illustration of an assumed charge cloud that is spread on a cross strip anode. Yellow depicts the anode carrier substrate, orange are the perpendicular layers of the anode's electrodes which are separated by an insulating layer drawn in gray. The black box shows the border of the charge distribution of the cloud.

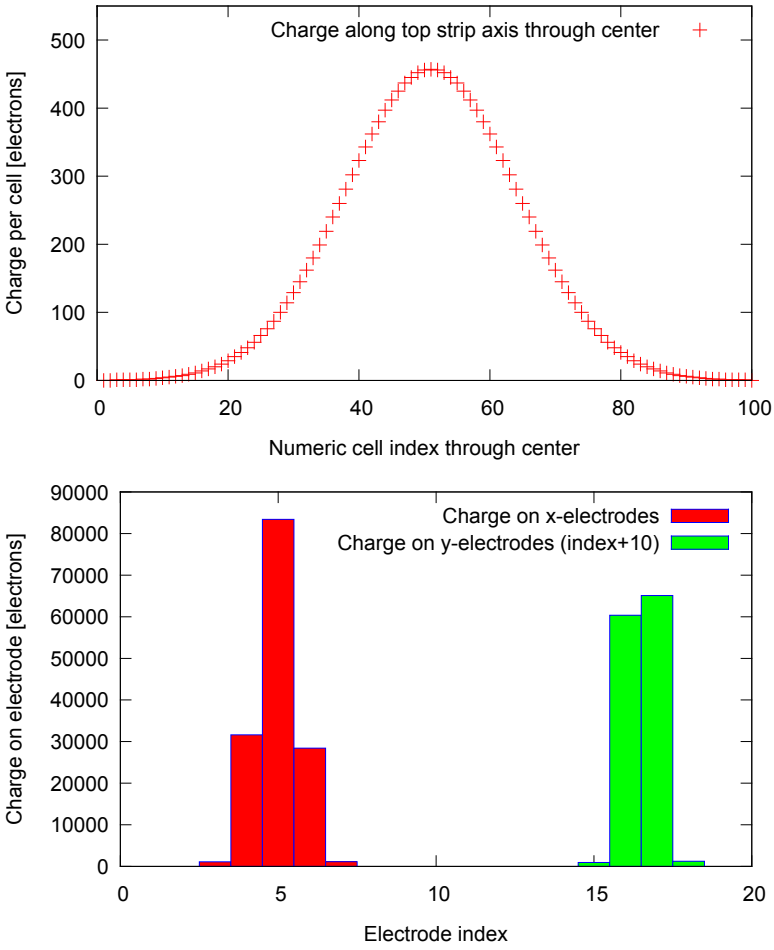

Figure 4.2.: Gaussian charge distribution in the assumed cloud (top) from Figure 4.1. The bottom plot shows the charge amount which is spread on each of the electrodes of the XS anode.

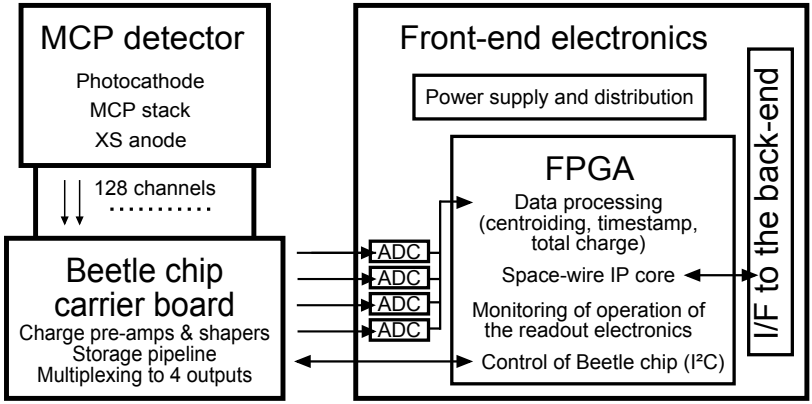

Figure 4.3.: The MCP detector readout electronics concept. Taken from Pfeifer et al. (2014a).

onto the back side of the detector tube and outside the vacuum of the detector tube. A double-sided spring-loaded contact connector connects the anode and the ceramics hybrid carrier board onto which the `Beetle` chip (Section 4.2) is mounted.

The main arguments for the application of the `Beetle` chip in the IAAT XSA MCP detector readout electronics are summarized at the end of the next section which describes the `Beetle` chip in detail.

The `Beetle` chip has 128 input channels and performs a pre-amplification, shaping and a buffering of all input channels in parallel. A discriminator stage in the `Beetle` chip can provide a trigger information. 160 samples are stored in the analog pipeline for each channel of which up to 16 samples can be marked for a consecutive readout. The charge information of all channels per sample is multiplexed to only four analog serial output ports and the information is driven off the `Beetle` chip by serial differential output drivers. Four ADCs that reside on the front-end electronics FPGA board of the readout electronics (Section 4.3.2) digitize the analog serial stream of charge information to a stream of 14 bit digital data samples.

The FPGA controls the readout of the data from the ADCs and is responsible for the correct timing of the `Beetle` chip readout control signals and the other fast control signals. The digitized data samples are processed in the FPGA afterward. The relevant subset of channel information has

to be filtered for each anode layer (event coordinate), the information from multiple samples has to be combined, and subsequently the centroid of the charge cloud, the total charge of the cloud, and a time stamp are determined. The FPGA furthermore implements the slow control in the form of an I^2C-bus-interface (see Section 4.2) for the configuration of the operating parameters of the `Beetle` chip. The information from each event is sent to a back-end via a standardized interface that can be SpaceWire (ECSS, 2008) or USB for the application in the laboratory. The FPGA implements a transfer protocol as RMAP for the case of SpaceWire (ECSS, 2010). Commands for the control and configuration of the components of the readout electronics are received in the FPGA from the back-end and decoded there. Status parameters can be requested from the FPGA which can be for example counters for the number of trigger conditions that occurred or the number of sent and received communication packets.

4.2. The `Beetle` pre-amplifier chip

The `Beetle` pre-amplifier chip was originally designed at the Max-Planck-Institute for Nuclear Physics (MPIK) in Heidelberg for the application in the Large Hadron Collider beauty (LHCb) experiment at CERN (Conseil Européen pour la Recherche Nucléaire, french for: European Organization for Nuclear Research). The description of the `Beetle` chip which is given here is based on Löchner (2006). In the LHCb experiment, the `Beetle` chip is designated for the readout of silicon strip detectors[3] and is applied in a large number at different sites.

Silicon detectors typically have a current pulse of a duration of up to 30 ns depending on the sensor thickness. The total charge created in the sensor is proportional to the energy that is deposited by an incident particle into the sensor. The `Beetle` chip operates as a charge-sensitive amplifier and is attached directly to silicon sensor strips. The operational parameters of the chip are therefore optimized for this purpose.

[3] Detector configuration to detect charged particles in a depleted region of doped semiconductor material. It consists of around 300 µm of Si bulk material. The one face is *n*-doped. On the other face, strips of *p*-doping are implanted into the material with a pitch of a few ten to a few hundred micrometer. Separated by an insulating layer, readout strips are deposited on the *p*-doped strips.

Front-end and comparator stage. A schematic of the Beetle readout chip functional layout is shown in Figure 4.4. The Beetle chip can process 128 charge input signals in parallel. The processing chain consists of an analog front-end, a comparator stage, a storage pipeline, and an output multiplexing and driver stage. For each channel, the analog front-end comprises a charge-sensitive pre-amplifier, a pulse shaper and a buffer. The front-end output-signal is a semi-Gaussian voltage profile of which the peaking time, the peaking voltage at the maximum of the voltage profile, and the remainder can be adjusted. The front-end output pulse shape is shown in Figure 4.5 for a variation of the front-end bias voltage *Vfs*. The minimum peaking time is around 25 ns, the voltage remainder after the peak maximum can be adjusted to be less than 30 % after 25 ns for an input load capacitance below 35 pF. The height of the remainder of the front-end output pulse is strongly dependent on the value of the input load capacitance C_p of the detector for a given set of front-end parameters as shown in Figure 4.6. C_p is the capacitance of the electrodes of the detector which is connected to the Beetle chip input like a strip of a silicon strip detector or the electrode of a cross strip anode. The equivalent noise charge (ENC)[4] of the front-end for the latest Beetle chip version 1.5 was measured to be $(531 \pm 10)\,e + (49.8 \pm 0.5)\,e\,\mathrm{pF}^{-1} \cdot C_\mathrm{p}$ (Löchner, 2006).

Following the analog front-end in the Beetle chip, a comparator stage discriminates the output-signal of the front-end. A common threshold can be selected for all input channels and a threshold offset can be adjusted for each channel individually. The comparator output of four consecutive input channels is combined by a logic *OR* circuit. Two of this quadruples are multiplexed and driven off the chip via low-voltage differential signaling (LVDS) ports at the two-fold sampling frequency which is 80 MHz nominal.

Analog pipeline and multiplexer stage. The output of the analog front-end or the output of the comparator stage is sampled into the analog pipeline for all channels in parallel with the sampling frequency of nominal 40 MHz. The pipeline is realized as an array of switched capacitors and has a depth of 160 samples for each input channel. A multi-event buffer can store the location of up to 16 samples in the pipeline to be read out consecutively. In particular, the latency of a pointer to the cell to be filled

[4] The number of electrons one would have to collect from a detector in order to create a signal equivalent to the noise signal of the detector.

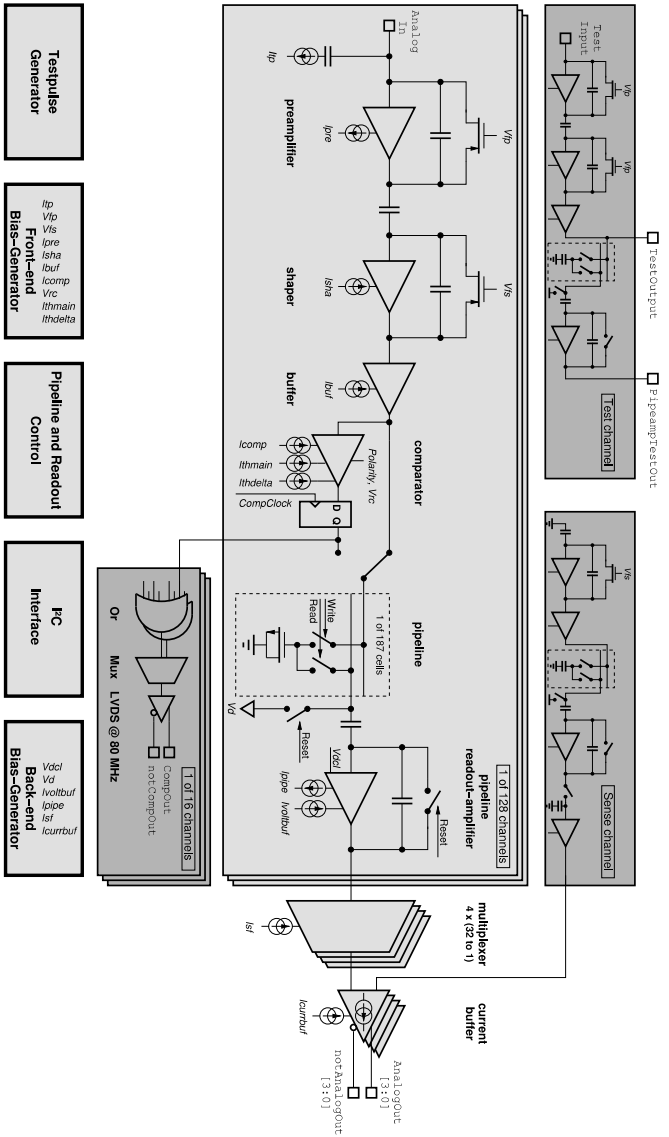

Figure 4.4.: `Beetle` functional layout. Taken from Löchner (2006).

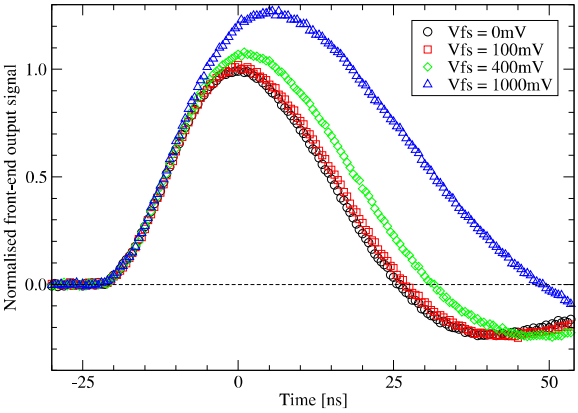

Figure 4.5.: Front-end output pulse of the Beetle chip for different settings of the shaper feedback voltage *Vfs* and nominal settings. The detector input load capacitance is $C_\mathrm{p} = 3\,\mathrm{pF}$. Taken from Löchner (2006).

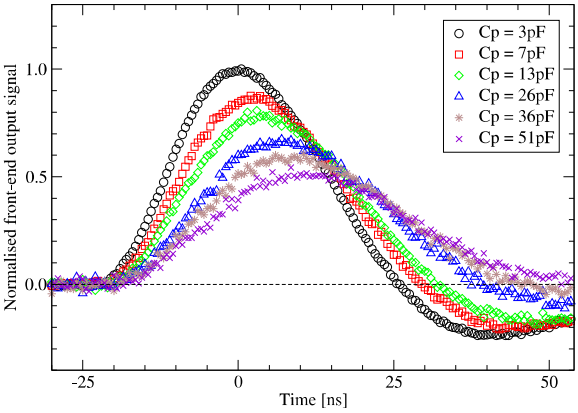

Figure 4.6.: Front-end output pulse of the Beetle chip for different values of the detector input load capacitance C_p. The Beetle chip is programmed to nominal settings. Taken from Löchner (2006).

next and the trigger pointer to the cell marked for a possible readout is programmable to be up to 4 µs. Hence, a delay of up to 4 µs for the trigger signal arrival time with respect to the arrival time of a sample at the front-end output is possible. Both pointers are incremented to the next pipeline cell on each sampling clock cycle and continue at the beginning of the pipeline when they reach the end. Locations marked for readout are not overwritten until the readout occurred.

Depending on the readout mode, the multiplexer stage connects groups of channels to the output ports. The modes that can be selected are the analog readout on one or four ports as well as the binary comparator readout on two ports. The readout is driven with a readout clock frequency which can be the sampling clock frequency or an integer quotient of the sampling clock frequency. Nominally, the ratio is one and hence the readout is done by 40 MHz. In the case of the *analog readout mode on four ports*, a total readout of one sample for all 128 channels including 4 header bits on each port will last 900 ns. At the maximum input signal amplitude, the maximum current through the output driver can be adjusted to be up to 20 mA. A readout header of 16 bit for diagnostic purposes is added in front of the analog data transmission of each sample.

Bias generators and digital control logic. To adjust the various parameters of the analog processing chain on the `Beetle` chip, bias voltages and currents are needed at various nodes at the different processing stages. These bias nodes, for example, influence the shaping time of the front-end, the threshold of the comparator stage, or the operating points of the amplifiers. All in all, 5 voltages and 11 currents have to be applied. The `Beetle` has on-chip bias generators. A current source to provide a constant reference current, a current digital-to-analog converter (DAC)[5], and a voltage DAC are placed various times across the chip area. All DACs have a resolution of 8 bit and are controlled by registers that are programmed via the slow control of the digital control logic block.

A digital control logic block is placed on the `Beetle` chip that comprises a slow and a fast control unit. The slow control unit implements an I^2C-interface. This interface standard was developed by Philips Semiconductors (now NXP Semiconductors, NXP Semiconductors (2012)). The I^2C-bus

[5] Integrated circuit that provides a current or voltage level at its output according to a certain value at the digital input.

is a bidirectional serial bus for the communication between integrated circuits that uses only two signal lines (serial clock and serial data). The bus is multi-master capable while only one master device is allowed to initiate a data transfer at the same time. The Beetle chip acts as a slave device on this bus and has to be addressed by a unique 7 bit address that is selected physically by bonding seven pads of the chip to either a logic high or logic low potential. The bus-master initiates a transfer and provides the synchronous I^2C-clock for the transfer with up to $100\,\mathrm{kbit\,s^{-1}}$. The communication is byte-based with the most significant bit transferred first. An I^2C-master core was designed and implemented in the FPGA VHDL firmware design of the MCP detector readout electronics to access the slow control block of the Beetle chip.

The fast control unit of the digital control block on the Beetle chip is the central control instance of the chip functions. It has multiple tasks among which are the control of the write and read switches of the analog pipeline, to keep track of and distribute the pipeline columns that are marked by a trigger for readout until they are read out, and the generation of the control, reset and start signals for the various components like the multiplexer block. Access to the slow control is possible by multiple external control signals. These signals enable the unit that controls the Beetle chip to monitor the pipeline operation via the signals WriteMon and TrigMon. The control unit has to synchronize itself to the data readout of the chip via the signal DataValid that is provided by the Beetle chip after a Trigger signal was applied to the chip. The readout timing, among other parameters, depends on the value of the trigger pointer latency. A dedicated component in the FPGA VHDL firmware design was implemented to access the fast control of the Beetle chip and to manage the readout of the chip (Section 4.4).

Output baseline in Beetle chip version 1.3 and version 1.5. Two versions of the Beetle chip have been applied in the MCP detector readout electronics setup. The output baseline behavior is different for the Beetle chip versions 1.3 and version 1.5. Figure 4.7 shows a measurement that was performed by Löchner (2006). It shows that the baseline of the Beetle chip readout is not constant during readout for the Beetle chip version 1.3. The absolute level of the output voltage rises as a function of the input channel number for Beetle 1.3. Furthermore, the slope of the baseline is smaller for the first sample than for the following samples of a series

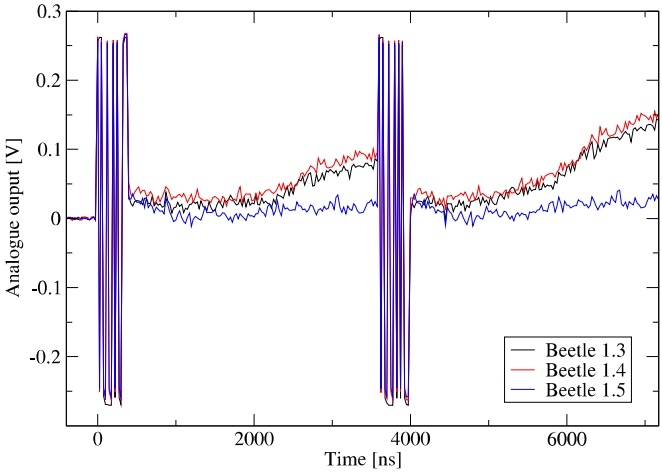

Figure 4.7.: The baseline behavior for different versions of the `Beetle` chip. Taken from Löchner (2006).

of consecutive samples that are read out. The difference corresponds to an input charge signal of around 5700 e. An improvement of the pipeline amplifier layout on the chip in version 1.5 faced this behavior. The baseline is flat for `Beetle 1.5` and there is only a difference between consecutive and non-consecutive readouts in the order of 700 e.

Radiation protection mechanisms. To realize a radiation hardening of the `Beetle` chip, several provisions are implemented. The transistors have a special layout and are surrounded by guard rings. Furthermore, an active single event upset (SEU)[6] detection and correction mechanism is implemented in the logic of the `Beetle` chip. The SEUs can occur for example in the radiation environment at LHCb or when operating the `Beetle` chip in the radiation environment in space as it is planned for the application of the `Beetle` chip in the readout electronics of the MCP detectors. In particular, the digital memory devices on the `Beetle` chip

[6] A temporary, non-destructive error that is for example a bit flip in a storage element as a register or a memory cell. It is caused by ionizing radiation that penetrates the semiconductor material.

in the form of the I^2C-registers as well as in flip-flops, counters and state registers of the control logic are effected by SEUs and without a monitoring and active correction mechanism, the front-end parameters might change during a measurement run or the control logic might even get stuck in an undefined state. See Löchner (2006) for details on the active correction mechanisms.

The expected total maximum dose for the Beetle chip in the setup at LHCb is calculated to be 7 Mrad. For the application in this environment, the chip has to be designed radiation hard and was tested for proper function under irradiation of up to 130 Mrad and showed only slight degradation in the performance.

Application of the Beetle chip in the IAAT XSA MCP detector readout electronics. The Beetle chip was chosen for the application in the IAAT XSA MCP detector readout electronics due to the following properties:

- Multiplexing capability of 128 input channels to only four analog output ports. It allows to reduce the power consumption compared to so far realized XSA readout electronics setups due to the fact that discrete digitization stages for each anode strip are replaced by one Beetle chip and four ADCs.

- Design of the Beetle chip front-end for an input load capacitance of below 35 pF. This specification is met by the measured capacitance for the IAAT XSAs in the order of 20 pF to ground.

- Nominal sampling frequency of 40 MHz and a output pulse shaping time of several ten nanoseconds. The acquisition of two to three samples for each photon event is possible and hence to average digitized charge information. A photon event rate of up to $300\,000\,s^{-1}$ is feasible.

- Active radiation protection mechanisms. This promises a good applicability of the Beetle chip in the radiation environment of space. Its behavior in a long-term space radiation environment has to be investigated.

4.3. Readout electronics setup

In this section, the MCP detector readout electronics setup that was developed and manufactured in this work is presented. The readout electronics comprises two main parts: the `Beetle` pre-amplifier chip on a ceramics hybrid carrier board or, with only 10 connected input channels, on a daughterboard provided by MPIK Heidelberg is one part. The front-end electronics FPGA board to control the `Beetle` chip and read out the data that are provided by the chip is the second of the two main parts. The ceramics hybrid carrier board for the `Beetle` chip and an earlier version as a `Beetle` chip motherboard (see Section 5.1) were designed at IAAT. The ceramics hybrid carrier board was designed and manufactured in a collaboration with partners from Micro-Hybrid Electronic GmbH[7]. The motherboard of the front-end electronics FPGA board assembly was designed and manufactured at IAAT.

4.3.1. `Beetle` chip ceramics hybrid carrier board

A `Beetle` chip is used for the pre-amplification of the charge information that is spread on the electrodes of a cross strip anode. The `Beetle` pre-amplifier chip is mounted on a ceramics hybrid carrier (CHC) board that is directly attached to the back side of the cross strip anode as described in Section 3.1. The anode and the CHC board have the same pattern of contact pads on their back side (Figure 3.5) and can thus be connected by a double-sided spring-loaded contact connector (Figure 3.6). The connector is adjusted to the CHC board by means of centering pins and holes in the ceramics, and mounted via screws.

The CHC board is a low temperature cofired ceramics (LTCC) multilayer board with an edge size of 50 mm (Figure 4.8). The electrode signals from the cross strip anode are fed through the carrier substrate and bonded to the `Beetle` chip as shown in Figure 4.10. The 128 charge signals from the anode are bonded to the `Beetle` chip in four rows of 32 bonding wires each. The `Beetle` chip resides in a cavity that is formed by cascaded bare layers of the ceramics. All signals from and to the `Beetle` chip are bonded to the die of the `Beetle` chip from either the CHC board or a flexible polyamide PCB. The flexible polyamide PCB is attached on top of the CHC board and provides the connection of the board to the front-end electronics FPGA

[7] http://www.micro-hybrid.de/en/home.html

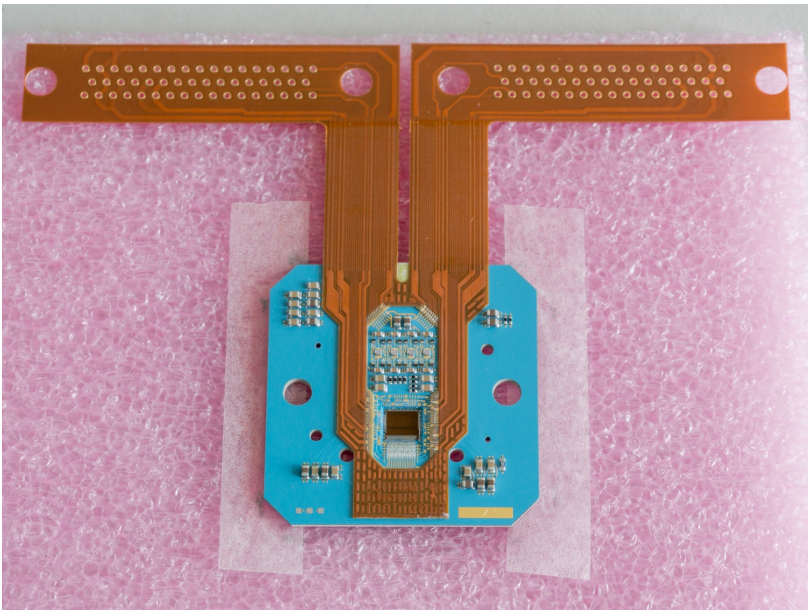

Figure 4.8.: The Beetle CHC board. The edge size of the blue multilayer ceramics board is 50 mm.

board of the readout electronics via two female 50-pin D-subminiature standard connectors. The two layers of the flexible polyamide PCB are also cascaded bare to support a bonding of the signal lines. Besides the Beetle chip and the flexible polyamide PCB itself, some passive parts are soldered on the CHC board. These are for example blocking capacitors at the power supply of the Beetle chip and resistors for the differential termination of the LVDS signals.

An operational amplifier circuit is located above to the Beetle chip. It is intended to drive the analog output of the Beetle chip off the CHC board and furthermore to adjust the analog output signal voltage range of the chip to the differential input range of the ADC that is located on the front-end electronics FPGA board.

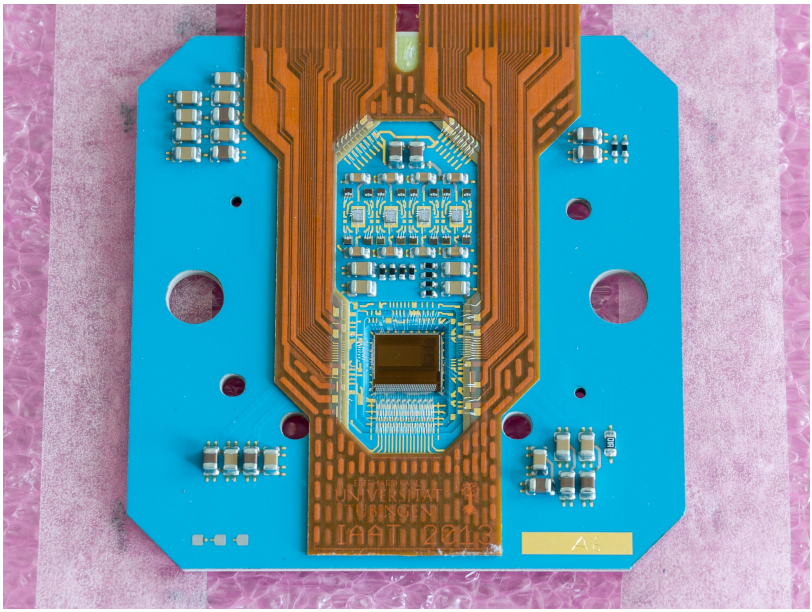

Figure 4.9.: Close up of the `Beetle` multilayer CHC board. The edge size of the substrate is 50 mm. The `Beetle` chip is mounted into the cavity in the center (Figure 4.10).

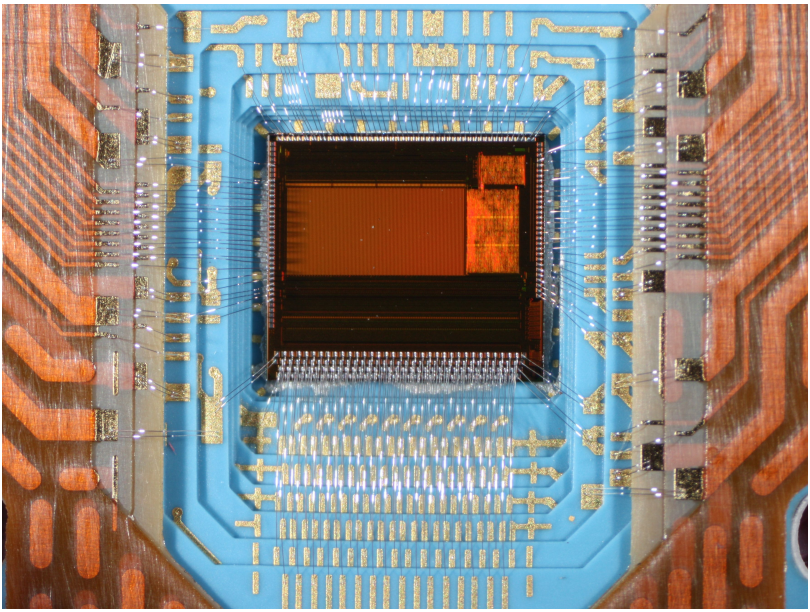

Figure 4.10.: Detail of the `Beetle` CHC board cavity where the `Beetle` resides. The die size of the chip is 5.4 mm by 6.1 mm.

4.3.2. Front-end electronics FPGA board

The front-end electronics FPGA board is intended to control the `Beetle` chip and to manage the readout, digitization, and processing of the analog data from the `Beetle` chip. The central control unit on the front-end electronics board is an FPGA. This is an integrated circuit that performs logic operations on its inputs and alters its outputs depending on the inputs and in most cases also depending on internal states. The logic operation of the FPGA is defined in the field after its production by a configuration from the user in contrary to application specific integrated circuits (ASICs) where the internal circuit is fixed after the manufacturing. The logic operation of an FPGA is described in a parallel hardware design language (HDL) as for example VHDL and can be synthesized to the logic cells of the FPGA using software tools that are usually supplied by the manufacturer of a specific FPGA. These tools furthermore allow to perform simulations on the HDL firmware design using a set of stimuli that are applied to the design in a virtual test bench. When its performance is simulated successfully, the HDL firmware design is programmed into the FPGA to test it under realistic hardware constraints.

The front-end electronics FPGA board is realized as a stacked assembly of boards (Figure 4.11). This solution is not optimal for best signal quality but was chosen to allow for a fast implementation of the FPGA VHDL firmware design and for its functional verification. In particular, the implementation and test of the functional block for the control and readout of the `Beetle` chip was the main focus.

The motherboard of the stacked board assembly is a PCB that was designed and manufactured at IAAT. It was initially manufactured for the purpose of fast hardware prototyping and to allow an easy access to the `Virtex-4` FPGA board connectors. Hence in the center of the motherboard, a micro module is stacked piggyback on the board on whose back side a `Virtex-4` FPGA is mounted. The pins of the FPGA are routed to the edges of the motherboard and can be accessed there via connectors.

On the left-hand side of Figure 4.11, the interface to the `Beetle` chip is shown. The laboratory interface board is stacked onto the motherboard and is manufactured using wire wrap technique[8]. The interface board

[8] A thin wire is used to connect electronic components that are mounted onto a paperboard. The wire is coated with an insulating material that evaporates on contact to a hot soldering iron. The bare wire and the electronic components are

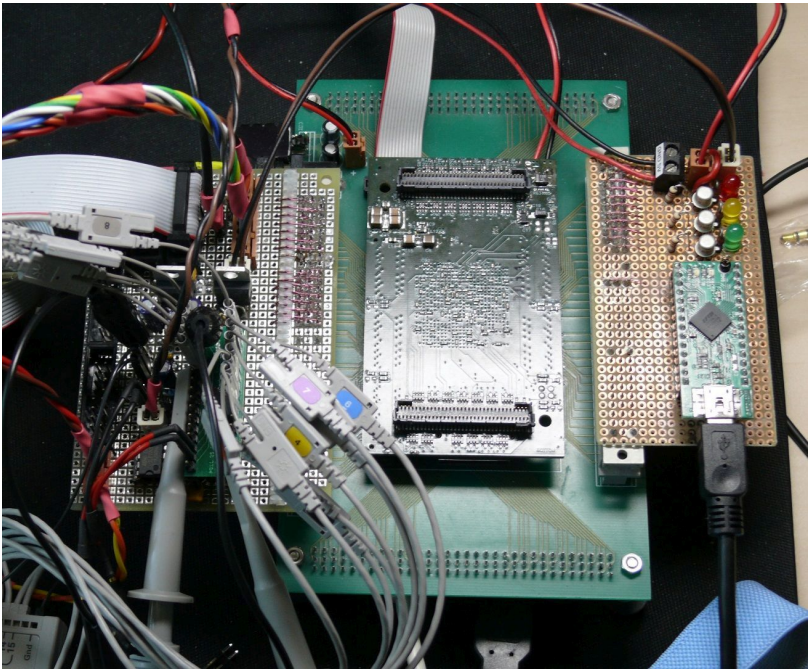

Figure 4.11.: The front-end electronics FPGA board setup which was assembled in this work.

carries the contacts to the Beetle chip and an AD9649 ADC (see below for details) to digitize the analog signals from the Beetle chip into a 14 bit data stream. In this work, analog data from the Beetle chip are read out via one ADC but the Virtex-4 VHDL firmware design is designed to be updated for a readout of the Beetle chip by four ADCs.

On the right-hand side of the front-end electronics FPGA board assembly, a second interface board is stacked that was also manufactured using wire wrap. The power distribution of the front-end electronics FPGA board assembly and a status LED circuit is placed here. Furthermore, the laboratory interface to the back-end laboratory PC is located here and supported by a FT232H USB interface chip (details below).

In future, both interface boards will be replaced and combined with the Virtex-4 FPGA in a printed circuit board design after prototyping and the functional verification of the current setup. This will enhance the signal integrity and enable us to increase the readout speed. The latter one is the case since the final design will also include four ADCs, one for each Beetle chip output.

In the following, the single parts of the front-end electronics FPGA board setup are introduced in more detail. The connection schematic of the stacked front-end electronics FPGA board assembly is shown in Figure A.1 of Appendix A.1.1. The pin assignment, and hence an overview of the signals that are employed, is given in Tables A.1 to A.4 of Appendix A.1.1.

Implementation of the central control unit

The central component of the front-end electronics FPGA board is a Virtex-4 SX35 FPGA micro module board that was manufactured by IAF GmbH[9] (see Figure 4.12).

The Virtex-4 is manufactured by Xilinx, Inc.[10] in a 90 nm CMOS process and provides on-chip distributed random access memory (RAM) and block RAM units. The SX35 is one of different versions of the Virtex-4 that are available and is dedicated for digital signal processing. It features a maximum of 240 kbit distributed and 3456 kbit of block RAM (Xilinx Inc., 2010). Dedicated components for clock-management and clock-distribution

connected by soldering tin.

[9] http://www.iaf-bs.de/en/products/fpga-modules/virtex4-sx35/

[10] http://www.xilinx.com/support/index.html/content/xilinx/en/supportNav/silicon_devices/fpga/virtex-4.html

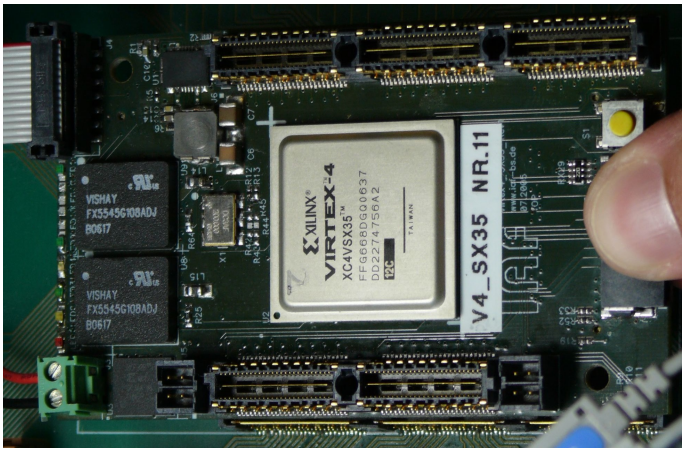

Figure 4.12.: The FPGA micro module used in the readout electronics. Connectors are seen on top and bottom. On the bottom left, the power supply is located. A JTAG programming interface to the FPGA and to a PROM is located on the top left.

are available for the VHDL firmware design software. 34 560 logic cells are implemented on the die of the `SX35` and 448 I/O (input or output) pins are available.

160 pins of the `Virtex-4` FPGA are accessible via two connectors mounted on the IAF micro module. On the module, DC/DC converters[11] are mounted that generate all necessary voltages to operate the core of the `Virtex-4` FPGA and its I/O banks. Hence, only one external 5 V power supply is necessary for the complete micro module. An on-board oscillator provides a clock signal of 200 MHz to the FPGA (IAF GmbH, 2006). A Joint Test Action Group (JTAG)[12] programming interface is mounted on the module to configure the VHDL firmware design content of the `Virtex-4` FPGA and also to load it into a programmable read-only memory (PROM)[13] that also resides on the board. The VHDL firmware

[11] Electronic circuit that converts direct current from one voltage level to another level.
[12] Common name for the IEEE programming interface standard *Standard Test Access Port and Boundary Scan Architecture*. Developed to debug and test PCBs and ICs.
[13] Particular form of data storage technology. Data is written into the device after

design can then automatically be loaded into the Virtex-4 FPGA from the PROM whenever the module is powered on.

The FPGA runs the VHDL firmware design that will be introduced in more detail in Section 4.4. The development and simulation of the VHDL firmware design consumed most of the time of this work. It performs the control and configuration of the Beetle chip as well as the timing of the readout cycles and synchronization of the ADC to this cycle. Raw data are acquired and sent to the back-end PC via a USB interface chip.

For a possible application of the MCP detector readout electronics in space, a radiation hard RTAX[14] FPGA from Microsemi was investigated as an alternative to the Virtex-4 FPGA. Due to SEU hardened flip-flops and its antifuse-based architecture[15], it is immune to a total ionizing dose of up to 300 krad. As RTAX devices are configurable only once, several prototyping options are available that span from reprogrammable hardware emulators, low-cost AX devices to RTAX PROTO devices that are identical to flight units but are tested less and are not hermetically sealed (Microsemi, 2013).

Implementation of the digitization stage

The AD9649 ADC that is used in the readout electronics setup is manufactured by Analog Devices, Inc.[16]. It has a digital resolution of 14 bit and is available in four versions that span a sampling rate of 20 MHz to 80 MHz (Analog Devices, Inc., 2009). The 40 MHz-version that matches the nominal sampling frequency of the Beetle chip is used in the current setup. The differential analog input voltage to be digitized by the AD9649 has to match its input voltage range of 2 V peak to peak. A bias voltage for the differential input voltage is generated on the AD9649 ADC and accessible via a pin to adjust the circuit in front of the ADC. The ADC core power supply voltage is 1.8 V and the digital output block can be operated at a supply voltage between 1.8 V to 3.5 V to match the digital signal level of the integrated circuit (IC) that receives the digital data as

manufacture and is permanent and hence also there after the power is removed.

[14] http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtax-s-sl

[15] The interconnections between logic blocks are open circuits after the manufacturing of the device. When programmed to connect, they form a permanent, passive interconnection.

[16] http://www.analog.com/en/analog-to-digital-converters/ad-converters/ad9649/products/product.html

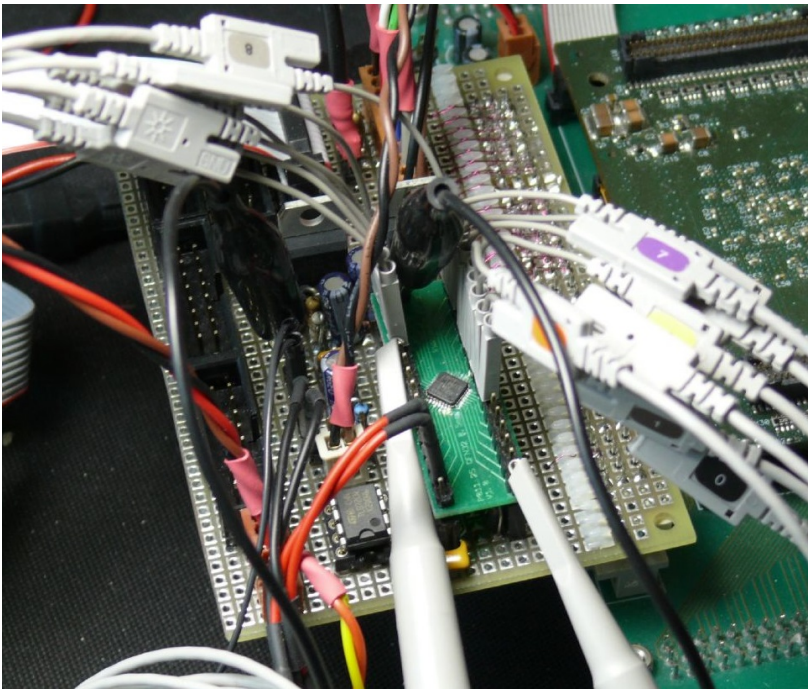

Figure 4.13.: The AD9649 ADC soldered on an adapter PCB. The wire wrap manufactured daughterboard also carries the interface to the Beetle chip.

for example the Virtex-4 FPGA. The data are driven off the ADC by a parallel interface. To synchronize the receiver IC to the ADC, a digital clock-out signal with the frequency of the sampling clock is provided by the AD9649 ADC. Furthermore, an out-of-range indication is available in the form of a logic signal given to the receiver IC.

The AD9649 ADC is soldered on an adapter PCB that is stacked into a wire wrap manufactured daughterboard on the readout electronics FPGA board (Figure 4.13). The daughterboard also carries the interface to the Beetle chip.

As a radiation-hardened alternative to the AD9649 ADC, a RHF1401[17] ADC from STMicroelectronics was investigated. It offers a similar functionality and resolution as the AD9649 ADC. For this, only minor changes in the VHDL firmware design and electronics architecture will be necessary for an application in space. As low-power radiation hard ADCs usually have a low sampling frequency, the sampling frequency or the readout clock of the Beetle chip can be adapted to the 20 MHz sampling clock of the RHF1401 (STMicroelectronics, 2012).

Interface of the readout electronics to the back-end

For the readout electronics interface to the back-end laboratory PC, a USB interface was chosen for the development phase. The FPGA interfaces a USB physical layer chip in the current configuration. The USB chip is an FT232H[18] UART IC soldered on a UM232H[19] that are both designed by Future Technology Devices International Ltd. (FTDI). The UM232H is a small development board that has connectors to interface the FT232H USB chip (Figure 4.14). It is mounted on a wire wrap manufactured laboratory interface board which is stacked into the motherboard of the front-end electronics FPGA board.

The FT232H USB chip is a single channel hi-speed USB to multipurpose interface chip and can thus be configured to provide a variety of interface standards to the user and handles the entire USB protocol on one chip. This makes it easy to use. For the case of the MCP detector readout electronics, the FT232H USB chip is configured to provide a 245 synchronous and parallel first in, first out (FIFO)[20] interface to the FPGA. 8 bit of data are transferred in parallel from or to the FT232H USB chip at a time with a data rate of up to 40 MB s^{-1} (Future Technology Devices International Ltd. (FTDI), 2012). To synchronize the user IC to the FIFO interface, the FT232H USB chip provides a 60 MHz clock signal.

The FT232H USB chip is used on the UM232H in a USB bus powered configuration. It is powered by a 3.3 V regulator on the UM232H adapter

[17] http://www.st.com/web/catalog/sense_power/FM137/SC1073/PF163456#
[18] http://www.ftdichip.com/Products/ICs/FT232H.htm
[19] http://www.ftdichip.com/Products/Modules/DevelopmentModules.htm
[20] A FIFO is a possible configuration of a data buffer where the first or oldest entry is read first. Electronic implementations of a FIFO can be of synchronous or asynchronous type. The read and write clocks are the same in the first case while two different clocks can be applied in the latter case.

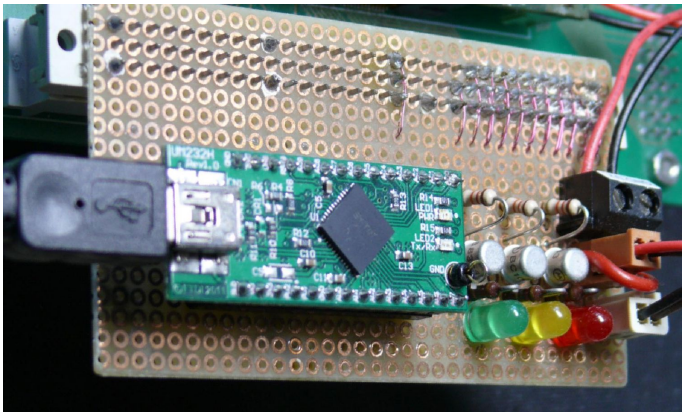

Figure 4.14.: Photograph of the FT232H USB chip soldered on a UM232H development PCB.The power distribution circuit can be seen on the right as well as status LEDs.

board. The interface type has to be programmed via a programming software to an electronical erasable PROM (EEPROM)[21] that is also soldered onto the UM232H board. The final configuration of the FT232H USB chip has to be performed via the driver in the readout and control software after powering the UM232H up by connecting it to a USB port (Future Technology Devices International Ltd. (FTDI), 2011).

As it was suggested by partners from industry, SpaceWire was investigated as a standard for the interface from the readout electronics to the back-end on a satellite. The standard defines the physical, signal, and the packet level of the interface (ECSS, 2008). In this work, VHDL SpaceWire receiver and sender-cores have been licensed. Hardware for tests and prototyping of the interface was ordered and investigated.

4.4. Virtex-4 FPGA VHDL firmware design

The FPGA of the readout electronics is the central part in the electronics setup besides the Beetle pre-amplifier chip and it has to perform the following tasks:

[21] PROM that can be erased and re-written electronically.

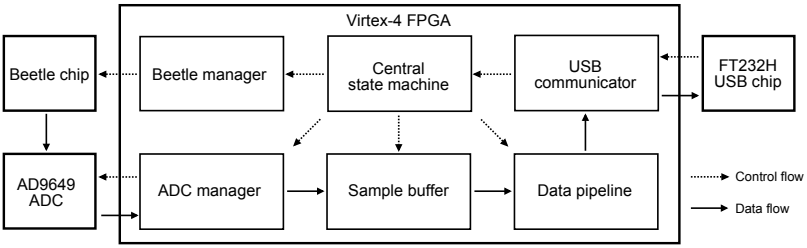

Figure 4.15.: The top level data and control flow inside the `Virtex-4` VHDL firmware design.

- Configuration of the `Beetle` chip after power-on
- Control of the `Beetle` chip during operation
- Control of the `AD9649` ADC
- Readout of the 14 bit digital data samples from the `AD9649` ADC
- Processing of the data samples
- Generation of packets from the data
- Transfer of packets to a back-end laboratory PC via the laboratory interface board
- Processing of configuration and control commands from the back-end laboratory PC

An overview of the modules of the VHDL firmware design that is configured into the `Virtex-4` FPGA of the readout electronics is shown in Figure 4.15 as well as the control and data flow in the design. The central finite-state machine controls all modules of the design. Control commands from the back-end enter the design via a USB communicator module and are processed in the central state machine. `Beetle` and ADC manager modules do the control and readout of the digital data from the `Beetle` chip. The data are buffered and processed in a data pipeline. Data packets from the data pipeline are transferred to the back-end via the `FT232H` USB interface chip.

In the following, an overview of the function of the separate modules in the VHDL firmware design in the Virtex-4 FPGA is given. Figure 4.16 shows the main tasks of the modules in the Virtex-4 VHDL firmware design and its structure.

Central state machine (CSM). The central module in the VHDL firmware design is a specific implementation of a finite-state machine (FSM)[22] called the central state machine. On start-up, the CSM initializes the overall VHDL firmware design and the modules in it are reset in an ordered manner. The most important task of the CSM is to control the other modules of the design depending on the current state of the CSM itself and the occurrence of specific commands. Hence, the CSM also has to decode commands from the back-end. These are commands for the acquisition control, Beetle chip configuration, and requests for Beetle register contents or internal status counters in different modules of the VHDL firmware design. An overview of the command identifiers and the command-packet structure, and hence the functionality that is implemented for the control of the electronics, is given in Tables A.5 and A.6, and Figure A.4 of Appendix A.1.2. Commands from the back-end can cause transitions in the current state of the CSM or they are passed to the destination module in the design.

Beetle manager module (BMM). For the configuration and control of the Beetle chip, a Beetle manager module is implemented. It comprises an I^2C-master core that was designed during this work and a RAM. The RAM stores the default configuration of the Beetle chip registers and an image of the configuration that is sent to the Beetle chip during power-on. The RAM content is also updated if a Beetle chip register content is altered by a command from the back-end. The BMM initializes the Beetle chip and performs write and read operations to the Beetle chip registers. Furthermore, the BMM provides the trigger signal to the Beetle chip and hence manages the trigger signal latency and duration. The determination of the number of samples that are submitted for a certain

[22] An FSM is a mathematical model of an automaton that can be in a finite number of states. It is only in one state at a time (current state) and the transition to another state can be triggered by an external or internal condition that is specific for each current state.

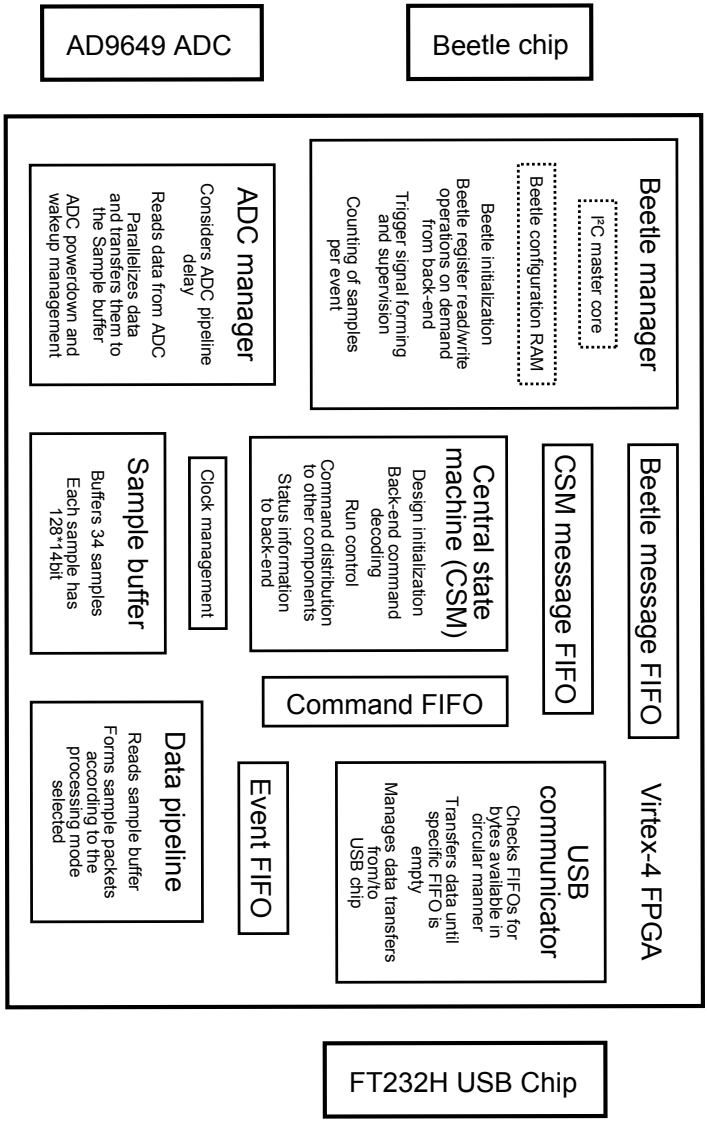

Figure 4.16.: The modules in the `Virtex-4` VHDL firmware design.

event is another important task of the BMM. This information is used to perform a subsequent assignment of samples to single events.

ADC manager module (AMM) and data pipeline. When the Beetle chip received a trigger, analog data are sent to the AD9649 ADC from the Beetle chip. The ADC is configured and read out by an ADC manager module in the VHDL firmware design. It supervises the ADC power down and wake up sequence. In addition, it keeps record of the correct readout timing of the Beetle chip and the AD9649 and considers as well the pipeline delay of the ADC. The data that are received from the ADC are parallelized by the AMM and passed further to a sample buffer module (see Figure 4.16).

The sample buffer module allows the FPGA to buffer up to 34 Beetle chip front-end samples for subsequent processing. Each sample consists of 128 vectors that are 14 bit in dimension.

The sample data is taken from the sample buffer module by a data pipeline module (DPM, Figure 4.16). Sample packets are formed in the DPM and passed to the USB communicator to send them to the back-end. The content of the packets depends on a selectable implementation of the DPM. The implementations available at the time of writing are a dummy packet mode, a mode where the index of the strips that carried the maximum ADC signal on each layer are transmitted, and a mode where all the raw data of a sample are transmitted to the back-end in addition. An overview of the packet structure depending on the selected implementation of the DPM is shown in Figure A.4 of Appendix A.1.2. The first implementation is intended for data transmission test purposes, the second one provides a rough 64 by 64 pixel image of the anode readout at low data rate. The implementation is selected via a generic variable in the code of the VHDL firmware design prior to the synthesis and hence prior to the configuration of the FPGA. The implementation of the mode selection via a command from the back-end is possible but is not implemented.

USB communicator module (UCM). A USB communicator module is the last of the main modules in the VHDL firmware design. It implements the interface of the VHDL firmware design to the FT232H USB chip on the laboratory interface board. All adjacent FIFOs are checked for available bytes in a circular manner. If a FIFO is empty, the UCM continues to

the next FIFO in the list and checks it. Waiting bytes in the FIFOs are transferred from the FIFOs in the VHDL firmware design to the FIFO in the FT232H USB chip or vice versa.

Clock domains and their organization. Several clock domains had to be implemented in the VHDL firmware design by enforcing asynchronous FIFOs which are buffering the command and packet transfer between different clock domains. The central state machine, the sample buffer module, the data pipeline module, and parts of the Beetle and ADC manager modules work in the global clock domain (GCD) of 100 MHz (see Figure 4.17). The Beetle chip induces a Beetle clock domain (BCD) of 40 MHz in which the second part of the BMM and AMM run. As the ADV7123 ADC is supposed to read data as soon as the analog data output of the Beetle chip is stable, it runs on a 180° inversely phased clock (ACD180) with respect to the Beetle chip clock domain and hence samples the analog output of the Beetle chip between the transitions of the Beetle chip output. The clock out signal of the AD9649 introduces an ADC clock domain (ACD3ns) to read the data from the AD9649 ADC. The ADC readout clock is phase shifted by 180° with respect to the ADC sampling clock and has an additional propagation delay of 3 ns. The USB clock domain (UCD) of 60 MHz is the last clock domain. The USB communicator module runs with a 180° phase-shifted version of this clock (UCD180) to assure that the in/outputs are sampled in the stable state between signal transitions. The command FIFO, the Beetle message FIFO, the CSM message FIFO, and the Event FIFO are all asynchronous and pass data across the clock domain borders.

The VHDL firmware design makes use of the clock management primitives that are available on the Virtex-4 FPGA. These primitives are logic blocks that are pre-optimized for this purpose and are implemented already during the manufacturing of the Virtex-4 FPGA. A 200 MHz clock signal is provided by an oscillator on the IAF micro module. The clocks in the different domains of the VHDL firmware design are derived from this clock signal or from the clock signals provided by the AD9649 and the FT232H chips. All the clocks that enter the FPGA are fed into IBUFG[23]

[23] Dedicated clock inputs of the Virtex-4 FPGA that are optimized for this purpose. They can be accessed by instantiating the IBUFG primitive in the VHDL firmware design.

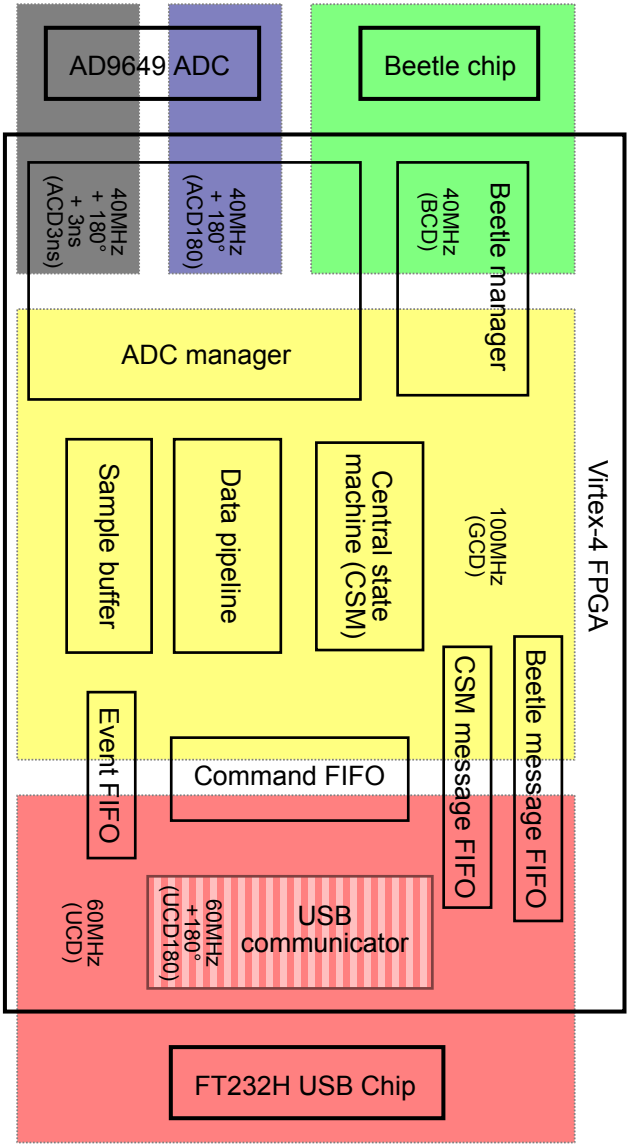

Figure 4.17.: The clock domains in the Virtex-4 VHDL firmware design.

global clock buffers. The buffered clock signal from the oscillator on the IAF micro module is divided by a factor of two via a phase-matched clock divider (PMCD)[24] primitive in order to generate the global clock signal. A digital clock manager primitive (DCM)[25] generates the Beetle chip and AD9649 ADC sampling clocks out of the global clock signal.

Resource utilization and timing constraints. An overview of the resource utilization of the VHDL firmware design depending on the data processing implementation which is selected in the Virtex-4 VHDL firmware design is shown in Table 4.1. In the implementations where only dummy packets or only the location of the strip on which the maximum charge was spread is sent to the back-end, the resource utilization is significantly smaller in the Virtex-4 SX35. This is because in these implementations, the internal data distribution of the raw data from the ADC is removed by the optimisation tool from the manufacturer since the information is not needed. In the raw data implementation, 128 14 bit-vectors transfer the raw data from one module to the next and the sample buffer VHDL module consumes a large amount of the Virtex-4 FPGA RAM primitives.

The maximum possible input clock for the three processing implementations is also shown in Table 4.1. As a 200 MHz input clock is fed into the FPGA and modified for the specific needs of the modules, the timing constraints are met in all implementations since a faster input clock could be applied.

4.5. Control and first-level analysis software

The MCP detector readout electronics is controllable via software that is installed on a back-end laboratory PC. The control software was designed and implemented in this work. It is written in C#[26], object-oriented, and in multiple parallel threads. Figure 4.18 presents an overview of the structure

[24] One type of clocking resource that is available on the Virtex-4 FPGA as a hardware macro cell. Its purpose is to provide clock signals that have a period which is an integer ratio of an input clock signal. In addition, up to three additional clock signals can be fed into the PMCD and delayed to match the modified clock signal.

[25] One type of clocking resource that is available on the Virtex-4 FPGA as a macro cell. A DCM is able to modify the period of an input clock signal as well as to delay the signal in certain limits which are selectable even during operation.

[26] C Sharp. Programming language that was developed by Microsoft.

Table 4.1.: `Virtex-4 SX35` VHDL firmware design resource utilization and timing performance. The parameters are given for the different data processing implementations that are available. The clock constraint to be met was 200 MHz.

Processing impl.	Registers	Slices	RAM	I/O	Max. clock
1: Dummy packets	6 %	12 %	4 %	14 %	259 MHz
2: Unprocessed data	17 %	30 %	30 %	14 %	225 MHz
3: Charge location	6 %	12 %	4 %	14 %	262 MHz

of the control and first-level analysis software. Several classes comprise two packets that control the readout electronics on the one hand and to perform a first-level analysis of the acquired data that are read via USB on the other hand. A screenshot of the user interface to the control software is shown in Figure 4.19. Figure 4.20 in the second part of this section displays the interface to the first-level analysis part of the software. In principle, the software is implemented in a way that also a console application can be launched with it besides the graphical user interface (GUI). A description of the two software parts follows.

Control class packet

The control-namespace[27] in the control and first-level analysis class packet of the MCP detector readout electronics software includes the actual main control class `MainControl` that can be accessed by a separately implemented user interface class. One member object of the `MainControl` class is an `FTDI` object that provides the access to the USB interface to which the `FT232H` USB chip of the readout electronics is connected. The `FTDI` class is a `.NET`-wrapper around the driver software, and the wrapper as well as the driver are provided by FTDI Inc., the supplier of the `FT232H` USB chip. The `FTDI` class manages transfers to read pending bytes that wait in the receive buffer of the `FT232H` USB chip as well as to write arrays

[27] A namespace is used in computer programming to group a set of symbols and identifiers that serve a particular functionality. All classes that are needed to control the readout electronics are grouped in the namespace `IAAT.MCPDetector.Control` for example. `IAAT.MCPDetector.Acquisition` and `IAAT.MCPDetector.Analysis` are further namespaces in the control and readout software packet.

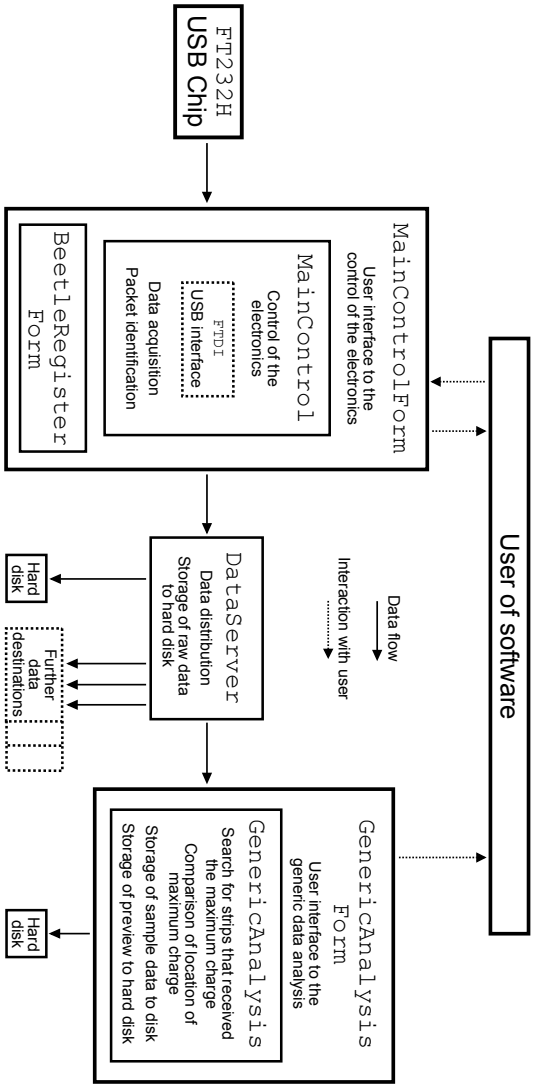

Figure 4.18.: Structure of the control and first-level analysis software.

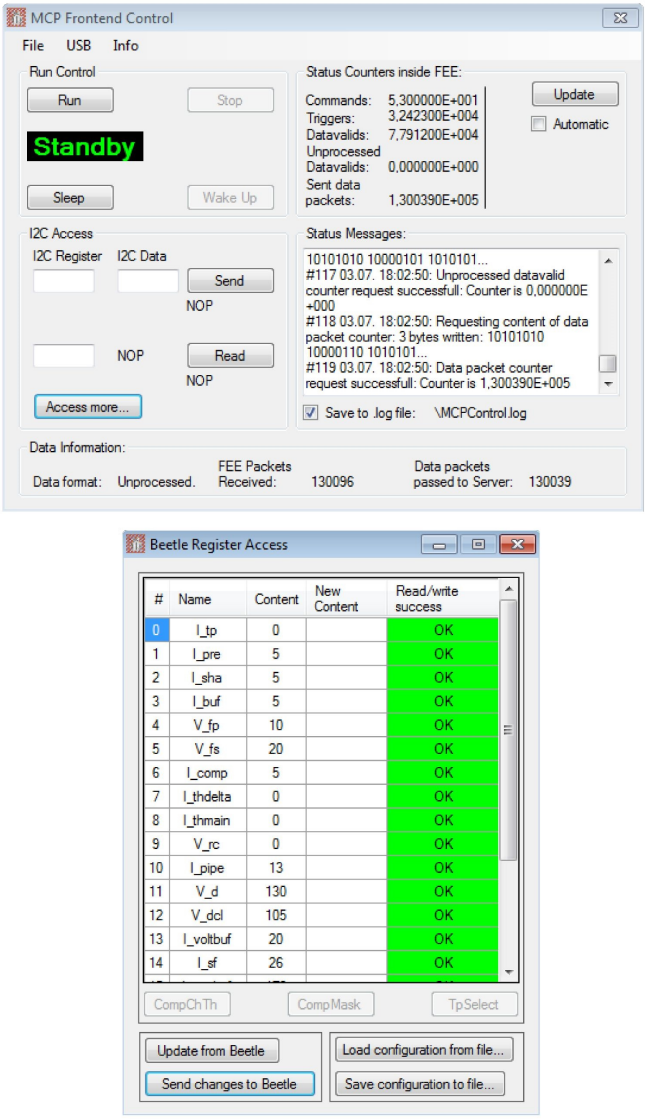

Figure 4.19.: The `MainControlForm` GUI.

of bytes to the FT232H USB chip via a USB port. The FT232H USB chip than manages the communication to the USB communicator module in the Virtex-4 VHDL firmware design of the readout electronics.

In the current implementation of the main program, on the start-up a MainControlForm graphical user interface object is created for the control of the readout electronics. The MainControlForm user interface has a MainControl object as a member and creates it when the form is loaded. The MainControl object starts several threads in parallel. They read data from the USB port as soon as data are available, filter the incoming stream of bytes and reconstruct data packets from the stream, run the data distribution process of a DataServer object, and, finally, run the data processing in a GenericAnalysis object. The DataServer and GenericAnalysis are discussed below.

The structure of the program was designed to allow to replace specific classes in the data processing chain by an alternative implementation. This is possible without the need to change the other modules of the processing chain as long as the specific interface requirements are fulfilled. The threads put data in internal queues and data are taken from one queue by the subsequent thread in the processing chain. In this way, the data are buffered as well. The multi-thread approach is state-of-the art and allows to deal with bursts of data though it induces the need for mechanisms to control the access to particular objects from multiple threads at a time.

The MainControl itself stays in operation as a further thread. It performs actions that are usually requested by the overlying MainControlForm graphical user interface. The user interface comprises five areas:

- Data acquisition run control
- Beetle chip configuration via I^2C
- Information panel for the status of the readout electronics
- Status message box
- Status bar to show the type and number of data packets that have been identified and passed to the DataServer object

The user interface areas to access the data acquisition run control, the Beetle chip via I^2C, and the status information in the readout electronics

all send particular commands to the Virtex-4 FPGA of the readout electronics via the MainControl class. These commands are shown in Tables A.5 and A.6 of Appendix A.1.2. The Virtex-4 FPGA of the readout electronics itself sends an acknowledging data packet for every command from the back-end. In case a command requests information, the acknowledging data packet can contain this information. The commands that are sent from the different user interface areas can be for the data acquisition run control, the configuration of the Beetle chip I^2C registers, and the request for the content of a specific Beetle chip register. Furthermore, current values of status counters in the Virtex-4 FPGA of the readout electronics can be requested. All commands are sent to the FPGA via the MainControl and its FTDI USB interface object.

The access to Beetle chip registers can be either performed as single register write and read accesses via input fields on the MainControlForm graphical user interface. Another way is to call a BeetleRegisterForm object via a button on the MainControlForm. The BeetleRegisterForm graphical user interface shows a matrix representation of the Beetle I^2C registers and their content. The matrix can be updated from the Beetle chip to check the current contents of the registers. Specific register contents can be altered and all sent to the Beetle chip subsequently in one cycle. A complete set of the Beetle I^2C register configuration can be saved to a file on disk and loaded into the matrix from a file as well. Currently, the Beetle chip shift registers access (see the Beetle chip description in Section 4.2) is not yet implemented on the MainControlForm graphical user interface.

The stream of bytes from the readout electronics is read by one thread continuously. A separate thread analyzes the stream and decodes the data packet structure from the stream. The data packet interpretation follows subsequently and depending on the content, specific actions are performed (Tables A.5 and A.6 of Appendix A.1.2). In the first case, the data packet received by the software is an acknowledging packet from the readout electronics that is the response to a command sent from the MainControl. Secondly, the data packet can contain information on the Beetle chip I^2C registers or the status counters in the readout electronics. The information is shown in the labels on the MainControlForm GUI. Data from the readout of the Beetle chip is the third possibility.

The data that is read out from the Beetle chip by the readout electronics and sent to the back-end is passed to a DataServer object when it was

identified by the MainControl. The DataServer acts in general as a connecting object between the MainControl control software part and the GenericAnalysis analysis part of the software. Furthermore, the DataServer allows to save the raw data stream into a text file or their transfer to further classes.

Analysis class packet

The first-level analysis part of the readout and control software receives the data that have been read from the Beetle chip by the DataServer class. The GenericAnalysis class is a member object of the MainControl and a process of the GenericAnalysis to analyze the data is started as a thread from inside the MainControl class. At the beginning of this process, a GenericAnalysisForm is created and shows up as a user interface to the GenericAnalysis object. A screenshot of the GenericAnalysisForm is shown in Figure 4.20.

When the GenericAnalysis process receives a sample from the MainControl, it is buffered in a queue. The process to analyze the data that are read from the Beetle chip checks the queue for samples available in a regular interval. The raw data of each sample are stored in a raw data file. Subsequently, the information of the sample is stored into several member variables of the GenericAnalysis class. The information depends on the type of the sample packet, which is determined by the actual configured implementation of the data pipeline module in the Virtex-4 FPGA of the readout electronics. Besides the data type identifier and the event and sample number, the electrode number that carries the peak charge on each cross strip anode layer can be included in the sample packet. In addition, the raw ADC data for each Beetle input channel, and hence for each anode strip, can be included in the sample packet and stored. The information that is acquired in this first-level analysis is stored into a further text file on disk.

If the raw ADC data are provided in the data of the sample that is processed, the software also searches for the electrode number that carries the largest ADC value for both anode layers. This is intended to test and verify these numbers that are earlier processed in the VHDL firmware design.

The coordinates (i.e. Beetle channel numbers from 0 to 63) for both peak charge locations that have been identified by the readout electronics

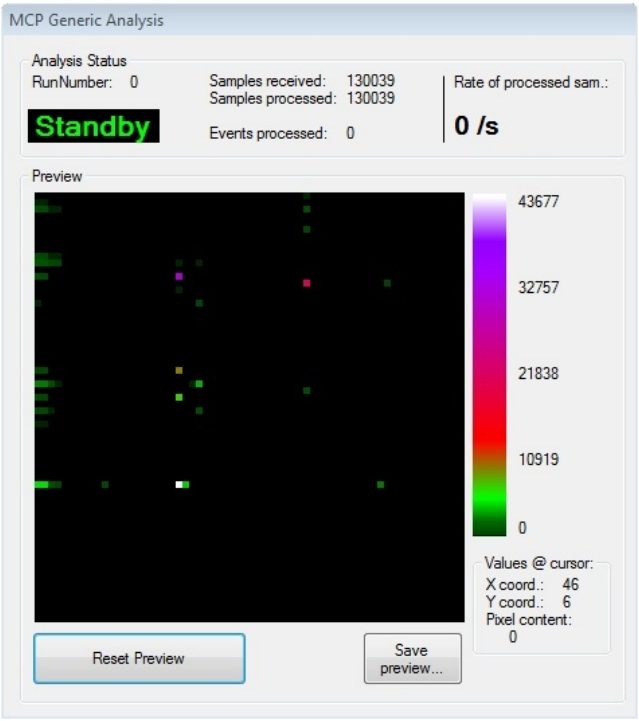

Figure 4.20.: The `GenericAnalysisForm` GUI.

and by the software are each incremented in an array with the dimension of 64 by 64. Each element of these arrays corresponds to a pixel of a raw image of the cross strip anode MCP detector readout. If the coordinates of the maximum charge information do not match, the raw data of the corresponding sample is saved to a text file for later consultation.

The raw picture of the location of the maximum ADC values of each sample that was identified by the VHDL firmware design is shown on the `GenericAnalysisForm` graphical user interface as a preview bitmap (Figure 4.20). Its content is updated regularly and can be reset via a button on the `GenericAnalysisForm`. The counts in each pixel is color coded. The color of the preview image is calculated on each update of the picture and by this also the color scale is adjusted to the pixel that has the largest content. A color bar next to the picture indicates the content of the pixels in the preview picture. The mouse cursor can be hovered over the picture and when doing this, the coordinate as well as the content of the pixel on which the cursor is pointing at is shown in a separate field of the `GenericAnalysisForm` graphical user interface. The preview image on the `GenericAnalysisForm` can be saved to a bitmap file.

The `GenericAnalysisForm` furthermore indicates the processing status of the `GenericAnalysis` on several labels which indicate the number of samples that have been received and processed as well.

The `GenericAnalysis` can not be controlled by the user directly in the current implementation but gets into action whenever a sample is available in the input queue of the `GenericAnalysis` that has been passed by the `DataServer`.

When the control software is terminated by the user, the content of the arrays that represent the raw pictures which have been determined by both the electronics and the software, are saved to a text file each. All the other text files of the `GenericAnalysis` are flushed and closed at this moment, too. In the current implementation, the software has to be restarted to do the storage of the data into a new file. For this, the data files that are generated by the control and analysis software must be copied manually to another directory after the software was closed.

5. Readout electronics tests and characterization

This chapter describes the tests and measurements that were performed in this work to validate the function of the MCP detector readout electronics. A series of test setups were used that have been developed especially to characterize the specifications of the electronics. Two main parts can be identified here, of which the first one is a device to inject charge pulses into the `Beetle` preamplifier chip as well as onto the electrodes of anodes for test purposes. The charge injector device was designed, developed, and manufactured at the beginning of this work. The second major part in the experimental test setup is a vacuum chamber that contains an MCP detector under vacuum conditions. The purpose of the vacuum chamber is to test the electronics under realistic conditions and furthermore to condition the MCPs for their subsequent installation into the sealed detector tubes.

The commissioning of the `Beetle` chip was the first milestone achieved. For this, specific modules of the FPGA VHDL firmware design had to be implemented and validated in function under realistic conditions. A deeper understanding of the `Beetle` chip control and operation was the outcome of these tests and the tests have been done by means of a small readout setup. It was successively upgraded to approach conditions where a detector tube is installed in front of the readout electronics. For this, tests with injected charges onto two anode versions and tests by means of the setup inside of the vacuum chamber have been performed. Prior to the design and assembly of the `Beetle` ceramics hybrid carrier (CHC) board, tests were performed with a reduced number of `Beetle` chip input signals.

The proper function of the FPGA VHDL firmware design, in particular the readout and control of the `Beetle` chip, the ADC management, and the communication to the back-end, could be validated for realistic readout conditions.

The chapter starts with a description of the charge injector device developed and manufactured in this work as well as a description of the

setup that is enclosed in the vacuum chamber. Following this, the tests and measurements to prove the function of the readout electronics are described.

5.1. Setups for the test and characterization of the readout electronics

As the development of the MCP detector tubes had been started in parallel to this work, no complete one (as described in Section 3.1) was available for test purposes during the readout electronics development phase. To be decoupled from the progress of the detector tube and photocathode investigation, a concept to support the readout electronics development by utilizing specialized test setups was realized. As the `Beetle` pre-amplifier chip is a complex integrated circuit, we had to start with its understanding and commissioning. After that, further progress could be made.

5.1.1. Description of the readout electronics setups

Initial setup

The initial setup consists of a charge injector device, the `Beetle` daughterboard from MPIK Heidelberg, and the front-end electronics FPGA board. It is shown in Figure 5.1.

The charge injector was designed and manufactured to be able to provide test pulses to a `Beetle` chip. The central component is a Xilinx `Spartan-3` FPGA and it uses `ADV7123` DACs in order to generate up to 10 programmable voltage jumps being coupled into a `Beetle` chip. A trigger signal is provided furthermore by the charge injector. The output parameters of the charge injector can be altered by software that is described in detail in Section 5.1.2.

Following the charge injector in the initial readout setup, a `Beetle` chip resides on a stacked assembly of printed circuit boards. The motherboard of this assembly was designed at IAAT. On top of it, a daughterboard that was designed and manufactured at MPIK in Heidelberg, is stacked. On this board, up to two `Beetle` chips can be mounted and up to 10 of their inputs can be bonded and used for test applications. In the initial readout setup, one `Beetle` chip is connected to the charge injector in this way.

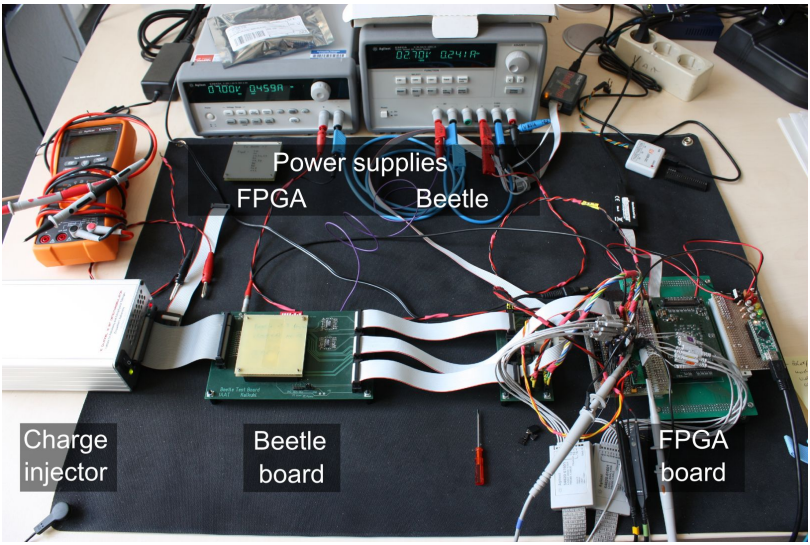

Figure 5.1.: The initial readout setup used for the commissioning of the `Beetle` chip and the development of the `Spartan-3` VHDL firmware design. Left: charge injector that provides charge signals to 10 `Beetle` chip inputs. Middle: a `Beetle` chip is mounted on a daughterboard stacked on a motherboard. Right: front-end electronics FPGA board where an ADC, FPGA, and a USB interface chip are located. Taken from Pfeifer et al. (2014a), modified.

Before the front-end electronics FPGA board of the readout electronics was implemented, the Beetle chip could be operated by a small test interface assembly replacing the front-end electronics FPGA board so far. It provided the power supply and a clock signal, among other signals, to the Beetle chip. The configuration via I^2C was tested by a commercial USB to I^2C converter which was controlled by software commands. This was the very first step to commission the Beetle chip and to understand its operation.

The front-end electronics FPGA board is the final stage in the readout electronics chain and the FPGA VHDL firmware design (Section 4.4) as well as the front-end electronics FPGA board have been manufactured gradually. The configuration of the Beetle chip via a custom-made I^2C -interface module in the FPGA VHDL firmware design was realized first. For this, default Beetle chip settings stored into a RAM in the FPGA have been used. A USB interface module was implemented in the FPGA VHDL firmware after that. It allowed for a configuration of the Beetle chip to settings selected in software and then sent to the readout electronics via a command. As the last part, the AD9649 ADC was integrated in the setup as well as in the Spartan-3 VHDL firmware design. The implementation of the data pipeline in three versions that provide different data complexity was done in parallel.

The initial readout setup was replaced during this work and the components have been connected to a laboratory setup.

Laboratory setup

The MCP detector readout electronics laboratory equipment that was set up at the time of this work is shown in Figure 5.2. A vacuum chamber accompanies the components used already in the initial readout setup. In the chamber, a vacuum environment of below 10^{-6} mbar can be achieved. It is designed for the conditioning of the MCPs that are integrated later in the detector tubes and to provide realistic signals to the readout electronics. For this, a stack of two MCPs, an anode, and a Beetle chip for signal pre-amplification are installed into the chamber. The MCPs in the stack can be illuminated by a UV lamp from outside the chamber through a quartz window and a high voltage supply for the operation of the MCPs is available. The setup in the vacuum chamber is described in detail in Section 5.1.3.

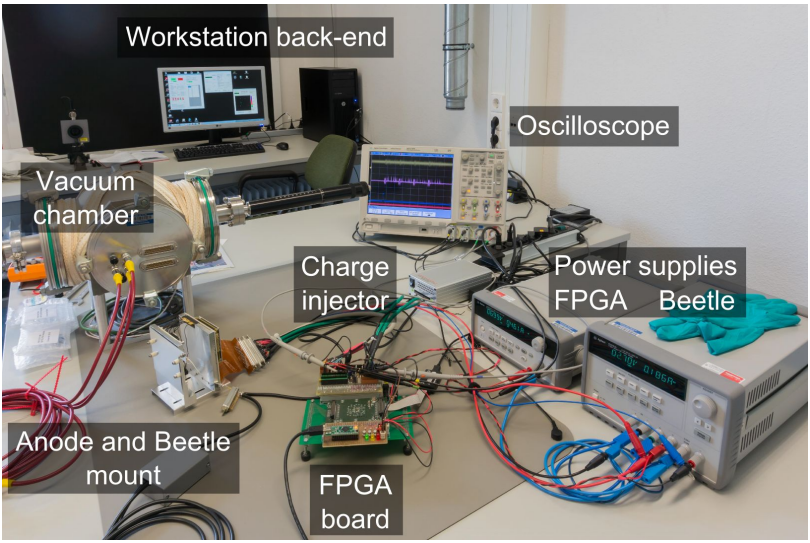

Figure 5.2.: The MCP detector readout electronics laboratory setup. The vacuum chamber on the left-hand side houses the setup shown in Figure 5.7. It provides signals from a stack of MCPs which are pre-amplified by a `Beetle` chip. Two vacuum feedthroughs are the interface to the readout electronics. For initial tests, the charge injector located in the center was used. In the front, the front-end electronics FPGA board of the readout electronics is seen. Control and readout of the electronics is performed by readout and analysis software which is installed on the back-end PC shown in the back of the picture. Two power supplies for the `Beetle` chip and the readout electronics exhibit a power dissipation of approximately 3.8 W including dissipation due to voltage regulators in front of the electronics. Taken from Pfeifer et al. (2014b), modified.

For further tests, the charge injector can be used to provide either a trigger signal to a Beetle chip or to provide test pulses onto an anode which is located outside the vacuum chamber, or both.

The front-end electronics FPGA board of the readout electronics as well as the Beetle chip are supplied by two laboratory power supplies.

The front-end electronics FPGA board performs the control and the readout of the Beetle chip via the ADC. Commands are sent to and received from a laboratory PC on which readout and control software is installed.

5.1.2. Charge injector

In this section, the charge injector that was developed to stimulate the readout electronics setups is described in detail. The PCB of the charge injector is shown in Figure 5.3. The connection schemes and the PCB layout can be found in Appendix A.2.1. A Xilinx Spartan-3 1000 FPGA is the central component. It is mounted on a micro module PCB. The Spartan-3 VHDL firmware design controls five ADV7123 DACs to provide 10 voltage jumps at the charge injector output and furthermore a trigger voltage signal. As the ADV7123 is a current source, the output is the voltage drop caused by the current driven across a resistor. The parameters of the outputs and the trigger signal can be selected in certain limits as well as the trigger latency relative to the voltage jumps. For this, the charge injector FPGA VHDL firmware design implements an interface to a USB interface chip. Commands for the output parameter configuration and run control are received via this interface from software on a PC.

Three control LEDs allow to supervise the power up and configuration sequence as well as the output activity status. A JTAG interface allows to program the Spartan-3 FPGA and to program a flash memory that stores the VHDL firmware design for a power-up configuration of the FPGA. The power supply of the components on the PCB is a single 7 V to 12 V power plug and two regulators power the Spartan-3 FPGA and the ADV7123 DACs on separate power lanes. The PCB layout comprises four layers which are a top and bottom signal layer, a ground plane and a power distribution layer. The PCB is enclosed in a housing and the charge injector can be switched on and off by a power switch. A fan for air cooling is included at the back of the housing and supplied when the power is switched on.

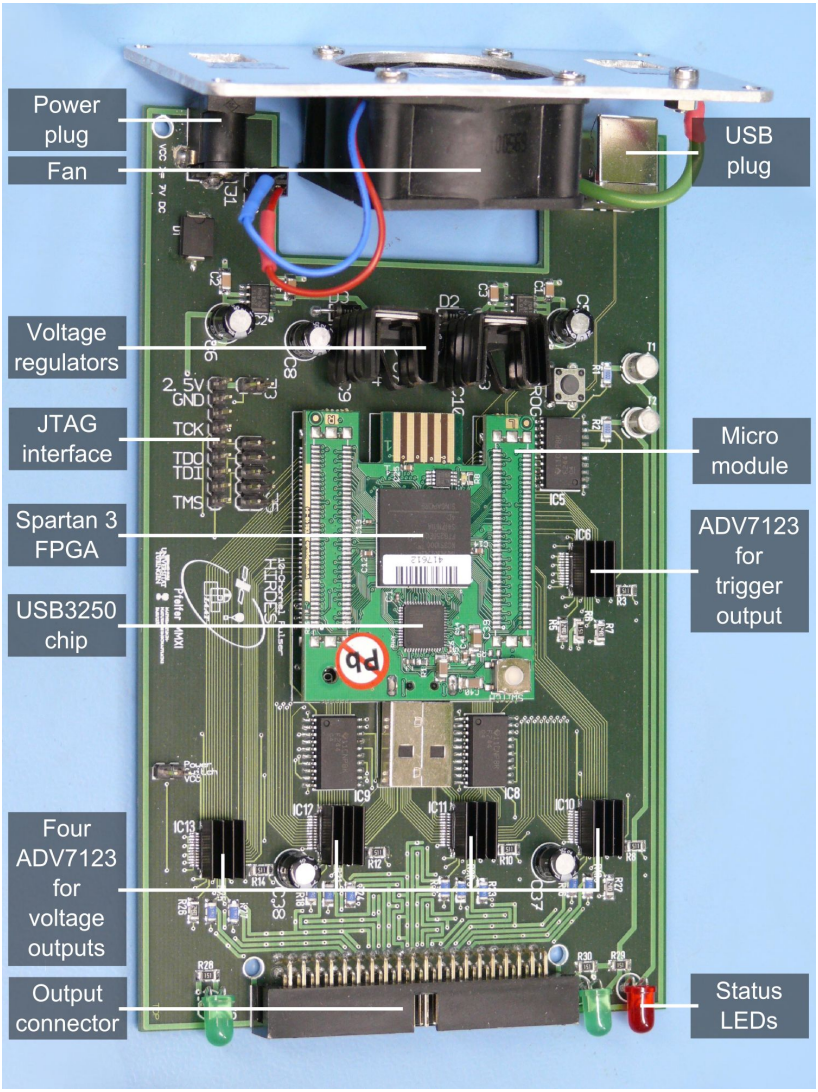

Figure 5.3.: The 160 mm by 100 mm charge injector assembly.

The charge injector connection scheme, the PCB layout, and the housing have been designed and manufactured during this work. Also the Spartan-3 VHDL firmware design and the control software have been designed and implemented.

Spartan-3 FPGA and Trenz micro module

The Spartan-3 FPGA is the central control component of the charge injector and is soldered on a micro module designed by Trenz Electronic GmbH[1].

The Spartan-3 FPGA is designed by Xilinx, Inc.[2]. Due to the low cost of the Spartan-3 FPGA, it is widely used also in a variety of consumer applications. The Spartan-3 1000 is a subversion that has 17 280 logic cells and 391 user I/Os. It features 120 kbit of distributed RAM as well as 432 kbit of Block RAM (Xilinx Inc., 2013).

As it provides an easy access to the I/O pins of the Spartan-3 FPGA, the TE0140-04BA micro module is used to operate the charge injector. A flash memory is mounted onto the micro module to store the VHDL firmware design that can then be loaded automatically in the Spartan-3 FPGA on power-up. An USB3250 USB transceiver chip from Microchip Technology, Inc.[3] is also mounted onto the micro module and connected to the Spartan-3 FPGA. Voltage regulators on the micro module convert a single 5 V power supply to the necessary voltages for the Spartan-3 FPGA core and I/O banks as well as for the other components on the micro module. 120 I/O pins of the Spartan-3 FPGA are accessible by two connectors of the micro module (Trenz Elektronik GmbH, 2008).

ADV7123 DAC

The ADV7123 is a triple 10 bit high speed video digital-to-analog converter (DAC) from Analog Devices, Inc.[4]. It provides a maximum output current of 18.5 mA on each of its three channels (Analog Devices, Inc., 2010).

[1] http://www.trenz-electronic.de/de/produkte/fpga-boards/trenz-electronic/te0140-spartan-3-series.html
[2] http://www.xilinx.com/products/silicon-devices/fpga/spartan-3.html
[3] http://www.microchip.com/wwwproducts/Devices.aspx?product=USB3250
[4] http://www.analog.com/en/audiovideo-products/video-encoders/adv7123/products/product.html

Table 5.1.: Output specifications of the charge injector. They are illustrated in Figure 5.4.

Parameter	Min	Max	Δ	Unit
Voltage outputs				
Output voltage	0.0	0.94	0.92×10^{-3}	V
Event rate	1.0	1000.0		$\times 10^3\,\mathrm{s}^{-1}$
Mean value	0	1023	1	DAC chn
Ramp-time	0.5	1000.0		µs
Trigger output				
Active value	0	1023	1	DAC chn
Inactive value	0	1023	1	DAC chn
Delay	0	10^6	16	ns
Duration	0	10^6	16	ns

Five of these DACs are used for the charge injector where four provide 10 voltage outputs and one provides the trigger output. The former are controlled and synchronized via two double driver/buffer ICs that are driven by the `Spartan-3` FPGA. The latter is controlled separately to realize an adjustable duration and delay of the trigger signal with respect to the voltage outputs. The current output of the `ADV7123` is driven across a 51 Ω and a 150 Ω resistor for the trigger output, respectively. Table 5.1 shows the resulting output voltages and further specifications of the charge injector. The charge injector output shape and the specifications are illustrated in Figure 5.4.

Charge injector `Spartan-3` VHDL firmware design

The top level structure of the charge injector VHDL firmware design is shown in Figure 5.5.

A command decoder module (CDM) is the central control entity in the design. It decodes commands from the back-end which can be either commands for output activity control or commands for the configuration of the output parameters of the charge injector like the rate, height and polarity of the output voltage jumps. An overview of the packet structure

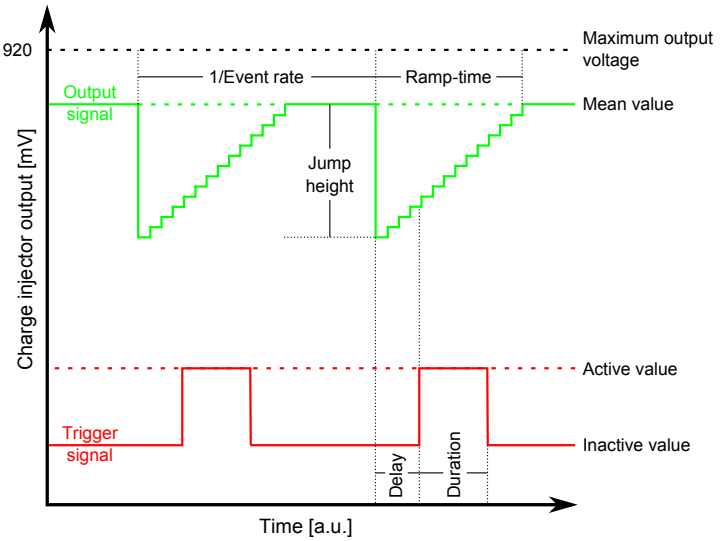

Figure 5.4.: The output shape and parameters of the charge injector.

and available commands is given in Figure A.8 and Table A.7 in the Appendix A.2.2. The identifier byte from Table A.7 is expected to be followed by the least significant byte and the upper byte of a 16 bit value for the specific parameter that is to be modified. The CDM provides all the parameters for the output behavior as bit-vectors to an event generator module (EGM). Commands from the back-end are acknowledged by the CDM. The output activity control is done from the CDM via simple reset signals that are connected to the residual modules of the `Spartan-3` VHDL firmware design.

Commands from the back-end enter the design via a USB serial core designed by Trenz Elektronik GmbH which is the interface to the `USB3250` USB chip. Transfers from the serial core into the `Spartan-3` VHDL firmware design and vice versa are performed byte-wise in a FIFO fashion and is supported by handshake signals.

The information of subsequent output voltage step heights is stored into a RAM in the `Spartan-3` VHDL firmware design. It can keep up to 3900 events that are arranged as clusters of 10 consecutive 10 bit memory

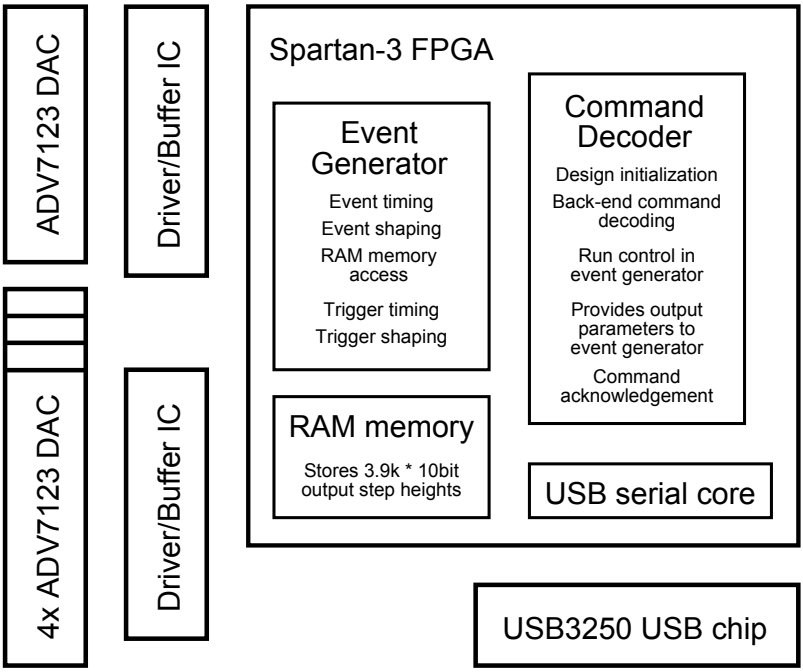

Figure 5.5.: A top level module overview of the `Spartan-3` VHDL firmware design and the connected ICs.

locations for the 10 output channels. To store the information in the memory, the CDM gains memory access from the EGM when a command from the back-end contains a value to be stored in the RAM.

When the output of the charge injector is active, the EGM reads the information for the output steps from the RAM as a ten-fold cluster of memory locations. If no further event is stored in the RAM, the previous information is read again beginning from the first memory location and hence the output pattern is repeated. According to the configuration that is encoded in bit-vectors which are provided by the CDM to the EGM, the output mean value, the recovery time, and the quiescence between subsequent events is formed by the EGM between the voltage jumps. The trigger signal is shaped in a separate process in the EGM. The delay of the signal with respect to the event output, the trigger duration and the output mean and active value are also encoded in bit-vectors that are provided by the CDM.

The EGM configures each of the 10 output channels of the `ADV7123` at 10 bit resolution. To synchronize the outputs of the `ADV7123`, the control signals for them are generated by distribution of a single signal from the `Spartan-3` FPGA in separate driver ICs. The trigger output is resolved with 10 bit as well. The `ADV7123` for this output is controlled via separate control signals from the `Spartan-3` FPGA independent of the four `ADV7123` DACs that form the voltage outputs.

Control software

The charge injector is controlled via a software installed on a PC. It was also implemented in the frame of this work. A screenshot of the user interface of the software is shown in Figure 5.6. The software is implemented in `C#` in the frame of the Microsoft `.NET`-framework. The communication to the `USB3250` USB chip is encapsulated in the `LibUsbDotNet C#` USB library[5]. The library is open source and free of charge. It allows access to USB devices independent of the specific driver and the operating system.

During the start of the software, the connection to the charge injector is initialized and a warning is given if the charge injector can not be found at one of the USB ports of the computer. Default values for the output behavior are written to the charge injector after the connection was

[5] http://sourceforge.net/projects/libusbdotnet/

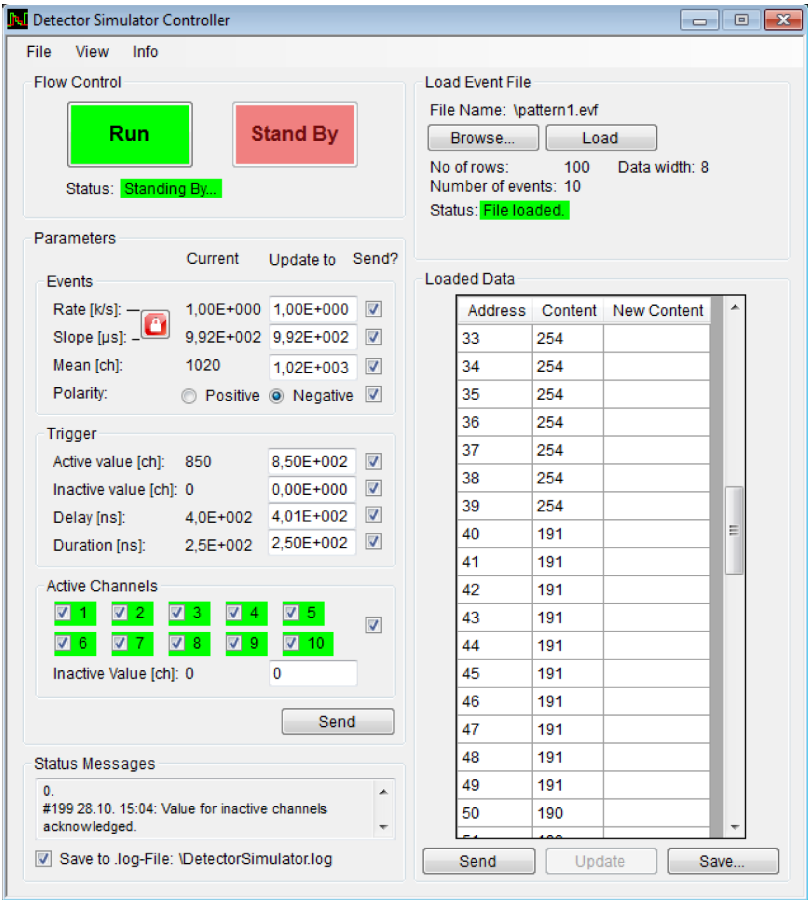

Figure 5.6.: The charge injector control software GUI.

established and the charge injector is put in standby mode. For a proper initialization of the USB connection from the charge injector to the PC, the charge injector has to be powered-up without the USB cable connected. On power-up, the FPGA and by this also the USB serial VHDL module and the USB chip are configured. After that, the USB interface of the charge injector is ready for operation and the USB cable can be connected.

The control software allows to start and stop the output activity of the charge injector by two buttons. If the charge injector is not active, the output parameters can be altered via input fields on the user interface and sent to the charge injector subsequently. The software performs the conversion of the parameters from physical units to units that are understood by the `Spartan-3` VHDL firmware design. This can be the conversion of the event rate per second into the spacing of two subsequent events in units of numbers of periods of the `Spartan-3` VHDL firmware design global clock for example. The user input is checked for plausibility and conformity with the limits that are given by the implementation of the charge injector shown in Table 5.1.

The voltage step height of the charge injector output events are read by the software from a human-readable text file. The necessary structure of this file is shown in Figure A.9 of Appendix A.2.3. The file has to start with an identification string to assure that a proper file is selected. Following this string, a set of four parameters must be given. This is intended to allow the software to support different possible implementations of the charge injector with differing output numbers or bit-widths of the DAC data. After that, the event information is written into the file where each line has to hold the value for the step height of one output channel.

The charge injector control software provides a tool to create, manipulate and store event files. Predefined event files can be read into a matrix representation that shows up on the user interface of the software. The content of the matrix can be altered and sent to the charge injector for its output configuration. To support an easy repeatability of measurements, the content of the configuration matrix can be stored to an existing or new event file on demand.

The overall configuration of the charge injector and furthermore the location of the event file that was loaded for a specific measurement can be stored to a file on the hard disk of the PC and can be recalled later on. By this, a fast repeatability of measurements is assured.

All activity of the software and hence also the USB traffic to the charge

injector is recorded in a .log file. The name and location of the file can be selected by the user. In this way, the information of the charge injector output parameters that have been applied in a certain measurement is stored in addition to the configuration file for a later consultation.

5.1.3. Setup in the vacuum chamber

A setup in a vacuum chamber was designed at IAAT for the burn-in of MCPs that are installed in the MCP detector tubes later. The burn-in process is intended to clean the MCPs from residuals and contaminations and condition them for use. The latter means that a certain amount of charge has to be extracted from the MCPs until the gain of them stabilizes.

Furthermore, the setup in the vacuum chamber is intended to test the readout electronics as long as the detector tube development is still in progress. The setup provides more realistic conditions compared to the stimulation of the `Beetle` chip directly or an anode in front of it via the charge injector. In addition, the setup in the vacuum chamber allows to determine the optimal values for the operational parameters of the components of the MCP detectors. The parameters are for example the high voltage across the MCPs in a stack or the spacing between an MCP stack and an anode.

Figure 5.7 shows the initial setup in the vacuum chamber prior to the installation of a `Beetle` CHC board and a cross strip anode. The setup is mounted on a vacuum flange and in this way it is inserted and placed into the vacuum chamber. A stack of two MCPs is followed by a wedge and strip anode in the initial vacuum chamber setup. A `Beetle` chip is mounted onto a revision of the motherboard that was already used in the initial readout setup (Figure 5.1). A `Beetle` chip on a daughterboard from MPIK pre-amplifies the signals of the wedge and strip anode. Digital and analog signals as well as supply voltages are interfaced by two connectors from outside the vacuum chamber. High voltages are supplied by dedicated feed-throughs. In front of the setup, an electron generator MCP is mounted to irradiate the MCPs in the stack with a uniform electron flux that is emitted when a high voltage is applied to the electron generator MCP. To alternatively illuminate the MCP stack using a UV lamp outside the vacuum chamber, the electron generator MCP is tiltable and a quartz window is mounted on one side of the chamber in opposite of the feed-throughs.

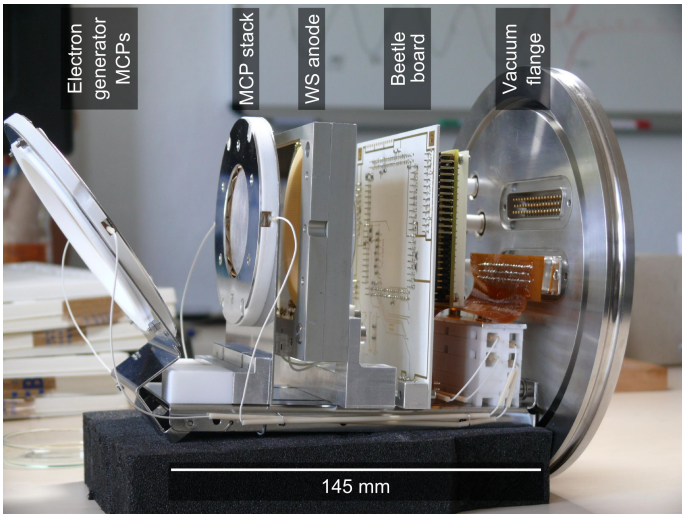

Figure 5.7.: Setup in the vacuum chamber. Modified from Pfeifer et al. (2014a).

To improve the setup in the vacuum chamber, mounts for a cross strip anode and a `Beetle` CHC board are available. The wedge and strip anode and the `Beetle` motherboard will be replaced by a cross strip anode and a `Beetle` CHC board. The advanced setup will be very close to the readout configuration in the MCP detector sealed tube and the readout electronics as well as the spatial and electrical parameters of the setup can be optimized.

5.2. Tests and characterization of the readout electronics

A series of test and verification measurements accompanied the development of the readout electronics setup in this work. This section gives an overview of the measurements and presents data that have been acquired and analyzed in this work to verify the function of the readout electronics setup.

The readout electronics development started with the commissioning of the `Beetle` chip using a commercial USB to I^2C-converter and a test

interface that provided the most important signals to the Beetle chip. The communication as well as the behavior of the chip was supervised by use of an oscilloscope and a logic analyzer. Following this, the Virtex-4 VHDL firmware design (Section 4.4) implementation was started and the central state machine as well as an I^2C master core have been implemented, simulated and tested with a Beetle chip. At the beginning, the Beetle chip was configured with a default set of I^2C-parameters stored in a RAM in the FPGA.

To be able to alter the front-end parameters of the Beetle chip dynamically via a command from a PC, the USB interface was manufactured and the USB communicator module in the Virtex-4 VHDL firmware design was implemented, simulated, commissioned, and tested. The control software packet development started at this time.

The control and readout of the ADC was the next step in the development procedure. The corresponding ADC manager module in the Virtex-4 VHDL firmware design was implemented, simulated and tested via the ADC interface board. It was followed by the implementation of the ADC data handling, buffering, and processing by the ADC manager as well as the sample buffer and data pipeline modules in the Virtex-4 FPGA.

Prior to the test of a specific function in the actual readout setup, the proper behavior of the feature in the Virtex-4 VHDL firmware design was tested using a VHDL test bench which operates the Virtex-4 VHDL firmware design in a simulated environment. A goal of this work was to provide a VHDL test bench that is capable to simulate control commands to the Virtex-4 VHDL firmware design, provide simulated external clocks from the FT232H USB chip and AD9649 ADC, and furthermore can provide the necessary signals to simulate the readout of the Beetle chip via the ADC. The data that are processed in the test bench as well as virtual trigger patterns are read from human-readable text files. The test bench is a full environment to study the Virtex-4 VHDL firmware design under determined conditions although differences to the application in the real world are always present.

In the following, results of the most important measurements that have been performed in this work are shown.The data that have been stored by the control and first-level analysis software (Section 4.5) have been further analyzed using the Interactive Data Language (IDL)[6].

[6]A programming language which is used for data analysis and image processing. It is

5.2.1. Direct charge injection into a Beetle chip

The charge injector was used in the initial readout setup to test the proper function of the readout electronics. After all components had been installed and the Virtex-4 VHDL firmware design was completed, a full Beetle chip readout sequence could be acquired and stored.

Figure 5.8 shows a readout sequence of four consecutive samples of one event that was coupled into a Beetle 1.3 via the charge injector. The Beetle chip is mounted on a daughterboard from MPIK Heidelberg. A 1 pF capacitor is installed on the daughterboard in front of each bonded Beetle chip input. The charge injector applies a voltage jump to the connected capacitors and hence couples charge into the Beetle chip inputs. Charge was coupled into two (channel numbers 18 and 93) of ten bonded Beetle chip inputs. The readout is done by one Beetle output port and the data is digitized by one ADC. The readout sequence is triggered by the charge injector trigger output. The gaps in the readout sequence that can be seen in Figure 5.8 between the individual samples are due to the fact that the Beetle chip readout header is not shown. The header bits are acquired but presently not processed further in the FPGA.

Figure 5.8 shows the characteristic baseline behavior that was found by Löchner (2006) for the version 1.3 of the Beetle chip. It was discussed in Section 4.2 and is shown in Figure 4.7. The baseline is inverted in Figure 4.7 compared to the measurement shown in this section due to the inverting driver stage which follows the Beetle chip output on the IAAT Beetle motherboard. The baseline characteristics are equal nevertheless. It has a slope as a function of the Beetle chip channel number which is driven off the chip. In addition, the slope is smaller for the first sample than for the following samples if a consecutive sequence of samples is driven off the Beetle chip.

All events of the measurement of which Figure 5.8 shows only one single event have been analyzed further. Figure 5.9 shows two plots. Each plot spans a plane of the ADC output versus the Beetle channel number. The color of each pixel in the plane encodes the counts of a certain ADC output pulse height for a given Beetle chip input channel number taking all samples of the measurement into account. The ADC output axis is rescaled and only the eight most significant bit of each ADC output pulse

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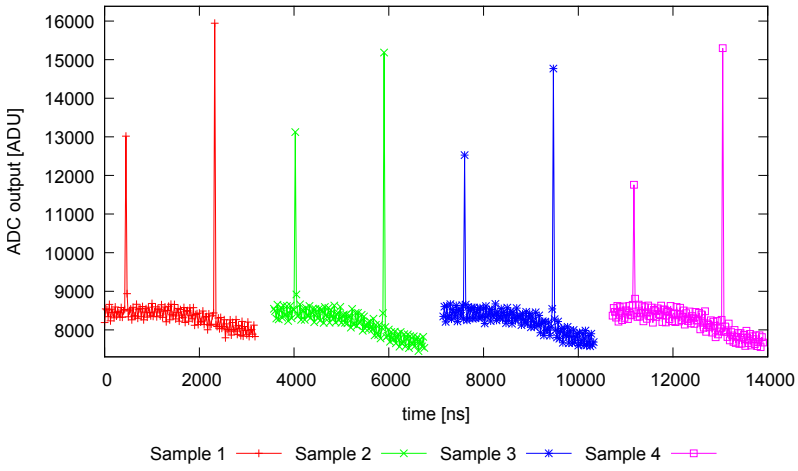

Figure 5.8.: A `Beetle` chip readout sequence using the initial readout setup and version 1.3 of the chip.

height are considered. To be able to illustrate the region of small event frequencies, the right plot shows only the ADC output versus the `Beetle` chip channel number in a range between 0 and 255.

As expected, only two spots above the baseline can be seen in the plots of Figure 5.9 which are located at the `Beetle` channel numbers 18 and 93 into which an input charge was injected. The baseline shows again the characteristic slope of the `Beetle 1.3`. In addition, the baseline spread between consecutive and non-consecutive readouts shows up in Figure 5.9 beginning from around channel number 80 as a widening of the baseline and two color shades. The colors correspond to a one in four ratio of non-consecutive to consecutive readouts as it is the case for a readout of four samples for each triggered event. The small spikes that show up next to the channel numbers into which a charge was injected, are most likely due to cross-talk between the channels.

The plots in Figure 5.10 show a cut through the plane of the left plot in Figure 5.9 for fixed channel numbers 18 and 93 in black and a Gaussian fit in green. The width of the distribution is caused by noise and the fact that the `Beetle` chip sampling clock and the clock of the charge injector which

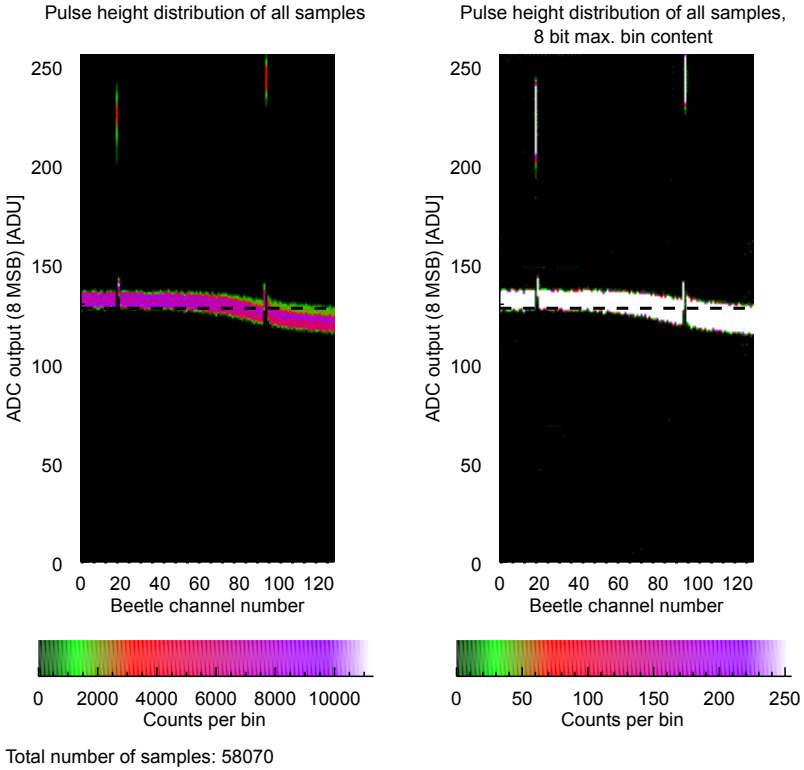

Figure 5.9.: Pulse height distribution as a function of the `Beetle` chip channels for all samples which have been acquired during this specific measurement. The charge injector couples charge into channels 18 and 93 of a `Beetle 1.3` in the initial readout setup. The ADC output spans the range from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$, the dashed line marks the numerical center of the ADC output range ($0\,\mathrm{V}$ input voltage amplitude).

triggers the readout are not yet synchronized at the time of this work. Hence, the sampling points on the output of the `Beetle` chip shaper into the chip's storage pipeline vary in a range of the `Beetle` chip sampling clock period and for this, the apparent input charge varies.

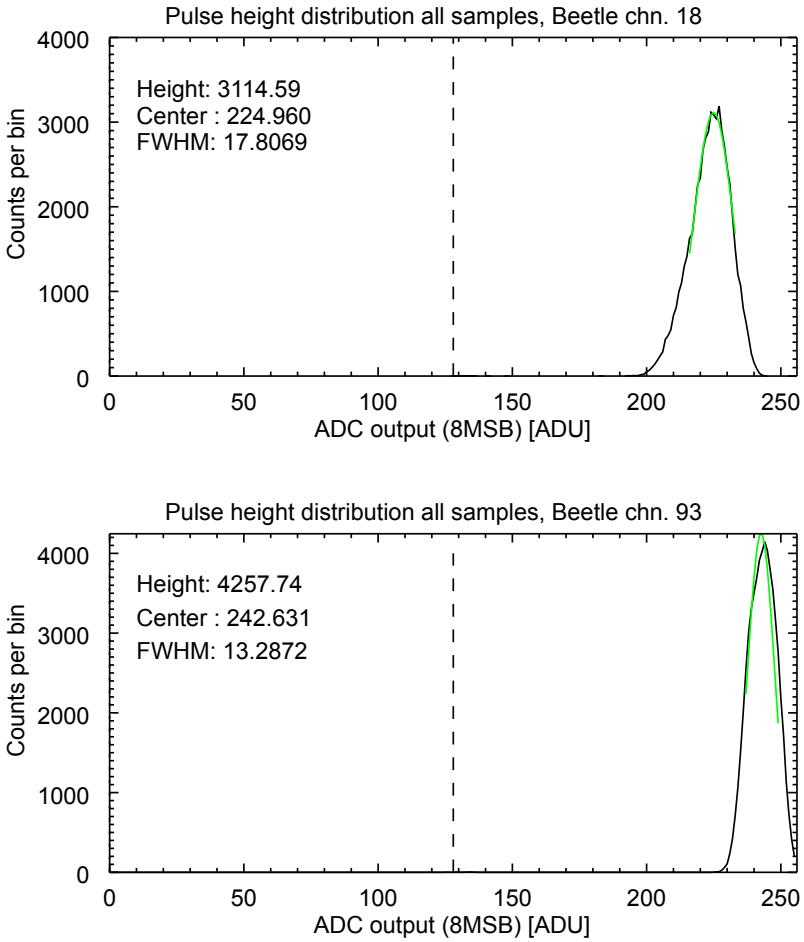

Figure 5.10.: Pulse height distribution of `Beetle` chip channels 18 and 93 for all samples of the the measurement in Figure 5.9 where the initial readout setup is used (black) and a Gaussian fit (green). The dashed line marks the numerical center of the ADC output for zero input signal amplitude.

Table 5.2.: Physical parameters of the test pulse electrodes of the WSA.

Parameter		Value	Unit
Absolute permittivity	ϵ_r	3.8	$\mathrm{F\,m^{-1}}$
Surface area	A	3.2	$\mathrm{cm^2}$
Thickness of substrate	d	5.0	mm
Capacity	C_{TPE}	4.37	pF

5.2.2. Charge injection onto a wedge and strip anode

On the rear side of the ORFEUS wedge and strip anodes (WSA) at IAAT, two test pulse electrodes for the injection of test charges onto the four electrodes of the anode are mounted. The test pulse electrodes are placed on two opposite corners of the rear side of the anode substrate and consist of chrome. The physical parameters of the test pulse electrodes are given in Table 5.2. The capacity C_{TPE} of each test pulse electrode through the quartz-substrate of the WSA against the electrode layer of the WSA was calculated at IAAT using the Finite Element simulation tool `FlexPDE 6`[7], to:

$$C_{\mathrm{TPE}} = 4.37 \times 10^{-12}\,\mathrm{F} \tag{5.1}$$

To do this, the geometry of the test pulse electrodes was assumed to be simply of rectangular shape and the area of the substrate and anode was assumed to be much larger than the area of the test pulse electrode itself. The amount of charge that is injected onto the electrodes of the WSA for a given voltage step of the charge injector connected to the test pulse electrode can be estimated via the output parameters of the charge injector given in Table 5.1. The results are given in Table 5.3.

Hence, a charge injector output voltage step height of 45 DAC channels corresponds to a charge of around $1.13 \times 10^6\,e$ that is injected onto the electrodes of the WSA. Parasitic capacitance is not taken into account here.

Figure 5.11 shows the pulse height distribution of data that have been acquired where the charge injector is attached to the test pulse electrode of a WSA. The output voltage step height of the charge injector is 45 DAC channels. The charge signal of the WSA is read out by a `Beetle` chip 1.5

[7]Distributed by PDE Solutions Inc.: http://pdesolutions.com/index.html

Table 5.3.: Parameters for the charge that is injected onto the electrodes of the WSA.

Parameter		Value	Unit
Maximum voltage step	$U_{\max}$	0.94	V
Maximum charge injected	$Q_{\max}$	4.1×10^{-12}	C
Maximum number of electrons	$N_{\max}$	2.6×10^{7}	e
Number of electrons per bit	N_{LSB}	2.5×10^{4}	e

mounted on an MPIK daughterboard. Wedges of the anode are connected to the input channels 90 and 121 of the `Beetle` chip, strips are connected to channels 94 and 107. The charge injector is connected to the test pulse electrode which shares most of its area with the wedge on channel 121 and the strip on channel 107. Earlier measurements in other setups show that around 85 % of the charge that is coupled into the test pulse electrode are induced equally into these electrodes while the electrodes on channels 90 and 94 receive the remaining charge. The expected charge ratio of the first to the latter electrodes is for this in the order of 6.

The improved baseline behavior of the `Beetle 1.5` is clearly visible in Figure 5.11 compared to the measurement shown in Figure 5.9 where a `Beetle 1.3` was applied. As can be seen from the pulse height distribution in Figure 5.11 and also from Figure 5.12, the four electrodes of the WSA show a nearly equal pulse height in contrary to the expectation of a 6:1 ratio, being most likely due to cross-talk. This assumption is supported by simulations of the setup that are reported in the next section.

Figure 5.13 plots the pulse height distribution in a plane of the pulse height sum of the two strips versus the pulse height sum of the two wedges. The pulse distribution concentrates around a line through the origin with a slope of unity. The center of the distribution is shifted to the direction of higher ADC outputs. Its shape in the scatter plot 5.13 can be interpreted as follows (Figure 5.14): the pulse distribution in the scatter plot forms an ellipse. The width of the ellipse along the semimajor axis projected to the axis of the plot is caused by signals that show up correlated in the plot. The nature of these signals can be either disturbing signals with an equal height on the four electrodes of the WSA or due to the fact that the sampling clock of the `Beetle` chip and the charge injector clock that

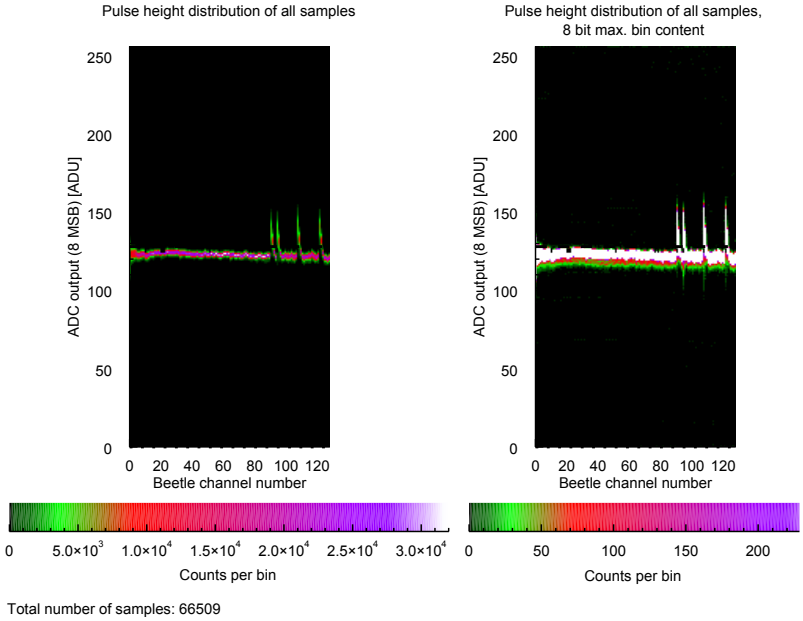

Figure 5.11.: Pulse height distribution of a measurement where the charge injector is coupled to the test pulse electrode of a WSA. Wedges of the anode are connected to the input channels 90 and 121 of a `Beetle` chip 1.5, strips are connected to input channels 94 and 107 of the chip. The charge injector output voltage step height is 45 DAC channels.

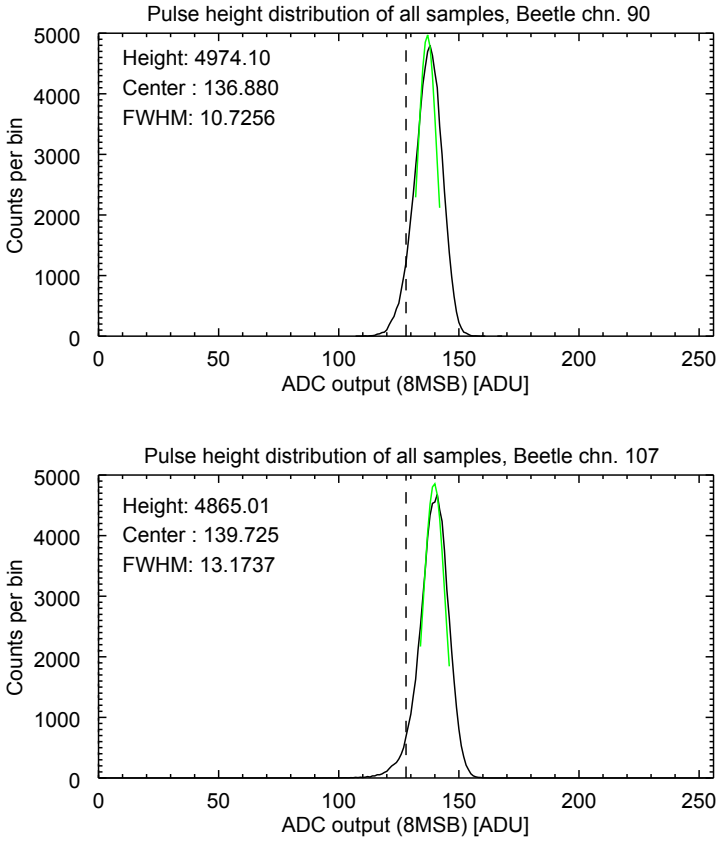

Figure 5.12.: Pulse height distribution of a measurement where the charge injector is coupled to the test pulse electrode of a WSA. `Beetle` input channel 90 corresponds to the wedge that is weakly coupled to the test pulse electrode, input channel 107 is connected to the strip which is coupled stronger to the test pulse electrode. The charge injector pulse height is 45 DAC channels. The expected ratio of the pulse height is in the order of 6.

updates the charge injector outputs are not synchronized as was already mentioned before. For this, the sampling points on the output of the `Beetle` chip shaper, and hence the apparent amount of injected charge, vary in a range of the `Beetle` chip sampling clock period.

The projection of a cut through the pulse distribution ellipse in parallel to the axis of the scatter plot (Figure 5.13) indicate an upper limit for the amount of uncorrelated noise on one axis for a given ADC output sum of the other axis. The uncorrelated noise is most likely pre-amplifier noise.

The concentration of the pulses in the scatter plot in Figure 5.13 on the line through the center with slope unity indicates a correlation of the pulses that are acquired in this measurement. This is expected as the charge injector triggers the readout electronics when it induces a charge on the WSA electrodes. The charge is equally split between the wedges and strips of the anode as expected for the test pulse electrode geometry and location.

The observed pulse height ratios and the shape of the ellipse in the scatter plot is the same if the voltage step height that is applied to the WSA is higher. This situation is shown in Figures 5.15, 5.16, and 5.17 for a charge injector output step height of 120 DAC channels. The plots show nevertheless that the pulse height depends on the amount of charge which is injected by the charge injector into the test pulse electrode of the WSA as it is expected. The ellipse in the scatter plot is shifted to higher ADC output values. The absence of pulses in the center of the scatter plot 5.17 for a larger output step height of the charge injector clearly shows that only events induced by the charge injector and no baseline events are acquired in this measurement.

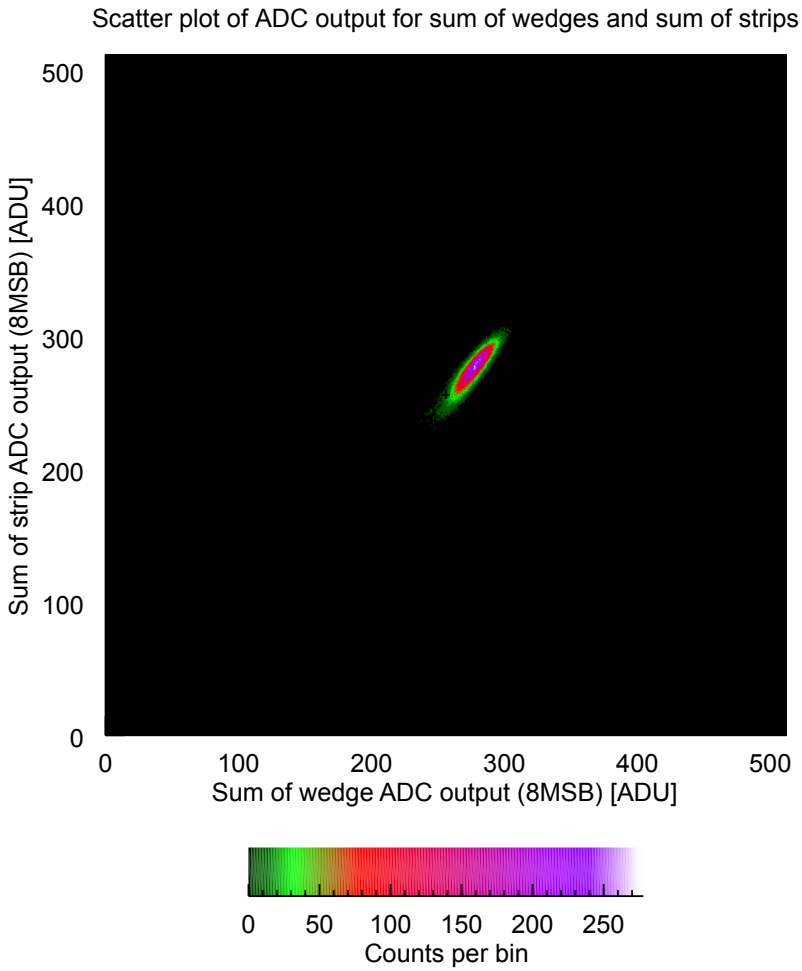

Figure 5.13.: Scatter plot of a measurement where the charge injector is connected to the test pulse electrode of a WSA. The charge injector pulse height is 45 DAC channels. The plot shows a plane of the pulse height sum on the strip versus the pulse height sum on the wedges of the WSA.

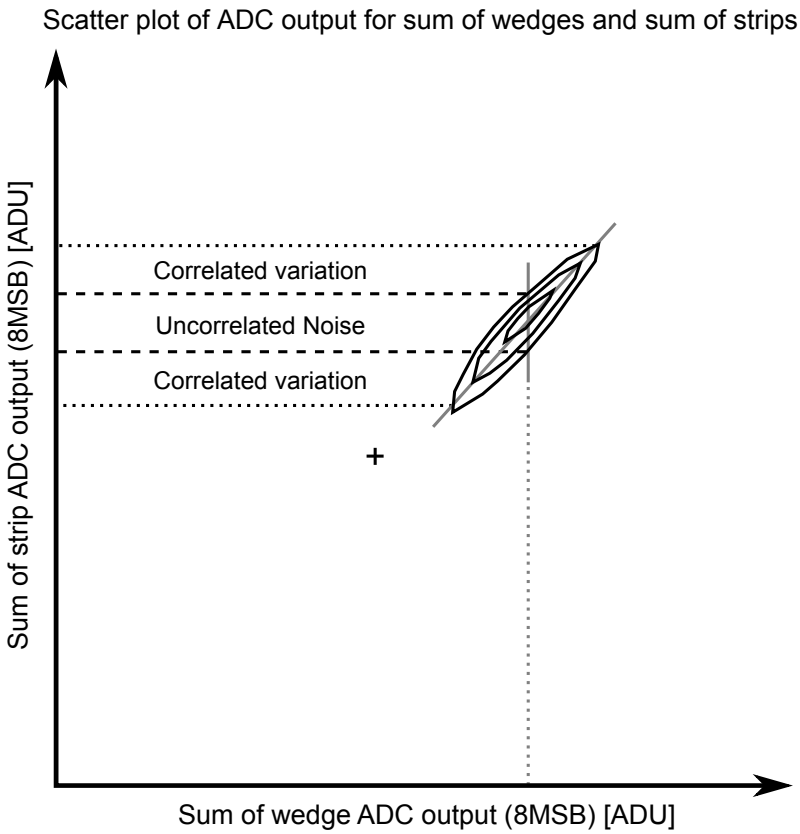

Figure 5.14.: Illustration of the influence of different factors on the shape of the scatter plot. The projection of a cut along the semimajor axis of the ellipse onto the axis of the plot indicates the correlated variations. The projections of a cut through the ellipse along one axis of the plot indicates an upper limit for uncorrelated noise distributions on this axis for a given value of the other axis. The illustrated projections are also valid for the axis of the wedge sum ADC output. The baseline location is indicated by the cross.

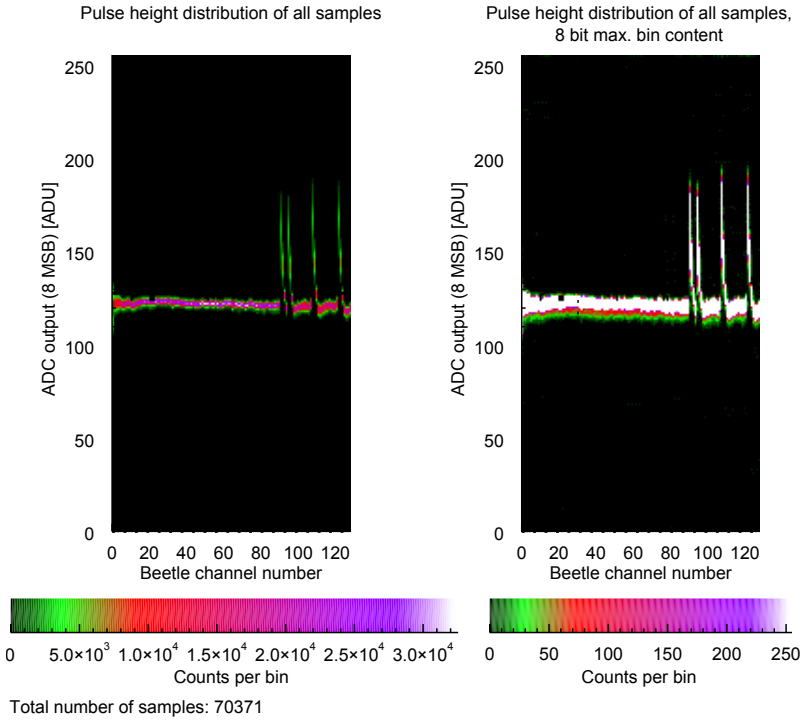

Figure 5.15.: Pulse height distribution for the same setup as in Figure 5.11. The charge injector output step height is 120 DAC channels for this measurement.

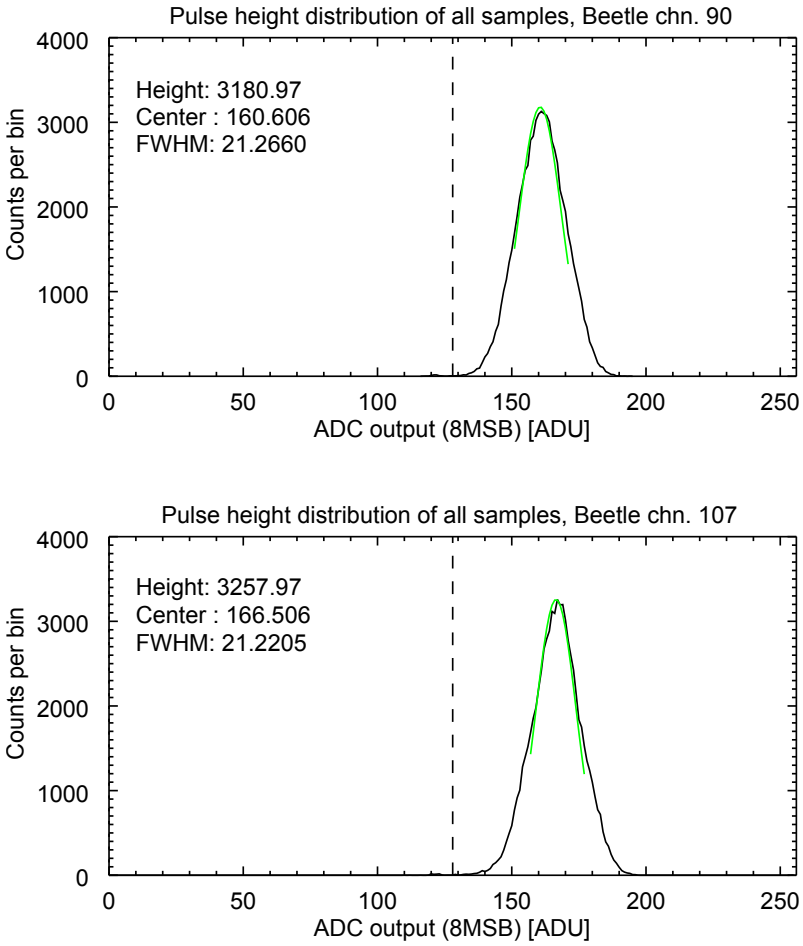

Figure 5.16.: Pulse height distribution for the same setup as in Figure 5.12. The charge injector output step height is 120 DAC channels for this measurement.

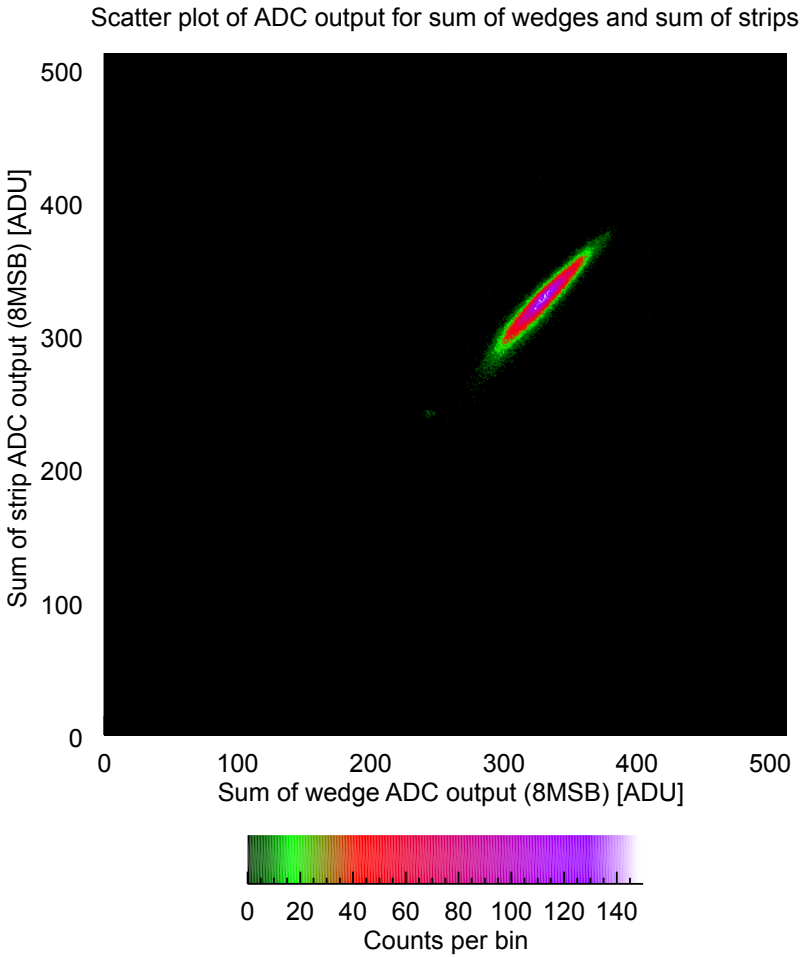

Figure 5.17.: Scatter plot for the same setup as in Figure 5.13. The charge injector output step height is 120 DAC channels for this measurement.

5.2.3. SPICE simulations of the charge injection into a WSA and an XSA

`LTSpiceIV`[8] is a tool to perform SPICE (Simulation program with integrated circuit emphasis)[9] simulations of analog electronic circuits. It was used in this work to simulate the interconnection of the charge injector with the test pulse electrode of a WSA and four `Beetle` chip input channels.

The small signal models of the `Beetle` front-end stages that are given by Löchner (2006) have been implemented into the simulation. A charge injector output step height of 5 DAC channels was simulated which corresponds to a charge amount of around $1.25 \times 10^5\, e$. The schematic that was simulated is shown in Figure A.10 of Appendix A.3. It contains the relative capacitance of the test pulse electrode to the separate electrodes of the WSA and in addition the measured capacitance of the electrodes with respect to each others. Four `Beetle` chip input channels have been considered. Figure 5.18 shows the simulated output of four `Beetle` chip shaper stages. It is clearly visible that the output of the `Beetle` chip front-end is nearly equal for the four channels despite the expectation that the output is around a factor 6 larger for the electrodes that are coupled stronger to the test pulse electrode of the WSA.

Due to the large capacitance of the anodes of the WSA in the order of 300 pF compared to the dynamic input capacitance C_m of the `Beetle` chip in the order of 6 pF, the charge response of the anode measured by `Beetle` is nearly equal for the four input channels to which the WSA is connected. This strongly supports that the measured discrepancy in the observed pulse heights in the measurement in the previous section are indeed due to cross-talk.

The dynamic input capacitance C_m of the `Beetle` chip was estimated considering the Miller-effect (Equation 5.2), using the feedback capacitance $C_\mathrm{fb} = 0.4006 \times 10^{-12}\,\mathrm{F}$ (Löchner, 2006), and the absolute value of the amplification $|A| \approx 14$ of the `Beetle` preamplifier as approximated from the simulated output of the `Beetle` chip pre-amplifier stage.

$$C_\mathrm{m} = C_\mathrm{fp} \times (1 + |A|) \tag{5.2}$$

[8] Provided by Linear Technology: `http://www.linear.com/designtools/software/`

[9] A general-purpose, open source analog electronic circuit simulator. It was developed by Nagel and Pederson (1973) at the University of California. SPICE is used to check the integrity of analog circuits and predict the behavior of circuit designs.

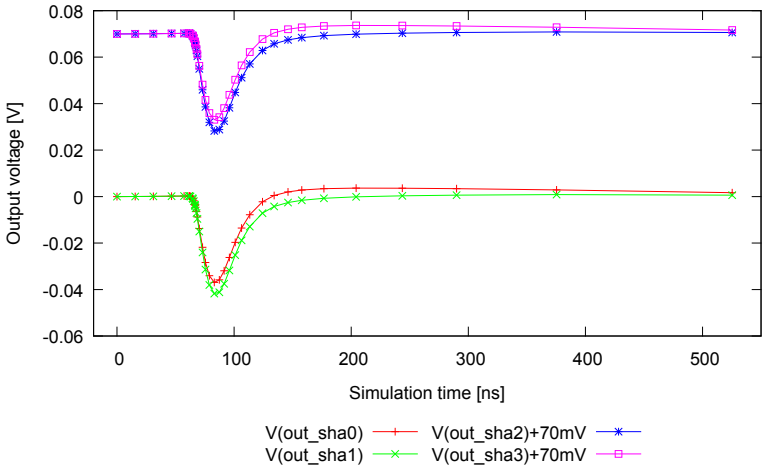

Figure 5.18.: A `LTSpiceIV` simulation of the output of four shaper stages in a `Beetle` chip when charge is injected into the test pulse electrode of a WSA which is connected to the four inputs of a `Beetle` chip. Output 3 and 4 are shifted for clarity.

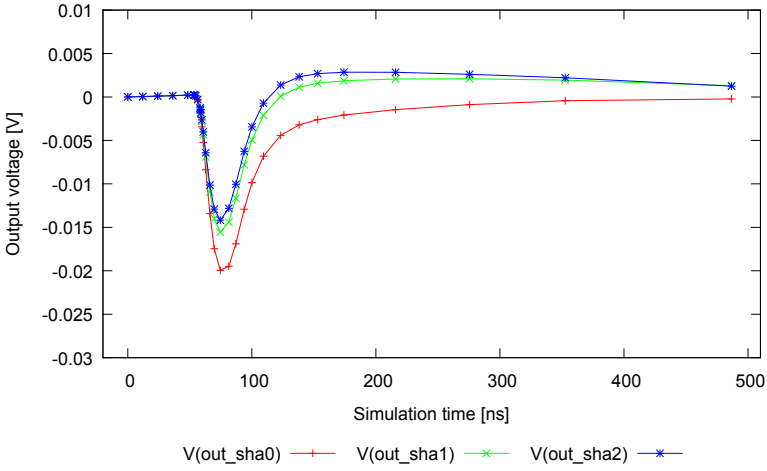

Figure 5.19.: A `LTSpiceIV` simulation of the output of three shaper stages of a `Beetle` chip where the electrodes of a WSA are connected to. Charge is injected only into one electrode of the WSA.

To illustrate the influence of the cross-talk between the electrodes of the WSA, Figure 5.19 shows the simulated `Beetle` chip front-end output of a configuration where the charge is virtually coupled only into one electrode of the WSA via the test pulse electrode. The schematic is shown in Figure A.10 of Appendix A.3. The parameters for the front-end stages and the charge injector step height are the same as in Figure 5.18. A fraction of the capacitance of the test impulse electrode was considered which is equal to the capacitance of the test impulse electrode to either a strip or a wedge that is coupled stronger to the test pulse electrode at one corner of the WSA. Figure 5.19 shows the output of three `Beetle` chip shaper stages where the electrodes of the WSA are connected to. The output where the charge injector is coupled to the electrode on the `Beetle` chip input directly has the largest response but it is not significantly higher then the output of the `Beetle` chip channels to which the other WSA electrodes are connected.

To estimate the `Beetle` output behavior for a cross strip anode (XSA), the simulation above was also performed with the capacitance of the

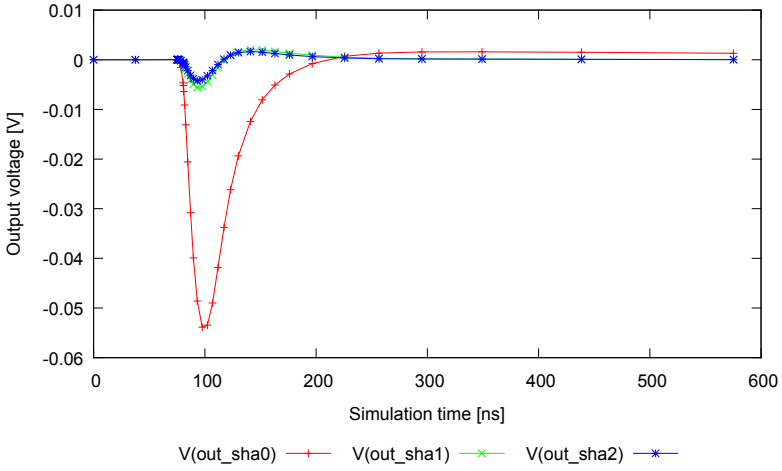

Figure 5.20.: A `LTSpiceIV` simulation of the output of three neighboring shaper stages in a `Beetle` chip when charge is injected into one electrode of an XSA which electrodes are connected to the chip's inputs successively.

XSAs that have been designed at the IAAT. The parameters of the front-end stages and the charge injector step height are equal to the previous simulations. Figure 5.20 shows the simulated output of the `Beetle` chip when a charge is coupled into one of the strips of the XSA via the charge injector directly. The cross-talk between the channels is present but considerably smaller compared to the WSA (Figure 5.19).

The figures show furthermore that the output response of the `Beetle` chip model to the XSA is higher than for the WSA for equal `Beetle` chip front-end parameters. This is expected from the difference in the electrode capacitance. A higher input capacitance causes a smaller and wider front-end output signal of the `Beetle` chip (see Figure 4.6).

The simulations above support the readout electronics concept of a cross strip anode which is read out by a `Beetle` chip.

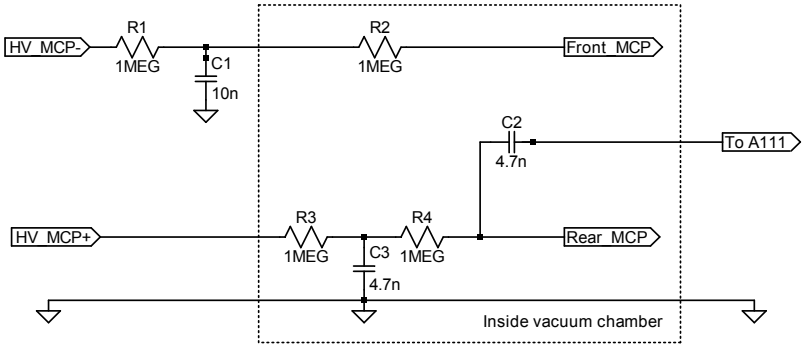

Figure 5.21.: Schematic of the trigger signal generation from the high voltage (HV) in the vacuum chamber.

5.2.4. UV illumination of the setup in the vacuum chamber

The setup in the vacuum chamber (Figure 5.7) has been used to test the readout electronics under realistic conditions where charge information created by UV photons in an MCP stack is processed. The photon events are read out by a WSA and are pre-amplified by a `Beetle 1.5` which is mounted on an MPIK daughterboard. In this measurement, the trigger is established from the setup itself.

When a charge cloud is generated in the MCP stack from an incoming photon, the high voltage supply has to compensate for the extracted charge. Figure 5.21 shows the schematic of the circuit that couples a pulse out of the high voltage supply of the MCP stack in the vacuum chamber when a charge cloud is multiplied in the pores of the stack. The pulse is fed into an Amptek `A111`[10] charge sensitive pre-amplifier and discriminator that is mounted onto a `pc21` evaluation board which was also designed by Amptek. The digital output of the `A111` comparator is fed into the FPGA where the signal is used as an input trigger signal. The FPGA forms an output trigger signal from it and passes it to the `Beetle` chip.

In Figure 5.22, the pulse height distribution of the measurement where the MCP stack in the vacuum chamber is illuminated through the quartz window with a pen-ray mercury UV lamp from outside the vacuum chamber

[10] http://www.amptek.com/products/a111-charge-sensitive-preamplifier/

can be seen. A voltage of 2 kV is applied across the MCPs in the stack. Figure 5.23 shows the pulse height distribution for two channels and Figure 5.24 displays the scatter plot of the measurement. Besides a contribution of pulses that concentrate around the baseline, a distinct pulse population at higher pulse heights can be identified. When the lamp is switched off, this population is absent as can be seen in Figures 5.25, 5.26, and 5.27. This indicates that the population besides the baseline population stems from UV photons that release charge clouds in the MCP stack in the vacuum chamber. For this, the readout electronics proved proper function also in this setup.

The pulses that concentrate around the baseline in the pulse height distribution plots are correlated noise which is recorded when the `A111` triggers due to the noise that is most likely produced by the MPC high voltage supply on the input of the `A111`. The noise itself most likely stems from the high voltage power supply and is induced equally into the input signals of the `Beetle` chip due to its correlated appearance. Noise rejection is presently investigated. As an alternative for the trigger signal generation from the HV, it is planned to apply the comparator stage in the `Beetle` chip to provide trigger information from photon events. The latter trigger generation scheme promises a better noise rejection.

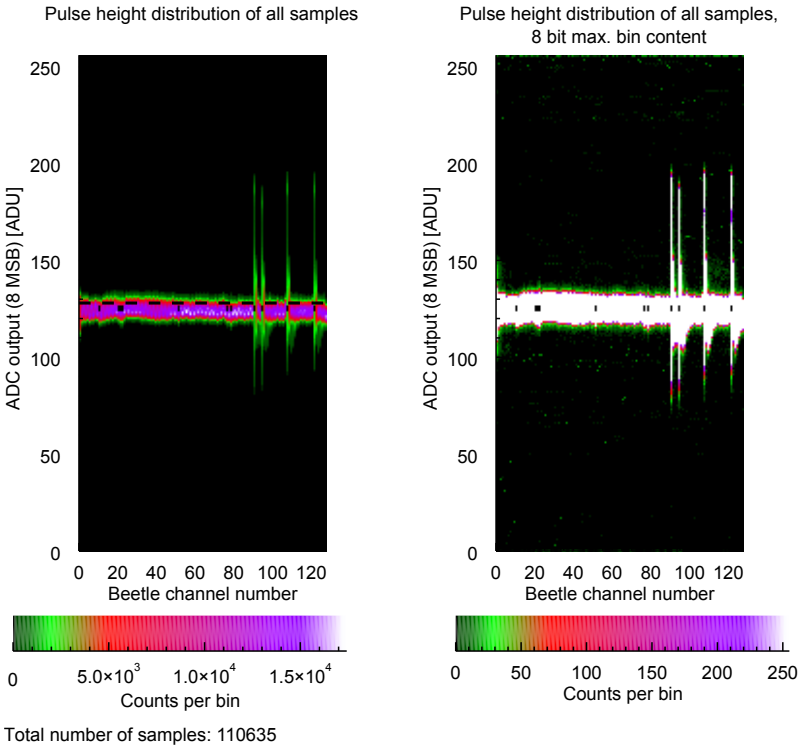

Figure 5.22.: Pulse height distribution of a measurement using the setup in the vacuum chamber. The MCP stack is illuminated with a mercury pen-ray UV lamp from outside the vacuum chamber. The charge clouds are spread onto a WSA. Wedges of the anode are connected to input channels 90 and 121 of a `Beetle` chip 1.5, strips are connected to input channels 94 and 107. A pulse population at higher pulse heights with respect to the pulses around the baseline can be seen.

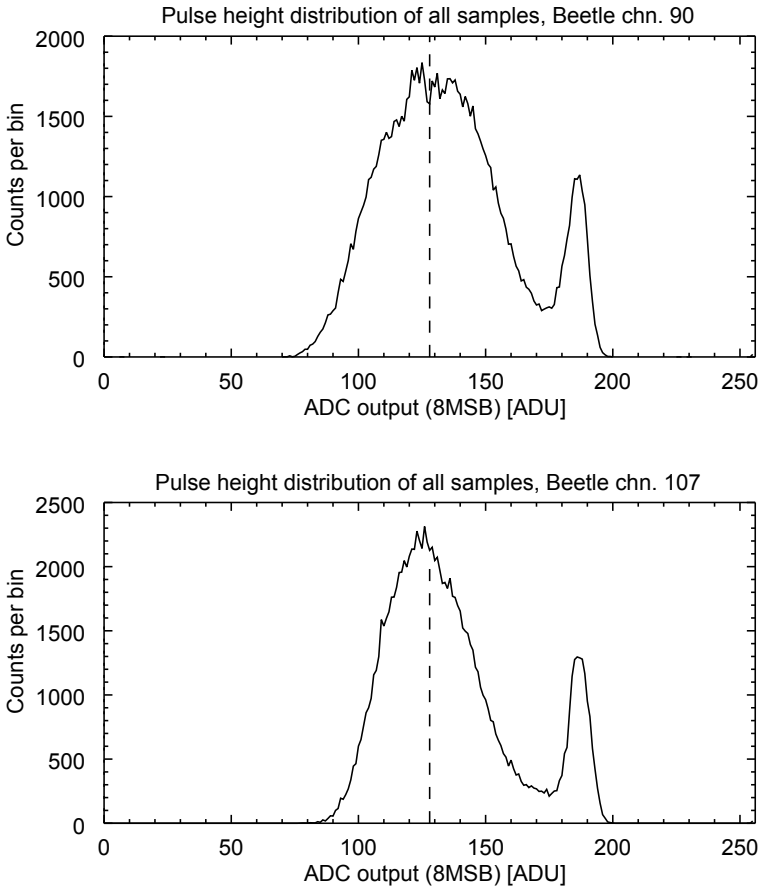

Figure 5.23.: Pulse height distribution for two `Beetle` chip 1.5 channels of a measurement using the setup in the vacuum chamber. The MCP stack is illuminated with a mercury pen-ray UV lamp from outside the vacuum chamber. The charge clouds are spread onto a WSA. The `Beetle` chip input 90 is connected to a wedge of the WSA, input channel 107 is connected to a strip. Besides a pulse population around the baseline, a distinct population at higher pulse heights can be identified here.

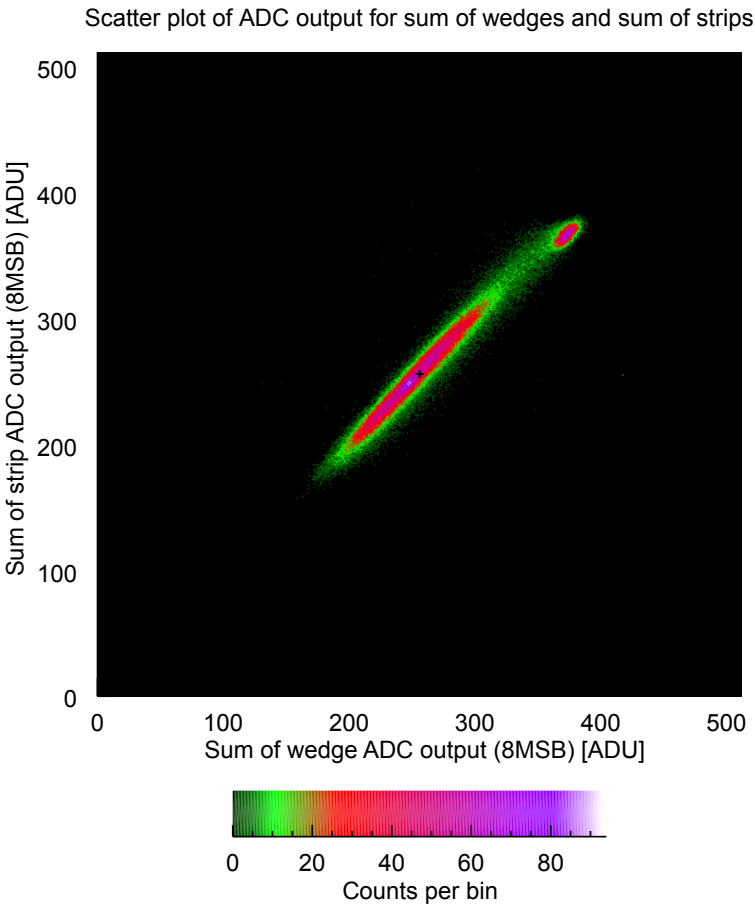

Figure 5.24.: Scatter plot of a measurement where the MCP stack in the vacuum chamber is illuminated by a mercury pen-ray UV lamp. The plot shows a plane of the pulse height sum on the strips versus the pulse height sum on the wedges of the WSA. A distinct pulse population can be identified which is absent when the UV lamp is switched off (Figure 5.27).

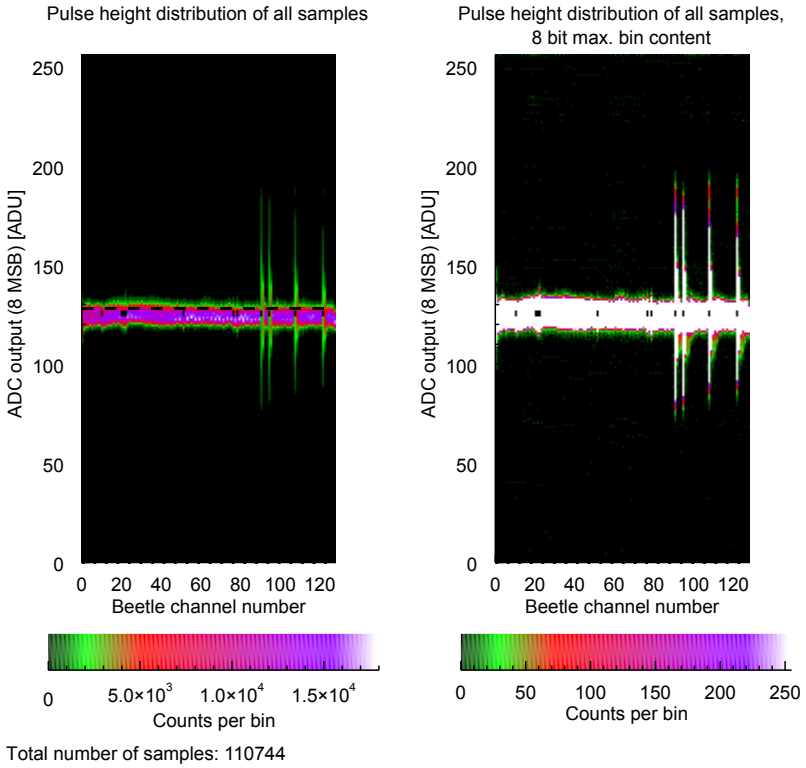

Figure 5.25.: Pulse height distribution of a measurement using the setup in the vacuum chamber. The setup is the same as in Figure 5.22 but the UV lamp is switched off.

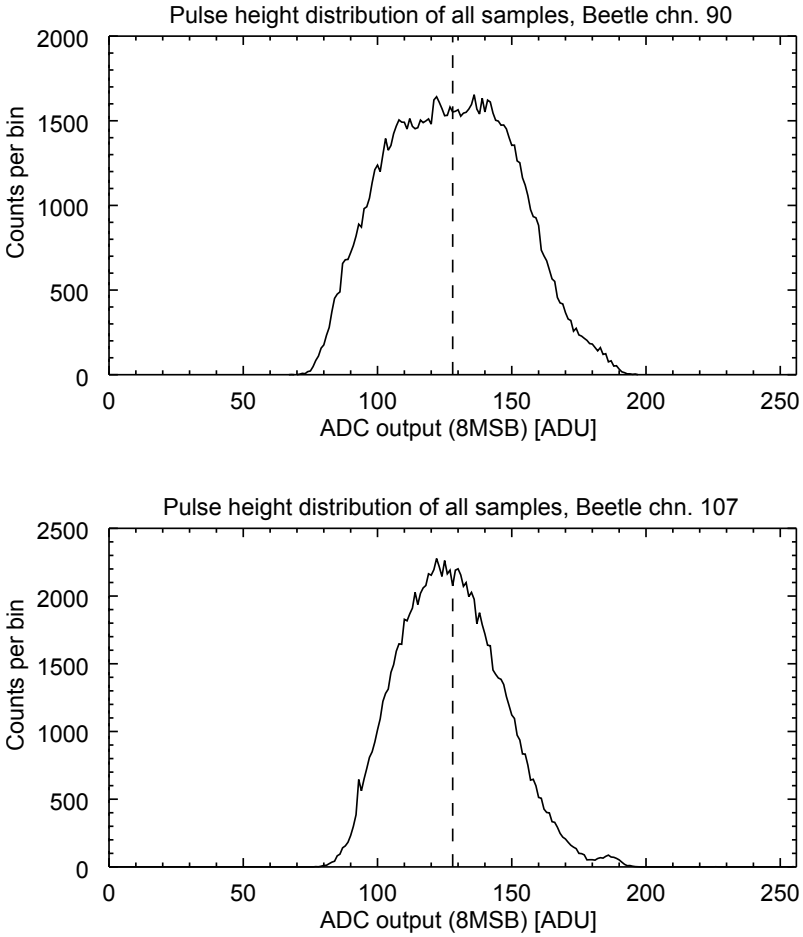

Figure 5.26.: Pulse height distribution for two `Beetle` chip channels of a measurement using the setup in the vacuum chamber. The setup is the same as in the measurement in Figure 5.23 but the lamp is switched off.

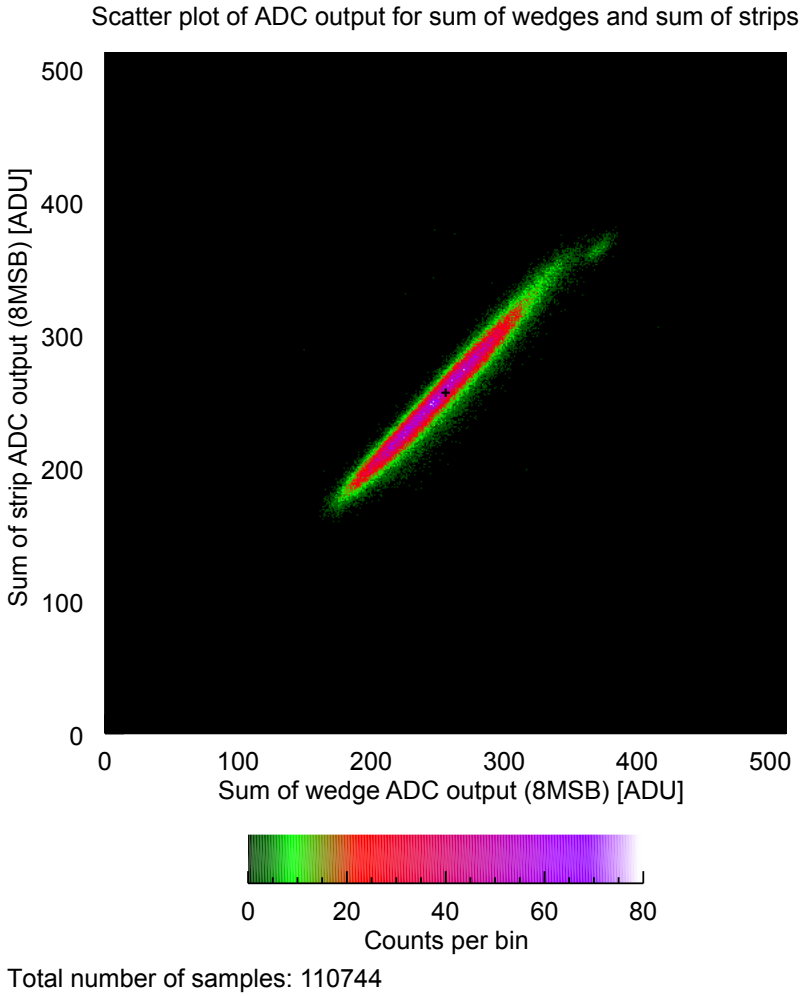

Figure 5.27.: Scatter plot of a measurement where the MCP stack in the vacuum chamber is not illuminated by a UV lamp. The distinct pulse population next to the population which is concentrates around the baseline that is present in Figure 5.24 is not seen here.

5.2.5. Commissioning of XSAs and a `Beetle` CHC board

The cross strip anodes that have been designed at IAAT have been applied in this work to verify the proper functionality of the readout electronics for the readout of XSAs. During the test measurements, issues concerning the manufacturing process of the XSAs could be identified. One issue is the presence of shorts among the electrodes on the active face of the anodes. Another issue is that the contact of the electrodes of the anodes to the contact pads at the rear side of the anodes is not established for several electrodes. A rework of the anodes is currently under discussion with the supplier.

The `Beetle` chip CHC board was commissioned as a part of this work and the communication to the `Beetle` chip as well as a readout of the chip by the readout electronics setup could be proven. At the end of this work, the signal quality of the `Beetle` CHC board is still below the expectations nevertheless. The baseline noise is a factor of four higher compared to early measurements using the `Beetle` chip on the daughterboards from MPIK Heidelberg. The operational amplifier circuit had to be disconnected due to common-mode oscillations and will be placed at the front-end electronics FPGA board. The source of the noise was identified to origin from the signal routing already in front of the `Beetle` chip input. Work is going on to identify and eliminate the sources of the noise at the time of this work.

5.2.6. Power consumption of the readout electronics setup

Table 5.4 shows the power consumption during a power-on of the readout electronics setup. The data in Table 5.4 are exemplary for the general power consumption of the setup. Power dissipation due to the voltage regulators on the the FPGA motherboard are not taken into account here. When the power supply is switched on, the FPGA and the `Beetle` chip are not started immediately and the power consumption is in the order of 1.4 W. When the VHDL firmware design is configured into the `Virtex-4` FPGA, the `Beetle` chip is started and default front-end parameters given by Löchner (2006) are loaded into the chip. For this, the power consumption reaches a peak value of 3 W at this point. In standby mode, when the `Beetle` chip was configured to the front-end parameters for the readout electronics setup and in particular to the readout mode on one analog output port, the power consumption of the setup drops slightly to around

Table 5.4.: Power consumption of the readout electronics laboratory setup. Dissipation in voltage regulators prior to the setup are not taken into account.

Condition	5 V lane current/mA	2.5 V lane current/mA	Total power consumption/W
Power on	262	22	1.365
FPGA configured	464	250	2.945
Standby	468	209	2.862
Sleep mode	437	185	2.648

2.9 W. When the electronics is put to the sleep mode via a command from the control software, the power consumption is 2.6 W. This is due to the fact that all modules in the `Virtex-4` VHDL firmware design as well as the logic blocks on the `Beetle` chip are held in reset state in this mode. During data acquisition, the power consumption is comparable to the standby mode. This is as expected, since all logic blocks of the setup are in operation in standby mode and only a trigger signal is not provided to the `Beetle` chip.

An estimate for the power consumption of the VHDL firmware design in a radiation hard FPGA was not at the focus of this work. As one `AD9649` is specified by the supplier to consume typically 73.8 mA for a sine wave input at 40 MHz sampling clock, the power consumption of the setup would increase in the order of 225 mW when four instead of one `AD9649` is used for the `Beetle` chip readout. When the radiation-hardened `RHF1401` would be applied, this estimate is not altered significant since the `RHF1401` is specified at 85 mW at a sampling frequency of 20 MHz.

The power consumption of the readout electronics setup is well below the limit of 10 W which was specified at the beginning of this work.

5.2.7. Discussion

The readout electronics has proven proper and plausible function during this work in VHDL simulations as well as in different test conditions as the initial readout setup and the readout electronics laboratory setup. The charge injector that was designed and manufactured in this work proved as

a valuable and reliable tool for the tests. A modified and enhanced version of it will be used for tests of the readout electronics of the FlashCam camera for the of the Cherenkov Telescope Array (CTA). The implementation of a detailed VHDL test bench supported the proper function of the FPGA in the setup.

The proper readout and processing of charges of different origin in the `Beetle` chip could be shown. The charge was provided by the charge injector directly, or coupled into a wedge and strip anode and then processed by the `Beetle` chip subsequently. Charge clouds from a stack of MCPs that were induced by UV photons have also been processed and identified in this work. The concept to apply a cross strip anode for the charge cloud sampling is supported by simulations of the `Beetle` chip response. A `Beetle` CHC board was commissioned and proper function of the `Beetle` chip communication and readout was possible. Efforts to identify sources that disturb the input signal quality of the `Beetle` CHC board are subject to future work.

6. Conclusion

In the beginning of this thesis, it was argued that astronomical UV observations provide a unique opportunity to study the physical phenomena in the Universe. The UV spectral band provides access to the resonance lines of the dominant species in distant objects where processes are highly energetic and harsh as in the vicinity of supernovae but also provides insight into objects nearby in our quiet solar neighborhood like the atmospheres of Mars or the giant planets.

Based on a history of successful observations by rockets and satellites where various technologies were applied for observational instruments, new technologies for UV instruments are crucial to expand the frontiers of scientific perception. Technical progress in the fields of detectors, optical components, and coatings is mandatory. As solar blind MCP detectors are the best detectors for UV space instruments, the enhancement of their components is in the focus of investigation. New technologies for photocathode materials as for example GaN will raise the sensitivity of MCP detectors. New designs of discrete anodes as the cross strip anode will lower the necessary operational gain for the MCPs and hence the lifetime of MCP detectors will be longer. Both factors are crucial for an application of the detectors in future UV space missions and hence are at the focus of research at IAAT.

As low power dissipation is mandatory on satellite observatories, the `Beetle` pre-amplifier chip was applied to realize a low power readout electronics concept in this work. A VHDL firmware design was implemented in a `Virtex-4` FPGA that performs the control and readout of the `Beetle` chip via an ADC. Data are acquired on a laboratory PC by means of a USB interface. Control and first-level analysis software was implemented for the readout electronics. Acquired data have been analyzed using IDL programs.

For the development of the VDHL design in the FPGA, a full VHDL test bench was implemented. For tests during and after the construction of the readout setup, a charge injector was designed and manufactured. For tests of the readout electronics under realistic conditions, the readout electronics

was integrated into a laboratory setup. A vacuum chamber that contains an MCP detector in an experimental setup under vacuum conditions was used for readout electronics tests. The commissioning of components to further improve the electronics setup in terms of the scientific constraints was done.

This work demonstrated a proper function and a low power consumption of the implemented readout electronics far below the original limit of 10 W. A space-qualified implementation of the readout electronics is possible.

To conclude, the readout electronics will allow to built MCP detectors that have a so far unmatched lifetime and dynamics. It will be a vital part on future UV missions for the exploration of celestial objects in the Universe.

A. Technical documentation

A.1. MCP detector readout electronics

A.1.1. Pin assignments of the `Virtex-4` front-end electronics FPGA board assembly

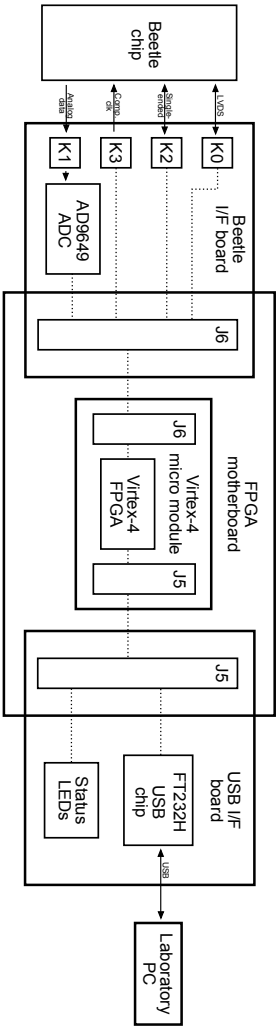

Figure A.1.: Schematic of the connection of the readout electronics boards. Connector names of the FPGA motherboard and the `Virtex-4` micro module follow the particular designers.

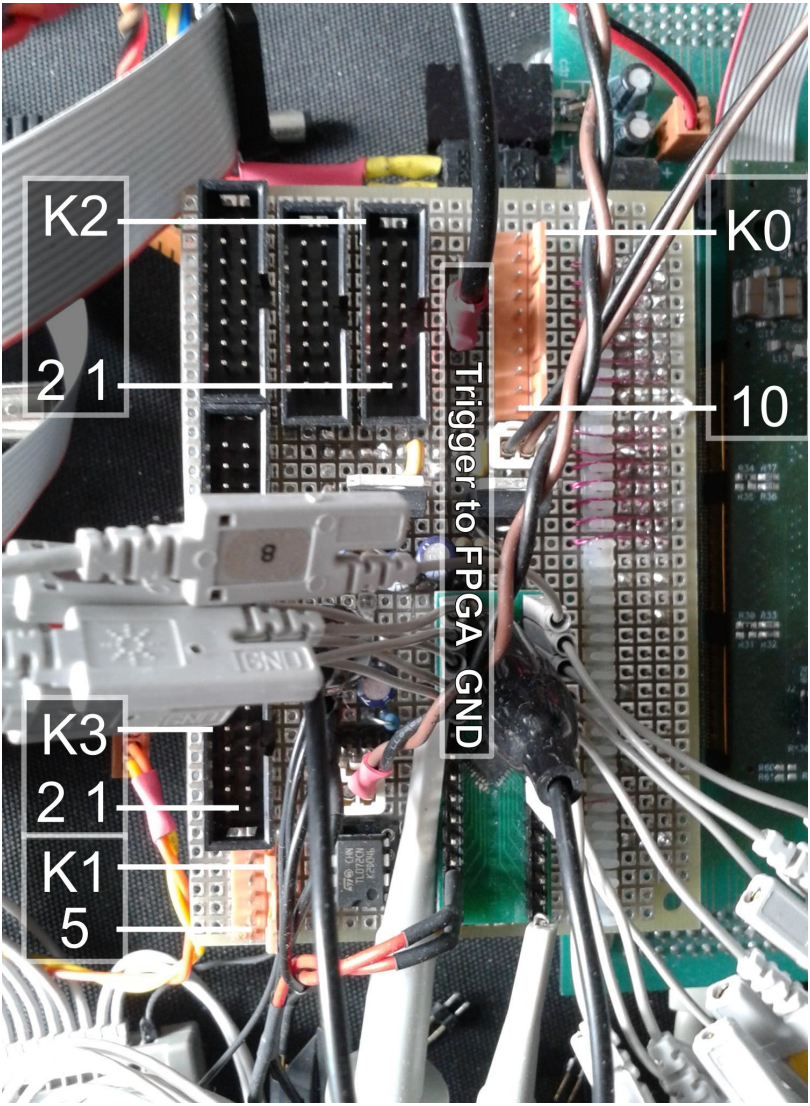

Figure A.2.: Pin numbers of the `Beetle` interface and `AD9649` board.

Table A.1.: Pin assignment of the `Beetle` and trigger interface (I/F) board. I/F board pin numbers are shown in Figure A.2. `Virtex-4` pin names are taken from IAF `Virtex-4` micro module (V-4 mimo) schematics, pin numbers from the `Virtex-4` datasheet.

Signal name	I/F board	Mother-board	V-4 mimo	FPGA Pin name	num.
DataValid+	K2 - 14	J6 - c1	J6 - 4	V4_B5_P1	C17
DataValid-	K2 - 15	J6 - b1	J6 - 6	V4_B5_N1	D17
Bee_Clk+	K2 - 5	J6 - b2	J6 - 10	V4_B5_P15	A22
Bee_Clk-	K2 - 6	J6 - a2	J6 - 12	V4_B5_N15	A21
Trigger+	K2 - 8	J6 - c3	J6 - 9	V4_B5_P13	A20
Trigger-	K2 - 9	J6 - b3	J6 - 11	V4_B5_N13	A19
Reset+	K2 - 2	J6 - b4	J6 - 15	V4_B5_P2	C20
Reset-	K2 - 3	J6 - a4	J6 - 17	V4_B5_N2	B20
Testpulse+	K2 - 11	J6 - c5	J6 - 22	V4_B5_P7	C19
Testpulse-	K2 - 12	J6 - b5	J6 - 24	V4_B5_N7	D18
FifoFull	K0 - 6	J6 - c6	J6 - 23	V4_B5_N10	B23
WriteMon	K0 - 7	J6 - b6	J6 - 30	V4_B5_P21	D23
TrigMon	K0 - 8	J6 - a6	J6 - 32	V4_B5_N21	C23
EnableEDC	K0 - 9	J6 - c7	J6 - 29	V4_B5_P14	D22
SDA	K0 - 2	J6 - b7	J6 - 31	V4_B5_N14	C22
SCL	K0 - 3	J6 - a7	J6 - 36	V4_B5_P16	D24
Trigger FPGA	-/-	J6 - c8	J6 - 38	V4_B5_N16	C24
Comp_Clk+	K3 - 5	J6 - c29	J6 - 140	V4_B9_P22	R24
Comp_Clk-	K3 - 6	J6 - a30	J6 - 142	V4_B9_N22	R23

Table A.2.: Pin assignment of the AD9649 ADC interface to the FPGA. I/F board pin numbers for the interface from the AD9649 to the Beetle are shown in Table A.3. Virtex-4 pin names are taken from IAF Virtex-4 micro module (mimo) schematics, pin numbers from the Virtex-4 datasheet.

Signal name	Mother-board	Virtex-4 mimo	FPGA Pin name	number
CLK+	J6 - b10	J6 - 48	V4_B5_P19	F20
CLK-	J6 - a10	J6 - 50	V4_B5_N19	E20
CSB	J6 - c11	J6 - 47	V4_B5_P11	F18
DFS	J6 - b11	J6 - 49	V4_B5_N11	E18
PWDN	J6 - a11	J6 - 56	V4_B5_P31	G26
D0	J6 - c12	J6 - 58	V4_B5_N31	G25
D1	J6 - b12	J6 - 55	V4_B5_P26	H22
D2	J6 - a12	J6 - 57	V4_B5_N26	H21
D3	J6 - c13	J6 - 62	V4_B5_P18	E23
D4	J6 - b13	J6 - 64	V4_B5_N18	E22
D5	J6 - a13	J6 - 61	V4_B5_P22	H20
D6	J6 - c14	J6 - 63	V4_B5_N22	G20
D7	J6 - b14	J6 - 68	V4_B5_P32	H26
D8	J6 - a14	J6 - 70	V4_B5_N32	H25
D9	J6 - c15	J6 - 67	V4_B5_P17	G19
D10	J6 - b15	J6 - 69	V4_B5_N17	F19
D11	J6 - a15	J6 - 74	V4_B5_P30	H24
D12	J6 - c16	J6 - 76	V4_B5_N30	H23
D13	J6 - b16	J6 - 73	...CC_LC_P9	G18
OR	J6 - a16	J6 - 75	...CC_LC_N9	G17
DCO	J6 - b30	J6 - 145	...GC_LC_P1	AF12

Table A.3.: Pin assignment of the AD9649 VCM OpAmp interface that is shown in Figure A.3. OFS_REF (see Figure A.3) is not applied in the Beetle hybrid board. Beetle I/F board pin numbers are shown in Figure A.2.

Signal Name	I/F board
S+	K1 - 4
S-	K1 - 5
OFS_REF	K1 - 1
TERM	K1 - 3
GND	K1 - 2

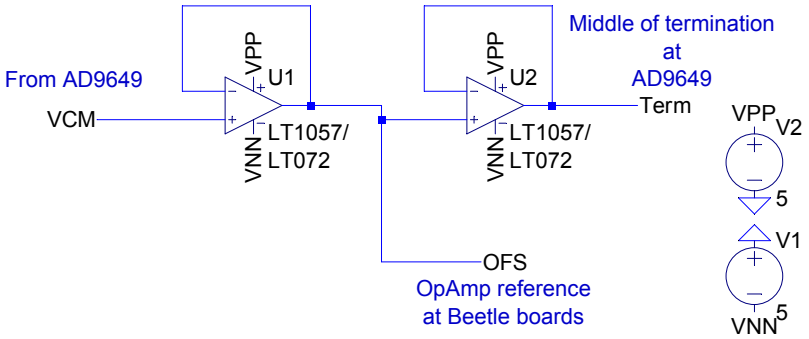

Figure A.3.: Schematic of the AD9649 VCM OpAmp circuit. It drives the baseline signal VCM that is provided by the AD9649 to the operational amplifiers located on the Beetle motherboards. OFS_REF is not applied in the Beetle hybrid board. Created by C. Kalkuhl (IAAT), modified.

Table A.4.: Pin assignment of the FT232H USB interface to the and status LEDs to the FPGA. Virtex-4 pin names are taken from IAF Virtex-4 micro module (V-4 mimo) schematics, pin numbers from the Virtex-4 datasheet.

Signal name	UM232H board	Mother-board	V-4 mimo	FPGA Pin name	num.
D7	J2 - 14	J5 - a30	J5 - 10	V4_B10_P3	K7
D6	J2 - 13	J5 - b30	J5 - 9	V4_B10_P6	K5
D5	J2 - 12	J5 - a29	J5 - 12	V4_B10_N3	K6
D4	J2 - 11	J5 - b29	J5 - 11	V4_B10_N6	K4
D3	J2 - 10	J5 - a28	J5 - 16	V4_B10_P7	K3
D2	J2 - 9	J5 - b28	J5 - 15	V4_B10_P5	L7
D1	J2 - 8	J5 - a27	J5 - 18	V4_B10_N7	K2
D0	J2 - 7	J5 - b27	J5 - 17	V4_B10_N5	L6
RxF#	J1 - 14	J5 - a26	J5 - 22	V4_B10_P13	M6
TxE#	J1 - 13	J5 - b26	J5 - 21	V4_B10_P10	L1
RD#	J1 - 12	J5 - a25	J5 - 24	V4_B10_N13	M5
WR#	J1 - 11	J5 - b25	J5 - 23	V4_B10_N10	K1
SIWU#	J1 - 10	J5 - a24	J5 - 30	V4_B10_P15	N5
OE#	J1 - 8	J5 - b24	J5 - 29	V4_B10_P11	M2
RST#	J1 - 4	J5 - a23	J5 - 32	V4_B10_N15	N4
PWREN#	J1 - 6	J5 - b22	J5 - 35	V4_B10_P14	N3
CLKOUT	J1 - 9	J5 - a18	J5 - 48	...CC_LC_P9	M8
STATUS[0]	R LED	J5 - b32	J5 - 3	V4_B10_P2	J5
STATUS[1]	Y LED	J5 - a32	J5 - 4	V4_B10_P1	J7
STATUS[2]	G LED	J5 - b31	J5 - 5	V4_B10_N2	J6

A.1.2. Readout electronics commands and packet structure

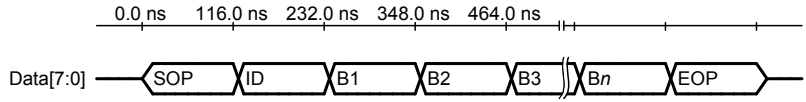

Figure A.4.: The packet structure of the readout electronics communication. The number n of bytes Bx that follow the packet-ID varies depending on the specific command (see Tables A.5 and A.6).

Table A.5.: Command overview of the readout electronics I: host to electronics. The ID is given in hexadecimal numbers. n corresponds to the number of bytes Bx that follow the packet-ID (Figure A.4). Commands in *italic* are reserved but not fully implemented.

ID	Command	n	Comment
0	NOP		
1	FLOW_NULL	0	For maintenance
2	FLOW_ACQUIRE	0	Start data acquisition
3	FLOW_STOP	0	Stop data acquisition
4	*FLOW_RESET*	0	Global reset to all entities
5	FLOW_SLEEP	0	Enter power saving mode
6	FLOW_WAKEUP	0	Leave power saving mode
10	BEE_Itp_READ	0	`Beetle` reg. read request
11	BEE_Ipre_READ	0	`Beetle` reg. read request
12	BEE_Isha_READ	0	`Beetle` reg. read request
13	BEE_Ibuf_READ	0	`Beetle` reg. read request
14	BEE_Vfp_READ	0	`Beetle` reg. read request
15	BEE_Vfs_READ	0	`Beetle` reg. read request
16	BEE_Icomp_READ	0	`Beetle` reg. read request
17	BEE_Ithdelta_READ	0	`Beetle` reg. read request
18	BEE_Ithmain_READ	0	`Beetle` reg. read request
19	BEE_Vrc_READ	0	`Beetle` reg. read request

Table A.5.: (continued)

ID	Command	n	Comment
1A	BEE_Ipipe_READ	0	`Beetle` reg. read request
1B	BEE_Vd_READ	0	`Beetle` reg. read request
1C	BEE_Vdcl_READ	0	`Beetle` reg. read request
1D	BEE_Ivoltbuf_READ	0	`Beetle` reg. read request
1E	BEE_Isf_READ	0	`Beetle` reg. read request
1F	BEE_Icurrbuf_READ	0	`Beetle` reg. read request
20	BEE_Latency_READ	0	`Beetle` reg. read request
21	BEE_ROCtrl_READ	0	`Beetle` reg. read request
22	BEE_RclkDiv_READ	0	`Beetle` reg. read request
23	BEE_CompCtrl_READ	0	`Beetle` reg. read request
24	BEE_CompChTh_RD	0	`Beetle` reg. read request
25	BEE_CompMask_RD	0	`Beetle` reg. read request
26	BEE_TpSelect_READ	0	`Beetle` reg. read request
27	BEE_SEUcounts_RD	0	`Beetle` reg. read request
30	BEE_Itp_WRITE	1	`Beetle` reg. write request
31	BEE_Ipre_WRITE	1	`Beetle` reg. write request
32	BEE_Isha_WRITE	1	`Beetle` reg. write request
33	BEE_Ibuf_WRITE	1	`Beetle` reg. write request
34	BEE_Vfp_WRITE	1	`Beetle` reg. write request
35	BEE_Vfs_WRITE	1	`Beetle` reg. write request
36	BEE_Icomp_WRITE	1	`Beetle` reg. write request
37	BEE_Ithdelta_WRITE	1	`Beetle` reg. write request
38	BEE_Ithmain_WRITE	1	`Beetle` reg. write request
39	BEE_Vrc_WRITE	1	`Beetle` reg. write request
3A	BEE_Ipipe_WRITE	1	`Beetle` reg. write request
3B	BEE_Vd_WRITE	1	`Beetle` reg. write request
3C	BEE_Vdcl_WRITE	1	`Beetle` reg. write request
3D	BEE_Ivoltbuf_WRITE	1	`Beetle` reg. write request
3E	BEE_Isf_WRITE	1	`Beetle` reg. write request
3F	BEE_Icurrbuf_WRITE	1	`Beetle` reg. write request
40	BEE_Latency_WRITE	1	`Beetle` reg. write request
41	BEE_ROCtrl_WRITE	1	`Beetle` reg. write request
42	BEE_RclkDiv_WRITE	1	`Beetle` reg. write request
43	BEE_CompCtrl_WR.	1	`Beetle` reg. write request

Table A.5.: (continued)

ID	Command	n	Comment
44	BEE_CompChTh_WR.	1	128 consecutive writes
45	BEE_CompMask_WR.	1	16 consecutive writes
46	BEE_TpSelect_WR.	1	17 consecutive writes
47	BEE_SEUcounts_WR.	1	`Beetle` reg. write request
50	*BEE_RESET*	0	`Beetle` reset request
51	*BEE_RECONF*	0	Rewrite `Beetle` reg. fr. RAM
55	EOP		End of packet marker
60	*BEE_I2CClk_READ*	0	I2C period read request
61	*BEE_TriggerDur_READ*	0	Trigger duration request
62	*BEE_TriggerDel_READ*	0	Trigger delay request
80	STATUS_NULL	0	For maintenance
81	*STATUS_ALL*	0	Burst status info
82	STATUS_COMMANDS	0	Read # of commands
83	STATUS_TRIGGERS	0	Read # of triggers
84	STATUS_DATAVALID	0	Read # of DataValid signals
85	ST._DAVAUNPROC	0	Read # of unproc. DataValid
86	ST._DAPACKSEND	0	Read # of sent data packets
A0	PARAM_NULL	0	For maintenance
AA	SOP		Start of packet marker

Table A.6.: Command overview of the readout electronics II: electronics to host. The ID is given in hexadecimal numbers. n corresponds to the number of bytes Bx that follow the packet-ID (Figure A.4). Commands in *italic* are reserved but not fully implemented.

ID	Command	n	Comment
0	NOP		
1	FLOW_NULL_ACK	0	For maintenance
2	FLOW_ACQUIRE_ACK	0	Acknowledge for start
3	FLOW_STOP_ACK	0	Ack. for acquisition stop

Table A.6.: (continued)

ID	Command	n	Comment
4	*FLOW_RESET_ACK*	0	Ack. for global reset
5	FLOW_SLEEP_ACK	0	Ack. for power saving mode
6	FLOW_WAKEUP_ACK	0	Ack. f. leaved power saving
10	BEE_Itp_READ	1	`Beetle` reg. read response
11	BEE_Ipre_READ	1	`Beetle` reg. read response
12	BEE_Isha_READ	1	`Beetle` reg. read response
13	BEE_Ibuf_READ	1	`Beetle` reg. read response
14	BEE_Vfp_READ	1	`Beetle` reg. read response
15	BEE_Vfs_READ	1	`Beetle` reg. read response
16	BEE_Icomp_READ	1	`Beetle` reg. read response
17	BEE_Ithdelta_READ	1	`Beetle` reg. read response
18	BEE_Ithmain_READ	1	`Beetle` reg. read response
19	BEE_Vrc_READ	1	`Beetle` reg. read response
1A	BEE_Ipipe_READ	1	`Beetle` reg. read response
1B	BEE_Vd_READ	1	`Beetle` reg. read response
1C	BEE_Vdcl_READ	1	`Beetle` reg. read response
1D	BEE_Ivoltbuf_READ	1	`Beetle` reg. read response
1E	BEE_Isf_READ	1	`Beetle` reg. read response
1F	BEE_Icurrbuf_READ	1	`Beetle` reg. read response
20	BEE_Latency_READ	1	`Beetle` reg. read response
21	BEE_ROCtrl_READ	1	`Beetle` reg. read response
22	BEE_RclkDiv_READ	1	`Beetle` reg. read response
23	BEE_CompCtrl_READ	1	`Beetle` reg. read response
24	BEE_CompChTh_READ	1	`Beetle` reg. read response
25	BEE_CompMask_READ	1	`Beetle` reg. read response
26	BEE_TpSelect_READ	1	`Beetle` reg. read response
27	BEE_SEUcounts_READ	1	`Beetle` reg. read response
30	BEE_Itp_ACK	0	`Beetle` reg. write ack.
31	BEE_Ipre_ACK	0	`Beetle` reg. write ack.
32	BEE_Isha_ACK	0	`Beetle` reg. write ack.
33	BEE_Ibuf_ACK	0	`Beetle` reg. write ack.
34	BEE_Vfp_ACK	0	`Beetle` reg. write ack.
35	BEE_Vfs_ACK	0	`Beetle` reg. write ack.
36	BEE_Icomp_ACK	0	`Beetle` reg. write ack.

Table A.6.: (continued)

ID	Command	n	Comment
37	BEE_Ithdelta_ACK	0	`Beetle` reg. write ack.
38	BEE_Ithmain_ACK	0	`Beetle` reg. write ack.
39	BEE_Vrc_ACK	0	`Beetle` reg. write ack.
3A	BEE_Ipipe_ACK	0	`Beetle` reg. write ack.
3B	BEE_Vd_ACK	0	`Beetle` reg. write ack.
3C	BEE_Vdcl_ACK	0	`Beetle` reg. write ack.
3D	BEE_Ivoltbuf_ACK	0	`Beetle` reg. write ack.
3E	BEE_Isf_ACK	0	`Beetle` reg. write ack.
3F	BEE_Icurrbuf_ACK	0	`Beetle` reg. write ack.
40	BEE_Latency_ACK	0	`Beetle` reg. write ack.
41	BEE_ROCtrl_ACK	0	`Beetle` reg. write ack.
42	BEE_RclkDiv_ACK	0	`Beetle` reg. write ack.
43	BEE_CompCtrl_ACK	0	`Beetle` reg. write ack.
44	BEE_CompChTh_ACK	0	`Beetle` reg. write ack.
45	BEE_CompMask_ACK	0	`Beetle` reg. write ack.
46	BEE_TpSelect_ACK	0	`Beetle` reg. write ack.
47	BEE_SEUcounts_ACK	0	`Beetle` reg. write ack.
50	*BEE_RESET_ACK*	0	`Beetle` reset ack.
51	*BEE_RECONF_ACK*	0	Register rewrite ack.
55	EOP		End of packet marker
60	*BEE_I2CClk_READ*	2	I2C period read response
61	*BEE_TriggerDur_RD*	1	Trigger duration response
62	*BEE_TriggerDel_RD*	1	Trigger delay response
70	*BEE_I2CClk_ACK*	0	# of CLK_GLOB periods
71	*BEE_TriggerDur_ACK*	0	# of CLK_`Beetle` periods
72	*BEE_TriggerDel_ACK*	0	# of CLK_`Beetle` periods
80	STATUS_NULL_ACK	0	For maintenance
81	*STATUS_ALL*	?	Burst status info
82	STATUS_COMMANDS	4	# of received commands
83	STATUS_TRIGGERS	4	# of received triggers
84	STATUS_DATAVALID	4	# of DataValid signals
85	ST._DAVAUNPROC	4	# of unproc DataValids

Table A.6.: (continued)

ID	Command	n	Comment
86	ST._DAPACKSEND	4	# of send data packets
A0	PARAM_NULL_ACK	0	For maintenance
AA	SOP		Start of packet marker
C0	ERROR_NULL	0	For maintenance
C1	ERROR_FSM	0	Unknown error in FSM
C2	ER._COMM	1	Unknown command in FSM
C3	ER._BEEMAN	0	Unknown `Beetle` error
C4	ERROR_I2C_READ	1	I2C read error
C5	ERROR_I2C_WRITE	1	I2C write
F0	DATA_NULL	0	For maintenance
F1	DATA_UNPROC	260	Unprocessed data packet
F2	DATA_MAXLOC	3	Charge location
F3	*DATA_EVENT*	?	Data packet in event format

A.2. Charge injector

A.2.1. Charge injector: schematics and PCB layout

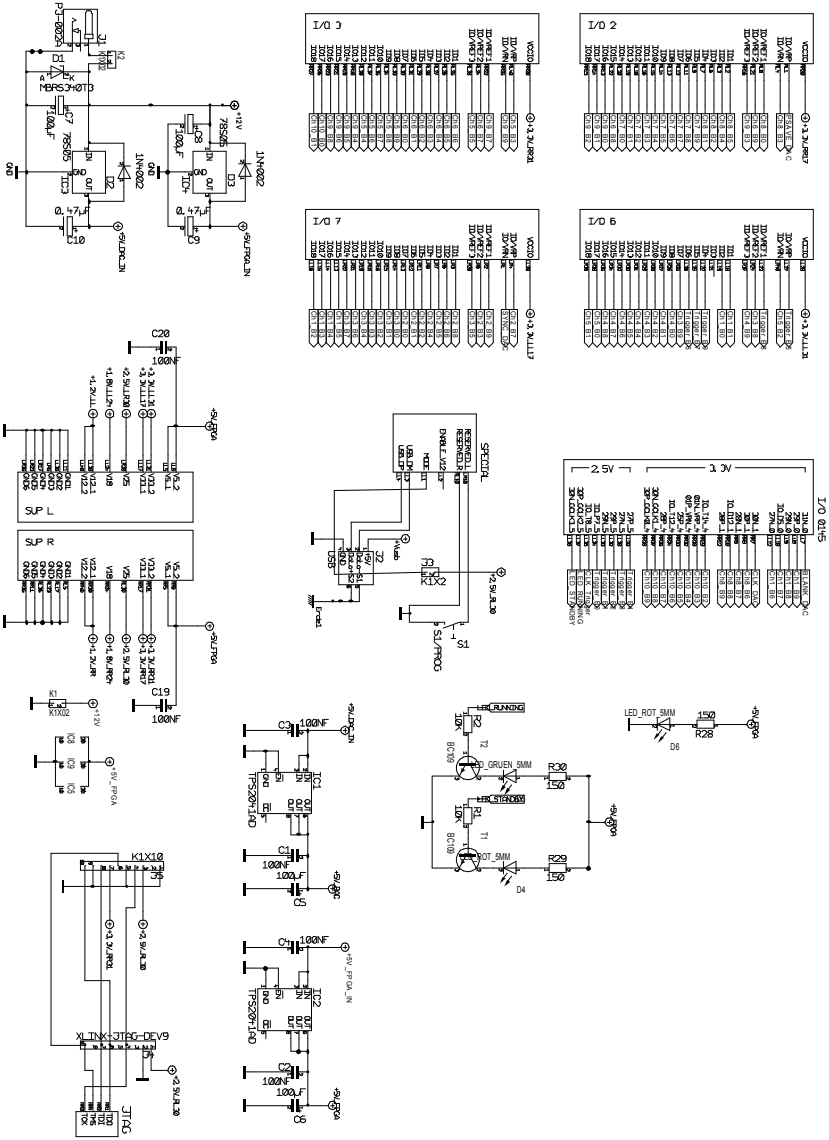

Figure A.5.: Charge inj. conn. scheme: `Spartan-3` and power supply.

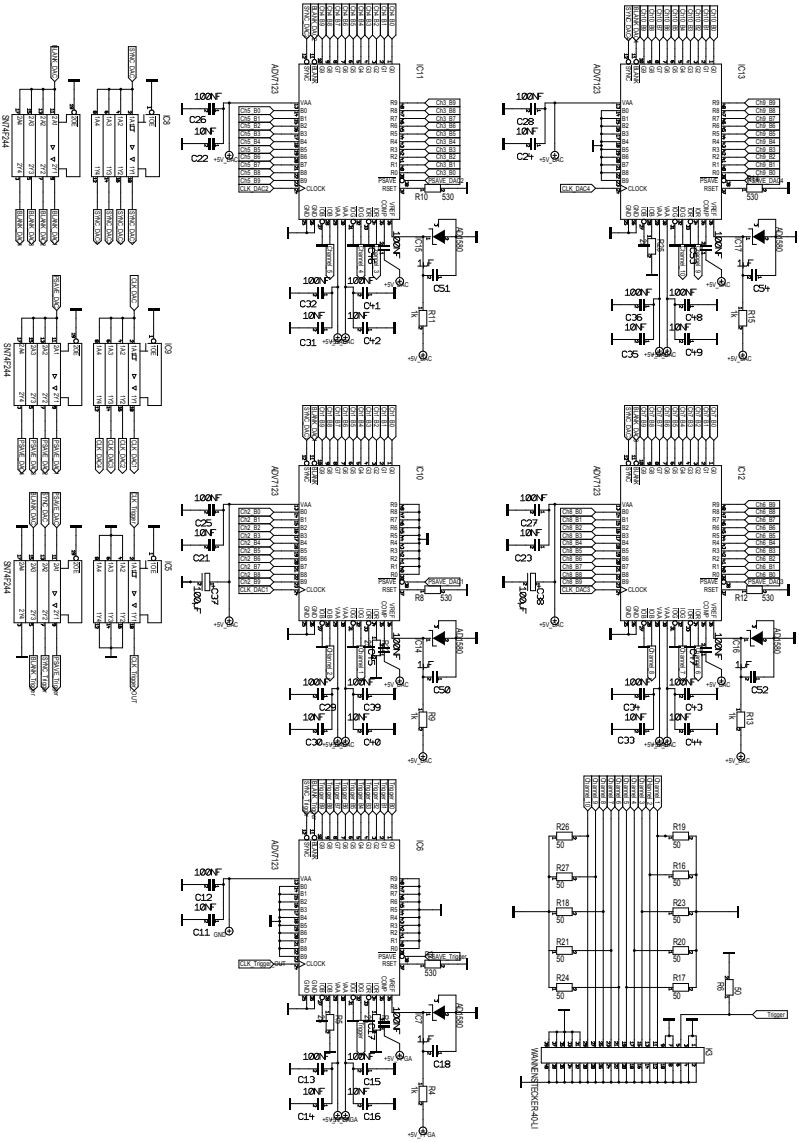

Figure A.6.: Charge injector connection scheme: ADV7123 and buffer.

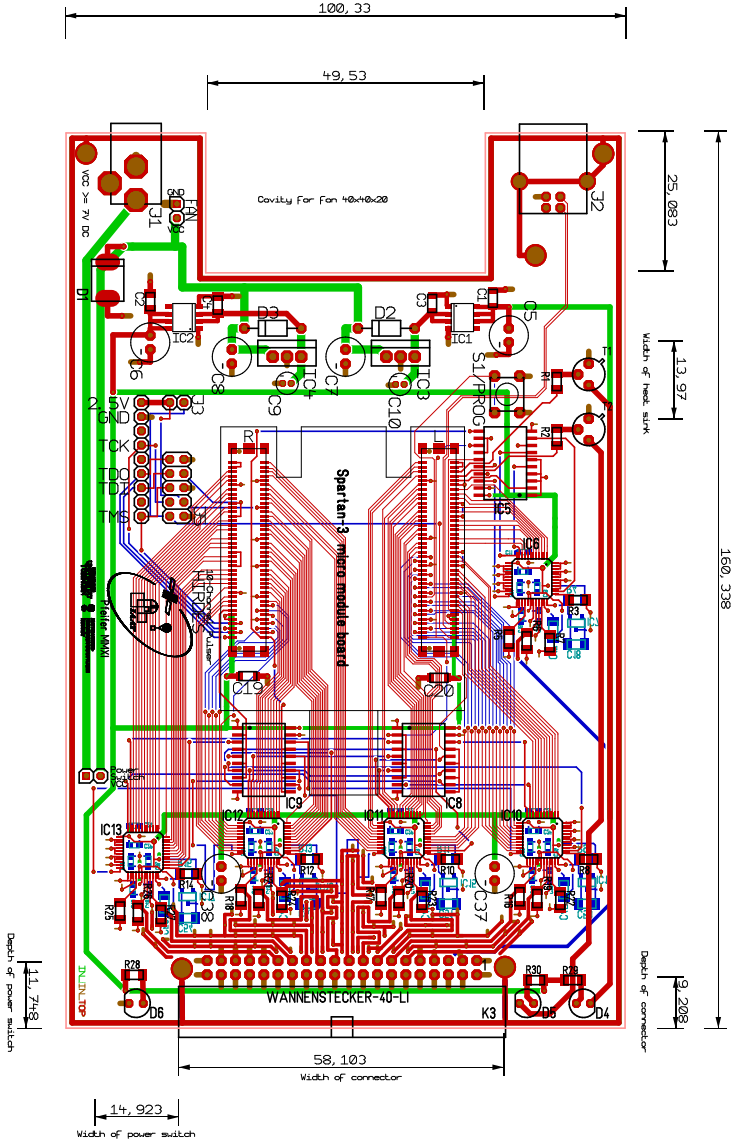

Figure A.7.: Charge injector PCB layout.

A.2.2. Charge injector: command encoding

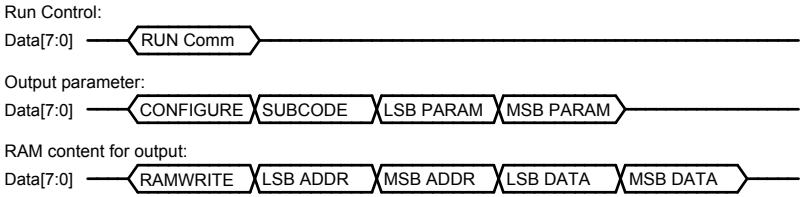

Figure A.8.: The packet structure of the charge injector communication. The structure depends on the specific command (see Table A.7).

Table A.7.: Overview of the charge injector commands. IDs are given in hexadecimal numbers. Possible subcodes for the configuration are given in Table A.8. The packet structure is shown in Figure A.8.

ID	Parameter	Comment
01	RUN	RAM data is read and output updated
02	STANDBY	No operation on output
03	CONFIGURE	Configuration state, wait for subcode
04	RAMWRITE	RAM cell, address and content follow

Table A.8.: Overview of the configuration parameters of the charge injector (subcodes). IDs are given in hexadecimal numbers. The packet structure is shown in Figure A.8.

ID	Parameter
01	Event delay
02	DAC Clock period
03	Channel mask
04	Value for inactive channels
05	Total number of events in RAM
06	Trigger high value
07	Trigger low value
08	Trigger delay
09	Trigger duration
0A	Channel mean value
0B	Gradient after event
0C	Event polarity
0D	Step with after event

A.2.3. Charge injector: event file structure

```
# This is a comment line
# This snippet shows the necessary structure of the event
# files which are read by the charge injector control
# software
Event File for Pulsegenerator Controller
# The description above is the identification string that is
# assumed by the software
Parameters: 10 10 1 10
# The parameters above are:
# (Number of memory cells in file)
# (Number of cells per event)
# (Total number of events in file)
# (Data width of data)
Content:
# The event memory content follows successively for one
# output event in this example.
# Each line is the step height of one channel.
# Hence, 10 lines comprise the information for one event.
250
240
240
240
220
220
240
240
240
240
```

Figure A.9.: Listing of the charge injector event file structure.

A.3. SPICE Simulation Schematics

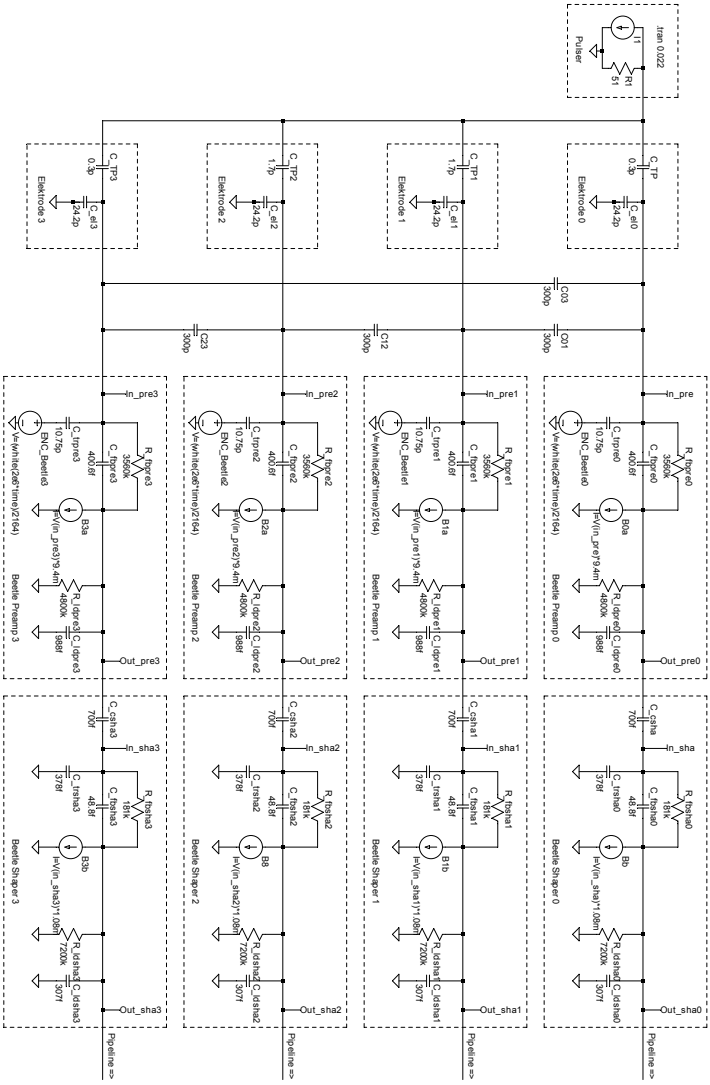

Figure A.10.: SPICE schem. for charge injector at TP of WSA.

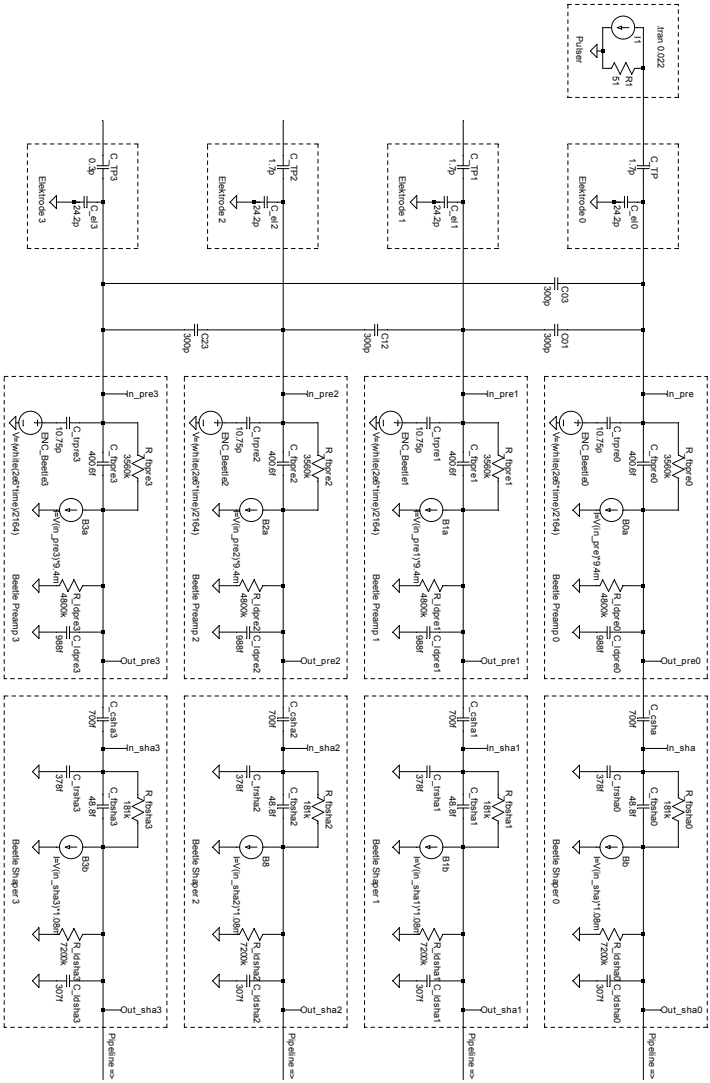

Figure A.11.: SPICE schem. for charge injector at WSA electrode.

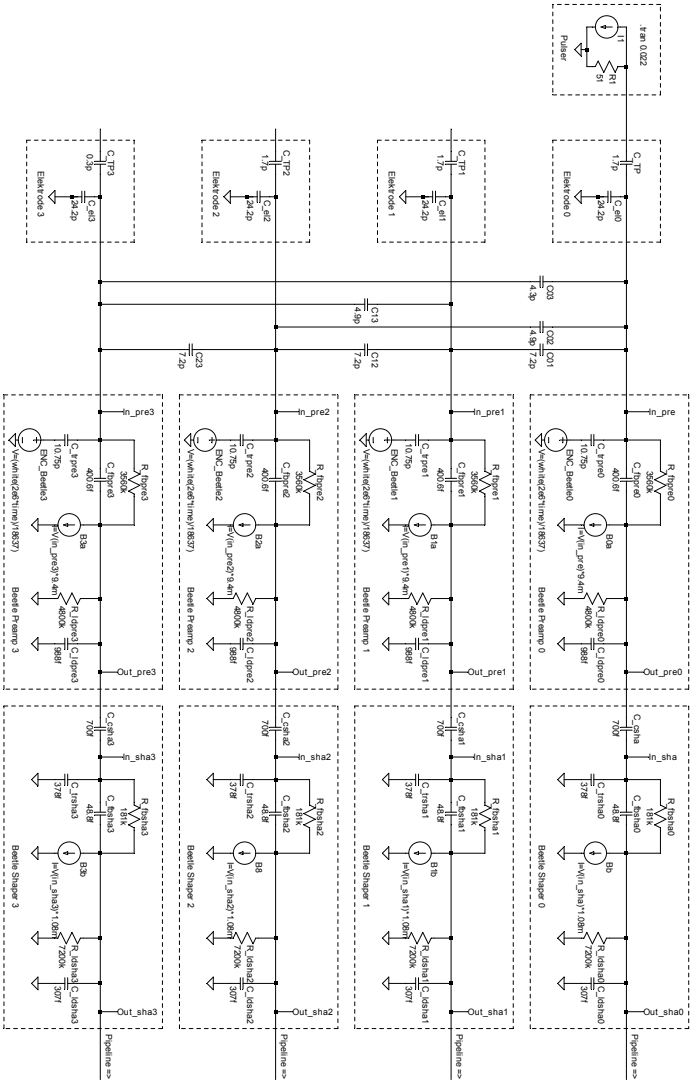

Figure A.12.: SPICE schem. for charge injector at one XSA electrode.

List of Abbreviations and Glossary

I^2C Inter-IC bus. Two-wire bidirectional serial communication bus standard that was developed by Philips Semiconductors (now NXP Semiconductors, NXP Semiconductors (2012), page 72

ADC Analog-to-digital converter. An integrated electronic circuit that converts a continuous physical measure (e.g. a voltages) to discrete digital information that represents the amplitude of the measure, page 47

AMM ADC manager module. A module in the front-end electronics firmware HDL design that manages the control and readout of the `AD9649` ADC, page 91

ASTRO-SPAS Astronomy Shuttle Pallet Satellite. Retrievable satellite platform which was built by Messerschmitt-Bölkow-Blohm (now a part of EADS) and managed by DARA (Deutsche Agentur für Raumfahrtangelegenheiten, today: DLR, German for: German Aerospace Center) that was in orbit for four flights. During two of these flights it was equipped with ORFEUS, page 13

ASTROSAT First satellite of India's Space Research Organization (ISRO) dedicated to astronomy. It carries several payloads amongst which the UltraViolet Imaging Telescope (UVIT) is a UV instrument that will perform imaging. Launch is scheduled for 2015 (Inter-University Centre for Astronomy and Astrophysics, 2012; Hindu, 2014), page 18

BMM `Beetle` manager module. A module in the front-end electronics VHDL firmware design that configures and controls the `Beetle` chip, page 89

CASTOR UV/optical 1 m telescope proposed by Canadian Space Agency (Côte et al., 2012; Côte and Scott, 2014), page 18

CDM Command decoder module. A specific module in the `Spartan-3` VHDL firmware design of the charge injector device, page 111

CHC Ceramics hybrid carrier. The `Beetle` chip carrier board. It is attached directly to the back side of the cross strip anode, page 76

COS Cosmic Origins Spectrograph. High-sensitivity spectrograph in operation on HST observing in the wavelength regime between 115 and 320 nm, page 16

CSA Canadian Space Agency, page 18

CSM Central state machine. Module of the front-end electronics firmware VHDL firmware design. It decodes commands from the back-end and controls the other module of the design, page 89

DAC Digital-to-analog converter. Integrated circuit that provides a current or voltage level at its output according to a certain value at the digital input, page 72

DC/DC converter Electronic circuit that converts direct current from one voltage level to another level, page 83

DCM Digital clock manager. One type of clocking resource that is available on the `Virtex-4` FPGA as a macro cell. A DCM is able to modify the period of an input clock signal as well as to delay the signal in certain limits which are selectable even during operation, page 94

DLR The German Aerospace Center (German: Deutsches Zentrum für Luft- und Raumfahrt e.V.). National center for aerospace, energy and transportation research of Germany, page 13

DPM Data pipeline module. A module in the front-end electronics VHDL firmware design that processes the data of `Beetle` chip samples and forms packets of the data, page 91

DQE Detective quantum efficiency. The total photon detection efficiency of a detector system. This includes for example the losses due to absorption of the UV radiation in an entrance window or losses due to the dead-time of a readout electronics, page 24

EBCCD Electron-bombarded CCD. Specific UV detector system. It comprises an opaque photocathode on a planar substrate where photoelectrons are released, an electromagnetic focusing and accelerating system, and a CCD, page 42

EEPROM Electronical erasable PROM. PROM that can be erased and re-written electronically, page 87

EGM Event generator module. A specific module of the `Spartan-3` VHDL firmware design in the charge injector, page 112

ENC Equivalent noise charge. The number of electrons one would have to collect from a detector in order to create a signal equivalent to the noise signal of the detector, page 69

EUV Extreme ultraviolet. Wavelength band below the ultraviolet band that spans from 10 nm up to 91.2 nm (Werner, 2010), page 1

FIFO First in, first out. A possible configuration of a data buffer where the first or oldest entry is read first. Electronic implementations of a FIFO can be of synchronous or asynchronous type. The read and write clocks are the same in the first case while two different clocks can be applied in the latter case, page 86

FPGA Field-programmable gate array. Integrated circuit which function is configured by a designer after its manufacturing. This can be done using a hardware description language (HDL) as for example VHDL, page 63

FSM Finite-state machine. Mathematical model of an automaton that can be in a finite number of states. It is only in one state at a time (current state) and the transition to another state can be triggered by an external or internal condition that is specific for each current state, page 89

FUSE Far Ultraviolet Spectroscopic Explorer. Important space observatory that obtained far-UV spectra. It was a cooperation of the space agencies of the United States, Canada and France. It was in operation between 1999 and 2007 (Moos et al., 2000; Kaiser and Kruk, 2009; Space Telescope Science Institute, 2014a), page 14

FUV Far-UV. Part of the UV wavelength band between 90 nm and 200 nm, page 1

GALEX Galaxy Evolution Explorer. Satellite observatory that performed, among other all-sky surveys, an extra-galactic UV survey. Decommissioned in June 2013 (Martin et al., 2005; Morrissey et al., 2005; GALEX science team at California Institute of Technology, 2014), page 14

GDR Global dynamic range. Maximum flux rate that is spread over the whole area of a detector, page 24

HST Hubble Space Telescope. Space-based observatory operated by a cooperation of ESA and NASA. It was deployed by Space Shuttle Mission (STS-31) in April 1990. A variety of instruments for imaging and spectrography in a wavelength range from the UV to the infrared are currently installed on HST (Space Telescope Science Institute, 2014b), page 16

ICCD MCP-intensified CCD. Specific type of UV detector. It contains an MCP that is coated with a photocathode. At the back of the MCP, a phosphor coated fiber optic bundle images the charge cloud that leaves the MCP onto a CCD, page 42

IDL Interactive Data Language. A programming language that is used for data analysis and image processing, licensed by Exelis Visual Information Solutions (Exelis Visual Information Solutions, 2014), page 119

IMF Initial mass function. A function that describes the distribution of the initial masses in a population of stars., page 4

IUE International Ultraviolet Explorer. Very successful satellite observatory that was a joint-venture between NASA, ESA and the UK. It was in operation from 1978 to 1996 (European Space Agency, 2014). IUE was the first real observatory-type UV satellite, page 13

JTAG Joint Test Action Group. Common name for the IEEE programming interface standard *Standard Test Access Port and Boundary Scan Architecture*. Developed to debug and test PCBs and ICs.

Used for example to configure the VHDL firmware design content of an FPGA, page 83

LDR Local dynamic range. Defined as the maximum flux level in a narrow area of a detector minus the faintest level that is three standard deviations above the background in acceptable integration times (Joseph, 1995), page 24

LTCC Low temperature cofired ceramics. Specific type of ceramics that is used for the cross strip anodes and `Beetle` chip ceramics hybrid carrier boards, page 52

MCP Micro channel plate. Thin plate of lead-oxide glass that has many microscopic channels than run from one face of the plate to the other face. A high electric potential that is applied causes the MCP to act as a multiplier for photoelectrons, page 23

NUV Near-UV. Part of the UV wavelength band between 200 nm and 300 nm, page 1

OAO Orbiting Astronomical Observatory. A series of four satellite observatories that performed the first observations in UV light. They have been launched by NASA between 1966 and 1972 (Code et al., 1970; Rogerson et al., 1973; Snow, 1975), page 12

OM Optical and UV Monitor. Imaging and low-resolution spectroscopy instrument on-board XMM-Newton X-ray observatory (Mason et al., 2001; Talavera, 2009), page 16

ORFEUS Orbiting Retrievable Far and Extreme Ultraviolet Spectrometers. Instruments on the retrievable ASTRO-SPAS platform which was built by Messerschmitt-Bölkow-Blohm (now a part of EADS) and managed by DARA (today: DLR). The telescope and instruments were manufactured by Kayser-Threde GmbH (now: OHB System AG). ORFEUS incorporated two spectrometer channels developed in Germany and the United States and was part of two shuttle missions in 1993 and 1996 (Mandel et al., 1994; Grewing et al., 1998; Barnstedt et al., 1999), page 13

PCB Printed circuit board. Used to mechanically support and electronically connect electronic components. The connections are done

by means of pads and tracks that are etched off copper layers on non-conducting supporting substrates, page 51

PMCD Phase-matched clock divider. One type of clocking resource that is available on the `Virtex-4` FPGA as a hardware macro cell. Its purpose is to provide clock signals that have a period which is an integer ratio of an input clock signal. In addition, up to three additional clock signals can be fed into the PMCD and delayed to match the modified clock signal, page 94

PROM Programmable read-only memory. Particular form of data storage technology. Data is written into the device after manufacture and is permanent and hence also there after the power is removed, page 83

SEU Single event upset. A soft error that is for example a bit flip in a storage element as a register or a memory cell. It is caused by ionizing radiation that penetrates the semiconductor material, page 74

Spektrum-R Also called `Radioastron`. Russian satellite observatory to perform observations for radio astronomy. It was launched in July 2011 (RadioAstron Science and Technical Operations Group, 2014), page 19

Spektrum-RG International high-energy astrophysics satellite under Russian leadership. The launch is scheduled for 2016, page 19

SPICE Simulation Program with Integrated Circuit Emphasis. A general-purpose, open source analog electronic circuit simulator. It was developed by Nagel and Pederson (1973) at the University of California. SPICE is used to check the integrity of analog circuits and predict the behavior of circuit designs, page 135

SSL Space Science Laboratory of the University of California in Berkeley, page 45

STIS Space Telescope Imaging Spectrograph. Instrument in operation on HST for two-dimensional spectroscopy in the band between 105 nm and 1000 nm, page 16

STS Space Transportation System. Also known as NASA's manned Space Shuttle Program. It lasted from 1981 to 2011. The Space Shuttle Orbiter could carry four to seven astronauts and launched vertically attached to an external tank and solid boosters. 135 missions have been flown of which two have been lost in 1986 and 2003, page 13

UCM USB communicator module. A specific module of the front-end electronics VHDL firmware design. It provides the access to the `FT232H` USB chip connected to the `Virtex-4` FPGA, page 91

UHV Ultra high vacuum. A vacuum environment below 10^{-9} mbar, page 50

UV Ultraviolet spectral band of the electromagnetic radiation. A possible characterization of this band is a lower wavelength limit at the hydrogen Lyman alpha absorption edge at 91.2 nm and an upper wavelength limit at 300 nm above which the absorption of the radiation in the atmosphere of the Earth is small enough to observe by ground-based telescopes (Werner, 2010), page 1

UVIT Ultraviolet Imaging Telescope. A twin 38 cm-aperture UV instrument on board `ASTROSAT` that will perform imaging in the range from 130 nm to 530 nm, page 18

UVOT Ultra-Violet/Optical Telescope. NUV imaging space telescope on-board the Swift Gamma-Ray Burst Mission (Roming et al., 2005; Roming et al., 2009), page 16

VHDL Very high speed integrated circuit (VHSIC) hardware description language. Parallel description language standard used in electronics design to describe digital or mixed-signal systems such as FPGAs. The standard is maintained and extended by the VHDL Analysis and Standardization Group (VHDL Analysis and Standardization Group, 2009), page 63

VUV Vacuum-UV. Part of the UV wavelength band between 10 nm and 200 nm. It incorporates the EUV and FUV bands, page 1

WSA Wedge and strip anode. Particular type of a position sensitive readout anode. It allows to physically divide the charge of an

electron cloud between four electrodes that are shaped in a pattern of wedges and strips, page 36

WSO-UV World Space Observatory Ultraviolet. Upcoming space observatory that is part of the Federal Space Program of Russia. Main instrument is a 1.7 m telescope. WSO-UV will be capable of imaging and spectroscopy in the band between 115 and 310 nm (INASAN, 2014; Sachkov et al., 2014b,a), page 17

XSA Cross strip anode. Particular type of a position sensitive readout anode. It allows to physically divide the charge of an electron cloud between several electrodes, page 26

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ECSS. *SpaceWire - Links, nodes, routers and networks. ECSS-E- ST-50-12C*. ECSS - European Cooperation For Space Standardization, ESA-ESTEC Requirements & Standards Division, Noordwijk, The Netherlands, 2008.

ECSS. *SpaceWire - Remote memory access protocol. ECSS-E-ST-50-52C*. ECSS - European Cooperation For Space Standardization, ESA-ESTEC Requirements & Standards Division, Noordwijk, The Netherlands, 2010.

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