2017

Chip-scale demonstration of hybrid III-V/silicon photonic integration for an FBG interrogator

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Abstract

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Keywords

interrogator, fbg, integration, photonic, iii-v/silicon, hybrid, chip-scale, demonstration

Disciplines

Engineering | Science and Technology Studies

Publication Details

Li, H., Ma, X., Cui, B., Wang, Y., Zhang, C., Zhao, J., Zhang, Z., Tang, C. & Li, E. (2017). Chip-scale demonstration of hybrid III-V/silicon photonic integration for an FBG interrogator. Optica, 4 (7), 692-700.

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Research Article Vol. 4, No. 7 / July 2017 / Optica 692

Chip-scale demonstration of hybrid III–V/silicon photonic integration for an FBG interrogator

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Received 3 March 2017; revised 27 April 2017; accepted 16 May 2017 (Doc. ID 287893); published 22 June 2017

Silicon photonic integration is a means to produce an integrated on-chip fiber Bragg grating (FBG) interrogator. The possibility of integrating the light source, couplers, grating couplers, de-multiplexers, photodetectors (PDs), and other optical elements of the FBG interrogator into one chip may result in game-changing performance advances, considerable energy savings, and significant cost reductions. To the best of our knowledge, this paper is the first to present a hybrid silicon photonic chip based on III–V/silicon-on-insulator photonic integration for an FBG interrogator. The hybrid silicon photonic chip consists of a multiwavelength vertical-cavity surface-emitting laser array and input grating couplers, a multimode interference coupler, an arrayed waveguide grating, output grating couplers, and a PD array. The chip can serve as an FBG interrogator on a chip and offer unprecedented opportunities. With a footprint of 5 mm × 3 mm, the proposed hybrid silicon photonic chip achieves an interrogation wavelength resolution of approximately 1 pm and a wavelength accuracy of about ±10 pm. With the measured 1 pm wavelength resolution, the temperature measurement resolution of the proposed chip is approximately 0.1°C. The proposed hybrid silicon photonic chip possesses advantages in terms of cost, manufacturability, miniaturization, and performance. The chip supports applications that require extreme miniaturization down to the level of smart grains.

OCIS codes: (060.2300) Fiber measurements; (060.2370) Fiber optics sensors; (060.3735) Fiber Bragg gratings; (130.3120) Integrated optics devices.

https://doi.org/10.1364/OPTICA.4.000692

1. INTRODUCTION

A fiber Bragg grating (FBG) is an optical sensor embedded within the core of a standard, single-mode optical fiber using spatially varying patterns of intense UV laser light. To use an FBG as a sensor, it is illuminated by a light source and the reflected wavelength is measured and related to local measurands of interest [1,2]. Shifts in Bragg wavelength can be monitored by any of the following analytical instruments: spectrometer is the most important and widely used instrument in current laboratories for measuring light intensity as a function of the reflected wavelength of the FBG. However, this instrument has several disadvantages, including low wavelength resolution (typically in dozens of picometers) and extensive but slow interrogation; these disadvantages arise from the need to scan and sample the spectral signal to be measured. FBG interrogators are accurate measuring instruments for rapid and high-resolution interrogation of the spectral shift detected by FBG sensors, and provide a complete and reliable resolution to the FBG sensor measurement system. Various FBG interrogation techniques have been developed, including matched grating interrogation [3,4], tunable fiber Fabry–Perot filter interrogation [5,6], unbalanced Mach–Zehnder interferometer interrogation [7,8], tunable narrow-linewidth laser-scanning interrogation [9], and arrayed waveguide grating (AWG) interrogation [10,11]. However, spectrometers and FBG interrogators have several disadvantages, including bulky sizes and high costs, which severely limit the popularization and application of the FBG sensing technology.

Users search for small, low-cost, and extremely ruggedized FBG interrogators for use in FBG sensor interrogator applications. The need for data captured in the field and the ubiquitous use of sensors for *in situ* monitoring of systems and environments drive this demand. In recent years, silicon photonic integration technology has achieved considerable advancements, and the components of salient silicon photonic devices currently meet relevant commercial standards [12–21]. The development of silicon

photonics facilitates the establishment of a feasible technique for miniaturization of optical systems [22–27]. Several silicon-on-insulator (SOI)-based spectrometers have been explored for mid-infrared [28–30] and short-infrared [31] operational wavelength ranges. Spectrometers have been significantly improved via hybrid photonic integration; however, integrated hybrid photonic spectrometers still require a connection to external light sources and photodetectors (PDs) to run. With photonic integrated technologies, FBG interrogators could possibly use a miniaturized photonic integrated circuit [32–34]. Photonic integration of the AWG interrogator has been developed to integrate an InGaAsP/InP light-emitting diode as a light source, but the approach exhibited inherent disadvantages, such as low output power and high drive current [35]. Vertical-cavity surface-emitting lasers (VCSELs) possess simplicity, high power at low drive current, easy coupling, and favorable spectral characteristics. In this study, we propose that hybrid III–V/silicon photonic integration for an FBG interrogator with VCSELs as the light source can be achieved on an SOI platform. Thereafter, we experimentally demonstrate its use. With a footprint of 5 mm × 3 mm, the hybrid silicon photonic chip achieves an interrogation wavelength resolution of approximately 1 pm and a wavelength accuracy of about ±10 pm. With the measured 1 pm wavelength resolution, the temperature measurement resolution of this chip is approximately 0.1°C. The use of hybrid silicon photonic integration allows a high level of integration and facilitates the commercial utilization of hybrid silicon photonics for FBG interrogators.

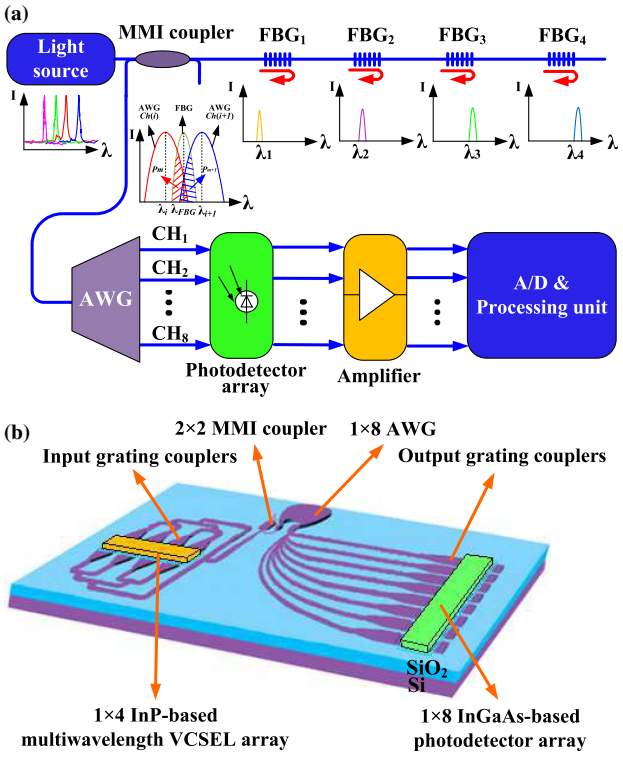

Fig. 1. Schematic of the proposed AWG interrogation system and hybrid silicon photonic chip structure. (a) Schematic of the AWG interrogation of FBG sensors. (b) Hybrid silicon photonic chip structure based on III–V/SOI photonic integration for the AWG interrogation of FBG sensors.

2. CHIP DESIGN AND FABRICATION

A. Interrogation Principle and Chip Structure

The proposed AWG interrogator of FBG sensors consists of a light source, a 2 × 2 multimode interference (MMI) coupler, four FBG distributed sensors, a 1 × 8 AWG, a 1 × 8 PD array, subsequent signal amplification circuits, an analog-to-digital (A/D) converter, and a data-processing unit [Fig. 1(a)]. When an FBG reflection spectrum passes through adjacent channels of the AWG, the FBG reflection spectrum overlaps with the transmission spectrum of the two AWG adjacent channels. P_i and P_{i+1} are two adjacent channels with the output light intensity of the AWG; they are the convolutions of the FBG reflection spectrum and the AWG adjacent channel transmission spectrum, respectively. When the channels of the AWG have the same transmission coefficient and half-peak bandwidths, a relationship exists between the adjacent channel light intensity ratio logarithm of the AWG and the FBG central wavelength. When the FBG is under constant stress, λ_{FBG} exhibits a linear relationship with temperature. The temperature change can be measured in real time by measuring the dual-channel light intensity and calculating the logarithm of the light intensity ratio. A schematic of the hybrid silicon photonic chip based on III–V/SOI photonic integration for the AWG interrogator is shown in Fig. 1(b). As shown in the structural diagram of the hybrid silicon photonic chip, light from the 1 × 4 InP-based multiwavelength VCSEL array irradiates vertically to the input grating couplers, diffracts into the input waveguide of the 2 × 2 MMI coupler, and enters the sensing FBG array, the light of which is transmitted and reflected through the 2 × 2 MMI coupler and then guided into the 1 × 8 AWG. Spreading from the output waveguides of the 1 × 8 AWG, the light enters through the output grating couplers, and the 1 × 8 InGaAs-based PD array detects the light intensity.

B. Characterization of Optical Elements

The commercial InP-based VCSEL used in this study plays a key role in the hybrid silicon photonic chip. The III–V single-mode, single-polarization-state VCSEL light source, an integrating sphere, a near-field optical microscope, and a spectrometer were used to characterize L–I–V, optical power, and spectra, as well as analyze the pattern and divergence angle of the commercial InP-based VCSEL. We constructed a finite-difference time-domain simulation model of the commercial InP-based VCSEL by using the commercial VCSEL-related performance parameters obtained from the experiment. This model possessed an emergent beam highly similar to that of the commercial InP-based VCSEL by accurately setting the Gaussian beam waist diameter, divergence angle, and other key parameters. The boundary conditions were set to those of the perfectly matched layer. The commercial multiwavelength VCSEL array (i.e., 1547.8, 1549.2, 1550.6, and 1552.2 nm) was used.

The key element for the interrogator of FBG sensors working in the reflection mode is an MMI coupler, which [36–38] has the advantages of a smaller footprint, lower loss, and a wider bandwidth over a cross-gap coupler and an X coupler. The splitting ratio of the coupler should be 50:50 to obtain maximum power for the subsequent AWG. The input/output waveguides are tapered to enhance the clarity of the image point, improve the splitting ratio, and reduce loss. The excess loss and uniformity

of the MMI coupler after optimization can be reduced to 0.46 and 0.06 dB, respectively [Fig. 2(a)]. The MMI coupler is highly compact and exhibits low excess loss, a wide bandwidth, and good uniformity, thereby meeting photonic integration requirements.

AWG devices are typically large and expensive because they are made of polymers [39,40] and other materials, such as $LiNbO_3$ [41,42], PLZT [43,44], and InP [45]; thus, the design of an ultracompact AWG for photonic integration is particularly important. SOI-based AWGs have been extensively investigated because of their ultrahigh relative refractive index difference Δ in the Si core and low-index claddings, which render their compact structure. In this study, we designed 12 types of 1 × 8 ultracompact AWGs on SOI (see Fig. S1, Supplement 1). The parameters considered for optimizing the design of the AWGs were adopted in the simulation using the beam propagation method. These parameters included insertion loss, loss uniformity, crosstalk, and passband width. The simulation result of the selected AWG used in the hybrid silicon photonic chip is shown in Fig. 2(b). The selected traditionally shaped AWG exhibits a central channel loss of −3 dB, a non-uniformity of 0.4 dB, and a crosstalk level of −25 dB.

We designed an input grating coupler comprising an optical waveguide and a grating formed on the optical waveguide, in which light is bidirectionally propagated for the optically coupled light rays inside and outside the optical waveguide. When designing a grating coupler, the performance should be optimized by appropriately setting various parameters, such as grating period, duty cycle, and etch depth. For the input grating coupler, we set the grating period to 570 nm, the duty cycle to 0.5, and the etch depth to 80 nm (see Fig. S2, Supplement 1). After optimizing the pitch of the input grating coupler and the duty cycle of the grating and following the technical dimension requirements of the Institute of Microelectronics (IME), we selected 285 nm as the grating groove width. The light-emitting surface of the VCSEL and the input grating coupler have the same length, thereby facilitating the matching of the input grating coupler. The thickness of the benzocyclobutene (BCB) layer was optimized at 440 nm to ensure the high coupling efficiency of the output waveguide. The relationship between coupling efficiency and incident light wavelength is shown in Fig. 2(c). The coupling efficiencies reached 72.4% at a wavelength of 1550 nm. The VCSEL and the optical interface of the grating coupler were co-simulated to optimize the design of the vertical optical interface and, consequently, realize mode-field matching and high-efficiency coupling with the actual VCSEL. The structure was simulated at an incident angle of 0°. We used input grating couplers to couple the lights from the 1 × 4 InP-based multiwavelength VCSEL array to the waveguide and the lights from different waveguides. Waveguide bends were specially designed to combine the lights according to a matching condition to suppress mode distortion and other undesirable effects. The bend was structured in consideration of its length and curvature. This approach suppresses mode distortion, transition losses, and other negative effects of waveguide bends. A schematic of the proposed combiners is shown in Fig. 2(d). The lights originating from the 1 × 4 multiwavelength VCSEL array are diffracted bidirectionally and coupled into the fundamental mode of the 0.65-μm-wide waveguides on each end of the input grating

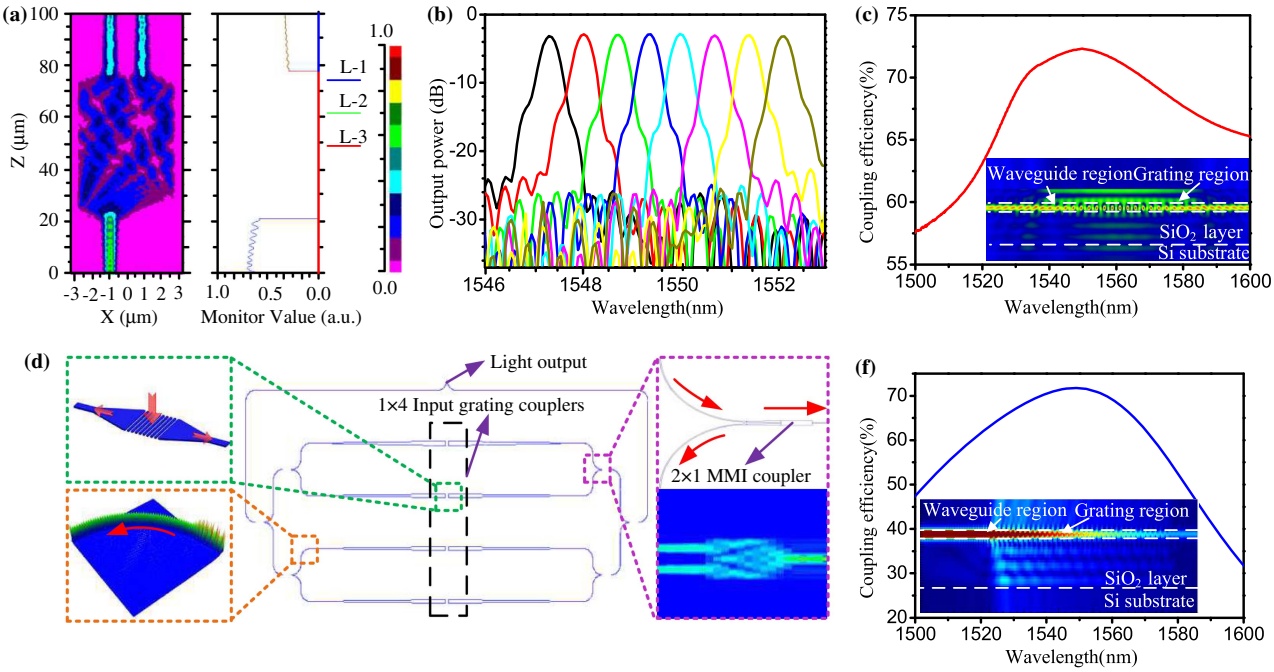

Fig. 2. Optical element simulation results of the hybrid silicon photonic chip for the AWG interrogator. (a) Optical field and output power of the MMI coupler with a tapered input/output waveguide. L-1 represents the light power of the input waveguide of the MMI coupler; L-2 represents the light power of the left output waveguide of the MMI coupler; and L-3 represents the light power of the right output waveguide of the MMI coupler. (b) Simulated optical response of the SOI AWG centered at approximately 1550 nm with eight output channels. Different colors denote different channels. (c) Input grating coupling efficiency with respect to wavelength. (Inset) Simulated output optical fields of the input grating coupler and VCSEL. (d) Schematic of the proposed combiners using the bent waveguides. The bend radius and angle are 51 μm and 90°, respectively. The width of each bent waveguide is 0.65 μm. (e) Output grating coupling efficiency with respect to wavelength. (Inset) Simulated output optical field of the output grating coupler.

coupler. The bend radius and angle of the waveguide bands are 51 μm and 90°, respectively. The mode-field profile of the waveguide was successfully designed to match the mode of the VCSEL. The coupling efficiencies of the bent waveguides reached 96.13% at a wavelength of 1550 nm.

Output grating couplers were used in the silicon-based hybrid integrated PD array. We selected 700 nm as the grating period, 0.7 as the duty cycle, 100 nm as the etch depth, and 210 nm as the grating groove width (see Fig. S3, Supplement 1). The photosensitive area of the PD used in this study is a circle with a diameter of 55 μm. Thus, the grating length was fixed at 25 μm in the simulation. A 1 × 8 PD array was bonded onto the grating couplers with a spin-coated BCB layer in the middle to construct the silicon-based hybrid integrated PDs. We optimized the thicknesses of the SiO_2 buffer and BCB layers, which exerted reflection and antireflection effects on power absorption efficiency, to 2 μm and 440 nm, respectively. The relationship between coupling efficiency and incident light wavelength is shown in Fig. 2(e). The coupling efficiencies reached 71% at a wavelength of 1550 nm.

C. Fabrication and Adhesive Bonding

The hybrid silicon photonic chip was fabricated at IME [Fig. 3(a)]. The initial substrate for the silicon photonic technology was an SOI substrate with a 220 nm top crystalline Si layer and a 2 μm buried oxide layer. Scanning electron microscopy (SEM) images of the fabricated optical elements are shown in Fig. 3(b)–3(f). Figures 3(g) and 3(h) show a micrograph of a 1 × 4 multiwavelength VCSEL array and that of a 1 × 8 PD array, respectively.

Integration of III–V compound semiconductors on the top of the SOI chip results in complex active/passive photonic integrated circuits. To obtain these circuits, the III–V materials must be transferred to the silicon waveguide chip. Adhesive bonding with organic materials, i.e., BCB [46–48] or SU-8 [49,50], is a simple process, which allows the construction of the hybrid silicon photonic chip for the AWG interrogator. The bonding procedure is based on the polymerization reaction of organic molecules to form long polymer chains during annealing. This cross-link reaction causes BCB and SU-8 to form a solid polymer layer. The intermediate layer is used by spin on, spray on, screen printing, embossing, dispensing, or block printing on one or two substrate surfaces. The adhesive layer thickness depends on the viscosity of the adhesive, rotational speed, and tool pressure. The thickness of the BCB layer in this study was optimized at 440 nm to ensure high coupling efficiency of the input/output waveguide (see Fig. S4, Supplement 1).

We adopted adhesive bonding technology to integrate the III–V compound semiconductors on the top of the SOI waveguide chip. The SOI chip surface was pretreated as follows: a mixed solution with concentrated sulfuric acid/aqua hydrogenii dioxidi (H_2SO_4/H_2O_2) in a ratio of 3:1 was prepared. The SOI chip was immersed in the mixed solution and heated for 5 min. The chip was then removed from the solution and naturally cooled. The VCSEL and PD chips were pretreated as follows: a mixed solution with hydrofluoric acid/water in a ratio of 1:10 was prepared. The VCSEL and PD chips were immersed in the mixed solution for hydrophilic treatment. The chips were then removed from the solution and washed. After washing, the adhesion promoter AP-3000 was applied to the SOI chip surface by spin coating and then preheated in a constant-heat oven at

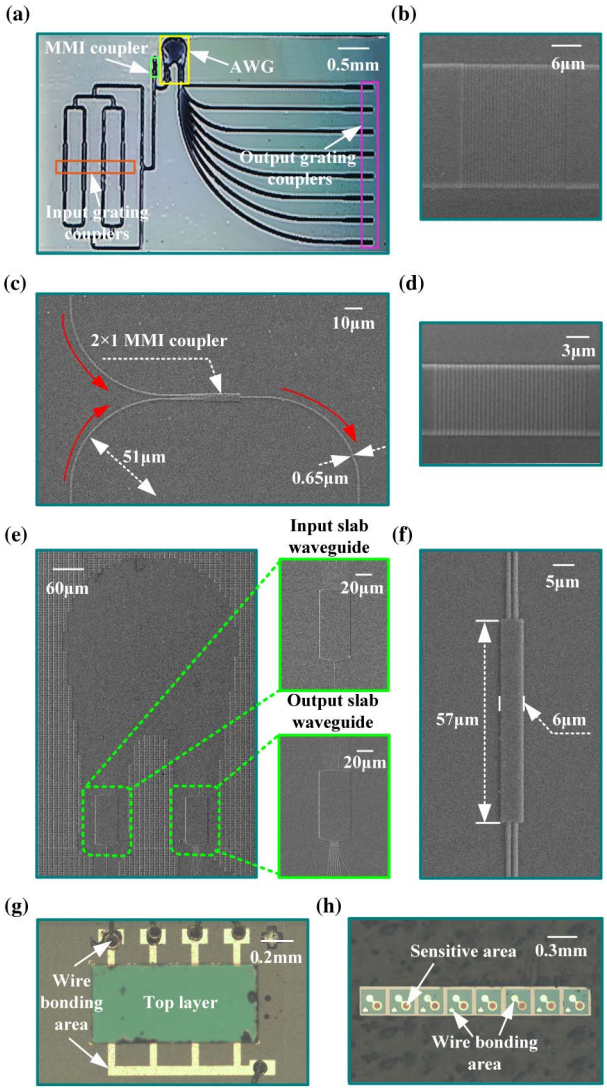

Fig. 3. (a) Micrograph of the final fabricated 5 mm × 3 mm proof-of-concept silicon photonic chip. (b) SEM image of the input grating coupler with a footprint of 17 μm × 20 μm. (c) SEM image of the 2 × 1 MMI coupler with a footprint of 20 μm × 6 μm and the bent waveguides with a diameter of 51 μm. (d) SEM image of the output grating coupler with a footprint of 25 μm × 10 μm. (e) SEM image of the 1 × 8 AWG with a footprint of 300 μm × 570 μm. (f) SEM image of the 2 × 2 MMI coupler with a footprint of 57 μm × 6 μm. (g) Micrograph of the 1 × 4 multi-wavelength VCSEL array with a footprint of 0.45 mm × 1 mm (light-emitting area with a diameter of 10 μm in the back). (h) Micrograph of the 1 × 8 PD array with a footprint of 0.3 mm × 2.4 mm (sensitive area with a diameter of 55 μm).

95°C for 2 min. Spin coating was performed by aggressive fluid expulsion from the SOI chip surface while controlling the spin speed and colloid concentration to achieve a uniform and desired thickness. A mixed solution was prepared with BCB and trimethyl benzene after dilution. After spin coating, the SOI chip was heated at 150°C until trimethyl benzene was completely vaporized. In an ultraclean environment, the VCSEL and PD chips were inverted onto the grating coupler corresponding to the SOI chip. Subsequently, the chips were bonded together, placed in an oven, and heated at 170°C for 30 min. The placement of the VCSEL and PD chips can be modified slightly during

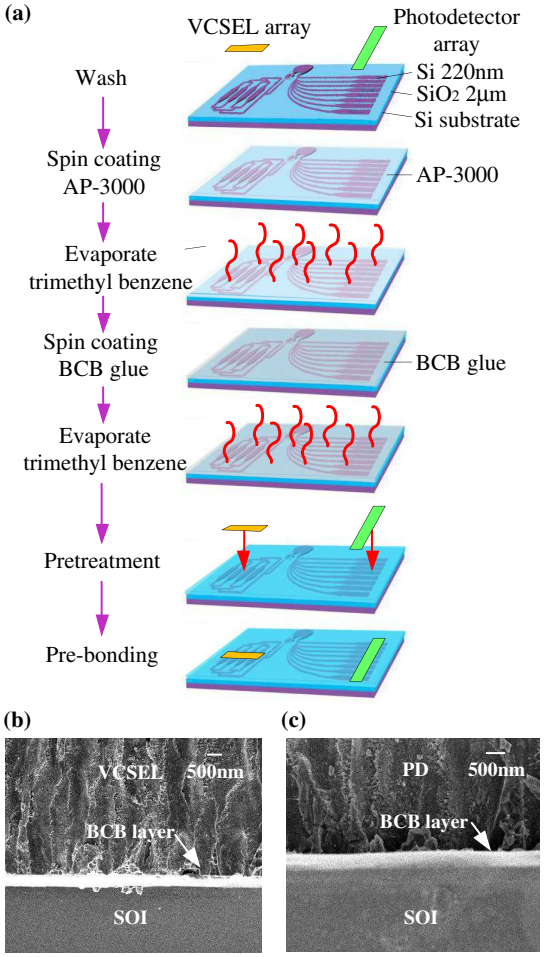

Fig. 4. (a) Schematic of the III–V-to-SOI adhesive bonding process flow. (b) SEM cross section of the SOI/BCB/VCSEL structure after bonding. (c) SEM cross section of the SOI/BCB/PD structure after bonding.

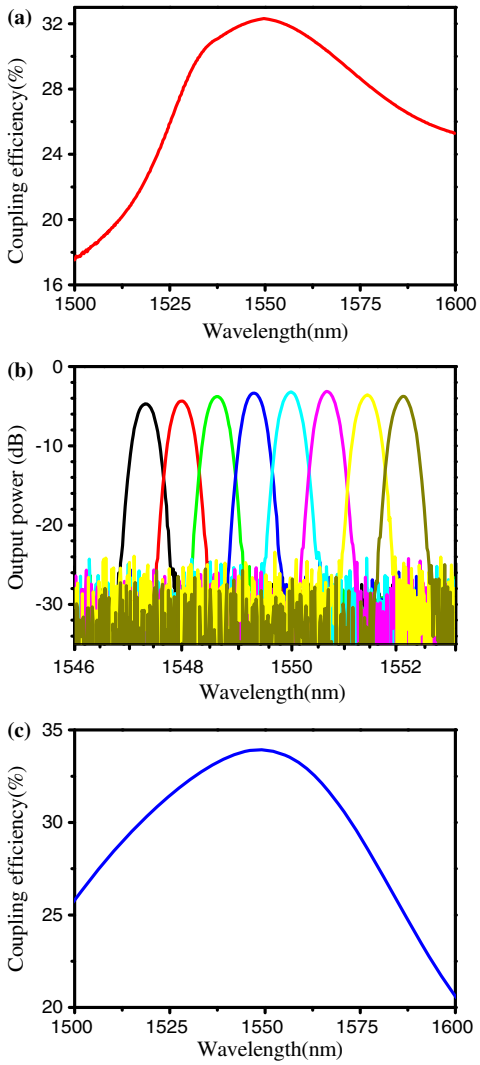

Fig. 5. Optical experimental results of the AWG and input/output grating coupler. (a) Experimentally measured input grating coupling efficiency with respect to wavelength. (b) Experimentally measured optical response of the SOI AWG centered around 1550 nm with eight output channels. Different colors denote different channels. (c) Experimentally measured output grating coupling efficiency with respect to wavelength.

the process to ensure seamless bonding. Figure 4(a) shows the bonding process flow of the III–V-to-SOI process in fabricating the hybrid silicon photonic chip. Figures 4(b) and 4(c) show SEM cross sections of the SOI/BCB/VCSEL and the SOI/BCB/PD structure after bonding, respectively.

3. EXPERIMENTAL RESULTS

A. Experiments of Optical Elements

The optical experiments indicated that the fabricated input grating coupler could sufficiently couple light to the waveguide, and the efficiency of coupling 1550 nm light to the in-plane waveguides reached a maximum of 32.4% with a 3 dB bandwidth of 39 nm [Fig. 5(a)]. The excess loss of the MMI coupler after fabrication was reduced to 0.45 dB and the uniformity decreased to 0.07 dB (see Fig. S5, Supplement 1). The fabricated traditionally shaped AWG with a 0.45-μm-wide waveguide exhibited the best transmission spectra. It also presented a central channel loss of −3.18 dB, a non-uniformity of 0.8 dB, and a crosstalk level of −23.1 dB [Fig. 5(b)]. The coupling efficiency of the fabricated output grating coupler reached a maximum of 33.6% with a 3 dB bandwidth of 38 nm when 1550 nm light was coupled, as shown in Fig. 5(c).

Given that a commercial VCSEL with an input voltage of 2 V and a current of 3 mA was used, the average output luminous power P_L was approximately 0.8 mW, which is equivalent to −1 dBm (see Fig. S6, Supplement 1). A PIN PD with a spectral response range of 1100–1650 nm was used in the photonic integration. The average response of the light in the vicinity of 1550 nm was 0.98 A/W. The minimum induced light intensity was 10 nW (−50 dBm) and the dark current was 0.1 nA. For the hybrid silicon photonic chip, if the estimated link power can meet the required sensitivity of the back-end receptor PD array, then the optical path is feasible in the entire chip.

The total link insertion loss IL of the chip is the summation of the input grating coupler loss $IL_{C\text{-in}}$, the total transmission loss of the 10 bent waveguides IL_{W1}, the input coupler loss of the straight waveguides IL_{W2}, the insertion loss of the three 2 × 1 MMI couplers IL_{MMI1}, the insertion loss of the 2 × 2 MMI

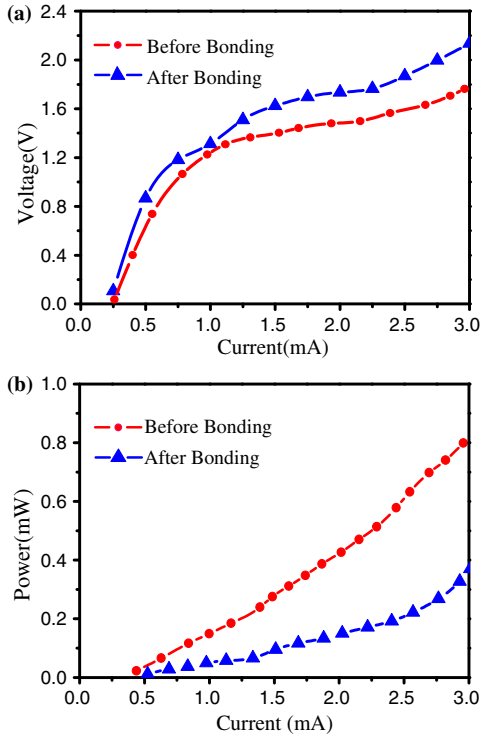

Fig. 6. Comparison of (a) the V–I curve and (b) the L–I curve of the VCSEL before and after bonding with the hybrid silicon photonic chip for AWG interrogation.

coupler IL_{MMI2}, the reflection loss of the FBG IL_{FBG}, the transmission loss of the AWG IL_{AWG}, and the output grating coupler loss IL_{C-out}.

The measurement results of the optical experiments indicated that IL_{C-in} is −4.89 dB, IL_{W1} is −5.90 dB, IL_{MMI1} is −5.61 dB, IL_{MMI2} is −3.46 dB, IL_{FBG} is −12.09 dB, IL_{AWG} is −3.18 dB, and IL_{C-out} is −4.74 dB. When the mean transmission loss of the straight waveguides is −3.04 dB/cm and the mean length is 0.75 cm, IL_{W2} is −2.28 dB. The IL of the entire chip is −42.15 dB. The minimum optical power detected by the PD array is −50.00 dBm; thus, the input optical power must be maintained above −7.85 dBm. A single VCSEL with maximum output power of −1 dBm can meet the theoretical design. Therefore, the optical path of the hybrid silicon photonic chip is proven feasible by the theoretical calculation of the total link insertion loss. Corresponding to four FBGs, a 1 × 4 multiwavelength VCSEL array was specifically designed in this study.

B. Experiments of VCSEL L–I–V Comparison

To verify the functionality of the VCSEL, its electrical and optical characteristics were measured before and after bonding with the silicon photonic chip for the AWG interrogator. The current–voltage (I–V) curves of the VCSEL were measured, as shown in Fig. 6(a). Similar behavior was observed for the VCSEL in both cases. However, the electrical performance of the VCSEL showed changes after bonding with the silicon photonic chip. Reasons for these changes include high-temperature aging when bonding with the silicon photonic chip, the heat dissipation effect after bonding, and the influence on the VCSEL structure after bonding. Figure 6(b) depicts the light–current (L–I) curves of the VCSEL before and after bonding. The measured optical power matched well in the two cases, illustrating the successful functioning of the bonded devices. The optical signal showed increased attenuation after bonding with the silicon photonic chip because the signal

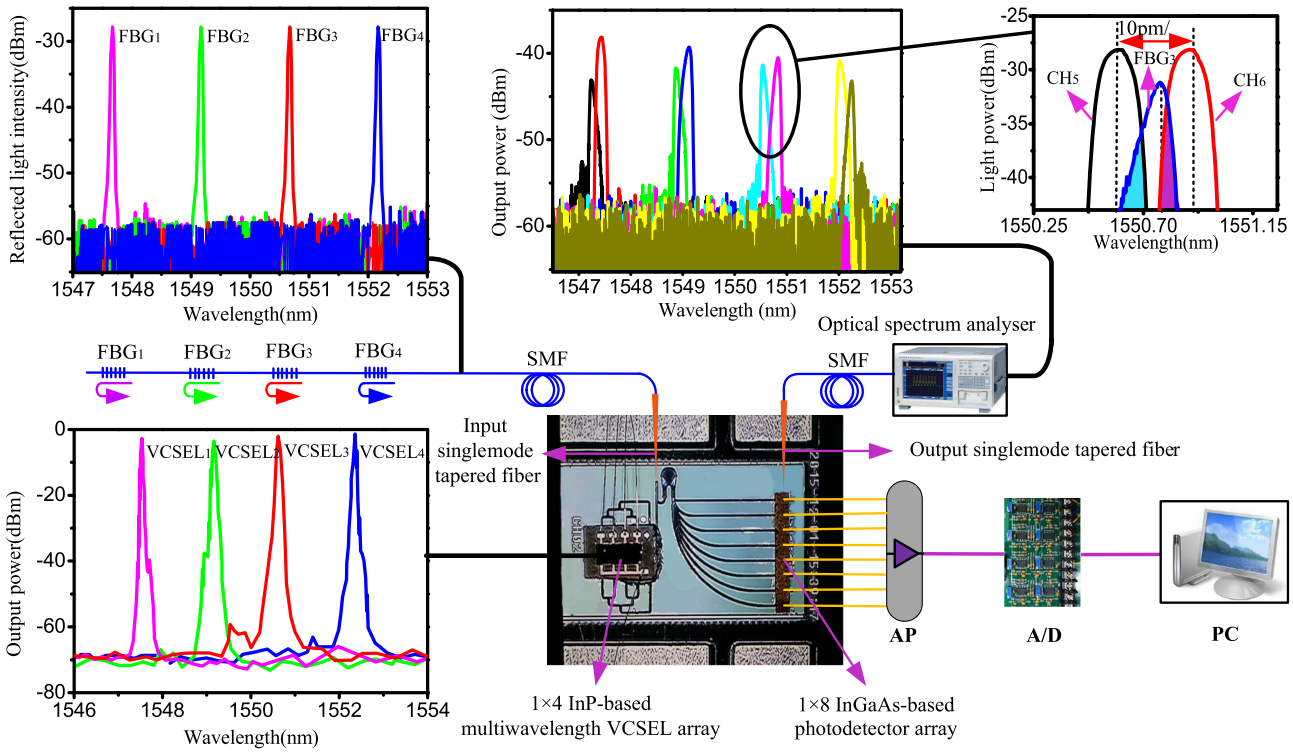

Fig. 7. (a) Interrogation experiments and measurements of the optical response results. The Bragg wavelength shift against temperature change in the wavelength range is about 10 pm/°C. AP, amplification and conditioning circuit; A/D, ADS8345; PC, computer.

was measured after coupling by the BCB bonding layer and input grating.

The effect of ambient temperature on the proposed photonic integrated chip was considered. VCSEL operations affect the performance of the entire chip directly. Only under constant temperatures can VCSELs perform stably; otherwise, their output wavelengths and power efficiencies would change dramatically. Effective control of the temperatures of these components is required to stabilize their optical parameters. Therefore, temperature control is an important task in the design process. During our study, we simplified the experimental conditions and completed the validation test of key parameters. A Peltier device, namely, a thermoelectric cooler (TEC), is usually employed in a laser module to stabilize the operational temperature of the laser. For our next step, we will design TEC control functions to meet the requirements of the proposed photonic integrated chip.

C. FBG Temperature Interrogation Experiment

At an ambient temperature of 25°C, the temperature was measured with four FBG sensors. In the interrogation experiment on the FBG wavelength shift signals, four FBG central wavelengths (i.e., 1547.7, 1549.2, 1550.6, and 1552.1 nm) were used. An ADS8345 chip was used for A/D conversion and the sampling frequency was set to 2 kHz. When the reflection light of the FBG penetrated the AWG during AWG interrogation, the light with a different wavelength separated and traveled to different adjacent array waveguides. P_i and P_{i+1} are two adjacent channels of the output light intensity of the AWG, and they are the convolutions of the FBG reflection spectrum and the AWG adjacent channel transmission spectrum, respectively. The expressions of P_i and P_{i+1} can be written as Eqs. (1) and (2), respectively:

$$P_i = (1 - L_i) \int_0^\infty S(\lambda)\dot{R}_{\mathrm{FBG}}(\lambda)\dot{T}_{\mathrm{AWG}}(i,\lambda)\mathrm{d}\lambda, \quad (1)$$

$$P_{i+1} = (1 - L_{i+1}) \int_0^\infty S(\lambda)\dot{R}_{\mathrm{FBG}}(\lambda)\dot{T}_{\mathrm{AWG}}(i+1,\lambda)\mathrm{d}\lambda. \quad (2)$$

In Eqs. (1) and (2), $S(\lambda)$ is the output power spectrum of the light source, with the assumption that the output power is constant, S0, within the AWG bandwidth, and L_i and L_{i+1} are the light attenuation coefficients. $R_{\mathrm{FBG}}(\lambda)$ is the reflection spectrum function of the sensory grating, $T_{\mathrm{AWG}}(i,\lambda)$ and $T_{\mathrm{AWG}}(i+1,\lambda)$ are the AWG channels, and i and $i+1$ are the transmission spectrum functions in the FBG interrogation system. The ratio of the light intensity in the adjacent channels i and $i+1$ measures the center wavelength of the reflection peak of the FBG sensor. The relationship between the adjacent channel light intensity ratio logarithm of AWG and that of the FBG central wavelength can be written as

$$\ln\left(\frac{p_{i+1}}{p_i}\right) = \frac{8(\ln 2)\Delta\lambda}{\Delta\lambda_i^2 + \Delta\lambda_{\mathrm{FBG}}^2}\lambda_{\mathrm{FBG}} - \frac{4(\ln 2)(\lambda_{i+1}^2 - \lambda_i^2)}{\Delta\lambda_i^2 + \Delta\lambda_{\mathrm{FBG}}^2}, \quad (3)$$

where $\Delta\lambda_i$ is the half-peak bandwidth of the AWG Gaussian spectrum. $\Delta\lambda_{i+1}$ is the adjacent two-channel central wavelength difference of the AWG at the initial temperature. With constant stress on FBG, λ_{FBG} exhibits a linear relationship with temperature. λ_i and λ_{i+1} are, respectively, the central wavelengths of the i and $i+1$ channels of the AWG. The FBG_3 reflection spectrum and the AWG adjacent channel (CH_5 and CH_6) transmission spectrum are shown in the top right corner in Fig. 7. The Bragg wavelength shift against temperature change in the wavelength range is approximately 10 pm/°C. We first measured the optical response and then the interrogation results after the VCSEL and PD arrays were bonded to the silicon photonic chip, as shown in Fig. 7.

The separate channel of the light signal is converted into a voltage signal after undergoing photoelectric conversion, amplification, and filtering. The voltage signal is then sent to the A/D converter and microcontroller. The quantization error of the A/D converter ADS8345 in the interrogation experiment is 0.002 V. When the output voltage of the PD changes within less than 0.002 V, the A/D converter ADS8345 becomes indistinguishable from the change. When the temperature change of the FBG sensing is 0.1°C, the output voltage of the photoelectric detector is approximately 0.002 V. The resolution of the FBG is approximately 10 pm/°C; hence, the temperature change that corresponds to 0.1°C can be obtained at a wavelength resolution of

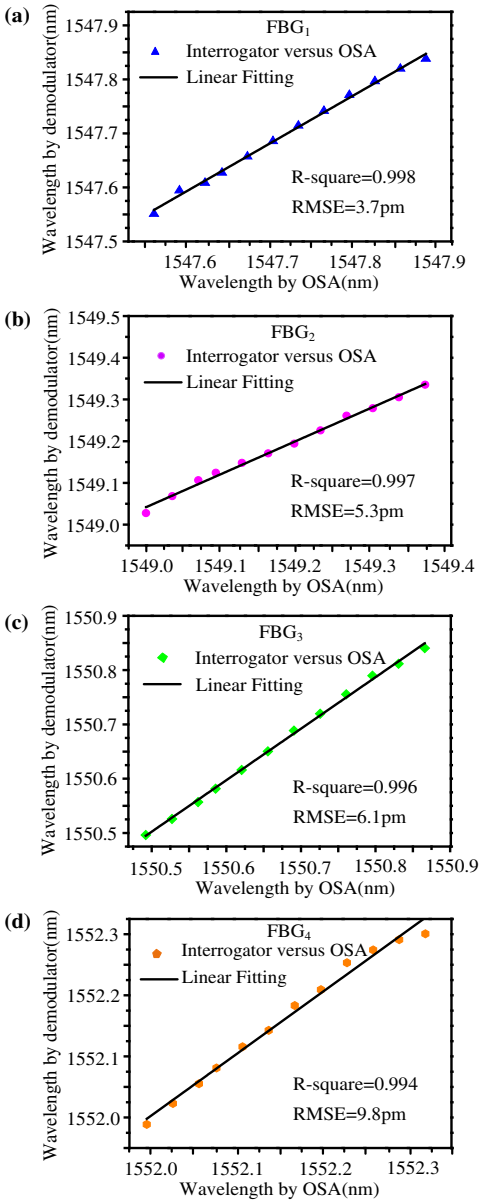

Fig. 8. Interrogation results of the temperature experiments. (a) FBG1, (b) FBG2, (c) FBG3, and (d) FBG4.

1 pm (see Fig. S7, Supplement 1). Figure 8 presents the interrogation results of the temperature experiments. The x axis represents the wavelength measured by an optical spectrum analyzer (OSA), and the y axis represents the wavelength measured by the chip. As shown in Fig. 8, all root-mean-square errors are less than 10 pm. Considering this result, we can presume that the wavelength accuracy of the hybrid silicon photonic chip for the AWG interrogator is about ±10 pm. For the measurable temperature range, experimental results show that temperature measurement can be performed between 5°C and 80°C, and high accuracy is obtained in the range of 20°C–55°C (see Fig. S7, Supplement 1).

4. CONCLUSIONS

We proposed a hybrid silicon photonic chip based on III–V/SOI photonic integration for the AWG interrogator of FBG sensors and experimentally demonstrated its use. The hybrid silicon photonic chip has a footprint of 5 mm × 3 mm, an interrogation wavelength resolution of approximately 1 pm, and a wavelength accuracy of roughly ±10 pm. With the measured wavelength resolution of 1 pm, its temperature measurement resolution is approximately 0.1°C, which is sufficiently accurate for many applications. The presented chip can serve as an FBG interrogator on a chip and offer unprecedented opportunities. The results of this study can serve as a basis for future studies on all-Si-based optoelectronic integration on the interrogation of FBG sensors. Moreover, integrated photonic chips can be produced at a large scale and low cost with the use of mature semiconductor technologies.

Funding. National Natural Science Foundation of China (NSFC) (31271871, 61177078, 61504093, 61675154); Opened Fund of the State Key Laboratory on Integrated Optoelectronics (IOSKL2014KF15).

Acknowledgment. Hongqiang Li proposed and guided the overall project with contributions from Xiangdong Ma; the devices were designed by Hongqiang Li, Xiangdong Ma, and Beibei Cui. Xiangdong Ma and Beibei Cui carried out the device fabrication and device characterization. Youxi Wang, Cheng Zhang, and Junfa Zhao participated in the design of the modulation experiments. Chunxiao Tang, Zanyun Zhang, and Enbang Li performed the optical measurements and analyzed the data. All authors read and approved the final paper.

See Supplement 1 for supporting content.

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