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Optimization of Nonlinear Switch Cells for Switching Converters

Bradley Alan Reese
University of Arkansas, Fayetteville

OPTIMIZATION OF NONLINEAR SWITCH CELLS FOR SWITCHING CONVERTERS

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By

Bradley A. Reese
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Abstract

Switch cells consist of an array of power switches and passive components which can replace the main switches alone in many power topologies, allowing reduced switching loss without altering the power topology directly. This thesis discusses the development of a switch cell topology that utilizes a saturable resonant inductor to reduce the size and power loss of the cell. Additionally, the cell transfers energy stored in the inductor into a capacitor for efficient energy storage during the cell's conduction region. This energy is then transferred back to the system when the cell turns off, thus reducing the total switching energy.

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Thesis Director:

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Dr. Simon Ang

Thesis Committee:

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Dedicated to my daughter, Presley

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CHAPTER 1
INTRODUCTION

Generally, higher switching frequencies lead to miniaturization of power systems and allow higher control bandwidths. However, higher switching frequency typically generates higher losses and higher temperature rises in components. Soft switching is one means of extending the switching frequency and/or increasing efficiency of a power system [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13]. However, soft switching topologies increase complexity and cost of a system.

Figure 1.1 shows a comparison of the resulting weight (red) and efficiency (blue) of a 1.3 kW dc-dc converter operating under hard switching (top) and soft switching (bottom). This analysis was performed in the first phase of the program funding this research. The minimum targeted efficiency for this system was 96 % (lower limit of efficiency axis) and the maximum targeted weight was 480 g (upper limit of the weight axis). A valid design for this system must have efficiency and weight traces within these limits simultaneously at a given switching frequency. Notice in the hard switching case that the efficiency decreases very rapidly with increasing switching frequency. This design space leaves very little room for error and results in non-optimal converter weight. In the soft switching case, the efficiency decreases at a much slower rate, allowing a large range of valid design points. The targeted power converter will also get a boost in power density (not shown) if it is allowed to have a control bandwidth >40 kHz. To achieve a bandwidth of this magnitude, the switching frequency must be at least 200 kHz. The hard switching design is not able to achieve 200 kHz while staying within the efficiency target. However, the soft switching design achieves this easily within a reasonable margin of the targeted efficiency. Furthermore, this switching frequency is at the knee of the weight curve, where further increases in frequency produce diminishing returns in weight loss.

Figure 1.2 compares hard switching (a) to zero-voltage switching (ZVS) soft switching (b) and zero-current switching (ZCS) soft switching (c) [7]. In the hard switching case, the switch voltage and current completely overlap. Assuming linear transitions on both voltage and current, the power waveform will be triangular in the transient region. Since this power is dissipated at every

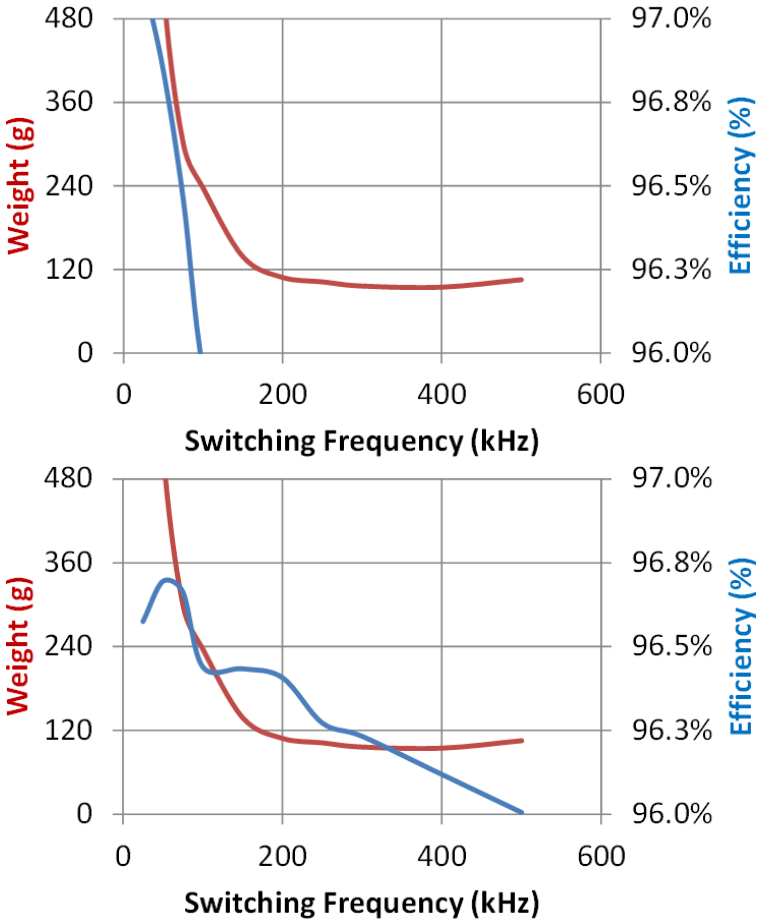


Figure 1.1: Weight and efficiency comparison of a 1.3 kW dc-dc converter under hard switching (top) and soft switching (bottom).

transition, the average switching loss is proportional to the switching frequency. Soft switching techniques seek to reduce this power loss by reducing the amount of overlap between the voltage and current waveforms. "True" soft switching is characterized by zero overlap, resulting in zero switching loss in that transition. "Pseudo" soft switching occurs when the overlap is reduced (i.e., non-zero) resulting in a reduction in switching loss. The switch cell presented in this thesis utilizes a combination of pseudo and true ZVS and ZCS effects to reduce switching loss in the main and auxiliary switch positions.

True soft switching is typically achieved by the action of external circuitry, such as auxiliary switches, passive resonance, or inherent characteristics of a particular power topology [1, 4, 6, 13, 5]. For example, a synchronous rectifier in a buck converter will turn on under true ZVS because the output inductor forces the switch's drain low once the main switch is turned off. A series resonant full-bridge converter utilizes resonance between the transformer's leakage inductance and a series capacitor to achieve true ZCS at turn off.

Pseudo soft switching can be achieved by use of "lossless" snubbers. Figure 1.3 shows an example of a lossless turn off snubber (left) and a lossless turn on snubber (right). The turn off snubber works by redirecting the switch current into the paralleled capacitor. If the capacitance is large enough, the drain voltage will increase little before the switch completely turns off, achieving pseudo ZVS. This snubber will increase turn on losses if the switch's drain voltage is not decreased by some external means. If voltage is present, the energy stored in the capacitor will be dissipated in the switch.

The turn on snubber works by limiting the rise time of current through the switch with an inductor. If the inductance is large enough, the drain current will increase little before the switch completely turns on, achieving pseudo ZCS. The turn on snubber will increase turn off loss unless the drain current is reduced to zero by external means. If current is present, the energy stored in the inductor will cause a voltage spike on the switch as it turns off, increasing the amount of switching loss. As the capacitance and inductance of the turn off and turn on snubbers increases, respectively, the switching loss of their snubbed transition will approach true soft switching performance. How-

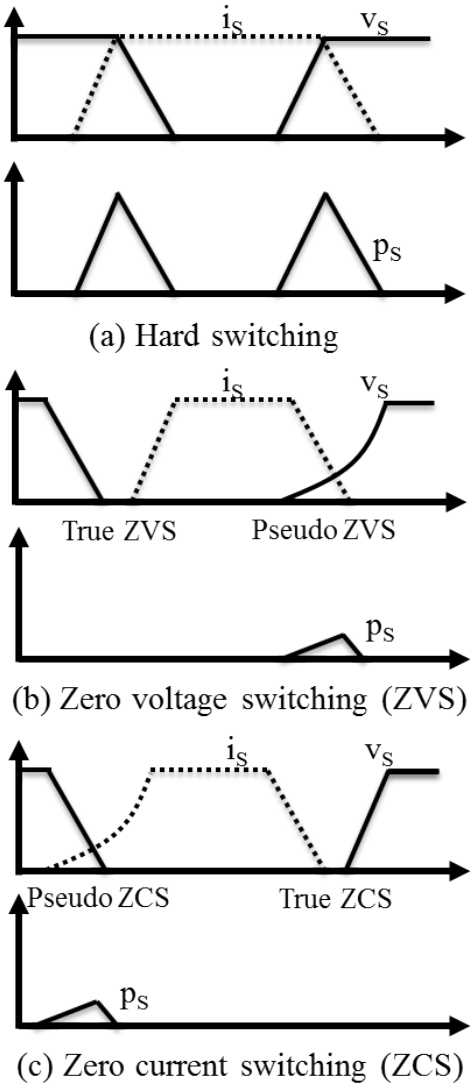


Figure 1.2: Main soft switching techniques [7].

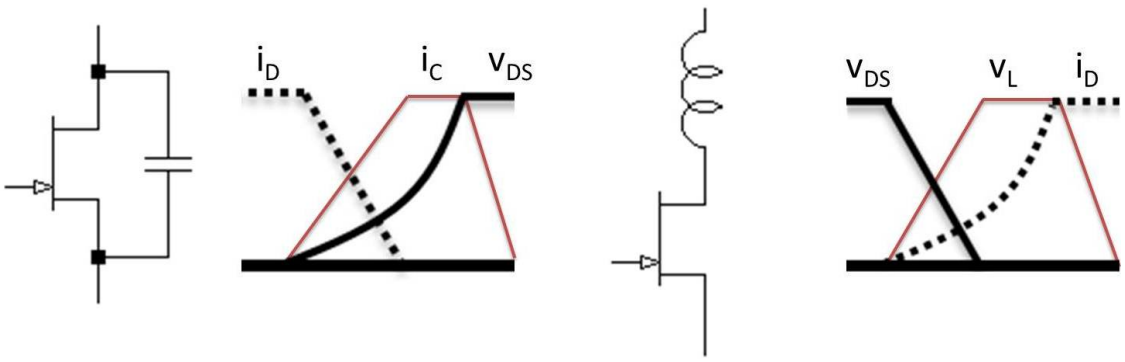


Figure 1.3: Examples of a turn off snubber (left) and a turn on snubber (right).

ever, the size required by the components is often prohibitive. Additionally, larger capacitance or inductance values will increase total switching time, which may affect control systems, will further limit maximum switching frequency, and may distort the output power waveform.

The use of nonlinear passives in the snubbers presented above offer size and power loss reductions over their linear counterparts [14, 15, 16, 17, 18, 19]. For the turn off snubber, high capacitance is only needed for the amount of time it takes to turn off the switch. When the current through the switch reaches zero, the capacitance can be allowed to decrease. In the turn on snubber, high inductance is only needed for the amount of time it takes the drain voltage of the switch to reach zero. In both of these cases, a drop in capacitance or inductance will decrease total switching time, thus reducing or eliminating the control system and switching frequency limitations discussed above. The size of these components is greatly reduced because they only store energy within a small operating area. Outside of this area energy storage is minimized. Since the total energy stored within the passives is reduced, the complementary switching transient (e.g., the turn on transient of a turn off snubber) power loss will also be reduced.

Saturable inductors impose an additional requirement on the power topology because their flux must be reset before each switching transient. Say for instance the inductor starts at zero flux density and zero magnetization. When voltage is applied to its terminals, the inductor current (and thus magnetization) increases slowly because it is passing through its linear, high-inductance region. If this voltage is applied long enough, its flux density will saturate and its current will

greatly increase due to a sudden decrease in its inductance. When the magnetization is removed (i.e., current reduced to zero) the flux density will relax back to its remnance point, which is sometimes (depending on the material) near its saturation point. If the core remains at its remnance point until the next transition, the inductor will almost instantly saturate. This would eliminate the pseudo ZCS effect desirable in turn on snubbers.

Soft-switched cells are an attractive means of reducing switching loss in power converters since the energy recovery method only needs to be developed once and the cell can then be reused on many types of power topologies. Some cell topologies can even absorb energy from the power topology's circuit elements (such as the winding capacitance of a power transformer). In these cases, the cell may require slight tuning for each topology to achieve optimal energy recovery.

Quasi-resonant switch cells offer simple circuit topologies and control; however, they exhibit high nonlinearity, their characteristics vary widely with changing loads, and they cannot be used with pulse width modulation (PWM) [8, 20]. Snubbers can also decrease switching loss by reducing the amount of overlap between the power switch voltage and current [2, 3, 18, 17, 16, 15, 21, 22, 13, 23]. Snubbers are less efficient than quasi resonant cells because they only achieve pseudo soft switching [7]. Many cell topologies, such as [11, 12], allow inductive energy to circulate within the cell which dissipates the stored energy in the semiconductor devices over time. Most of the aforementioned topologies could not be implemented with saturable inductors because they are not able to reverse the inductor's flux before the next transition. The topology presented in this thesis aims to mitigate some of these issues.

Chapter 2 of this thesis details analysis of the switch cell's power topology. Chapter 3 presents the semiconductor selection criteria and packaging approach. Chapter 4 steps through the design process and testing results of the saturable resonant inductor. Chapter 5 details the gate driver design and testing. Testing results of the switch cell as a whole are presented in Chapter 6, and the thesis concludes with Chapter 7.

CHAPTER 2
NONLINEAR RESONANT SWITCH CELL TOPOLOGY

The switch cell topology was developed with several goals in mind. First, the cell should be able to operate under PWM control so the switch cell can be applied to many existing power topologies and controllers. PWM-capable switch positions are also capable of many other control methods that may be required by specific power topologies, including frequency, constant on-time, and constant off-time control. The switch cell should not impose additional restrictions on the controller, such as generating additional control signals for auxiliary switches.

Second, the switch cell should allow each switch to operate under true or pseudo soft switching at both turn on and turn off. Hard switching of just one device could increase the overall switch cell losses over the losses of a single, standard switch position.

Third, if a resonant inductor is used, the switch cell should transfer the inductive energy into a capacitor or auxiliary sink as quickly as possible for more efficient energy storage. Current circulating throughout the inductor will add resistive losses from the inductor's winding resistance, switch on-resistances, and diode forward voltage drops. Additionally, if capacitive energy is transferred into the inductor during transients, this energy will be dissipated quickly (100's ns) in the aforementioned resistances; thus, if this capacitive energy is to be recovered it must be removed from the inductor as quickly as possible.

Fourth, applications of nonlinear passives are to be investigated in order to reduce the overall size, power loss, and duty cycle limitations of the switch cell (see Chapter 1). This thesis focuses on the design of saturable inductors for use in the switch cell; thus, the cell must be capable of resetting the inductor's flux. Nonlinear capacitors can also increase performance of the switch cell; however, this subject is not covered in detail within this thesis.

Figure 2.1 shows the schematic diagram of the nonlinear switch cell. The cell can replace main switch positions in many topologies of switching power converters with little modification to the power topology or controller. The "Energy Recovery" block in this diagram represents some energy sink within the power system. The cell redirects a portion of the switching energy into

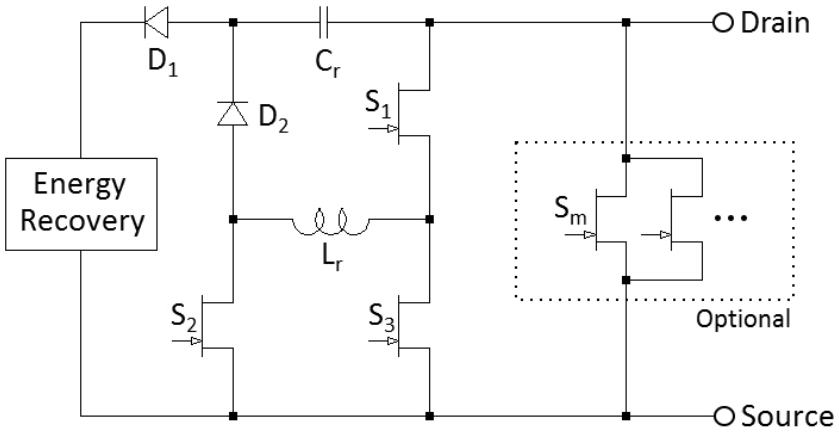


Figure 2.1: Schematic of the nonlinear resonant switch cell.

this sink during both turn on and turn off. This could include the input power bus, the converter's output, or an auxiliary power supply for the power system's controller and/or gate drivers.

The key feature of this switch cell topology is the use of a nonlinear (saturable) resonant inductor, L_r. In its linear region, L_r will have a very high inductance which can virtually eliminate current rise in power switches during turn on. When L_r saturates, its inductance becomes very low, causing the current through it to increase rapidly. If the saturation time is timed well with the transition time of the power switch, the switch will transition under a very effective pseudo ZCS switching event. This allows significant reduction in the inductor's volume, weight, and power loss. Another benefit is that the saturable inductor will fully transition much faster than a linear inductor, allowing higher switching frequencies. The main requirement for using a saturable inductor in a switch cell is insurance of flux resetting. When the inductor saturates in one direction, its flux density will remain near saturation (remnance point) even under zero magnetization. Thus, at the next switching event the inductor will not be able to pass through its linear region because it is already virtually saturated. Most of the switch cell topologies surveyed could not reverse the flux in the inductor, and none were able to accomplish flux reversal efficiently. Portions of the topology presented here are designed specifically for efficient flux reversal of L_r.

The S_m power switch is optional if lower on-resistance is desired. Removal of S_m may be

desirable to reduce complexity of the cell's gate driver circuity. If S_m is removed, all of the drain current flows through S_1 and S_3 in the on-state. It is desirable to have S_1 and S_3 be fast devices to reduce the size of L_r. However, this has the effect of increasing on-resistance and, thus, power dissipation of these components during conduction. S_m can be a much larger device with low on-resistance. Its larger drain-source capacitance will present more stored energy; however, some of that energy can be absorbed by the cell and redirected to the energy recovery circuit. Since this redirection is imperfect, switching losses will continue to increase with increasing size of S_m and the optimal sizing of S_m will eventually reach a maximum.

The nine operational modes of the switch cell are displayed in Figure 2.2 and the corresponding key waveforms are shown in Figure 2.3. The mode diagrams are analyzed in a clamped-inductive circuit, which is a standard means of measuring switching loss in power devices. The clamped inductance is assumed to be large enough that the load current, I_o, does not change significantly during the switching period. Power switch capacitances are shown in the mode diagrams to clarify transient current paths. The waveforms assume that the energy recovery voltage is half of the bus voltage, V_o. The modes are explained as follows:

Mode 1 (t_0 - t_1): This Mode is the switch cell's off-state. S_1 and S_m are off and the load current is flowing through the freewheeling diode of the clamped-inductive test setup. S_2 and S_3 are on to prevent any ringing at the drain from affecting L_r.

Mode 2 (t_1 - t_2): This Mode initiates the switch cell's turn on process. S_3 is turned off to insert dead time between the transition of S_3 and S_1 in the next Mode.

Mode 3 (t_2 - t_3): S_1 turns on with pseudo ZCS since L_r is at 0 A and cannot change instantaneously. With sufficiently large inductance L_r, the contribution of switching loss due to load current is insignificant. Energy required to transition the capacitances of S_1 and S_3 are the main source of loss in this Mode. When S_1 fully turns on, V_o is applied across L_r. This increases its flux density until it reaches saturation at $t_2 + t_{sat}$. After saturation, L_r reduces to a very small inductance, allowing a rapid increase in current through S_1, L_r, and S_2. The time $t_3 - t_2$ is defined by the time required to saturate L_r and increase its current to I_o.

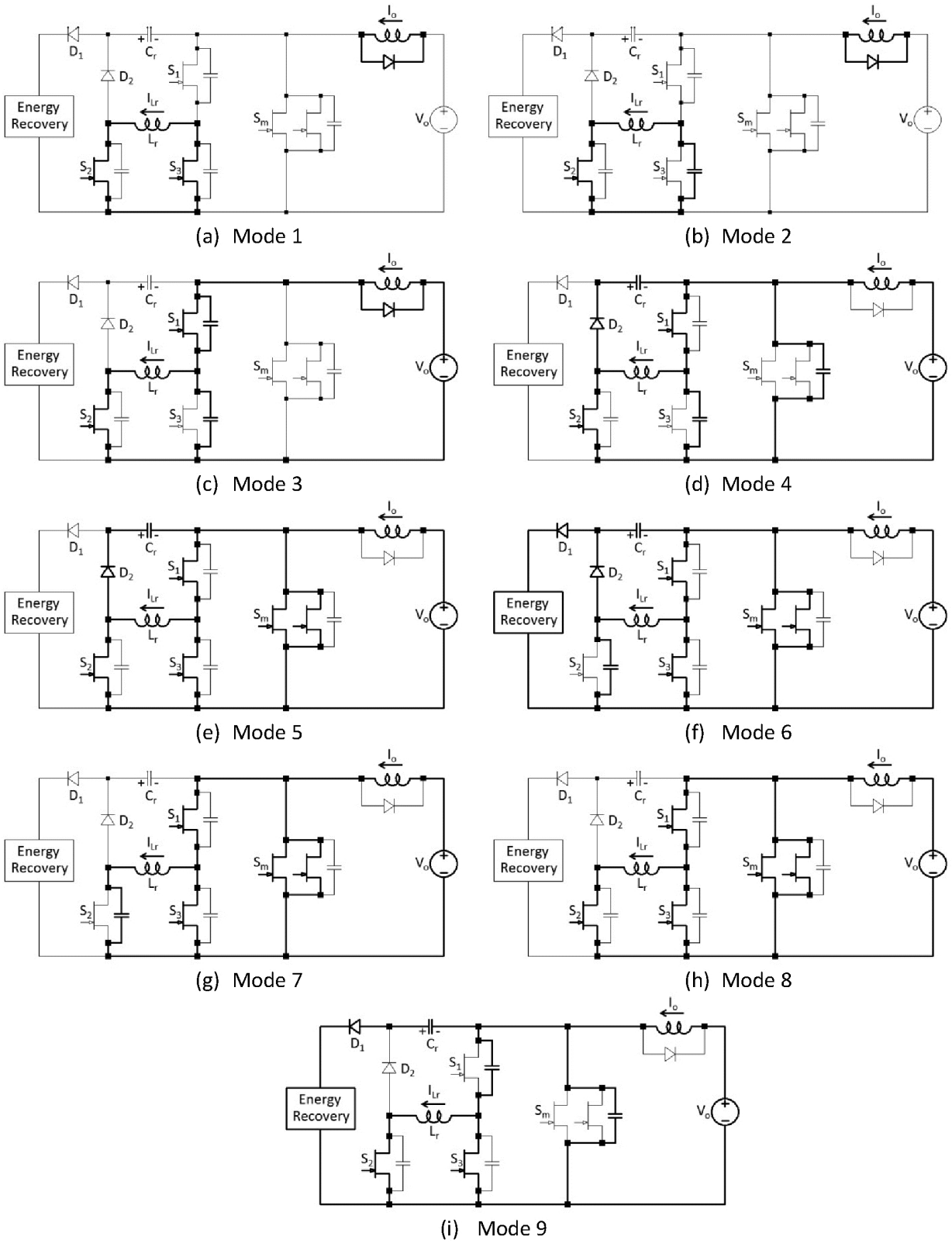


Figure 2.2: Equivalent operational modes of the nonlinear resonant switch cell.

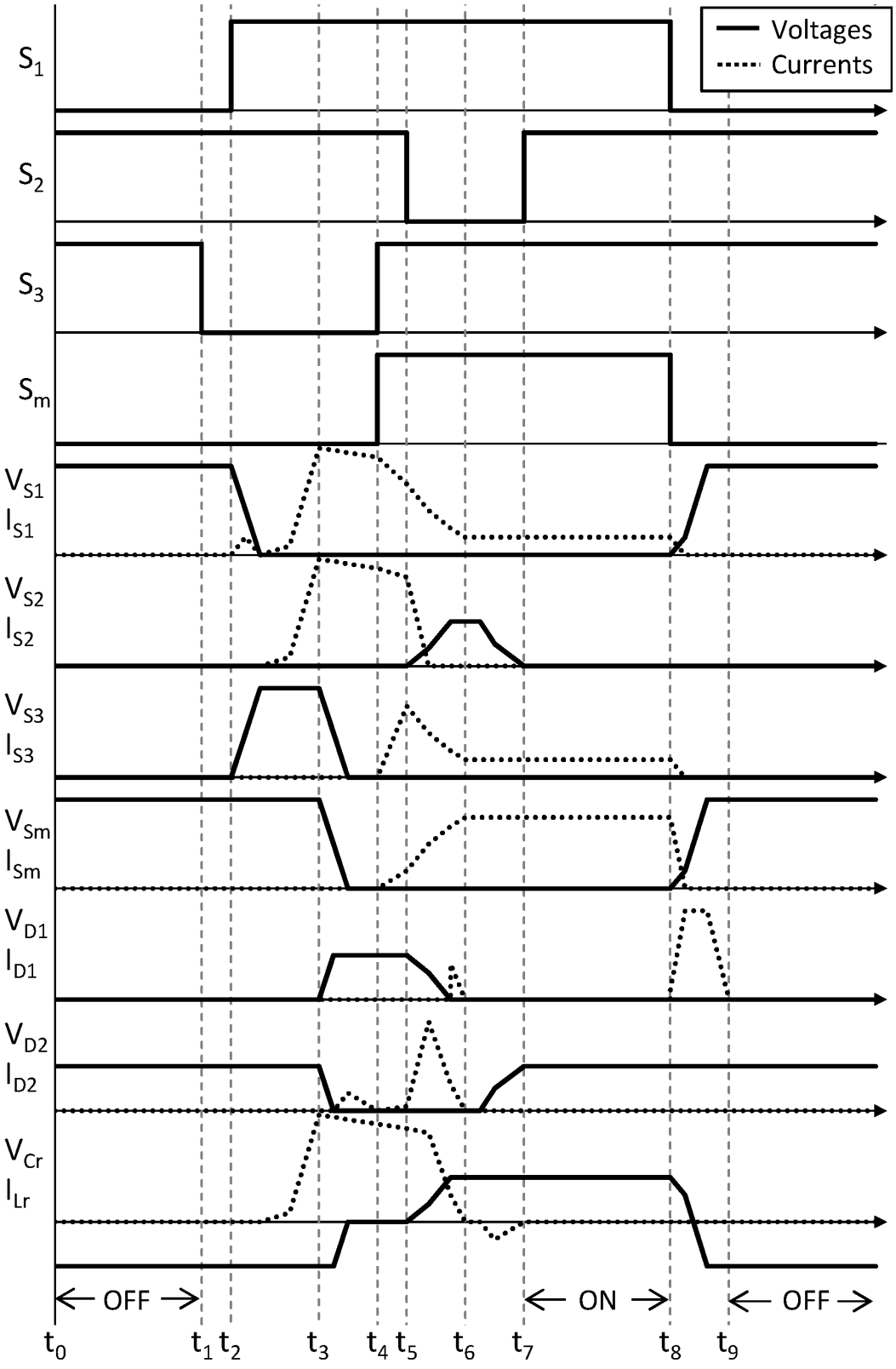


Figure 2.3: Timing diagram of the nonlinear resonant switch cell.

Mode 4 (t_3 - t_4): When I_{Lr} reaches I_o the freewheeling diode becomes reversed biased and the drain voltage begins to fall. Energy stored in the capacitances of S_m and S_2 are transferred into L_r. When the drain voltage equals $-V_{Cr}$, D_2 conducts and clamps the positive side of C_r to ground. Energy stored in C_r is transferred into L_r. The transferred capacitive energy manifests itself as increased current over I_o in L_r. The time t_4 - t_3 is defined by the time required to reach the steady state on the drain voltage.

Mode 5 (t_4 - t_5): The drain voltage fully transitions low. S_m and S_3 are turned on with true ZVS. S_m will most likely be physically located far away from the rest of the cell since it is a larger device. The resulting parasitic inductance will cause the current to rise slowly in S_m and may span several Modes. Thus, S_3 "catches" S_1 in this Mode, preventing the drain from transitioning high in the next Mode where the main current path would otherwise be redirected away from ground. The time t_5 - t_4 is defined by the time required to fully turn on S_3.

Mode 6 (t_5 - t_6): S_2 turns off under pseudo ZVS. I_{Lr} charges the capacitance of S_2 and C_r through D_2. I_{Lr} decreases as the energy stored in L_r is transferred into C_r and S_2. If the energy in L_r is enough to make V_{Cr} increase to the energy recovery voltage, D_1 will forward bias and any remaining energy will be delivered to the energy recovery circuitry. The time t_6 - t_5 is defined by the time required to fully deplete I_{Lr} to zero.

Mode 7 (t_6 - t_7): This Mode completes the switch cell's turn on process. The voltage on S_2 is retained by S_2's capacitance. This voltage is applied across L_r, which reverses its magnetization until it saturates in the opposite direction. This causes the voltage on S_2 to fall to ground. The energy transferred from S_2's capacitance is dissipated as conduction loss in L_r, S_2, and S_3 in the next Mode. The time t_7 - t_6 is defined by the time required to fully transition the voltage on S_2 to zero.

Mode 8 (t_7 - t_8): This Mode is the switch cell's on-state. S_2 is turned on with true ZVS. S_2 prevents a possible oscillation with L_r and S_2's capacitance, and preserves the polarity of flux density in L_r. The latter is especially important since a flux reversal at this point would cause L_r to instantly saturate at the next turn on, thus eliminating the pseudo ZCS of S_1.

Mode 9 (t_8 - t_9): This Mode is the switch cell's turn off state. S_1 and S_m are turned off with pseudo ZVS. If D_1 is already forward biased, the drain current instantly transfers to C_r, delivering current to the energy recovery circuitry and discharging C_r. S_3 must remain on during this transient to prevent the capacitance of S_1 from pulling up the voltage across L_r, which could cause flux reversal. The time t_9 - t_8 is defined by the time required to fully transition the drain voltage to V_o.

CHAPTER 3

SEMICONDUCTOR SELECTION

Many semiconductor materials and structures are available for use in the switch cell's auxiliary and main switches. To understand how different technologies affect the overall performance of the switch cell, one can determine the switching loss of a particular device in terms of switch cell overall specifications and physical properties of individual components. The switch of most interest is S_1 (see Chapter 2), which operates under pseudo ZCS at the beginning of the switch cell's turn on transient. To determine the amount of loss, one must calculate the instantaneous power loss of the switch and integrate it over the switching transient time period to determine the switching energy. The energy can then be multiplied by the switching frequency to determine the average switching loss:

$$P_{sw,on} = fE_{on} = f\int_0^{t_{f,sw}} V_{DS}(t)I_D(t)dt \tag{3.1}$$

where $V_{DS}(t)$ is the switch drain-to-source voltage and $I_D(t)$ is the instantaneous drain current. Assuming a linear voltage transition and neglecting the on-state voltage drop, the drain-to-source voltage is calculated as:

$$V_{DS}(t) = \begin{cases} V_{DS,max} - \frac{V_{DS,max}}{t_{f,sw}}t & t \le t_{f,sw} \\ 0 & t > t_{f,sw} \end{cases} \tag{3.2}$$

where $V_{DS,max}$ is the peak steady-state voltage across the switch and $t_{f,sw}$ is the voltage fall time of the switch. The current rise of this switch is dependent on the charge rate of the saturable resonant inductor, L_r. Assuming the switch will completely turn on before L_r saturates, the inductance can be estimated as an "initial effective" inductance, L_{ie}, defined by the core geometry and material properties as:

$$L_{ie} = \mu_{ie}N^2\frac{A_e}{l_e} \tag{3.3}$$

where μ_{ie} is the effective permeability before saturation, N is the number of turns, A_e is the effective cross sectional area of the core, and l_e is the effective length of the core. Assuming zero initial current, the drain current can be calculated as:

$$I_D(t) = \frac{1}{L_{ie}} \int_0^t V_L(\theta) d\theta = \frac{1}{L_{ie}} \int_0^t \left(V_{DS,max} - V_{DS}(\theta) \right) d\theta \tag{3.4}$$

$$= \begin{cases} \frac{1}{L_{ie}} \int_0^t \frac{V_{DS,max}}{t_{f,sw}} \theta d\theta & t \leq t_{f,sw} \\ \frac{1}{L_{ie}} \int_{t_{f,sw}}^t V_{DS,max} d\theta + I_D(t_{f,sw}) & t_{f,sw} < t < t_{sat} \end{cases} \tag{3.5}$$

$$= \begin{cases} \frac{1}{2L_{ie}} \frac{V_{DS,max}}{t_{f,sw}} t^2 & t \leq t_{f,sw} \\ \frac{1}{L_{ie}} V_{DS,max} \left(t - t_{f,sw} \right) + \frac{1}{2L_{ie}} V_{DS,max} t_{f,sw} & t_{f,sw} < t < t_{sat} \end{cases} \tag{3.6}$$

where t_{sat} is the saturation time of the inductor at $V_{DS,max}$. Combining (3.1), (3.2), and (3.6):

$$P_{sw,on} = \frac{f}{2L_{ie}} \int_0^{t_{f,sw}} \left(V_{DS,max} - \frac{V_{DS,max}}{t_{f,sw}} t \right) \frac{V_{DS,max}}{t_{f,sw}} t^2 dt \tag{3.7}$$

$$= \frac{f V_{DS,max}^2}{2L_{ie} t_{f,sw}^2} \int_0^{t_{f,sw}} \left(t_{f,sw} t^2 - t^3 \right) dt \tag{3.8}$$

$$= \frac{f V_{DS,max}^2}{2L_{ie} t_{f,sw}^2} \left(\frac{1}{3} t_{f,sw}^4 - \frac{1}{4} t_{f,sw}^4 \right) \tag{3.9}$$

$$= \frac{f V_{DS,max}^2 t_{f,sw}^2}{24 L_{ie}} \tag{3.10}$$

Note that terms for $t > t_{f,sw}$ are removed since $V_{DS} = 0$ in this region. Substituting (3.3) into (3.10), $P_{sw,on}$ can be expressed as a function of material properties, switch cell specifications, and inductor geometry (to be analyzed in Chapter 4):

$$P_{sw,on} = \frac{f V_{DS,max}^2 t_{f,sw}^2 l_e}{24 \mu_{ie} N^2 A_e} \tag{3.11}$$

These equations show that, as expected, the switching loss decreases as L_{ie} increases. Con-

versely, the required inductance of the saturable inductor can be reduced by choosing a switch with high switching speed. This not only reduces the physical size of the inductor but decreases its loss as well. Therefore, a main criteria for selecting the semiconductor devices is their switching speed. The targeted converter under the funding program was limited to silicon carbide (SiC) enhancement-mode junction field effect transistors (JFETs) due to their high tolerance to radiation effects. Fortunately these devices are very fast and would be a likely candidate for the switch cell's semiconductors even without the restriction.

SemiSouth 1200 V, 50 mΩ, SiC JFETs were selected because of their low on-resistance and high voltage capability. The JFETs require a steady-state current at the gate to achieve low on-resistance from drain to source and a negative turn off voltage to increase noise immunity during transients. From a gate driver perspective, the gate of the JFET can be modeled as a diode junction. The specific JFETs used for this project had an unfavorable ratio of gate-to-drain capacitance and gate-to-source capacitance. Transients at the drain of the JFET are coupled into the gate which can cause ringing and undesirable turn on of the device. Therefore, 4.7 nF capacitors were added between gate and source of each JFET to alter the capacitance ratio and increase controllability. Additionally, Zener diodes between gate and source are also desirable to clamp any over voltage that may occur due to the parasitic inductance between the gate driver and JFET.

Figure 3.1 shows the packaged auxiliary switches, S_1 - S_3 and Figure 3.2 shows the main switch, S_m, which consists of twelve power devices of the same size as the auxiliary devices. The switches are packaged on direct bond copper (DBC) substrates in a metal package and passivated with a high voltage gel. The gate-to-source capacitors and Zener diodes are located very close to their respective JFETs to limit parasitic inductance. C_r is also included in the package to reduce parasitic inductance between C_r and the auxiliary switches.

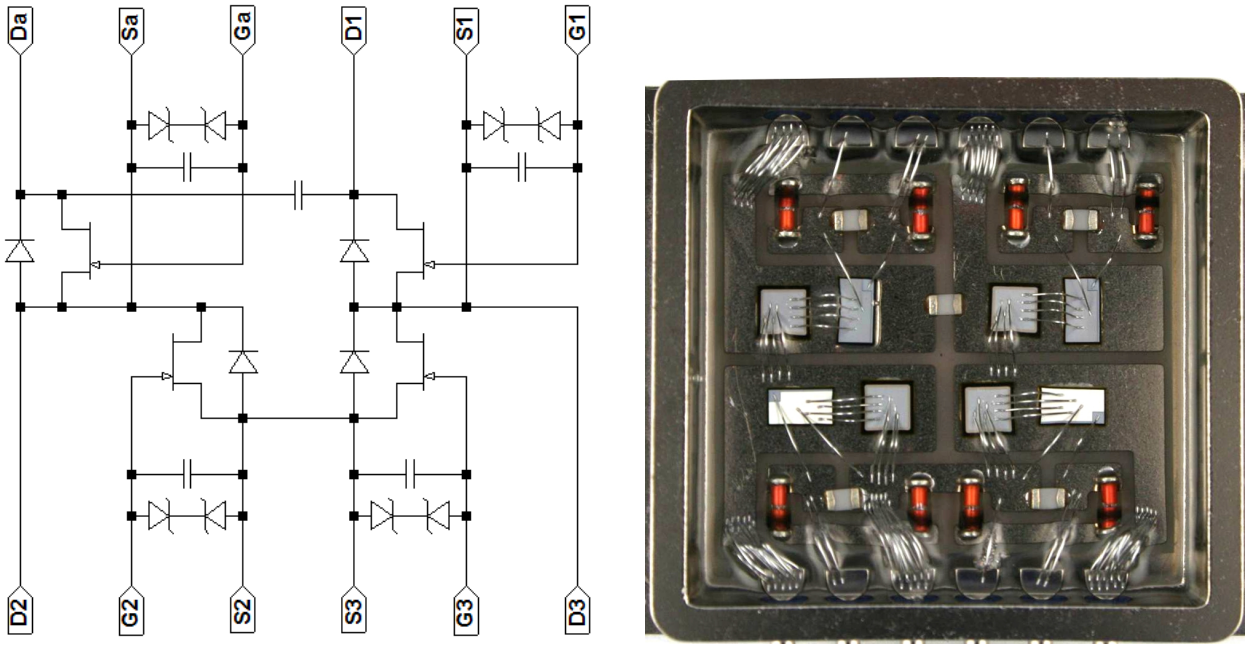


Figure 3.1: Schematic (left) and packaged semiconductors (right) of the auxiliary switches.

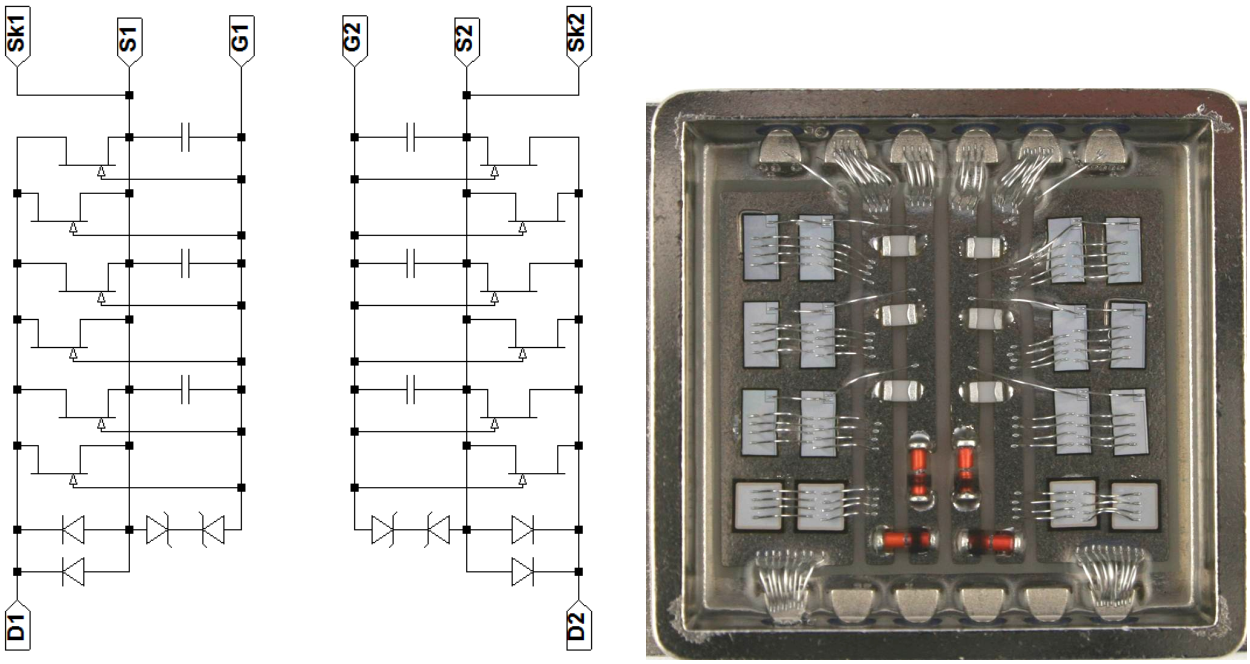


Figure 3.2: Schematic (left) and packaged semiconductors (right) of the main switch.

CHAPTER 4

SATURABLE INDUCTOR DESIGN

The first step in the inductor design process is to determine a figure of merit (FOM) function that takes into acount the main contributors of power loss within the cell affected by the inductor. The main categories identified in this research are the switch turn-on loss (derived in Chapter 3), the inductor's core loss, and its winding loss. Thus, the FOM can be expressed as:

$$FOM_L = P_{sw,on} + P_{core} + P_{wdg} \tag{4.1}$$

The FOM should be formulated in terms of the switch cell's specifications, core material properties, and core geometry. The switch cell specifications are defined by the application. The analysis presented below can be applied to one core material at a time, allowing the material properties to also be considered constants. The materials can then be compared against each other once the analysis is complete. The core geometry, number of turns, and winding wire gauge are left as variables. These could be solved numerically through nonlinear optimization algorithms and/or analytically. The method chosen in this thesis is a combination of the two, with equations derived for the core geometry and wire gauge and the number of turns solved numerically.

The inductor's core loss can be expressed as a specific core loss, $P_{core,sp}$, multiplied by its effective volume, V_e. The effective volume can be broken down into the more common effective cross sectional area, A_e, and effective length, l_e:

$$P_{core} = P_{core,sp} V_e = P_{core,sp} A_e l_e \tag{4.2}$$

A_e can be expressed in terms of the switch cell's rated voltage, $V_{DS,max}$, the desired time to saturation at $V_{DS,max}$, t_{sat}, the core's saturation flux density, B_{sat}, and the number of turns, N:

$$A_e = \frac{V_{DS,max} t_{sat}}{2 B_{sat} N} \tag{4.3}$$

Since the saturation time contributes to the size and power loss of the inductor, t_{sat} should be

minimized. It must, however, be larger than the voltage transition time of the switch to be snubbed to attain the full benefit of pseudo ZCS. Thus, setting $t_{sat} = t_{f,sw}$ should be the most optimal operating point.

4.1 Specific Core Loss Estimations

The improved generalized Steinmetz equation (iGSE) has been shown to accurately predict specific core loss for arbitrary flux waveforms using Steinmetz parameters commonly provided by core manufacturers [24, 25, 26, 27]. The iGSE is expressed as:

$$P_{core,sp} = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} \Delta B^{\beta-\alpha} dt \tag{4.4}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{4.5}$$

where k, α, and β are the Steinmetz parameters. From Faraday's law, the definition of flux density, and obtaining the voltage across the inductor $V_L = V_{DS,max} - V_{DS}(t)$, the rate of change in flux density can be expressed as:

$$\frac{dB_{on}}{dt} = \frac{1}{A_e}\frac{d\Phi}{dt} = \frac{V_L(t)}{NA_e} \quad = \quad \begin{cases} \frac{1}{NA_e}\frac{V_{DS,max}}{t_{f,sw}} t & t \le t_{f,sw} \\ \frac{1}{NA_e} V_{DS,max} & t_{f,sw} < t < t_{sat,on} \\ 0 & t > t_{sat,on} \end{cases} \tag{4.6}$$

The inductor will fully transition from negative saturation to positive saturation during a switching cycle; thus, $\Delta B = 2B_{sat}$. Assuming dB/dt during the flux reset period is equal to dB_{on}/dt, the specific core loss becomes:

$$P_{core,sp} = 2 f k_i (2B_{sat})^{\beta-\alpha} \int_0^{t_{sat,on}} \left|\frac{dB_{on}}{dt}\right|^{\alpha} dt \tag{4.7}$$

The integral term in the equation above can be solved independently:

$$\int_0^{t_{sat,on}} \left|\frac{dB_{on}}{dt}\right|^{\alpha} dt = \int_0^{t_{f,sw}} \left|\frac{V_{DS,max}}{NA_e t_{f,sw}} t\right|^{\alpha} dt + \int_{t_{f,sw}}^{t_{sat,on}} \left|\frac{V_{DS,max}}{NA_e}\right|^{\alpha} dt \tag{4.8}$$

$$= \left(\frac{V_{DS,max}}{NA_e}\right)^{\alpha} \left(\frac{1}{t_{f,sw}^{\alpha}} \int_0^{t_{f,sw}} t^{\alpha} dt + \int_{t_{f,sw}}^{t_{sat,on}} dt\right) \tag{4.9}$$

$$= \left(\frac{V_{DS,max}}{NA_e}\right)^{\alpha} \left(\frac{1}{t_{f,sw}^{\alpha}} \frac{t_{f,sw}^{\alpha+1}}{(\alpha+1)} + t_{sat,on} - t_{f,sw}\right) \tag{4.10}$$

$$= \left(\frac{V_{DS,max}}{NA_e}\right)^{\alpha} \left(\frac{t_{f,sw}}{(\alpha+1)} + t_{sat,on} - t_{f,sw}\right) \tag{4.11}$$

Now the specific core loss can be expressed in terms of the core material properties, the switch cell specifications, and characteristics of the power switch:

$$P_{core,sp} = 2fk_i (2B_{sat})^{\beta-\alpha} \left(\frac{V_{DS,max}}{NA_e}\right)^{\alpha} \left(\frac{t_{f,sw}}{(\alpha+1)} + t_{sat,on} - t_{f,sw}\right) \tag{4.12}$$

4.2 Core Geometry

Magnetic cores are offered in many shapes, including E, C, I, and toroid to name a few. This research focused on analyzing toroidal cores since many types of core materials are available in toroid shapes and custom machined toroids are fairly straightforward. Toroid geometry is commonly defined by its inner radius, r_1, outer radius, r_2, and height, h. The mathematics presented below can be simplified if the core width, w = r_2 - r_1, is used as an independent variable instead of r_2. Figure 4.1 illustrates these definitions.

The IEC standard for calculating l_e is:

$$l_{e,IEC} = \frac{2\pi ln\left(\frac{r_2}{r_1}\right)}{\frac{1}{r_1} - \frac{1}{r_2}} \tag{4.13}$$

However, differentiation of this function is also problematic. The geometric mean path of the core provides a reasonable approximation to the IEC calculation while significantly simplifying equations to follow:

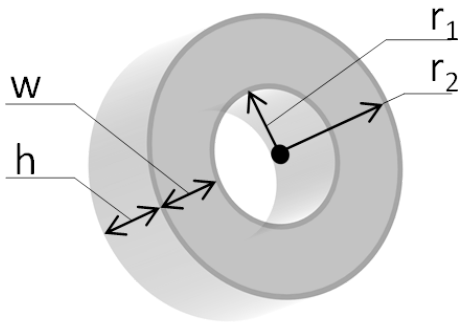


Figure 4.1: Definitions of core geometry parameters.

$$l_{e,mean} = \pi (r_1 + r_2) = \pi (2r_1 + w) \tag{4.14}$$

Core geometry is completely defined by l_e and A_e, which was defined at the beginning of the chapter. This completes calculation of the inductor's core loss. The last term in the FOM is the winding loss, which can be approximated as dc resistive loss in terms of core geometry, cell specifications, and the resistivity of the winding conductor, ρ:

$$P_{wdg} = I_{L,rms}^2 R_{dc} = I_{L,rms}^2 \frac{2\rho N^2 (h+w)}{\pi r_1^2} = I_{L,rms}^2 \frac{2\rho N^2 \left(\frac{A_e}{w} + w\right)}{\pi r_1^2} \tag{4.15}$$

$I_{L,rms}$ will be much smaller than the switch cell's rated current since the inductor conducts for very short amounts of time. The terms above can be integrated into the FOM equation as a function of r_1 and w:

$$
\begin{aligned}
FOM_L &= P_{sw,on} + P_{core} + P_{wdg} && (4.16)\\
&= \frac{fV_{DS,max}^2 t_{f,sw}^2 l_e}{24\mu_{ie}N^2 A_e} + P_{core,sp}A_e l_e + I_{L,rms}^2 \frac{2\rho N^2\left(\frac{A_e}{w}+w\right)}{\pi r_1^2} && (4.17)\\
&= K_{Lt1}l_e + K_{Lt2}l_e + K_{Lt3}\frac{\frac{A_e}{w}+w}{r_1^2} && (4.18)\\
&= \pi\left(K_{Lt1}+K_{Lt2}\right)\left(2r_1+w\right) + K_{Lt3}\frac{\frac{A_e}{w}+w}{r_1^2} && (4.19)
\end{aligned}
$$

where

$$
\begin{aligned}
K_{Lt1} &= \frac{fV_{DS,max}^2 t_{f,sw}^2}{24\mu_{ie}N^2 A_e} && (4.20)\\
K_{Lt2} &= P_{core,sp}A_e && (4.21)\\
K_{Lt3} &= I_{L,rms}^2 \frac{2\rho N^2}{\pi} && (4.22)
\end{aligned}
$$

Optimization of the inductor can be accomplished by determining the values of r_1 and w that minimize the FOM function. This can be accomplished by finding the function's inflection points ($\nabla FOM_L = 0$), where local minimums would occur. First, solve the partial of FOM with respect to w:

$$\frac{\partial FOM_L}{\partial w} = \pi\left(K_{Lt1}+K_{Lt2}\right)+K_{Lt3}\left(\frac{1}{r_1^2}-\frac{A_e}{w^2 r_1^2}\right)=0 \tag{4.23}$$

$$\pi\left(K_{Lt1}+K_{Lt2}\right)+K_{Lt3}\frac{1}{r_1^2} = K_{Lt3}\frac{A_e}{w^2 r_1^2} \tag{4.24}$$

$$\pi\left(K_{Lt1}+K_{Lt2}\right)r_1^2 = K_{Lt3}\frac{A_e}{w^2}-K_{Lt3}=K_{Lt3}A_e\left(\frac{1}{w^2}-\frac{1}{A_e}\right) \tag{4.25}$$

$$r_1^2 = \frac{K_{Lt3}A_e\left(\frac{1}{w^2}-\frac{1}{A_e}\right)}{\pi\left(K_{Lt1}+K_{Lt2}\right)} \tag{4.26}$$

$$r_1 = \sqrt{\frac{K_{Lt3}A_e}{\pi\left(K_{Lt1}+K_{Lt2}\right)}}\sqrt{\left(\frac{1}{w^2}-\frac{1}{A_e}\right)} \tag{4.27}$$

This solution of r_1 causes difficulty in the solution of w. To simplify the mathematics, this function can be approximated as:

$$r_1 \approx \sqrt{\frac{K_{Lt3}A_e}{\pi\left(K_{Lt1}+K_{Lt2}\right)}}\left(\frac{1}{w}-\frac{0.7}{A_e}w\right)=K_{Lt4}\left(\frac{1}{w}-\frac{0.7}{A_e}w\right) \tag{4.28}$$

where

$$K_{Lt4}=\sqrt{\frac{K_{Lt3}A_e}{\pi\left(K_{Lt1}+K_{Lt2}\right)}} \tag{4.29}$$

Now solve the partial of FOM with respect to r_1:

$$\frac{\partial FOM_L}{\partial r_1} = 2\pi\left(K_{Lt1}+K_{Lt2}\right)-2K_{Lt3}\left(\frac{w}{r_1^3}+\frac{A_e}{wr_1^3}\right)=0 \tag{4.30}$$

$$\frac{\partial FOM_L}{\partial w}-\frac{1}{2}\frac{\partial FOM_L}{\partial r_1} = K_{Lt3}\left(\frac{1}{r_1^2}-\frac{A_e}{w^2 r_1^2}+\frac{w}{r_1^3}+\frac{A_e}{wr_1^3}\right) \tag{4.31}$$

$$= 1-\frac{A_e}{w^2}+\frac{w}{r_1}+\frac{A_e}{wr_1}=0 \tag{4.32}$$

$$\frac{A_e}{w^2}-1 = \frac{1}{r_1}\left(\frac{A_e}{w}+w\right) \tag{4.33}$$

$$r_1 = \frac{\frac{A_e}{w}+w}{\frac{A_e}{w^2}-1}=w\left(\frac{A_e+w^2}{A_e-w^2}\right) \tag{4.34}$$

Equating the two solutions of r_1:

$$K_{Lt4}\left(\frac{1}{w}-\frac{0.7}{A_e}w\right) = w\left(\frac{A_e+w^2}{A_e-w^2}\right) \tag{4.35}$$

$$K_{Lt4}\left(1-\frac{0.7}{A_e}w^2\right)\left(A_e-w^2\right) = w^2\left(A_e+w^2\right) \tag{4.36}$$

$$K_{Lt4}\left(A_e-0.7w^2-w^2+\frac{0.7}{A_e}w^4\right) = w^2A_e+w^4 \tag{4.37}$$

$$\left(1-0.7\frac{K_{Lt4}}{A_e}\right)w^4+\left(A_e+1.7K_{Lt4}\right)w^2-K_{Lt4}A_e = 0 \tag{4.38}$$

Now the solution of w can be found with the quadratic equation:

$$w=\sqrt{\frac{-b\pm\sqrt{b^2-4ac}}{2a}}=\sqrt{\frac{-\left(A_e+1.7K_{Lt4}\right)\pm\sqrt{\left(A_e+1.7K_{Lt4}\right)^2+4\left(1-0.7\frac{K_{Lt4}}{A_e}\right)K_{Lt4}A_e}}{2\left(1-0.7\frac{K_{Lt4}}{A_e}\right)}} \tag{4.39}$$

Since w is a physical parameter, it must be real, positive, and nonzero. These limitations will usually eliminate all but one of the solutions. If two solutions are found, each value should be evaluated in the FOM equation to determine which one is the global minimum. r_1 can be calculated by one of the equations above and h can be calculated from A_e and w.

The first evaluations of this analysis produced solutions that were not easily manufacturable at the time of this research. Thus, manufacturing restrictions were added to the process. If the optimal r_1 is smaller than the minimum inside radius of the core, $r_{1,min}$, solve the FOM partial with respect to w with $r_1 = r_{1,min}$:

$$r_{1,min}^2 = \frac{K_{Lt3}A_e\left(\frac{1}{w^2}-\frac{1}{A_e}\right)}{\pi\left(K_{Lt1}+K_{Lt2}\right)} \tag{4.40}$$

$$\frac{1}{w^2} = \frac{\pi r_{1,min}^2\left(K_{Lt1}+K_{Lt2}\right)}{K_{Lt3}A_e}+\frac{1}{A_e} \tag{4.41}$$

$$w = \left(\frac{\pi r_{1,min}^2\left(K_{Lt1}+K_{Lt2}\right)}{K_{Lt3}A_e}+\frac{1}{A_e}\right)^{-\frac{1}{2}} \tag{4.42}$$

If this solution for w is smaller than the minimum core width, w_{min}, set w = w_{min}.

4.3 Analysis Results

A set of Octave scripts, included in Appendix A, were developed to calculate these equations for several core materials. Additionally, the number of turns was swept from 1 to 100 and the FOM was calculated for each point. The final output of the scripts is a full design for the inductor, including specific geometry, number of turns, wire gauge, and core material. Figure 4.2 shows the outcome of this analysis in graphical form and Table 4.1 lists relavent material properties of each core in decreasing order of FOM. Ferroxcube 3C90, 3C30, 3F3, and Metglas Finemet achieved similar performance and are all good candidates for the saturable inductor. Metglas Powerlite was in the middle range and could be utilized at lower switching frequencies. Ferroxcube 3C94 and 3F4 performed poorly under the targeted operating conditions. No obvious conclusions could be drawn on a general relationship of a single material parameter's effect on the FOM. Thus, at the present time, the above procedure must be followed to properly design the inductor. The 3F3 material was chosen for this reseach because it was among the best performing materials and was readily availble in the laboratory.

4.4 Fabrication and Testing

Figure 4.3 shows the saturable resonant inductor (left) along with an equivalent linear inductor (right). The current through the saturable inductor is pulsed; therefore, its wire diameter can be

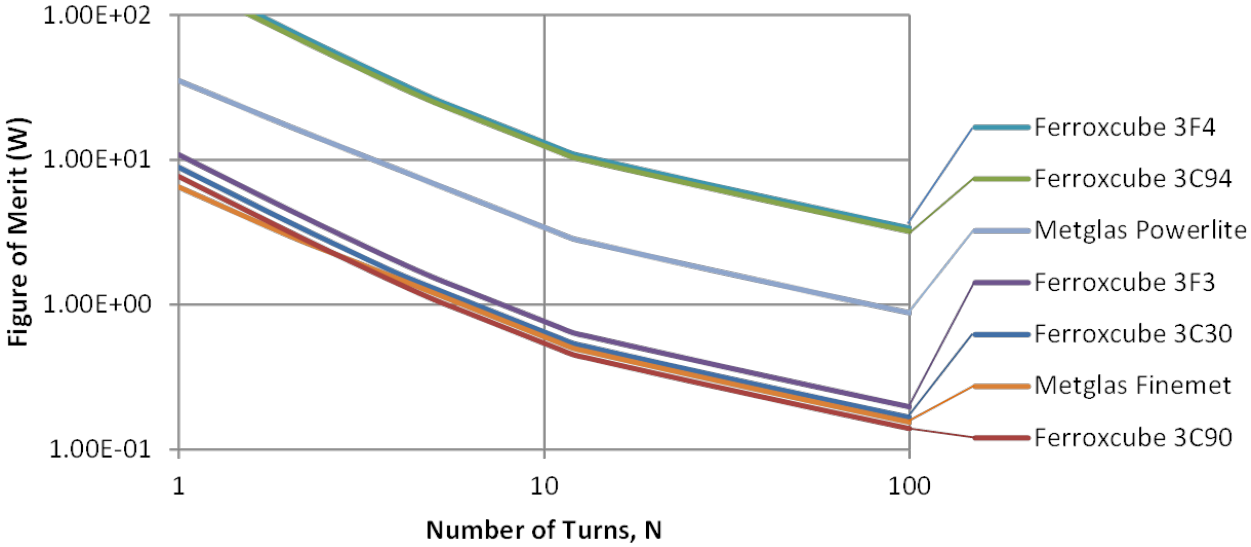


Figure 4.2: Comparison of FOM among several core materials versus the number of turns, N.

Material	Min FOM	B_{sat}	μ_r	α	β	k
Ferroxcube 3F4	3.38	0.38	1700	1.75	2.90	1.20e00
Ferroxcube 3C94	3.20	0.40	5000	2.60	2.75	2.00e-6
Metglas Powerlite	0.88	1.56	5000	1.51	1.74	1.38e00
Ferroxcube 3F3	0.20	0.40	4000	1.80	2.50	2.00e-2
Ferroxcube 3C30	0.17	0.45	5000	1.42	3.02	7.13e00
Metglas Finemet	0.15	1.20	15000	1.53	1.52	2.23e-1
Ferroxcube 3C90	0.14	0.40	5000	1.46	2.75	3.20e00

Table 4.1: Comparison of core material properties in descending order of minimum FOM.

Figure 4.3: Size comparison of a 20 A pulsed, 40 μH saturable inductor (left) and a 20 A continuous, 40 μH linear inductor (right).

Table 4.2: Comparison of saturable and linear inductor characteristics.

Parameter	Saturable	Linear	Improvement Factor
Power Loss	1.05 W	10.8 W	10x
Weight	0.2 g	353 g	1800x
Volume	0.03 in^3	2.3 in^3	77x

greatly reduced. Most of the switch cell topologies implementing linear inductors allow the main current to pass through them continuously, thus requiring a larger wire size. The saturable inductor has 10x lower power loss, 77x smaller volume, and 1800x lighter weight than the linear inductor, as indicated in Table 4.2. Since the reduction in volume is greater than the reduction in power loss, the temperature rise of the saturable inductor is higher. Depending on operating conditions, the saturable inductor may require attachment to the power system's heatsink.

Hysteresis measurements were taken of the core and compared to simulation models for validation, as shown in Figure 4.4. Several hysteresis models were evaluated for this work, including the Jiles Atherton model [28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47,

48, 49, 50], the Carpenter model [48, 49], and the Hodgdon model [51, 52, 53, 54, 55, 49]. While the Jiles Atherton model the most popular model for various magnetic effects, its implementaiton in SPICE causes convergence errors when the inductor is driven by a voltage. This was caused due to derivative calculations that exceeded the computational range of the simulator. The Hodgdon model is somewhat the inverse of the Jiles Atherton model. Most of the terms now require integration, rather than differentiation, which greatly increases the convergence rate. As can be seen in the figure, the model does not accurately predict minor loops, but it does model the main loop very well. Since the inductor in this project only operates along the main loop, the Hodgdon model worked quite well. The SPICE netlist for this model is included in the switch cell netlist in Appendix B.

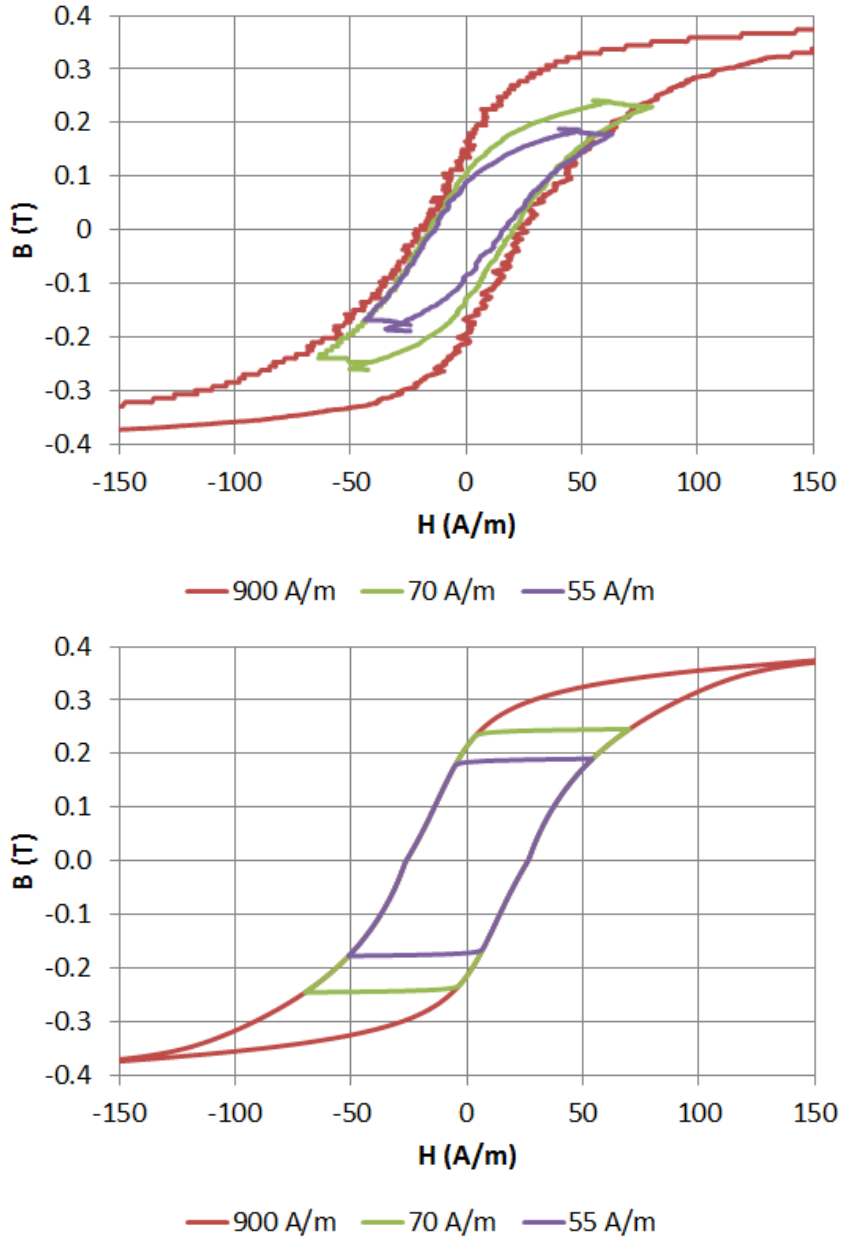


Figure 4.4: BH measurement (top) and Hodgdon hysteresis model (bottom) of the custom 3F3 core with 20 turns.

CHAPTER 5
GATE DRIVER DESIGN

A main goal of the gate driver design was to generate all required timing and sequencing of the various switches within the gate driver, with the only input being the PWM signal generated by the power system's controller. The gate driver includes two volt-second detectors to determine the optimal timing of Modes 3 and 7, and fixed timing circuitry to provide deadtime between S_1 and S_3 in Mode 2 and overlapping of S_2 and S_3 in Mode 5. The output stages of the gate driver increase the voltage and current levels needed to drive the power devices. All output stages are referenced to ground, except the output for S_1 which must be isolated or level shifted.

The schematic for the volt-second detector is shown in Figure 5.1. The sensed voltage, Vsen, is attenuated, filtered, and buffered with U1 and Q1. The output of U1/Q1 produces a current through R3 proportional to Vsen. This current is mirrored through Q2 and Q3 to the VCCS node. A positive transition on the input of the detector causes the output, P, to go high and M1 to turn off. This allows C2 to charge at a rate defined by the current flowing from Q3. Once C2's voltage crosses the input high threshold of X1, the output goes low and M1 discharges C2 to zero. This effectively creates a monostable multivibrator (i.e., one-shot) whose pulse width is controlled by Vsen with an inverse relationship (e.g., increasing Vsen decreases the output pulse width).

The gate driver schematic is shown in Figure 5.2. One of the volt-second detectors monitors the bus voltage to determine the saturation time of L_r during turn on. The other monitors the energy recovery voltage to determine saturation time during flux reset. When the PWM input goes high, the output of the first detector goes high and causes the output of S_3's gate driver, X3, to go low. The PWM signal is delayed by R3 and C3 to insert dead time between the transitions of S_3 and S_1. This delayed PWM signal passes through an isolator since the gate driver X6 must float with the source of S_1. X6 goes high after the programmed delay. The output of the first detector will go low at a time determined by Vbus. This will cause X3 to transition high, turning on S_3. X4, R2, and C2 invert and delay the detector output, which triggers the second detector and causes X9 to go high, turning off S_2. The output of the second detector goes low after a time determined by

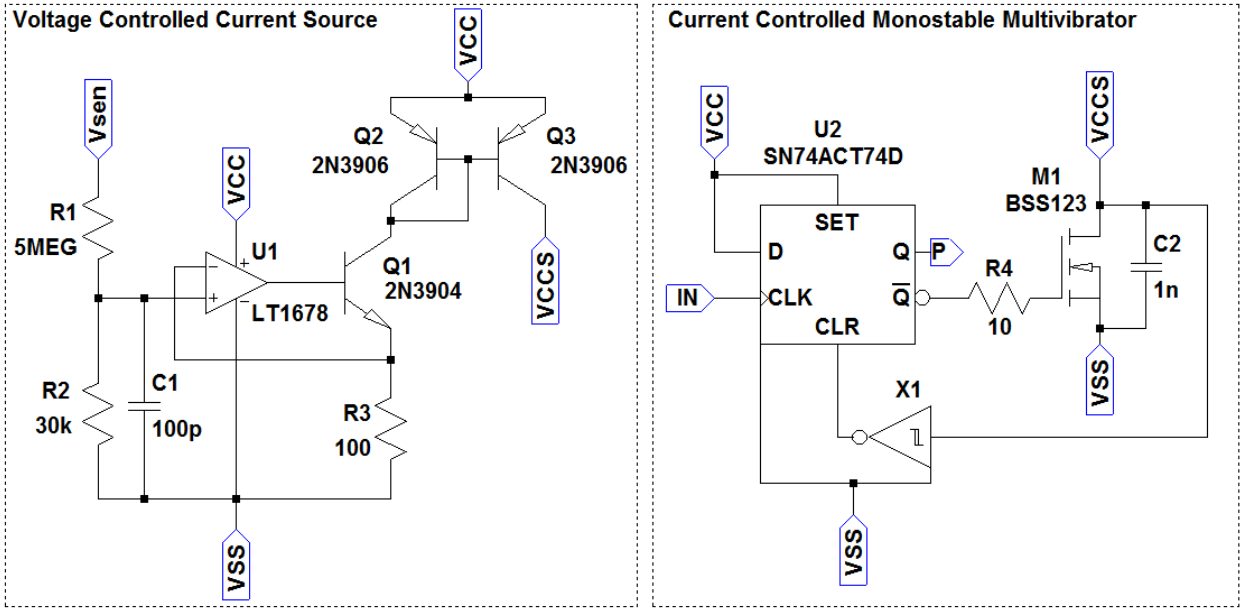


Figure 5.1: Schematic of the volt-second detector block.

Vrec, turning S_2 on again. The gate driver then rests in this state while the PWM is high. When the PWM transitions low, D1 bypasses R3 to turn off S_1 with low propagation delay. Note that control of the optional main switch, S_m, was not implemented in this version of the gate driver to simplify the design. The effect S_m has on the switching loss of the cell is dependent only on its capacitance in the off state, so there is no need to switch S_m for the purposes of this research.

Simulations of the gate driver design are plotted in Figure 5.3. The figure shows how the timing of the gate driver's outputs are affected by increasing (a) the dead time values R_{dt} and C_{dt}, (b) the overlap values R_{ol} and C_{ol}, (c) the bus voltage Vbus, and (d) the recovery voltage Vrec. The dead time in (a) should be adjusted so that S_3 fully turns off before S_1 turns on. The overlap in (b) should be adjusted so that S_2 turns off only after S_3 fully turns on. Both of these times should account for packaging parasitics and add some margin to ensure proper operation of the cell under unforseen operating conditions. Increasing Vbus in (c) will cause the inductor to saturate more quickly; thus, the gate driver's response time is reduced to prevent excess conduction loss while the inductor current circulates throughout the semiconductors. Increasing Vrec in (d) will cause the inductor to reset flux more quickly, so the response time should also be reduced to ensure the

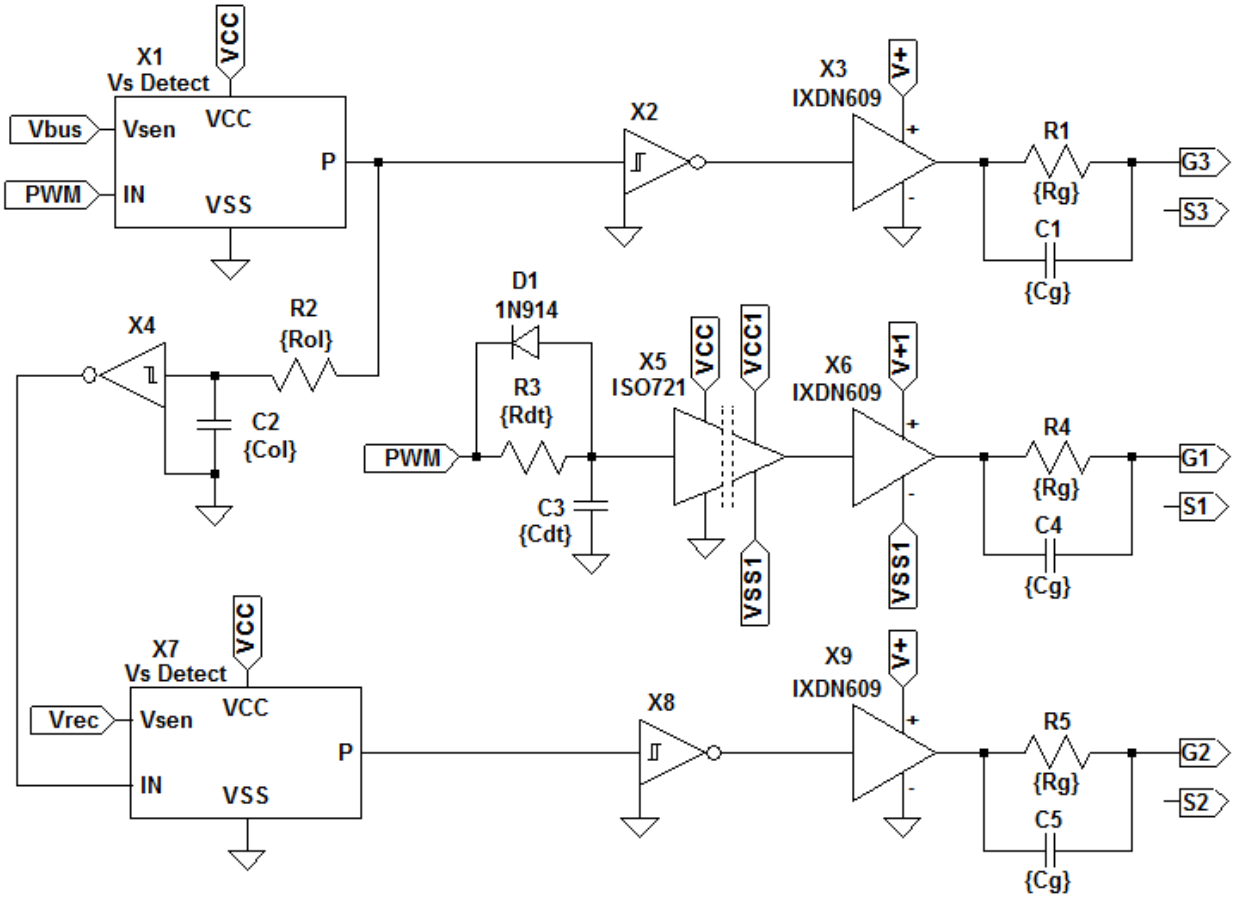


Figure 5.2: Schematic of the switch cell's gate driver.

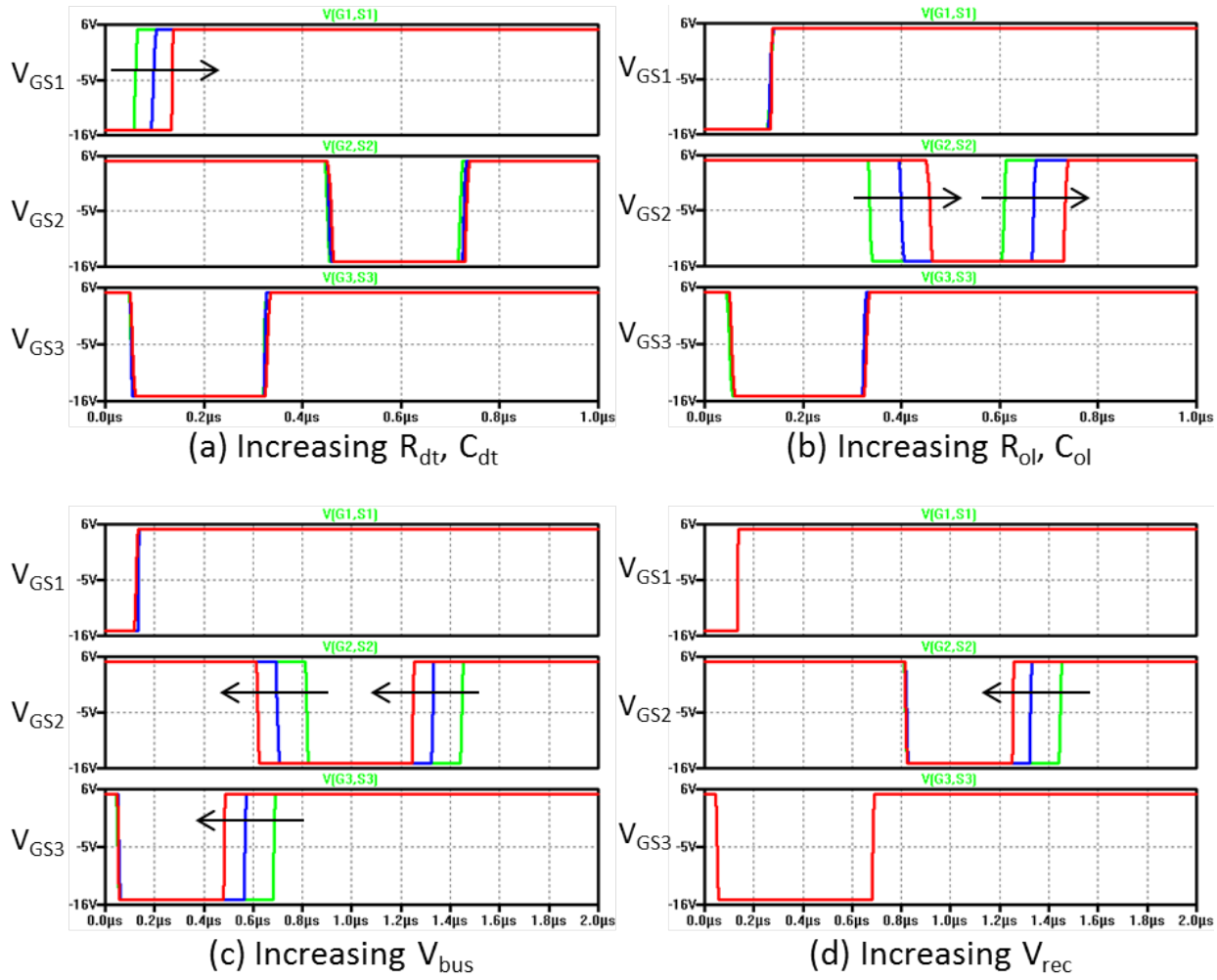


Figure 5.3: Simulation results of the switch cell gate driver, showing the effects of (a) adjusting the deadtime components, (b) adjusting the overlap components, (c) variation in bus voltage, and (d) variation in the recovery circuitry voltage.

flux reset level is locked in.

Figure 5.4 shows the auxiliary and main switches mounted with the cell's gate driver PCB. The gate driver's output stages are located as close as possible to the pins of the power packages to reduce parasitic inductance between the gate drivers and power switches. This will increase controllability and allow faster switching transients. The driver spans two PCBs so it can be connected to the power packages with horizontal, surface mount sockets. The two PCBs are connected electrically via socketed jumpers. Figure 5.5 shows an oscilloscope capture of the three gate driver outputs, along with the PWM input signal. Note that the PWM width was reduced so that all tran-

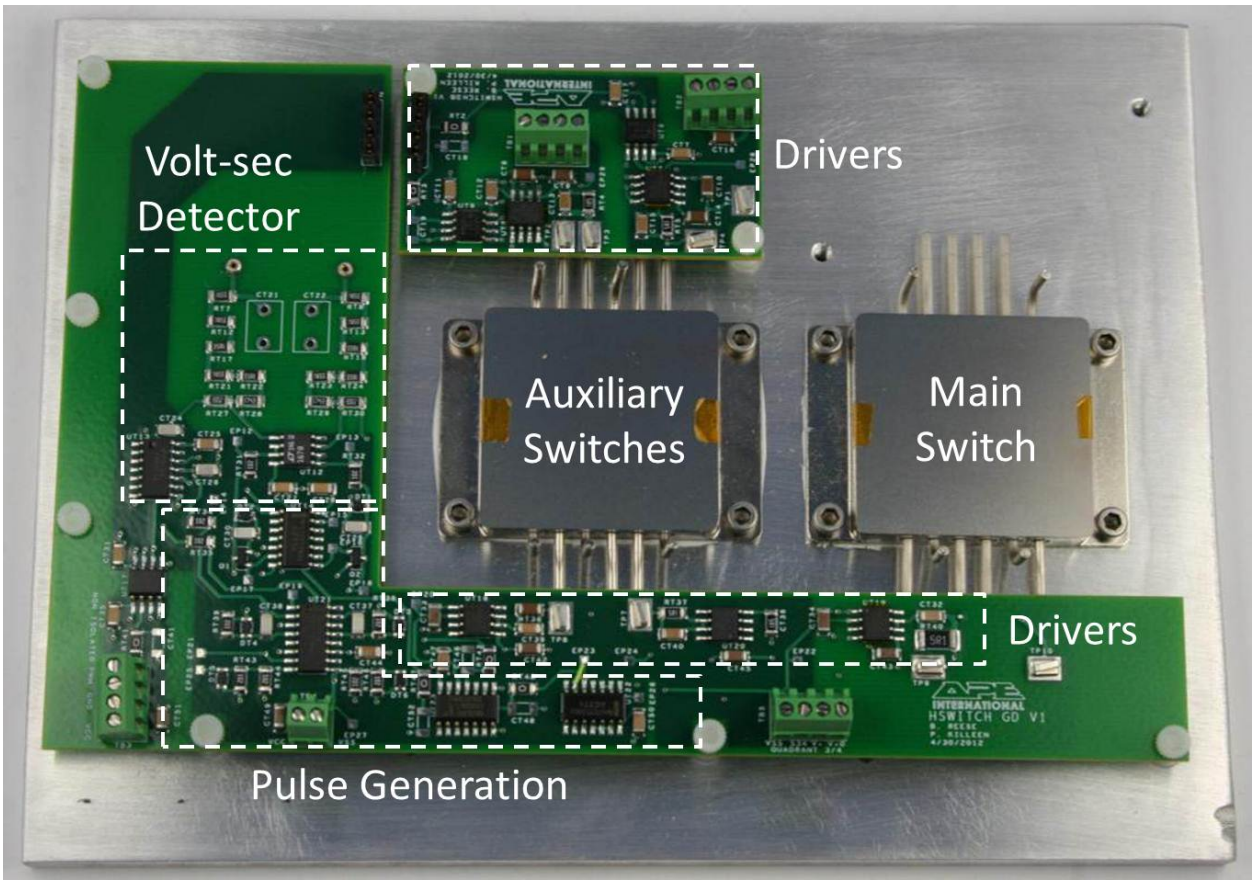


Figure 5.4: Completed gate driver circuitry connected to auxiliary and main switch cells.

sitions could be viewed in the same window. If the switch cell were to operate in this condition it would have very low efficiency since the time required to complete all transitions within the cell are on the same order of magnitude as the conduction time.

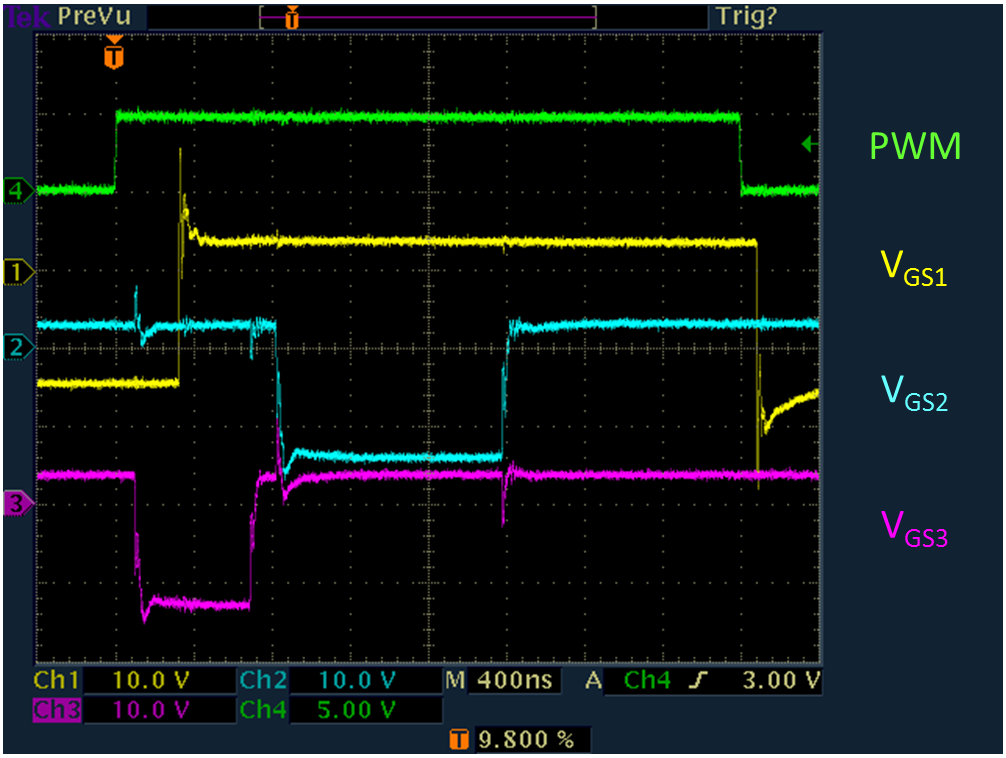


Figure 5.5: Switch cell gate driver waveforms.

CHAPTER 6
SWITCH CELL TESTING

The switch cell's performance was evaluated with a clamped inductive test setup, which is a typical means of measuring switching loss in power switches. The schematic of the test setup is shown in Figure 6.1. An arbitrary function generator was used to provide the PWM signal to the gate driver. The generator was configured for a 50 kHz square wave at 10% duty cycle in burst mode, where the output delivers a finite number of pulses when manually triggered. The gate driver also requires isolated power supplies to power the ground referenced and floating reference gate drivers. The gate driver then provides the gate-to-source signals to the various switch cell devices. The power filtering and sensing board makes connections to the switch cell's power terminals. The board contains an additional diode needed for the recovery circuit, D1, and the recovery sink capacitor, C1. R1 and R2 set the steady state voltage on C1. These components together model an arbitrary recovery circuit whose voltage is a fraction of the input bus. The board also contains the freewheeling diode, D2, of the clamped inductive circuit and a local filtering capacitor, C2, across the input bus. Resistive shunts with 50 Ohm BNC terminations measure the currents through the switch cell and the recovery circuit. The total current path through C2, D2, and the switch cell was minimized to reduce parasitic inductance. The C1, D1, and switch cell path was also minimized for the same reason. Voltage probe sockets are also located on the board to measure the switch cell's drain voltage and the recovery voltage. The sockets were located close to their respective measuring nodes to minimize induced noise. The load inductor was designed for 5 mH and 20 A with low winding capacitance. Several large capacitors were located a longer distance from the switch cell to provide enough energy for the ramp-up stage of the test. A low current power supply was used to charge these bulk capacitors; thus, virtually all of the instantaneous current was supplied from the capacitors. Figure 6.2 shows a photograph of the test setup and locations of the individual blocks. A missing pulse detector circuit (not shown) was used to trigger the oscilloscope on the last pulse received from the function generator.

The first step in the test procedure was to power on all of the circuitry and ensure the cell was in

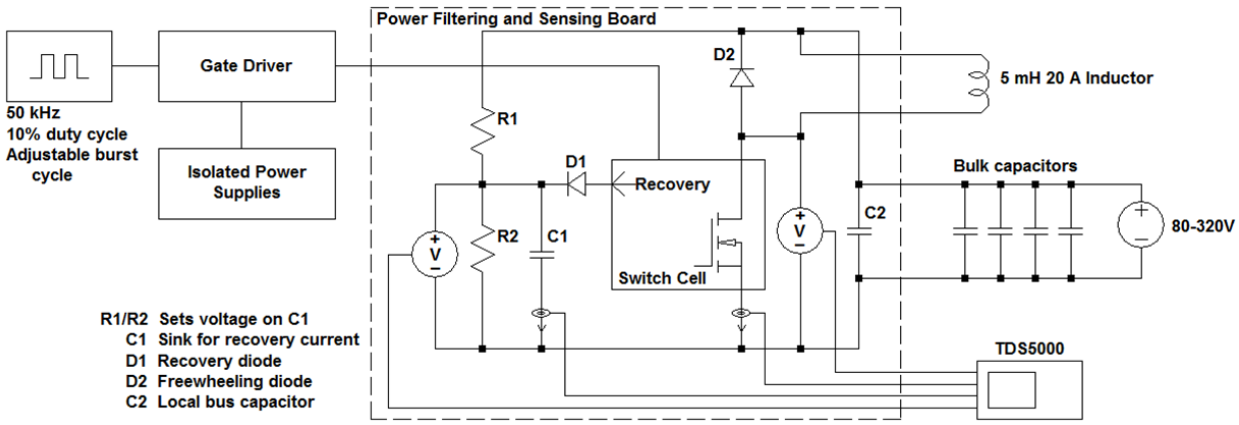
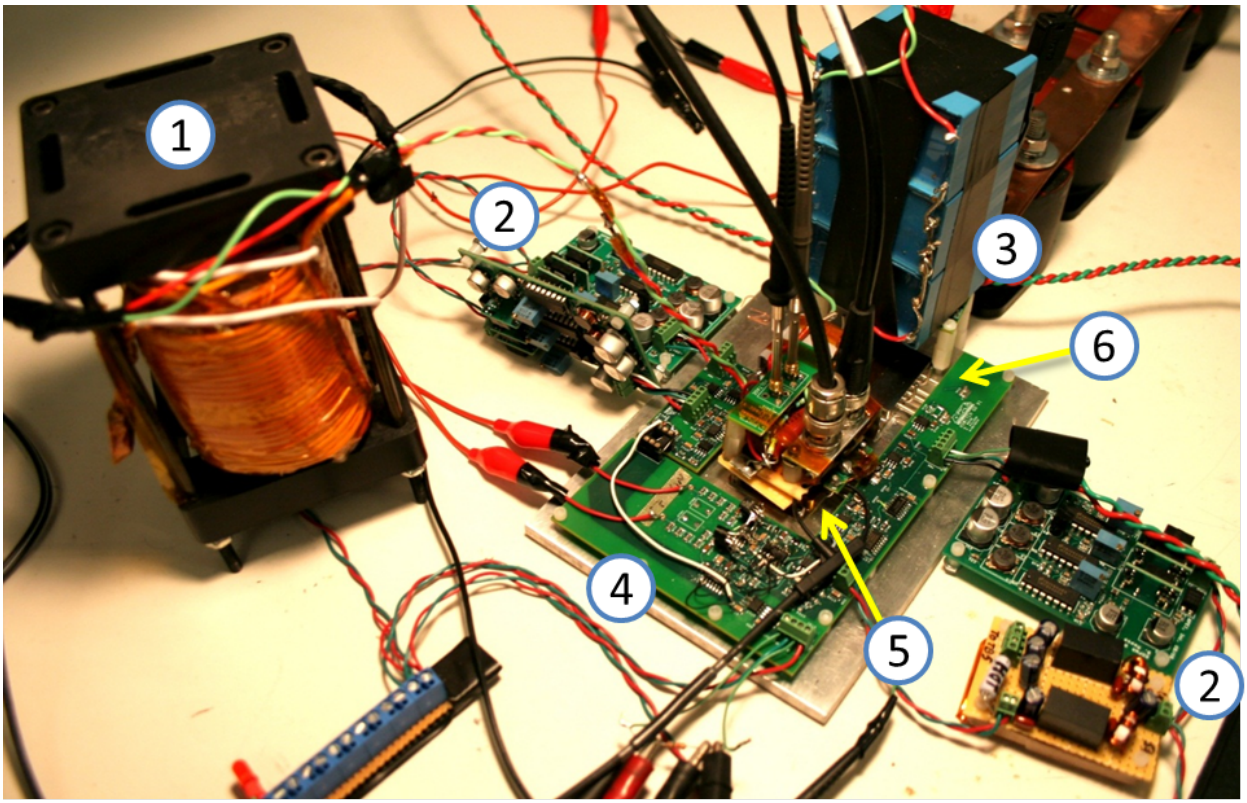


Figure 6.1: Schematic of test setup.



1 Inductor

2 Gate driver power supplies

3 Bus capacitors

4 Gate driver

5 Power filtering and sensing board on top of auxiliary switch

6 Main switch

Figure 6.2: Switch cell test setup.

the off-state while keeping the main power supply turned off. The power supply was then adjusted to the desired voltage. The number of burst pulses from the function generator were varied to achieve the desired inductor current. The oscilloscope triggers on the last pulse (with some delay) where the highest current level takes place. Since the voltage drop across the freewheeling diode is relatively small, the inductor current decreases very little in the switch cell's off-state. Thus, by capturing the turn on and turn off events adjacent to a single off-state the two events occur at virtually the same current. The voltage and current data of both the switch cell and recovery circuit were then saved an analyzed by a spreadsheet designed for switching loss measurements. This process was then repeated for each of the voltage and current data points presented below.

Figures 6.3 and 6.4 detail the results of the spreadsheet analysis at the 160 V and 10 A data point. The figures display the measured voltage (blue), current (red), power loss/gain (purple), and energy loss/gain (green). The power waveforms of the switch cell are shown in Figure 6.3 during turn on (a) and turn off (b). During turn on, the initial disturbance in drain voltage and current is caused by charging the capacitance of S_3 when S_1 turns on. This increases the energy loss to 10 μJ. The main switching event takes place 100 ns later when the inductor saturates. Energy loss increases to 25 μJ. 200 ns later another disturbance on the drain voltage and current occurs when the inductive energy is transferred into the resonant capacitor and recovery circuit. This is caused by parasitic inductance in the switch cell's power paths because the resulting di/dt of changing conductor paths induces transient voltage across the traces. Energy loss increases to 32 μJ. The turn off transition is similar to a single power device with some non-dissipative oscillation. Total turn off loss is 6 μJ. Note that soft switching of the switch cell cannot be observed from its external power terminals. Switches within the cell operate under soft switching during the various transient events. Some of the switching energy shown in these figures is dissipated through the cell, but a significant portion of it is recovered in the recovery circuit.

Figure 6.4 shows the power waveforms of the recovery circuitry during turn on (a) and turn off (b) of the switch cell. The initial disturbance is caused by turning on S_1, just as in the switch cell waveform. 0.7 μJ is taken from the recovery circuit. When the inductor energy is released, the

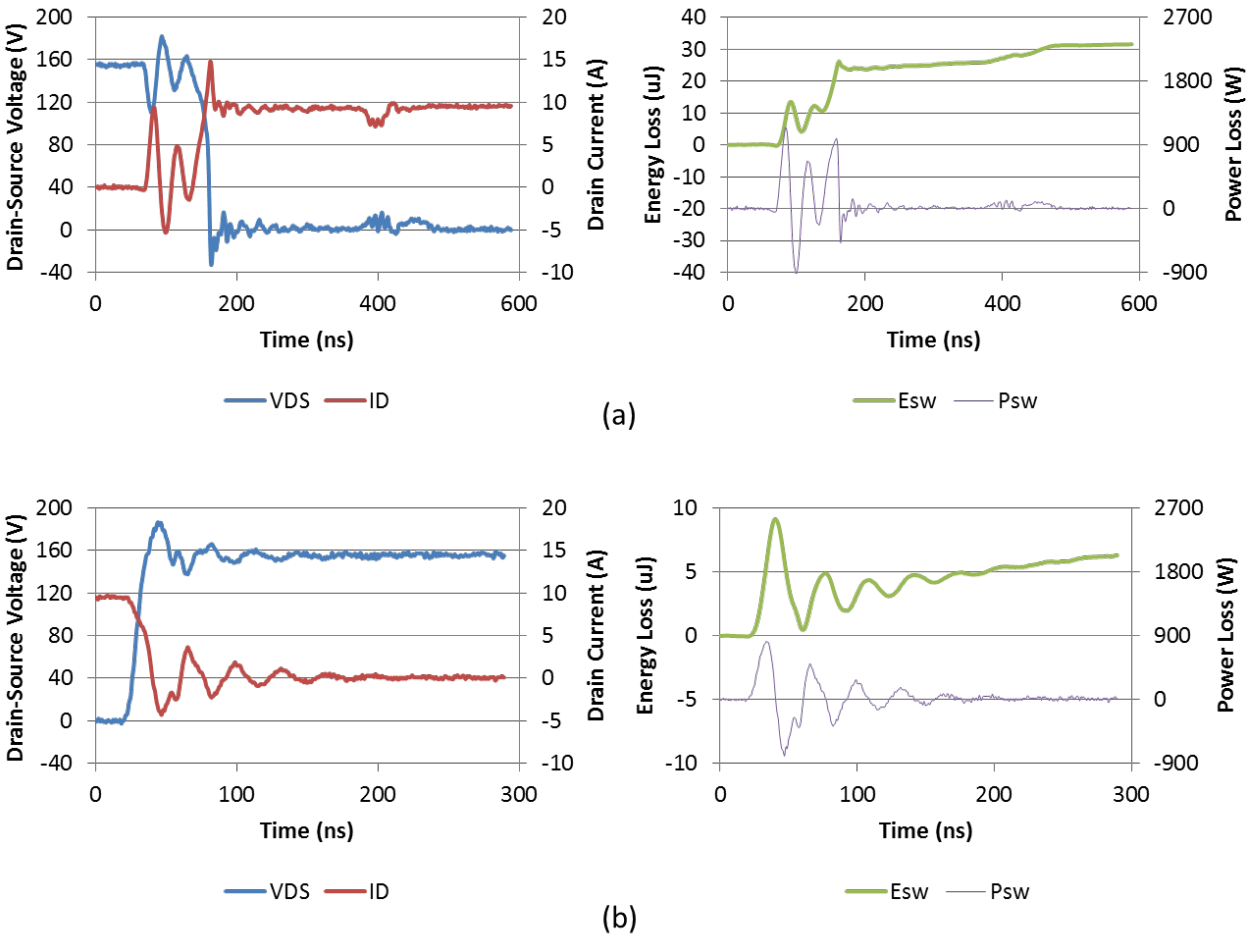


Figure 6.3: Switch cell power waveforms at (a) turn on and (b) turn off, at 160 V and 10 A.

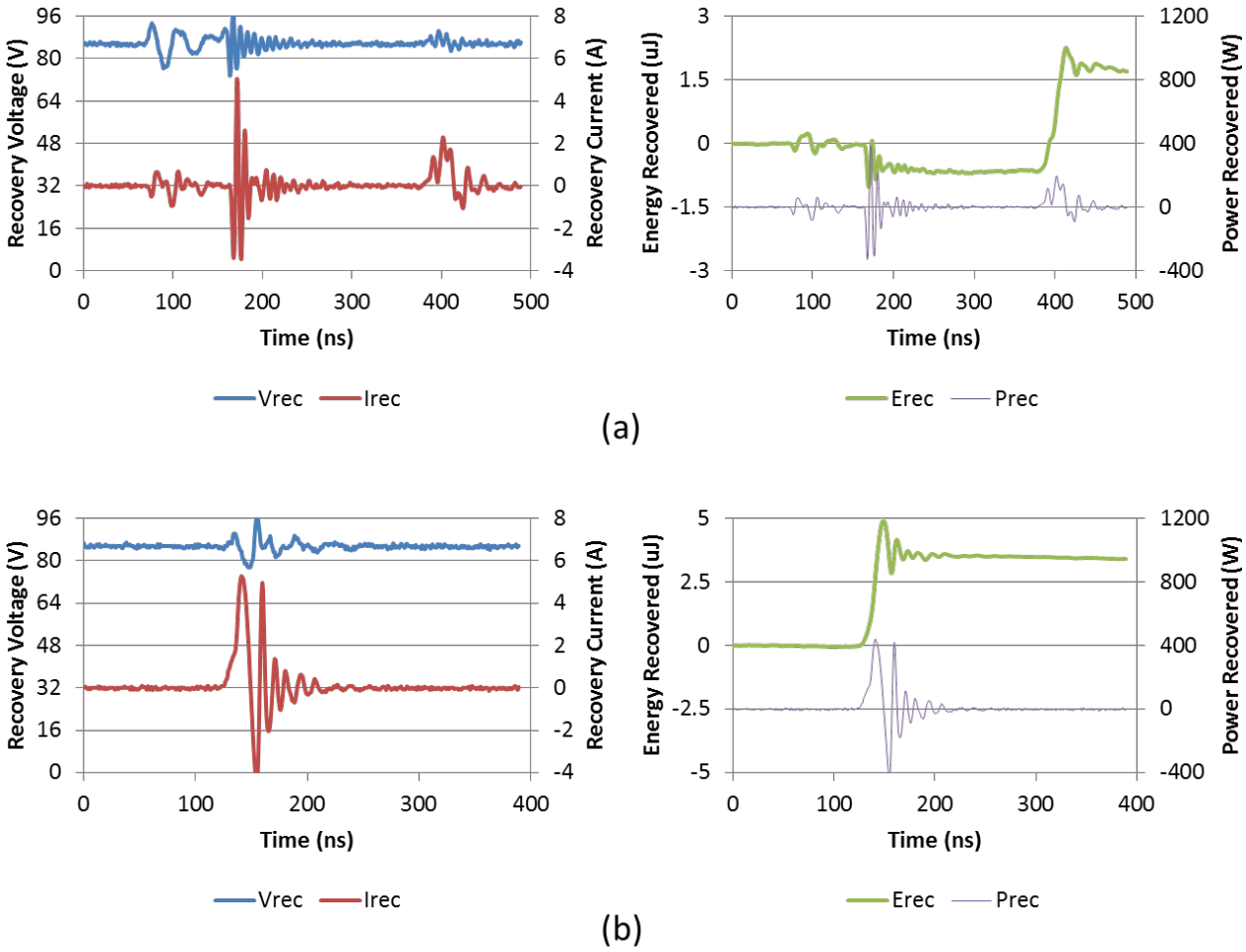


Figure 6.4: Recovery circuit power waveforms at (a) turn on and (b) turn off, with switch cell operating at 160 V and 10 A.

resonant capacitor charges completely and a small amount of energy transfers into the recovery circuit, increasing the total recovered energy during turn on to 1.8 μJ. At turn off, the main current through the switch cell is redirected through the recovery circuit, increasing recovered energy during turn off to 3.5 μJ. The total switching loss of the switch cell is then calculated as the difference between the switch cell energy loss and the energy recovered in the recovery circuit. In this case, the total switching loss is 32 + 6 - 1.8 - 3.5 = 32.7 μJ. The total switching loss of a single power switch under hard switching is 70 μJ. The switch cell reduces total switching loss by a factor of two at this data point.

The process presented above was repeated for several data points in the range of 80-320 V and

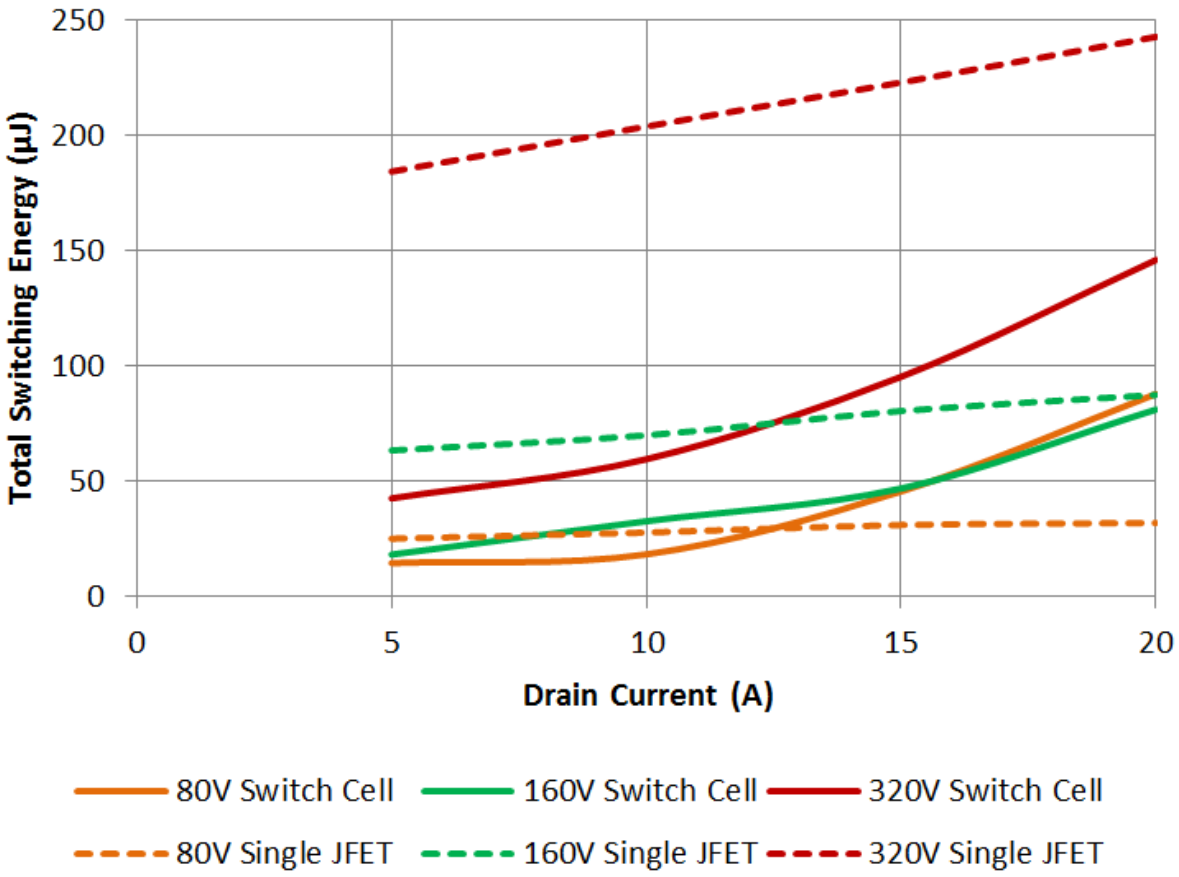


Figure 6.5: Switching loss measurement of the nonlinear resonant switch cell.

5-20 A. This range was chosen to align with the targeted application's operating points. Figure 6.5 shows a comparison of switching energy vs. drain current between a single JFET (dashed) and the switch cell (solid) at 80 V (orange), 160 V (green), and 320 V (red). At 80 V the switch cell has minimal improvement and is actually less efficient at higher current levels. At 160 V the switch cell outperforms the single JFET at all current levels, but they begin to converge as the drain current approaches 20 A. At 320 V the switch cell achieves up to 4.3x reduction in switching loss compared to the single JFET and maintains a high reduction rate over the entire current range.

CHAPTER 7
CONCLUSION

A novel nonlinear switch cell is presented which achieves up to 4.3x reduction in switching loss over a single power device. The cell utilizes a saturable resonant inductor which is much smaller and more efficient than equivalent linear inductors. The switch cell topology allows proper flux resetting of the saturable inductor and transfers energy stored in the inductor into capacitances for more efficient storage during steady-state operation. Additionally, the switch cell is capable of redirecting switching energy to an arbitrary sink, such as the main power bus, the load, or an auxiliary supply (e.g. to supply a power system's controller and/or gate driver circuitries).

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APPENDIX A

OCTAVE/MATLAB CODE

A.1 ind_tb.m

```
function indopt = ind_tb ()


## define inductor operational parameters
ind.f      = 200000; # switching frequency
ind.Vdsmax = 600; # max rated voltage
ind.Ilrms  = 0.1; # rms current of inductor (NOT switch)
# saturation time at VDS,max -  same as switch fall time at that voltage
ind.tsat   = 50e-9;
# Ratio of max rated voltage to max resonant capacitor voltage
ind.Kcd    = 0.5;

## manufacturing constraints
ind.r1min  = 0; #2.54e-5*20; # minimum practical core inside radius, in m
ind.wmin   = 0; #2.54e-5*10; # minimum core practical width, in m
ind.Nmax   = 100; # maximum number of turns
ind.hmax   = 1000; #2.54e-5*155*8; # maximum core height
ind.Dwdgmin = 0; #0.00026; # minimum wire diameter

## winding material constants
ind.rho  = 0.5*1.68e-8;  # Resistivity in ohm-m (prefixed with fill factor)

## choose core materials
ind.FOM = 1e12;
indtest = ind;
indopt = ind;
for i=1:7
  indtest = ind_material(ind,i);
  indtest = ind_opt(indtest);
  FOM(i)=indtest.FOM;
  if (indtest.FOM < indopt.FOM)
 indopt = indtest;
  endif
  ind.FOM_N=indtest.FOM_N;
endfor

indopt.FOM_material=FOM;
indopt.FOM_N=ind.FOM_N;
```

```
orderfields(ind);

loglog(1:indopt.Nmax,indopt.FOM_N)
legend('1','2','3','4','5','6','7')

endfunction
```

A.2 ind_material.m

```
## define inductor core material constants
# ind.corename = "ferrox-3C30";
# ind.uie  = 5e3*uo; # absolute
# ind.Bsat = 0.45; # Tesla
# ind.a    = 1.42; # Steinmetz frequency exponent, f in Hz
# ind.B    = 3.02; # Steinmetz flux density exponent, B in T
# ind.k    = 7.13e-3/1e3*1e6; # Steinmetz coefficient, Psp in W/m^3
# ## calc ki, depends only on core material params
# ind.ki = ind.k/( (2*pi)^(ind.a-1) *
#      quadgk(@(x) abs(cos(x)).^ind.a,0,2*pi) * 2^(ind.B-ind.a));
## Author: Bradley Reese

function ind = ind_material (ind,i)

 uo=4*pi*10^-7;   # permeability of free space

 switch i

  case {1} # Ferroxcube 3C30
ind.corename = "ferrox-3C30";
ind.uie  = 5e3*uo;
ind.Bsat = 0.45;
ind.a    = 1.42;
ind.B    = 3.02;
ind.k    = 7.13e-3/1e3*1e6;

  case {2} # Ferroxcube 3C90
ind.corename = "ferrox-3C90";
ind.uie  = 5e3*uo;
ind.Bsat = 0.4;
ind.a    = 1.46;
```

```
ind.B    = 2.75;
ind.k    = 3.2e-3/1e3*1e6;

  case {3} # Ferroxcube 3C94
ind.corename = "ferrox-3C94";
ind.uie  = 5e3*uo;
ind.Bsat = 0.4;
ind.a    = 2.6;
ind.B    = 2.75;
ind.k    = 2e-9/1e3*1e6;

  case {4} # Ferroxcube 3F3
ind.corename = "ferrox-3F3";
ind.uie  = 4e3*uo;
ind.Bsat = 0.4;
ind.a    = 1.8;
ind.B    = 2.5;
ind.k    = 2e-5/1e3*1e6;

  case {5} # Ferroxcube 3F4
ind.corename = "ferrox-3F4";
ind.uie  = 1.7e3*uo;
ind.Bsat = 0.38;
ind.a    = 1.75;
ind.B    = 2.9;
ind.k    = 12e-4/1e3*1e6;

  case {6} # Metglas Finemet
ind.corename = "metglas-finemet";
ind.uie  = 15e3*uo;
ind.Bsat = 1.2;
ind.a    = 1.53;
ind.B    = 1.52;
ind.k    = 1.19/1000^1.53/1e3*7.3*1e6;

  case {7} # Metglas Powerlite
ind.corename = "metglas-powerlite";
ind.uie  = 5e3*uo;
ind.Bsat = 1.56;
ind.a    = 1.51;
ind.B    = 1.74;
ind.k    = 6.5/1000^1.51/1e3*7.18*1e6;


 otherwise
```

```
error("ind_material: invalid value");
 endswitch

## calc ki, depends only on core material params
ind.ki = ind.k/( (2*pi)^(ind.a-1) * ...
quadgk(@(x) abs(cos(x)).^ind.a,0,2*pi) * 2^(ind.B-ind.a));

  ind.coreindex = i;

endfunction
```

A.3 ind_opt.m

```
## -*- texinfo -*-
## @deftypefn {Function File} {} ind_opt (@var{ind})
## This function optimizes the nonlinear switch cell inductor given
## material and operational constants.
##
## @example
## @group
##
##      @result{}
## @end group
## @end example
##
## @seealso{}
## @end deftypefn

## Author: Bradley Reese

function ind_out = ind_opt (ind)

# initialize inductor
ind_out.err = 1;
ind_out.FOM = 1e12;

## for toroidal cores:

#N LOOP!!!
for ind.N = 1:ind.Nmax
```

```
# set r1min based on min wire size and number of turns
ind.r1min = max(ind.r1min,sqrt(ind.N*ind.Dwdgmin^2/pi));

# define cross sectional area
ind.Ae = ind.Vdsmax*ind.tsat/2/ind.Bsat/ind.N;

# initialize core geometry
ind.r1 = 1;
ind.r2 = 2;
ind.h  = ind.Ae;

# calculate FOM constants
ind = ind_eval(ind);

# calculate w solution constants
ind.Klt4 = sqrt(ind.Klt3*ind.Ae/(pi*(ind.Klt1+ind.Klt2)));

a = 1-0.7*ind.Klt4;
b = ind.Ae+1.7*ind.Klt4;
c = -ind.Klt4*ind.Ae;

# initialize test inductors
ind.FOM = 1e12;
ind.err = 0;
ind1 = ind;
ind2 = ind;


% test first width solution
ind.w = sqrt((-b+sqrt(b^2-4*a*c))/(2*a));
if (isreal(ind.w) && ind.w!=0)
 ind.r1 = ind.w*(ind.Ae+ind.w^2)/(ind.Ae-ind.w^2);
 ind.r2 = ind.r1 + ind.w;
 ind.h = ind.Ae/ind.w;
 ind1 = ind_eval(ind);
endif

% test second width solution
ind.w = sqrt((-b-sqrt(b^2-4*a*c))/(2*a));
if (isreal(ind.w) && ind.w!=0)
 ind.r1 = ind.w*(ind.Ae+ind.w^2)/(ind.Ae-ind.w^2);
 ind.r2 = ind.r1 + ind.w;
 ind.h = ind.Ae/ind.w;
 ind2 = ind_eval(ind);
endif
```

```
# error checking, assignment
if (ind1.FOM == 1e12 && ind2.FOM == 1e12)
#fprintf("ind_opt: ERROR - w solution not found");
ind.err = 1;
 elseif(ind1.FOM < ind2.FOM)
ind = ind1;
 else
ind = ind2;
endif


# alternate solution for w if r1 violates constraint
# or if w solution not found
 if (ind.r1 < ind.r1min || ind.FOM==1e12)
  ind.r1 = ind.r1min;
  ind.w = (pi*ind.r1^2*(ind.Klt1+ind.Klt2) ...
/ind.Klt3/ind.Ae+1/ind.Ae)^-0.5;
  ind.r2 = ind.r1 + ind.w;
  ind.h = ind.Ae/ind.w;
endif

# check for min width
 if (ind.w < ind.wmin)
  ind.w = ind.wmin;
  ind.r2 = ind.r1 + ind.w;
  ind.h = ind.Ae/ind.w;
endif

# check for max height
 if (ind.h > ind.hmax)
  ind.h = ind.hmax;
  ind.w = ind.Ae/ind.h;
  ind.r2 = ind.r1 + ind.w;
endif

ind = ind_eval(ind);

if (ind.err !=1 && ind.FOM < ind_out.FOM)
ind_out = ind;
endif

FOM_N(ind.N)=ind.FOM;
```

```
endfor

ind_out.FOM_N(ind_out.coreindex,:)=FOM_N;

endfunction
```

A.4 ind_eval.m

```
## Author: Bradley Reese
## requires core material params, geometry,
## resistivity, number of turns
function ind = ind_eval (ind)

## for toroidal cores:
ind.w = ind.r2 - ind.r1;
ind.Ae = ind.h*ind.w;
ind.le = 2*pi*log(ind.r2/ind.r1)/(1/ind.r1-1/ind.r2);
ind.Pcsp = ind.f*ind.ki*(2*ind.Bsat)^(ind.B-ind.a)* ...
(ind.Vdsmax/ind.N/ind.Ae)^ind.a*(ind.tsat/(ind.a+1)+ ...
ind.Kcd^ind.a*(ind.tsat/(ind.a+1)+ind.tsat/ind.Kcd-ind.tsat));
ind.Klt1 = ind.f*ind.Vdsmax^2*ind.tsat^2 ...
/(24*ind.uie*ind.N^2*ind.Ae)*(1+ind.Kcd^2);
ind.Klt2 = ind.Pcsp*ind.Ae;
ind.Klt3 = 2*ind.Ilrms^2*ind.rho*ind.N^2/pi;
ind.Psw = ind.Klt1*ind.le;
ind.Pcore = ind.Klt2*ind.le;
ind.Pwdg = ind.Klt3*(ind.Ae/ind.w+ind.w)/ind.r1^2;
ind.FOM = ind.Psw + ind.Pcore + ind.Pwdg;
ind.err = 0;

endfunction
```

APPENDIX B

SPICE NETLISTS

B.1 Nonlinear Resonant Switch Cell

```
I1 N001 DRN {Id}
V1 N001 0 PULSE(0 {Vbus} 10n 500n 500n 1 1)
D3 DRN N001 Cree
V3 stepparam 0 PULSE(0 {stepparam} {(perstart+Nper)/fs-60n}
+20n 20n 20n {Nper/fs})
I2 N002 DRNstan {Id}
V5 N002 0 {Vbus}
D1 DRNstan N002 Cree
XX1 P001 N026 hodgdon
XX2 C N020 N030 N021 N022 N025 N028 switch_packaged
V4 2 0 PULSE(0 1 5n 1p 1p {0.5/fs} {1/fs})
XX4 DRNstan N011 DRNstan 0 N007 N008 pmeter
C2 N002 DRNstan 1n
V6 4 0 PULSE(1 0 -20n 1p 1p 800n {1/fs})
XX7 3 N026 N034 N031 E1 N033 Et1 switch_packaged
V7 3 0 PULSE(1 0 800n 1p 1p 1600n {1/fs})
D5 N004 N012 Cree
C1 N003 N006 470p
B1 Etot 0 V=V(Et1)+V(Et4)+V(Et2)+V(Et3)+V(Et5)+V(Et6)
L1 P001 N027 {100n+2*Lconn}
XX3 2 N003 N027 N010 E4 NC_01 Et4 switch_packaged
XX5 4 N027 N035 N032 E2 NC_02 Et2 switch_packaged
L2 N030 0 {Lconn}
L3 N011 N020 {Lconn}
XX6 0 N006 N026 N009 E3 NC_03 Et3 switch_packaged
L4 N036 N035 {Lconn}
L5 N003 DRN {Lconn}
L6 N006 N005 {Lconn}
L7 N035 N034 {Ls}
V2 N017 0 {Vbus/2}
L8 N005 N004 {Lconn}
XX8 N036 0 DRN 0 N037 N038 pmeter
XX9 N012 N017 N012 0 N013 N016 pmeter
XX10 0 N014 N029 N018 E5 N023 Et5 switch_packaged
L9 N029 N036 {Lconn}
L10 N001 N014 {Lconn}
B5 Esw 0 V=V(E1)+V(E4)+V(E2)+V(E3)+V(E5)+V(E6)
XX11 0 N015 N029 N019 E6 N024 Et6 switch_packaged
```

```
L11 N015 N014 15n

* block symbol definitions
.subckt hodgdon V+ V-
B1 V+ V- I=V(H)*{le/N}
B2 dB 0 V=(V(V+)-V(V-))/{N*Ac}
B3 B 0 V=idt(V(dB))
B4 f 0 V=if( {Bbp} - abs(V(B)) +0.5, {A1}*tan({A2}*V(B)) ,
+if( V(B) + 0.5, {A1}*tan({A2*Bbp})+(V(B)-{Bbp})/{us},
+{-1*A1}*tan({A2*Bbp})+(V(B)+{Bbp})/{us}) )
B5 df 0 V=if( {Bbp} - abs(V(B)) +0.5, {A1*A2}/cos({A2}*V(B))**2,
+ {1/us} )
B6 g 0 V=if(abs(V(B))+0.5-({Bcl}),V(df),V(df)*(1-({A3})*V(c)*
+exp(-({A4})*abs(V(B))/({Bcl}-abs(V(B)))))
B7 dH 0 V=a*abs(V(dB))*(V(f)-V(H))+V(dB)*V(g)
B8 H 0 V=idt(V(dH))
B9 c 0 V=1
R1 V+ V- 1meg
.param N=3 le=6.1594e-3 Ac=6.725e-6
.param uo=4*3.14e-7

.param Bcl=0.41 Bbp=0.41725 Hcl=500 us=1e-5 a=400 A1=30.03
+A2=3.685 A3=-95.4 A4=0.52

.ends hodgdon

.subckt switch_packaged P D S Psw Esw Pt Et
J1 N008 N007 N011 SS
L2 D N001 {Ld} Rser={RL}
C2 N007 N011 {Cgs} Rser={RCgs} Lser={LCgs}
L4 N011 S {Ls}
D2 N011 N009 Cree
L5 D N002 {Ld} Rser={RL}
L6 N007 N006 {Lg+Lconn} Rser={RL}
L7 N011 N014 {Lg+Lconn} Rser={RL}
B1 N003 N014 V=if(V(P),{GDp},{GDn})
R1 N006 N005 {Rg}
C1 N006 N005 {Cg} Rser={RCg} Lser={LCg}
XX1 N001 N008 N001 N011 Ps Es pmeter
XX2 N002 N009 N002 N011 Pd Ed pmeter
J2 N013 N016 0 SS
R2 N016 N015 {Rg}
B2 0 N012 I=Id(J1)
V1 N015 0 {GDp}
XX3 N012 N013 N012 0 Pscond Escond pmeter
```

```
B3 Psw 0 V=V(Ps)-V(Pscond)+V(Pd)
B4 Esw 0 V=V(Es)-V(Escond)+V(Ed)
B5 Pt 0 V=V(Ps)+V(Pd)
B6 Et 0 V=V(Es)+V(Ed)
R3 N005 N010 4.25
D1 N003 N010 IdealDiode
D3 N004 N003 IdealDiode
R4 N005 N004 1
C3 N009 N011 1p
.param GDp=5 GDn=-15 Rg=1
.param Lg=1n Ld=10n Ls=15n Lconn=40n RL=10u
.param Cgs=4.7n RCgs=10m LCgs=2n
.param Cg=0.1u RCg=10m LCg=1n
.model IdealDiode D(Ron=1m Roff=1Meg Vfwd=0)
.model SS NJF(Pb=3 Is=1e-17 Beta=800 Rd=15m Rs=0.025 Vto=1.35
+N=3 B=1  Cgd=1.5n Cgs=1.5n mfg=SemiSouth Lambda=.1)
.model Cree D(Cjo=1000p Eg=1.6 BV=1200 mfg=Cree type=Schottky
+Rs=0.0573 Vj=0.92 Is=3.2e-16)
.ends switch_packaged

.subckt pmeter I+ I- V+ V- P E
V1 I+ I- 0
B1 P 0 V=I(V1)*(V(V+)-V(V-))
B2 E 0 V=idt(V(P),0,inv(0.5+time-{Estart}))
.ends pmeter

.model D D
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.dio
.model NJF NJF
.model PJF PJF
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.jft
.tran 0 {(perstart+Nper)/fs} {(perstart+Nper)/fs-60n}
.ic V(SD)={Vbus}
.param VCC=5 Vbus=320 Id=stepparam Vctl=Vbus stepparam=20
+Cload=1p Csn1=10n Csn2=2n Lconn=40n Ls=15n
.param fs=100000 perstart=0 Nper=3 Estart=1/fs
.model Cree D(Cjo=1000p Eg=1.6 BV=1200 mfg=Cree type=Schottky
+Rs=0.0573 Vj=0.92 Is=3.2e-16)
.model IdealDiode D(Ron=1p Roff=1000Meg Vfwd=0)
*.OPTIONS abstol=1n vntol=1u reltol=0.01 itl1=150 itl2=150
+itl4=500 method=GEAR
.OPTIONS abstol=1n vntol=1u reltol=0.005 itl1=150 itl2=150
+itl4=500 method=GEAR
.step param stepparam list 1 5 10 15 20
.backanno
```

```
.end
```

B.2 Gate Driver

```
V1 VCC 0 5
V2 PWM 0 PULSE(0 5 0 1p 1p {0.5/fs} {1/fs})
V3 Vrec 0 {Vrec}
XX7 VCC N010 0 N006 Vrec vsdetect
XX1 VCC N001 0 PWM Vbus vsdetect
R3 N005 PWM {Rdt}
C3 N005 0 {Cdt}
XX5 N005 0 0 N008 VCC VCC1 iso721 params: ISO721
XX6 N008 N009 V+1 0 ixdn609
R1 G3 N003 {Rg}
C1 G3 N003 {Cg}
R5 G2 N012 {Rg}
C5 G2 N012 {Cg}
R4 G1 N009 {Rg}
C4 G1 N009 {Cg}
XX3 N002 N003 V+1 0 ixdn609
XX9 N011 N012 V+1 0 ixdn609
C2 0 N007 {Col}
XX4 N007 0 N006 invert
R2 N001 N007 {Rol}
XX2 N001 0 N002 invert
XX8 N010 0 N011 invert
V7 N004 0 15
V8 V+1 N004 5
V4 Vbus 0 {Vbus}
D1 N005 PWM 1N914
XX10 N004 S3 jmp
XX11 N004 S2 jmp
XX12 N004 S1 jmp
XX13 VCC1 VCC jmp
XX14 VSS 0 jmp

* block symbol definitions
.subckt vsdetect VCC P VSS IN Vsen
C2 VCCS VSS 1n
M1 VCCS N006 VSS VSS BSS123
XU1 N004 N002 N003 VCC VSS LT1678
```

```
R3 N002 VSS 100
R1 Vsen N004 5MEG
R2 N004 VSS 30k
XU2 VCC IN VSS N007 N005 P VCC sn74act74d params: SN74ACT74D
Q1 N001 N003 N002 0 2N3904
C1 N004 VSS 100p
Q2 N001 N001 VCC 0 2N3906
Q3 VCCS N001 VCC 0 2N3906
R4 N006 N005 10
XX1 VCCS VSS N007 invert
.ends vsdetect

.subckt iso721 IN VSS1 VSS2 OUT VCC1 VCC2
R1 OUT N001 35
E2 N001 VSS2 N002 VSS1 1
A2 IN VSS1 VSS1 VSS1 VSS1 VSS1 N002 VSS1 SCHMITT Vt={0.5*VCC}
+Vh=0.15 Vhigh={VCC} Vlow=0 Td=20n Trise=2n Tfall=2n
.param VCC=5
.ends iso721

.subckt ixdn609 IN OUT VCC VSS
S1 OUT VCC N003 VSS MySW
S2 OUT VSS N005 VSS MySW
A1 N001 N004 VSS VSS VSS VSS N005 VSS AND
A2 N002 N001 VSS VSS VSS VSS N003 VSS AND
A3 N002 VSS VSS VSS VSS N004 VSS VSS BUF
R1 VCC N001 200k
A4 IN VSS VSS VSS VSS VSS N002 VSS SCHMITT Vt=1.9 Vh=1.1 Vhigh=1
+Vlow=0 Td=40n Trise=2n Tfall=2n
.model MySW SW(Vt=0.5 Ron=0.8 Roff=1MEG)
.ends ixdn609

.subckt invert in VSS out
A1 IN VSS VSS VSS VSS OUT VSS VSS SCHMITT Vt={0.5*VCC} Vh=1
+Vhigh={VCC} Vlow=0 Td=6n Trise=2n Tfall=2n
.ends invert

.subckt jmp 1 2
R1 2 1 1m
.ends jmp

.subckt sn74act74d D CLK VSS CLR _Q Q SET
A1 D VSS CLK N001 N004 N003 N002 VSS DFLOP Vhigh={VCC} Td=6n
A2 SET VSS VSS VSS VSS N001 VSS VSS BUF Vhigh={VCC}
A3 CLR VSS VSS VSS VSS N004 VSS VSS BUF Vhigh={VCC}
```

```
R1 Q N002 50
R2 _Q N003 50
.param VCC=5
.ends sn74act74d

.model D D
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.dio
.model NPN NPN
.model PNP PNP
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.bjt
.model NMOS NMOS
.model PMOS PMOS
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.mos
.tran 0 22u 20u
* External Signals
.step param Vrec list 100 125 150
.param VCC=5 fs=1/20u Vbus=100 Vrec=100
+ Rol=1k Col=100p
+ Rdt=1k Cdt=100p
+ Rg=1 Cg=1n
.lib LTC2.LIB
.backanno
.end
```