Bendix
Aerospace Systems Division

NO.	REV. NO.
ATM-962	

Array E System Grounding Philosophy

DATE

This ATM briefly describes modifications to system grounding philosophy from those applied on previous flights and provides system, component, and experiment grounding details.

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This ATM is written to document the ALSEP Array E grounding philosophy which has been modified from that employed in previous ALSEP systems. The grounding philosophy employed in flights A thru D is documented in ATM-411, 484 and 530.

Figures 1 thru 11 provide the details of the Array E component, central station and experiment grounding arrangements. The most significant changes in grounding philosophy from that of previous systems involves the use of the central station thermal plate as a ground plane. Previous systems employed a single point ground located in the PDU. In Array E the ground plane approach, which essentially enlarges the magnitude of the single point ground, is used to minimize inductance of paths between components. Inter-component inductance must be minimized in Array E because low power TTL logic, capable of faster switching rates than previous employed logic, is used extensively in the redesigned command decoder, data processor and PCU/PDU. Reducing inductance thus reduces $L(di/dt)$ noise generated by logic switching coupled from circuit to circuit in the grounds.

Inductive paths in the central station are minimized by employing ground planes on component PC boards and by using the component mounting structure and base plate as an electrical signal return path. The thermal plate therefore provides the remaining portion of the signal return path. This concept minimizes inductance by employing the largest physical structures as a conducting ground path. To successfully implement this concept the component mounting structure, base and the thermal plate surface must be designed to provide good electrical continuity and a low impedance path at high frequencies. A design goal of less than 20 millivolts IX_C or IX_L drop and less than 20 milliohm resistance between two signal points has been established. The thermal plate and new components will employ gold mounting interfaces to optimize electrical continuity between mechanical interfaces. Thermal grease will not be employed if it is detrimental to electrical characteristics. The entire thermal plate will be gold plated to provide a low impedance path between components.

The thermal plate ground plane provides three means for completing ground connections.

a. Component mechanical mounting interface.
b. Terminal board mounting interface.
c. Two ground studs.

New component designs will employ method (a) but will carry a "safety" ground wire thru the component connector for test purposes. Previously designed components have been designed to operate on an anodized thermal plate. Their grounds will therefore be connected thru the central station harness to the thermal plate ground studs (method c). The RTG PCU/PDU and experiment grounds will use method b) to complete ground connections to the thermal plate ground plane. The use of multiple grounding techniques on the thermal plate does not violate the single point ground philosophy. This is possible because the impedance of signal return paths will be maintained below a level which can cause significant noise.

Figures 1 thru 9 depict the component grounding arrangements. The following comments apply:

a. Capacitors are depicted in signal lines to show DC isolation.

b. Internal dashed lines indicated component chassis which may be isolated from mounting surface chassis.

c. A chassis ground symbol depicts the conductive component/ experiment mounting surface.

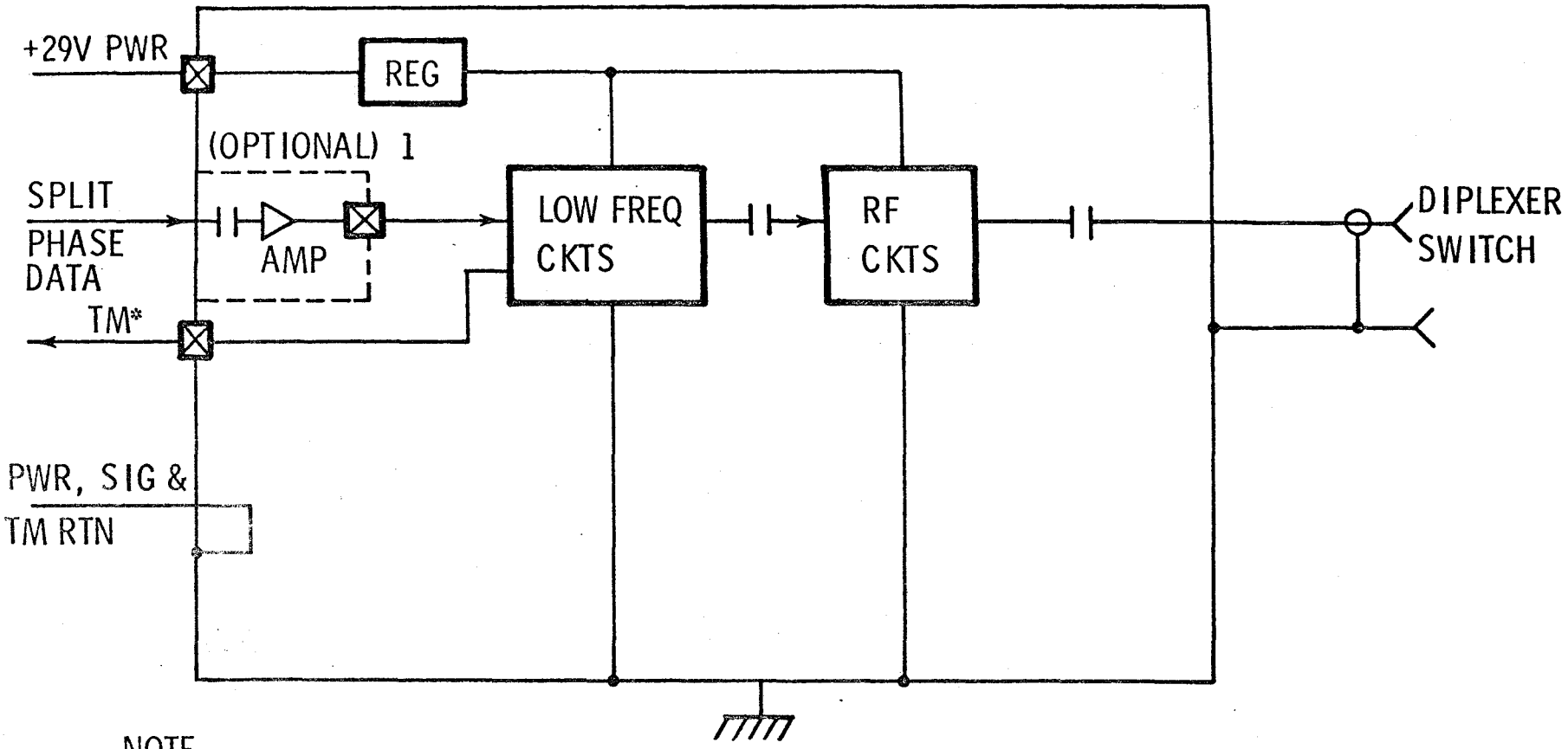
d. To minimize capacitive pickup the LEAM experiment may not use a separate chassis ground. The grounding arrangement employed will be dependent on development testing.

System grounding arrangements are depicted in Figures 10 and 11. The following comments apply:

a. Parallel alternate signal return conductors will be used in the experiment flat cables in lieu of the previously employed alternate shield conductors. This modification will reduce crosstalk on the timing and control lines.

b. The receiver mounting surface is not compatible with the gold finish and will thus be isolated from the thermal plate by an anodized aluminum shim less than 1/32 inch thick.

c. The PSE CSE will be isolated from the thermal plate in a manner similar to the receiver because its mounting surface is incompatible with gold.



ALSEP TRANSMITTER - TELEDYNE

FIGURE 1

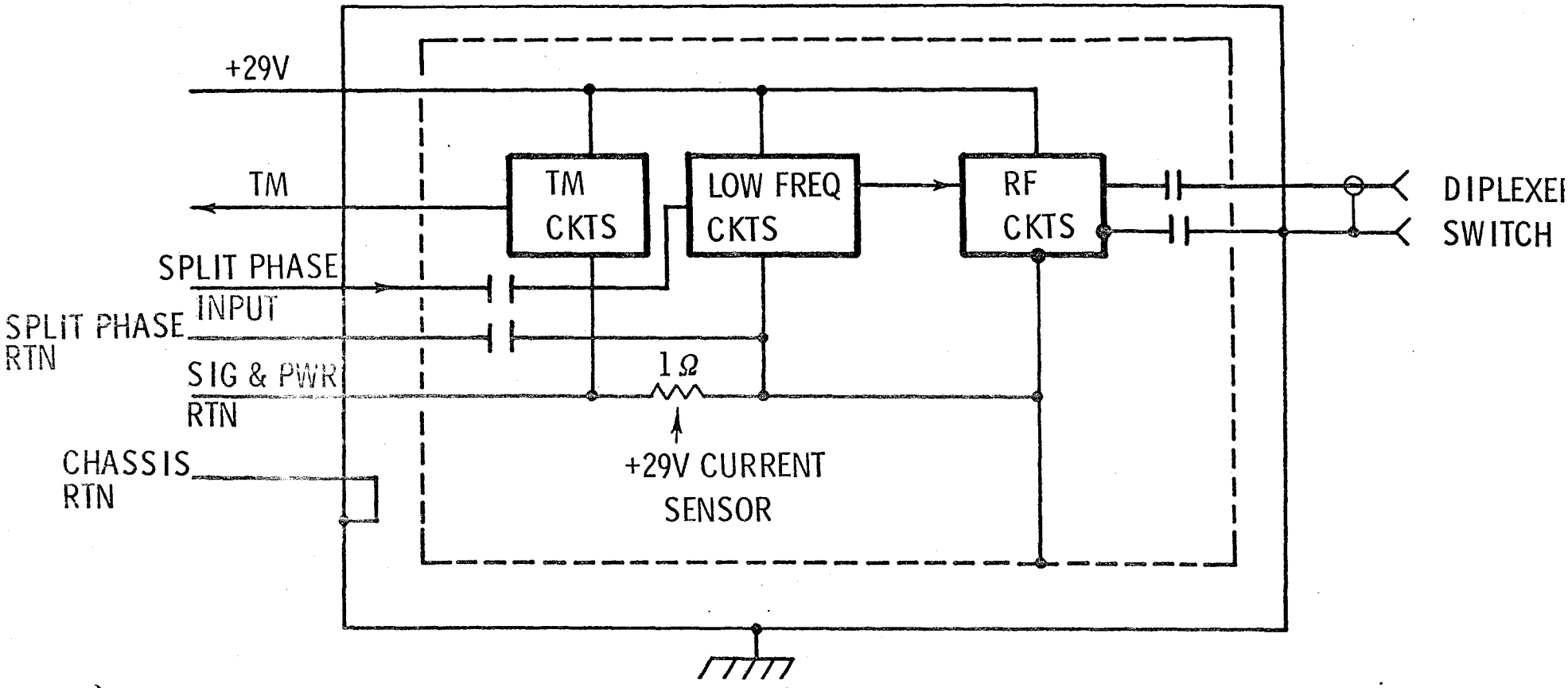


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FIGURE 2

ALSEP ARRAY E RECEIVER

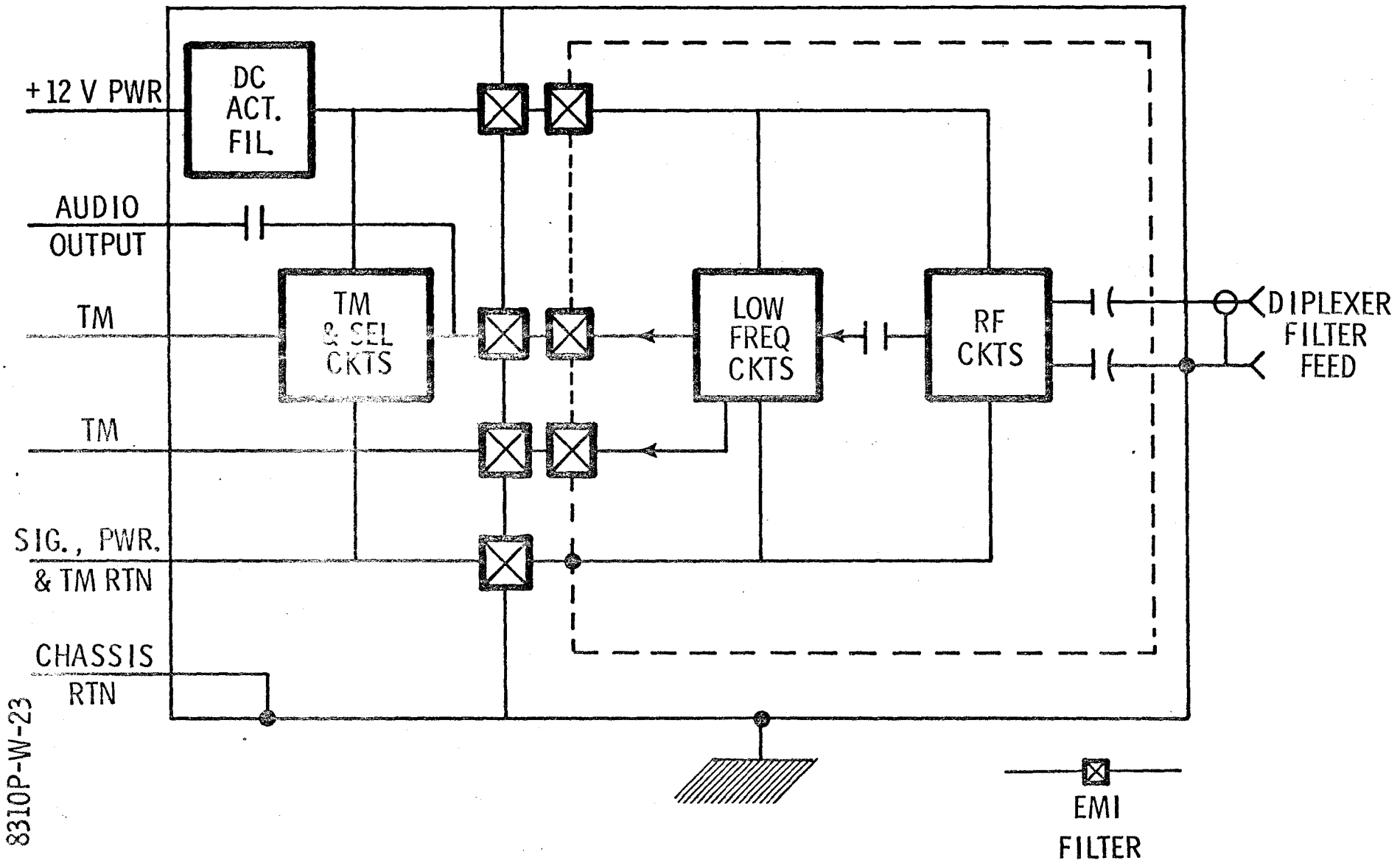

FIGURE 3

ALSEP ARRAY E DIPLEXER SWITCH & FILTER

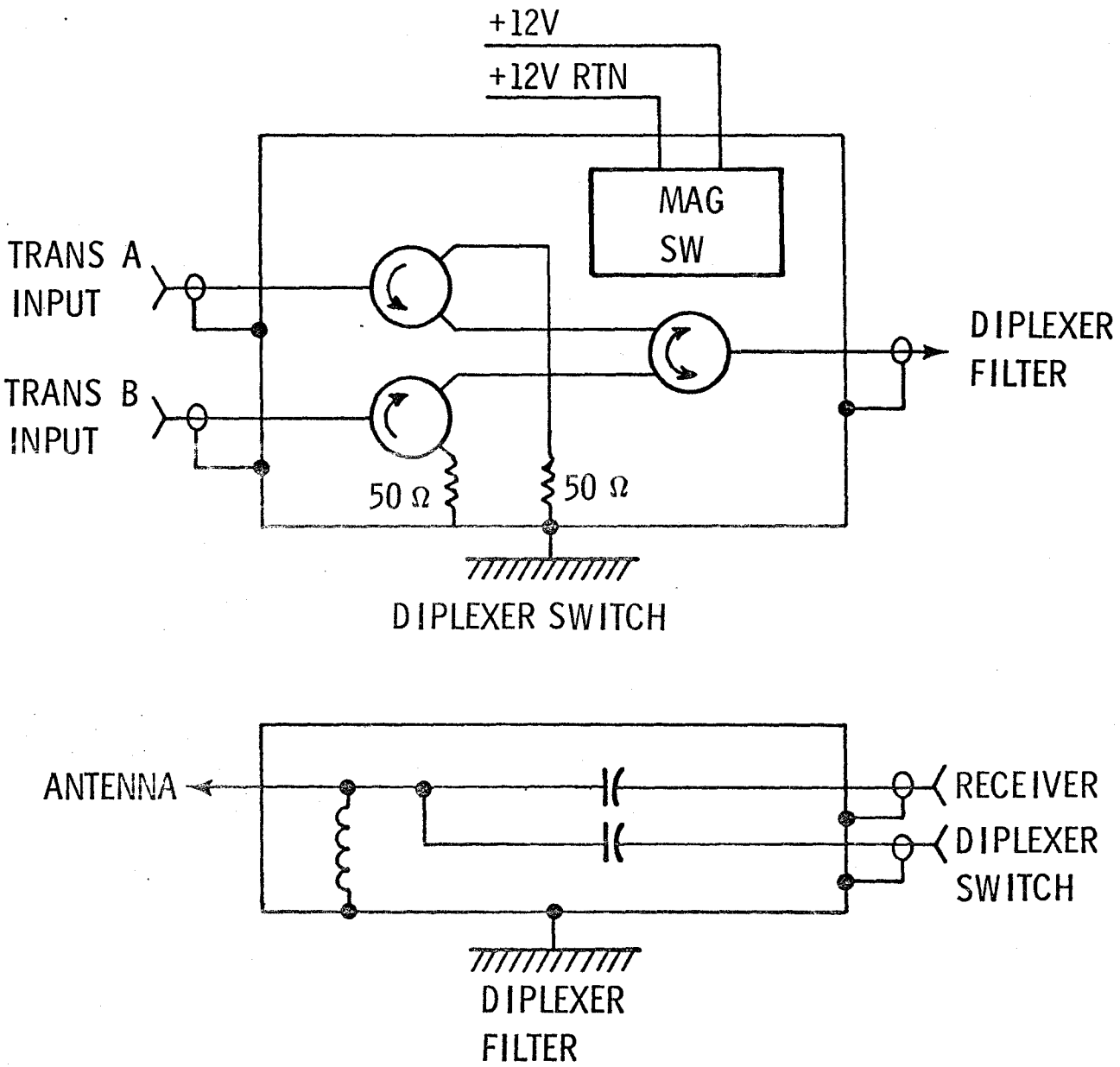

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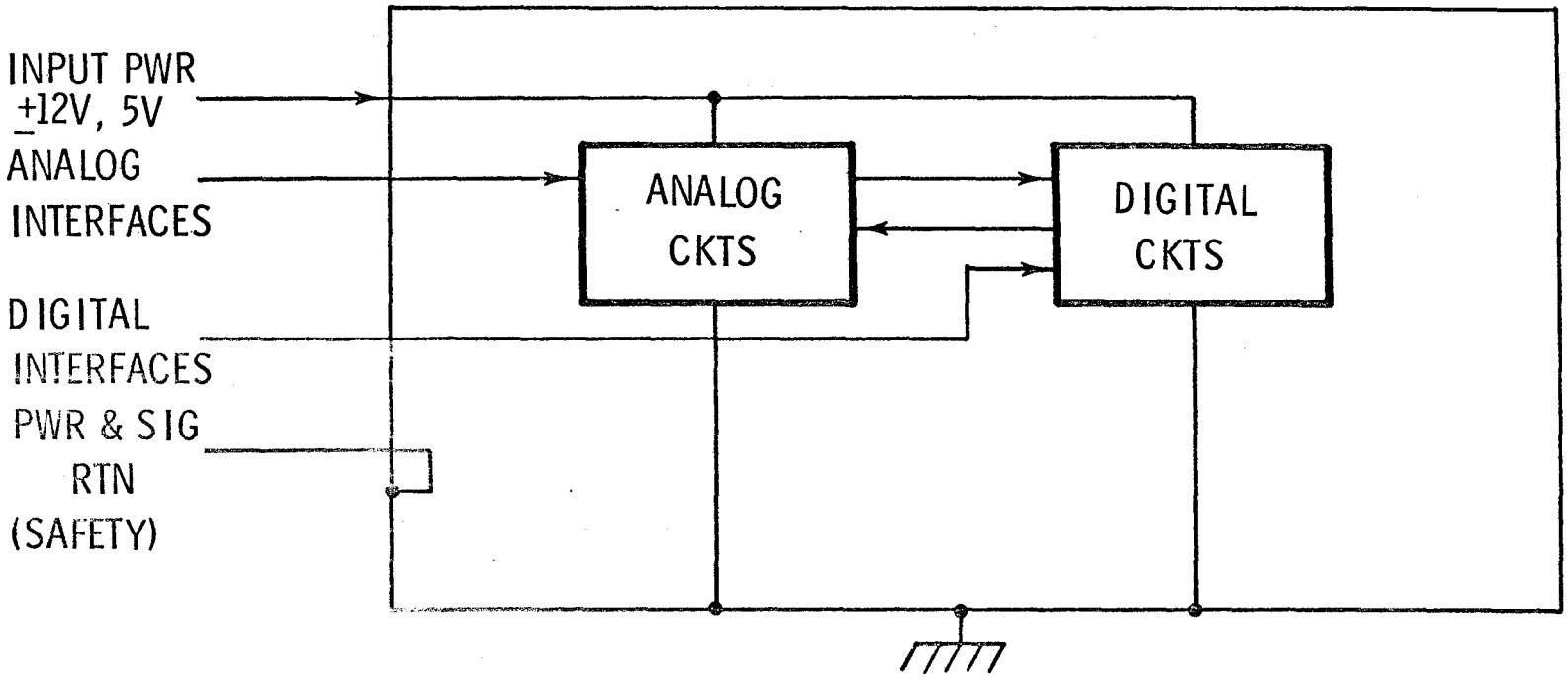
FIGURE 4



ALSEP ARRAY E COMMAND DECODER
& DATA PROCESSOR 8310P-W-22

FIGURE 5

ALSEP ARRAY E PCU/PDU

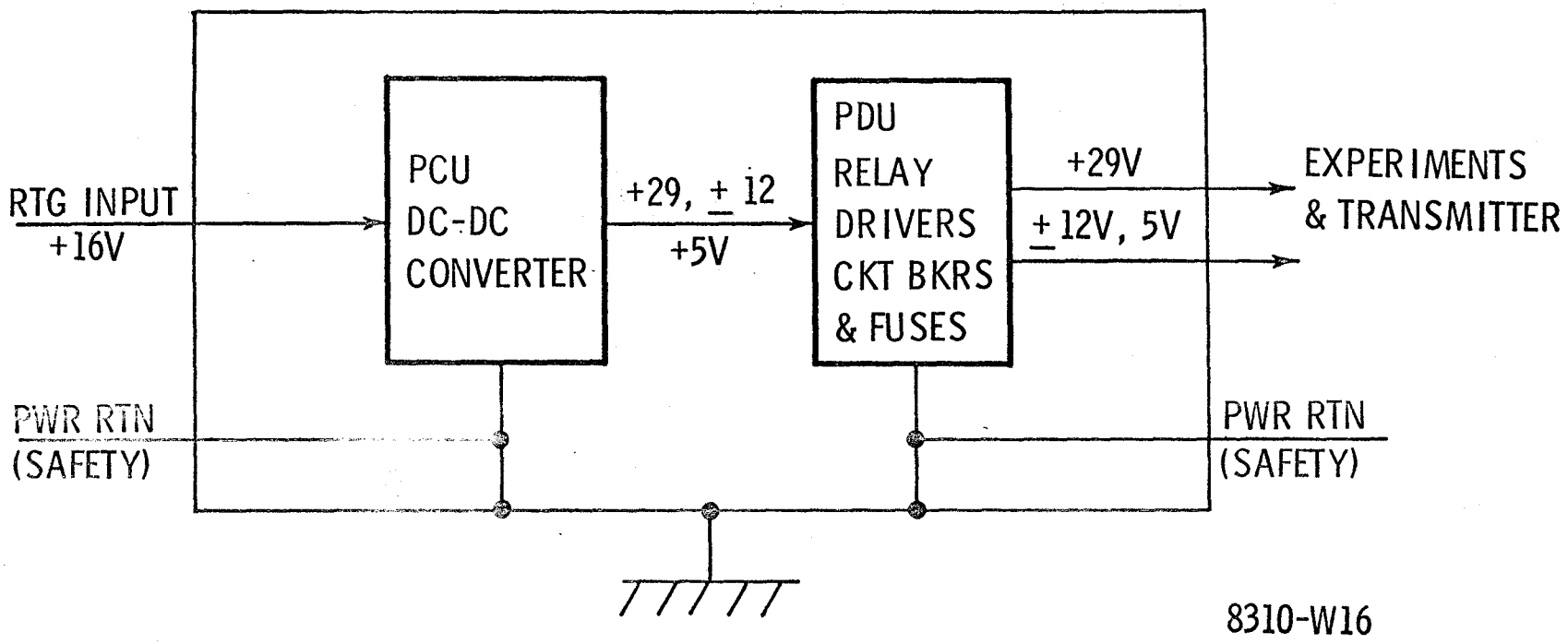


FIGURE 6

EXPERIMENT GROUNDING - TYPICAL FOR LMS, LSG, HFE AND PSE

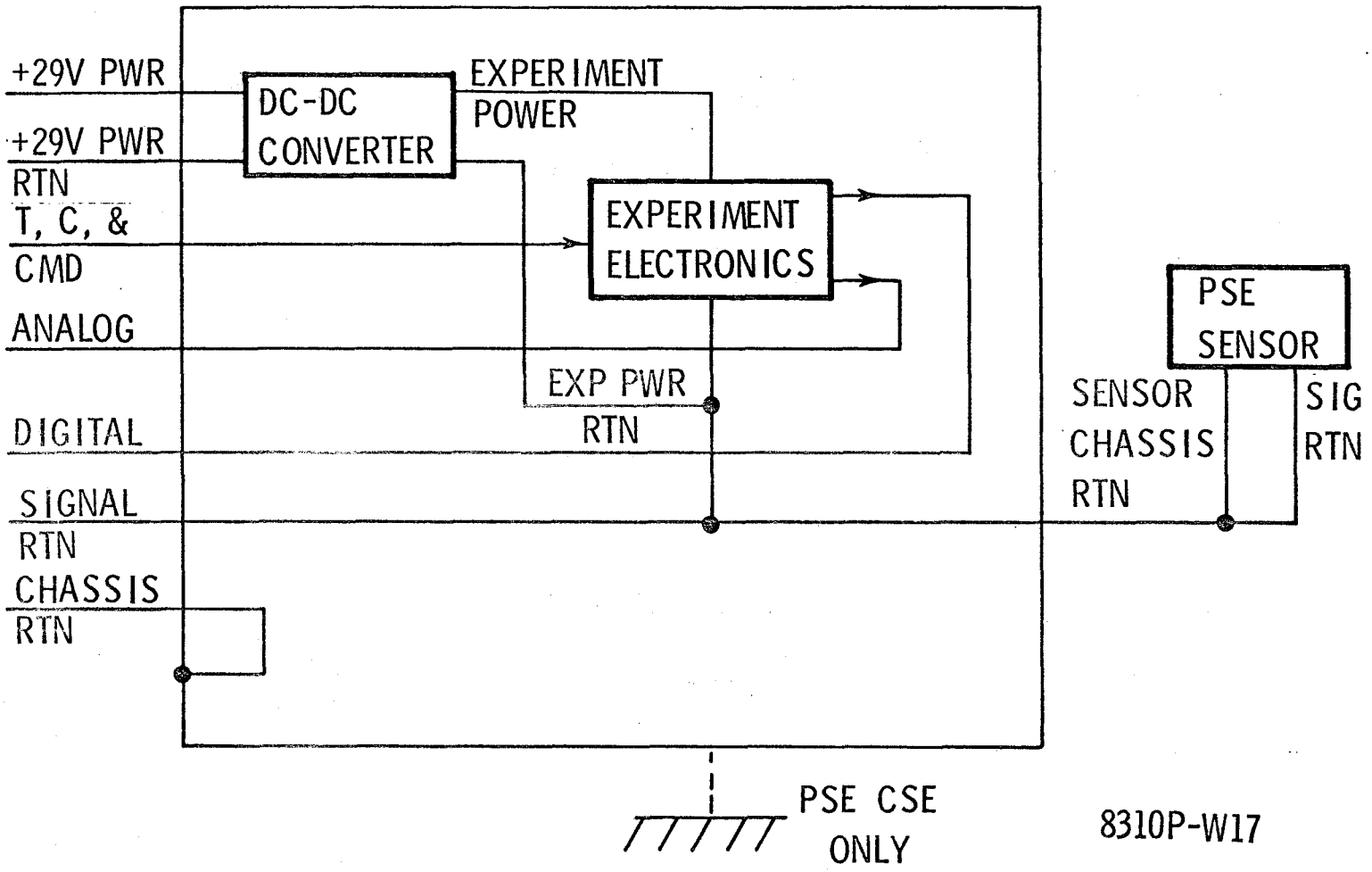


FIGURE 7

EXPERIMENT GROUNDING - LEAM

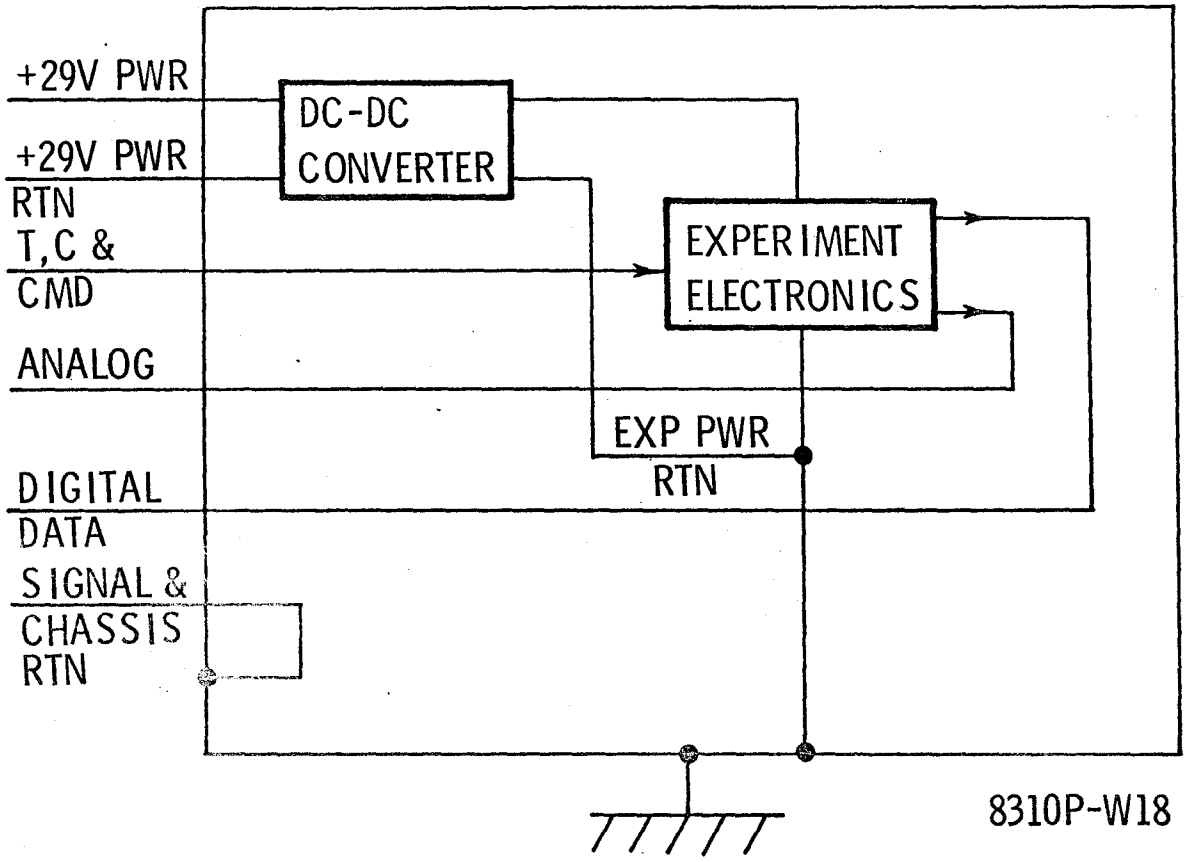


FIGURE 8

EXPERIMENT GROUNDING - LSPE

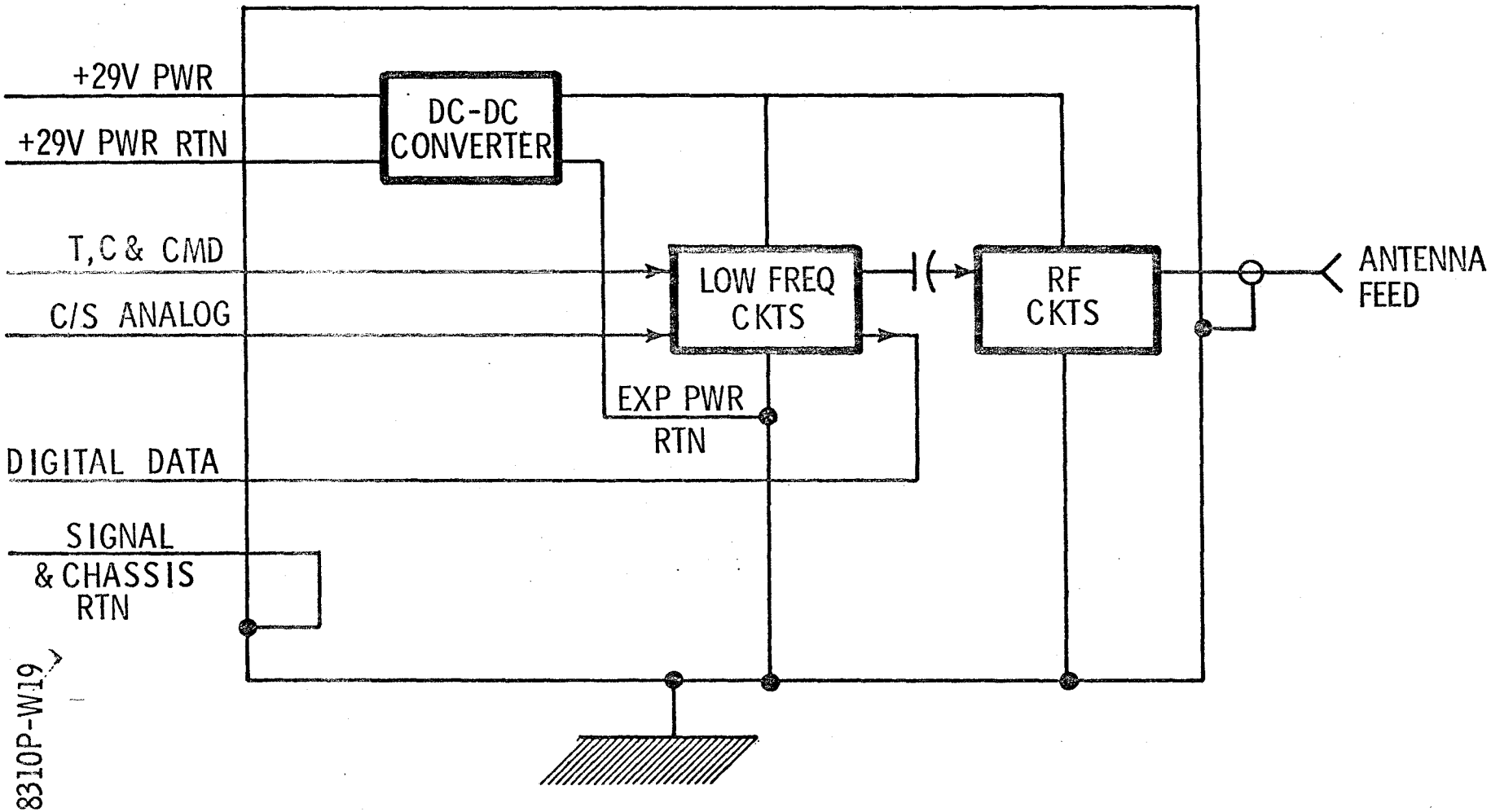


FIGURE 9

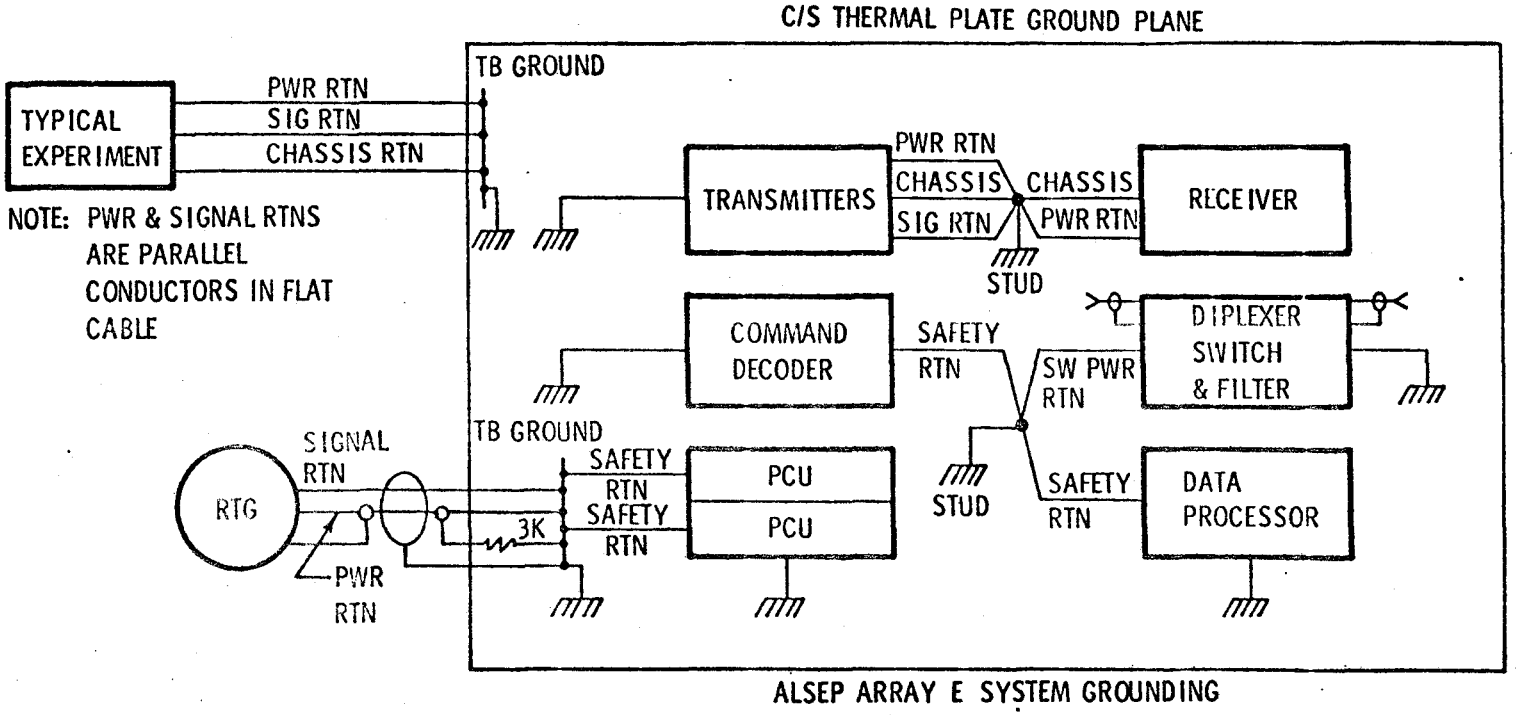

C/S THERMAL PLATE GROUND PLANE
TB GROUND
TYPICAL EXPERIMENT
PWR RTN
SIG RTN
CHASSIS RTN
NOTE: PWR & SIGNAL RTNS ARE PARALLEL CONDUCTORS IN FLAT CABLE
TRANSMITTERS
PWR RTN
CHASSIS
SIG RTN
CHASSIS
PWR RTN
RECEIVER
STUD
COMMAND DECODER
SAFETY RTN
SW PWR RTN
DIPLEXER SWITCH & FILTER
TB GROUND
SIGNAL RTN
RTG
3K
PWR RTN
SAFETY RTN
SAFETY RTN
PCU
PCU
STUD
SAFETY RTN
DATA PROCESSOR
ALSEP ARRAY E SYSTEM GROUNDING
8310P-W20

FIGURE 10

ALSEP ARRAY E EXPERIMENT GROUNDING

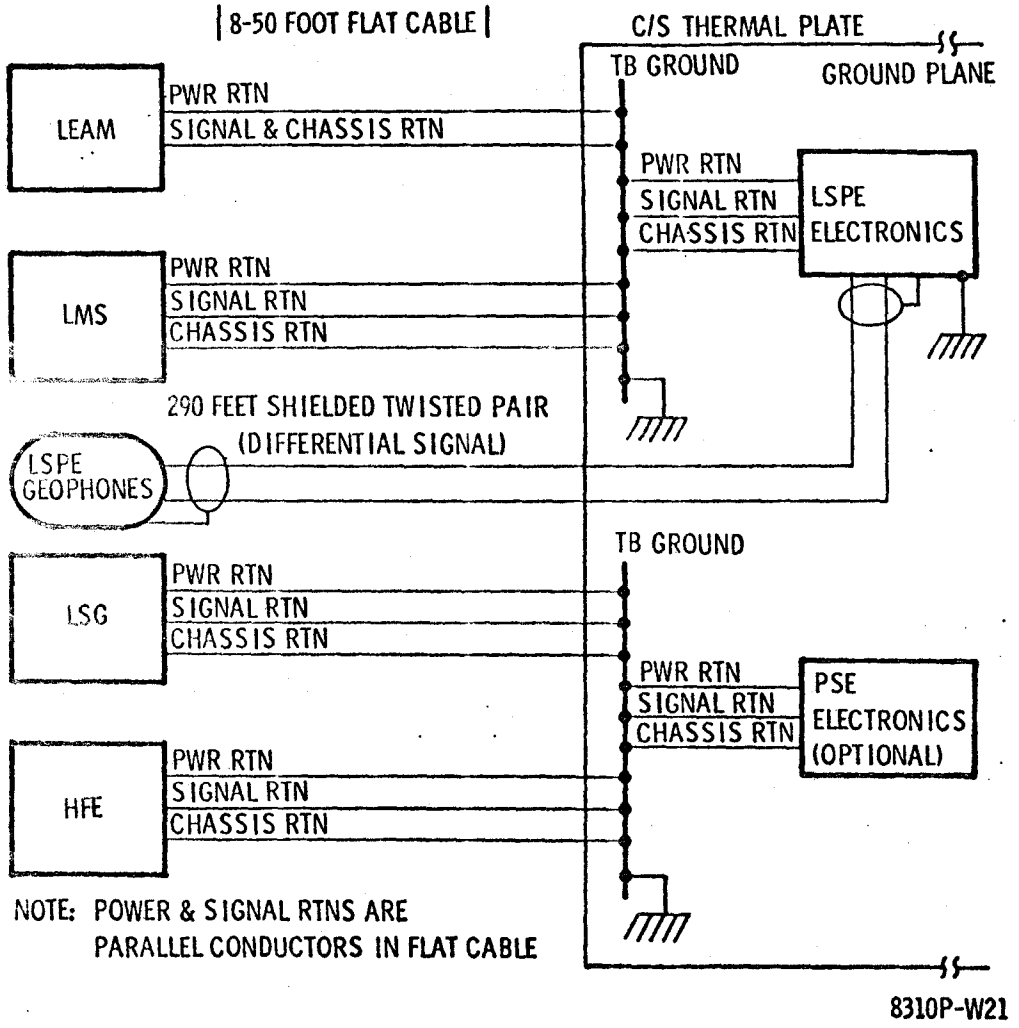


FIGURE 11