ARRAY E

ALSEP COMMAND DECODER

DATA DEMODULATOR ANALYSIS

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Summary

The analysis presented in this report was undertaken in response to Action Item 170.

This report presents the design equations used in the selection of part values, the theoretical performance for the specified uplink transmission, and the theoretical response of the command decoder with no uplink transmission.

The theoretical results for no uplink transmission are compared to measured data taken on the Design Verification Model, which was presented at the Critical Design Review.

The analysis of this model is lengthy, but the essential points can be summarized as follows.

The "EXCLUSIVE OR" logic following the bit detectors rejects the input if the receiver is saturated throughout a bit time. Because of the low-frequency character of the noise, this happens about 50% of the time. When the receiver does not remain saturated, the bit detector inputs are essentially uncorrelated, and the "EXCLUSIVE OR" rejects about 50% of these bits. There is roughly a 25% chance that the digital threshold signal will be maintained for one more bit, if at least one bit has been detected.

24 bits in succession are required for the Command Decoder control logic to go through its full cycle. Roughly 128 such 24 bit threshold signals are required before an address recognition and false CVW are generated. The probability of this event is very small compared to specification requirements.

This ATM, together with the breadboard test data reported in ATM-985, substantiates the preliminary considerations previously mentioned in the response to Action Item 18 revision E.

1. INTRODUCTION

This report details the analysis undertaken in the Data Demodulator design together with its theoretical performance with a noisy input signal.

The description of the unit testing is given in ATM-985.

The details of circuit operation are given in ATM-974.

The description that follows uses the nomenclature from the schematic 2367646. (Fig. 1)

2. VOLTAGE CONTROLLED OSCILLATOR

2.1 The VCO consists of three sections;

(a) The current source Q1A, Q1B which supplies a charging current to C13, which is a linear function of the input voltage on R_9.

(b) The U.J.T. oscillator Q2 whose period of oscillation is a function of the charging current into C13.

(c) The amplifier Q3, which acts as both an inverter and a translator to TTL logic levels.

2.2 Condition for oscillation of UJT Q2

(a) $$I_{EQ1B} > I_{P\ Max}$$

$$< I_{V\ Min}$$

From data sheets.

$$12\,\mu A < I_{EQ1B} < 8\ mA.$$

Make

$$I_{EQ1B} = 100\ \mu A.$$

(b) Choosing R_{15} for minimum change in frequency with temperature.

Motorola App. Note AN122 gives optimum resistance of:

$$R_{15} = 0.015 \cdot V_{CC} \cdot r_{BB} \cdot \eta$$

$$= 670\,\Omega$$

$\therefore$ We will choose,

$$R_{15} = 649\,\Omega.$$

(c) Choosing C_{13} for 8 kHz oscillation.

For constant current of 100 μA

$$C_{13} = \frac{125 \times 100}{\Delta V_E} \text{ pF}$$

$\Delta V_E \sim 6$ V

$\therefore$ $C_{13} = 2,080$ pF

Choose $C_{13} = 0.002\,\mu F$

(d) Choosing R_9 to give 100 μA constant current

$$I \sim \frac{V^+}{R_9} \qquad V^+ = 12 \text{ v}$$

$$R_9 = \frac{12 \text{ Ma}}{100} = 120 \text{ K } \Omega$$

Choose R_9 from a kit of 100 K to 255 K resistors to cope with parameter variations in UJT.

(e) Choosing R_{18} for logic sinking

Max logic '0' is 0.3 v

Total load is 2 low power TTL gates
$\therefore$ Total sink current = 360 μA

$$\therefore R_{18} \leq \frac{0.3}{0.36} \text{ K}\Omega = 830\,\Omega$$

$\therefore$ We will choose 649 $\Omega = R_{18}$.

3. SYNCHRONOUS DETECTOR (PSR) IN PHASE LOCK LOOP.

The input circuitry to AR3 (U1, and AR2, etc.) may be replaced by an equivalent circuit as shown.

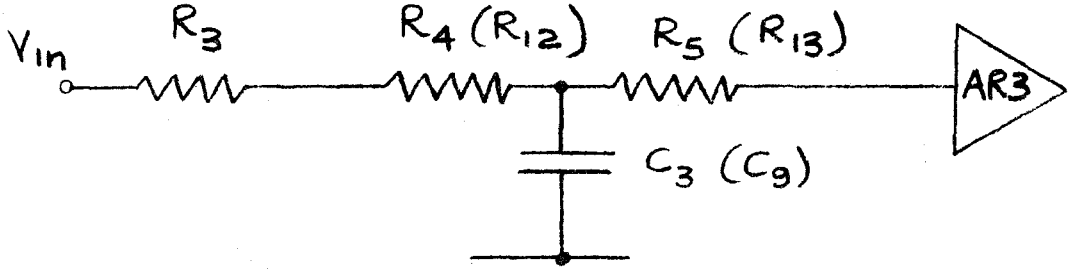


Figure 1 Phase-Lock Loop Input

Where V_{in} is the sum of two voltages the average value of which is given by:

$$V_{in} = \frac{V_{pp}}{2\pi} \sin\phi - \left\{ -\frac{V_{pp}}{2\pi} \sin\phi \right\}$$

$$= \frac{V_{pp}}{\pi} \sin\phi$$

For small angles $\frac{V_{pp}}{\pi}\ \phi = V_{in}$

Where V_{pp} is the peak to peak 1 kHz voltage appearing at the output of AR1 and ϕ is the phase shift from 90° between the input and switching signals.

$$\therefore \quad \frac{V_{in}}{V_{pp}\,\phi} = \frac{1}{\pi} = 0.32$$

4. PHASE LOCK LOOP

(a) We may represent the loop in block diagram form as

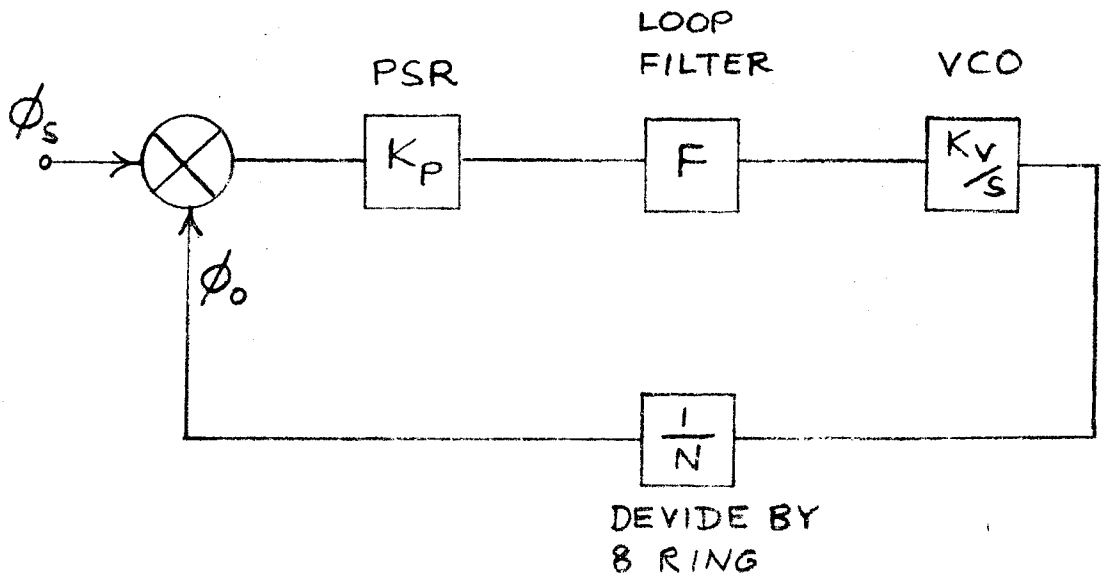


Figure 2 Phase-Lock Loop Block Diagram

Closed Loop T. F.

$$\frac{\phi_o}{\phi_s} = \frac{1}{1 + \frac{N}{K_p K_v F} \cdot s}$$

We will approximate the loop filter by its two main time constants T_A and T_B, i. e.,

$$F = K_A \left\{ \frac{1 + sT_A}{1 + sT_B} \right\}$$

This yields

$$\frac{\phi_o}{\phi_s} = \frac{1 + sT_A}{1 + s\left\{ T_A + \frac{N}{K_p K_v K_A} \right\} + s^2 \frac{NT_B}{K_p K_v K_A}}$$

i. e., a 2nd order loop where,

$$\omega_n = \frac{K_p K_v K_A}{NT_B} = \frac{G_0}{T_B}$$

$$\zeta = \frac{G_0 T_A^2}{4\, T_B}$$

Where G_0 is the open loop d. c. gain

(b) To ensure a static phase error of 2 degrees with a VCO frequency variation with temp of $\pm$ 60 Hz we must make G_0 = 12, 000 for minimum input signal.

(c) Similarly, to cope with the VCO variation worst case we will choose a capture range of 200 Hz.

Viberbi quotes a capture frequency range for a second order system with imperfect integrator as:

$$B_c = \frac{2\sqrt{3}\ G_0 T_A}{\pi\ T_B}$$

When $B_c = 200$ this yields,

$$\frac{T_B}{T_A} = \frac{1 \cdot 1 \times 12,000}{200} = 66$$

We will choose T_B to be as large as possible, say 1 sec.

Then $T_A = \frac{1}{66}$ secs or 15.2 ms.

$$\omega_n = \sqrt{\frac{12,000}{1}} = 110 \text{ rad/sec}$$

$$\zeta = \sqrt{\frac{12,000 \times 15.2^2}{4 \times 1}} = 0.83$$

(d) The noise bandwidth is given by

$$B_N = \omega_n \left\{ \frac{1 + 4\zeta^2}{8\zeta} \right\} = 62 \text{ Hz}$$

(e) The system lock range is given by

$$B_L = \frac{G_0}{2} = 6000 \text{ Hz}$$

NOTE: The capture range figures in Figure 1 of ATM 985 show fair agreement with theory. The theoretical lock range, however, does not agree; this effect is due to non linearities, particularly amplifier saturation.

(f) The loop filter is implemented with op amp AR3

$$\frac{V_o}{V_i} = \frac{R_6}{R_3 + R_4 + R_5} \cdot \frac{(1 + s R_7 C)}{\left[s^2 C_4 C_5 R_6 R_7 + s(R_6 C_4 + R_7 C_5 + R_6 C_5) + 1 \right]}.$$

i.e. of the form

$$\frac{K_A (1 + sT_A)}{(1 + sT_B)(1 + sT_C)}$$

Where

$$T_A = R_7 C_5$$

$$T_B T_C = C_4 C_5 R_6 R_7$$

$$T_B + T_C = R_6 C_4 + R_7 C_5 + R_6 C_5$$

Assuming

$$T_B > T_A > T_C; \quad R_6 > R_7; \quad C_5 > C_4$$

Then

$$T_B \sim R_6 C_5; \quad T_C \sim R_7 C_4$$

Now $T_B = 1$ sec and making $R_6 = 1M$

Yields $C_5 = \frac{T_B}{1} = 1 \mu F$

Also $T_A = 15.2$ mS

$\therefore R_7 = \frac{15.2 K}{1}$.

We will choose $R_7 = 15.8\ K\Omega$.

Let $T_C = .1ms$

Then $C_4 = \frac{.1}{15.8}\ \mu F = .0063\mu F$

We will choose $C_4 = .0068\mu F$

(g) We may now obtain K_A from the loop gain G_0 since

$$G_0 = \frac{K_P K_V K_A}{N} = 12,000$$

Now $\frac{K_V}{N}$ the VCO gain at 1 KHz was measured at 80 Hz/volt.

or 500 rad/sec/volt
(See Fig. 3 of ATM-985)

Also $K_P = \frac{V_{PP}}{\pi}$ volts/radian $= 0.32\ V_{PP}$

For an input amplifier gain of 1.3 and a minimum input signal of 2 volts peak to peak (at 1 KHz)

$$K_P = 1.3 \times 2 \times .32 = .83$$

$$K_A = \frac{G_0}{K_P \frac{K_V}{N}} = \frac{12000}{.83 \times 500} = 28$$

Let $K_A = 25$

Now $K_A = \frac{R_6}{R_3 + R_4 + R_5}$

$$R_3 + R_4 + R_5 = \frac{1M\Omega}{25} = 40\ K\Omega$$

for $R_3 + R_4 = R_5$

R_3 & R_4 = 10KΩ

& R_5 = 20KΩ

(h) The input time constant

$$T_D = \frac{(R_3 + R_4)R_5}{R_3 + R_4 + R_5} \quad C_3$$

T_D is chosen to be as small as possible since it affects the phase shift between the 1 and 2 KHz signals. It is therefore chosen to match the phase shift in the 2KHz data loop (measured at ~ 2μs). It also removes the output ringing of the switch U1.

C_3 is fixed at 470 pF.

(i) A further time constant is needed to improve the noise bandwidth. The break frequency of this is chosen to be about 300 Hz. This network is included between AR3 output and R_9.

Now for 300 Hz break point

$$T_E = \frac{1}{2\pi \times 300} = 0.53 \text{ mS}$$

Make $R_{38} >> R_9$, choose R_{38} = 1KΩ

$$\therefore \quad C_{32} = \frac{0.53}{1} \ \mu F$$

Choose C_{32} = 0.47 μF

5. INPUT AMPLIFIER

The input amp is designed to buffer the receiver signals. The receiver requires a load of at least 22K. In this case, R1 was chosen at 33.2K and C1 was chosen to give a roll off at very low frequency in order to minimize

phase shifts between 1 and 2 KHz signals. The receiver already has a series cap of 1μF. Therefore, C1 was chosen also to be 1μF. The input amplifier T.F is given by,

$$\frac{V_o}{V_i} = \frac{R_2 sC}{1 + R_1 sC} \quad \text{where } \frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_{RX}}$$

The lower break frequency is given by,

$$R_1 C = \frac{1}{2\pi f} \; ; \quad f = \frac{1}{2\pi \times 33.2 \times .5}$$

$$f = 9.5 \text{ Hz}$$

The gain at higher frequencies is given approximately by,

$$\frac{R_2}{R_1}$$

This gain is chosen to give a voltage swing of 8 volts peak to peak for maximum input signal of 6 volts peak to peak.

$$\frac{R_2}{R_1} = \frac{8}{6}$$

$$R_2 = \frac{4}{3} \times 33.2K = 44K \sim 42.2K.$$

The output swing is also clamped at about 8.5 volt peak to peak. This ensures correct switching at U1 and U9.

6. DATA DEMODULATOR

The data demodulator circuit may be functionally represented as:

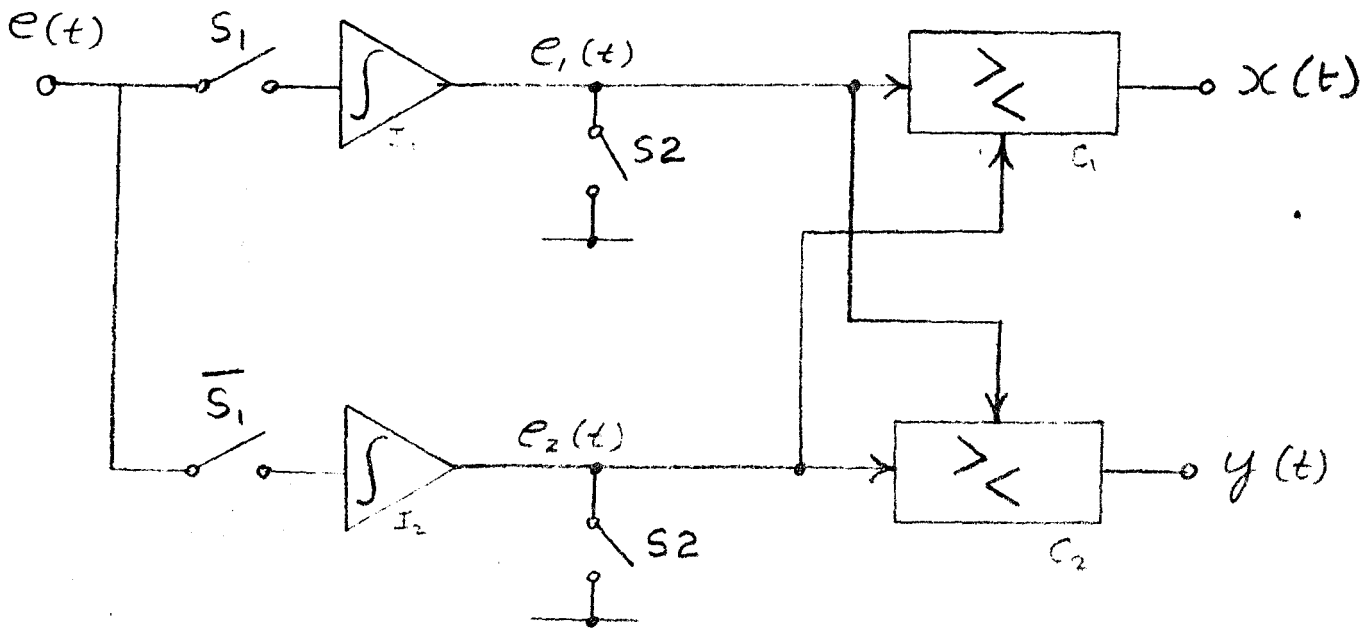


Figure 3 Data Demodulator Block Diagram

Where e(t) is the baseband data input; S_1 and $\overline{S}_1$ are the complementary switches, driven at 2 kHz; I_1 and I_2 are integrators; S_2 are the dump switches, driven at the 1 kHz bit rate; and C_1 and C_2 are redundant comparators which output the data in complementary NRZ form.

The switches S_1 and $\overline{S}_1$ are contained in U9; S2 switches are in U10; and the comparators are AR4 and AR5. The integrators are approximated by single time constant passive networks with a near optimal time constant of 1ms, to produce a data bandwidth of 500 Hz, centered at about 2kHz. The integrator time constants are given by

$$T_1 = (R_{20} + R_{21})\, C_{25}$$

$$T_2 = (R_{20} + R_{24})\, C_{26}$$

If C_{25} & C_{26} are 0.01μF

$$(R_{20} + R_{24}) = (R_{20} + R_{21}) = \frac{T_1}{.01} \quad K$$

$$= 100\ K$$

Therefore, let $R_{20} = R_{24} = R_{21} = 49.9K$ say.

It is assumed that resistors R_{22}, R_{25}, R_{26}, R_{27} and R_{30} are large enough to be neglected, i.e., about an order larger at 511K. These resistors are included to produce a threshold bias on the comparators. This bias is fixed by the resistor chain across the +5v line of R28 and R29 and is set at 0.5v.

7.0 STATISTICAL ANALYSIS OF SIGNAL DETECTION

Details of calculations are given in the appendices attached. The equivalent circuit for the bit detector is given in Figure 4.

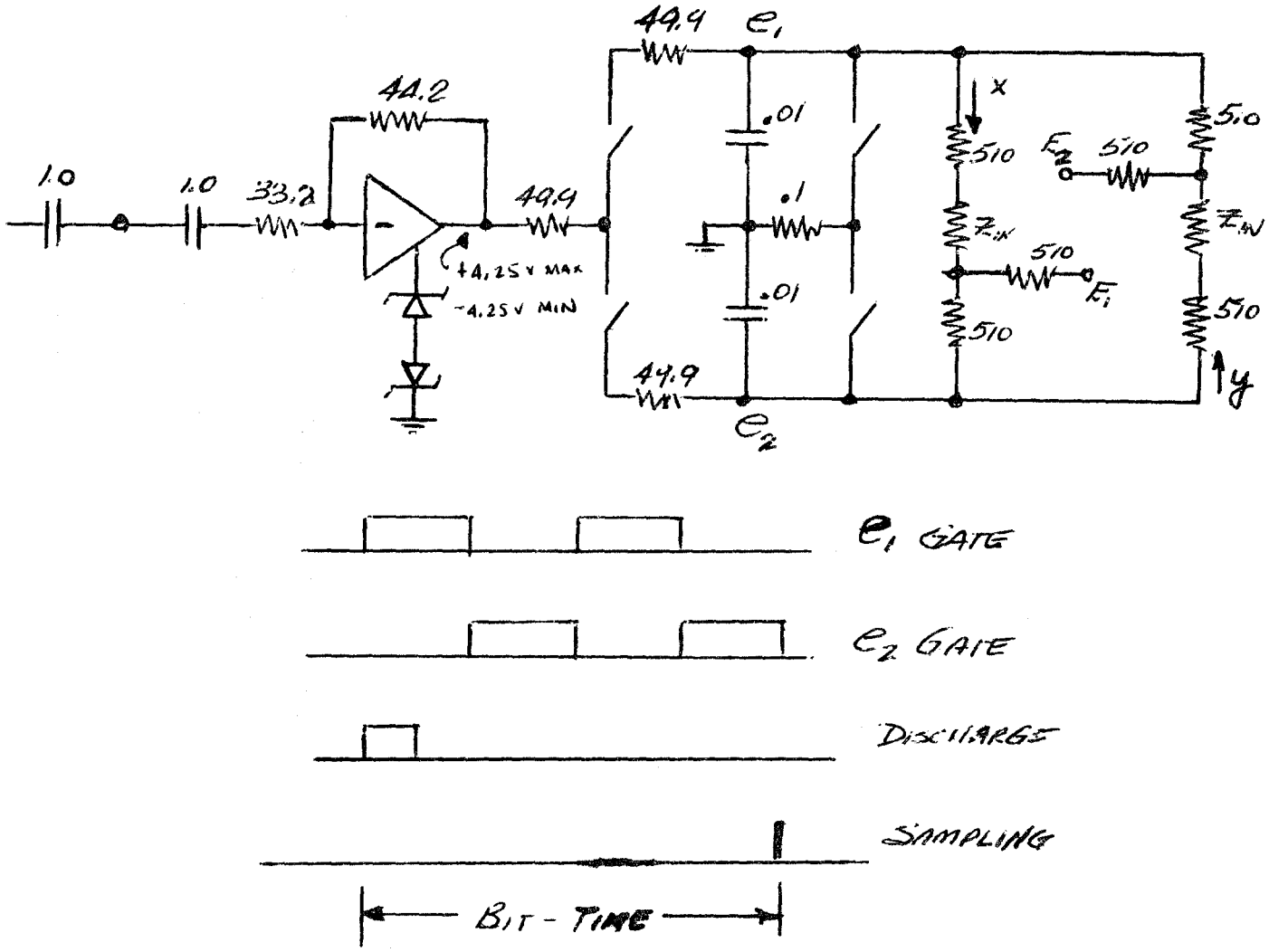
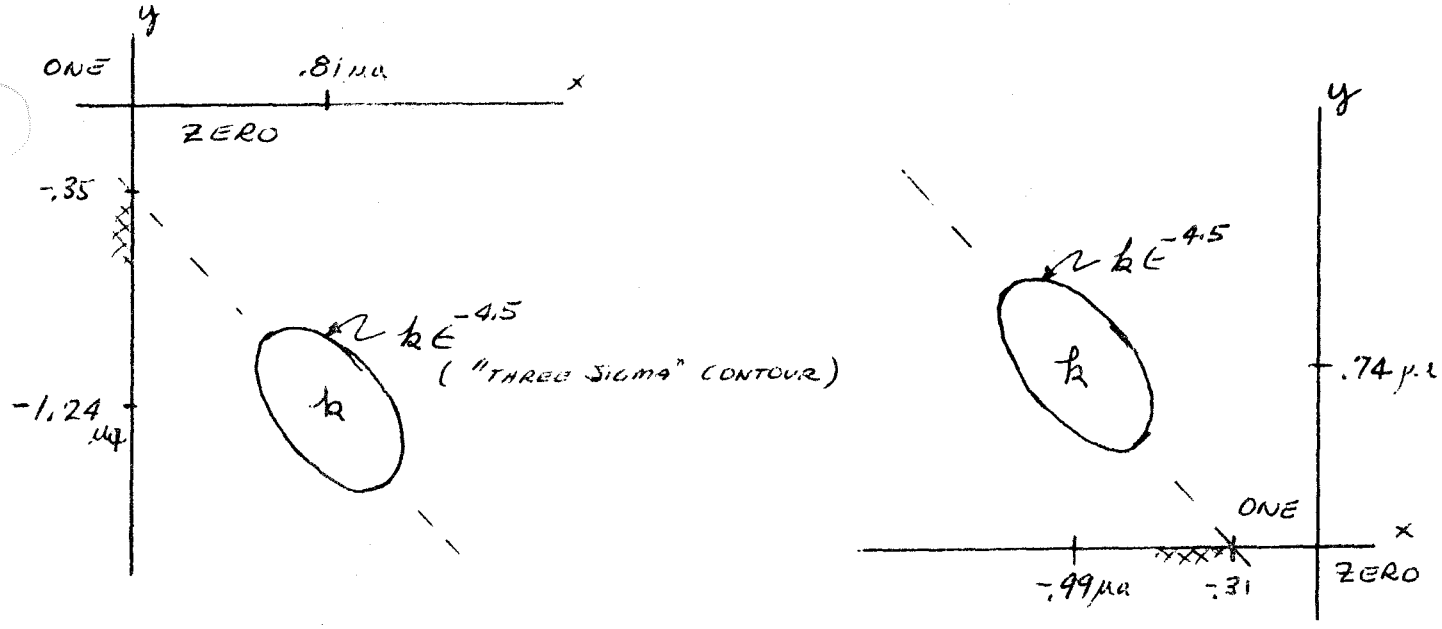


FIGURE 4 - Bit Detector Circuitry
(Microfarads and kilo-ohms)

If the current labeled x is greater than zero at the sampling instant, then a ZERO is detected. If the current labeled y is positive at the sampling instant, a ONE is detected. If both are detected, that particular bit is erased and the threshold drops out.

Figure 5 shows the probability density function for x and y for the minimum specified signal (3.8 volts peak-to-peak) at the minimum signal to noise ratio of 17 dB. The correlation coefficient between noise in x and noise in y is calculated to be -.78. The ellipse centered at $\bar{x}$, $\bar{y}$ is a "3 sigma" contour of constant probability density. The crosshatched areas on the third quadrant represent the probability that both x and y are negative. If both x and y should ever be positive, the signal is rejected by the exclusive or circuitry which follows the bit detectors. The RMS noise current in x is calculated to be .053 microamperes. The RMS noise current in y is calcluated to be .058 microamperes. The noise distributions are jointly Gaussian and the probability of not accepting the minimum signal is very small, exceeding requirements on noise permitted by more than 12 dB, and exceeding system requirements on signal power required by more than 6 dB.



5a. ZERO transmitted 5b. ONE transmitted

FIGURE 5 - Probability densities with Signal Transmitted

8.0 STATISTICAL ANALYSIS OF NOISE REJECTION

With no uplink transmission, the command receiver output is at one of its saturation levels most of the time. Figure 7 shows 900 milliseconds of typical operation. The probability density function for the bit detector input current now becomes multimodal, as is indicated in Figure 6.

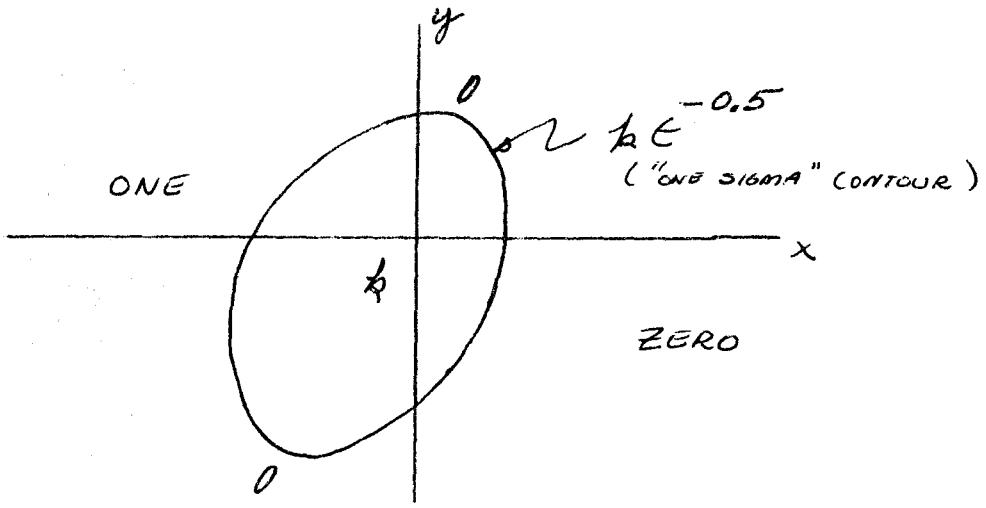
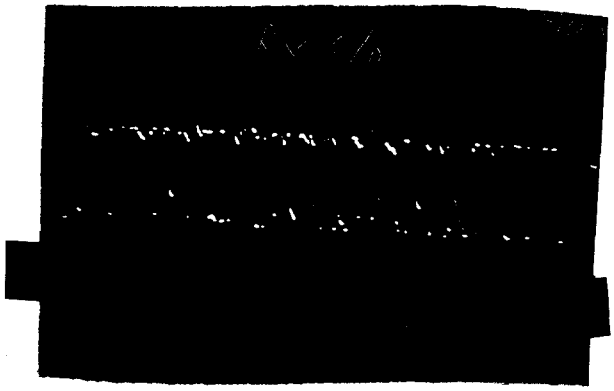


FIGURE 6 - Probability Density of Comparator Currents with No Signal

If the buffer amplifier output remains positive throughout the bit time, both x and y currents tend to be positive. This condition results in a large peak in the first quadrant. If the buffer amplifier output remains negative throughout the bit time the large peak at the lower left results. The remaining possibility is that a transition occurs during a bit time, which results in the peak in the middle.

It is shown in the appendices that if there is no transition in the receiver output during a bit time the exclusive or circuit will recognize the input as noise. The threshold signal will become false as a result, resetting the command decoder control logic.

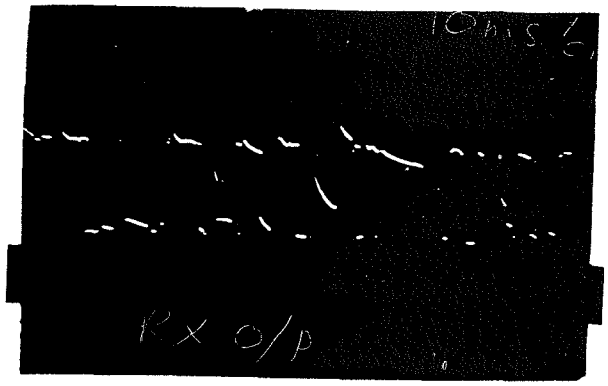
If there are one or more transitions from saturation to saturation, the probability of interpreting noise as a ZERO is 0.251. The probability of interpreting noise as a ONE is 0.272.



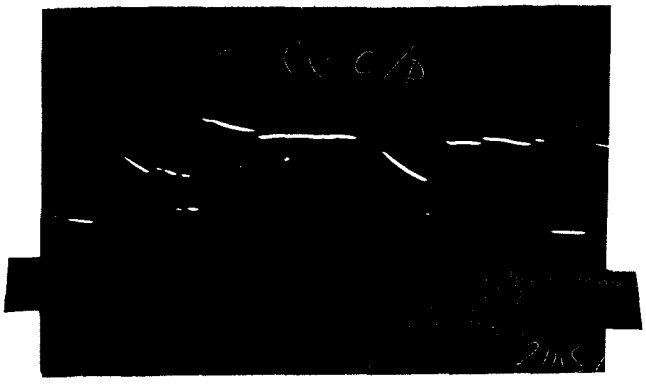
50 ms/cm

50 ms/cm

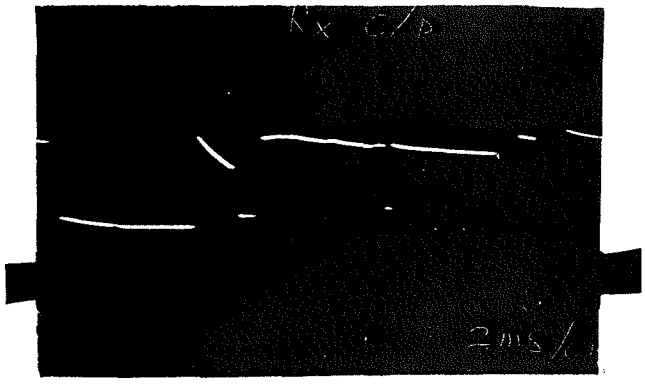
20 ms/cm



10 ms/cm



2 ms/cm



2 ms/cm

Figure 7 Command Receiver Output, No Signal

With no knowledge of the previous receiver output, the probability of one or more zero crossings is 0.33. The probability of a false detection is 0.33 (0.272 + 0.251) = 0.17.

If a bit is detected, it is concluded that the receiver phase detector output is close to zero during the following millisecond. The probability of one or more zero crossings increases to 0.43. The probability of a false detection increases to 0.43 (0.272 + 0.251) = 0.23.

In an observation time T milliseconds in duration, the number of false detections which are K bits in duration is

$$N = \left[P(B/A)\right]^{K-1} P(A) \quad T$$

If we plot N versus K on semilogarithmic paper

$$M = \log N = (K-1) \log P(B/A) + \log P(A) + \log T$$

By differentiating M with respect to K, we see that the slope of the curve is a constant equal to log P(B/A). In these expressions P(A) is the probability of a false detection, with no prior knowledge of the receiver output, P(B/A) is the probability of a false detection if the previous bit was detected.

Figure 8 shows theoretical curves as solid lines with measured data shown as circles. The slope for the measured data is

$$\log P(B/A) = -0.603$$

$$\text{or } P(B/A) = 0.250$$

The first three false detections are removed from the threshold signal output of the data demodulator by a four bit shift register and coincidence gate. The coincidence gate generates the threshold signal. The discrepancy between theory and measurement is due to the fact that the theoretical model was developed for a receiver which has only two output levels. The measurements were made with the DVM receiver, which has a significant amount of diagonal clipping for negative saturation, reducing the weighting of the peak in the first quadrant.

The theory developed does indicate that the measured values of P (B/A) will not increase for longer threshold measurements, and that the curve can therefore be extrapolated. A 21 bit threshold is required for the generation of the "command verification enable" signal and the probability of this event is very small. An address recognition is also required. Extrapolating the measured data, the time interval between false CVW's, due to this noise source, exceeds specification requirements by a substantial margin.

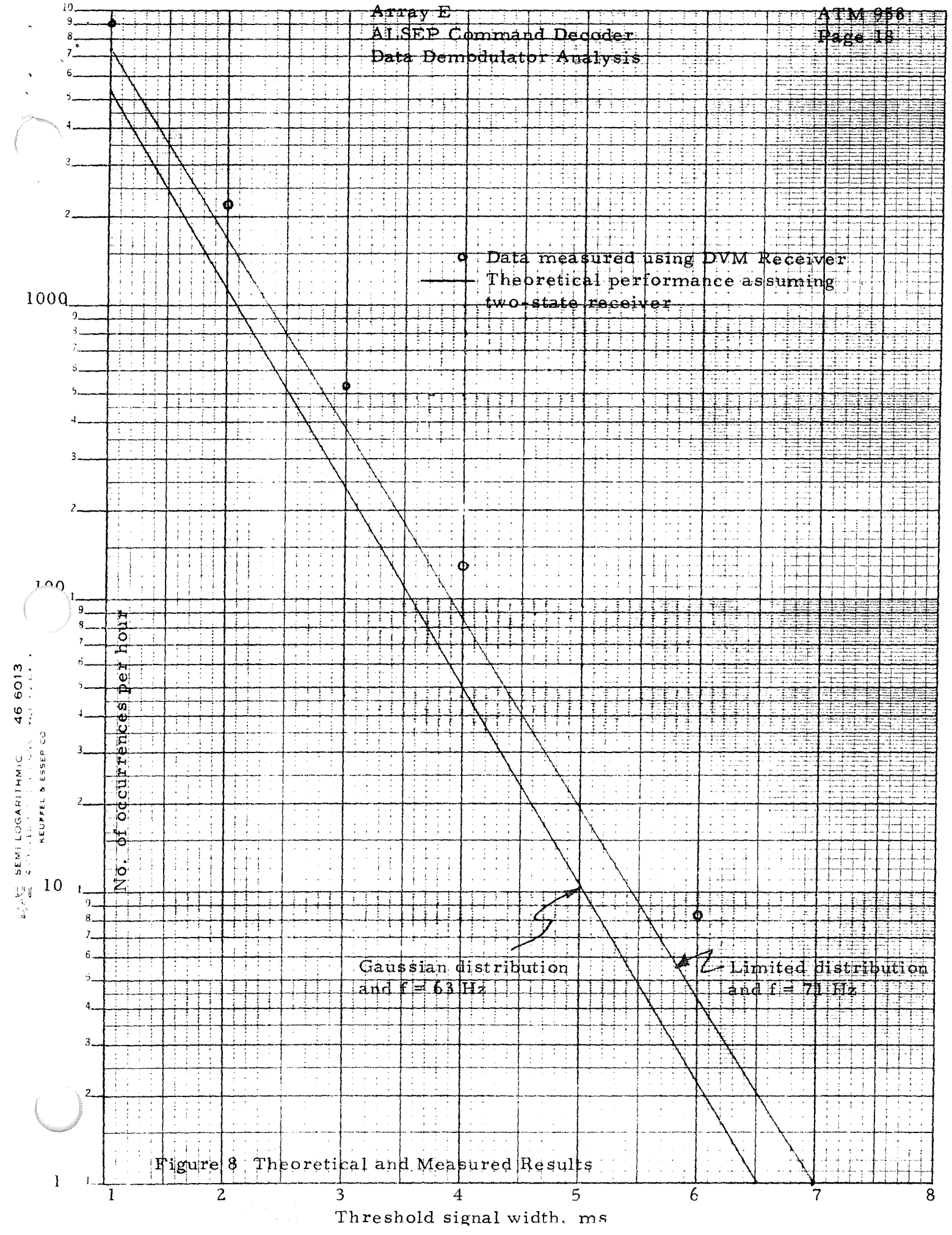


Figure 8 Theoretical and Measured Results

APPENDIX A

Receiver output statistics, signal present

With signal greater than noise in the IF amplifier, the component of noise which is orthogonal to the signal produces a phase modulation of the total waveform. With the signal, $S \cos (W_{IF} t + W_S t)$, W_S requires one millisecond to go through its range. The noise waveform has a bandwidth equal to the IF bandwidth. We can choose a time segment small compared to one millisecond, so that $W_{IF} + W_S$ can be considered a constant, and larger than the reciprocal of the IF bandwidth, so that noise samples from adjacent segments are uncorrelated. The noise voltage in each segment can be decomposed into orthogonal components.

$$\text{IF voltage} = S \cos wt + N_c(t) \cos wt + N_s(t) \sin wt$$

$$\text{IF voltage} = A \cos (wt + \phi(t))$$

For large signal to noise ratio

$$A \simeq S$$

$$\phi(t) = \tan^{-1} \frac{N_s(t)}{S} \simeq \frac{N_s(t)}{S}$$

The frequency discriminator responds to the time derivative of phase modulation, and the integration (low pass filter) recovers the phase modulation. The noise output of the receiver with signal present has a bandwidth equal to 1/2 the IF bandwidth, and is band limited in the audio stages. The phase-lock loop accepts noise in a narrow band of frequencies centered on 1000 Hz and the bit detector accepts noise in a narrow band centered on 2000 Hz. The significant parameter is the noise power spectral density at these frequencies. The command decoder performance is specified for a SNR of +17 dB or more measured in a 10 KHz bandwidth. The signal power specified is described by a range of voltage from 3.8 volts p-p to 6.2 volts peak-to-peak. Assuming that the signal power in the 1000 Hz subcarrier equals the signal power in 2000 Hz subcarrier sidebands, and that the 2000 Hz subcarrier is bi-phase modulated with a random bit stream, the receiver output statistics (signal present) can be defined by the spectrum shown in Figure 9. As in conventional, power levels are referenced to one ohm.

APPENDIX A (CONT)

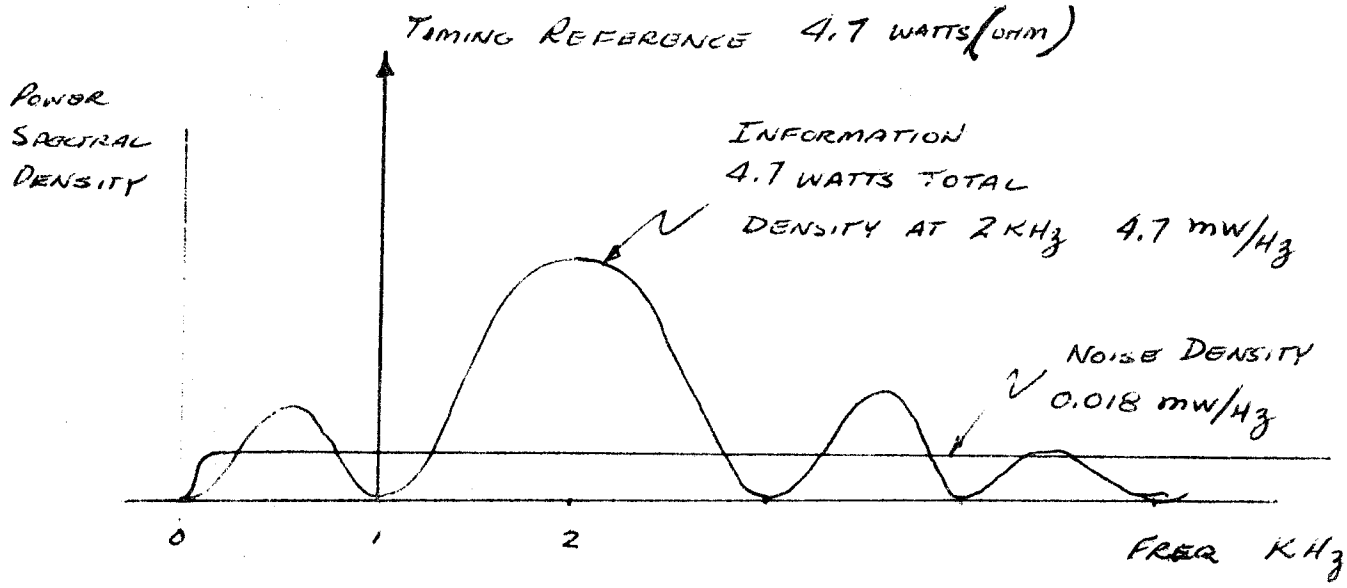


FIGURE 9 - Receiver Output Spectrum, Signal Present

APPENDIX B

Statistics of bit detector currents, with signal

In calculating these currents, the circuit of Figure 4 was approximated by replacing the RC charging circuits with integrators and ignoring the input capacitor. The performance exceeds requirement by a large margin and more precise calculations are not warranted.

With a ZERO transmitted, composite signal 3.8 volts p-p at the input, the integral under the e_1 gate less the discharge gate yields +0.82 volts for e_1 at the sampling instant. The integral under the e_2 gate yields −0.92 volts for e_2 at the sampling instant. With a ONE transmitted e_1 becomes −0.55 volts at the sampling instant and e_2 becomes +0.92 volts. The lack of symmetry here arises because the width of the disc.arge gate is significant.

An RC circuit with a time constant of one millisecond has an integrated noise bandwidth (one-sided) of 250 Hz. The noise power at e_2 is calculated to be $.018 \times 10^{-3} \times 250 = .0045$ watts (referred to one ohm). The noise voltage at e_2 is therefore 0.067 volts RMS. The noise power reaches its steady state value (approximately) in 1/2 time constant. The noise power at e_1 reaches 3/4 of its steady state value approximately, resulting in an RMS voltage of 0.058 volts. The noise at e_1 is not correlated with the noise at e_2 since they are samples 1/4 millisecond apart from a source whose bandwidth is greater than 10 KHz.

Circuit analysis of Figure 4 yields the following expressions for the input currents of the bit detectors.

$$x = \frac{2e_1 - e_2 - E_1}{3R + 2Z_{in}} \text{ for the ZERO detector}$$

and

$$y = \frac{2e_2 - e_1 - E_2}{3R + 2Z_{in}} \text{ for the ONE detector}$$

APPENDIX B (CONT)

From the specification for the operational amplifiers $Z_{in} \geq R$. The exact value affects the scaling on the current axes but does not affect the volumes under the probability density surfaces. The maximum bias current is 300 nanoamperes and the maximum offset current is 100 nanoamperes. The capacitors are dumped once each millisecond. The voltages which result from the amplifier currents can be lumped with tolerance variations in E_1 and E_2 and neglected. Z_{in} can be set equal to R. Differences in comparator recovery time are small enough to be neglected.

The average values for x and y which result are:

For a ZERO transmitted

$$\bar{x} = \frac{2(.82) - (-.92) - (.5)}{2.55} = +0.81$$

$$\bar{y} = \frac{2(-.92) - (.82) - (.5)}{2.55} = -1.24 \text{ microamperes}$$

For a ONE transmitted

$$\bar{x} = \frac{2(-.55) - (.92) - (.5)}{2.55} = -0.99 \text{ microamperes}$$

$$\bar{y} = \frac{2(.92) - (-.55) - (.5)}{2.55} = +0.74 \text{ microamperes}$$

The RMS noise currents are:

$$\sigma_x = \frac{(4(.058)^2 + (.067)^2)^{1/2}}{2.55} = 0.053 \text{ microamperes}$$

$$\sigma_y = \frac{(4(.067)^2 + (.058)^2)^{1/2}}{2.55} = 0.058 \text{ microamperes}$$

x and y are correlated, although e_1 and e_2 are not.

APPENDIX B (CONT)

Taking central moments,

$$\rho_{xy} = \frac{E\left\{(x-\bar{x})(y-\bar{y})\right\}}{\sigma_x \sigma_y}$$

Let v_1, v_2 be the noise components of e_1 e_2.

$$E\left\{(2v_1 - v_2)(2v_2 - v_1)\right\} = \overline{5v_1v_2} - \overline{2v_2^2} - \overline{2v_1^2}$$

$$\rho_{xy} = \frac{-2(.058)^2 - 2(.067)^2}{(2.55)^2 (.05)(.058)} = -0.78$$

With a ZERO transmitted, the probability of $x<0$ is much greater than the probability of $y>0$. $P(x<0)$ depends only on $\bar{x}$ and σ_x. $x = 0$ is at the 15 σ_x level. The probability of erasing a ZERO bit, $P(x<0) = .001$ occurs at 3.09 σ_x. Holding signal voltage and threshold constant, noise could be increased by 14 db before this will occur, for the assumptions made in this analysis.

With a ONE transmitted, the probability of $y<0$ is much greater than the probability of $x>0$. $P(y<0)$ depends only on σ_y and $\bar{y}$. $y = 0$ is at the 12.7 σ_y level. Holding signal voltage and threshold constant, noise could be increased by 12.5 db before the probability of a ONE bit being erased reaches .001.

The wide discharge pulse costs 1.5 db of excess performance, but it is easier to mechanize and more reliable than a narrow discharge pulse.

It should be noted that if the SNR is degraded by reducing the signal power by 6 db, the noise power output increases by 6 db approximately, since the phase modulation by noise is inversely proportional to IF signal voltage. The system as a whole has a 6 db margin over the specified performance.

APPENDIX C

Receiver output statistics, no signal

A total of 900 milliseconds of time samples is shown in Figure 7. The statistics of this waveform will be approximated for this analysis by assuming a probability density function which consists of two equal delta functions, one at +5 volts and one at -5 volts, and assuming that the autocorrelation of the output is

$$25\left(\frac{2}{\pi}\right) \text{arcsine } (\exp(-.425T)).$$

Assume that the frequency discriminator consists of two tuned circuits with differentially connected envelope detectors generating the output. One of the tuned circuits responds to frequencies from W_1 to W_2, and the other responds to frequencies from W_2 to W_3, with the IF bandpass being from W_1 to W_3. The attenuation curves must overlap at W_2 for linear frequency discriminator operation, but (with no signal) the bulk of the noise power in each tuned circuit comes from the frequency bands as given. Any noise sample waveform from the IF amplifier can be decomposed by Fourier analysis, into a sum of noise generators, in adjacent frequency bins. The sum from W_1 to W_2 is, for all practical purposes, independent of the sum from W_2 to W_3. The outputs of the two envelope detectors are two essentially independent Rayleigh distributed variables, with bandwidth 1/4 the IF bandwidth. The convolution of these two distributions yields a distribution which is approximately Gaussian. The discriminator output is then passed through an integrator to recover phase modulation. The integrator consists of a low pass filter with corner frequency at 67 Hz. Summation in the integrator yields an output which must be considered Gaussian. Passing this noise voltage through a hard limiter at +5 and - 5 volts yields the autocorrelation function given above. (See Papoulis Section 14.4)

A. Papoulis "Probability, Random Variables, and Stochastic Processes" McGraw-Hill 1965.

APPENDIX D

Phase-lock loop output statistics, no signal

The probability of noise getting through the exclusive or circuit, and maintaining a false threshold signal, depends upon the cross-correlation between x and y, the bit detector input currents. If these two currents have opposite signs at the sampling instant, noise during that bit time is accepted as a valid signal and the threshold signal is maintained for one more bit-time.

Timing jitter tends to increase the probability of a false detection. Any gate width modulation of the gates shown in Figure 4 tends to increase x and decrease y, or vice versa, given the low frequency character of the noise. On the other hand, displacement of the leading and trailing edges of a gate in the same direction tends cancel itself out.

In order to attach an accurate number to the magnitude of the effect of timing jitter, it is necessary to compute the autocorrelation of the phase modulation waveform.

The model used in computing this function is shown in Figure 10.

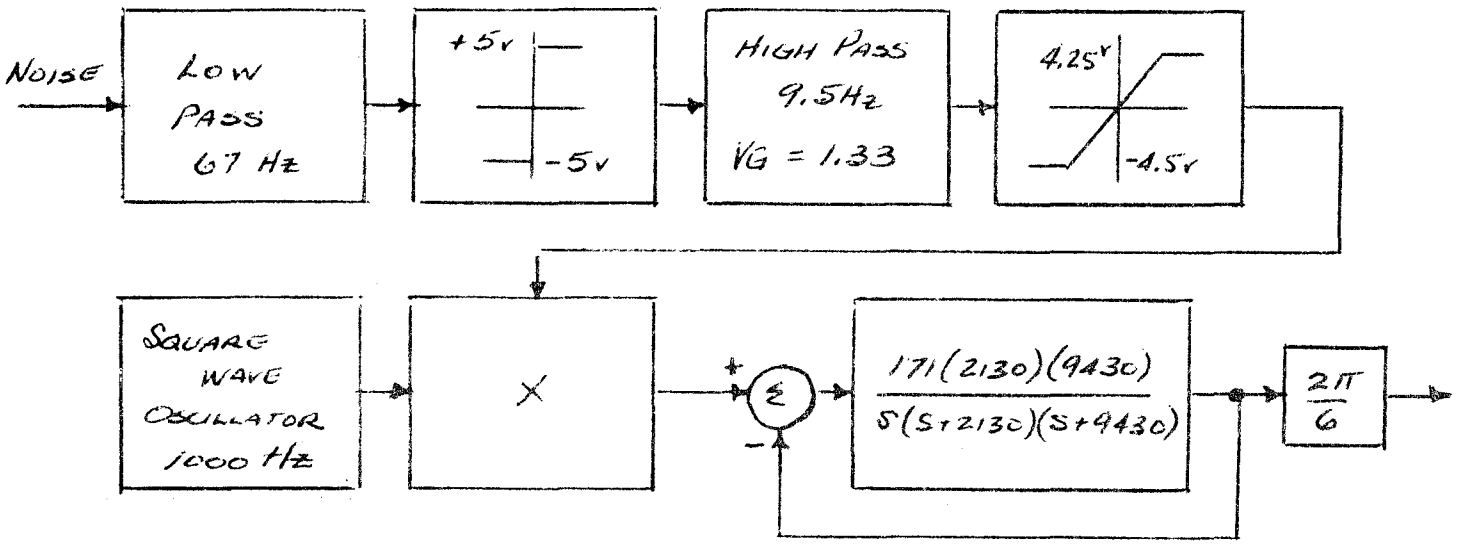


Figure 10 - Estimation of Phase Modulation with no Uplink Transmission

APPENDIX D (CONT)

The equivalent circuit for a phase-lock loop which is normally used is not applicable. Usually frequency or phase modulation of a 1000 Hz sub-carrier is the only input of significance. The noiseband here is from 10 to 100 Hz. The bulk of power in the chopper output is in a band from 900 to 1100 Hz, which is 2 to 3 octaves above the open loop gain cross-over. The summing point and transfer function shown in Figure 10 simulate the actual filter at frequencies above gain crossover, and $2\pi/6$ scaling converts from voltage to radians of phase modulation.

The model used is an approximation in that the output waveform does not modulate the reference oscillator. If this refinement were incorporated the oscillator sidebands would lie from 970 to 1030 Hz approximately and this would modify the filter output, etc. The additional complexity of simulating this feedback is not warranted.

The result of the computer program written to find the output autocorrelation is plotted in Figure 11.

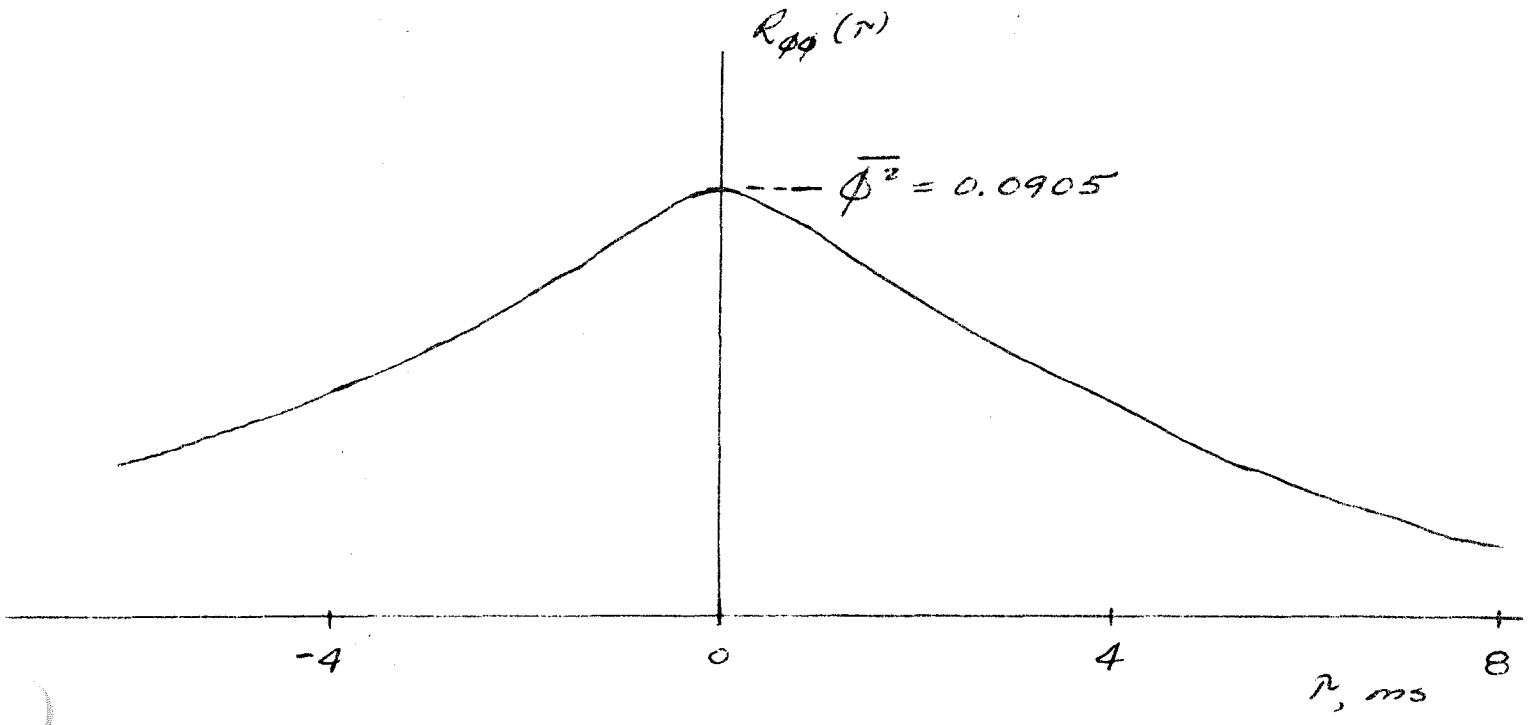


Figure 11 - Autocorrelation of Phase Modulation with no Uplink Transmission

APPENDIX D (CONT)

From Figure 11, the RMS phase modulation is 0.30 radians at 8.5 volts peak-to-peak input, with a bandwidth at half-power points from 970 Hz to 1030 Hz. For this approximate model the spectral density of the phase modulation is down 20 dB at 700 Hz and at 1300 Hz.

APPENDIX E

Probability of false detection, given a positive buffer output

The time constant of the buffer amplifier shown in Figure 4 is 16 milliseconds. The receiver output samples shown in Figure 7 do not have any saturated conditions which last as long as 8 milliseconds although there are one or two of about 6 milliseconds. Droop due to charging of the coupling capacitors will be less than 30%.

With the receiver output between -3.5 and -5 volts the buffer output is clamped at +4.25 volts by the Zener diodes. With no timing jitter the voltage e_1 is 1.33 volts and the voltage e_2 is 1.67 volts, at the sampling instant.

The average input current of the comparators will be (at sampling time),

$$\bar{x} = \frac{2(1.33) - (1.67) - (.5)}{2.55} = +0.19 \text{ microamperes}$$

$$\bar{y} = \frac{2(1.67) - (1.33) - (.5)}{2.55} = +0.59 \text{ microamperes}$$

The time constant of the bit detector RC circuit is one millisecond. Expressing time in milliseconds

$$e_1 = 4.25\left[1 - \exp\left(-.75 + \Delta_4 + .5 + \Delta_3 + .25 + \Delta_2 + .125 + \Delta_1\right)\right]$$

$$e_1 = 4.25\left[1 - \exp(-.375)\exp\left(-\Delta_4 + \Delta_3 + \Delta_2 + \Delta_1\right)\right]$$

Here the deltas are the delays in the gate edges, numbering from the trailing edge of the discharge gate. The deltas are small compared to one (millisecond).

$$e_1 = 4.25\left[1 - \exp(-.375)\left(1 \mp \Delta_4 \pm \Delta_3 \mp \Delta_2 \pm \Delta_1\right)\right]$$

APPENDIX E (CONT)

Designating the perturbation in e_1, e_2 by

v_1, v_2 and subtracting out the mean of e_1, e_2,

$$v_1 = 4.25 \exp(-.375)(\Delta_4 - \Delta_3 + \Delta_2 - \Delta_1)$$

$$v_2 = 4.25 \exp(-.500)(\Delta_5 - \Delta_4 - \Delta_3 + \Delta_2)$$

With a phase modulation angle of ϕ radians the delay in any circuit is $\phi/2\pi$ milliseconds.

$$v_1 = 0.46(\phi_4 - \phi_3 + \phi_2 - \phi_1) \text{ volts}$$

$$v_2 = 0.41(\phi_5 - \phi_4 + \phi_3 - \phi_2) \text{ volts}$$

The reason for the difference is that the capacitor for e_2 is closer to being fully charged, where timing jitter does not affect the results.

$$E\{\phi_4 \phi_3\} = E\{\phi_3 \phi_2\} = E\{\phi_{n+1} \phi_n\} = \overline{\phi_{n+1} \phi_n}$$

The variances in v_1 and v_2 are:

$$\sigma_1^2 = 0.21(4\overline{\phi_n \phi_n} - 4\overline{\phi_n \phi_{n+1}} + 2\overline{\phi_n \phi_{n+2}} - 2\overline{\phi_1 \phi_2} + 2\overline{\phi_1 \phi_3} - 2\overline{\phi_1 \phi_4})$$

$$\sigma_2^2 = 0.17(4\overline{\phi_n \phi_n} - 6\overline{\phi_n \phi_{n+1}} - 4\overline{\phi_n \phi_{n+2}} - 2\overline{\phi_n \phi_{n+3}})$$

Applying the results given in Appendix D,

$\sigma_1 = 0.028$ volts RMS

$\sigma_2 = 0.030$ volts RMS

The crosscorrelation between v_1 and v_2

APPENDIX E (CONT)

$\rho_{1,2} = \frac{\overline{v_1 v_2}}{\sigma_1 \sigma_2}$ turns out to be

$$\rho_{1,2} = \frac{0.19\,(-3\overline{\phi_n\phi_n} + 5\,\overline{\phi_n\phi_{n+1}} - 3\overline{\phi_n\phi_{n+2}} + \overline{\phi_n\phi_{n+3}} + \overline{\phi_1\phi_2} - \overline{\phi_1\phi_3} + \overline{\phi_1\phi_4} - \overline{\phi_1\phi_5})}{\sigma_1\sigma_2}$$

$\rho_{1,2} = +0.84$

The RMS noise in the comparator input currents is

$$\frac{(4(.028)^2 + (.030)^2 - 4(.84)(.028)(.030))^{1/2}}{2.55}$$

$$x_{noise} = \frac{0.041}{2.55} = 0.016 \text{ microamperes}$$

The decision levels $x = 0$ and $y = 0$ are 13 sigmas or more from the mean current. It is concluded that if the receiver remains saturated throughout a bit-time, the exclusive or circuitry will recognize this input as noise and reject it.

APPENDIX F

Probability of a false detection, given a transition in the buffer output

If the buffer output voltage changes polarity one or more times during a bit time, there is a possibility that the comparator input currents at the sampling instant will have opposite signs, and that this noisy bit will therefore be accepted as a signal.

For the assumed noise output of the receiver phase detector, (Gaussian, low pass), the probability of an odd number of zero crossings is arccosine exp (-AT), with A the low pass corner frequency in radians per second. Over temperature variations, A is expected to range from 400 to 450 rad/sec. (63 to 71 Hz). During one millisecond, the probability of an odd number of zero crossings will be 0.265 for the lower value of corner frequency and 0.278 for the higher value. The probability of an even number of zero crossings (0, 2, 4, . . .) is 0.735 for 63 Hertz and 0.722 for 71 Hertz.

In the noise output of the low pass filter, the power spectral density at 500 Hz is four times the density at 1000 Hz. Since the spectrum is a time average, it is expected that the number of bit-times with single crossings will be four times the number of bit-times with double crossings, and nine times the number of bits with triple crossings.

During any one millisecond, chosen at random on the entire time axis, for the 63 Hz filter the probability of no zero crossing is estimated at 0.675, the probability of one crossing is estimated at 0.239, two crossings, 0.060, and three or more crossings in a millisecond has an estimated probability of 0.026.

For the 71 Hz filter, the probability of no zero crossings is estimated at 0.660, the probability of one crossing is estimated at 0.250, two crossings, 0.062 and three or more 0.028. These probabilities apply for any millisecond selected at random.

In order to calculate the probability of a false detection, it is necessary to determine statistical averages for the comparator currents.

A computer program was written, using the theory outlined in Papoulis, Section 12.1, multiple terminals, to determine the variances and crosscorrelation of x and y at the sampling instant.

APPENDIX F (CONT)

The input autocorrelation used was $(4.25)^2 (1 - 2.5/T/+ T^2)$, with T being measured in milliseconds. This function is that of a 500 Hz square wave of random phase, multiplied by a 125 Hz square wave of random phase, and has the correct probabilities for single and double zero crossings, during a millisecond, (given that there are one or more zero crossings).

The results of running this program are:

σ_1 = 0.94 volts RMS

σ_2 = 1.07 volts RMS

$\rho_{1,\ 2}$ = 0.75

The corresponding values for the input currents of the comparators are:

σ_x = 0.51 microamperes RMS

σ_y = 0.61 microamperes RMS

ρ_{xy} = -0.134

The mean values of x, y are determined by the bias resistors and are approximately equal to 0.19 microamperes.

The averages obtained are independent of the actual probability density function, since the theory used does not depend upon the shape of the p.d.f.

The probability of a false detection given a transition, can be obtained by integrating over the appropriate regions.

$$P(\text{one}) = P(y > o,\ x < o) = \int_{\text{second quadrant}} (\text{p.d.f.})\, dx\, dy$$

$$P(\text{zero}) = P(y < o,\ x > o) = \int_{\text{fourth quadrant}} (\text{p.d.f.})\, dx\, dy$$

APPENDIX F (CONT)

If we assume that the comparators currents have a Guassian distribution, the results of this integration are:

P (one) = .258

P (zero) = .234

To determine the dependence of the results upon the assumed p.d.f., the integration is repeated for a more plausible function. In order to describe the density by a simple function, coordinate transformations are used to covert the sample points to unit variance, zero mean, uncorrelated variables.

With the transformation

$$W = \frac{x - \bar{x}}{\sigma_x} \qquad z = \frac{y - \bar{y}}{\sigma_y}$$

Normalized, zero mean variables are obtained.

With the rotational transformation

$$u = .707\ W + .707\ z$$

$$v = -.707\ W + .707\ z$$

The data points are expressed by uncorrelated variables, i.e.,

$$E\{uv\} = o.$$

However the distribution no longer has unit variances. With a scaling change

$$S = u/(1 + \rho_{xy})^{1/2}$$

$$t = v/(1 - \rho_{xy})^{1/2}$$

APPENDIX F (CONT)

The data points have a symmetrical distribution, unit variance, zero mean and are uncorrelated.

In this coordinate system, the decision lines no longer are parallel to the axis. The line x = o in the S, t plane has zero intercepts at

$$S = \frac{.19}{\sigma_x}\sqrt{\frac{2}{1+\rho}} = 0.567$$

$$t = -\frac{.19}{\sigma_x}\sqrt{\frac{2}{1-\rho}} = -0.495$$

The line y = o in the S, t plane has zero intercepts at

$$S = \frac{.19}{\sigma_y}\sqrt{\frac{2}{1+\rho}} = +0.473$$

$$t = \frac{.19}{\sigma_y}\sqrt{\frac{2}{1-\rho}} = +0.413$$

If p (x, y) is a Gaussian density function then p (S, t) is a Gaussian density function. Integration over the appropriate regions yields exactly the same probabilities as before, since coordinate transformations have not altered the relationship between data points and decision levels.

If on the other hand, it is assumed that the points are uniformly distributed over a circle of radius 2 on the S, t plane, the probability density becomes the simple function $p(S, t) = \frac{1}{4\pi}$.

Integration over t yields

$$p(s) = \frac{(4 - S^2)^{1/2}}{2\pi}, \quad \sigma_S = 1$$

Integration over S yields

$$p(t) = \frac{(4 - t^2)^{1/2}}{2\pi}, \quad \sigma_t = 1$$

APPENDIX F (CONT)

These curves are semicircles, which more nearly conform to the limited nature of the input than Gaussian functions. Note that although S and t are uncorrelated, they are not statistically independent, since they are subject to the constraint, $S^2 + t^2 \leq 4$

The combinations of S and t which will pass through the exclusive or logic are plotted in Figure 12.

Integration over the pie-shaped regions yields

P (one) = .272

P (zero) = .251

The conditional probability of a false detection, given one or more transitions in a bit time, for this distribution is 0.523. Choosing a one-millisecond interval at random from the entire time axis, the probability of a false detection for the four cases considered is as follows:

Max. freq, limited distribution = (.523) (.340) = .178

Max. freq, Gaussian distribution = (.492) (.340) = .167

Min. freq, limited distribution = (.523) (.325) = .170

Min. Freq, Guassian distribution = (.492) (.325) = .160

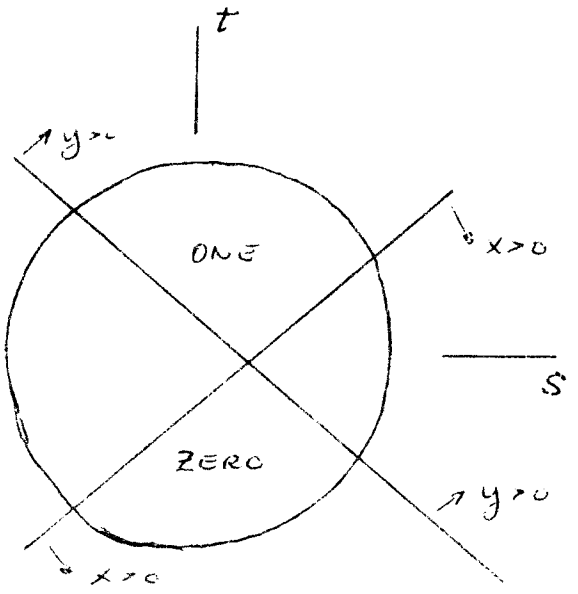


Figure 12 Decision Regions for Limited Distribution

APPENDIX G

Correlation between successive noisy bits

Zero crossings of a single pole low pass filter output tend to come in clusters. The output voltage has somewhat the characteristics of a random walk, wandering off to large values (saturating the receiver) then wandering back across the axis. When we take averages for the whole process on the entire time axis, the probability of one or more zero crossings in a millisecond is calculated to lie between 0.325 and 0.340.

When it is known that the filter output voltage is close to the axis (zero crossing in the previous millisecond) the probability of one or more zero crossings in a millisecond is increased. This is because the output of a single pole filter contains a significant amount of high frequency noise.

The solution for the problem of successive noisy bits is given in Papoulis, section 14-4, Distance between Zeros. In the Command Decoder, if a bit is detected, it is a foregone conclusion that a zero crossing occurred during the bit, because of the unbalanced summation at the comparators.

Assume that a zero crossing occurred at the center of the bit. The probability of an odd number of zero crossings occurring between 0.5 and 1.5 milliseconds later can be obtained from

$$\text{Cos}\,(\pi\,\text{Podd}) = \frac{\exp(-A) - \exp(-0.5A)\exp(-1.5d)}{\sqrt{[1-\exp(-A)][1-\exp(-3A)]}}$$

Assuming a 1, 4, 9 ratio between the probabilities for 1, 2, 3 zero crossings

P (zero crossings) = 1.225 Podd

$A = 2\pi f$ with f ranging from 63 to 71 Hz. Making appropriate substitutions,

P (zero crossings/previous detection) ranges from 0.425 to 0.432.