**Bendix**

**Aerospace Systems Division**

| | NO. | REV. NO. |
|---|---|---|
| | ATM-863 | |

Dual 90 Channel Multiplexer
Reliability Prediction and
Failure Mode, Effects & Criticality
Analysis

PAGE ___1___ OF ___18___

DATE May 28, 1970

This ATM documents the Reliability Prediction and Failure
Modes and Effects analysis of the Bendix designed Dual 90
Channel Multiplexer. The analysis reflects the final flight
configuration for the A2 ALSEP system.

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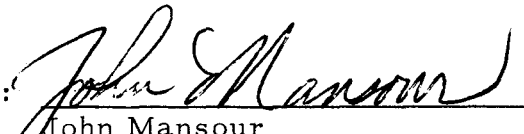**Aerospace Systems Division**

| | Dual 90 Channel Multiplexer Reliability Prediction and Failure Mode, Effects, & Criticality Analysis | NO. ATM-863 | REV. NO. |
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## 1.0 INTRODUCTION

The results of the reliability prediction and failure modes and effects analysis for the ALSEP A2 Dual 90 Channel Multiplexer are documented in this report. This multiplexer represents the Bendix designed unit which utilizes MOS-FET integrated circuits. The multiplexer was integrated with the Dynatronics A/D Converter. This design now provided complete redundancy for ALSEP Housekeeping engineering status data while retaining the interface design requirements specified for basic ALSEP.
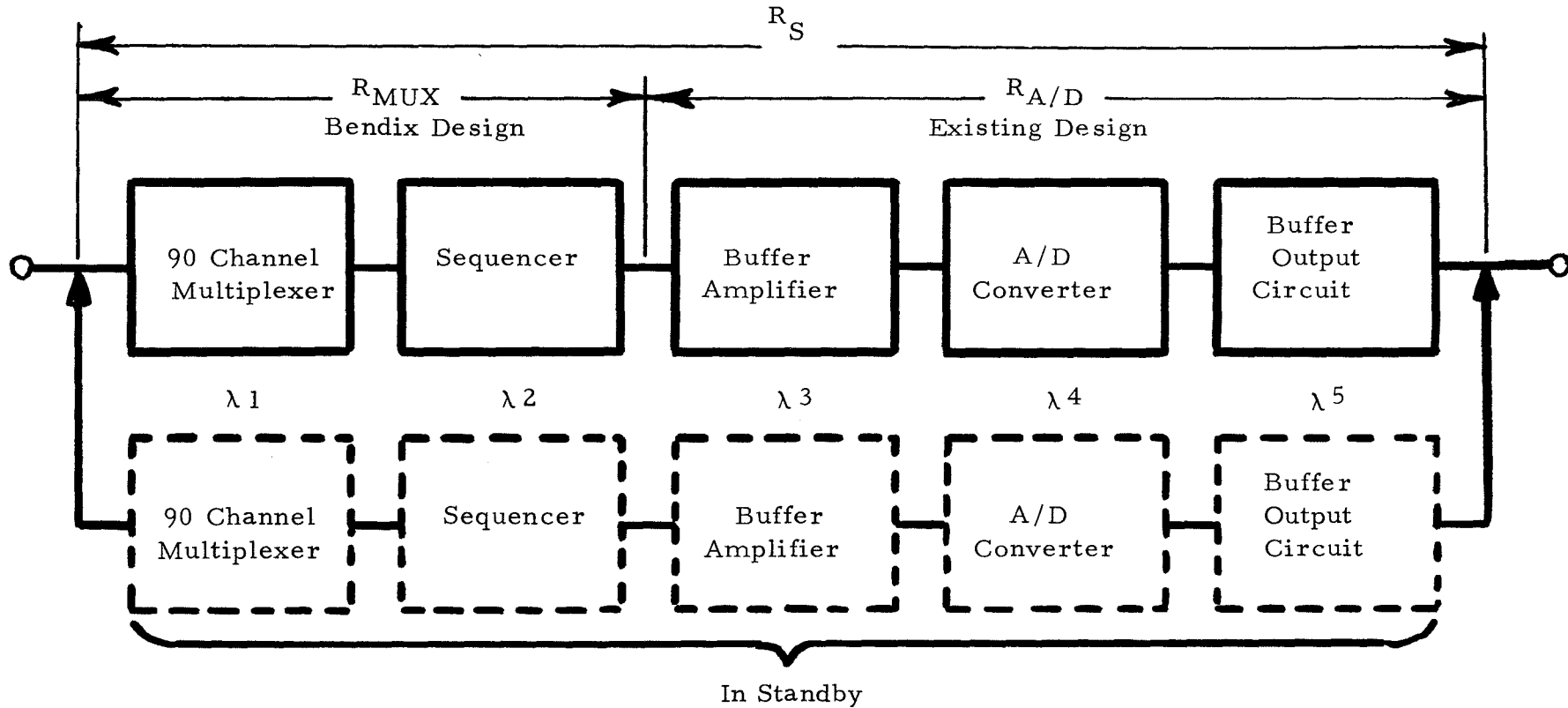
The reliability prediction for the Dual 90 Channel Multiplexer and A/D Converter is calculated to be 0.9981 for one year of lunar operation, which exceeds the specified design goal of 0.9956. All reliability objectives have been achieved or exceeded.

## 2.0 RELIABILITY PREDICTION

The reliability prediction for the Dual 90 Channel Multiplexer and A/D Converter, operating in the standby redundant configuration, is calculated to be 0.9981 for launch, deployment, and one year of lunar operation. The predicted reliability exceeds the specified goal of 0.9956.

Figure 1 defines the reliability block diagram and mathematical model for the Multiplexer and A/D convert component. The standby elements are activated by earth command. Functionally, the system operates in conjunction with the redundant Data Processor. However, the Data Processor was not included as part of this analysis.

The failure rates for each functional component identified in Figure 1 are tabulated in Table I. The failure rates shown represent composite totals derived from the part application stress ratios of each electronic piece part. The application reflects the anticipated "use" environment.

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$R_S$

$R_{MUX}$
Bendix Design

$R_{A/D}$
Existing Design

| 90 Channel Multiplexer | Sequencer | Buffer Amplifier | A/D Converter | Buffer Output Circuit |

$\lambda 1$ $\qquad$ $\lambda 2$ $\qquad$ $\lambda 3$ $\qquad$ $\lambda 4$ $\qquad$ $\lambda 5$

| 90 Channel Multiplexer | Sequencer | Buffer Amplifier | A/D Converter | Buffer Output Circuit |

In Standby

**Non-Redundant System**

$$R_{MUX} = \epsilon^{-(\lambda 1 + \lambda 2)t}$$

$$R_{A/D} = \epsilon^{-(\lambda_3 + \lambda_4 + \lambda_5)t}$$

$$R_S^1 = R_{MUX} \cdot R_{A/D}$$

**Standby Redundant System**

$$R_S \approx 1 - \frac{\lambda_o \lambda_s t^2}{2} - \frac{\lambda_o^2 t^2}{2}$$

DUAL 90 CHANNEL MULTIPLEXER & A/D CONVERTER
RELAIBILITY BLOCK DIAGRAM & MATHEMATICAL MODEL
FIGURE 1

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TABLE I

FAILURE RATE SUMMARY

| Assembly | $\lambda i$ | $\lambda oi$ (%/1000 Hrs.) Operating | $\lambda si$ (%/1000 Hrs.) Standby | Failure Rate Source |
|---|---|---|---|---|
| 90 Channel MOS-FET's | 1 | 0.1445 | 0.0001445 | ATM-860A |
| Sequencer | 2 | 0.387611 | 0.0003876 | ATM-860A |
| Buffer Amp. | 3 | 0.08579 | 0.01349 | ATM-274G |
| A/D Converter | 4 | 0.05350 | 0.01501 | ATM-274G |
| Output Buffer Circuit | 5 | 0.01426 | 0.00402 | ATM-274G |
| TOTALS $\sum \lambda i$ | | 0.685661 | 0.033052 | |

Reliability Calculation

$$R_{MUX} = \epsilon^{-(0.532111 \times 10^{-5})(8760.52)} = \epsilon^{-0.046616}$$

$$= 0.9544691$$

$$R_{A/D} = \epsilon^{-(0.15364 \times 10^{-5})(8760.52)} = \epsilon^{-0.01346}$$

$$= 0.986591$$

$$R_S = R_{MUX} \cdot R_{A/D} = (0.9544691)(0.986591)$$

$$= 0.9416706 \text{ (non-redundant System)}$$

$$R_S = \frac{(0.685661)(0.033052)(0.0876052)^2}{2} - \frac{[(0.685661)(0.0876052)]^2}{2}$$

$$= 1 - \frac{(0.00017388)}{2} - \frac{0.0036081}{2} = 1 - 0.00008694 - 0.00180405$$

$$= \underline{0.998109} \quad \text{(Standby Redundant System)}$$

## 3.0 FAILURE MODES, EFFECTS & CRITICALITY ANALYSIS

The failure mode and effects analysis for the 90 Channel Multiplexer are documented in Tables II and III. Table II describes the functional failure modes and the resultant effects on the end item and system level. Table II delineates the failure modes at the piece part level. Each identified failure is numerically itemized for cross reference between Tables II and III. (Note: the cross reference must be correlated by Assembly).

The Failure probabilities reflect the identified line item. The criticality ranking lists, by order of magnitude, the highest down to the lowest failure probabilities. Subcategories of failures (e.g., 2.1 2.2 of 2.0) are not ranked.

The format of Tables II and III is designed to provide the reader with a narrative description of the varying types of failures that could occur, combined with the resultant performance characteristics. This information is useful to system support in performing fault isolation should an anomally occur.

There are no ALSEP single point failures in either the 90 Channel Multiplexer or the A/D converter. Careful parts selection and circuit design coupled with the switching of most supply voltages in the redundant units has enabled the Bendix design to have zero single point failures. Failure Mode 1.1 of Table II implies a loss of a single housekeeping data channel. This loss cannot be restored by switching the redundant unit. This is a single thread failure for one channel only, the other 89 channels are unaffected. Thus, only 1% of the total functional ability of the multiplexer is lost with this one and only single thread failure mode. Further discussion will be found under Reliability Assessment on Page 6 of this ATM.

The loss of both 90 Channel Multiplexers or A/D converters will not cause the loss of any science data except for the dust detector, since this is the only science data handled by the multiplexer. Other than the dust detector, the 90 Channel Multiplexer handles only house-keeping data.

The A/D converter is treated in the reliability prediction but since the design of the A/D converter has not been changed, the FMECA for the converter is not included in this ATM. The A/D converter FMECA may be found in ATM 501, the complete FMECA for The ALSEP System.

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## 4.0    RELIABILITY ASSESSMENT

The purpose of performing a reliability prediction and failure modes analysis is to identify inherent design weaknesses. From the results of these analyses it has been concluded the reliability and design objectives have been fully satisfied.

With exception to one failure mode the multiplexer is mutually exclusive of its redundant counterpart. That is, full capability can be restored by switching to the redundant unit. The exception is item 1.1 of Table II. The failure mode is a loss of one (1) housekeeping data channel caused by an electrical short between the drain and substrate of a 1st tier MOS-FET gate on the multiplexer gate assembly. What happens is the +12V supply, which presently is not switched, will feed back into the analog source, thus offsetting the analog data signal being sampled by the redundant multiplexer. This failure mode was identified early in the design phase and prompted a reliability investigation. The results of the investigation disclosed that switching off the +12V supply was feasible. However to implement this capability would necessitate a modification of the PCU mother board assembly. In addition, the central station interface requirement would have to be modified. This in turn would preclude the interchangeability between multiplexers of previous arrays as is presently required.

The system criticality of the subject failure mode is low, therefore, the reliability improvement that would have been derived if the switching capability was incorporated would not have offset the program impact relative to cost and schedule. Therefore, the decision was made not to incorporate the +12V switching capability into the A2 system. However, in the event future ALSEP systems are built (Apollo 17 and subsequent) it is recommended the +12V switching capability be incorporated.

TABLE II

# FAILURE  MODE,  EFFECT  &  CRITICALITY  ANALYSIS

| CIRCUIT OR FUNCTION | ASSUMED FAILURE MODE | CAUSE OF FAILURE | EFFECT OF FAILURE | | FAILURE PROBABILITY Q x 10⁻⁵ | CRITIC-ALITY |
|---|---|---|---|---|---|---|
| | | | END ITEM | SYSTEM | $Q \times 10^{-5}$ | |
| 1.0 First Tier MOS-FET Gates | 1.0 Loss of one (1) Housekeeping Data Channel. | 1.0 Loss of one (1) FET gate in the 1st Tier, caused by the following mode of failure | 1.0 Multiplexer will continue to operate, minus the loss of the affected channel | 1.0 Minor degradation of overall system performance. Full data information can be restored via redundant multiplexer, except for item 1.1 | 801.717 | 1 |
| | | 1.1 Short: Drain to Substrate | 1.1 +12v signal will be sampled for A/D conversion. | | | |
| | | 1.2 Electrical Short form Drain to Gate, or Gate to Substrate. | 1.2 Analog channel will not turn on. | 1.1 Affected HK Data appears as all "1s" regardless of selected redundant multiplexer. Remaining 89HK channels are good. | 133.617 | - |
| | | 1.3 Open circuit on input terminal of Drain or Gate of one MOS FET. △VT> (10v) | 1.3 Analog channel will not turn on. | 1.2 Affected HK Data appears as all "0s". | 200.43 | - |
| | | | | 1.3 Same as 1.1.2 | 467.67 | - |
| 2.0 First Tier MOS-FET Gates | 2.0 Loss of six (6) Housekeeping Data Channels | 2.0 Failure of a six (6) ch. MOS FET in a manner such as to render the part totally inoperative. The 15 MOS FET 6 ch parts that compromise the 1st Tier can fail in the identified mode. | 2.0 Multiplexer will continue to operate minus the loss of the six affected data channels. | 2.0 System performance is further degraded, but considered minor unless the affected data channels are critical for system performance. | 20.78 | 3 |
| | | 2.1 Open circuit on the source or substrate output/input terminal. | 2.1 Loss of substrate voltage precludes turn-on of FET gate. Six gates per chip are summed at the source terminal, thus preventing data transfer to the A/D converter. | 2.1 Data for six consecutive HK channels will read all "0s". | 5.94 | - |
| | | 2.2 Electrical short from Source-Substrate, Source-Drain or Source to Gate for HK channels 85-90 only. | 2.2 The eighth bank of 1st Tier has only six data channels. This failure mode in other data banks would affect 12 channels. | 2.2 HK Data for chs 85-90 would be erroneous. Could read either all "0s" or all "1s". | 14.84 | - |

TABLE II

# FAILURE  MODE, EFFECT & CRITICALITY  ANALYSIS

| CIRCUIT OR FUNCTION | ASSUMED FAILURE MODE | CAUSE OF FAILURE | EFFECT OF FAILURE | | FAILURE PROBABILITY $Q \times 10^{-5}$ | CRITIC-ALITY |
|---|---|---|---|---|---|---|
| | | | END ITEM | SYSTEM | | |
| 3.0 MOS-FET Multiplexer Gates | 3.0 Loss of twelve (12) House-keeping Data Channels<br><br>3.1 Failure of a 1st Tier MOS-FET part.<br><br>3.2 Failure of a 2nd Tier MOS-Fet part (one channel only) | 3.0 Failure of a six channel MOS-FET part in one of the identified modes.<br><br>3.1 Electrical short cct source to substrate, Drain, or Gate<br><br>3.2 Electrical short cct from Drain to Substrate<br><br>3.2.1 Electrical short cct from Drain to Gate or Gate to Substrate. Open circuit on input terminal of Drain or Gate of one MOS-FET channel. An increase in threshold voltage which precludes turn-on of the MOS-FET. | 3.0 One 1st Tier data bank (12 HK channels) will be lost Multiplexer remains operational but at de-graded performance level.<br><br>3.1 An error signal (12v max) will be continuously present on the out-put of the affected data bank. This voltage will sum with the data channel being sampled.<br><br>3.2 +12v error voltage will be summed with the sampled analog signal.<br><br>3.2.1 The second Tier analog channel will not turn on. | 3.0 Good Housekeeping data re-duced to 78 channels using the failed multiplexer. Full data can be restored via redundant multi-plexer.<br><br>3.1 The digital data for the affected 12 channels will reflect the sum of the error voltage and the analog signal.<br><br>3.2 The affected HK Data Bank appears as all "1s".<br><br>3.2.1 Twelve HK channels of the affected bank will appear as all "0". | 44.39<br><br>20.78<br><br>17.82<br><br>57.9 | 2<br><br>-<br><br>-<br><br>- |
| 4.0 Second Tier MOS-FET Gates on Assy Board No. 2 | 4.0 Loss of Forty-two (42) Housekeeping Data Channels. | 4.0 Failure of the 2nd Tier multi-channel MOS-FET that controls HK channels 49 thru 90.<br><br>4.1 Open circuit on the Source or Substrate Output/Input Terminal | 4.0 Approximately 47% of the multiplexer becomes inoperative.<br><br>4.1 Loss of substrate voltage precludes turn-on of any FET gate An open source terminal prevents data transfer the A/D converter. | 4.0 Housekeeping data information significantly degraded. Full data restored via redundant multiplexer<br><br>4.1 HK channels 49 thru 90 will read all "0s". | 5.94<br><br>5.94 | 6<br><br>- |

TABLE II

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

| CIRCUIT OR FUNCTION | ASSUMED FAILURE MODE | CAUSE OF FAILURE | EFFECT OF FAILURE | | FAILURE PROBABILITY $Q \times 10^{-5}$ | CRITIC-ALITY |
|---|---|---|---|---|---|---|
| | | | END ITEM | SYSTEM | | |
| 5.0 Second Tier MOS-FET Gate on Assy Board No. 1 | 5.0 Loss of Forty-eight (48) Housekeeping data channels. | 5.0 Failure of 2nd Tier multi-channel MOS-FET that controls HK channels 1-48 | 5.0 53% of the multiplexer becomes inoperative. | 5.0 Housekeeping data information significantly degraded. Full data restored via redundant multiplexer. | 5.94 | 6 |
| | | 5.1 Open circuit on the Source or Substrate Output/Input terminal | 5.1 Loss of substrate voltage precludes turn-on of any FET gate. An open source terminal prevents data transfer the A/D converter. | 5.1 HK channels 1-48 will read all "0"s. | 5.94 | - |
| 6.0 Second Tier MOS-FET Gate on Assy Board No. 1 or 2 | 6.0 Loss of 78 or 84 HK Data channels. | 6.0 Failure of either 2nd Tier 6 channel MOS-FET. | 6.0 The multiplexer becomes effectively inoperative. The number of channels lost is contingent on which MOS-FET part that failed. | 6.0 All Housekeeping data is effectively lost. Full HK data can be restored via redundant multiplexer. | 17.82 | 4 |
| | | 6.1 Electrical short circuit from the Source to Drain | 6.1 The failed channel controls the analog signal of 12 1st gates. The eighth 2nd Tier switch controls only 6 1st Tier gate. An elect. short would result in the summation of two analog data channels. The resultant analog data would be in error. | 6.1 The 12 (or 6) analog signals controlled by the failed FET switch would be the only valid data. However, practically speaking it would be difficult to determine which data channels were correct unless a known analog signal was sampled in each 1st Tier Data Bank. | 17.82 | - |
| 7.0 Same as 6.0 | 7.0 Loss of all HK Data Channels. | 7.0 Failure of either 2nd Tier 6 channel MOS-FET. | 7.0 The multiplexer becomes inoperative. | 7.0 All HK data is lost. Redundant switch over is required. | 11.88 | 5 |
| | | 7.1 Electrical short cct from Source to Substrate or Gate. | 7.1 A +12v signal will be continuously transmitted to the A/D converter as an analog signal. | 7.1 All HK Data will read all "1"s. | 5.94 | - |
| | | | 7.1.1 When failed FET gate signal is at -12v the -12v level (for source to gate short) will be summed with analog data. | 7.1.1 Twelve HK channels will read all "0"s. The remaining 78 will be all "1"s. | 5.94 | - |

TABLE II

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

| CIRCUIT OR FUNCTION | ASSUMED FAILURE MODE | CAUSE OF FAILURE | EFFECT OF FAILURE — END ITEM | EFFECT OF FAILURE — SYSTEM | FAILURE PROBABILITY $Q \times 10^{-5}$ | CRITIC-ALITY |
|---|---|---|---|---|---|---|
| 1.0 DTL-MOS Interface circuit | 1.0 The DTL-MOS interface circuit becomes inoperative. | 1.0 Discrete component part failure. | 1.0 Sequencer shift register will not advance. Multiplexer will be slaved to the last analog data channel sampled. | 1.0 Only one (1) Housekeeping Data Channel will be transmitted. Switchover to redundant multiplexer will restore all Housekeeping Data. | 371.045 | 2 |
| | 1.1 Voltage level shifter fails in the logic "0" state. | 1.1 The output transistor either failed or is slaved in the off state. | 1.1 A -6v is continuously applied to the input of the Ø2 clock generator. The multiplexer advance pulse is inhibited. | | 150.145 | – |
| | 1.2 Voltage level shifter fails in the logic "1" state | 1.2 The output transistor stage either shorted collector to emitter or is slaved in the ON state. | 1.2 A +12v is continuously applied to the input of the Ø2 clock generator. The multiplexer advance pulse is inhibited | | 220.90 | – |
| 2.0 Phase Two (Ø2) Clock Generator | 2.0 The Ø2 clock generator circuit becomes inoperative. | 2.0 Failure of discrete part(s) or MOS logic. | 2.0 The shift register can not be sequenced. Multiplexer will remain in the last analog channel sampled. | 2.0 Only one housekeeping data channel will be transmitted. Switch-over to the redundant multiplexer will restore full Housekeeping Data. | 17.474 | 6 |
| | 2.1 Loss of Ø2 clock pulse | 2.1 Output of clock generator remains in continuous state (either + or - 12v) | 2.1 Ø1 clock pulse cannot be generated. Loss of both clock pulses disables the shift register. | | 15.149 | – |
| | 2.2 Ø2 clock pulse overlaps Ø1 clock pulse. | 2.2 Degradation of input coupling capacitor causing RC time constant to decrease by a factor greater than 10. | 2.2 The shift register will not sequence properly if the Ø1 & Ø2 clock pulses overlap. | | 2.325 | – |
| 3.0 Phase One (Ø1) Clock Generator | 3.0 The Ø1 clock generator circuit becomes inoperative. | 3.0 Failure of discrete part(s) or MOS logic. | 3.0 The shift register cannot be sequenced. | 3.0 Multiplexer becomes inoperative. Backup redundant unit available. | 71.752 | 4 |
| | 3.2 The Ø1 clock pulse remains at a continuous logic "0". | 3.1 Output of clock generator fails in continuous state at +12v. | 3.1 The shift register remains in last state. | 3.1 One HK data channel will be continuously sampled. | 28.90 | – |
| | 3.3 The Ø1 clock pulse remains at a continuous logic "1". | 3.2 Output of clock generator fails in continuous state at -12v. | 3.2 The shift register bit outputs will shift to all logic "0" (e.g., at +12v). | 3.2 All HK data channels will be off. HK telemetry data reads all "0"s. | 7.419 | – |

TABLE II

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

| CIRCUIT OR FUNCTION | ASSUMED FAILURE MODE | CAUSE OF FAILURE | EFFECT OF FAILURE | | FAILURE PROBABILITY $Q \times 10^{-5}$ | CRITIC-ALITY |
| --- | --- | --- | --- | --- | --- | --- |
| | | | END ITEM | SYSTEM | | |
| | 3.4 The $\emptyset1$ clock pulse or logic for 2nd Tier Gating function becomes inoperative.<br><br>3.4.1 Function fails in the logic "0" state.<br><br>3.4.2 Function fails in the logic "1" state. | 3.3 MOS logic fails as indicated.<br><br>3.3.1 $\emptyset1$ clock pulse to 2nd shift resigter is at continuous +12v.<br><br>3.3.2 $\emptyset1$ clock pulse to 2nd shift register is at continuous -12v. | 3.3 The sequencer operation becomes erratic.<br><br>3.3.1 2nd shift register will hang up in the last state. This will preclude sequencing of the 2nd Tier multiplexer gate.<br><br>3.3.2 All 2nd Tier multiplexer gates will eventually turn on. | 3.3 A minimum of 78 HK data channels will be lost.<br><br>3.3.1 The 12 HK channels corresponding to the selected 2nd Tier FET will be telemetered in the data stream.<br><br>3.3.2 All HK data will become erratic. | 35.876<br><br>17.938<br><br><br><br>17.938 | —<br><br>—<br><br><br><br>— |
| 4.0 The 1st and 2nd Tier Shift Register(s) | 4.0 The 12 Bit Serial to Parallel Shift Register (s) become inoperative.<br><br>4.1 All output stages fail in the logic "0" state.<br><br>4.2 All output stages fail in the logic "1" state.<br><br>4.3 Shift register fails to sequence.<br><br>4.4 Bit output of shift register fails in the logic "0" state. | 4.0 Failure of any stage<br><br>4.1 Shift register remains in the reset state. 1st stage fails in reset state. MOS logic (internal) will not accept the initial Vin pulse.<br><br>4.2 Set output of the 1st stage fails in the logic "0" level. Vin function remains at -12v.<br><br>4.3 Failure of any shift register Flip-Flop stage such that it will not toggle. The failed stage is in the "0" logic state.<br><br>4.4 The logic "0" Bit output FET fails in the ON mode.<br><br>4.4.1 Failed FET is for 1st Tier gate drive signal.<br><br>4.4.2 Failed FET is for 2nd Tier gate drive signal. | 4.0 The shift register controls the gating sequence of the 90 channel multiplexer.<br><br>4.1 All multiplexer MOS-FET gates will be turned OFF.<br><br>4.2 All multiplexer gates will be turned ON simultaneously.<br><br>4.3 The shift register will not transfer a logic "1" through the failed state.<br><br>4.4 Loss of multiplexer FET gate drive pulse.<br><br>4.4.1 Loss of every 12th data channels in the 1st Tier.<br><br>4.4.2 Loss of a bank of 12 1st Tier HK channels controlling 2nd Tier FET will not turn ON. | 4.0 Housekeeping data becomes degraded or erratic. Switchover to redundant unit restores all HK data.<br><br>4.1 No HK data. HK telemetry will appear as all "0"s.<br><br>4.2 HK telemetry data will be erroneous, for all 90 channels.<br><br>4.3 Only one HK telemetry channel will be transmitted.<br><br>4.4 Loss of 8 or 12 HK Data channels.<br><br>4.4.1 Loss of 8 HK Data channels.<br><br>4.4.2 Loss of a group of 12 HK Data measurements. | 1954.547<br><br><br><br>149.813<br><br><br>492.623<br><br><br>434.159<br><br><br>552.415<br><br><br>385.661<br><br>166.754 | 1<br><br><br><br>—<br><br><br>—<br><br><br>—<br><br><br>—<br><br><br>—<br><br>— |

TABLE II

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

| CIRCUIT OR FUNCTION | ASSUMED FAILURE MODE | CAUSE OF FAILURE | EFFECT OF FAILURE | | FAILURE PROBABILITY Q x 10⁻⁵ | CRITIC-ALITY |
|---|---|---|---|---|---|---|
| | | | END ITEM | SYSTEM | | |
| | 4.5 Bit Output of shift register fails in the logic "1" state. | 4.5 Either the Logic "0" FET fails in the off mode or the Logic "1" FET fails in the ON mode. | 4.5 Sequencer will provide multiple FET gate drive pulses. | 4.5 Either 78 or 82 HK data measurements are erroneous. The multiplexer becomes effectively inoperative. | 325.537 | — |
| | | 4.5.1 Failure is for a 1st Tier FET gate drive signal. | 4.5.1 Two channels for each 1st Tier bank of 12 FETS will be on simultaneously. (exception-when failed channel should be ON.) | 4.5.1 All but eight HK Data measurements will be erroneous. | 196.651 | — |
| | | 4.5.2 Failure is for a 2nd Tier FET Gate drive signal. | 4.5.2 Two 2nd Tier FET gates will be continuously ON. (Exception-when remaining seven 2nd Tier FETS are turned OFF). | 4.5.2 All but 12 HK Data measurements will be erroneous. | 128.886 | — |
| 5.0 Reset Logic | 5.0 The reset logic becomes inoperative. | 5.0 MOS Logic fails to generate the necessary timing functions. | 5.0 Sequencer becomes inoperative. | 5.0 Loss of all HK Telemetry Loss of 90th Frame pulse to the Data Proc. | 35.876 | 5 |
| | 5.1 Reset logic output fails in the logic "0" state. | 5.1 Output MOS FET either fails or is slaved to the on mode, thus providing a +12v to the reset input of each shift register. | 5.1 Sequencer will clock out to HK channel #1 and remain there. However, 90th Frame pulse will not be generated. | 5.1 Loss of 89 HK data measurements. No 90th Frame pulse signal will be sent to the Data Processor. | 17.938 | — |
| | 5.2 Reset logic output fails in the logic "1" state. | 5.2 Output MOS-FET either fails or is slaved to the OFF mode, thus providing a -12v to the reset input of each shift register. | 5.2 Sequencer will eventually turn all HK channels on simultaneously. | 5.2 All HK Data will be erroneous. A 90th Frame pulse signal will be sent to the Data Processor once every 0.6 sec. | 17.938 | — |
| 6.0 The 90th Frame Pulse Circuit | 6.0 The 90th Frame Pulse circuit becomes inoperative. | 6.0 Failure of the MOS Logic or MOS to DTL interface circuit. | 6.0 The analog multiplexer will continue to function properly. | 6.0 Loss of HK channel reference. Data Proc. Frame counter becomes inoperative. | 297.302 | 3 |
| | 6.1 The 90th Frame pulse is not generated. | 6.1 The circuit output transistor either fails in the ON mode, or is slaved to the ON mode. | 6.1 Same as 6.0 | 6.1 HK data stream will have to be synchronized on known data channels. | 141.177 | — |
| | 6.2 The 90th Frame pulse is continuously present. | 6.2 The cct output xstr opens or is slaved to the off condition. | 6.2 Same as 6.0 | 6.2 Data Proc. Frame counter is slaved to the reset state. The D/P even frame mark & heat flow 90th F. mark become erroneous. | 156.125 | — |

TABLE III

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

| PART/COMPONENT SYMBOL | FAILURE MODE ($\alpha$) | EFFECT OF FAILURE | | FAILURE PROBABILITY $Q \times 10^5$ | CRITIC-ALITY |
| | | ASSEMBLY | END ITEM | | |
|---|---|---|---|---|---|
| 1.0   Board No. 1 or Board No. 2 IST Tier MX02D MOS FET GATES <br><br> Brd No. 1, MX02D location X1-4, X6-9. <br><br> Brd. No. 2 MX02D Location X1-4, X6-8 | 1.0   Loss of one (1) FET channel in the IST Tier caused by the following mode of failure. <br><br> 1.1   Identified part fails short from Drain to Substrate (0.1059) <br><br> 1.2   Short: Drain to Gate, or Gate to Substrate. (0.1588) <br><br> 1.3   Open cct on input terminal of Drain or Gate of one (1) MOS Channel. <br><br> $\Delta V_T > 10V$ <br> (0.3706) | 1.0   Loss of one (1) HK Data Channel | 1.0   Multiplexer will continue to operate, minus the loss of affected channel. <br><br> 1.1   Affected HK Data Channel appears as all "Is" regardless of selected redundant multiplexer. Remaining 89 HK Channels are good. <br><br> 1.2   Analog Channel willnot turn on. <br><br> 1.3   Analog Channel will not turn on. | 801.717 <br><br><br> 133.617 <br><br><br><br><br> 200.43 <br><br> 467.67 | 1 <br><br><br> — <br><br><br><br><br> — <br><br> — |
| 2.0   Board Nos. 1 & 2 IST Tier MX02D MOS FET Gates <br><br> Board No. 1 MX020 Location X1-4, X6-9 <br><br> Board No. 2: MX020 Location X1-4, X6-8 | 2.0   Failure affecting the six (6) channels of an MX02D part in the identified manner. <br><br> 2.1   Open cct on the Source or Substrate (.0047) <br><br> 2.2   Electrical Short: Source to Substrate or Drain to Source or Source to Gate on MX02D (X8) of Board No. 2 (0.1176) | 2.0   Loss of Six (6) Housekeeping Data Channels | 2.0   Mux will function minus six affected channels. Redundant switch over will restore full capability. <br><br> 2.1   Data for Six conservative HK channels will read all "Os" <br><br> 2.2   HK Data Chs. 85-90 would measure either all "O's" or "1s" | 20.78 <br><br><br><br> 5.94 <br><br> 14.84 | 3 <br><br><br><br> — <br><br> — |

TABLE III

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

| PART/COMPONENT SYMBOL | FAILURE MODE (α) | EFFECT OF FAILURE ASSEMBLY | EFFECT OF FAILURE END ITEM | FAILURE PROBABILITY Q x 10⁵ | CRITIC-ALITY |
|---|---|---|---|---|---|
| 3.0 MX02D MOS FET Gates on Boards No. 1 or 2 as indicated<br><br>3.1 Location X1-4 and X6-9 (X6-7 on Brd. No. 2)<br><br>3.2 Location X5 on Boards No. 1 or 2 | 3.0 Failure of a six (6) Ch MX02D MOS FET as indicated.<br><br>3.1 Electrical Short Source to Sub-strate Source to Drain or Source to Gate (0.1647)<br><br>3.2 Electrical Short from Drain to Substrate (0.0141)<br><br>3.2.1 Short cct from Gate to Drain or Gate to Substrate. Open cct on input terminal of Gate or Drain of one channel. (0.0459) | 3.0 Loss of twelve (12) Housekeeping Data Channels | 3.0 Good HK Data reduced to 78 channels. Redundnat switch over will restore full capability.<br><br>3.1 The digital data for the affected 12 channels will reflect the sum of the erros voltage and the analog signal.<br><br>3.2 The +12V error voltage will be summed with the sampled analog signal.<br><br>3.2.1 The 2nd Tier analog channel will not turn on. | 44.39<br><br>20.78<br><br>17.82<br><br>57.9 | 2<br>–<br>–<br>– |
| 4.0 MX02D, X5 on Board No. 2 | 4.0 Failure of 2nd Tier multichannel MOS FET Gate as follows: Open on Source or Substrate (0.0047) | 4.0 Loss of Forty-Two (42) House-keeping Data Channels. | 4.0 Multiplexer degraded by approxi-mately 47% of capability. Full capability restored by redundant switchovers HK Channels 49-90 are affected. | 5.94 | 6 |
| 5.0 MX02D, X5 on Board No. 1 | 5.0 Failure of 2nd Tier gate as follows: Open cct on Source or Substrate (0.0047) | 5.0 Loss of Forty-eight (48) House-keeping Data Channels. | 5.0 Loss of HK Data Channels 1-48. Full capability restored by switch-over to redundant sides. | 5.94 | 6 |
| 6.0 MX02D, X5 on Boards No. 1 or 2 | 6.0 Failure of either 2nd Tier Gate as follows: Elect Short from Source to Drain (0.0141) | 6.0 Loss of 78 or 84 HK Data Channels | 6.0 Twelve or Six data channels would still be good. However, practically speaking identifying the correct data channels would be difficult. | 17.82 | 4 |
| 7.0 MX02D. X5 on Boards No. 1 or 2 | 7.0 The 2nd Tier gate fails short cct from Source to Substrate or Source to Gate. (0.0094) | 7.0 Loss of all HK Data Channels. | 7.0 All HK Data is lost. Redundant switchover will restore full capability. | 11.88 | 5 |

TABLE III

| SYSTEM ALSEP (A2) | PREPARED BY J. Mansour | NO. ATM 863 | REV. |
|---|---|---|---|
| END ITEM 90 Ch. Multiplexer | DWG NO. 2338900 | PAGE 15 of 18 | |
| ASS'Y Sequencer | DWG NO. 2338909 | DATE May 28, 1970 | |

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

| PART/COMPONENT SYMBOL | FAILURE MODE ($\alpha$) | EFFECT OF FAILURE | | FAILURE PROBABILITY $Q \times 10^5$ | CRITIC-ALITY |
|---|---|---|---|---|---|
| | | ASSEMBLY | END ITEM | | |
| 1.0 DTL-MOS Interface circuit and designated piece parts. <br><br> 1.1 Resistors: R1, R2 and R3 Diode: CR1 <br> 1.2 XSTRS: Q1 and Q2 ULO2C-X3: NGIA | 1.0 Open or short cct <br><br> 1.1 Open Cct: R1, R2, R3 Q1, C-E, C-B, E-B, Q2, C-E, C-B, B-E, Short Cct: CR1, Q1, E-B, B2, E-B, C-B, NGIA: Fails in logic "1" state. (0.0452) <br><br> 1.2 Open Cct: CR1 Short Cct: Q1, C-E, C-B, Q2, C-E, NGIA: Fails logic "0" state. (0.0665) | 1.0 The DTL-MOS interface cct becomes inoperative. <br><br> 1.1 Voltage level shifter fails in the logic "0" state. <br><br> 1.2 Voltage level shifter fails in the logic "1" state. | 1.0 Sequencer shift register will not advance. Multiplexer will be slaved to the last data channel sampled. <br><br> 1.1 A-6V is continuously applied to the input of the $\phi_2$ clock generator. The mux advance pulse is inhibited. <br><br> 1.2 A +12V is continuously applied to the input of the $\phi_2$ clock generator cct. The mux advance pulse is inhibited. | 371.045 <br><br><br><br> 150.1454 <br><br><br><br> 220.900 | 2 <br><br><br><br> — <br><br><br><br> — |
| 2.0 Phase two ($\phi_2$) Clock Generator Resistors: R5, ULO2G-X3: NGIB | 2.0 Open or short <br><br> 2.1 Open Cct: NGIB: Fails logic "1 or 0". (0.005) <br><br> 2.2. Open Cct: R5 - Parameter Drift NGIB turn on, turn off characteristics Degrades (0.0007) | 2.0 The $\phi_2$ Clock Generator circuit becomes inoperative. <br><br> 2.1 Loss of $\phi_2$ clock pulse. Output continuously @ + or - 12V. <br><br> 2.2 $\phi_2$ clock pulse becomes eratic i.e. multiple pulses, pulses overlap with $\phi_1$ pulses, etc. | 2.0 The Shift Register can not be sequenced. Multiplexer will remain in the last analog channel sampled. <br><br> 2.1 The $\phi_1$ clock pulse can not be generated. Loss of both clock pulses disables the shift register. <br><br> 2.2 The Shift Register will not sequence properly. | 17.474 <br><br><br><br> 15.149 <br><br><br><br> 2.325 | 6 <br><br><br><br> — <br><br><br><br> — |

TABLE III

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

| PART/COMPONENT SYMBOL | FAILURE MODE ($\alpha$) | EFFECT OF FAILURE — ASSEMBLY | EFFECT OF FAILURE — END ITEM | FAILURE PROBABILITY $Q \times 10^5$ | CRITIC- ALITY |
|---|---|---|---|---|---|
| 3.0 Phase One ($\phi_1$) Clock Generator Resitors: R6, and R7 Capacitors:C1 and C3 Diode: CR3, ULO2C -X3: NGIC ULO2C-X2: NG2A, B ULO2C-X5: NG3D | 3.0 Open or short<br><br>3.1 Open Cct: C2, R7, NGIC fails in logic "0" state.<br><br>Short Cct: C2, CR3, NGIC fails in logic "0" state. (0.0087)<br><br>3.2 NGIC fails in the logic "1" state. (0.0021)<br><br>3.3 As shown below.<br><br>3.3.1 NG2A fails in Off mode NG2B fails in logic "1" state. (0.0054)<br><br>3.3.2 NG3D fails in logic "1" state NG2B fails in logic "0" state. (0.0054) | 3.0 The $\phi_1$ Clock Generator circuit becomes inoperative.<br><br>3.1 Loss of $\phi_1$ clock pulse. Output continuously @ +12V.<br><br>3.3 The $\phi_1$ clock output pulses remains continuously @ -12V.<br><br>3.4 The OR Logic the 2nd teir $\phi_1$ gating function becomes inoperative.<br><br>3.4.1 The 2nd Tier $\phi_1$ clock pulse fails to occur.<br><br>3.4.2 The 2nd Tier $\phi_1$ clock pulse is continuously present. | 3.0 The Shift Register can not be sequenced properly.<br><br>3.1 Multiplexer will remain in the last analog channel sampled.<br><br>3.2 The Shift Register bit outputs will shift to all logic "0". All HK data channels will be in the Off mode.<br><br>3.3 The sequencer operation becomes erratic. A minimum of 78 HK data channels will be lost.<br><br>3.3.1 The 2nd Tier Shift register will hang up in its last state.<br><br>3.3.2 All 2nd Tier gates will eventually turn on. | 71.752<br><br>28.980<br><br>7.419<br><br><br>35.876<br><br><br>17.938<br><br>17.938 | 4<br><br>–<br><br>–<br><br><br>–<br><br><br>–<br><br>– |

TABLE III

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

| PART/COMPONENT SYMBOL | FAILURE MODE (α) | EFFECT OF FAILURE | | FAILURE PROBABILITY Q x 10⁻⁵ | CRITIC-ALITY |
|---|---|---|---|---|---|
| | | ASSEMBLY | END ITEM | | |
| 4.0 1st and 2nd Tier Shift Register Shift Register: A1, A2 Resistors: R14 thru R24 R27 thru R33 MX02D: NG4 NG5, NG6 ULO2C-X5: NG 3C | 4.0 Open or short | 4.0 The 12 Bit Serial to Parallel Shift Register becomes inoperative. | 4.0 The multiplexer gating sequence becomes inoperative or erratic. | 1954.547 | 1 |
| | 4.1 A1, A2 fails in reset state NG4, NG5, NG3C or NG6 fails logic "0". (0.0451) | 4.1 All output stages fail in the logic "0" state. | 4.1 All multiplexer MOS-FET gates will be turned off. | 149.813 | – |
| | 4.2 A1, A2 Vin function continuously present. Set output of first stage fails logic "0" NG4, NG5, or NG6 fails in logic "1" state. (0.1483) | 4.2 All output stages fail in logic "1" state. | 4.2 All multiplexer gates will be turned on simultaneously. | 492.623 | – |
| | 4.3 A1 S.R. Any stage fails in the logic "0" output. (0.1307) | 4.3 Shift Register fails to sequence. | 4.3 Only one (1) HK data channel will be transmitted. | 434.159 | – |
| | 4.4 A1 or A2 Shift Register Resistors: R14-24, 27-37. | 4.4 A bit output stage of Shift Register fails in the logic "0" state. | 4.4. Either 8 or 12 HK Data channels will be lost. | 552.415 | – |
| | 4.4.1 A1 S.R. fails. A bit output stage remains slaved or shorted in the On Mode. NG4, NG5 shorts thus failing in logic "0" state R13-23: Open Cct. (0.1161) | 4.4.1 Failure in the A1 Shift Register or Pulldown resistors. 4.4.2 Failure is in the A2 Shift Register | 4.4.1 Every 12th date in the first Tier for the affected drive pulse will note turn on. (Maximum of 8 channels will be lost). | 385.661 | – |
| | 4.4.2 A2 S.R. fails similar to A1 above R25, R27-33: Open Cct NG6 fails logic "0" state. (0.0502) | 4.5 Bit Output of S.R. A1 or A2 fails in the logic "1" state. | 4.4.2 One of eight second Tier gates will fail to turn on Loss of 12 HK data channels. | 166.754 | – |
| | 4.5 Shift Register A1 or A2 | 4.5.1 Failure is for a 1st Tier FET gate drive signal. | 4.5 The Sequencer will provides multiple FET gate drive pulses. A minimum of 78 HK Data Channels will be erroneous. | 325.537 | – |
| | 4.5.1 A1, bit output FET fails to turn on NG4, NG5 fails in logic "1" mode. (0.0592) | 4.5.2 Failure is for a 2nd Tier FET gate drive signal. | 4.5.1 Two channels in each 1st Tier bank will remain on simultaneously. | 196.651 | – |
| | 4.5.2 A2 bit output FET fails to turn on NG6 fails in logic "1" mode. (0.0388) | | 4.5.2 Two 2nd Tier gates will be on simultaneously. | 128.651 | – |

TABLE III

| SYSTEM ALSEP (A2) | PREPARED BY J. Mansour | NO. ATM-863 | REV. |
|---|---|---|---|
| END ITEM 90 Ch. Multiplexer | DWG NO. 2338900 | PAGE 18 of 18 | |
| ASS'Y Sequencer | DWG. NO. 2338909 | DATE May 28, 1970 | |

TABLE III

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

| PART/COMPONENT SYMBOL | FAILURE MODE (α) | EFFECT OF FAILURE ASSEMBLY | EFFECT OF FAILURE END ITEM | FAILURE PROBABILITY $Q \times 10^{-5}$ | CRITIC- ALITY |
|---|---|---|---|---|---|
| 5.0 Reset Logic ULO2C-X5: NG3A NG3B | 5.0 Open or short | 5.0 The reset logic becomes in-operative. | 5.0 All 90 channels will be lost. Sequencer will not transmit a 90th Frame Pulse to the Data Processor. | 35.876 | 5 |
| | 5.1 NG3A output continuously at -12V. NG3B output continuously at +12 V. (0.0054) | 5.1 Reset logic fails in the logic "0" state. | | | |
| | | 5.22 Reset logic fails in the logic "1" state. | 5.1 Sequencer will clock out to HK channel #1 and remain there 90th Frame Pulse will not be generated: | 17.938 | – |
| | 5.2 NG3A output continuously at +12V. NG3B output continuously at -12V. (0.0054) | | | | |
| | | | 5.3 Sequencer will eventually turn all HK channels on simultaneously. | 17.938 | – |
| 6.0 90th Frame Pulse cir- cuit Q3, Q4, R8, R9, R10 R11, R12, CR4. | 6.0 Open or short | 6.0 The 90th Frame Pulse circuit becomes inoperative. | | | |
| | 6.1 Short Cct. Q4, CE, Q3 CE, R11 and R12: Open. (0.0425) | 6.1 The 90th Frame Pulse circuit not generated. | 6.0 The Multiplexer will continue to function. However, Data Processor operation will be degraded. | 297.302 | 3 |
| | 6.2 Short Cct. Q3 BE Open Cct. R9, R10, CR4, Q4 CE, Q3 CE. (0.047) | 6.2 The 90th Frame Pulse is continuously present. | 6.1 HK Data stream will have to be synchronized on known data channels. | 141.177 | – |
| | | | 6.2 Data Processor Frame Counter is slaved to the reset state. | 156.125 | – |