A Cold-Startup SSHI Rectifier for Piezoelectric Energy Harvesters with Increased Open-circuit Voltage

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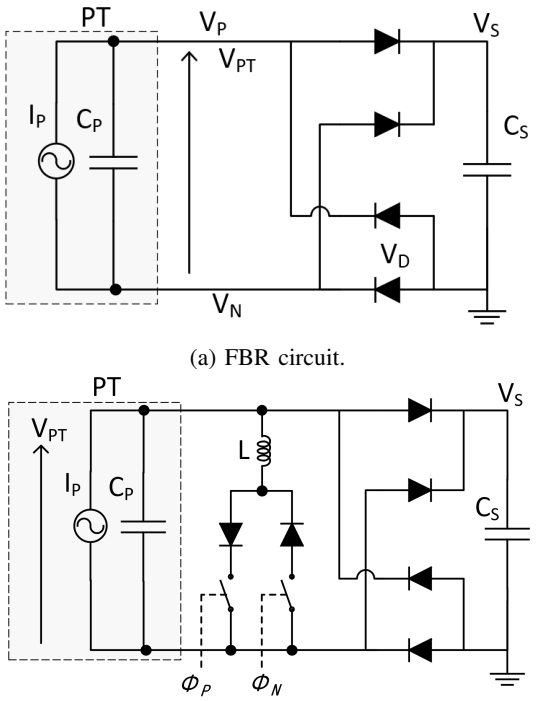
***Abstract*—Piezoelectric vibration energy harvesting has drawn much research interest over the last decade towards the goal of enabling self-sustained wireless sensor nodes. In order to make use of the harvested energy, interface circuits are needed to rectify and manage the energy. Among all active interface circuits, SSHI (synchronized switch harvesting on inductor) and SECE (synchronous electric charge extraction) are widely employed due to their high energy efficiencies. However, the cold-startup issue still remains since an interface circuit needs a stable DC supply and the whole system is completely out of charge at the beginning of implementations or after a certain period of time without input vibration excitation. In this paper, a new cold-startup SSHI interface circuit is presented, which dynamically increases the open-circuit voltage generated from the piezoelectric transducer (PT) in cold-state to start the system under much lower excitation levels. The proposed circuit is designed and fabricated in a $0.18\,\mu\mathrm{m}$ CMOS process and experimentally validated together with a custom MEMS (microelectromechanical systems) harvester, which is designed with split electrodes to work with the proposed power extraction circuit. The experiments were performed to start the system from the cold state under variable excitation levels. The results show that the proposed system lowers the required excitation level by at least 50% in order to perform a cold-startup. This aids restarting of the energy harvesting system under low excitation levels each time it enters the cold state.**

Keywords: Energy harvesting, energy conversion, piezoelectric transducers, power conditioning, CMOS, rectifiers, synchronized switch harvesting on inductor (SSHI).



(a) FBR circuit.

(b) SSHI circuit.

Fig. 1: Widely employed FBR and SSHI circuits.

I. Introduction

Along with the wide expansion of Internet of Things (IoT), low-power sensor modules are being designed to interface between the physical world and the Internet [1]. Powering these ubiquitous wireless sensor nodes and making them fully self-sustained still remains a key challenge for industrial and academic research. In the past decade, there has been increasing research interest in harvesting energy from the environment to power distributed low-power electronics [2]–[4]. Among all energy harvesting solutions, harvesting ambient kinetic vibration energy becomes more promising in applications where kinetic vibration continuously or periodically occurs [5]–[8]. Over the past several years, different types of vibration energy transducers have been proposed based on a variety of transducer types, such as electrostatic, piezoelectric, electromagnetic, etc [9], [10]. Among all these energy transducers, piezoelectric transducers (PT) are widely employed to harvest ambient kinetic energy due to their relatively high power density and the compatibility with conventional CMOS processes. In PTs, Lead Zirconate Titanate (PZT) is widely used for macroscopic harvesters due to its high piezoelectric charge constant and other materials, such as Aluminum Nitride (AlN) and Zinc Oxide (ZnO), are typically used in MEMS (Microelectromechanical System) PTs [11].

As the transduced energy from the PTs is of a highly variable AC form over a wide range of excitation levels, this energy cannot be directly used to drive an electrical load since most electronic devices require stable DC voltage supplies. Hence, an interface circuit is needed to rectify the harvested energy and store it in an energy storage device to provide continuous DC power [12]–[16]. Among all interface circuits, full-bridge rectifiers (FBR) are widely used due to their simplicity and stability. A circuit implementation of a FBR is shown in Fig. 1a. While a PT is vibrating, it can be modeled as a current source I_P in parallel with a capacitor C_P. Despite the advantages, a FBR usually sets a high voltage

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threshold to overcome before it starts to extract energy from the PT to a storage capacitor, C_S, connected at the output. In order to overcome the threshold set by the FBR, the voltage across the PT, V_{PT}, has to attain either $V_S + 2V_D$ or $-(V_S+2V_D)$. Hence, V_{PT} must be flipped between these two threshold values for every half period of I_P and the electric charge used to flip V_{PT} is wasted. Assuming the open-circuit voltage amplitude (zero-to-peak) generated from the PT is V_{OC}, the threshold voltage can be expressed as:

$$V_{OC} > V_S + 2V_D \tag{1}$$

This threshold can be as high as several volts in some cases and this is relatively hard to be attained for MEMS PTs. Although this condition can be marginally satisfied under high excitation levels, the power extraction efficiency of a FBR can be extremely low since most of generated charge is wasted due to the threshold. In order to improve the power efficiency under low excitation levels, many active interface circuits, using linear or nonlinear energy extraction techniques, have been proposed recently [17]–[27].

Among all active interface circuits, SSHI (synchronized switch harvesting on inductor) is believed to be one of the most energy-efficient circuits [28]–[35]. Fig. 1b shows a widely used SSHI rectifier. In a SSHI circuit, an inductor is employed to synchronously flip the voltage across the PT with a RLC oscillation loop. At each zero-crossing moment of I_P, V_{PT} starts to decrease or increase from V_S+2V_D or $-(V_S+2V_D)$, respectively. This is also the moment while $|V_{PT}|$ attains its peak value. Assuming V_{PT} is positive before voltage flipping is performed, a pulse signal ϕ_P is generated to close the RLC loop for a certain period of time to allow current to flow through the diode located on the left. While V_{PT} needs to be flipped in the other direction, ϕ_N is generated to close the right-side path of the RLC circuit. As a SSHI circuit helps flip V_{PT}, the amount of wasted charge is significantly decreased; hence, the overall power efficiency is increased.

In order to keep the operation of the SSHI circuit, a DC power supply is needed. However, while the system is in a cold state, all the capacitors in the system are not charged and the DC supply is not available. The cold state corresponds to the time while the energy harvesting system is initially implemented or the stored energy decreases to a near-zero level due to leakage and quiescent power consumption after a long period of time without ambient vibration. Hence, the cold-startup of an energy harvesting system is crucial to keep the operation of the system. For a SSHI circuit with an built-in voltage regulator, the voltage across the capacitor C_S needs to attain a certain level to generate a stable DC supply, represented as V_{DD}. Before V_{DD} is available, all the switches are open and the SSHI circuit simply works as a full-bridge rectifier (FBR). As the FBR introduces high voltage thresholds, as previously mentioned, the energy extraction efficiency in this case can be extremely low or even zero when the excitation level is low. Therefore, the voltage V_S may never be charged up to provide a functional V_{DD} under low excitation levels and the circuit does not extract any energy.

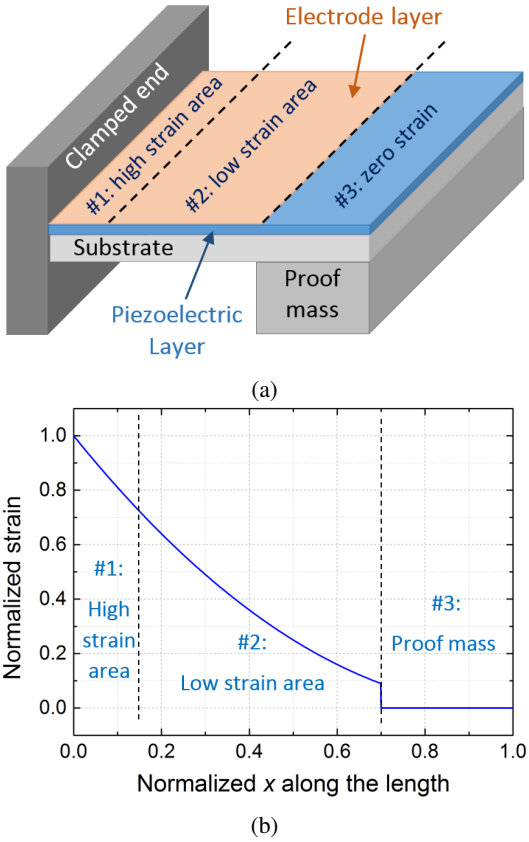


Fig. 2: A cantilevered piezoelectric transducer with strain distribution along the length to explain the inspiration of the proposed cold-startup SSHI circuit.

In this paper, a new SSHI interface circuit with cold-startup capability is presented in Section II. The detailed circuit implementations and simulations are shown in Section IV. The fabricated CMOS circuit is co-integrated with a custom MEMS PT for experiments in the following section and a conclusion is provided at the end.

II. Proposed System

For most of reported SSH rectifiers [30], [32], [36]–[38], cold-startup issue has not been addressed. When these systems are in cold-state, the whole system is out of charge and the synchronized switching signals cannot be generated. In this case, the SSH circuits are not working actively and whole system works as a passive FBR. As previously discussed, the voltage threshold for a FBR is that the open-circuit voltage from the PT should satisfy the condition expressed in (1). Before a regulated DC power supply, noted as V_{DD}, is available from the extracted power by the FBR, the high voltage threshold set in (1) can be too high to be satisfied under low excitation levels, where the cold-startup issue arises.

In this section, a new SSHI interface circuit with cold-startup capability is presented. As discussed, before V_{DD} is available in the system to generate synchronized switching signals, the system simply works as a passive FBR. In order to help start the system under low excitation levels, the proposed system dynamically changes the effective open-circuit voltage

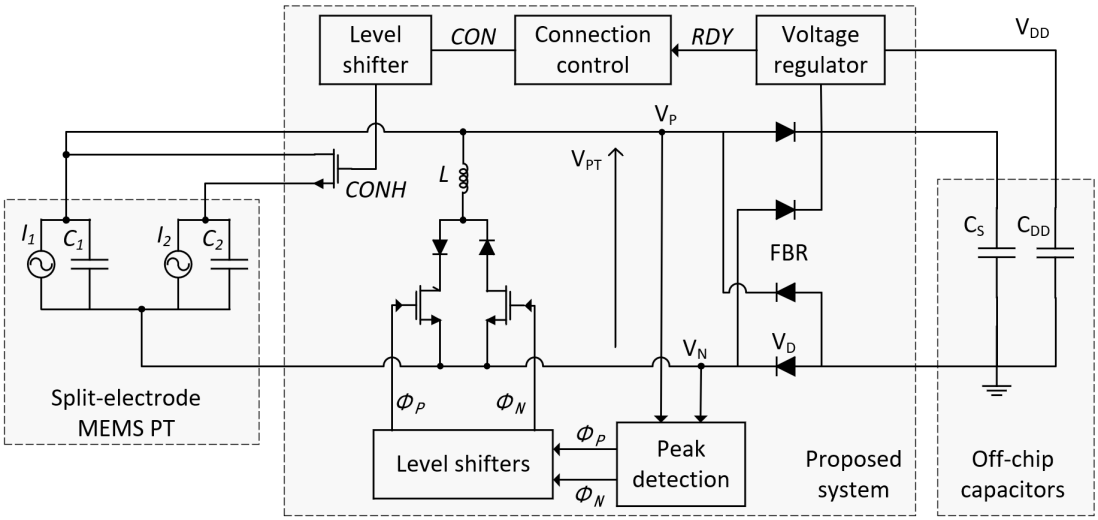


Fig. 3: System architecture of the proposed circuit.

(V_{OC}) generated from the PT to overcome the threshold of (1). For instance, when the system is in the cold-state, the system chooses to use only a specific region of the PT to effectively increase V_{OC} by sacrificing some generated power. This idea is inspired by analysis on the strain distribution in a cantilevered PT, as shown in Fig. 2a. Along the length of the cantilever, the strain due to the mechanical deformation during vibration decreases from the clamped end to the free end. The strain distribution is plotted in Fig. 2b. In order to explain how to increase V_{OC} during the cold-state by the proposed circuit, the cantilever is analyzed by splitting it into three regions. The first region is close to the clamped end, where the strain is high. The second region is the rest of non-zero strain region, where strain is relatively low. The third region is where the proof mass is present and the strain in this region is zero.

While the cantilever is vibrating, the generated open-circuit voltage from each region is proportional to the strain in this region. Hence, it can be seen that the open-circuit voltage generated in only region 1 can be much higher than using the two regions 1+2. In order to start the SSHI rectification system from its cold state, it is preferred to have higher V_{OC} when then system is working as a passive FBR during the cold state due to the voltage threshold set in (1). Hence, the proposed system dynamically disconnects the region 2 to use only the region 1 to effectively increase V_{OC}. As a result, V_{OC} can be significantly increased even under low excitation levels and the SSHI rectification system can be started after V_S is charged to a level to provide a stable V_{DD} power supply to the system. When the region 2 is disconnected by the proposed system, the total generated power from the PT is decreased since the power in the region 2 is sacrificed for the purpose of obtaining a higher V_{OC}. Hence, after the system is started and V_{DD} is available, the proposed system is able to dynamically connects the region 2 back to the system to make use of the energy generated in this region.

As the proposed cold-startup SSHI interface circuit dynamically chooses different connection configurations on different regions in a PT, a specific PT with split electrode is required for the proposed system. In this implementation, the electrode layer of the PT is split into two regions which cover a small high-strain area close to the clamped end and a large low-strain area close to the free end. The inherent capacitors of the high-strain and low-strain regions of the PT are noted as C_1 and C_2, respectively. The ratio of the two regions is chosen according to the environmental excitation conditions and C_1 is recommended to be smaller than C_2 to have an obvious V_{OC} increase for the region 1. The split-electrode design of a PT is not the focus of this work since this specific design is just adopted to co-integrate with the proposed cold-startup SSHI interface circuit. The fabricated MEMS PT is just used to experimentally evaluate the proposed system.

Similar electrode-splitting designs have been reported previously. In [39], the electrode is split into three regions along the strain direction so that the power generated in different regions can be used for different parts of the rectification system. In this design, the open-circuit voltage amplitudes generated in all the three regions is approximately equal due to the splitting direction. Hence, this design does not inherently increase open-circuit voltage level to help cold startup. In [40], electrode is split along a direction orthogonal to the strain direction. Hence, the generated open-circuit voltage amplitudes are different for different regions. In this work, the electrode is split in a similar way to [40]; however, this electrode-splitting design is first used to inherently increase the open-circuit voltage to help cold startup together with a new CMOS rectification circuit.

The architecture of the proposed system is shown in Fig. 3. The proposed cold-startup SSHI interface circuit is implemented on-chip (except the inductor L) in a $0.18\,\mu\mathrm{m}$ CMOS process. Two off-chip capacitors are employed to serve as energy storage capacitors. While the system is in the cold state, the DC supply to the system, V_{DD}, is 0V and the SSHI rectifier is not operating. The two regions of the PT, noted as C_1 and C_2, are disconnected by default and only C_1 is connected to the rectifier since the signal CON (short for connect) is low. The signal $CONH$ is the shifted version of

CON with a higher voltage level for logic '1'. In this case, the switches controlling the inductor are kept OFF due to low ϕ_P and ϕ_N signals and the system simply works as a passive FBR. As the voltage generated in C_1 is high, it can easily overcome thresholds set in (1) and charge the storage capacitor C_S to a voltage level until a DC supply V_{DD} is available. Once the V_{DD} is available, the signal $CONH$ goes high to connect C_2 into the system and the SSHI circuit is powered ON. As a result, the extracted power can be significantly increased due to the additional energy from the region 2 and the operating SSHI circuit. Level shifters are employed to provide over-drive the gates of the analog switches. Detailed circuit implementations for all the blocks of the proposed system will be provided in Section IV.

III. Modeling

In this section, the proposed system is modeled and the extracted power is calculated. In the time domain, the modeling can be performed in two stages. The first stage is when the system is started from the cold state until V_{DD} is available. In this stage, the system works as a full-bridge rectifier (FBR) and only region 1 of the PT is active. The second stage is the time after the system is started and V_{DD} is available. In this stage, region 2 is connected to the system and the SSHI circuit operates to increase extracted power.

A. First stage

Assuming the open-circuit voltage amplitude generated from the region 1 is V_{OC1} and the internal capacitance of the region 1 is C_1, the total amount of charge generated in the region 1 in one vibration period is:

$$Q_1 = 4C_1V_{OC1} \tag{2}$$

As previously mentioned, the FBR sets a threshold on the input voltage and the voltage generated from the PT should attain $V_S + 2V_D$ or $-(V_S + 2V_D)$ in order to transfer energy to the storage capacitor C_S, as shown in Fig. 4a. Hence, the charge between these two thresholds is wasted and this wastage occurs twice in one period since the voltage across the PT, V_{PT}, needs to be flipped twice. This wasted amount charge in one period can be expressed as:

$$Q_{loss1} = 4C_1(V_S + 2V_D) \tag{3}$$

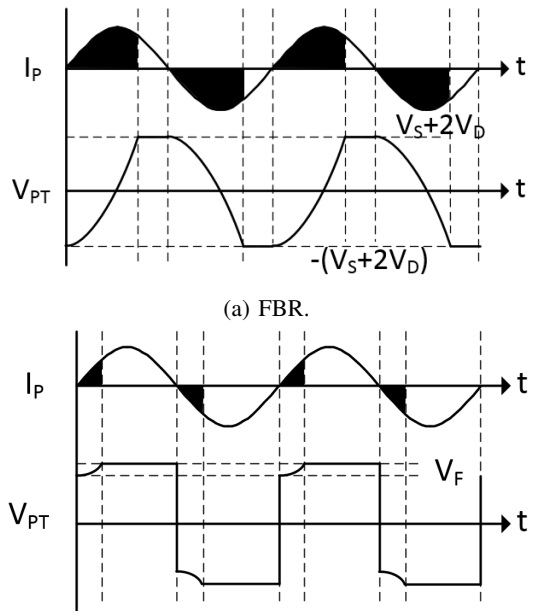
The remaining charge is transferred into C_S and is expressed as:

$$Q_S = 4C_1(V_{OC1} - V_S - 2V_D) \tag{4}$$

Assuming the voltage increase in C_S is small, the power transferred into C_S can be calculated as:

$$P_S = f_P Q_S V_S = 4f_P C_1 V_S (V_{OC1} - (V_S + 2V_D)) \tag{5}$$

where f_P is the vibration frequency. There is a small voltage increase in the capacitor C_S and it can be expressed as:



(a) FBR.

(b) SSHI.

Fig. 4: Waveforms of I_P and V_{PT} for a FBR and a SSHI circuit.

$$\Delta V_S = 4\frac{C_1}{C_S}(V_{OC1} - (V_S + 2V_D)) \tag{6}$$

Hence, the voltage V_S after each vibration period can be expressed as:

$$V_S(n) = V_S(n-1) + \Delta V_S \tag{7}$$

where $V_S(0) = 0\,\mathrm{V}$ is assumed to be the initial condition.

B. Second stage

After V_S attains V_{DD} (assuming a buck converter or a simple voltage regulator is employed to generate V_{DD}), a stable power supply is available and the system goes into the second stage. Now, the region 2 of the PT is connected into the system and the SSHI circuit is being powered to flip the voltage across the PT. Assuming the capacitance of the region 2 is C_2, the total capacitance connected to the system in this stage is $C_{1+2} = C_1 + C_2$. The open-circuit voltage generated by regions 1+2 is assumed as V_{OC1+2} and it is obvious that this value is lower than V_{OC1}, which is generated by region 1. Hence, the total amount of charge generated in one period for this stage is:

$$Q_2 = 4C_{1+2}V_{OC1+2} \tag{8}$$

After V_{PT} is flipped, there is a voltage loss, V_F, due to the resistive damping in the RLC oscillation loop, as shown in Fig. 4b. The voltage loss can be approximately expressed as:

$$V_F = (V_S + 2V_D)(1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C_P} - 1}}}) = (V_S + 2V_D)\eta_F \tag{9}$$

where L is the inductor, R is the total resistance in the RLC loop and $\eta_F = (1 - e^{-\frac{\pi}{\sqrt{\frac{4Ln^2}{R^2C_P} - 1}}})$ is the loss ratio. Hence, the remaining charge to be transferred into C_S is:

$$Q_S = 2C_{1+2}(2V_{OC1+2} - \eta_F(V_S + 2V_D)) \tag{10}$$

The power transferred to C_S can also be calculated as:

$$P_S = f_P Q_S V_S = 2f_P C_{1+2} V_S (2V_{OC1+2} - \eta_F(V_S + 2V_D)) \tag{11}$$

The voltage increase in C_S in one period is:

$$\Delta V_S = 2\frac{C_{1+2}}{C_S}(2V_{OC1+2} - \eta_F(V_S + 2V_D)) \tag{12}$$

Hence, the V_S value after each period can be calculated as:

$$V_S(n) = V_S(n-1) + \Delta V_S \tag{13}$$

where $V_S(0)$ equals to V_{DD} in this stage.

C. Simulation

In this section, a simulation is performed to calculate V_S and the output power before and after the circuit is started. In the simulation, the capacitors in the two regions are set as $C_1 = 0.9\,\text{nF}$ and $C_2 = 3.6\,\text{nF}$, the vibration frequency is $f_P = 219\,\text{Hz}$, the open-circuit voltages generated by the region 1 and region 1+2 are $V_{OC1} = 4.2\,\text{V}$ and $V_{OC12} = 2\,\text{V}$, respectively. The voltage flipping loss ratio η_F is assumed to be 0.5. The required DC supply for the system is $V_{DD} = 1.5\,\text{V}$. These assumptions are based on the same values to be used in the experiments in this paper.

Fig. 5a shows the simulated V_S and output power values for 500 seconds starting from the cold state. The V_S is calculated with equations (7) and (13) and the output power is calculated with equations (5) and (11). The V_S value goes to a level around $8\,\text{V}$ and does not go higher because the excitation level cannot overcome the threshold set by the SSHI voltage flip loss V_F, which is increased by a higher V_S value, as expressed in (9). Since V_S does not increase, the power tends to zero. A zoom-in figure showing the first $100\,\text{s}$ is shown in Fig. 5b. It can be seen from the zoom-in figure that V_S attains $1.5\,\text{V}$ at around $63\,\text{s}$ and from this moment, the SSHI circuit is powered ON and the region 2 is connected to the system. Hence, V_S increases faster after this moment due to much higher output power, which is shown as a dashed line in the figure. The abrupt jump in the power graph is due to the combining of region 2 and the startup of the SSHI circuit.

IV. Circuit Implementations

This section describes the implementation of the proposed cold-startup SSHI energy harvesting system, which consists of three sub-sections: the conventional SSHI interface circuit (including synchronous signal generation, inductor driving, etc.), the cold-startup circuit (including voltage regulation, connection configuration circuits and circuit to generate signals to dynamically configure the connection of the two regions of the PT) and an example of the PT to experimentally evaluate the proposed system.

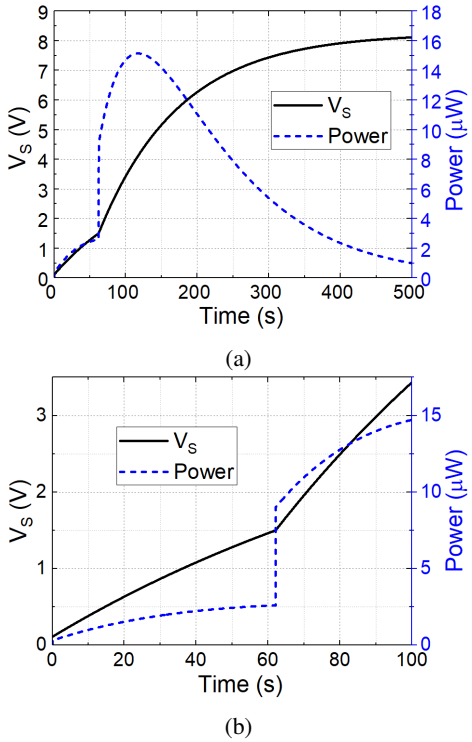
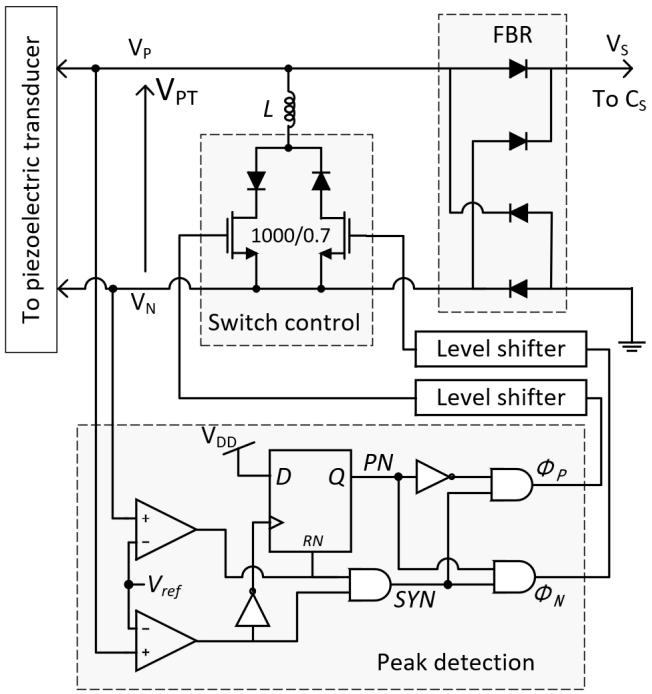


Fig. 5: Simulated V_S and output power values for (a) the first $500\,\text{s}$ and (b) the zoom-in figure in the first $100\,\text{s}$.

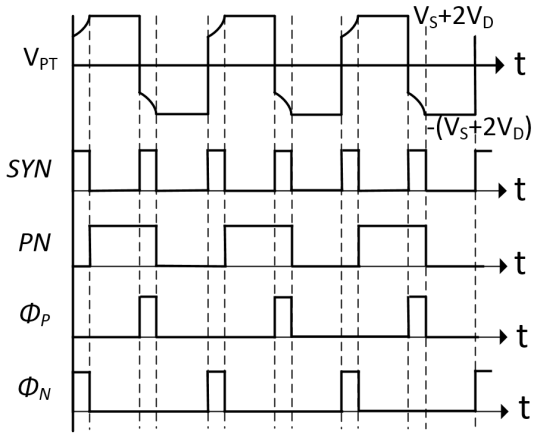
A. SSHI circuit

A SSHI interface circuit is presented in this section and the circuit diagram and associated waveforms are shown in Fig. 6. The figure shows that the SSHI circuit interconnects between the PT and a storage capacitor with three blocks: FBR, peak detection and switch control blocks. The FBR employs four on-chip Schottky-barrier diodes with measured forward voltage drop at around $V_D \approx 0.25\,\text{V}$.

The peak detection block aims to detect the moment while $|V_{PT}|$ (or $|V_P - V_N|$) attains its peak value, which is also the zero-crossing moment of the current source I_P in the PT [30], [32]. While $|V_{PT}|$ is at its peak value and begins to decrease, the diodes of the FBR are just about to turn OFF. At this instant, one of V_P and V_N is close to $-V_D$ and it starts to increase. In this block, two continuous-time comparators are employed to compare V_P and V_N with a reference voltage V_{ref}, which is set slightly higher than $-V_D$. Hence, while V_P or V_N starts to increase from $-V_D$, one of the two comparators is triggered and this signal indicates the moment when the voltage needs to be flipped. The outputs of these two comparators are ANDed and the resulting signal SYN is a synchronous signal to control voltage flipping. A D-flip-flop is employed to detect the polarization of V_{PT} while it needs to be flipped. The signals ϕ_P and ϕ_N selectively copy the signal SYN according to the level of PN to drive the two analogue switches in the switch control block. Two level shifters are employed to shift the ON-state voltage level of ϕ_P and ϕ_N to a higher level to over-drive the gates to fully turn ON the two switches. The waveforms of these signals are shown in Fig. 6b. In the switch control block, two large NMOS



(a) Circuit diagram.



(b) Waveforms.

Fig. 6: SSHI interface circuit and associated waveforms.

transistors are employed as switches and the two Schottky diodes are on-chip implemented. The inductor is implemented off-chip and the circuit is tested with different values of L in order to implement different voltage flip efficiencies.

B. Level shifters and DC-DC converter

Since the voltage at any node in the system, especially V_P and V_N, can be any voltage between $-V_D$ and $V_S + V_D$ during operation, the gate of the three NMOS switches, as shown in the proposed system architecture in Fig. 3, need to be over-driven. In order to fully turn ON these three analog switches, three level shifters are employed. The signals, CON, ϕ_P and ϕ_N, are shifted from V_{DD} to a higher voltage level V_{DDA} for the logic '1', where $V_{DDA} = 3V_{DD}$. Fig. 7 shows the circuit diagram of the voltage level shifter used in this implementation, where $V_{DD} = 1.5\,\mathrm{V}$ and $V_{DDA} = 4.5\,\mathrm{V}$.

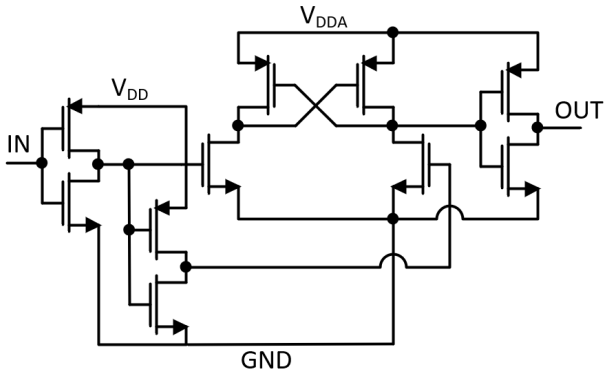


Fig. 7: Circuit diagram of the level shifter.

A switched-capacitor (SC) DC-DC converter is employed to generate the gate over-driving voltage level V_{DDA} and the circuit implementation is shown in Fig. 8. In order to drive the SC DC-DC converter, an on-chip ring-oscillator is designed to output a clock signal of around $8\,\mathrm{kHz}$. The clock signal is down-scaled to $1\,\mathrm{kHz}$ with a frequency divider. The $1\,\mathrm{kHz}$ signal is then cross-coupled with its delayed and inverted version with two NAND gates to provide two non-overlapping clock signals ϕ_1 and ϕ_2. These two signals are then shifted with two identical level shifters to drive the SC DC-DC converter. The level shifters are the same as shown in Fig. 7. The SC DC-DC converter has a output-to-input voltage ratio of 3/1; hence, a voltage level of $3V_{DD}$ is generated at the output. The SC converter generates V_{DDA}, which is used in the level shifters providing the switch driving signals ϕ_1 and ϕ_2. Hence, the two level shfiters depend on the voltage level generated in the following converter. As a result, in the first several clock cycles, the V_{DDA} level is charged up gradually from $0\,\mathrm{V}$ and it attains $V_{DDA} = 3V_{DD}$ after some clock cycles. The ring oscillator employed in this implementation consumes $184\,\mathrm{nW}$ power and the whole DC-DC converting block shown in Fig. 8 consumes $195\,\mathrm{nW}$.

C. Cold-startup circuit

This section presents the cold-startup circuit to be employed together with the split-electrode PT introduced in previous sections. According to Fig. 3, the key signal to be generated from the cold-startup circuit is CON, which connects the region 2 of the PT to the rectification circuit. The circuit diagram is shown in Fig. 9a, which consists of a voltage regulator and a connection control block. V_{DD} is designed to be $1.5\,\mathrm{V}$ in this implementation. C_S and C_{DD} are two energy storage capacitors, which are also shown in Fig. 3. The voltage regulator block employs a band-gap voltage reference and a continuous-time comparator to generate a signal RDY to transfer energy from C_S to C_{DD}. The signal RDY is shifted to a higher level, $RDYH$, to fully drive the PMOS switch with a level shifter and the shifted version of RDY is measured in the measurement section. The circuit diagram of the nano-power comparator is shows in Fig. 10. The comparator compares the reference voltage with a divided version of V_{DD} to turn OFF the PMOS switch while V_{DD}

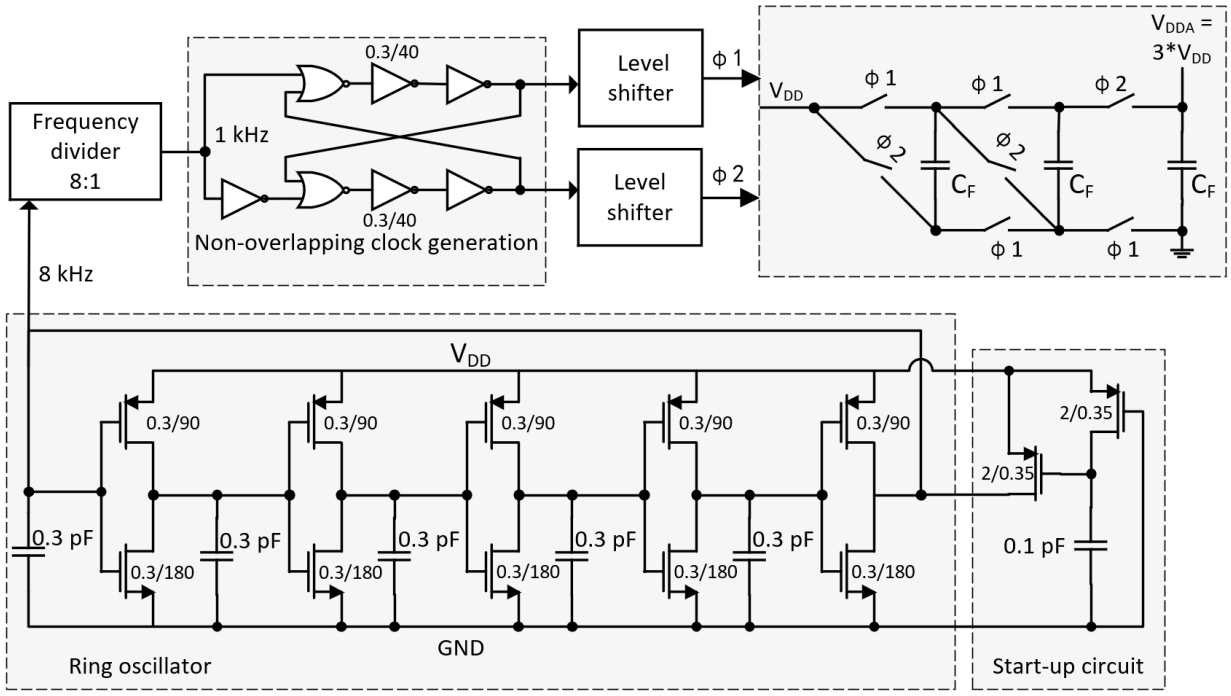
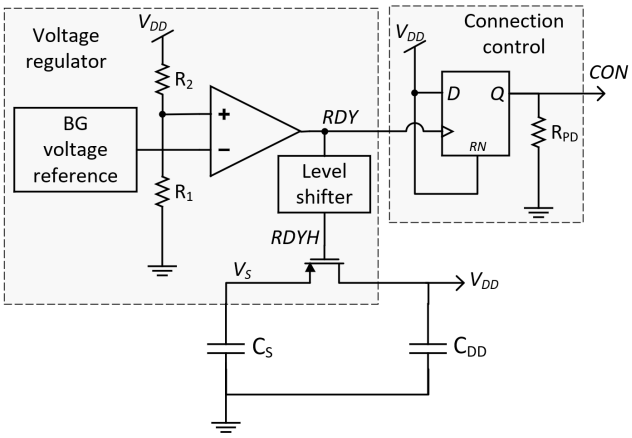
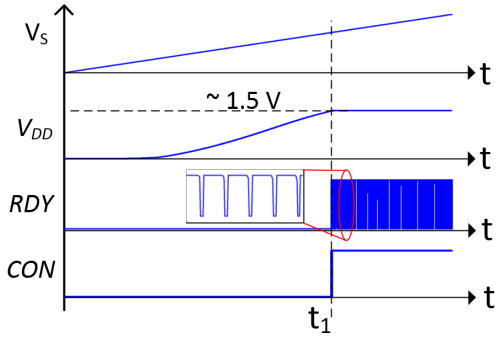


Fig. 8: Generation of gate over-driving voltage level V_{DDA}.



(a) Circuit diagram.



(b) Waveforms.

Fig. 9: Cold-startup circuit and associated waveforms.

attains 1.5 V and turn ON the PMOS switch while V_{DD} goes too low in order to keep V_{DD} around 1.5 V. While the system is in the cold state, the signal RDY keeps low. Hence, C_S and C_{DD} are connected in this case to buildup V_{DD}. This corresponds to the period before t_1 in Fig. 9b. During this period, since V_{DD} is gradually increased from 0 V to 1.5 V, the output signal CON of the D-flip-flop in the connection control block keeps low via a pull-down resistor. While V_{DD} achieves 1.5 V at t_1, RDY and $RDYH$ go high to turn OFF the PMOS switch to stop increasing V_{DD}. The rising edge of RDY triggers the flip-flop to generate a high level CON. As the DC supply V_{DD} is available and the SSHI circuit is powered from t_1, the high CON signals connects the region 2 of the PT to the system to further increase the extracted power and; therefore, the SSHI circuit is started from its cold state.

D. Custom MEMS PT to test the circuit

This section presents the split-electrode MEMS PT used to experimentally evaluate the proposed interface circuit. The PT is shown in Fig. 11, where the top electrode of the PT is split into two regions. The size of the cantilever is 9 mm × 9 mm. The proof mass occupies 9 mm × 3 mm at the free end and rest area of the cantilever is covered by the two electrodes. The two regions share a common bottom electrode and only the top electrode is split, so there are three electrode pads shown in the die photo, which correspond to the two top electrodes and the bottom electrode. The top electrode of C_1 is always connected to the proposed system; however, that of C_2 is connected with a NMOS switch to the system. The switch is controlled by a signal $CONH$, which is maintained at a low level during the cold-state. After the system is started, $CONH$ goes high to connect the region 2 to the system to extract the energy

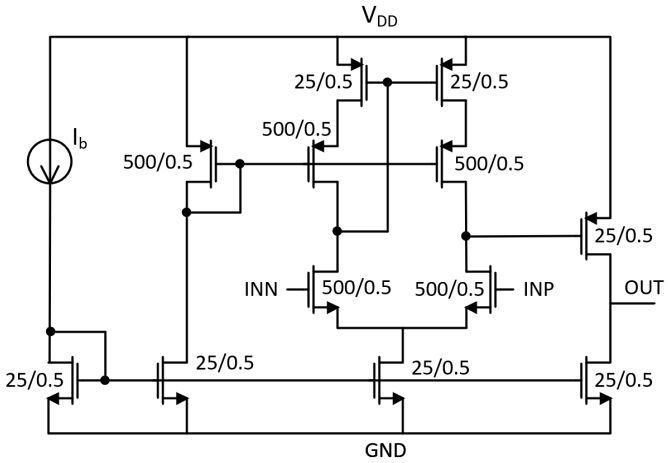


Fig. 10: Circuit diagram of the comparator used in the system.

generated in this region. In the following section, this PT is co-integrated with the proposed system to experimentally evaluate the cold-startup capability under low excitation levels.

V. Measurement results

A. Experimental setup

The experimental setup is shown in Fig. 12. The split-electrode MEMS PT is placed on a shaker (LSD V406 M4-CE) excited by a sine wave signal at the natural frequency of the PT (219 Hz). The signal is generated from a function generator (Agilent Technologies 33250A) and amplified by a power amplifier (LDS PA100E). There are three signal wires connecting between the PT and the test chip, of which one is for the bottom electrode and the other two are for the two top electrode regions of the PT. The chip is fully self-powered with an on-chip voltage regulator and the experiment starts from the cold state, while both energy storage capacitors, C_S and C_{DD}, are out of charge. As previously explained, during the cold state, V_{DD} is not available and the SSHI circuit is not operating. Hence, the whole system simply works as a passive full-bridge rectifier (FBR). In addition, as the region 2 of the PT is disconnected from the system by default, the small region 1 can generate a high open-circuit voltage compared to using a monolithic electrode covering both the two regions.

Before measurements on the proposed cold-startup system, the MEMS PT is first characterized to show the increased open-circuit voltage from the region 1 compared to the regions 1+2. The measured open-circuit voltage levels are shown in Fig. 13. The results show that, when only region 1 is used, the open-circuit voltage is increased by more than 2×. This is a significant improvement since it implies that, when the proposed cold-startup SSHI circuit is employed, the required excitation level to start the whole system from its cold state is lowered by at least 50% while the system dynamically disconnects the region 2 during the cold state. For instance, the open-circuit voltage generated from the PT, V_{OC}, should be greater than $V_S + 2V_D$ in order to overcome the threshold set by the FBR. Assuming V_S needs to attain 1.5 V before the system can be started, it requires V_{OC} to be at least 2 V (since $V_D \approx 0.25$ V). Hence, for conventional SSHI interface circuits, the excitation level should be higher than 1.6 g, as shown in Fig. 13, to perform a cold-startup. However, the proposed system is able to start the system at 0.8 g, since only the region 1 is used and the open-circuit voltage from the region 1 attains 2 V at 0.8 g.

B. Cold-startup measurements

Fig. 14 shows the die photo of the proposed cold-startup SSHI interface circuit. The circuit was implemented in a 0.18 µm CMOS process. The active area of the proposed circuit together with the on-chip FBR is around 0.2 mm^2. The measurements are focused on how the circuit is started from its cold state. Hence, before the measurements, the remaining charge in the two energy storage capacitors, C_S and C_{DD}, is cleared to ensure that $V_S \approx 0$ V and $V_{DD} \approx 0$ V. These two capacitor are implemented off-chip and their capacitance values are $C_S = 100$ µF and $C_{DD} = 4.7$ µF.

Fig. 15 shows the measured waveforms of V_{PT}, SYN, $RDYH$ and CON, which are illustrated in the circuit schematics in Fig. 6a and Fig. 9a. The signal V_{PT} is the mathematical difference between the two nodes V_P and V_N. As the oscilloscope used in the measurements has only four channels, two oscilloscopes are employed to measure the voltage at five nodes. As seen in Fig. 15, the first three signals are obtained with the four channels of the first oscilloscope (at nodes V_P, V_N, SYN and $RDYH$) and last signal, CON, is obtained with the second oscilloscope. Three time markers are labeled in the figure: t_1, t_2 and t_3. At t_1, the voltage across the storage capacitor V_S is very low and the system is still in the cold state. Hence, the SYN, $RDYH$ and CON signals are low because there is no DC supply available in the system. The low SYN signal indicates that the voltage V_{PT} is not flipped using the SSHI circuit. The low $RDYH$ signal indicates that V_{DD} is not available as it does not yet attain its preset value 1.5 V. The low CON signals indicates that region 2 of the PT is not connected into the system in order to generate a higher open-circuit voltage from region 1. At the moment t_2, V_{DD} reaches 1.5 V and the voltage regulator block starts to regulate V_{DD} with the regulating signal $RDYH$. Once the regulating signal $RDYH$ is present, CON goes high to connect the region 2 of the PT into the system. CON also enables SYN signal to start to flip the voltage V_{PT}, hence, starting the SSHI circuit. The top outline of the signal V_{PT} equals to the voltage V_S+2V_D. After t_2, it can be clearly observed that V_S increases faster. This is due to the additional charge from region 2 of the PT and the operating SSHI circuit.

Fig. 16 shows the measured transient waveforms for short periods of time at moments t_1 and t_3, which are labeled in Fig. 15. In Fig. 16a, the SSHI is not started; hence, the system works as a FBR, which can be seen from the waveform of V_{PT}. During this period, SYN keeps low indicating the non-operating SSHI circuit and CON keeps low indicating that region 2 of the PT is not connected. In Fig. 16b, a stable V_{DD} is available to power the system; hence, the SSHI circuit is operating and the voltage V_{PT} is being flipped correctly at each rising edge of SYN. In addition, signal CON goes high to connect region 2 of the PT to the system.

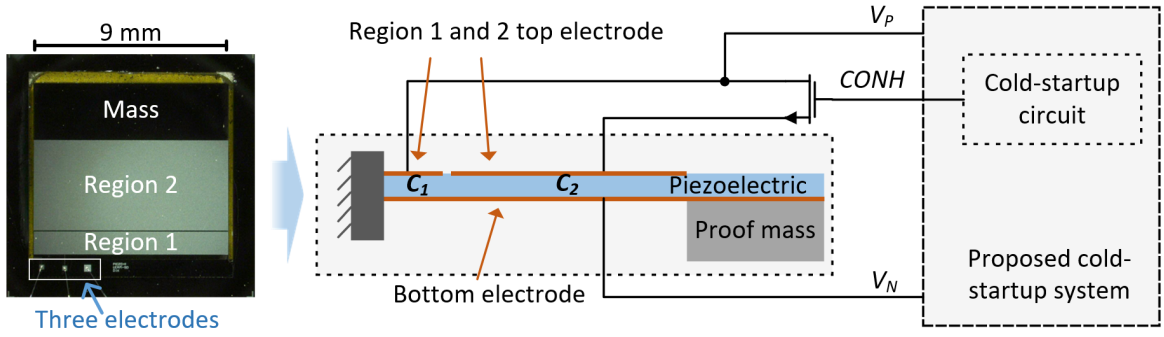


Fig. 11: Die photo and diagram of the MEMS PT connected to the proposed system during measurements.

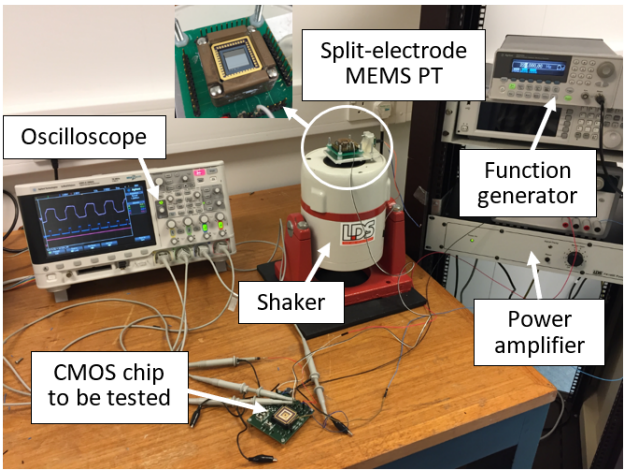


Fig. 12: Experimental setup.

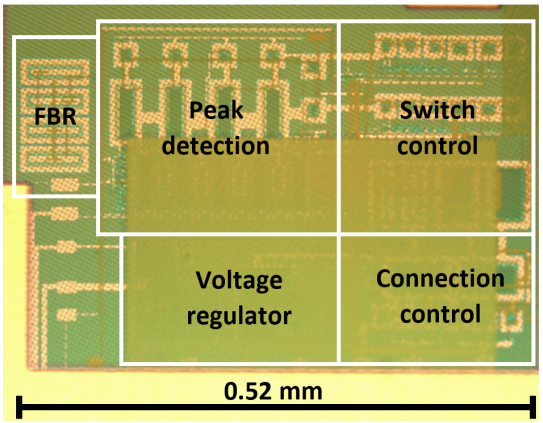


Fig. 14: Optical micrograph of the proposed circuit.

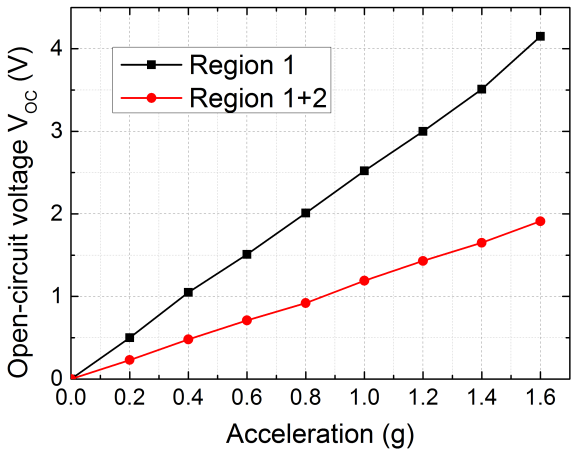


Fig. 13: Measured open-circuit voltage amplitude, V_{OC}, from only region 1 and from region 1+2.

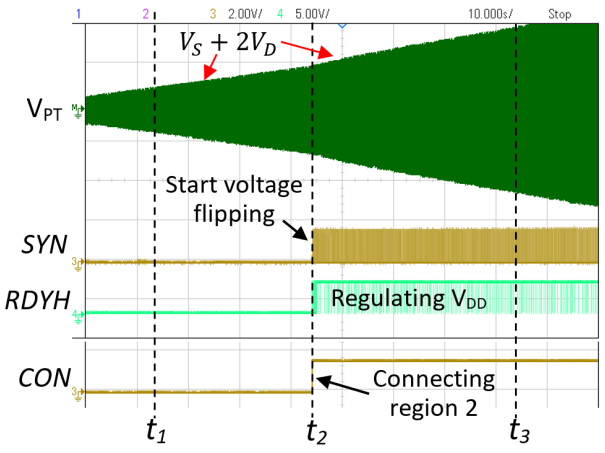
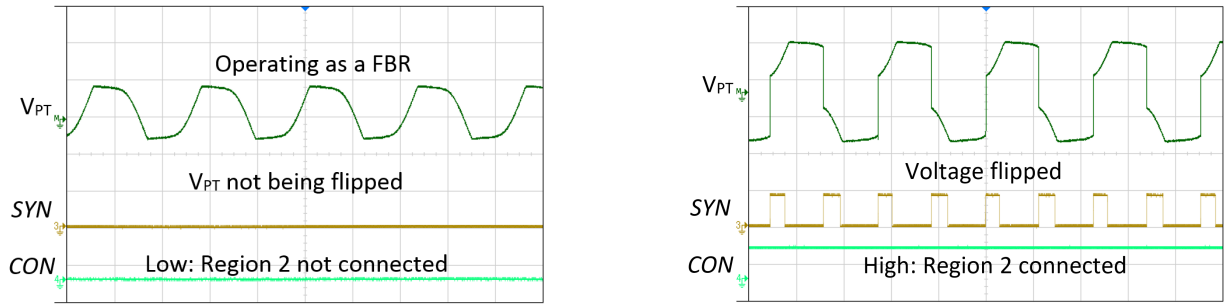


Fig. 15: Measured waveform starting from the cold state under 1.6 g acceleration level.

Fig. 17a shows the measured V_S for 100 s and the initial V_S is near 0 V. The excitation level is 1.6 g; hence, the corresponding open-circuit voltage amplitude for region 1 is around 4.2 V and that for regions 1+2 combined is around 2 V, which can be observed in Fig. 13. The experiments were performed with three inductor values for the SSHI circuit: 0.22 mH, 0.47 mH and 1 mH. The V_S values were noted every 5 s until 100 s. It can be seen from the figure that V_S increases slowly at the beginning until it achieves around 1.57 V at 45 s. This moment corresponds to the time instant t_2 labeled in Fig. 15, when the V_{DD} achieves its preset value and the SSHI circuit starts to operate. Hence, after 45 s, V_S increases faster than before. The output power transferred into C_S in this 100 s is shown in Fig. 17b. The values obtained in this figure are calculated from the measured V_S values in Fig. 17a by dividing the increased energy in C_S by 5 s. The increased energy in C_S can be calculated by $\Delta E = \frac{1}{2}C_S(V_S(n)^2 - V_S(n-1)^2)$. As seen from the figure, the power stays extremely low before the



(a) Waveforms at time t_1.

(b) Waveforms at time t_3.

Fig. 16: Measured waveforms before and after the circuit is started from its cold state at t_1 and t_3 respectively, corresponding to Fig. 15.

system is started since it works as a FBR in this case. After the SSHI is powered at $45\,\mathrm{s}$, the output power is significantly increased to higher values.

Additional measurements were performed by decreasing the vibration excitation level from $1.6\,\mathrm{g}$ to $1.0\,\mathrm{g}$, which corresponds to an open-circuit voltage from region 1 at $2.5\,\mathrm{V}$. From Fig. 13, it can be seen that the regions 1+2 can only generate an open-circuit around $1.2\,\mathrm{V}$ under $1.0\,\mathrm{g}$. In order to overcome the threshold set by a full-bridge rectifier (FBR), the open-circuit voltage amplitude should be greater than $V_S + 2V_D$. Hence, for a $1.2\,\mathrm{V}$ input voltage if the electrode of the PT is monolithic, V_S can only be charged to $0.7\,\mathrm{V}$ theoretically ($V_D \approx 0.25\,\mathrm{V}$). This low V_S value is not enough to generate a valid V_{DD} and start the system from the cold state. However, the proposed scheme can increase the open-circuit voltage to $2.5\,\mathrm{V}$ and eventually charge V_S to a high value to start the system. The measured V_S and output power over $200\,\mathrm{s}$ measurements is shown in Fig. 18. The V_S values shown in this figure were measured for every $10\,\mathrm{s}$ and the output power is calculated in a similar way as in Fig. 17b, but dividing the increased energy by $10\,\mathrm{s}$. Due to the lower excitation level, it takes around $130\,\mathrm{s}$ to charge V_S to start the system, which is much longer than the $45\,\mathrm{s}$ under $1.6\,\mathrm{g}$. However, it shows the capability of starting the system from cold state under an excitation level comparable to that of a conventional system, which cannot be started using a monolithic PT electrode.

In this implementation, the capacitance ratio between the two electrode regions (C_1 and C_2) was chosen at 1/4 and the results in Fig. 13 show that the open-circuit voltage from C_1 is approximately twice of the voltage from C_{1+2}. The percentage of C_1 can be chosen even smaller to increase the voltage generated from this region; however, this would decrease the power in this region and take longer time to start the system from the cold state. Hence, the trade-off on the percentage of C_1 should focus on the environmental excitation levels to enable the system to perform cold-startup operations in a short time period.

VI. Conclusion

This paper presents a new cold-startup SSHI interface circuit capable of starting the SSHI circuit from its cold-start under much lower excitation levels. A CMOS chip is designed and fabricated and a custom MEMS PT is co-integrated with the CMOS chip to experimentally evaluate the proposed interface circuit. In order to test the chip, the MEMS PT is designed to have its electrode split into two regions: one small high-strain region close to the clamped end and, one large low-strain region close to the free end. At the cold state, all energy storage devices in the system are not charged and there is no stable DC power supply for the SSHI circuit. Hence, the system works as a simple full-bridge rectifier (FBR) in this case. With the proposed cold-startup circuit, the system dynamically disconnects the low-strain region of the PT in order to increase the open-circuit voltage generated only in the high-strain region. Due to the high voltage generated from this region, the proposed system can be easily started under much lower excitation levels. After the SSHI circuit is started with a valid power supply V_{DD}, the system dynamically enables the low-strain region to further improve the power performance due to the additional charge generated in this region and the operating SSHI circuit. The experimental results show that the proposed system can be started from its cold state under a much lower excitation level compared to conventional energy harvesting interfaces. The required excitation level to start the proposed system is lowered by 50% compared to a conventional SSHI interface.

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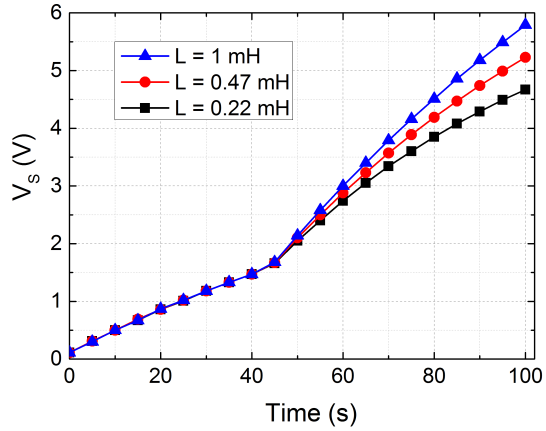
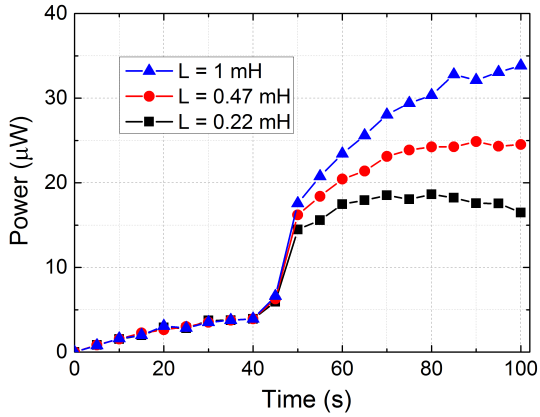
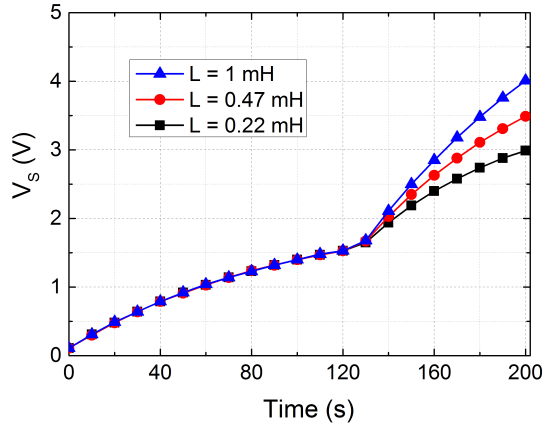


(a) V_S.

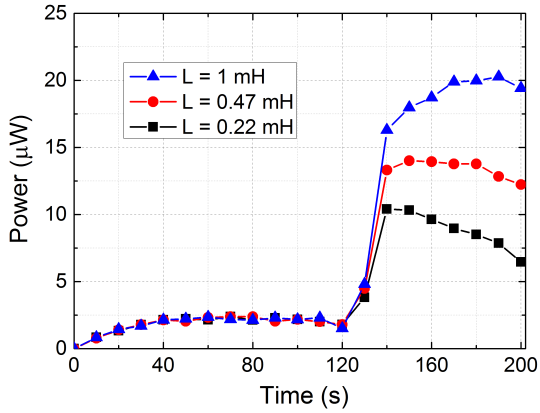


(b) Output power.

Fig. 17: Measured V_S and output power in 100 s under 1.6 g excitation.



(a) V_S.



(b) Output power.

Fig. 18: Measured V_S and output power in 200 s under 1.0 g excitation.

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