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Centralised Busbar Differential and Wavelet-based Line Protection System for MTDC grids, with practical IEC-61869-compliant Measurements

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Abstract: This paper presents a method for discriminative detection of DC faults on VSC-powered multi-terminal HVDC transmission systems using two fundamental guiding principles, namely instantaneous current-differential and travelling waves. The proposed algorithm utilises local voltage and current measurements from all transmission lines connected to a DC busbar, and current measurement from the DC side of the converter. The scheme operates at a sampling frequency of 96 kHz which conforms with IEC 61869-9. No long distance communication is involved while measurements and signal exchange within DC substations are enabled by the utilisation of IEC 61850. Performance is assessed firstly through detailed transient simulation, using verified models of modular multi-level converters, hybrid DC circuit breakers and inductive DC-line terminations. Furthermore, practical performance and feasibility of the scheme is evaluated through laboratory testing, using the real time Opal-RT hardware prototyping platform. Simulation and experimental results demonstrate that the proposed protection algorithm can effectively, and within a very short period of time (i.e. less than 1 ms), discriminate between busbar and line faults (internal faults), while remaining stable during external faults. Additionally, it has been demonstrated that IEC 61869-9 is suitable for enabling fast DC protection schemes incorporating travelling waves.

1 Introduction

High Voltage Direct Current (HVDC) networks, utilising Voltage Source Converters (VSCs) are expected to become the preferred technology for connecting renewable generation over long distances [1] and also for upgrading and interconnecting existing AC systems. This is due to the fact that such systems offer improvements in terms of system stability, lower cost and operational losses. A natural extension of the existing point-to-point HVDC transmission technology is a Multi Terminal Direct Current (MTDC) system, which utilises more than two VSC stations, effectively forming a DC grid. Such configuration can provide further technological and economic advantages. Consequently, it is essential to study, analyse and address potential challenges imposed by MTDC systems to enable widespread adoption. One of the main challenges associated with HVDC systems is to detect and isolate DC-side faults which leads to the development of protection systems.

For the implementation of non-communication-based schemes (i.e. non-unit), there is a noteworthy trend towards the placement of DC reactors at both ends of transmission lines. The intentional placement of such inductive components reduces the rate of rise of DC current, while it changes the resulting DC voltage signatures. The fact that voltage is different, depending on the faulted line, can assist towards the implementation of a discriminative protection system. This is achieved by utilising under-voltage and voltage derivative criteria [2–4] or ratio of transient voltages [5].

A few other methods are proposed by utilising current measurements [6] or handshaking methods [7] to achieve discriminative and fast detection of DC-side faults.

The analysis of travelling waves has also been found to be useful for developing protection schemes. The scheme reported in [8] utilises Wavelet Transform of DC voltage to detect and discriminate between different faults. The voltage and current derivative has also been used to further enhance the performance of the scheme during close-up terminal faults. The method proposed in [9] is based on voltage and current measurements and uses a two-stage approach to detect faults in MTDC networks. The first stage is fault incident detection which is performed based on travelling waves detected by Wavelet Transform. The second stage is to locate the fault by a fault locator element which functions based on current harmonic contents.

A number of differential-based schemes can also be found in the technical literature. These are mainly based on current measurements from both line ends, which are used to perform Discrete Wavelet Transform (DWT) [10] or for the calculation of differential current and comparison with a constant predefined threshold [11]. In [12], a high-speed differential scheme is proposed based on a network of distributed current sensors along eith the transmission line. The proposed approach has been found to be fast, sensitive and reliable for solid and highly resistive internal faults, while maintaining stability during external faults.

1.1 Contribution of the Proposed Scheme

A review of existing MTDC protection techniques leaves the impression that much of the reported research focuses on the conceptual aspects but neglects important practical facets such as sampling frequency, time window and breaking capacity, and time response of DC interruption devices. Most importantly, there is no discussion or studies on the practical feasibility of the schemes, and the way measurements and signals exchange can be implemented locally (either on a line or busbar) or within a DC substation [13]. Taking into account the requirement of fast DC protection, all above-mentioned issues play a significant role in the physical implementation of any protection scheme. Accordingly, this paper proposes a new primary protection system, suitable for rapid and discriminative fault detection and isolation in MTDC grids. The proposed scheme is designed

to detect both busbar and line faults within an MTDC grid, as a centralised protection solution [14], complying with IEC 61869-9 [15] and IEC 61850 [16]. The design, practical feasibility of the scheme and case studies, have also been validated using hardware prototyping and comprehensive laboratory testing. Moreover, it should be also highlighted that even though IEC 61869-9 has promoted the sampling frequency of 96 kHz for DC applications, its performance and suitability for DC protection has not been studied and reported in open literature (neither practically nor simulation-based). Consequently, another significant contribution of the present work is the utilisation and examination of IEC 61869-9 with regard to DC protection applications.

2 Proposed Protection Scheme

2.1 Algorithm and Scheme Outline

The centralised protection scheme presented in this paper requires voltage and current measurements from all transmission lines and the converter attached to a DC busbar, as depicted in Fig. 1.

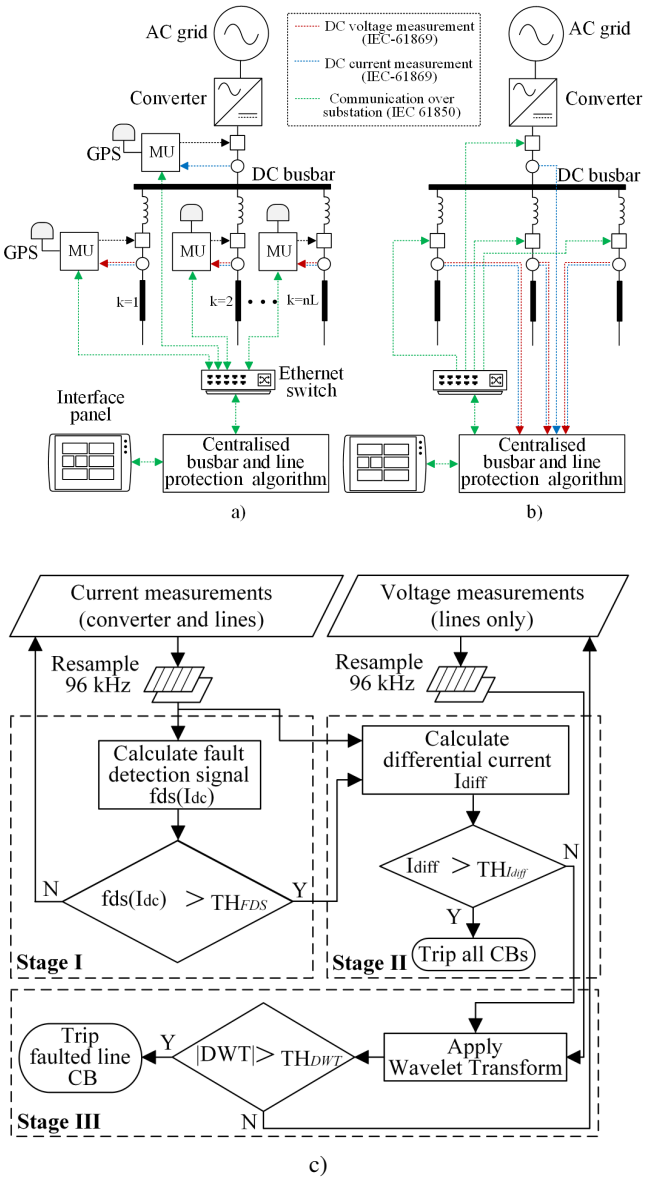

Fig. 1: Overview of protection scheme.
a Merging unit with GPS.
b Direct wiring.
c Protection algorithm.

There are two major options for the practical implementation of the proposed scheme. The first option (see Fig. 1.(a)) utilises Merging Units (MUs) to digitise local DC voltage and current measurements and transmit them, including a timestamp, to the centralised protection system using the IEC 61850-9-2 Sampled Value (SV) protocol. Time synchronisation is shown as being achieved using Global Positioning System (GPS) receivers, but other methods, such as using IEEE 1588, to synchronise devices over the Ethernet network could be used instead. IEC 61850-8-1 GOOSE messaging would be used to transfer tripping signals to CBs. In the second option (see Fig. 1.(b)), direct wiring of DC measurements to the centralised protection system is adopted. In this case, GOOSE messaging and the corresponding communication infrastructure is used only for tripping signals. The first option is particularly appropriate for larger substations, where the distance between the measurement locations and the central controller prohibits the use of analogue signalling. In this paper, the first option has been assumed. It should be noted that measurements are not required to be transferred between substations.

The algorithm consists of three stages as illustrated in Fig. 1(c) which are explained in detail in the following subsections.

2.2 Stage I: Fault Detection

The initial stage of operation is where the fault incident is detected using all the currents from the converter and the lines attached to the same busbar. Using a moving ten-sample window W, for each current I_{dc}, a fault detection signal $fds(I_{dc})$ is calculated as defined by equation (1).

$$fds(I_{dc}) = \frac{1}{n_s/2-1}\sum_{k=1}^{n_s/2}(W_k - \mu_{W_k})\cdot(W_{k+n_s/2} - \mu_{W_{k+n_s/2}}) \quad (1)$$

where $n_s = 10$ is the measuring window length in samples, W_k are the individual samples contained in W, and the mean values μ_{W_k} and $\mu_{W_{k+n_s/2}}$ are calculated for the two adjacent five-sample half-windows W_1 and W_2 included in W (as illustrated in Fig. 2).

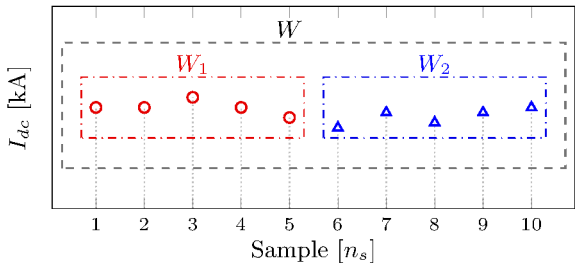

Fig. 2: Ten-sample measuring window with two five-sample sub-windows W_1 and W_2 used the calculation of the fault detection signal.

2.3 Stage II: Busbar Fault Detection

In this stage, the protection algorithm determines whether the fault is on the busbar or on one of the lines. This is achieved by calculation of the differential current I_{diff} utilising converter and line current measurements, as expressed in (2).

$$I_{diff} = \sum_{k=1}^{n_L} I_{dc-Line,k} + I_{dc-Conv} \quad (2)$$

where n_L is the number of lines connected to the busbar (as illustrated in Fig. 1), $I_{dc-Line,k}$ is the current in line k; and $I_{dc-Conv}$ is the converter output current.

During line faults the locally-calculated busbar differential current is expected to be theoretically close to zero while for busbar faults it should obviously reach high values. The presence of a busbar fault is perceived by comparing the differential current with a threshold $TH_{I_{diff}}$. If such threshold is exceeded, then a busbar fault is deemed to exist and all CBs connected to the busbar will be tripped and the algorithm will terminate at this point; otherwise, algorithm proceeds to Stage III, considering that the fault is present on one of the connected lines.

2.4 Stage III: Faulted Line Selection

This is the final stage of the protection algorithm where the faulted line(s) are detected by observing travelling waves on the voltage measurements. This is achieved by applying DWT to voltage waveforms captured on the line side of the current-limiting inductor (for each line separately).

The wavelet transform of a function $v(t)$ can be expressed as the integral of the product of $v(t)$ and the daughter wavelet $\Psi^*_{a,b}(t)$ as per following equation:

$$W_\psi v(t) = \int_{-\infty}^{\infty} v(t) \underbrace{\frac{1}{\sqrt{\alpha}}\Psi\left(\frac{t-b}{a}\right)}_{\text{daughter wavelet } \Psi^*_{a,b}(t)} dt \tag{3}$$

The daughter wavelet $\Psi^*_{a,b}(t)$ is a scaled and shifted version of the mother wavelet $\Psi_{a,b}(t)$. Scaling is implemented by α which is the binary dilation (also known as scaling factor) and shifted by b which is the binary position (also known as shifting or translation).

Two categories of wavelet transform can be distinguished: Continuous Wavelet Transform (CWT) and Discrete Wavelet Transform (DWT). The difference lies upon the resolution of binary dilation α and binary position b. In DWT, they move discretely in dyadic blocks. Specifically, α and b, can only take values of the power of two as expressed in set of equations (4).

$$\begin{cases} \alpha_L = 2^L, \ (\alpha_0 = 2^0 = 1, \alpha_1 = 2^1 = 2, ...) \\ b_L = 2^L N, \ (b_0 = 2^L 0 = 0, b_1 = 2^L 1 = 2^L, ...) \end{cases} \tag{4}$$

where L is the level of decomposition, and N is the sample index.

The selection between CWT and DWT is a trade-off between time accuracy of the wave detection, and processing resources and their associated time delays [17]. In the case of CWT, the daughter wavelet can be positioned smoothly over the signal, hence the accuracy of the wave time detection is higher than for DWT techniques. This is the reason that CWT is preferred for fault location applications [18], where the computational time is not crucial. However, DWT is computationally more efficient [17], which enables faster wave detection. As a result, DWT is considered more suitable for power system protection applications [19]. Therefore, for the studies carried out in this paper, DWT is the chosen technique.

The key to discrimination of the faulted line lies in the inductive termination of each line. When a fault occurs on one of the busbar-connected lines, the voltage measured at the line side of the inductor will be subjected to a severe depression; and, hence the DWT is expected to reveal sharp edges and possess high magnitude. The voltage change measured on the healthy lines is expected to be more gradual due to the inductances included in the fault current path from one healthy line, through the busbar, to the faulted line. As a result, travelling waves calculated using DWT will be attenuated both in sharpness and magnitude compared to those on the faulted line. Such differences allow for a reliable discrimination of the faulted lines. In particular, faulted line is identified by comparing the calculated DWT magnitude with a predefined threshold TH_{DWT}. Once such threshold is exceeded, a tripping signal is sent to the corresponding CB.

It is anticipated that in case of fault, power converters will turn-off the IGBTs for self protection at some stage. However, any control action from the converter should not affect the proposed protection scheme due to the fact that Stage I and II are primarily dependent on the inrush current introduced by the discharge of system capacitance. This is a fast transient which takes place before the converter IGBTs are turned off. Moreover, Stage III is based on travelling waves phenomenon which is mainly determined by the parameters of the line, and therefore, is very much independent of the power source (especially during the first ms of the fault).

2.5 Selecting Thresholds and Wavelet

As described in the previous subsections, the sensitivity and stability of the proposed scheme is determined by the three thresholds TH_{FDS}, $TH_{I_{diff}}$ and TH_{DWT}, which are compared against the fault detection signal, differential current and DWT respectively. This section elaborates on the procedure of selecting appropriate values for these thresholds.

Firstly, regarding the fault detection signal threshold TH_{FDS}, the following equation (5) has been used:

$$TH_{FDS} \leq \frac{C_{min} \cdot dV_{cap}^{min}}{t_s \cdot n_s^2} \tag{5}$$

where C_{min} is the minimum capacitance expected to discharge during the fault, dV_{cap}^{min} is the expected minimum voltage drop across the capacitance C_{min}, t_s is the sampling frequency, and n_s is the number of samples used in calculating fault detection signal.

Equation (5) has been derived based on the fact that a capacitive current (generated by the discharge of the minimum capacitance C_{min}) should be captured within the fault detection signal measuring window (i.e. n_s = 10 samples). The average value of such discharging current over the time window sets the maximum value of TH_{FDS} and ensures that in case of a fault, the resulting $fds(I_{dc})$ will exceed TH_{FDS}.

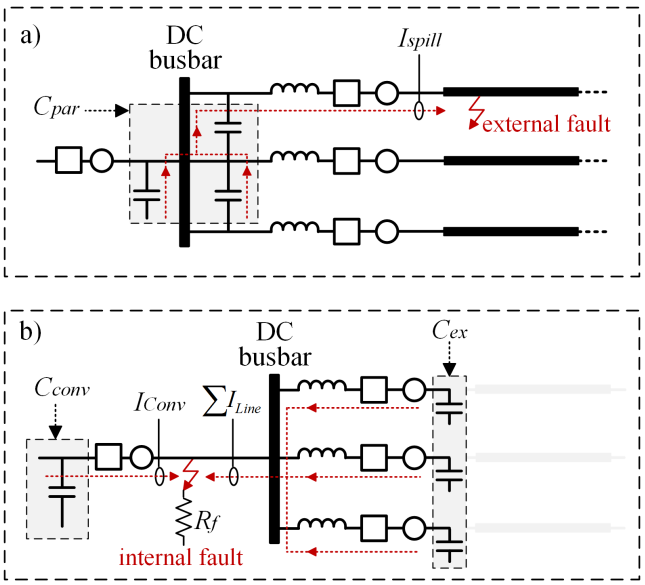

Fig. 3: Illustration of faults currents for threshold selection.
a Illustration of spill current during external line fault.
b Illustration of fault currents during internal busbar fault.

For explaining the procedure of selecting the threshold $TH_{I_{diff}}$, the circuits depicted in Fig. 3 are utilised. For the differential protection to operate correctly, two main criteria should be fulfilled. Firstly, for protection security purposes the threshold $TH_{I_{diff}}$ needs to be higher than the spill current I_{spill} generated during external faults. As illustrated in Fig. 3(a), a spill current I_{spill} is produced by the discharge of combined shunt capacitance C_{par} during external line faults. This capacitance is formed between the live conductors, includes additional lumped circuits (e.g. resistive-capacitive DC voltage transformers), and any other capacitance formed between

the substation components and earth. The spill current I_{spill} can be approximated by the following equation (6):

$$I_{spill} = C_{par}\frac{dV_{C_{par}}}{dt} \tag{6}$$

where $dV_{C_{par}}/dt$ is the expected (or estimated) maximum value of the rate-of-change of voltage across the shunt capacitance C_{par}.

Secondly, to ensure differential protection dependability, the directed sum of all busbar currents (i.e. the differential current) should be higher than $TH_{I_{diff}}$, even for the worst case highly-resistive faults. For the first ms of the fault, a high burst differential current is formed by the discharge of capacitance C_{conv} and C_{ext} as illustrated in Fig. 3(b). The term C_{conv} represents the equivalent capacitance of the converter and C_{ext} is the total external capacitance of the neighbouring feeders. The algebraic sum of all busbar currents can be estimated as follows:

$$\sum I_{Line} + I_{Conv} = C_{par}\frac{dV_{C_{conv}}}{dt} + C_{ext}\frac{dV_{C_{ext}}}{dt} \tag{7}$$

where $dV_{C_{conv}}/dt$ and $dV_{C_{ext}}/dt$ are the expected (or estimated) minimum rate-of-change of voltage across the converter and external capacitance C_{conv} and C_{ext} respectively.

Taking into account the above analysis for internal and external faults together with the associated equations (6) and (7), the following equation (8) sets the range of acceptable values for $TH_{I_{diff}}$.

$$k_{sf} \cdot I_{spill} < TH_{I_{diff}} < \left(\sum I_{Line} + I_{Conv}\right) \tag{8}$$

It can seen that spill current is multiplied by a safety factor k_{sf} to reduce the possibility of spurious tripping. The selection of thresholds for fault detection signal and differential current depends on the approximation of capacitive currents during the first ms of the fault. This is due to the fact that the proposed scheme is designed as a primary protection system and hence high speed of operation is required. The analysis requires the expected or estimated rate-of-change of voltage on capacitive elements which should take into consideration highly resistive pole-to-ground faults as explained in [20].

Regarding the selection of thresholds related to DWT, the following impedances need to be estimated: i) impedance seen from the point of measurement to the remote end of the protected line, and ii) impedance seen from the point of measurement to the nearest point outside the protected line. The analysis should include the highest considered fault resistance R_f, as it will affect the resulting amplitude of travelling waves. The estimated impedance can be used to calculate the corresponding transfer function with regards to voltage. The frequency response of each transfer function should provide sufficient margin for successful internal/external fault discrimination. As the lines are terminated by lumped inductors (with inductance being much higher than that of the lines) there is a significant attenuation boundary for high frequency travelling waves resulting from external faults. For further insight on the selection of DWT related thresholds the literature in [19, 21] provides a useful guidance.

To satisfy the requirements of both sensitivity and stability, in the case studies included in section 3, the thresholds have been established following the above guidelines, with the assumed sensitivity to highly resistive faults up to 500 Ω, and taking into account known system capacitances (i.e. lines and converter). The resulting thresholds were: TH_{FDS}=43.5 A, $TH_{I_{diff}}$=75 A and TH_{DWT}=1000. Those thresholds have also been verified by systematic search routines, using multiple simulations and post-processing, and have been found to be appropriate for the proposed protection scheme. With regards to DWT tuning, the second, third and fourth scales have been tested (the first scale has been omitted since it corresponds to the highest frequency band, and due to undesirable noise-related effects it was considered unsuitable [21]). For the needs of proposed scheme the second scale has been ultimately selected. Based on orthogonal wavelets the high and low order frequency coefficients have been set to $K_{hf} = \{0, -0.1768, 0.3536, 1.0607, 0.3536, -0.1768\}$ and $K_{lf} = \{0, 0.3536, -0.7071, 0.3536, 0, 0\}$ respectively.

2.6 Measurement and communications delays within DC substation

It is important to ensure that the proposed method will operate correctly, despite delays from a realistic implementation. Assuming the use of MUs as illustrated in Fig. 1, the maximum delay, t_d, to be expected from the measurement and communications can be calculated as follows:

$$t_d = t_s + t_{MU} + t_n + t_{cc} \tag{9}$$

where t_s is the maximum delay due to analogue sampling (i.e. $t_s = 1/96\ \text{kHz}^{-1} = 10.42\ \mu s$), t_{MU} is the processing time in the MU (i.e. the time to encode the SV frame), t_n is the total maximum Ethernet network latency, and t_{cc} is the processing time for the central controller (i.e. the time to decode the SV frame). The size of the SV Ethernet frame would be 64 bytes (the minimum frame size) because a maximum of two DC values are digitised within the dataset which would require only 58 bytes, including overhead and quality values [22]. As suggested by IEC 61869-9, a dedicated 1 Gbps Ethernet network is assumed, and therefore t_n is composed of: the data transmission time for two Ethernet links (i.e. $2 \times 0.7\ \mu s$), the switch processing delay (assumed to be $1\ \mu s$), and jitter associated with queuing due to other traffic. These could include IEEE 1588 frames and data from other measurement locations; assuming a maximum of four simultaneous competing frames and a transmission delay of $0.58\ \mu s$ per frame [23], the maximum queuing delay is $4 \times 0.58\ \mu s$. t_{MU} and t_{CC} can be estimated as $12\ \mu s$ and $9.5\ \mu s$, respectively, based on the measurements in [24] for approximately double the frame size, but this depends on the performance of the platform. Combining all of these factors, the worst case delay can be estimated as:

$$t_d = 10.42 + 12 + (1.4 + 1 + 4 \times 0.58) + 9.5 = 36.64\ \mu s \tag{10}$$

Further delays are introduced by the protection system and they arise from the window-based processing required by the fault detection signal calculation and DWT. Time delay t_{df} associated with the window-based processing is given by

$$t_{df} = (N_W - N_{WO}) \cdot t_{si} \tag{11}$$

where N_W is the length of the processing window in samples, N_{WO} is the amount of window overlap between two consecutive calculations frames, and t_{si} the sampling period of the input signal. Since a ten-sample time window has been used with a nine-sample overlap, and considering 96 kHz as the sampling frequency, the total time delay t_{df} is $10.42\ \mu$s. It should be highlighted that since the DWT and fault detection signal use different processing windows which run in parallel, there is no additional queuing of the voltage and currents measurements. As such, the value $10.42\ \mu s$ is not subjected to any additional delays.

2.7 Discussion on fault detection techniques

Due to the fast nature of DC-side faults there is a need for very fast protection systems in terms of both, fault detection and current interruption. Academic research on HVDC protection has provided a plethora of fast operating fault detection techniques [**?**] in recent years. It needs to be stressed that selection of the optimal method including its corresponding characteristics (e.g. sampling frequency and time window length) is not a trivial task due to the variety of influencing factors involved, such as network architecture, performance of measuring and sensing equipment, time response of HVDC breakers, and many others. Although such detailed considerations stretch beyond the scope of this paper it needs to be noted here that

further work is needed to develop specific guidelines for the optimisation of various elements of HVDC protection schemes, including fault detection stage.

3 Simulation Results

3.1 MTDC Study Network

For the purposes of validating the proposed protection scheme, a five-terminal HVDC grid model illustrated in Fig. 4 has been developed in Matlab/Simulink®. The network architecture is an enhanced version of a network from the Twenties Project case study on DC grids. There are five modular multi-level converters (MMCs) in the network operating at ± 400 kV (in symmetric monopole configuration), current-limiting inductors and hybrid circuit breakers (HbCBs).

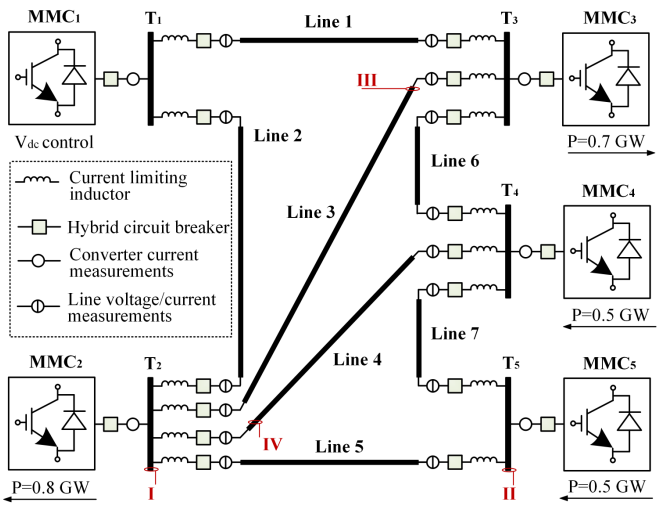

Fig. 4: MTDC case study grid.

The MMC models utilised in this paper are identical to those used in [1, 12, 25, 26] and the AC-DC network parameters are presented in Table 1. The lines have been modelled using a distributed parameter model. The HbCB is modelled by adopting a hybrid concept by ABB as reported in [27] (2 ms operation time with a maximum breaking current of 9 kA).

Table 1 Parameters for AC and DC network

Parameter	Value
AC voltage $[V_{AC}]$	400 [kV]
AC frequency $[f_{AC}]$	50 [Hz]
AC short-circuit level $[SCL]$	40 [GVA]
DC voltage $[V_{DC}]$	800 [kV]
DC line inductor $[L_{DC}]$	150 [mH]
MMC arm inductor $[L_{arm}]$	0.1 [p.u.]
MMC number of cells per arm	400
Line lengths (Lines 1 to 7)	300, 200, 600, 180, 150, 120, 100 [km]

3.2 Fault Scenarios

This section presents simulation results which quantify the overall performance of the proposed protection scheme under different fault scenarios, including pole-to-pole faults (PPFs), pole-to-ground faults (PGFs) (incorporating highly resistive faults) and busbar faults. In all scenarios the faults are permanent and are triggered at $t = 0.5$ ms, and the measurements have been contaminated with white noise to account for possible effects due to measurement-related noise on the protection response.

Table 2 Fault scenarios

Scenario	Description
I	PPF at busbar T_2 ($R_f \approx 0\ \Omega$)
II	PPF at busbar T_5 ($R_f \approx 0\ \Omega$)
III	PGF at Line 3 (590 km from T_2, $R_f = 500\ \Omega$)
IV	PPF at Line 4 (5 km from T_2, $R_f \approx 0\ \Omega$)

It is assumed that the assessed protection scheme is placed at terminal T_2. A selection of representative test cases have been included here (summarised in Table 2 and also depicted on Fig. 4) which demonstrate the worst case scenarios in terms of stability and sensitivity of the scheme. In recognition of page length limits, for fault scenarios II, III and IV, differential current I_{diff} and tripping signals are not depicted. However, the response of the protection system is fully summarised in Table 3. It should be noted that the counter for the calculation tripping time included in Table 3, is set after the arrival of voltage and current travelling waves (i.e. after the fault is 'seen' at DC terminals).

3.3 Fault scenario I

This fault scenario illustrates the protection performance under a busbar fault. Fig. 5(a) shows there is a rapid increase in the current from the converter immediately after the fault.

This is due to the discharge of the capacitance in the converter's sub-modules (prior to IGBT blocking). There is also a current infeed from the connected lines (Lines 2, 3, 4 and 5) but their rate of rise is limited because of the inductive terminations. As a result, there is a rapid increase in $fds(I_{dc})$ (Fig. 5(b)), which satisfies Stage I (fault detection) of the protection algorithm.

The rapid increase in current infeed from both the converter and the lines, results in the rapid rise of differential current I_{diff} as shown in Fig. 5(c). This satisfies Stage II (busbar fault detection) of the protection algorithm and is followed by the tripping of all the HbCBs (Fig. 5(d)), after which the algorithm terminates.

3.4 Fault scenario II

This fault scenario is designed to demonstrate the stability of the protection system during external faults (i.e. faults on remote lines or busbars). A solid external fault at the remote end of the shortest line (i.e. Line 5: 150 km) is applied on terminal T_5. The performance of the protection system located at terminal T_2 is depicted in Fig. 6.

Approximately 0.7 ms after the fault occurrence (which corresponds to the propagation delay along Line 5) a change in the DC currents can be observed both in the converter output and the lines (Fig. 6(a)). This results in an increase in $fds(I_{dc})$ (Fig. 6(b)), especially for Line 5. This satisfies the Stage I criterion (fault inception) and the algorithm will proceed to Stage II (busbar fault detection). The differential current I_{diff} would remain at an extremely low level, and consequently the algorithm will proceed to Stage III (line fault detection). As illustrated in Fig. 6(d), there is no visible transient observed in DWT magnitude. Since the voltage change is measured on the healthy lines, the DWT is extremely attenuated both in sharpness and magnitude. Therefore, there is no tripping signal initiated for any of the CBs at terminal T_2 (see Table 3), i.e. the scheme is stable during this worst case external fault.

3.5 Fault scenario III

In this scenario, the sensitivity and discrimination of the protection scheme is demonstrated. As shown in Fig. 7, after the fault occurrence, there is a current increase not only from the converter but also from the lines (Fig. 7(a)). Similarly, due to the inductive terminations, the rate of rise of current in the healthy lines is limited.

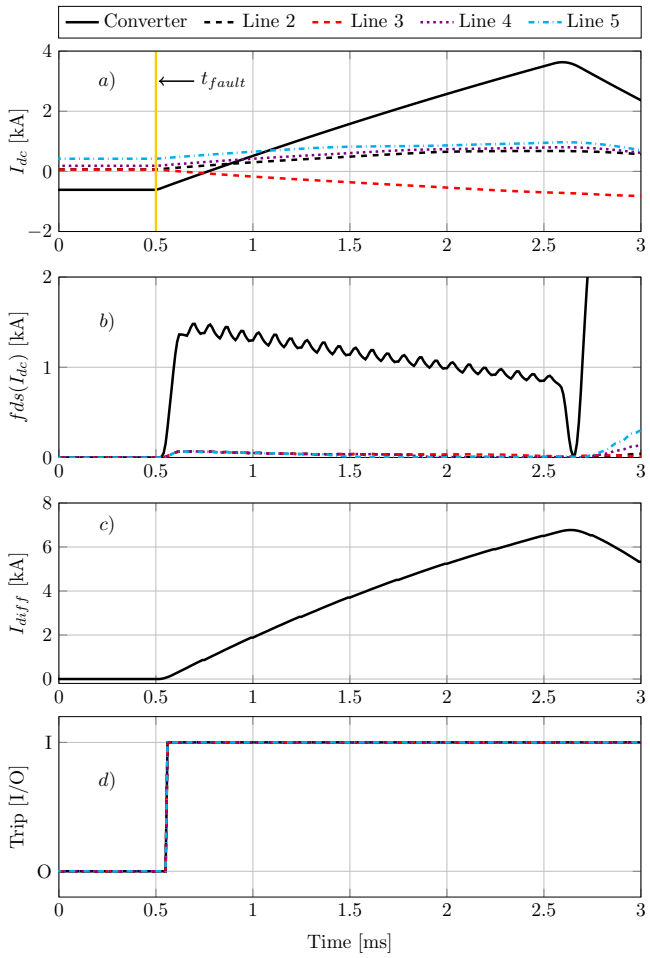

Fig. 5: Response of T_2 protection system for fault scenario I.
a Converter and line DC currents.
b Converter and line DC current fault detection signal.
c Differential current at busbar T_2.
d Tripping signals for each CB connected to T_2.

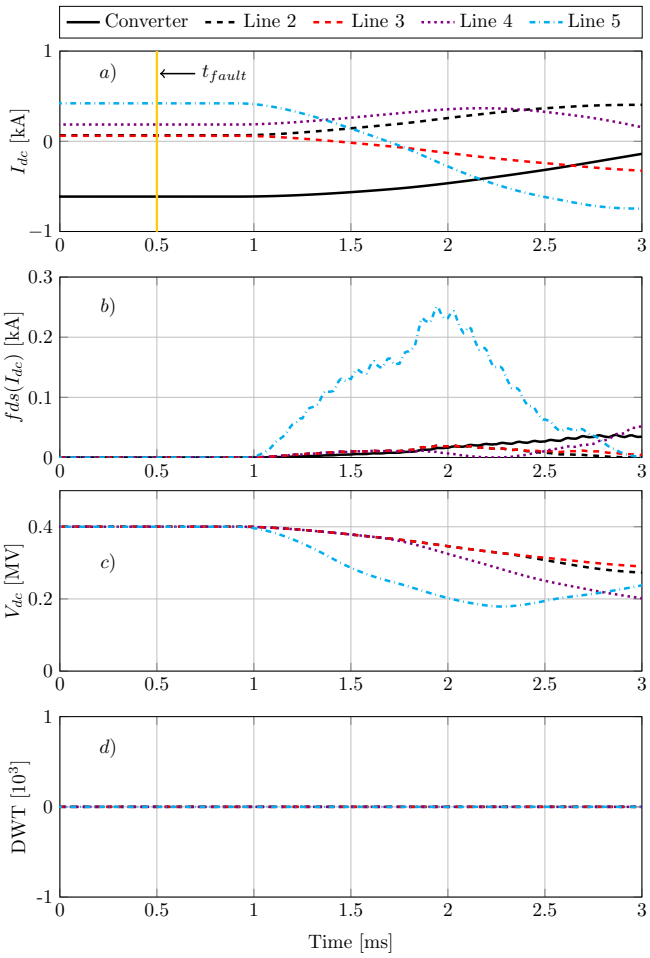

Fig. 6: Response of T_2 protection system for fault scenario II.
a Converter and line DC currents.
b Converter and line DC current fault detection signal.
c Line DC voltages.
d DWT magnitude of line voltages.

Moreover, it can be noted that there is a time delay t_{prop} corresponding to the electromagnetic propagation speed and distance to the fault on Line 3. After approximately 2 ms, the value of $fds(I_{dc})$ of the currents (especially from Line 3) increase to high values and the criterion of Stage I is satisfied.

The algorithm proceeds to Stage II, where the differential current I_{diff} is calculated. Since the values of differential current I_{diff} would remain close to zero, the algorithm proceeds to Stage III considering the presence of a line fault. As can be seen in Fig. 7(c), the voltage of the faulted line (i.e. Line 3) shows a relatively steeper transient phenomena (i.e. travelling waves). Such transients cannot be seen in the healthy lines, since they are attenuated by the inductive terminations. Another reason is that the voltages are captured on the line-side of the current-limiting inductors. The difference becomes more pronounced when the DWT is executed as shown in Fig. 7(d). It is evident that the faulted line can be discriminated using the magnitude of DWT, as its value is three orders of magnitude greater than those obtained from the healthy lines. This will results in selective tripping of CBs connected to Line 3 (see Table 3).

3.6 *Fault scenario IV*

In this scenario, the discrimination of the protection scheme for close up faults is demonstrated. It can be seen that approximately 0.1 ms after the fault there is an increase in $fds(I_{dc})$ (Fig. 8(b)) and significant voltage depression on faulted Line 4 (Fig. 8(c)). The resulting DWT reaches extremely high values (Fig. 8(d)), which ultimately results in selective tripping CBs connected to Line 4.

The results in selective tripping of the HbCB corresponding to the faulted line can be seen for all fault scenarios in Table 3.

Table 3 Summary of T_2 protection responses to fault scenarios I, II, III an IV

Fault scenario	Tripped components	Tripping time t_{trip}
I	MMC_2, Line 2, Line 3, Line 4, Line 5	0.1025 ms
II	MMC_5, Line 5, Line 7	0.1003 ms
III	Line 3	0.1219 ms
IV	Line 4	0.1131 ms

The tripping time t_{trip} included in Table 3 is established as:

$$t_{trip} = t_{resp} + t_{d-tot} \tag{12}$$

where t_{resp} is the response of the protection system and t_{d-tot} the total time delay. As such, based on equation 12 one can deduce the actual response time of the protection algorithm.

3.7 *Impact of Sampling Frequency*

In order to investigate the impact of sampling frequency on the protection performance, fault scenario IV has been repeated for different sampling frequencies. The summary of the protection responses is presented in Table 4. It is evident for the frequencies below 60 kHz protection has failed to operate correctly due to the failure of Stage

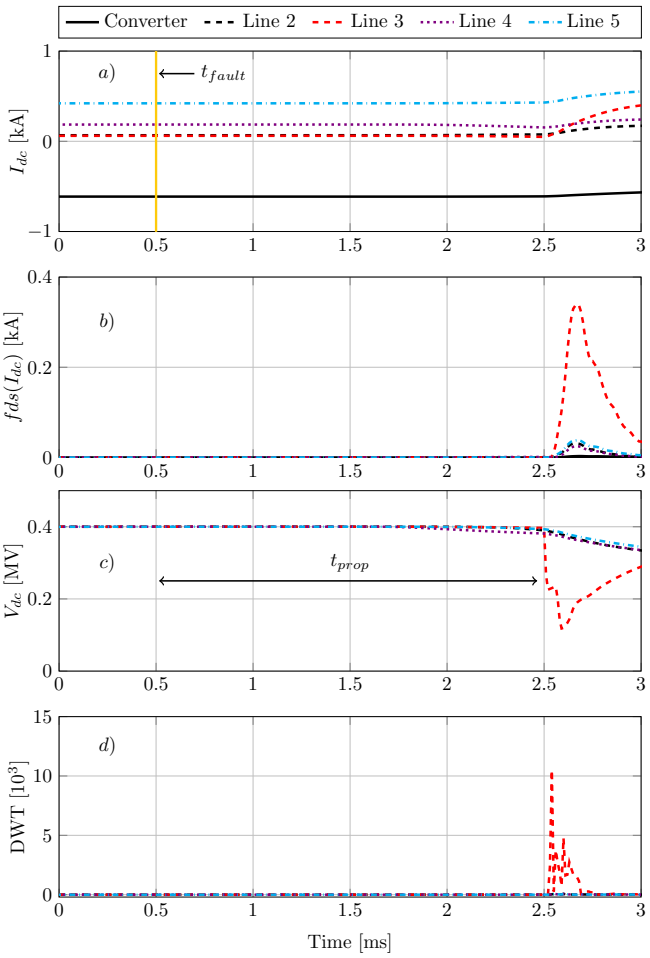

Fig. 7: Response of T_2 protection system for fault scenario III.
a Line and converter DC currents.
b Line and converter DC current fault detection signal.
c Line DC voltages.
d DWT of line voltages.

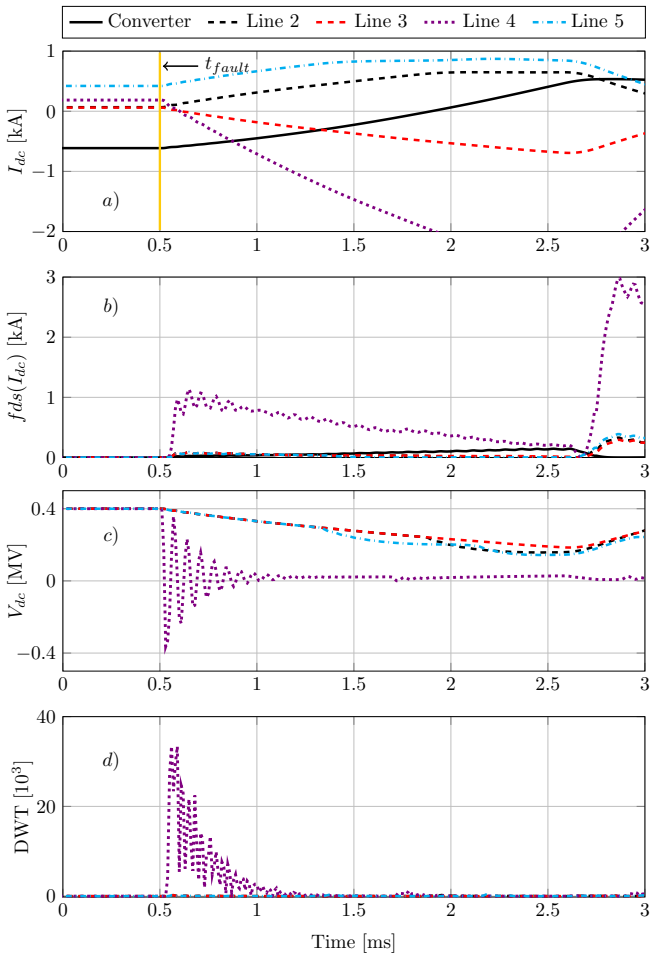

Fig. 8: Response of T_2 protection system for fault scenario IV.
a Line and converter DC currents.
b Line and converter DC current fault detection signal.
c Line DC voltages.
d DWT of line voltages.

III (faulted line discrimination). The correct discriminative operation of the proposed scheme relies on the correct, accurate and fast detection of travelling waves which evidently requires an adequate sampling frequency. Consequently, the recommendation of 96 kHz in IEC-61869 provides enough confidence for the correct and fast detection of transient phenomena in DC systems.

Table 4 Impact of sampling frequency on protection Performance

f [kHz]	1	10	20	50	60	70	80	96	100
Stage I	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
Stage II	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
Stage III	Fail	Fail	Fail	Fail	Pass	Pass	Pass	Pass	Pass

4 Hardware Validation

4.1 Experimental Arrangement

A real-time hardware prototype has been developed in order to validate the practical implementation of the proposed scheme. For such development, the Opal-RT OP5600 HILBOX has been utilised, integrating digital-analogue I/O and GPS cards.

As illustrated in Fig. 9(a), the entire system is divided into two subsystems, one for the MTDC test network and one for the protection scheme algorithm. The input signals to the protection scheme are current and voltage signals (both converted to proportional voltages) recorded from the MTDC network simulation. Time-synchronised measurements are implemented through a GPS TSync-PCIe card. As all the input signals have been scaled-down to remain within the safe operating range of the I/O cards (i.e. ± 16 V), the protection thresholds have been scaled-down accordingly. The analogue inputs are sampled at 96 kHz as per IEC 61869-9.

Communication and measurement delays within DC substation communication have been emulated taking into account Equation 9, and hence, physical Ethernet switch has not been used. There is also a user interface panel, from which the user can monitor and control the simulation; specifically the user can trigger or reset the fault scenarios or monitor the tripping status of the protection system and CBs. The MMC models utilised in the experimental validation are the same as those used in the simulation based analysis (i.e. Type 3).

4.2 Experimental Results

For the experimental validation of the proposed scheme, a PPF in the middle of Line 1 is utilised. Due to the limited number of channels of the available oscilloscope, only the results for the protection system placed at terminal T_3 is reported.

In Fig. 10, the results are presented as captured during real-time simulation of the aforementioned fault, triggered at $t_{fault} = 1.5$ ms. Following the fault, there is a DC current infeed from the converter and Lines 1, 3 and 6 (Fig. 10(a)), which in turn results in the

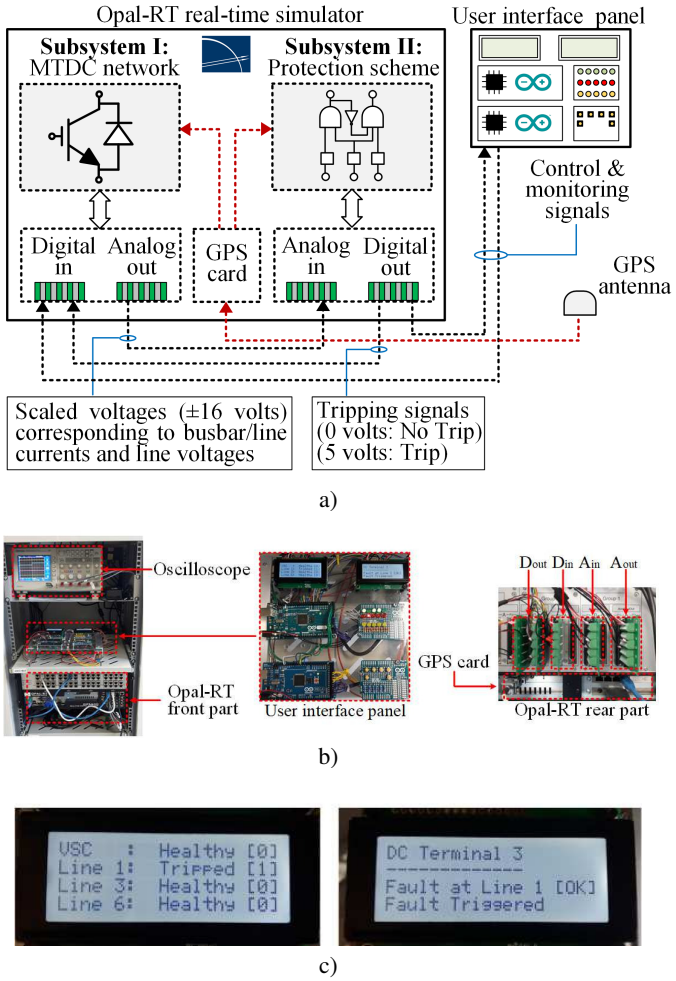

Fig. 9: Experimental arrangement.
a Diagram of experimental setup.
b Photo of experimental setup.
c LCD output.

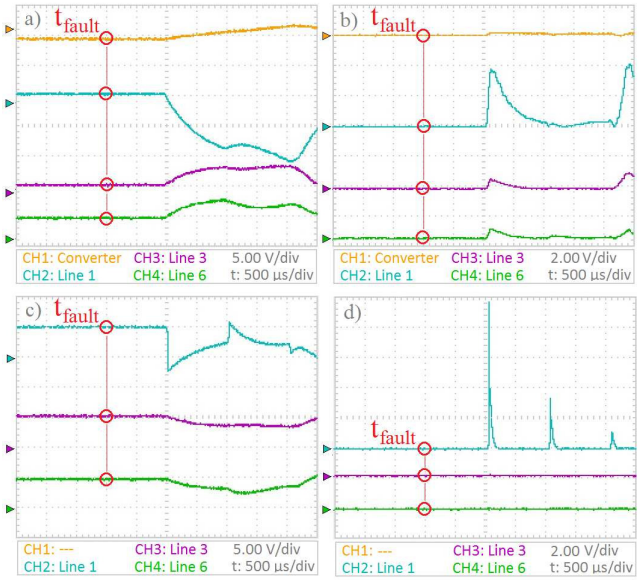

Fig. 10: Hardware prototype response to fault at Line 1.
a DC currents.
b DC current fault detection signal.
c Line DC voltages.
d DWT of line DC voltages.

increased $fds(I_{dc})$ values (Fig. 10(b)) enabling protection Stage I. Since there is no change in the differential current, the algorithm proceeds to Stage III. As shown in Fig. 10(c), the DC voltage of the faulted line (i.e Line 1) reveals steep changes, while there is a much smoother transition for the healthy lines. As a result, the DWT magnitude (Fig. 10(d)) for Line 1 increases significantly. It should be noted here that even in such small scale, the discrimination of the faulted line is very distinct as the DWT magnitude of the healthy lines is practically zero. After approximately 1.1 ms, the algorithm proceeds to the selective tripping of Line 1, which is also depicted in the alphanumeric LCD screen of the user interface panel in Fig. 9(c).

It should be noted that the noise seen in the experimental results, originates both from the artificial noise added to the signals at the simulation stage and actual noise arising from the signal conversion and exchange within analogue and digital I/O cards.

5 Conclusions

In this paper a new centralised protection scheme for MTDC grids has been proposed which utilises the principles of busbar differential protection and travelling waves and conforms with IEC 61869-9 and IEC 61850. It has been found that the proposed scheme can provide fast and discriminative protection for busbar and line faults (both solid and highly resistive). This has been validated in detailed transient simulation, and further demonstrated using a real-time hardware-based laboratory prototype. This prototype provides a high level of confidence that the proposed method is practical, considering realistic measurements, communications and computation. The use of line terminating inductors leads to the limitation of the current rise in case of a fault, assists in the discrimination of the faulted line and also prevents the currents from exceeding the breaking capability of the HbCB (9 kA). Additionally, it has been found that the recommended frequency of 96 kHz reported in IEC 61869-9 is suitable for the detection of fast transient phenomena in HVDC grids, and hence can be utilised for the implementation of fast and reliable DC busbar and line protection incorporating travelling waves. Further sensitivity analysis revealed that a minimum sampling rate of 60 kHz would be adequate for this application.

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