JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.18, NO.2, APRIL, 2018
https://doi.org/10.5573/JSTS.2018.18.2.270
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

A 2-40 Gb/s PAM4/NRZ Dual-mode Wireline Transmitter with 4:1 MUX in 65-nm CMOS

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***Abstract*—This paper presents a 2-40 Gb/s dual-mode wireline transmitter supporting the four-level pulse amplitude modulation (PAM4) and non-return-to-zero (NRZ) modulation with a multiplexer (MUX)-based two-tap feed-forward equalizer (FFE). An edge-acceleration technique is proposed for the 4:1 MUX to increase the bandwidth. By utilizing a dedicated cascode current source, the output swing can achieve 900 mV with a level deviation of only 0.12% for PAM4. Fabricated in a 65-nm CMOS process, the transmitter consumes 117 mW and 89 mW at 40 Gb/s in PAM4 and NRZ at 1.2 V supply.**

***Index Terms*—Four-level pulse amplitude modulation (PAM4), non-return-to-zero (NRZ), edge-acceleration technique, linearity optimization, dual-mode wireline transmitter**

I. INTRODUCTION

The ever-increasing bandwidth demand for data communications has necessitated the wireline connections towards data rates of 40 Gb/s or beyond [1], [2]. When the data rate reaches 40 Gb/s and above, two methods are used to further improve the wireline data throughput. One is to precede with non-return-to-zero (NRZ) signaling by increasing the clock speed [1-3]. The other employs high-order modulations (HOM) such as four-level pulse amplitude modulation (PAM4) [4-6] and eight-level pulse amplitude modulation (PAM8) [7], [8], which are attracting more and more attention owing to their bandwidth efficiency. Since PAM4 exhibits excellent balance among performance, cost, power and complexity, it is currently considered as the best HOM for the upcoming Ethernet 400GE [9]. To keep the compatibility with the existing NRZ components and avoid developing multiple IPs, the wireline transceivers are required to support both multiple-modulation and wide operation range [10], [11].

The major challenge in designing NRZ transmitter (TX) is the final-stage serialization. For the widely used half-rate architecture shown in Fig. 1, the delay difference between the data and the clock tree buffer paths (t_1-t_2) may fluctuate beyond 1 unit interval (UI) at high-speed rate under different PVT corners [12], thus causing setup/hold timing violations for the high-speed latches. To solve this problem, reference [13] uses an

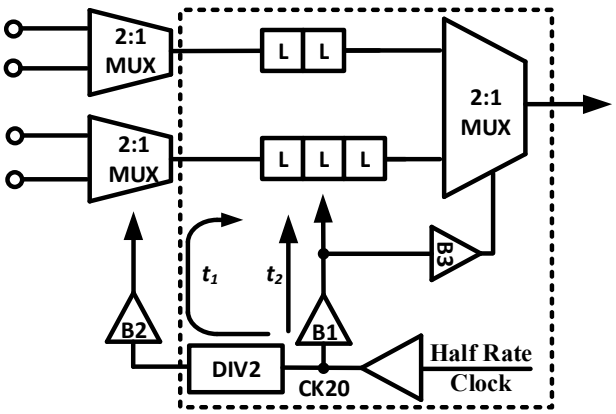

Fig. 1. Conventional half-rate transmitter.

Manuscript received Jul. 27, 2017; accepted Oct. 26, 2017
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additional calibration loop to guarantee the timing constraint between the data and the clock. Nonetheless, the calibration loop significantly increases the complexity and consumes additional power. On the other hand, the quarter-rate architecture has been proved to be a promising solution for high-speed applications [1], [2], [14], [15] because it not only relaxes the critical path timing to 3 UI, but also halves the maximum clock speed. Additionally, the power consumption can be saved by replacing the last two-stage 2:1 multiplexers (MUXs) and the retiming latches with one 4:1 MUX. However, the 4:1 MUX suffers from limited bandwidth due to its doubled self-loads.

The main difficulty in designing the PAM4 TX focuses on the output nonlinearity associated with the desired large swing. Compared with the NRZ modulation, PAM4 applies four voltage levels to transmit two bits in one symbol to improve the channel efficiency. Nevertheless, the vertical swing is reduced to one third of the full swing, which means that the signal-to-noise-ratio (SNR) is attenuated by 9.5 dB, thus leaving a smaller margin for the receiver-side data recovery. Therefore, a high-output swing is crucial for the PAM4 TX. However, this usually leads to nonlinearity problem that is particularly severe in the current mode logic (CML)-based topology, because the high-output swing inevitably compresses the VDS of the tail current source.

Another challenge in implementing the feed-forward equalizer (FFE) for both NRZ and PAM4 TX is the generation of several accurate 1 UI-delayed sequences. Fig. 2(a) shows a typical D flip-flop (DFF)-based FFE, which sums the delayed sequences using different weight coefficients to compensate for the channel loss. In this structure, the delayed versions of the sequences are generated by the DFF, thus it can operate at a wide range. However, limited by the large CK-to-Q delay, the flip-flop-based FFE structure [16] is impractical in designs of over 24 Gb/s in 65-nm CMOS process. An alternative solution is to use analog delay line to produce the 1 UI-delayed sequences, as displayed in Fig. 2(b). These analog delay lines are usually based on cascaded CML buffers [17], [18], or LC-cells [2], [19]-[21], which have been proved in ultra-high-speed applications such as 64 Gb/s [2]. Nonetheless, they cannot support a wide operation range because of their limited adjusting range. Besides, the multiple CML buffers-based FFE is power

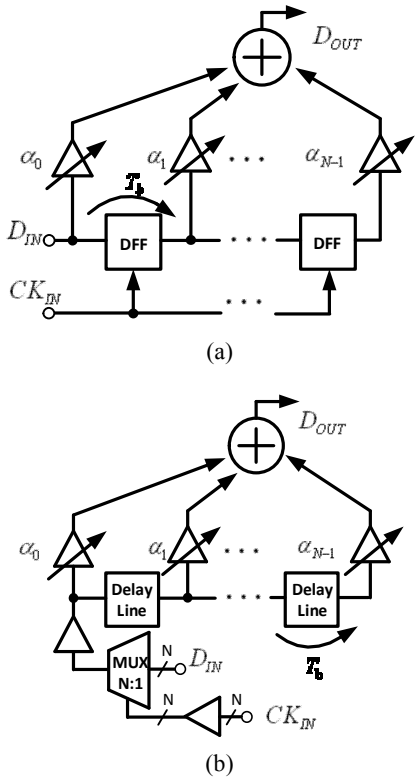


Fig. 2. FFE structure (a) DFF-based FFE, (b) delay line-based FFE.

hungry due to the need of multiple stages to realize 1 UI delay, and the LC-cell-based FFE occupies a large chip area due to the involvement of many inductors.

To address these issues, a quarter-rate NRZ/PAM4 dual-mode transmitter supporting a wide frequency range with a MUX-based two-tap FFE is proposed. To further increase the bandwidth of the MUX with high power efficiency, an improved 4:1 MUX with edge-acceleration technique is designed. Additionally, a dedicated cascode current source is utilized to guarantee large output swing, high output linearity, and small parasitic capacitance.

The remainder of this paper is organized as follows. Section II describes the proposed NRZ/PAM4 dual-mode transmitter. Section III presents the crucial circuit blocks of the transmitter, and Section IV gives the measurement results of the chip. The conclusion is drawn in Section V.

II. PROPOSED NRZ/PAM4 DUAL-MODE TRANSMITTER

Fig. 3 shows the block diagram of the NRZ/PAM4 dual-mode transmitter. It consists of two quarter-rate

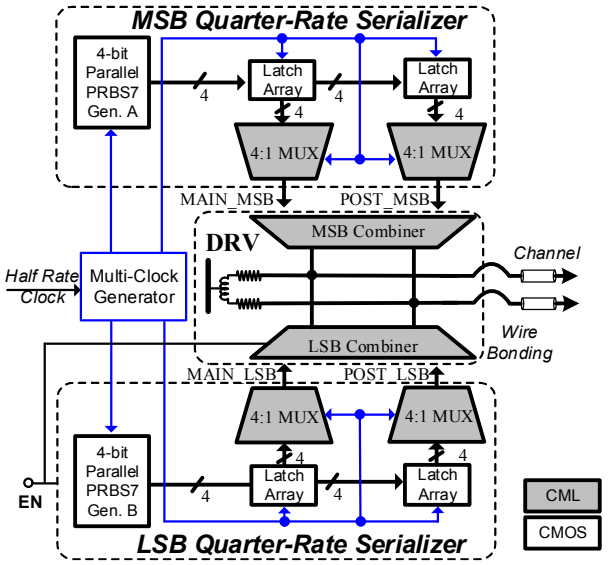


Fig. 3. NRZ/PAM4 dual-mode transmitter architecture.

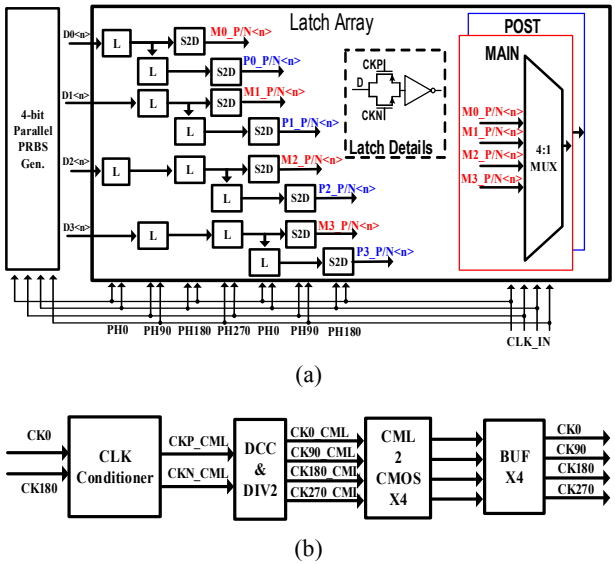


Fig. 4. (a) Multi-MUX-based FFE, (b) MCG.

serializers for MSB and LSB, one output driver (DRV), and one multi-clock generator (MCG). Each quarter-rate serializer contains one 4-bit parallel PRBS generator, two 4:1 MUXs, and two latch arrays. The operation mode of the transmitter is controlled by the external signal EN. When EN is logic high, both the MSB and LSB quarter-rate serializers along with the combiners are activated and then the transmitter works in the PAM4 mode. Here, the combiners adopt the 2:1 tail current sources to generate the four voltage levels. When EN is logic low, the LSB quarter-rate serializer and the LSB combiner are disabled, thus the transmitter works in the NRZ mode. To make up for the ability of the driver (the LSB combiner is disabled) in the NRZ mode, the currents in the MSB combiner are correspondingly increased.

In each quarter-rate serializer, an independent PRBS7 generator is employed to produce the 4-bit parallel data, which are applied to two interleaved latch arrays to generate the 1 UI-delayed data sequences. These sequences are then serialized into two full-rate data streams for the main tap and post tap in the two 4:1 MUXs. The two serialized data streams are finally fed into the combiners to produce the pre-emphasis signal.

Fig. 4(a) describes the details of the latch array, where the interleaved latching technique presented in [22] is adopted. The latch array and S2D triggered by the four orthogonal clocks provide proper delay data for the main and post 4:1 MUXs. The latches and S2D circuits are implemented by dynamic latches, which are power efficient and compact because they are consisting of only four transistors. The four orthogonal clocks are generated by the MCG shown in Fig. 4(b). The MCG receives single-end half-rate clock, and then transforms it into differential CML clocks in the CLK conditioner. The four orthogonal CML clocks are divided by the CML differential flip-flop-based divider, which are then converted into CMOS clocks in the CML2CMOS circuits. These clocks are first buffered to enhance their driving capabilities and then applied to the latch array and 4:1 MUXs for the parallel data retiming and serializing. Compared with traditional DFF and LC-cells-based FFE, the multi-MUX-based FFE together with the latch array not only supports a wide data-rate range, but also improves the power efficiency.

III. Crucial Circuit Blocks

1. 4:1 MUX

The block diagram of a typical 4:1 MUX is depicted in Fig. 5(a). It includes two peaking inductors, two resistors, and four equivalent unit cells. Each unit cell takes two clocks with 90-degree phase skew and one quarter-speed data as the inputs and generates 1 UI output pulse. Thus, the combined four unit cell serializes four quarter-speed data into a single full-speed output signal, which is described in Fig. 5(b). The unit cell that is the critical block of the 4:1 MUX usually has three basic structures

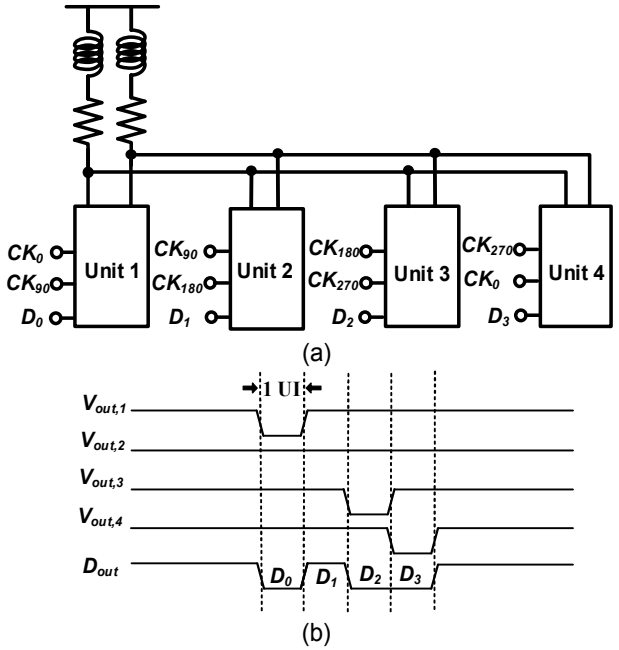


Fig. 5. Typical 4:1 MUX (a) Blok diagram, (b) timing diagram.

for implementation, as shown in Fig. 6.

The first unit cell structure and its timing are given in Fig. 6(a). It stacks three transistors to generate the 25% duty cycle output pulse. The timing shows that the two clocks (CK_1, Ck_2) with 90-degree phase skew and the input data (D_{in}) are combined into one stage. The main drawback is its small current driving ability. To overcome the difficulty, large-size transistors need to be adopted [14], which increases the output capacitance and adds the load of the preceding stage. So, this structure is bandwidth limited and has low power efficiency.

The second structure of the unit cell and its timing are shown in Fig. 6(b), which only consists of two transistors at the output stage. The 25% duty cycle clock pulse generated in the preceding stage samples the quarter-rate input data at the output stage. To guarantee the serialized data with low jitter performance, the 25% duty cycle clock pulse must have sharp edges to drive the output transistor in every clock period. In [17], [22], [23], a large-size inverter is employed to provide steep transition edges, which is power hungry.

Fig. 6(c) illustrates the third structure and its timing. It also utilizes two transistors at the final stage to generate the output pulse. In comparison with the second structure, it replaces the 25% duty cycle pulse with the 50% duty clock to sample the data at two stages, which is power efficient. As depicted in its timing diagram, at the output

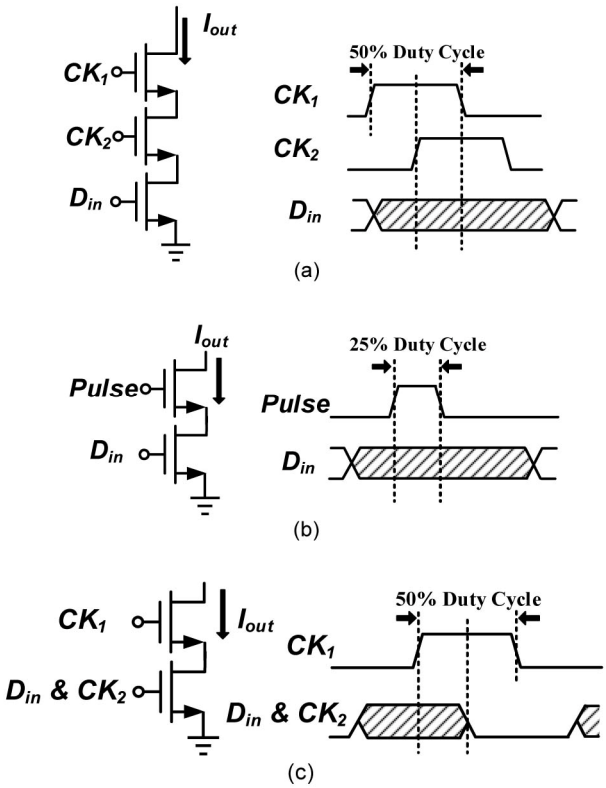


Fig. 6. Three different structure of the unit cell and their timing diagrams.

stage, the rising edge of CK_1 and the falling edge of CK_2 that is dependent on the input data are combined together to control the output pulse width. In the implementation of this unit cell, another structure can be obtained by placing CK_1 ahead of CK_2 with 90-degree skew. Furthermore, switching the input signals at the final stage can also evolve another two structures. Thus, the method of two-stage sampling with quarter-clock has four structures to realize this unit cell, three of which are introduced in [1], [2], [17], respectively.

In order to further extend the bandwidth and improve the power efficiency, we propose an improved 4:1 MUX based on the work in [2], which is a variation of the third structure illustrated in Fig. 6(c). Fig. 7(a) depicts the block of the proposed 4:1 MUX and the details of the unit cell. Each unit cell contains a differential pair of pulse generators. The pulse generator circuit is illustrated in Fig. 7(b), which utilizes two logic gates (INV_A and INV_B) to output V_a and V_b to drive the stacked transistors M_6 and M_7, respectively. By inserting the data-controlling transistor M_4 into the INV_A, transistor M_7 only opens when D_{in} and CK_a are both logic low, thus

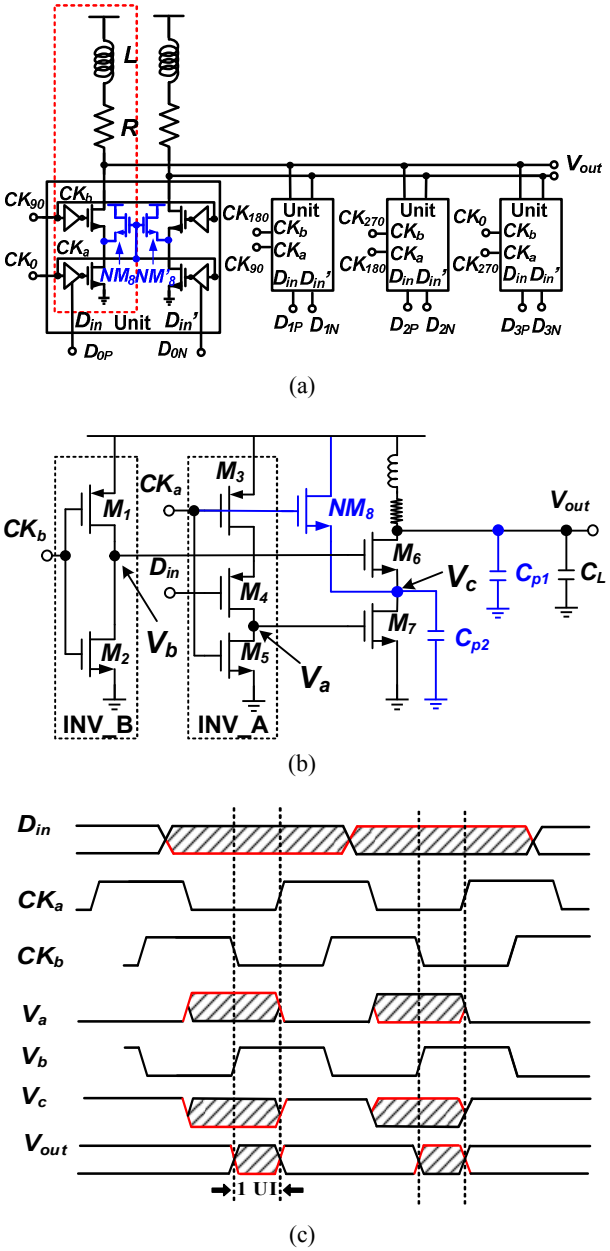


Fig. 7. (a) Proposed 4:1 MUX, (b) details of the pulse generator, (c) timing diagram of the unit cell operation.

the data can be transmitted to the output. The inserted transistor NM_8 is used to accelerate the rising edge of the output pulse to further extend the bandwidth and improve the signal quality. The timing of the input data (D_{in}), input clocks (CK_a, CK_b), intermediate nodes (V_a, V_b, V_c), and output data (V_{out}) is shown in Fig. 7(c). Here, V_a depends on D_{in} and CK_a, V_b is the inverting version of CK_b, and V_c is the connecting node of M_6 and M_7. The output of the stacked M_6 and M_7 is Vout. The logic function of the pulse generator is as follows,

$$V_{out} = \overline{\overline{CK_a} \bullet \overline{CK_b} \bullet \overline{D_{in}}} = CK_a + CK_b + D_{in}. \quad (1)$$

As shown in Fig. 7(c), the input data D_{in} can be transmitted to the output only when CK_a and CK_b are both low. If D_{in} is low, the pulse generator generates the negative pulse; otherwise the generator output will keep high. Here, the falling edge of the output negative pulse is determined by the rising edge of V_b, while its rising edge is subjected to the falling edge of V_a. Besides, both the rising and falling edges of the negative pulse are determined by the load capacitance of V_{out} (C_{p1} and C_L). Therefore, its bandwidth can be increased by sharping the edges of the negative pulse transition. This target can be realized by improving the driving ability that sharpens V_a's falling edge and V_b's rising edge. On the other hand, it can also be met by reducing the output parasitic capacitance.

In the first method, the two transition edges can be sharpened by skewing the P-to-N ratio of the INV_A and INV_B, and enlarging M_1 and M_5. At the same time, this method reduces the falling and rising time of V_a and V_b, respectively, which can save the power [2]. Fig. 8 reveals the simulation waveform of V_a and V_b.

In the second method, reducing the output parasitic capacitance is not easy in traditional structure due to the large size of the two stacked transistors that provide large current drive. It is also difficult to reduce the self-load that is contributed by the parasitic capacitance of V_{out} and V_c. Fig. 7(b) indicates the parasitic capacitance on the critical path, where C_L denotes the next-stage input load, C_{p1} represents the output parasitic capacitance that is mainly contributed by the transistors of the four unit cells, and C_{p2} stands for the parasitic capacitance of V_c. In the MUX operation, C_L and C_{p1} influence both the rising time and falling time of the negative output pulse. However, C_{p2} only affects its rising time because when M_7 is driven by V_a's falling edge and starts to be turned off, C_{p2} extracts charge from V_{out} at the same time. When M_6 is driven by V_b's rising edge and starts to be turned on, the charge of C_{p2} has been discharged through M_7 [see Fig. 7(c)].

In fact, this improved structure can further reduce the output parasitic capacitance by introducing an acceleration transistor. In Fig. 7(b), after adding the acceleration transistor NM_8, the parasitic capacitance of V_c (C_{p2}) has no influence on the rising and falling time of

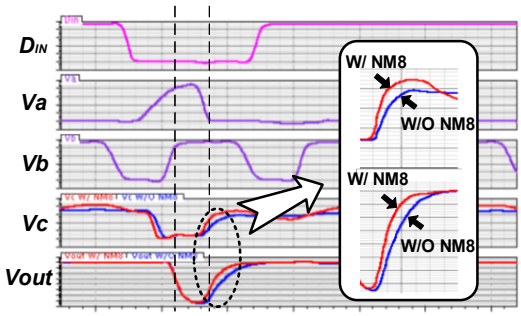


Fig. 8. Simulated waveform of the pulse generator with and without NM_8.

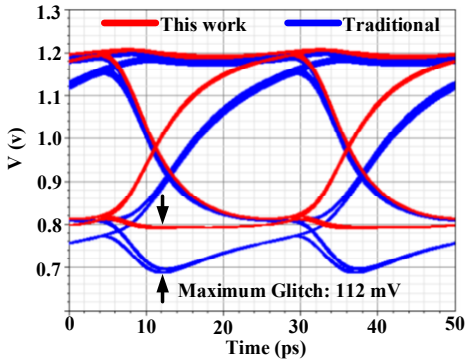


Fig. 9. Simulated eye-diagram of the proposed 4:1 MUX and the traditional 4:1 MUX.

the negative output pulse, which extends its bandwidth. When M_7 is driven by V_a's falling edge and starts to be turned off, NM_8 is already opened and charges C_{p2} since CK_a's rising edge is ahead of V_a's falling edge. At the same time, C_{p2} doesn't extract charge from V_{out}, which accelerates the rising time of the negative output pulse. When M_6 is driven by V_b's rising edge and starts to be turned on, NM_8 has been turned off and the charge of C_{p2} also has been discharged through M_7, which has no impact on the falling time of the negative output pulse. Consequently, when the acceleration transistor NM_8 is added, the self-load contributed by C_{p2} has been eliminated. Fig. 8 shows the simulated waveform of the pulse generator with and without adding NM_8. The result indicates that the rising times of V_c and V_{out} are both accelerated by NM_8 when M_7 is switched off. In addition, the falling edge of V_{out} is not changed compared with the traditional structure.

Besides, we can extend the bandwidth through shrinking the M_6 size, which becomes possible after introducing the acceleration transistor NM_8. In the traditional design, when the pulse generator has fixed output swing with a specific pull-up resistor, the on-resistance of M_6 and M_7 in series is determined. The parasitic capacitances of these two transistors contribute to limiting the bandwidth. Consequently, changing their size when maintaining constant on-resistance of M_6 and M_7 in series is not obvious for extending the bandwidth. However, when adding the acceleration transistor, this situation is different. When keeping the on-resistance of M_6 and M_7 in series the same as that in the traditional design, we can shrink M_6 and increase M_7 with proper size to greatly reduce C_{p1} and slightly increase C_{p2}. This is because the parasitic capacitance of V_c (C_{p2}) can be ignored in this structure as explained earlier. So, shrinking M_6 and increasing M_7 with proper size can further extend the bandwidth. Fig. 9 shows the simulated eye-diagram of the proposed MUX, whose rising edge is faster than that of the traditional design when they have the same load.

The simulation result depicted in Fig. 9 also shows that the glitch of the traditional structure is suppressed by introducing the accelerating transistor. In the traditional design, when the MUX continuously outputs two logic-low bits, a negative glitch occurs at the second unit opening. When the V_{out} dragged down by the second unit cell already arrives its required low voltage, C_{p2} in the first unit cell also extracts charge from V_{out} at the falling edge of V_a. However, in the proposed structure, by introducing the accelerating transistor, C_{p2} avoids extracting charge from V_{out} when the improved MUX continuously outputs two logic-low bits.

2. Linearity Optimization on the Output Driver

The output DRV is one of the most important circuits in the PAM4 transmitter design. Compared with the eye-height of the NRZ signaling, the PAM4 eye-height shrinks to one third of that of the NRZ, hence there is little margin left for the receiver-side data recovery. Moreover, lower eye-height compression makes this effect more severe as the transmitting bit error rate (BER) is subject to the worst eye. Consequently, large output swing with uniform level spacing is crucial for the PAM4 DRV to improve the SNR and relax the complexity of the receiver design.

The transmitter in [11] cannot operate at ultra-high-speed since it incorporates the source-series terminated

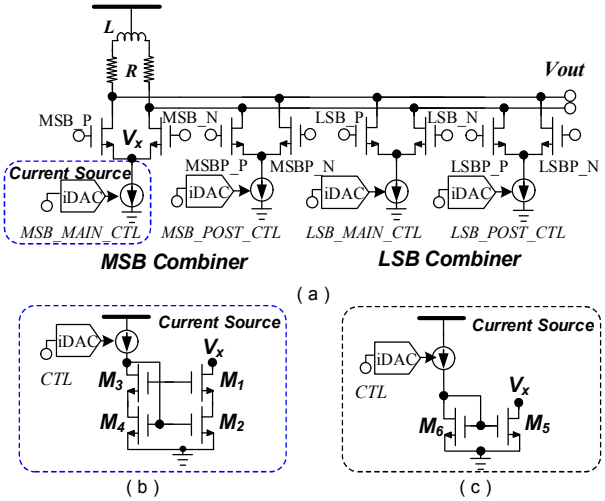


Fig. 10. (a) Output driver, (b) dedicated cascode current source, (c) traditional current source.

(SST) driver, which is a voltage-mode driver. Reference [4] adopts an 8-bit DAC-based driver, which employs a 1.5 V supply to increase the output swing for improving the linearity. Nevertheless, the heavy drain-loading significantly limits its maximum operation speed. Additionally, the uniformity of the voltage level spacing can be deteriorated by the nonlinearity of the DAC. This work applies a CML-based driver with dedicated cascode current sources to enlarge the output swing and improve the output linearity.

Fig. 10(a) illustrates the details of the output driver. It comprises four current-mode differential pairs and a pair of shut-peaked loads. In the CML-based driver, the linearity is mainly constrained by the channel-modulation effect of the tail current sources. Although the internal resistance of the traditional current source [see Fig. 10(c)] can be improved by adopting a long channel device, the increased device size inevitably enlarges the parasitic capacitance at the output. This enlarged parasitic capacitance in return lower the internal impedance at high frequencies, thus degrading the output linearity. In addition, the large parasitic capacitance is also detrimental to the impedance matching at high frequencies.

To address these issues, a low-voltage cascode current source is utilized, as shown in Fig. 10(b). To satisfy the requirements of both high output resistance and low parasitic capacitance at V_x, a large-size M_2 is used to improve the output resistance while a minimum-size M_1 is cascoded to isolate the large drain capacitance of M_2.

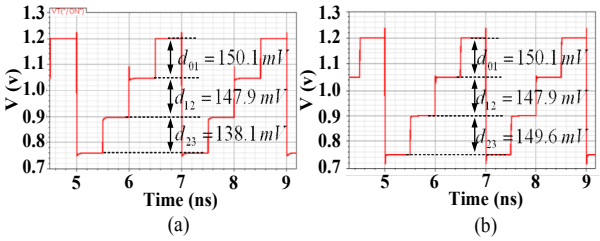


Fig. 11. Single-end output waveforms (a) Traditional driver, (b) low-power cascode drive.

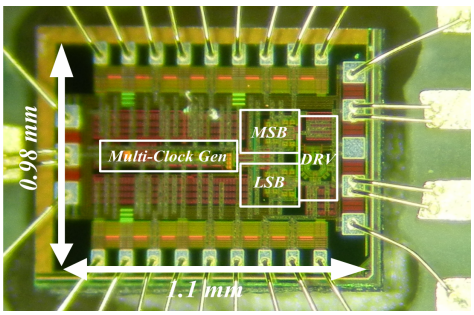
Fig. 11 gives the single-end output linearity comparison between the traditional current source-based driver and the proposed cascode current source-based driver. The simulated results show that the level deviation is optimized from 3.3% to 0.1% for an output swing of 450 mV with a 1.2 V power supply. The level deviation is defined as,

$$Level\ deviation = \frac{1}{3}\sum_{i,j=10,21,32}\frac{\left|d_{ij} - V_{Pk-Pk}/3\right|}{V_{Pk-Pk}/3}\times 100\%, \tag{2}$$

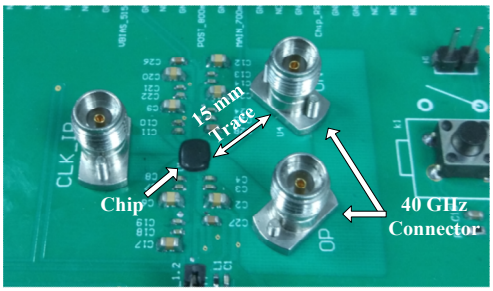
where d_{ij} is the vertical space of level i and level j, and V_{Pk-Pk} is the full eye height of the output.

IV. Measurement Results

The chip is fabricated in a 65-nm CMOS technology and its die photo is given in Fig. 12(a). The whole transmitter is 1.1×0.98 mm^2, where the core circuit occupies an area of 0.48 mm^2. Fig. 12(b) presents the photograph of the test setup. The chip is packaged in chip-on-board, and the half-rate clock is generated by Agilent E8257D. After 15 mm PCB trace, the differential signal is measured through a center-mounted 40 GHz connector and 1 m cable. The overall channel loss is 4.5 dB and 11 dB at 10 GHz and 20 GHz, respectively. The eye-diagrams are measured by an Agilent Digital Signal Analyzer 93204A (33 GHz). When the transmitter works at the PAM4 mode, it consumes 117 mW with a 1.2 V supply, which corresponds to an energy efficiency of 2.93 pJ/bit. The power breakdown of the transmitter is shown in Fig. 12(c). The power consumption of the PRBS, MCG, latch array, MUX, and DRV with FFE is 9%, 47%, 5%, 24%, and 14%, respectively. When the transmitter operates at the NRZ mode, the LSB quarter-



(a)



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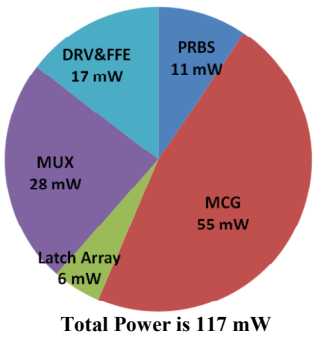

(c)

Fig. 12. (a) Die photograph, (b) photograph of the testing board, (c) power breakdown.

rate serializer and LSB combiner consume less and the total power consumption is 89 mW at 40 Gb/s.

Fig. 13 presents the measured PAM4 output, where Fig. 13(a) and (b) displays the output eye-diagrams at 2 Gb/s without equalization and with over-equalization, respectively. The output swing is 900 mV and the level deviation is 0.12%. Fig. 13(c) and (d) gives the properly-equalized eye diagrams at 35 and 40 Gb/s. The minimum vertical eye-opening is about 100/82 mV and the minimum horizontal eye width is about 34/30 ps. Fig. 14 depicts the measured NRZ output eye-diagrams, where the output eye-diagrams at 10 Gb/s without equalization and with over-equalization are displayed in Fig. 14(a) and (b). Fig. 14(c) and (d) shows the properly-equalized eye-diagrams at 40 and 50 Gb/s, where the eye height

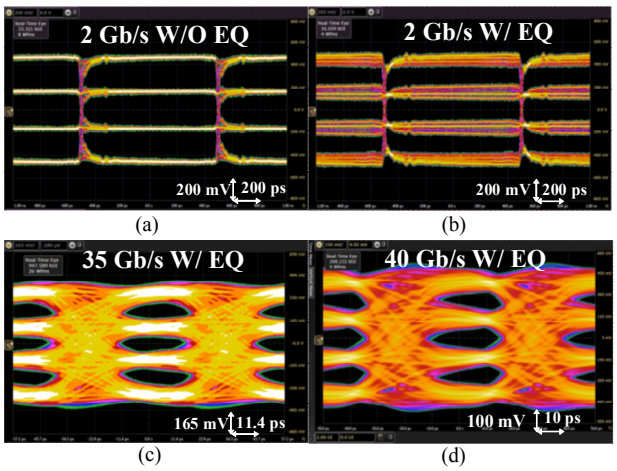

Fig. 13. PAM4 eye diagrams (a) Without equalization at 2 Gb/s, (b) over-equalized at 2 Gb/s, (c) properly-equalized at 35 Gb/s, (d) properly-equalized at 40 Gb/s.

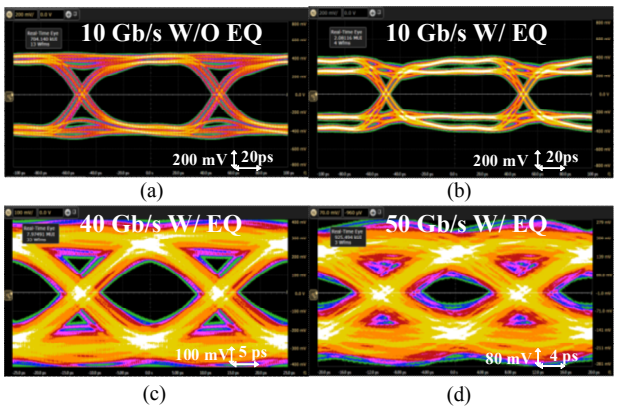

Fig. 14. NRZ output eye diagrams (a) Without equalization at 10 Gb/s, (b) over-equalized at 10 Gb/s, (c) properly-equalized at 40 Gb/s, (d) properly-equalized at 50 Gb/s.

and total jitter are equalized to 300/130 mV and 9.6 /16.8 ps, respectively.

In Table 1, the performance of the designed 2-40 Gb/s wireline transmitter is summarized and compared with other state-of-the-art works with similar data rates. The results indicate that our transmitter achieves excellent power efficiency and high-quality eye diagrams in both NRZ and PAM4 modes, owing to the proposed quarter-rate architecture and edge-acceleration 4:1 MUXs.

V. CONCLUSION

A 2-40 Gb/s PAM4/NRZ dual-mode wireline transmitter with two-tap multi-MUX-based FFE is implemented in 65-nm CMOS technology. The robust multi-MUX-based FFE has been validated that it can

Table 1. Performance summary and comparison

	This work		[10]		[11]		[13]
Technology	65 nm		65 nm		14 nm		65 nm
Supply (V)	1.2		1.2		N/A		1.3
Chip Area (mm^2)	1.08		0.06 (core)		0.0279		1.14
Modulation	NRZ	PAM4	NRZ	PAM4	NRZ	PAM4	PAM4
Data Rate (Gb/s)	40	40	16	32	40	40	60
Data Range (Gb/s)	1-50	2-40	N/A	N/A	16-40	16-40	56-62
FFE (Taps)	2	2	4	2	4	N/A	3
Output Swing Vpp (V)	0.9	0.9	1.2	1.2	0.6	0.6	0.25
Vertical Eye Opening (mV)	300	82	100	100	200	80[a]	50
Horizontal Eye Opening (UI)	>0.6	>0.5	>0.5	>0.4	>0.5	>0.4[a]	>0.6
Power (mW)	89	117	N/A	159	518[b]	167[b]	290
Energy Efficiency (pJ/bit)	2.22	2.93	N/A	4.97	12.9[b]	4.19[b]	4.84[b]

[a]Including software-based CTLE at scope, [b]including PLL consumption.

provide a wide data-rate range from 1 to 50 Gb/s, while the proposed edge-acceleration technique in the 4:1 MUX extends its bandwidth and suppresses the glitch. In addition, the linearity of the PAM4 output is improved by utilizing the dedicated cascode current sources, and the level deviation reaches 0.12%. With a 1.2 V supply, the transmitter consumes 117 mW in the PAM4 mode and 89 mW in the NRZ mode, both at 40 Gb/s.

ACKNOWLEDGMENT

This work was supported by Beijing Engineering Research Center under grant BG0149.

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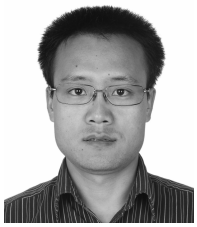

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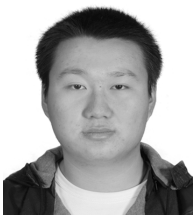

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