# The over-reset phenomenon in $Ta_2O_5$ RRAM device investigated by the RTN-based defect probing technique

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***Abstract*— Despite the tremendous efforts in the past decade devoted to the development of filamentary resistive-switching devices (RRAM), there is still a lack of in-depth understanding of its over-reset phenomenon. At higher reset stop voltages that exceed a certain threshold, the resistance at high resistance state reduces, leading to an irrecoverable window reduction. The over-reset phenomenon limits the maximum resistance window that can be achieved by using a higher $V_{reset}$, which also degrades its potential in applications such as multi-level memory and neuromorphic synapses. In this work, the over-reset is investigated by cyclic reset operations with incremental stop voltages, and is explained by defect generation in the filament constriction region of $Ta_2O_5$ RRAM devices. This is supported by the statistical spatial defects profile obtained from the random telegraph noise based defect probing technique. The impact of forming compliance current on the over-reset is also evaluated.**

***Index Terms*—Resistive switching, RRAM, over-reset, defect profile, random telegraph noise, $Ta_2O_5$, $HfO_2$**

Resistive-switching random access memories (RRAMs) have attracted extensive interest in the past decade as a promising candidate for future non-volatile memory applications [1-5]. RRAM devices can be categorized into either filamentary or non-filamentary [6,7] types. The filamentary type has a relatively longer development history and represents the current mainstream RRAM technology. Tremendous effort has been devoted to improving their performance such as endurance, retention, on/off window, etc. A large resistance window (RW) is always desirable for achieving better performance in applications such as multi-level memory [4] and neuromorphic synapses [8].

Resistive switching in filamentary devices has been attributed to the reversible migration of either metal ions in CBRAMs [9-11] or oxygen ions/vacancies in RRAMs [2-6]. A conductive filament is generated in RRAM during the forming through a field assisted and thermally activated hopping process. During alternate reset and set operations, the filament ruptures and restores repeatedly, leading to the high resistance state and low resistance state, respectively (HRS/LRS). It has been observed in RRAMs with various oxides such as $HfO_2$ and $Ta_2O_5$ [12, 13] that once $V_{reset}$ increases beyond a certain level, $R_{HRS}$ will start to decrease instead of further increase; it is difficult to recover from the consequent window reduction [12, 13]. This over-reset phenomenon will therefore limit the achievable RW by using a higher $V_{reset}$.

The over-reset phenomenon has been explained by the migration of defects near the bottom electrode (BE) moving back into the constriction region of the filament at higher reset voltages, which re-connects the defect-rich filamentary regions near the top electrode (TE) and BE. This effect leads to a reduced resistance at HRS [12]. An alternative explanation is by the horizontal out-diffusion of defects from the filament into the surrounding dielectrics which forms additional conduction paths, hence the higher conduction current and lower resistance [13]. However, there is a lack of direct experimental evidence to support either of the above assumptions. By using the random telegraph noise (RTN)-based defect probing technique (RDT) developed in our recent work [6, 7], we provide a novel microscopic insight into the defect's spatial locations and compare the defect profiles after normal- and over- reset. The over-reset can be explained by defect generation in the filament constriction region at higher reset voltages. The impact of the compliance forming current on over-reset is also evaluated and discussed.

The $Ta_2O_5$ filamentary RRAM devices used in this work were fabricated in a cross-point structure with a size of 75 nm × 75 nm. The device consists of a TiN/$Ta_2O_5$/TaOx/TaN/TiN stack. The TiN BE was sputtered at room temperature and patterned, followed by the ALD deposition of a 4-nm-thick high-quality stoichiometric $Ta_2O_5$ layer. A nonstoichiometric 20-nm-thick TaOx film was then deposited by reactive DC magnetron sputtering using a Ta target in oxygen ambient. Without breaking the vacuum, a 10-nm-thick TaN capping layer was sputtered followed by a 30-nm-thick TiN film sputtering to form the TE. A long wire was patterned to connect the probe pad to the TE, enabling an integrated access resistance which effectively suppresses reset current overshoot [14]. We have also observed similar over-reset in other devices with either a Ti/$Ta_2O_5$(15nm)/ Pt stack [15] or a TiN/Hf(10nm)/$HfO_2$(5nm)/ TiN stack [6].

DC electrical measurements were carried out by using a Keysight B1500A semiconductor parameter analyzer with the bias applied to the TE, and the BE at ground. A forming step using the positive voltage sweep in the fresh device activates the reversible resistive switching behavior, which is capped by a compliance current (Icc) to protect the device from hard breakdown. The device structure and its I-V characteristics are shown in Fig. 1(a). It is switched between LRS and HRS during the positive set and negative reset voltage sweeps, respectively. In our previous work [6, 7], RTN has been used as the electrical measurement technique to evaluate the defect profile, providing a defect-level explanation of switching mechanisms in filamentary [6] and non-filamentary

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[7] devices. The over-reset phenomenon is investigated in this work by the RDT technique carried out in both normal-reset and over-reset devices for comparison. The origin of RTN is attributed to the random electron trapping/de-trapping process in a defect located in the oxide [16]. The spatial and energy location of defects can be extracted from the dependence of time constants on the TE bias. To obtain the statistical defect profile, the device was switched on and off repeatedly for 100 cycles under fixed conditions, and the RTN measurement was carried out after each reset. The accumulative occurrence of defects at HRS can therefore be used to evaluate the statistical defect profile. Details and discussion of this technique can be found in refs. [6, 7].

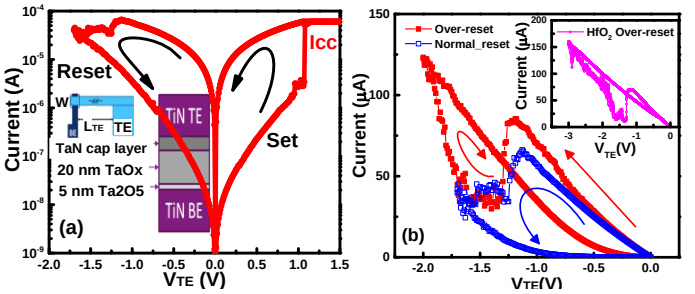


Fig.1 (a) The structure (inset) and bipolar resistive switching characteristics of a 75 nm × 75 nm $Ta_2O_5$ memory cell. (b) Comparison of normal reset (Vstop=-1.7V) and over-reset (Vstop=-2V) of the $Ta_2O_5$ RRAM. The inset shows the over-reset phenomenon in $HfO_2$ RRAM devices (Vstop=-3V).

I-V characteristics of a normal reset at a stop voltage of -1.7 V and an over-reset at a stop voltage of -2 V are compared in Fig. 1(b). Both devices were formed with an Icc of 20 μA. It is clear that the currents overlap in a large part of the upward voltage sweep, suggesting that both devices start from the same LRS level, and the reset process is similar for the bias level up to -1.7 V. Since the over-reset stop voltage is higher, its current starts to increase from -1.7 V onward, and also becomes higher during the downward voltage sweep, leading to the over-reset, i.e., a lower resistance at HRS. As shown in the inset of Fig. 1(b), a similar over-reset phenomenon is also observed in $HfO_2$ RRAM devices, suggesting it is a universal issue for filamentary RRAM devices.

To further demonstrate the impact of over-reset on the HRS, the reset bias sweep cycle (0 V→$V_{reset,stop}$ →0 V) was repeated with the stop voltage incremented for each cycle, without invoking the set sweep in between. I-V curves during the reset and over-reset cycles, and the resistance read-out current after each reset cycle measured at $V_{read}$=0.1 V, are shown in Fig. 2 (a)-(c), respectively. The device reset starts from $V_{reset}$ = -1.1 V, reaching the minimum HRS current at $V_{reset}$ = -1.7 V, and the over-reset starts from there onwards, the downward sweep current becomes higher than the upward sweep, and the read-out current also starts to increase, leading to lower HRS resistance. The upward and downward I-V curves of adjacent sweeps agree well, supporting the view that the resistance switching occurs at the higher range of $V_{reset}$ during each cycle. This phenomenon is contrary to the expectation that a larger $V_{reset}$ should always lead to a higher resistance at HRS.

The over-reset phenomenon causes irrecoverable damage to the resistance window, as shown in Fig. 2(d). After the normal set and reset switching cycle in step (1), the device underwent an over-reset and set cycle with a higher reset stop voltage at $V_{reset}$ = -2.3 V in step (2). After the over-reset, the window almost disappears in step (3) in which the device is set and reset with the same conditions used in step (1), demonstrating that the detrimental effect of over-reset on RW. RW can only be partially recovered in step (4) even if $V_{reset, stop}$ is increased to the value used in step (2), as the current sweeping direction is reversed. This clearly shows that the over-reset causes irrecoverable reduction to RW, even at higher reset voltage and current, therefore higher power consumption. The physical mechanism of over-reset is explored next with the RTN based defect probing technique.

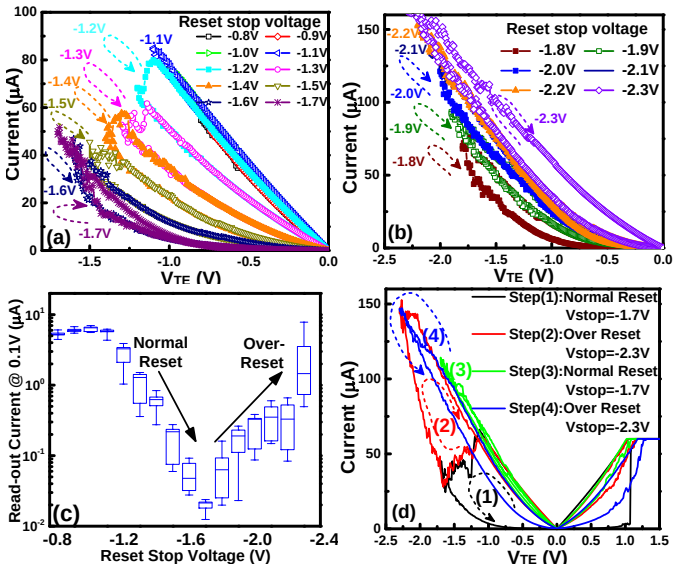


Fig. 2. (a) I-V curves of a $Ta_2O_5$ device being reset with incremental $V_{reset,stop}$ in the range from -0.8 V to -1.7 V. (b) I-V curves of device being over-reset with $V_{reset,stop}$ in the range from -1.8 V to -2.3 V. (c) The read-out current at $V_{read}$=0.1 V, measured after each cycle, against $V_{reset,stop}$ on 8 devices under the same condition. (d) I-V curves of a $Ta_2O_5$ device going through 4 set and reset cycles sequentially with different reset conditions. The set condition is fixed in each cycle at Icc = 60 μA.

Defect locations in the $X_T$-$E_T$ plane are extracted using the RDT technique described in refs. [6, 7] in detail, and compared after the normal reset and over- reset. The device was switched on and off repeatedly for 100 cycles under fixed conditions for normal reset and over-reset, respectively. The extracted defects are plotted as spheres and the corresponding statistical profiles of the defect occurrence at HRS are shown in Fig. 3(a)-(b). The typical RTN data are shown in Fig. 3(c). For the normal reset device, a region with no defect occurrence is observed at the center of the filament, as shown in Fig. 3(a). This result indicates that the filament constriction location is centered in the $Ta_2O_5$ layer of our $TiN/TaO_x/Ta_2O_5/TiN$ device. Early work has reported that the filament in $TaOx/Ta_2O_5$ dual-layer RRAM with Pt [17] or Ir [18, 19] metal electrodes ruptures in the $Ta_2O_5$ layer near the TE interface, by the redox reaction of oxygen ions or vacancies. Since filament growth/dissolution dynamics is strongly dependent on the oxide and electrode materials and their combinations, the centered constriction location in our device is mostly likely caused by the lower Schottky barrier and lesser scavenging power of the TiN electrode used in this work, and the similar oxygen scavenging power of the nonstoichiometric TaOx layer on top of the $Ta_2O_5$ switching layer, which leads to a more symmetric hour-glass shaped filament in the $Ta_2O_5$ layer [20]. In our previous work we have observed that in $HfO_2$ devices, the constriction is located near to, but not at, the BE [6]. This difference can be attributed to the Hf cap layer used under the TE in $HfO_2$ devices, which has stronger oxygen scavenging power

than the TiN BE, so that more oxygen vacancies are generated near the Hf cap, pushing the constriction region towards the BE.

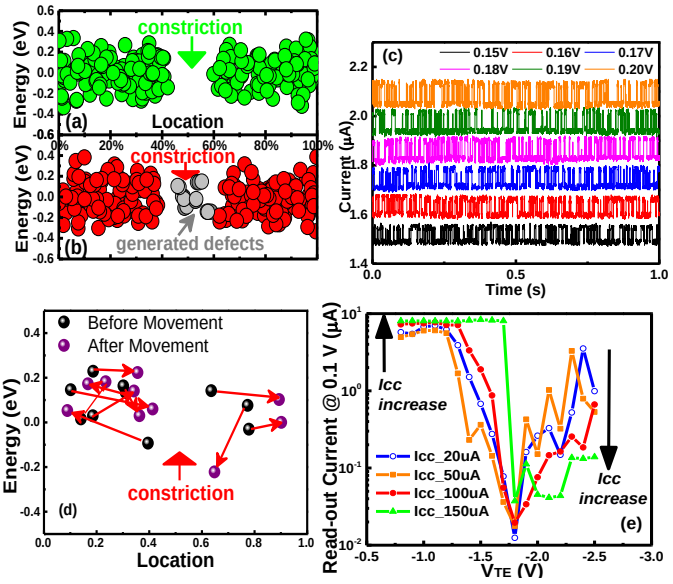


Fig. 3. Statistical defect profile in the filament region of $Ta_2O_5$, after (a) normal- and (b) over- reset, respectively. For the normal-reset device, $V_{reset}$ = -1.7 V, $I_{cc}$ = 60 μA. For the over-reset device, $V_{reset}$ = -2.3 V, $I_{cc}$ = 60 μA. (c) Typical RTN measured at various TE biases, from which the emission/capture time constants dependence on bias are obtained to extract the defect location [6, 7]. (d) Defect movements detected during the over-reset. There is no defect movement observed within the constriction, where the defects are generated. (e) Incremental reset voltages applied on devices formed with different Icc, affecting the over-reset phenomenon.

In the over-reset $Ta_2O_5$ device, as shown in Fig. 3(b), the constriction is also observed at the center of the filament, but there are several clusters, each consisting of several defects as labelled with grey color, being detected within the constriction. A cluster of defects observed at the same location is caused by the same defect repeatedly detected by the RTN technique during a number of the set and reset cycles, indicating that a cluster is actually only one defect that is generated at a fixed location and hardly moves during the switching cycles. The defect generation process causing the over-reset effect could be similar to that causing the permanent component of NBTI/PBTI degradations occurred in conventional high-k metal oxide gate dielectrics [21, 22]. Once generated, these defects cannot move, or be involved in the redox reaction of "normal" mobile defects moving into/out of the constriction during resistive switching [6]. The defect generation could also follow a power law for electric field acceleration with a power factor in the range of 2 and 3. The on-set of over-reset effect observed in the experiments in this work could be explained by the acceleration of defect generation at higher electric field, which happens to overtake the normal reset process at -1.7 V. To verify that the defects generated in the constriction are different from those "normal" ones, we look into the defect movement during the over-reset operations, where defect movements are extracted from the abrupt jump in read current and simultaneous changes in RTN signals, as introduced in detail in [6]. As shown in Fig. 3(d), defects outside of the constriction at HRS are mobile. However, we cannot observe any defect movement occurred to the defects generated during over-reset within the constriction at the center of the filament, i.e. they are not mobile. This is a strong indication that these generated immobile defects are different from those "normal" mobile defects responsible for resistive switching [6, 7], therefore causing partially irrecoverable over-reset phenomenon, due to the co-existence of both types of defects, and both of them could be originated from the positively charged oxygen vacancies, within a few tenths of eV from the electrode's Fermi level [6, 23].

In early work [12] the over-reset has been interpreted as the activation and movement of defects from the BE side into the constriction, subsequently moving further towards TE under a higher reset stop voltage. This results in the constriction being gradually narrowed and shifted. But this assumption cannot explain why this type of defect movement is not reversible. In another work [13], the assumption of horizontal out-diffusion of defects from the filament into the surrounding dielectrics, leading to additional conduction paths, has been used to explain the over-reset. Our results cannot completely rule out this possibility but do provide an alternative explanation supported with experimental evidence. Additional immobile defects are generated in the constriction under strong reset field during over-reset. These defects facilitate current conduction typically through trap-assisted-tunneling, leading to lower resistance at HRS. Meanwhile, their existence in the constriction leads to lower local electric field and makes the reset operation by normal defect movement less effective, even under the over-reset condition. This explains why the RW cannot be fully recovered.

Since the over-reset causes irreversible window reduction, it is desirable to alleviate this phenomenon. As shown in Fig. 3(d), devices formed under different Icc were tested to evaluate its impact, using the same incremental $V_{reset, stop}$ method as shown in Fig. 2. The higher forming $I_{cc}$ leads to higher read-out current at LRS, due to the formation of a stronger filament. All devices reach the maximum HRS at around -1.7 V, with a steeper reset process at higher $I_{cc}$. Interestingly, the extent of over-reset is reduced by using higher $I_{cc}$, which can be explained as follows. The stronger filament formed at higher $I_{cc}$ can only be ruptured at higher $V_{reset}$, leading to a more abrupt reset process. The conduction at HRS becomes less sensitive to the newly-generated defects in the constriction during over-reset, due to the overall larger effective filament cross section caused by higher $I_{cc}$ [4]. Using a higher $I_{cc}$ can alleviate, to some extent, but cannot completely avoid the over-reset problem, due to the defect generation in the filament constriction. A higher forming compliance current will lead to a number of side effects, such as higher power consumption, greater probability of device breakdown, larger resistance variation. The trade-off between higher Icc and lower level of over-reset should be carefully considered in practical application. It cannot be the ultimate solution for memory applications that primarily pursue low-current operation, therefore. Further efforts should be made to increase the critical reset voltage that causes the over-reset, potentially by using materials having lower defect generation rates and higher breakdown voltages.

In summary, the statistical defect profile in the conductive filament of $TiN/TaO_x/Ta_2O_5/TiN$ RRAM devices has been analyzed using the RTN-based defect tracking technique. It is revealed that the constriction region is located at the center of the filament in the $Ta_2O_5$ layer. The irrecoverable over-reset is caused by the generation of immobile defects in the constriction region which facilitates current conduction at HRS and lowers the local field in following set/reset operations. It is also found that a higher forming compliance current can alleviate, to certain extent, the over-reset phenomenon. These findings provide valuable information for improving the on/off window in filamentary metal-oxide RRAM devices.

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