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Towards electromechanical computation: An alternative approach to realize complex logic circuits

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Electromechanical computing based on micro/nano resonators has recently attracted significant attention. However, full implementation of this technology has been hindered by the difficulty in realizing complex logic circuits. We report here an alternative approach to realize complex logic circuits based on multiple MEMS resonators. As case studies, we report the construction of a single-bit binary comparator, a single-bit 4-to-2 encoder, and parallel XOR/XNOR and AND/NOT logic gates. Toward this, several microresonators are electrically connected and their resonance frequencies are tuned through an electrothermal modulation scheme. The microresonators operating in the linear regime do not require large excitation forces, and work at room temperature and at modest air pressure. This study demonstrates that by reconfiguring the same basic building block, tunable resonator, several essential complex logic functions can be achieved. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4961206]

I. INTRODUCTION

Significant research has recently focused on the development of computing elements based on microelectromechanical system or nanoelectromechanical system (MEMS/NEMS) resonators.[1–17] Although there have been successful demonstrations of memory components, fundamental logic gates, as well as multi-bit logic circuits, realization of complex logic circuits has remained elusive. The next natural step moving forward in electromechanical computing is to develop logic circuits capable of performing complex logic operations.

One stream of research has focused on the development of dynamic memory devices utilizing the bistable vibration characteristics of a nonlinear MEMS/NEMS resonator. Two stable vibration amplitudes in the hysteretic regime were defined as the two states of a dynamic memory. The switching between the states was performed by various means, such as the addition of a secondary squared wave signal to the AC driving signal,[1] modulation of the DC signal,[3] or change in the DC magnetic field.[9] Also, a logic-memory device[6] and a binary counter[7] were demonstrated utilizing feedback control to switch between the two vibrational states of nonlinearly resonating MEMS resonators. A mechanical random access memory device has been demonstrated based on the nonlinear vibration of a piezoelectrically active localized membrane resonator in a phonon circuit.[8]

The other stream of research has focused on the development of logic devices based on both linear and nonlinear operations of the MEMS/NEMS resonators.[10–16] The first resonator-based logic gates were realized by utilizing the presence of high (low) amplitude of vibration at on-resonance (off-resonance) of a NEMS resonator in the linear regime.[10] Later, the bistability of a nonlinear NEMS resonator was used to realize a reprogrammable logic function, such as 2-bit AND/NAND and OR/NOR gates.[11] A universal logic device capable of performing parallel operations of 2-bit AND, OR, and XOR logic functions as well as multi-bit logic operations was realized based on a parametrically excited electromechanical resonator.[12,13] Later, several components of a microcomputer, namely, a byte memory, a shift register, and a controlled-Not gate, have been successfully realized based on the parametric electromechanical excitation.[14] It was a remarkable advancement towards building a realistic computing framework where crucially all these functions were underpinned by the same physical principle, i.e., parametric resonance. Recently, an unconventional and reversible logic gate (Fredkin gate) has been realized based on the four coupled linear NEMS resonators.[15] Both physical and logical reversibilities were demonstrated with successful implementation of 2-bit AND, OR, NOT, and FANOUT gates. More recently, we have proposed and demonstrated a reprogrammable microelectromechanical logic device based on the electrothermal frequency tuning of a linearly excited MEMS arch shaped resonator.[16] We have demonstrated all the fundamental 2-bit and selective n-bit logic operations on a single device. The same device has been also demonstrated to function as a memory device.[17]

To build a realistic electromechanical computing machine, different functional elements, such as memory, logic gates, and complex logic circuits, need to be developed within a single conceptual framework.[14] We demonstrate here an alternative approach to construct complex logic circuits based on the electrothermally tunable multiple MEMS resonators, where complex logic functions are executed through reconfiguring the electrothermal actuation circuits. The basic concept will be demonstrated in this paper through

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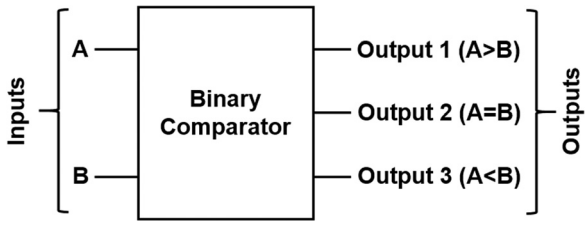

FIG. 1. Block diagram of a single-bit comparator.

several logic elements, mainly a single-bit binary comparator, 2-bit parallel logic gates, and a single-bit 4-to-2 encoder. As indicated previously, we realize these functions based on the basic building block of electrothermally tuned linear MEMS resonators, thereby vividly illustrating the prospect of building a single conceptual framework towards the realization of an electromechanical computer.

II. CASE STUDIES

A. A binary comparator

A binary comparator is a combinational logic circuit, which compares two binary inputs, A and B, and produces three outputs representing A = B (equality), A > B (greater than), and A < B (less than) functions. Figure 1 shows a block diagram of a single-bit comparator with the corresponding inputs, A and B, and the three outputs, namely, Output 1 (A > B), Output 2 (A = B), and Output 3 (A < B). Table I shows the corresponding truth table of a single-bit binary comparator. Based on the input bit patterns, only one of its outputs can be high. In Secs. II A 1–II A 3, we show how the proposed resonator based circuit performs the desired operation of a single-bit comparator.

Figure 2(a) shows an SEM image of an arch microbeam resonator. The microresonators' fabrication process has been described elsewhere.[16] The dimensions of the arch beams are 500 μm in length, 3 μm in width, and 30 μm in thickness (thickness of the Si device layer of a silicon on insulator wafer). The gap between the actuating electrode and the resonating beam is 8 μm at the fixed anchors and 11 μm at the mid-point of the microbeam due to its 3 μm initial curvature. Figure 2(b) shows a schematic of the experimental setup for realizing the proposed comparator using three electrically connected arch microresonators. The pictorial top view depicts drive electrodes, sense electrodes, and the three arch microbeam resonators (Res. 2 in yellow, Res. 1 and Res. 3 in violet).

TABLE I. Truth table of a single-bit comparator showing two inputs, A and B, and three outputs, namely, Output 1 (A > B), Output 2 (A = B), and Output 3 (A < B).

Inputs		Outputs		
A	B	Output 1 (A > B)	Output 2 (A = B)	Output 3 (A < B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Res. 1, Res. 2, and Res. 3 are placed in between node 1–2, node 2–3, and node 3–4, respectively. All the drive electrodes are electrically connected and provided with the same AC drive signal from the output port of the network analyzer (Agilent E5071C) at node 5. All the microbeams are biased with a single DC voltage source, $V_{DC} = 40$ V, connected at node 4. The three outputs, namely, Output 1 (node 6), Output 2 (node 7), and Output 3 (node 8), demonstrate A > B (greater than), A = B (equality), and A < B (less than) functions, respectively. These outputs are connected to a low noise amplifier (LNA), one at a time, to amplify the AC current generated due to the in-plane motion of the corresponding microbeam at resonance. The output of the LNA is coupled to the network analyzer input port for S_{21} transmission signal measurement. Note that for practical realization of the proposed comparator, all three outputs need to be measured simultaneously; however, as a proof of concept, we sense here the outputs discretely. All the experiments have been conducted at 1 Torr pressure and at room temperature with the following preset conditions: $V_{DC} = 40$ V, $V_{AC} = 0$dBm (0.224V_{rms}), and AC operating frequency, $f_{op} = 143$ kHz. Note that the preset conditions are only chosen for the particular frequency of operation and it is by no means restricted to this single value. In fact, any values of V_{DC}, V_{AC}, and pressure can be selected to get linear operating condition, and accordingly, the thermal voltages should be selected for successful logic operation. We use three nominally identical arch resonators: Res. 1, Res. 2, and Res. 3 of resonance frequencies 122–124 kHz. When measuring the resistances across the anchors of the individual resonators, Res. 1 and Res. 3 show identical resistances of 115 Ω, whereas Res. 2 shows 117 Ω. Note that capacitive parasitic feedthrough is intrinsic to all electrically interfaced micromechanical resonators resulting in increased challenges to their integration in more complex circuits, particularly as devices

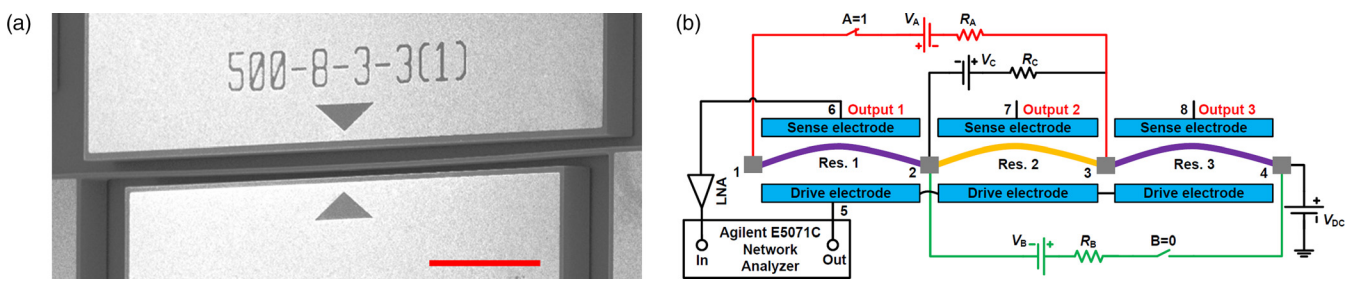

FIG. 2. (a) An SEM image of the arch microbeam resonator. The scale bar is 100 μm. (b) Schematic of the comparator realized using three electrically coupled arch microresonators. V_A and V_B represent two binary inputs controlled by switches A and B, respectively. Three logic outputs are obtained from the three resonator sensing ports, namely, Output 1(A > B), Output 2(A = B), and Output 3(A < B).

are scaled to operate at higher frequencies. The sources of this capacitive feedthrough parasitic include direct overlap capacitance of the transducer, capacitive coupling through the substrate, interconnects, and bond pads. Although the estimated feedthrough capacitance for the devices used in these studies is relatively small (typically around pF), for applications operating in the high frequency (HF) region, the electrical path through this capacitor is significant and could potentially obscure any observable signal from the motion of the structure. Hence, it is necessary to cancel the effect of the feedthrough signal using active feedthrough signal cancellation circuits and/or using data post-processing techniques. Here, we employed data post-processing technique to extract the motional signal.[18,19] Toward this, we first measure the S_{21} signal using the network analyzer and save the data into the memory while keeping the DC bias to zero. In this case, the data only contain the parasitic feedthrough signal. Then, we measure the S_{21} transmission signal through the device by applying the DC bias; hence, it contains both the motional and feedthrough components. Then, we subtract the memory data from the final data, which results into the desired motional signal only.

Next, the curvature of Res. 2 is adjusted from its initial fabricated value of 3 μm by passing a DC current through it using a voltage source, $V_C = 0.7$ V, and a series resistance, $R_C = 50\ \Omega$, as shown in Fig. 2(b). This DC current induces resistive heating, and accordingly compressive stress on the microbeam, which increases its curvature and stiffness. As a result, the resonance frequency of Res. 2 increases, which is measured around 143 kHz. We use this frequency (143 kHz) as the operating frequency for the demonstration of the comparator operation. Hence, Res. 2 will vibrate at on-resonance state at this frequency, while Res. 1 and Res. 3 will be at off-resonance. This represents the case for the binary input condition (0,0). Note that this is a necessary condition for realizing the proposed comparator.

It is worth to mention here that we have used nominally identical resonators for the implementation of the proposed comparator, and thus, it was necessary to use V_C to set the resonance frequency of Res. 2 at a higher value compared to Res. 1 and Res. 3 to demonstrate the proof-of-concept. By intentionally fabricating Res. 2 with a higher resonance frequency compared to Res. 1 and Res. 3, one can eliminate the need for V_C. The use of V_C actually demonstrates the flexibility of our proposed approach for realizing the desired complex logic operations since it does not rely on perfect fabrication tolerances.

Next, two logic inputs are provided with two separate DC voltage sources, V_A (0.4 V) and V_B (1.3 V), connected across nodes 1–3 and node 2–4, respectively, with the corresponding series resistances, $R_A = 50\ \Omega$ and $R_B = 50\ \Omega$ along with two switches, A and B, as shown in Fig. 2(b). The difference in the voltage levels for inputs A and B is due to the necessary presence of V_C in our experimental setup. Otherwise, both voltage sources are expected to be nominally identical. The binary logic input 1(0) is represented by connecting (disconnecting) V_A and V_B from the electrical network by the two switches A and B, respectively. Hereafter, switch ON (OFF) condition for switches A and B corresponds to the binary logic input 1(0). The sensing electrodes are used to obtain the logic outputs, where a high (low) S_{21} transmission signal at the on-resonance (off-resonance) state corresponds to logic output 1(0).

Figure 3 shows the electrical circuit diagram for the electrothermal actuation for implementing the proposed comparator, which shows the corresponding DC current flow through the microbeams at different logic input conditions. For logic input condition, A = B = 0, the currents flowing through Res. 1 and Res. 3 are zero, as shown in Fig. 3(a). At the same time, the current flowing through Res. 2 is I_{R2} due to the applied DC voltage, V_C. At $f_{op} = 143$ kHz, both Res. 1 and Res. 3 are at off-resonance, while Res. 2 is at on-resonance. Hence, the signal detected at Output 2 is high (1), whereas the signals from Output 1 and Output 3 are low (0).

For logic input condition, A = 0 and B = 1, there is no current flow through Res. 1, but there are DC currents flowing through Res. 2 and Res. 3, as shown in Fig. 3(b). The amount of current through Res. 2 is now I'_{R2}, which is different from I_{R2}. Hence, it changes the resonance frequency of Res. 2 from its initial value of 143 kHz to some other value, making it vibrating at off-resonance at $f_{op} = 143$ kHz. Due to the proper choice of voltage amplitude for V_B (1.3 V), the current I_{R3}, which flows through Res. 3, shifts its resonance frequency to 143 kHz. Consequently, both Res. 1 and Res. 2 are off-resonance, while Res. 3 is on-resonance. Thus, the signal from Output 1 and Output 2 will be low (0), and at the same time, it will be high (1) from Output 3.

For the logic input condition, A = 1 and B = 0, there is no current flow through Res. 3, but DC currents flow through Res. 1 and Res. 2, Fig. 3(c). The amount of current flow through Res. 2 is now $I''_{R2} \neq I_{R2}$, which changes its resonance frequency making it vibrate at off-resonance at $f_{op} = 143$ kHz. At the same time, I_{R1}, which flows through Res. 1, shifts its resonance frequency to 143 kHz due to the proper choice of the voltage amount ($V_A = 0.4$ V). This indicates that both Res. 2 and Res. 3 are off-resonance and only Res. 1 is on-resonance at $f_{op} = 143$ kHz. Hence, the output from Output 2 and Output 3 will be low (0) and high (1) from Output 1.

When A = B = 1, the currents flowing through Res. 1 and Res. 3 are I'_{R1} and I'_{R3}, respectively, which shift their corresponding resonance frequencies away from $f_{op} = 143$ kHz. However, due to the polarity arrangement of the voltage sources, V_A and V_B, the current flow through Res. 2 is $I'''_{R2} \approx I_{R2}$, as shown in Fig. 3(d). The reason is that the additional currents flowing through Res. 2 due to the presence of both voltage sources (V_A and V_B) are nominally identical in magnitude but opposite in direction; hence, they cancel each other. As a result, the resonance frequency of Res. 2 remains unchanged at 143 kHz. Thus, Res. 1 and Res. 3 are off-resonance, while Res. 2 is on-resonance at $f_{op} = 143$ kHz. Consequently, Output 1 and Output 3 will show low (0) and Output 2 will show high (1) S_{21} transmission signal.

In Secs. II A 1–II A 3, we provide frequency response plots and time sweep data for the proposed comparator and demonstrate its successful operation.

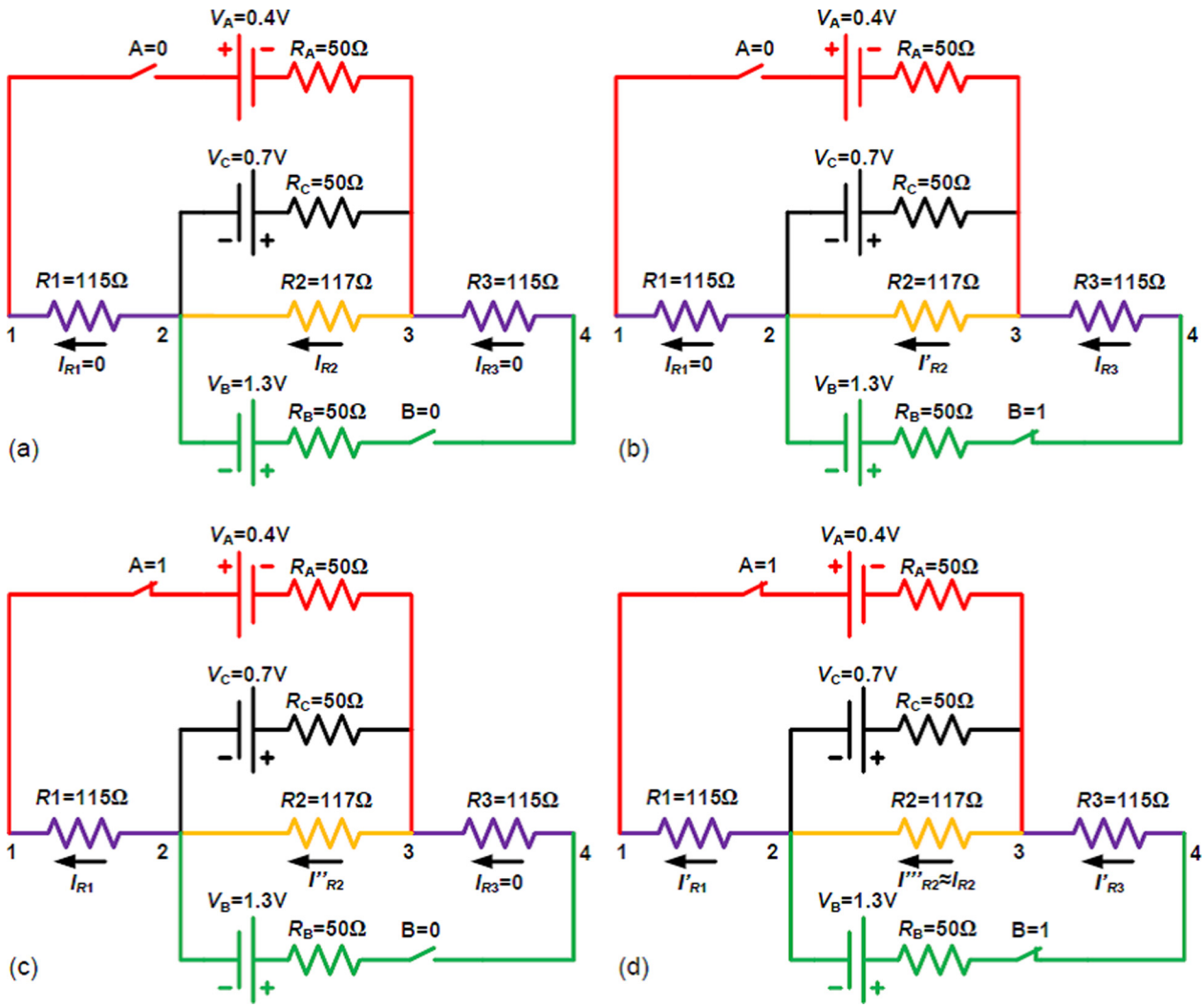

FIG. 3. Electrical circuit configurations for the different logic input conditions. (a) The electrical circuit represents the (0,0) logic input condition where the current flowing through Res. 1, Res. 2, and Res. 3 are $I_{R1}=0$, I_{R2}, and $I_{R3}=0$, respectively. (b) The electrical circuit representing the (0,1) logic input condition, where the current flowing through Res. 1, Res. 2, and Res. 3 is $I_{R1}=0$, I'_{R2}, and I_{R3}, respectively. (c) The electrical circuit representing the (1,0) logic input condition, where the current flowing through Res. 1, Res. 2, and Res. 3 is I_{R1}, I''_{R2}, and $I_{R3}=0$, respectively. (d) The electrical circuit representing the (1,1) logic input condition, where the current flowing through Res. 1, Res. 2, and Res. 3 are I'_{R1}, $I'''_{R2}\approx I_{R2}$, and I'_{R3}, respectively.

1. Input A "greater than" input B

The comparator function "Input A 'greater than' Input B" is realized on Res. 1 (Output 1) at node 6. The frequency responses of Res. 1 (Output 1) for different logic input conditions are shown in Fig. 4(a). The frequency responses due to logic inputs (0,0), (0,1), (1,0), and (1,1) are plotted in black, red, blue, and green, respectively. For both logic inputs (0,0) and (0,1), the voltage source V_A is disconnected from the electrical network responsible for the electrothermal actuation, as shown in Figs. 3(a) and 3(b), as switch A is in OFF (0) state for each case. Hence, Res. 1 is on-resonance around 122 kHz, showing low S_{21} transmission signal at $f_{op}=143$ kHz (in black and red). For logic input (1,0), the voltage source V_A is connected to the electrical network, Fig. 3(c), as switch A is in the ON state. Res. 1 is now on-resonance at $f_{op}=143$ kHz; hence, it shows high S_{21} transmission signal (in blue). For logic input (1,1), both voltage sources V_A and V_B are connected to the electrical network, Fig. 3(d), since both switches A and B are in the ON state. The total current in this case is different than logic input condition (0,1) case ($I'_{R1}\neq I_{R1}$); hence, it modulates the resonance frequency of Res. 1 to around 155 kHz, away from $f_{op}=143$ kHz (in green). Output 1 shows high S_{21} transmission signal at $f_{op}=143$ kHz in this case, denoting logic output (1). The time response of Res. 1 (Output 1) is depicted in Fig. 4(b), showing S_{21} transmission signal (in red) corresponding to Input A "greater than" Input B function and the corresponding binary inputs A and B. It clearly shows that when input A = 1 and B = 0, the S_{21} transmission signal has logic high (1), whereas it is low (0) for all other conditions.

2. Input A "less than" input B

The comparator function "Input A 'less than' Input B" is realized on Res. 3 (Output 3) at node 8. The frequency responses of Res. 3 (Output 3) for different logic input conditions are shown in Fig. 5(a). The frequency responses due to logic inputs (0,0), (0,1), (1,0), and (1,1) are plotted in black, red, blue, and green, respectively. For both logic inputs (0,0)

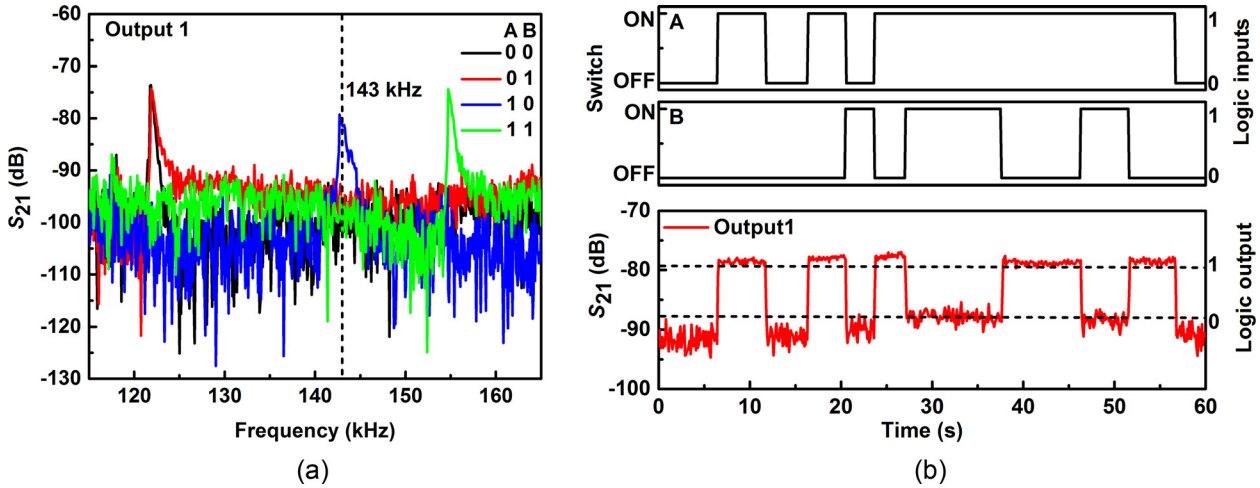

FIG. 4. (a) Frequency responses of Res. 1 from Output 1 for different logic input conditions where (1,0) logic input condition shown in blue has high S_{21} signal at 143 kHz and others have low signal represented by 1 and 0, respectively. (b) Demonstration of Input A "greater than" Input B (A > B) logic function when the frequency of the AC input signal is chosen as 143 kHz. Two input signals A and B are shown in black, where the switch OFF/ON corresponds to 0/1 input conditions. The S_{21} transmission signal in red corresponds to logic output and fulfills the comparator A > B function.

and (1,0), the voltage source V_B is disconnected, as shown in Figs. 3(a) and 3(c) (switch B is OFF (0)). Hence, Res. 3 vibrates at on-resonance state around 124 kHz, showing low S_{21} transmission signal at $f_{op} = 143$ kHz (in black and blue). For logic input (0,1), the voltage source V_B is connected as shown in Fig. 3(b) (switch B is in ON). Res. 3 is now on-resonance at $f_{op} = 143$ kHz; hence, it shows high S_{21} transmission signal at this frequency (in red). For logic input (1,1), both voltage sources V_A and V_B are connected to the electrical network, Fig. 3(d), since both switches A and B are ON. The total current in this case is different than the logic input (1,0) case ($I'_{R3} \neq I_{R3}$); hence, it modulates the resonance frequency of Res. 3 to around 155 kHz, away from $f_{op} = 143$ kHz (in green). Output 3 shows low S_{21} transmission signal at $f_{op} = 143$ kHz. The time response of Res. 3 (Output 3) is depicted in Fig. 5(b), showing S_{21} transmission signal (in green) corresponding to Input A "less than" Input B function and the corresponding binary inputs A and B. It clearly shows that only for inputs A = 0 and B = 1, the S_{21} transmission signal has logic high (1), whereas it is low (0) for all other conditions.

3. Input A "equal to" input B

The comparator function "Input A 'equal to' Input B" is realized on Res. 2 (Output 2) at node 7. The AC driving frequency is fixed at $f_{op} = 143$ kHz, as before. The frequency responses of Res. 2 (Output 2) for different logic input conditions are shown in Fig. 6(a). The frequency responses due to logic inputs (0,0), (0,1), (1 0), and (1,1) are plotted in black, red, blue, and green, respectively. For logic input (0,0), the voltage sources V_A and V_B are disconnected, Fig. 3(a) (switches A and B are OFF (0)). Hence, Res. 2 vibrates at on-resonance state around 143 kHz due to the I_{R2} flowing through Res. 2 due to V_C. Res. 2 shows a high S_{21} transmission signal at $f_{op} = 143$ kHz (in black). For logic input

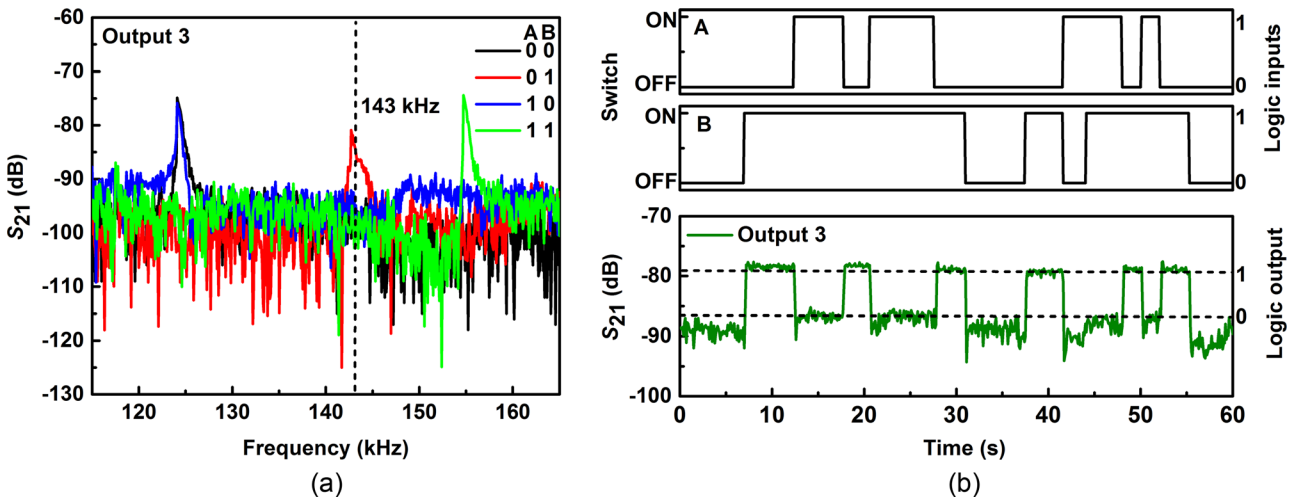

FIG. 5. (a) Frequency responses of Res. 3 from Output 3 for different logic input conditions where (0,1) logic input condition shown in red has high S_{21} signal at 143 kHz and others have low signal represented by 1 and 0, respectively. (b) Demonstration of Input A "less than" Input B (A < B) logic function when the frequency of the AC input signal is chosen as 143 kHz. Two input signals A and B are shown in black, where the switch ON (OFF) corresponds to 1(0) input condition. The S_{21} signal in green corresponds to logic output and fulfills the comparator A < B function.

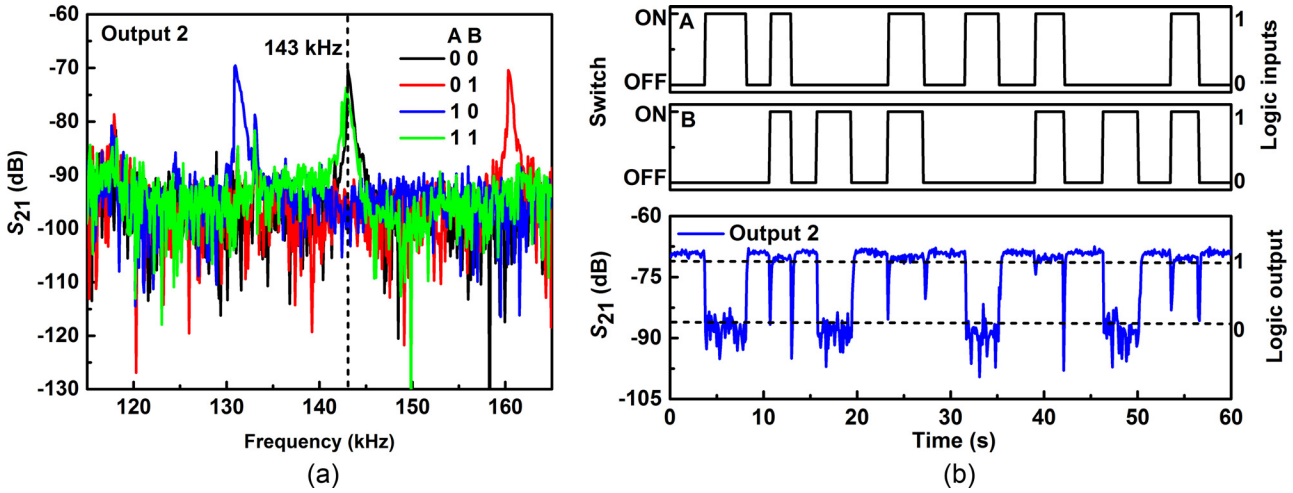

FIG. 6. (a) Frequency responses of Res. 2 from Output 2 for different logic input conditions, where (0,0) and (1,1) logic inputs shown in black and green have high S_{21} signal at 143 kHz and others have low signal represented by 1 and 0, respectively. (b) Demonstration of Input A "equal to" Input B (A = B) when the frequency of the AC input signal is chosen as 143 kHz. Two input signals A and B are shown in black, where the switch OFF/ON corresponds to 0/1 input conditions. The S_{21} signal in blue corresponds to logic output and fulfills the comparator A = B function.

conditions (0,1), the voltage source V_B is connected to the electrical network as shown in Fig. 3(b). The current flowing through Res. 2 in this case is $I'_{R2} \neq I_{R2}$ as switch B is in the ON state only. As a result, Res. 2 is now at resonance around 162 kHz; hence, off-resonance at $f_{op} = 143$ kHz, showing low S_{21} transmission signal at that operating frequency (in red). For logic input condition (1,0), the voltage source V_A is connected to the electrical network as shown in Fig. 3(c). The current flowing through Res. 2 in this case is $I'_{R2} \neq I_{R2}$ as switch A is in the ON state only. As a result, Res. 2 is now at resonance around 135 kHz; hence, off-resonance at $f_{op} = 143$ kHz shows low S_{21} transmission signal at that operating frequency (in blue). Finally, for logic input (1,1), both voltage sources V_A and V_B are connected, Fig. 3(d), and both switches A and B are in the ON state. The total current in this case flowing through Res. 2 is I'''_{R2}. However, due to the assigned polarity of V_A and V_B, the resulting current from these voltage sources through Res. 2 cancels each other; hence, $I'''_{R2} \approx I_{R2}$. Thus, Output 2 shows high S_{21} transmission signal at $f_{op} = 143$ kHz (in green). Fig. 6(b) depicts the time response of Res. 2 (Output 2), showing S_{21} transmission signal (in blue) corresponding to Input A "equal to" Input B function and the corresponding binary inputs A and B. It clearly shows that for input A = B = 0/1, the S_{21} transmission signal shows logic high (1), whereas it is low (0) for all other conditions.

The truth table in Table II shows full agreement with that of a 1-bit binary comparator shown in Table I.

TABLE II. Truth table obtained from the experimental results, which match that of Table I.

Inputs		Outputs		
A	B	Out 1 (S_{21}) A > B	Out 2 (S_{21}) A = B	Out 3 (S_{21}) A < B
0	0	0 (−90 dB)	1 (−65 dB)	0 (−90 dB)
0	1	0 (−90 dB)	0 (−85 dB)	1 (−78 dB)
1	0	1 (−78 dB)	0 (−85 dB)	0 (−90 dB)
1	1	0 (−90 dB)	1 (−68 dB)	0 (−90 dB)

B. Parallel logic gates

Parallel logic operation in a single architecture is of paramount importance as it offers the possibility of energy cost reduction per logic operation. We demonstrate here that the same architecture of Fig. 2 can be utilized to realize parallel logic operations.

1. XOR/XNOR

One can note that Output 2, Fig. 6, performs a 2-bit XNOR logic operation at $f_{op} = 143$ kHz. Interestingly, once the other two outputs (Output 1 and Output 3) are combined together, it produces a 2-bit XOR logic operation at $f_{op} = 143$ kHz. Hence, it is possible to realize 2-bit XOR and XNOR simultaneously, on a single architecture, which were used to demonstrate the comparator operation in Sec. II A.

2. AND/NOT

We can also perform a 2-bit AND logic operation on either Res. 1 output (Output 1) or Res. 3 output (Output 3) or on the combined output (Output 1 and Output 3 connected together), by selecting a proper AC driving frequency. Based on Figs. 4(a) and 5(a), one can note that the outputs show high S_{21} transmission signal at 155 kHz only for the logic input condition of (1,1). Hence, by selecting 155 kHz as the AC driving frequency, a successful realization of AND operation is feasible where only (1,1) logic condition will produce logic output high (1). Also, by setting logic Input B at high state (switch ON), one can perform NOT operation on the Output 3 at $f_{op} = 143$ kHz. In this case, Output 3 will produce complementary logic output with respect to logic input A, i.e., when logic Input A is high (1), Output 3 is low (0) and vice versa.

These demonstrations of parallel 2-bit XOR/XNOR as well as AND/NOT logic gates vividly illustrate the fact that the proposed architecture can be potentially used as a reprogrammable logic architecture where different logic

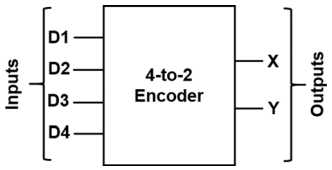

FIG. 7. Block diagram of a single-bit 4-to-2 encoder.

operations can be realized by simply selecting different output ports and choosing the right operating frequency.

C. A single-bit 4-to-2 encoder

An encoder is a digital device that compresses information for efficient transmission or storage by converting data into a code. In principle, a single-bit 4-to-2 encoder converts 4 input bits into 2 output bits. Fig. 7 shows the block diagram of a single-bit 4-to-2 encoder with the corresponding inputs D1, D2, D3, and D4, and outputs X and Y, respectively. The working principle of a 4-to-2 encoder is as follows: the electrical signals are at low level at both Outputs X and Y, representing logic output (0 0) for input condition D1 = 1, D2 = 0, D3 = 0, and D4 = 0. For the case of D1 = 0, D2 = 1, D3 = 0, and D4 = 0, the Output Y is high while the Output X is low, representing logic output (0 1). The electrical signal is high at Output X and low at Output Y, representing the logic output (1 0), for the input case D1 = 0, D2 = 0, D3 = 1, and D4 = 0. Finally, both Outputs X and Y are high, representing logic output (1 1), for input condition D1 = 0, D2 = 0, D3 = 0, and D4 = 1. The corresponding truth table is provided in Table III.

Fig. 8 shows a schematic of the configuration for realizing the proposed encoder using two electrically connected arch microresonators. The specifications of the arches are the same as those used for the comparator of Fig. 2(a), except they differ in the internal induced axial force from fabrication. The resonance frequency and microbeam resistance for these resonators are measured around 120 kHz and 118 Ω, respectively. Res. Y and Res. X are placed in between nodes 1 and 2, and 2 and 3, respectively. All the drive electrodes are electrically connected and provided with an AC signal from the output port of the network analyzer (Agilent E5071C) at node 4. The microbeams are electrically connected in series and biased with a DC voltage source, $V_{DC} = 40$ V, at node 3. The two Outputs, X (at node 6) and Y (at node 5), constitute the encoder output. These output ports are connected to a low noise amplifier (LNA), one at a time, to amplify the AC current generated due to the in-plane

TABLE III. Truth table of a single-bit 4-to-2 encoder showing four data inputs, D1, D2, D3, and D4, and two outputs, X and Y.

Inputs				Outputs	
D1	D2	D3	D4	X	Y
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

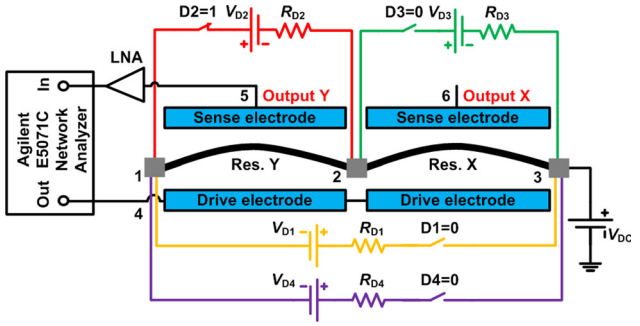

FIG. 8. Schematic of the proposed 4-to-2 encoder using two electrically connected arch microresonators. Four input bits correspond to four switches, D1, D2, D3, and D4. Switch ON (OFF) corresponds to input 1(0) for all the switches. Two outputs for the encoder are X and Y.

motion of the corresponding microbeam resonator to measure S_{21} transmission signal. The high (low) S_{21} transmission signal sensed at the Output ports, X and Y, at the on-resonance (off-resonance) state is defined as the output 1(0). Four DC voltage sources, $V_{D1} = 0.6$ V, $V_{D2} = 0.52$ V, $V_{D3} = 0.52$ V, and $V_{D4} = 1.04$ V, are suitably connected across the microbeams with four resistors, $R_{D1} = R_{D2} = R_{D3} = R_{D4} = 50$ Ω, and four switches, D1, D2, D3, and D4, respectively. This arrangement then forms the inputs for the proposed encoder where the switch ON (OFF) condition for each of these switches is defined as input 1(0).

It is worth to mention that the proposed encoder is a common encoder, not a priority encoder. It is active when one of the inputs (D1, D2, D3, and D4) is high (switch ON). Therefore, only four input combinations (1 0 0 0, 0 1 0 0, 0 0 1 0, 0 0 0 1) are possible. It is also worth to mention that no matter whether the input D1 is ON (1) or OFF (0), the corresponding encoder output is always (0 0). Note that all the experiments have been conducted at a pressure = 1 Torr, temperature = 25 °C, $V_{AC} = 0$ dBm (0.224V_{rms}), and $f_{op} = 140$ kHz.

Fig. 9 shows the electrical circuit diagram for the electrothermal actuation scheme to implement the proposed encoder. It shows the corresponding DC current flow through the microbeams for different encoder input conditions. The frequency responses of the microresonators sensed at Output X and Output Y for different encoder inputs are shown in Figs. 10(a) and 10(b), respectively. The frequency responses for inputs (1 0 0 0), (0 1 0 0), (0 0 1 0), and (0 0 0 1) are plotted in black, red, blue, and green, respectively. For the encoder input (1 0 0 0), the DC current flow through Res. X and Res. Y is $I'_X = I'_Y$, as shown in Fig. 9(a). Due to the choice of the voltage load, $V_{D1} = 0.6$ V, both resonators are at on-resonance state around 125 kHz, but importantly, at the off-resonance state at $f_{op} = 140$ kHz. Hence, both Outputs X and Y will show low S_{21} transmission signal, representing the encoder output (0 0). For input (0 1 0 0), the DC currents through Res. X and Res. Y are $I_X = 0$, and I_Y, respectively, Fig. 9(b). In this case, Res. Y is at the on-resonance state at 140 kHz, as shown in Fig. 10(b), while Res. X is at the on-resonance state at 120 kHz, Fig. 10(a). Hence, for this encoder input, Output X is (0) and Output Y is (1) at $f_{op} = 140$ kHz, representing the encoder output (0 1).

For input (0 0 1 0), the DC currents flowing through Res. X and Res. Y are I_X and $I_Y = 0$, respectively, Fig. 9(c).

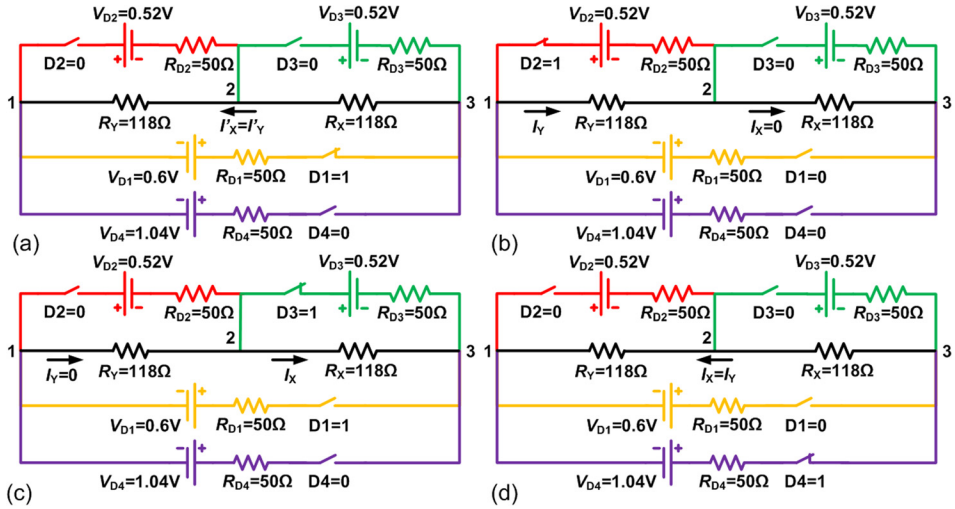

FIG. 9. Electrical circuit configurations for the different encoder input conditions. (a) For (1 0 0 0) input, the currents flowing through Res. X and Res. Y are $I'_X = I'_Y$. (b) For (0 1 0 0) input, the currents flowing through Res. X and Res. Y are $I_X = 0$ and I_Y, respectively. (c) For (0 0 1 0) input, the currents flowing through Res. X and Res. Y are I_X and $I_Y = 0$, respectively. (d) For (0 0 0 1) input, the currents flowing through Res. X and Res. Y are $I_X = I_Y$.

In this case, Res. X is at the on-resonance state at $f_{op} = 140$ kHz, Fig. 10(a), while Res. Y is at the on-resonance state at 120 kHz, Fig. 10(b). Thus, Output X is (1) and Output Y is (0) at $f_{op} = 140$ kHz, representing the encoder output (1 0). Finally, for input (0 0 0 1), the DC current flows through Res. X and Res. Y are $I_X = I_Y$, Fig. 9(d). Due to the DC voltage, $V_{D4} = 1.04$ V, both Res. X and Res. Y are at the on-resonance state at 140 kHz, as shown in Figs. 10(a) and 10(b), respectively. Hence, it will produce the encoder output (1 1) at $f_{op} = 140$ kHz.

The time responses of the microresonators sensed at Output X and Output Y are shown in Figs. 11(a) and 11(b), respectively. The input signals (D1, D2, D3, and D4) are plotted as switches and their high (1) and low (0) levels are represented by the ON and OFF conditions, respectively. The S_{21} transmission signal at Output X is plotted in green, Fig. 11(a). The high (1) level is defined at −70 dB and the low level is defined at −88 dB. For logic inputs (0 0 1 0) or (0 0 0 1), switch D3 or D4 is ON. For each of these conditions, Res. X is at the on-resonance state at 140 kHz and shows high (1) S_{21} transmission signal. Similarly, for logic inputs (0 1 0 0) or (0 0 0 1), switch D2 or D4 is ON, Fig. 11(b). The S_{21} transmission signal at Output Y is plotted in pink. The high (1) level is defined at −72 dB and the low level is defined at −82 dB.

Note that for Output X, the signal levels are the same for logic (0) but slightly different for logic (1) for different encoder inputs. This is mainly due to the different amplitude levels of the responses of the microresonators for different inputs. Similar explanation is also applicable for Output Y. However, for a correct threshold value defined for the logic output levels (1 or 0), the proposed circuit performs the desired logic operations of a single-bit 4-to-2 encoder successfully. Finally, the truth table in Table IV shows full agreement with that of a single-bit 4-to-2 encoder shown in Table III.

III. DISCUSSION

The flexibility to construct complex logic circuits is vital for realizing high logic depth. In principle, resonator based logic devices are faced with two pressing challenges that may hinder their application in building complex logic circuits, which are essential for computation. The first challenge is the strength of the output AC signal, which requires a transimpedance amplifier. Second is the fact that the signal waveforms as logic inputs and logic outputs are often of different forms.[10–16] Apart from the work in Ref. 14, these unavoidable obstacles have restricted the development of complex logic circuits based on resonators. In this work, the complexity in the logical operations is performed at the actuating circuit level (electrothermal actuation), whose output is a DC electric current passing through various resonators to modulate their respective resonance frequencies. In other words, the required logic operations to achieve complex

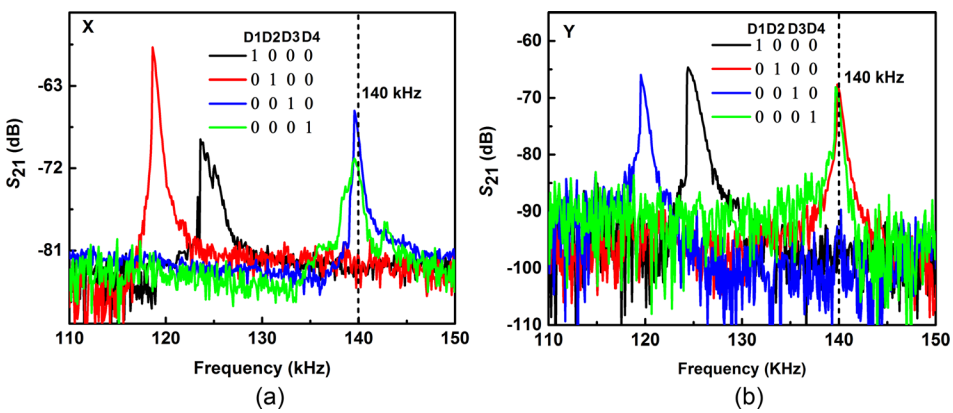

FIG. 10. (a) The frequency response of Res. X sensed at Output X for four different inputs shown in black, red, blue, and green, respectively. (b) The frequency response of Res. Y sensed from Output Y for four different inputs shown in black, red, blue, and green, respectively.

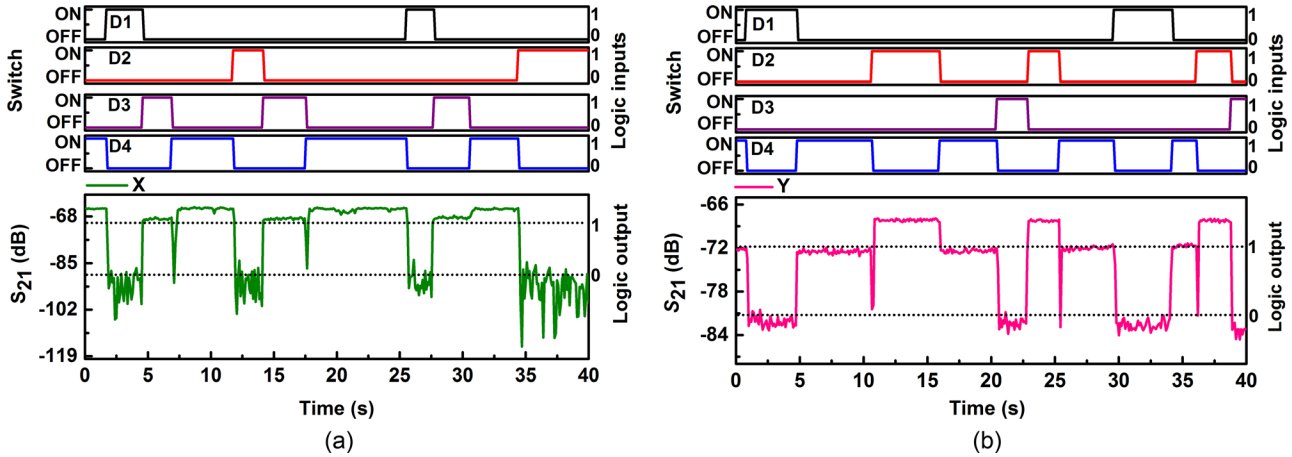

FIG. 11. (a) Time response of the device from Output X. Four input signals D1, D2, D3, and D4 are represented by black, red, purple, and blue, respectively. Switch ON (OFF) is represented by 1(0). The S_{21} signal in green corresponds to the logic Output X. (b) Time response of the device from Output Y is shown in pink. Four input signals D1, D2, D3, and D4 are represented by black, red, purple, and blue, respectively.

logic functions are executed at the actuating circuit level, hence eliminating the need for any serial connection between the inputs and outputs of multiple microresonators. The final logic outcome depends on the resonance states of the individual resonators in the system, which are controlled by the amount and direction of the electrothermal DC current passing through the microbeams for each logic input conditions. This approach eliminates the need for any intermediate AC/DC converters and/or amplifier circuits simply because no series connection exists between resonators. Although the sensing circuitry needs CMOS based amplifier circuits, the present results are encouraging for the development of other necessary complex logic circuits based on suitably arranged electrothermally tunable microresonators.

The energy cost and speed of logic operation, sensitivity to temperature variation, and sensitivity to phase noise are crucial aspects to be considered for any resonator based computing. All these aspects have been discussed in detail in Ref. 16 for similar experimental conditions and device geometries. It is worth to mention that electrothermal actuation needs to be optimized to minimize the generated heat. The required thermal load can be minimized in several ways to enhance the effectiveness of the proposed architectures. One can reduce the resistance of the mechanical structure and thus reduce the thermal load to reach the desired resonance frequencies. Also, by properly selecting narrow frequency ranges from the as fabricated values for the desired logic operations, the required thermal loads can be minimized.

TABLE IV. Single bit 4-to-2 encoder truth table obtained from the experimental results, which match that of Table III.

Inputs				Outputs	
D1	D2	D3	D4	X (S_{21})	Y (S_{21})
1	0	0	0	0 (−88 dB)	0 (−82 dB)
0	1	0	0	0 (−88 dB)	1 (−68 dB)
0	0	1	0	1 (−70 dB)	0 (−82 dB)
0	0	0	1	1 (−66 dB)	1 (−72 dB)

It is also worth to mention that the core concept utilized here is to influence the stiffness of a structure actively such as that one can change its resonance frequency on demand. Hence, by selecting an operating frequency, the structure can be either at resonance (on condition) or off-resonance (off condition). Through this active axial force (through electrothermal heating in this case), we have the ability to put the structure at on- or off-resonance which can be treated as logic bit 1 or 0. In addition, mechanical devices are radiation-hard and can survive severe electromagnetic radiations (for example, in space applications). Under these conditions, transistor-based devices usually do not survive. Moreover, small mass of the microbeam facilitates excellent shock resistance.

IV. CONCLUSIONS

In summary, we have demonstrated an alternative approach to construct complex logic circuits, where the required logic functions are executed through reconfiguring the electrothermal actuation circuits of multiple resonators. We demonstrated several essential computing elements, which depend on complex logic operations, based on a single conceptual framework: an electrothermal frequency tuning. The standard electrostatic transduction technique and the CMOS friendly fabrication techniques used in this work naturally allow the systems to be compact and integrated on-chip. The demonstration of complex logic elements based on a single conceptual framework is a promising step toward achieving the ultimate goal of an electromechanical microcomputer.

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