Fault Mode Operation Strategies for Dual H-Bridge Current Flow Controller in Meshed HVDC Grid

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Abstract

Current flow controllers (CFCs) can remove grid bottlenecks or extend grid operation area by changing amount of power flowing through dc transmission lines. This study focuses on behavior of interline H-bridge CFC in a dc grid in fault condition. In addition to the CFC circuit level fault studies, non-linear and linearized simplified models are developed for system level analysis. The analysis and fault study shows that the interline H-bridge CFC cannot survive during DC transmission line and bus faults due to an overvoltage occurring in its capacitor. Further investigation figures out that this overvoltage cannot be avoided even in presence of fast HVDC circuit breakers. Hence, an improved control system together with circuit level modifications are proposed to improve the CFC post-fault operation and to retain its components from possible damages.

Keywords: DC Circuit Breaker, Meshed dc Grid, dc Fault Currents, Current Flow Controller, DC/DC Converter.

1. Introduction

As a consequence of development of large offshore wind farms, there is an increasing demand for realization of multi-terminal HVDC (MT-HVDC) grids [1]. The complex form of MT-HVDC grid is identified as meshed HVDC (M-HVDC) grid, which offers interconnection between different geographical areas to increase renewable energy resources diversity and supply reliability [1].

In addition to protection issues, a meshed dc grid might face power flow control problems [1, 2]. The power flow in M-HVDC grid is controlled by regulating dc voltage of converters considering transmission line impedance. Due to grid topology, multiple paths for current

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flow between two different nodes may exist. Consequently, some of the lines can be overloaded because of their lower impedances. Current flow controllers (CFCs) can be inserted into the M-HVDC grid to solve this issue [2].

Several variants of CFCs, including modular bidirectional PFC with fault blocking capability [3], switched resistors for power flow control of the short transmission lines, DC/DC converters for long transmission lines [4], floating CFC [5] and thyristor based power flow controllers [6, 7] have been proposed in the literature. Furthermore, IGBT based CFCs with the ac grid connection [8], dual H-bridge CFC [9], cascaded and hybrid PFCs [10], double full-bridge DC/DC converters based CFC [11], a multi-port CFC [12] and interline CFC based on coupled inductors [13] have been investigated in recent years.

Among several proposed topologies the interline series connected CFCs without the ac grid connection are more attractive due to their lower voltage rating, power losses and implementation costs [2]. Particularly, the H-bridge based floating CFC topology with reduced number of switches has several technical superiorities [5]. Although the modeling and control principles of the interline CFC has been scrutinized [2], its behavior during a dc fault has not been considered, yet.

The present paper analyzes behavior of the interline dual H-bridge CFC during M-HVDC grid faults. The system and the circuit level analysis confirms the vulnerability of CFC against short circuit faults in M-HVDC grid even in presence of fast dc circuit breakers (DCCBs) and fast protection schemes. To overcome this issue, the CFC control system and its circuit topology are improved. The performance of CFC based on the proposed methods are validated through simulation studies.

2. Interline CFC with Reduced Switch Number

The topology of CFC under study is depicted in Fig. 1(a) [5, 9]. The CFC can be placed between two lines and a dc bus to control the current in one line by charging and discharging its capacitor and exchanging power between two lines.

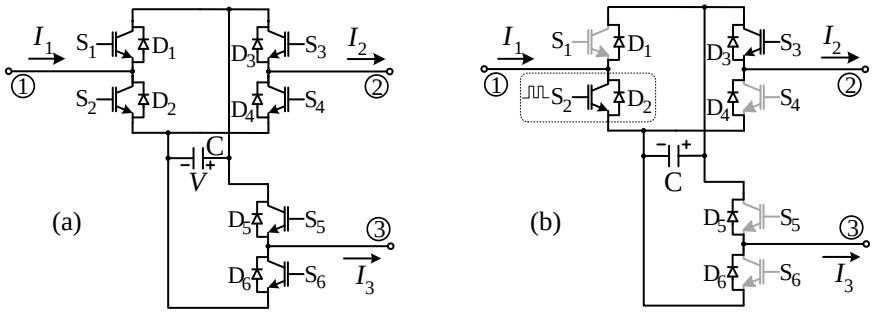

Figure 1: (a) The topology of H-bridge based interline CFC topology with reduced number of switches [5], (b) Switch states to control I_{12}

2.1. Normal Operation

Depending on current direction, the desired voltage can be generated by selecting a suitable set of states of switches. Table 1 shows the switch sates for both negative and positive currents [2]. The capacitor voltage is represented by V in Table I. The current can be controlled using a PI and a second order compensator. The linearized average model of the CFC represented by a couple of voltage sources can be used to design the current control system [2]. As shown in Fig. 1, I_1, I_2 and I_3 are the currents flowing through terminal 1, 2 and 3 of the CFC, respectively. Based on the switching states in [2], I_2 can be controlled by applying PWM signal to S_2 if I_1 is incoming and I_2 and I_3 are outgoing currents. As shown in Fig. 1(b), S_1, S_4, S_5 and S_6 and are opened and S_3 is closed. A generic control system of CFC including a PI controller, a second order compensator and a filter is shown in Fig. 2.

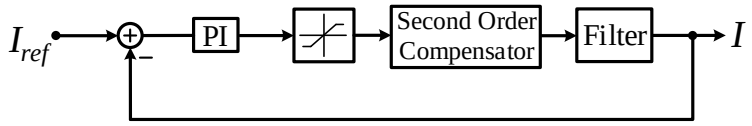

Figure 2: Generic control system of the interline CFC [2]

Table 1: Switching states for positive and negative current scenarios [2]

Positive currents						**Negative currents**					
Set	$\mathbf{sw_1}$	$\mathbf{sw_6}$	$\mathbf{sw_2}$	$\boldsymbol{V_{31}}$	$\boldsymbol{V_{32}}$	**Set**	$\mathbf{sw_3}$	$\mathbf{sw_4}$	$\mathbf{sw_5}$	$\boldsymbol{V_{31}}$	$\boldsymbol{V_{32}}$
1	0	0	0	$-V$	$-V$	**9**	0	0	0	$+V$	$+V$
2	0	0	1	$-V$	0	**10**	0	0	1	$+V$	0
3	0	1	0	0	$-V$	**11**	0	1	0	0	$+V$
4	0	1	1	0	0	**12**	0	1	1	0	0
5	1	0	0	0	0	**13**	1	0	0	0	0
6	1	0	1	0	$+V$	**14**	1	0	1	0	$-V$
7	1	1	0	$+V$	0	**15**	1	1	0	$-V$	0
8	1	1	1	$+V$	$+V$	**16**	1	1	1	$-V$	$-V$

3. CFC Integration into the M-HVDC Grid

3.1. M-HVDC grid

M-HVDC grid can be formed by connecting dc sides of more than two converters through transmission lines. Various VSC technologies can be employed in an M-HVDC grid. Modular multilevel converters (MMCs) demonstrate better performance versus other types of converter for HVDC applications. Among various MMC topologies, the half-bridge MMC has less power losses and lower implementation cost. Nowadays, different variants of half-bridge MMC are widely employed by HVDC project developers. [1]. However, the half-bridge MMC is unable to block dc short circuit fault current [1]. In an M-HVDC grid, due to the contribution of adjacent transmission lines [14] and significant reduction in faulty transmission line frequency dependent inductive characteristics due to the high frequency components of dc fault current

[15], the dc fault current can rise up quickly . Hence, the meshed dc grids need to be effectively protected against the dc side faults [1, 16, 17].
Several protection strategies have been proposed for MT-HVDC and M-HVDC grids [14, 1, 18, 19, 20]. However, fast dc circuit breakers (DCCB) are to be most promising solution for M-HVDC grid. In a system protected by a fully selective protection scheme, every line is equipped with one DCCB at each end. The converter may be protected by either a DCCB at its dc side or an ac circuit breaker at its ac side [18]. A possible arrangement of DCCBs in a fully protected M-HVDC grid is shown in Fig. 3(a). The fast DCCBs such as hybrid (HCB) and solid-state (SSCB) ones employ a current limiting inductor in series with their structure that should be considered in modeling [14, 21].

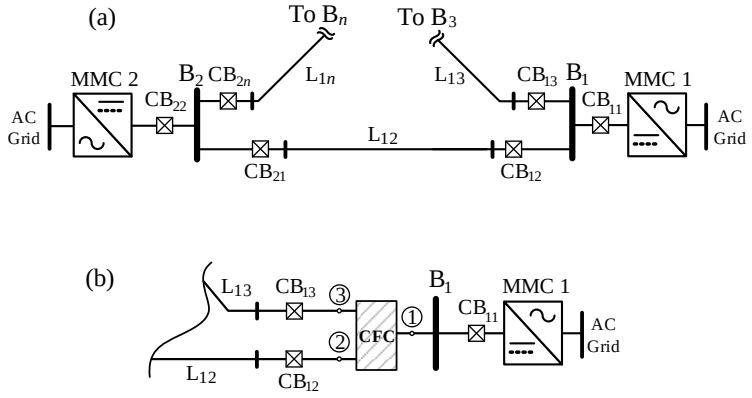

Figure 3: M-HVDC grid (a) DCCB arrangement (b) CFC integration

3.2. CFC integration into M-HVDC grid

Typically, the interline CFC is installed between two transmission lines and a dc bus. A possible integration of interline CFC into a dc bus is depicted in Fig. 3(b). The CFC is installed between L_{12}, L_{13} and B_1. For sake of protection selectivity, the DCCBs should be relocated as seen in Fig. 3(b). No DCCB is required between the CFC and dc bus, but a disconnector might be needed. Therefore, fault on either L_{12} or L_{13} can be cleared by CB_{12} or CB_{13} (and remote DCCBs) and a fault at B_1 can be interrupted by adjacent DCCBs.

4. CFC During dc Fault

DC fault may occur on adjacent lines or at dc bus. The mentioned incoming and outgoing CFC currents scenario in subsection 2.1 is used to analyze the fault behavior of the CFC from system and circuit points of view. However, this study can be extended to other possible scenarios. The CFC behavior is analyzed when it operates in the normal condition and a dc fault occurs.

4.1. System level modeling

The CFC behavior in an HVDC grid during a dc fault is studied considering a three-terminal M-HVDC grid. Fig. 4 shows the three-terminal grid model including the current

limiting inductors of DCCBs. The parameters of three-terminal grid are illustrated in Table .4.

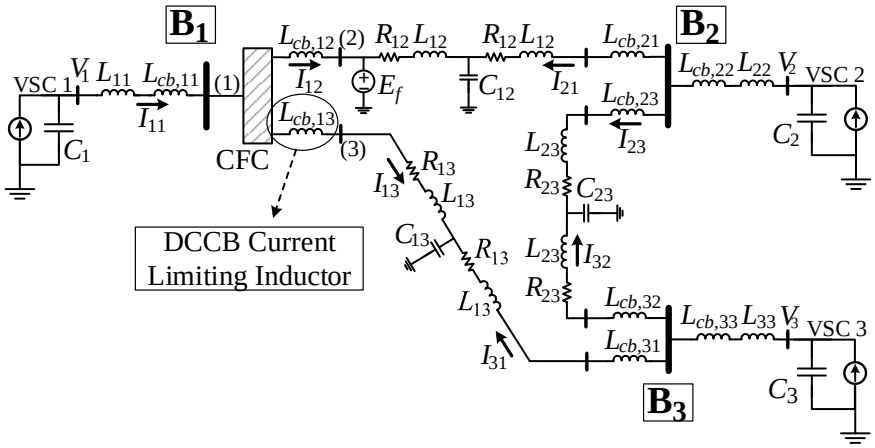

Figure 4: Three-terminal grid including CFC and DCCBs

In this study, the DCCB is modeled as an ideal switch in series with an inductor, which interrupts the current independently of its magnitude after an operation delay defined by T_{cb} upon receiving a trip command [18]. Note that in this study no trip signal is applied to the DCCBs in order to study the fault current behavior. The studied grid has an asymmetric monopole configuration. The simplified average model of VSCs are considered [2] and the cables are modeled as T-equivalent. VSC 1 injects constant power into the grid and VSCs 2 and 3 operate in voltage droop control, whose expressions are described as:

$$I_{ii} = \frac{P_i}{V_i}, \qquad I_i = k_i \left(V_i^* - V_i\right) \tag{1}$$

where, P_i, V_i and I_{ii} are the power, voltage and current of VSC i, respectively. V_i^* and k_i are the voltage reference and droop constant for VSC i, respectively. The fault is modeled as a grounded voltage source with the value of E_f. In normal condition of the grid the value of E_f is equal to the value of line steady-state voltage and it changes to 0 V upon occurrence of a pole-to-ground dc fault.

The linearized model of grid without the CFC and considering a fault on line 12 very close to terminal 2 of the CFC can be derived assuming that the cable capacitance is shared and included in the node capacitances. Thereafter, the system can be linearized and described by following equations, where subscript 0 indicates the linearization point and Δ expresses the increment over linearization point:

$$\frac{\mathrm{d}\Delta V_1}{\mathrm{d}t} = \frac{1}{C_1}\left(\frac{\Delta P_1 V_{10} - \Delta V_1 P_{10}}{V_{10}^2} - \Delta I_{13} - \Delta I_{12}\right) \tag{2}$$

$$\frac{\mathrm{d}\Delta V_2}{\mathrm{d}t} = \frac{1}{C_2}\left(-k_2 \Delta V_2 + \Delta I_{12} - \Delta I_{23}\right) \tag{3}$$

$$\frac{\mathrm{d}\Delta V_3}{\mathrm{d}t} = \frac{1}{C_3}\left(-k_3\Delta V_3 + \Delta I_{13} + \Delta I_{23}\right) \tag{4}$$

$$\frac{\mathrm{d}\Delta I_{21}}{\mathrm{d}t} = \frac{1}{L_{12} + L_{cb,21}}\left(\Delta V_2 - 2R_{12}\Delta I_{21} - \Delta E_f\right) \tag{5}$$

$$\frac{\mathrm{d}\Delta I_{13}}{\mathrm{d}t} = \frac{1}{2L_{13}}\left(\Delta V_1 - \Delta V_3 - 2R_{13}\Delta I_{13}\right) \tag{6}$$

$$\frac{\mathrm{d}\Delta I_{23}}{\mathrm{d}t} = \frac{1}{2L_{23}}\left(\Delta V_2 - \Delta V_3 - 2R_{23}\Delta I_{23}\right) \tag{7}$$

$$\frac{\mathrm{d}\Delta I_{12}}{\mathrm{d}t} = \frac{1}{L_{cb,12}}\left(\Delta V_1 - \Delta E_f\right) \tag{8}$$

where, I_{ij} is the current flowing from bus i to j. R_{ij} and L_{ij} are the T-model resistance and inductance of line ij and C_i is the capacitance of bus B_i. The linearized state-space of dc grid including the CFC can be given by:

$$\frac{\mathrm{d}}{\mathrm{d}x}\Delta\mathrm{x} = \mathbf{A}\Delta\mathrm{x} + \mathbf{B}\Delta\mathrm{u} \tag{9}$$

where, **A** and **B** are 7x7 and 7x2 matrices, respectively. **x** is the linearized state variables vector and **u** is the linearized inputs vector:

$$\Delta\mathrm{x} = (\Delta E_1, \Delta E_2, \Delta E_3, \Delta I_{21}, \Delta I_{13}, \Delta I_{23}, \Delta I_{12}) \tag{10}$$

$$\Delta\mathrm{u} = (\Delta P_1, \Delta E_f) \tag{11}$$

The non-linear (NL) model of system can be simulated using the CFC and T-model of transmission lines. The CFC is modeled based on Fig. 1(a). The lumped parameters of adjacent lines are used to design the preliminary control system. The cable and the CFC parameters are illustrated in Table .4. The developed linearized model can be compared to NL model of dc grid with and without the CFC. In all the models, a dc fault happens on line 12 at time t = 4.5 s. I_{12} for three models including linearized and no-linear models without the CFC and non-linear model with the CFC is depicted in Fig. 5. It can be seen that I_{12} reaches approximately 30 kA in 5 ms in all the models. However, the rate of rise of current is slightly higher in the linearized model as compared to other models.

4.2. Circuit level analysis

The three-terminal grid model is used for circuit-level studies. Fig. 6 shows a part of equivalent circuit of system including the CFC. A dc fault can be activated by closing its corresponding switch (F_1-F_3). The highest rate of rise of the fault current happens when a fault occurs next to the DCCB. In this case, inductance between the CFC and the fault location is equal to the inductance of current limiting inductor of DCCB. Hence, to consider the worst fault scenarios the transmission line faults are placed very close (distance is equal 0 km) to the DCCB. All the fault scenarios are studied through the non-linear model from subsection 4.1.

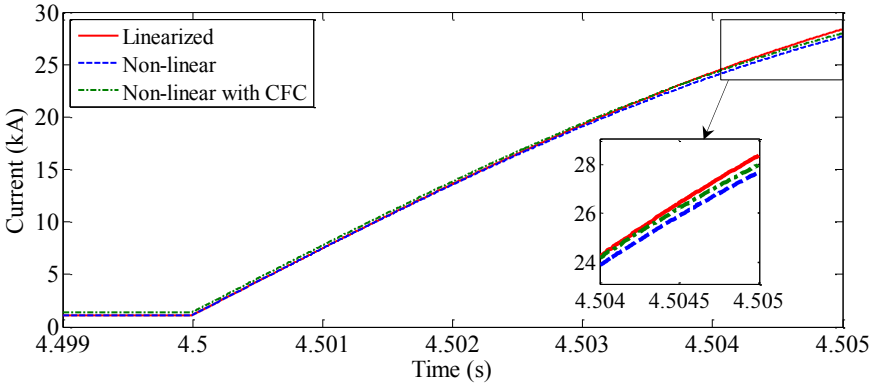

Figure 5: I_{12} in different models with and without the CFC

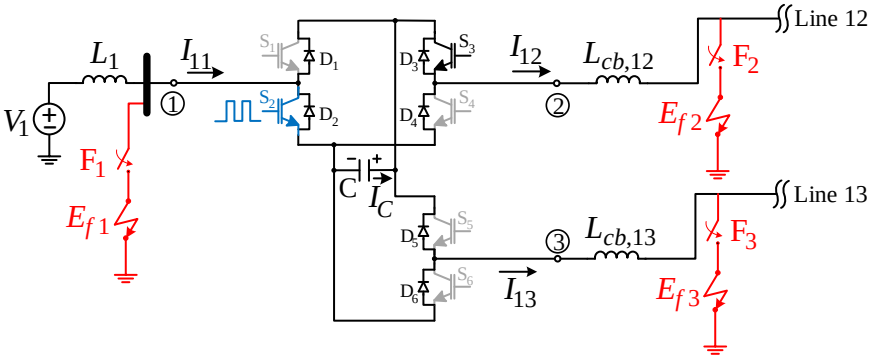

Figure 6: System simplified equivalent circuit during fault

4.2.1. Fault on line connected to terminal 2 (controlled line)

The fault occurs next to CB_{12} and thus very close to terminal 2 of the CFC on line L_{12}. This fault can be activated by closing switch F_2 in Fig. 6. In Fig. 6 L_1 represents the sum of inductances between the CFC and B_1. Initially, I_{13} is positive but its direction is to be reversed due to the fault occurrence on on line L_{12}. Fig. 7 shows various currents and voltages of the CFC and the system.

$V_C > 0$. In the initial stage of fault and after the direction of I_{13} is reversed, $V_C > 0$. Therefore, when S_2 is closed I_1 flows through S_2 into the CFC capacitor and then via S_3 into the fault point. Also, I_{13} flows through D_5 and S_3 into the fault location. In this stage the capacitor discharges when S_2 is closed. When S_2 is opened I_1 flows through D_1 and S_3 into the fault location whereas I_{13} maintains its path. As it is shown in Fig. 7, when S_2 is turned off the flowing current into capacitor falls to zero and capacitor voltage remains constant. However, the capacitor voltage reduces when S_2 is closed.

$V_C = 0$. Previous stage continues until the capacitor voltage falls to zero. Due to antiparallel diodes of S_1-S_6 the capacitor cannot be negative and thus its voltage remain approximately zero. In this stage, when S_2 is closed I_1 has two parallel paths to flow: i) through D_1 and S_3,

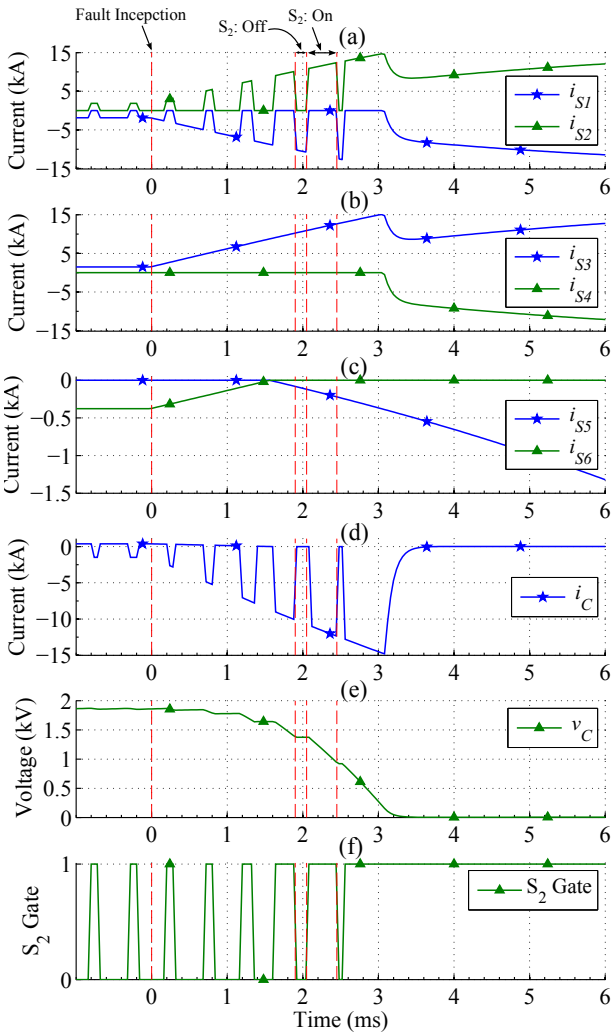

Figure 7: CFC and system waveforms during fault on line 12

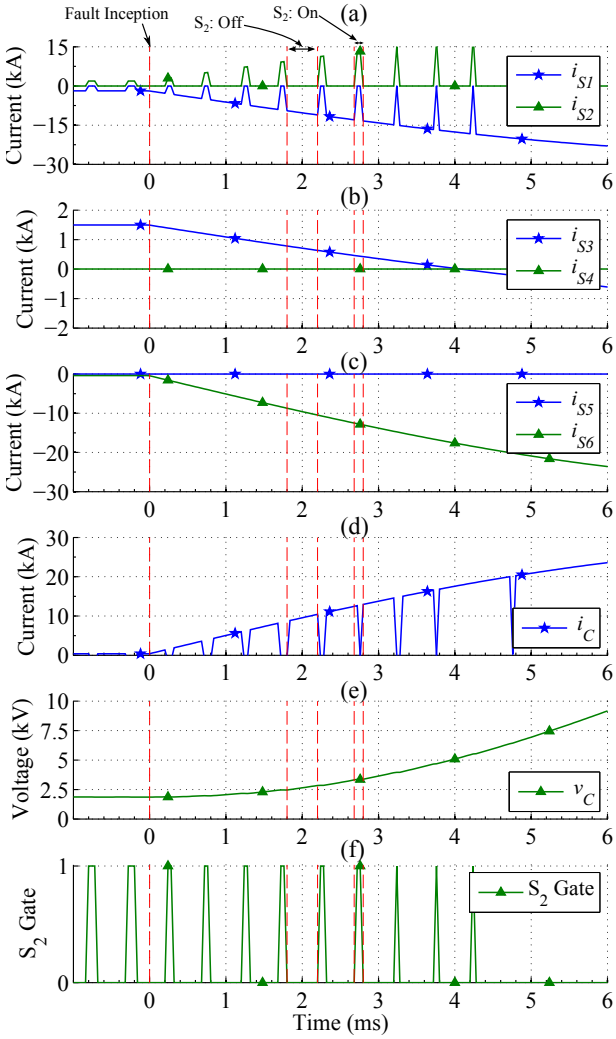

Figure 8: CFC and system waveforms during fault on line 13

ii) through S_2 and D_4. When S_2 is opened the CFC behavior is similar to the previous stage. As can be seen in Fig. 7, the CFC control system keeps S_2 in on-state after the capacitor voltage falls to zero. Although the capacitor voltage does not increase in this fault scenario, its discharge current may reach undesirable levels (here it reaches 15 kA). S_1-S_4 conduct high fault current, which is out of safe operation area of single commercial switches (here it reaches 12 kA.). The most severe case happens when S_2 is kept open in this stage, which prevents the fault current from being shared between S_1 and S_2 and hence D_1 must carry whole the current.

4.2.2. Fault on line connected to terminal 3

In this case direction of I_{12} is to be reversed. When S_2 is closed I_1 flows through S_2 and D_6 into the fault point on L_{13}. At the same time, I_{12} flows through D_3, capacitor and D_6 into

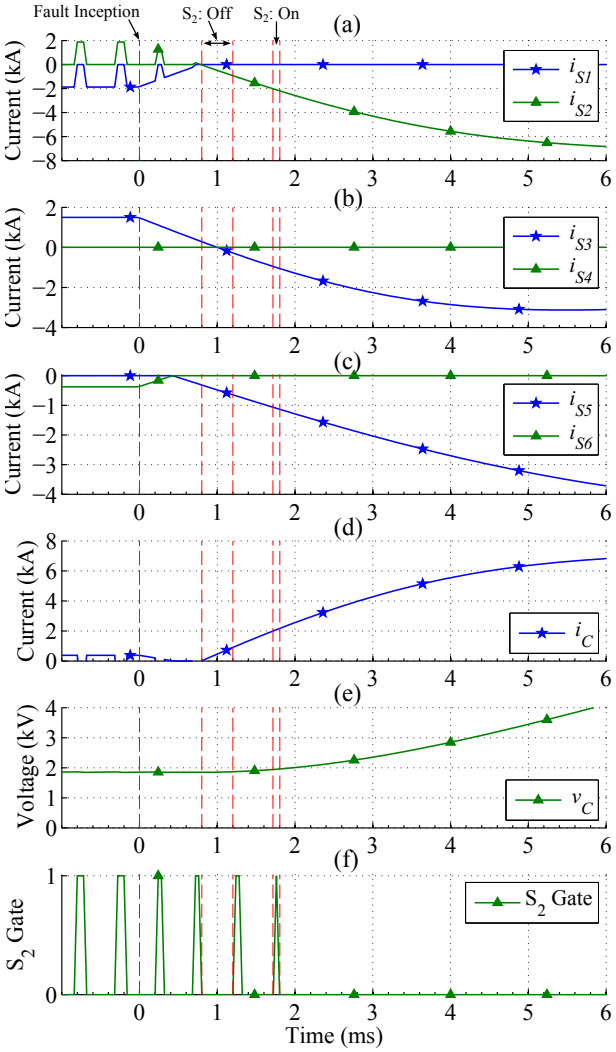

Figure 9: CFC and system waveforms during fault at bus 1

the fault location. When S_2 is opened I_1 flows through D_1 into the capacitor and then via D_6 into the fault point. The state of S_2 does not affect the I_{12} flow path. Hence, the capacitor is continuously charged by the fault current. Therefore, the capacitor voltage increases and can exceed its rated voltage. Fig. 8 shows various currents and voltages of the CFC and system when a fault occurs on L_{13}. As can be seen in the figure, prior to direction reversal of I_{12} the capacitor does not charge continuously. However, after current reversal it is charged up continuously and the rate of rise of capacitor voltage increases. Note that when S_2 is closed the flowing current into the capacitor decreases but does not fall to zero. This is due to higher inductance between the CFC and system at its terminal 2. In this scenario D_1, S_2 and D_6 are required to carry high current. For instance, the current in D_1 and D_6 reaches 25 kA. Also, Fig. 8(e) shows that V_C reaches 9 kV in 6 ms.

4.2.3. Fault at terminal 1 (dc bus)

When a fault happens at B_1, directions of all incoming and outgoing currents are to be reversed. I_{12} flows through D_3 and I_{13} flows via D_5 and both charge the capacitor and flow to the fault location. Therefore, the capacitor voltage increases. Fig. 9 shows the CFC and line currents and the capacitor voltage during a bus fault. As can be seen in the figure, state of S_2 does not have any impact on the fault current after the direction of I_{12} is reversed. In this scenario, D_2, D_3 and D_5 are stressed. Fig. 9(e) shows that the capacitor voltage reaches more than 4 kV in 6 ms.

4.2.4. Remarks

The fast protection schemes in M-HVDC grids are expected to detect and clear the DC transmission line and DC bus faults in less than 5 ms [14, 17, 19]. Hence, the switches and the capacitor can be stressed during this time period. Table 2 illustrates the absolute values of current in different switches and also the value of capacitor voltage at $t = 5$ ms.

Table 2: Absolute values of different currents and voltages at $t = 5$ ms

	Fault on L_{12}	Fault on L_{13}	Fault at B_1
$\lvert i_{s1}(t)\rvert$	11 kA	0 kA	0 kA
$\lvert i_{s2}(t)\rvert$	11 kA	22 kA	6.4 kA
$\lvert i_{s3}(t)\rvert$	11 kA	0.3 kA	3.1 kA
$\lvert i_{s4}(t)\rvert$	11 kA	0 kA	0 kA
$\lvert i_{s5}(t)\rvert$	0.95 kA	0 kA	3.3 kA
$\lvert i_{s6}(t)\rvert$	0 kA	22 kA	0 kA
$\lvert i_C(t)\rvert$	0 kA	22 kA	6.4 kA
$v_C(t)$	0 kV	7 kV	3.5 kV

As can be seen in Table 2, during the short circuit fault on the controlled transmission line (Line 12) the current in S_1, S_2, S_3 and S_4 reaches almost 11 kA, which is definitely out of safe operation area of a single semiconductor switch. On the other hand, the short circuit fault on the uncontrolled line (Line 13) causes very large current (almost equal to 22 kA) in the S_2 and S_6. In addition, during this type of fault large current (almost equal to 22 kA) flows though the capacitor. Moreover, the voltage of capacitor increases up to 7 kV when the fault occurs on the uncontrolled transmission line. During the fault at DC bus 1, S_2 is more stressed as compared to the other semiconductor switches.

4.3. Maximum fault current approximation

As shown in Fig. 7(f), 7(g), 8(f), 8(g), 9(f) and 9(g), the current derivative in the CFC terminals is equal to that of transmission lines in grid without the CFC for similar faults. However, the initial current is not identical for the mentioned cases. Considering the results from subsection 4.1 it can be confirmed that the linearized model considering the high frequency inductances of transmission lines [15] can be used for approximating the maximum fault current at the CFC terminals and consequently in switches and diodes at interruption instant.

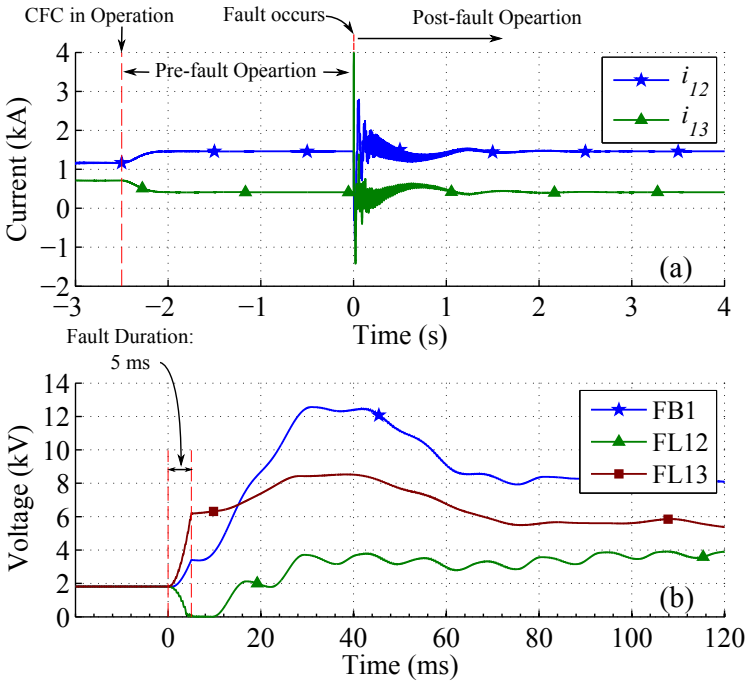

Figure 10: CFC post-fault (a) lines current, (b) capacitor voltage

4.4. CFC post-fault behavior

CFC post-fault behavior can be affected due to the controller saturation during the fault condition. Fig. 10(a) shows the CFC currents when a non-permanent short circuit fault happens on line 13 for duration of 5 ms. The CFC regulates I_{12} after the fault is removed. Fig. 10(b) depicts the capacitor voltage for faults on lines 13 (FL13), 12 (FL12) and at bus 1 (FB1). After FLB1 removal the capacitor voltage rises up to 12.5 kV, which is several times more than its rated value. Also, the capacitor voltage reaches almost 8 kV after removal of FLB13.

5. CFC Fault Mode Operation Strategies

The fault clearing time for fast protection schemes in M-HVDC grid equipped by HCBs considering the fault identification time and peripheral circuits delays lies in range of 3.5-5 ms [18, 22]. Therefore, the capacitor voltage may exceed its rated value and the semiconductor switches can be damaged by high current even within the short fault clearing time. In this section, an enhanced control system and two fault operation methods are suggested and compared for possible fault scenarios.

5.1. Enhanced control system

As shown in Fig. 11 an anti-windup scheme is included the control system. In addition, an internal fault mode activator (FMA) is considered. The FMA activates the fault mode when any switch current exceeds I_{max}. The fault mode stays active for the period of t_{FMA}

after the current falls below I_{max}. I_{max} can be determined according to the components characteristics. During system disturbances that may not be detected by protection system, the fault mode may be activated. In other words, the possible destructive impacts of system transients, which are not detected by the system protection scheme as dc faults can be negated by the application of FMA. In order to tune the controller parameters of the CFC, the system under study including the meshed HVDC grid and the CFC is linearized following the same procedure as in [2]. Then, using the linearized model, the controller (including the PI, the second order compensator and the low pass filter) is tuned using modeling software namely MATLAB Simulink to achieve a first order system response. The time constant of the closed loop system response is set to 150 ms, which can be seen in Fig. 10(a). The parameters of control system are illustrated in Table .8.

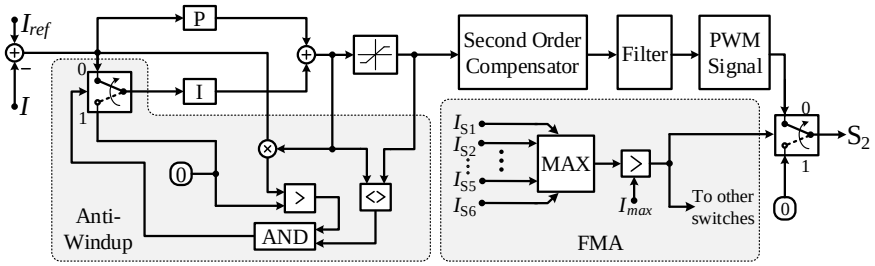

Figure 11: CFC enhanced control system

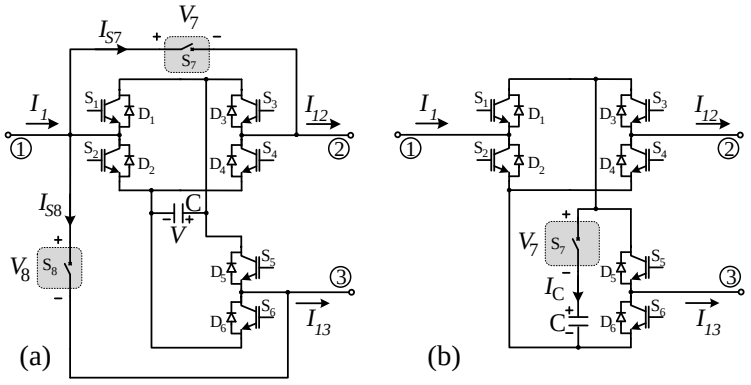

Figure 12: Modified CFC based on: (a) Method 1, (b) Method 2

5.2. Method 1

Fig. 12(a) depicts a CFC with parallel bypass branches. The bypass valves (S_7 and S_8) are bidirectional switches. After the fault mode is activated S_2, S_4 and S_6 should be opened and then S_1, S_3 and S_5 have to be closed (Stage B) to the capacitor current. The next step is closing S_7 and S_8 (stage C). Finally, S_1, S_3 and S_5 are opened (Stage D) and the current is commutated into the parallel branches. Time $t_C - t_B$ sets the current requirements of S_1, S_3 and S_5. Therefore, it can be minimized to reduce the current capacity of the mentioned

switches. In addition, $t_D - t_C$ has to be short enough to prevent the current in the mentioned switches from exceeding its value at t_C. The current requirement of S_7 and S_8 is set by the maximum fault current and the current requirement of S_2, S_4 and S_6 depends on I_{max} in the FMA.

5.3. Method 2

As shown in Fig. 12(b) a bidirectional semiconductor switch (S_7) is placed in series with the capacitor. Voltage rating of S_7 is equal to that of capacitor. In normal operation, S7 is closed. Upon fault mode activation, S_2, S_4 and S_6 should be turned off and then S_1, S_3 and S_5 have to be turned on (Stage B). Consequently, the capacitor current falls to zero and S_7 can be turned off in zero current (Stage C). After S_7 is opened S_2, S_4 and S_6 can be closed (Stage D). Thereafter, the fault current is shared between all the switches. The current capability for S_1 to S_6 is equal to half of maximum fault current.

5.4. Comparison

In addition to the proposed methods, the standard CFC can survive during the fault if it is designed according to maximum fault current of system. Table 3 illustrates the number of required switches for different methods. In Table 3, k_p and k_s represent the number of parallel branches and switches in series connection, respectively. Method 2 requires less number of switches as compared to the other methods.

Table 3: Number of switches in various methods

	Standard	**Method 1**	**Method 2**
CFC's switches	$3k_s(k_p+1)$	$6k_s$	$3k_sk_p$
Additional switches	0	$4k_sk_p$	$2k_s$
Total No. of switches	$3k_s(k_p+1)$	$2k_s(2k_p+3)$	$k_s(3k_p+2)$

6. Simulations

Two simulation sets are carried out to validate the functionality of the proposed methods. The three-terminal grid model from section 4.1 and a four-terminal M-HVDC detailed model from [23] are implemented in PSCAD/EMTDC software. To consider the most severe fault situation from the CFC point of view, non-permanent dc fault with duration of 5 ms is considered and the fault is removed before DCCBs act.

6.1. Three-terminal M-HVDC model

Three-terminal M-HVDC model under study is depicted in Fig. 4 and the model parameters are illustrated in Table .4. The CFC starts regulating current in line 12 based on its reference value ($I_{12ref} = 1.45$ kA). A pole-to-ground fault occurs at time 4.5 s. I_{max} and t_{FMA} are set to 2.8 kA and 2.5 s in the FMA, respectively. Note that time $t = 4.5$ s is shifted to $t^{'} = 0$ s in the plotted figures. Therefore, the negative times show the pre-fault operation of the system.

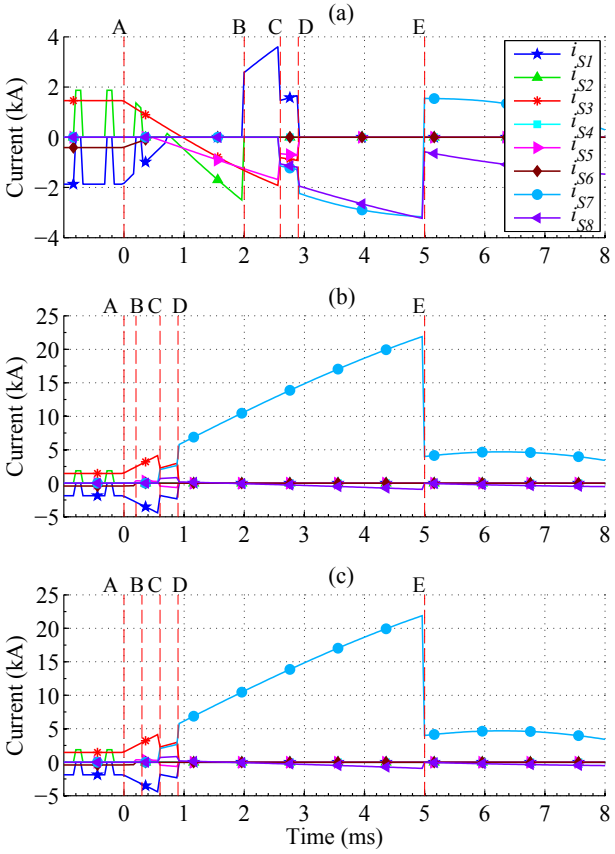

Figure 13: Current in switches of the CFC based on method 2 in three-terminal grid for fault on: (a) bus 1, (b) line 12, (c) line 13

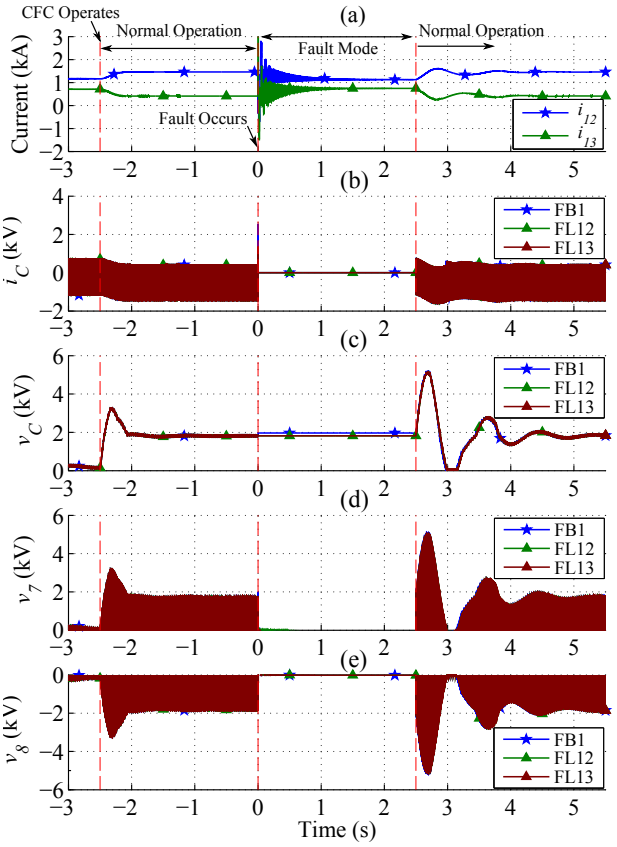

Figure 14: Method 1: (a) line currents, (b) capacitor current, (c) capacitor voltage, (d) S_7 and (e) S_8 voltage

6.1.1. Method 1

Fig. 15 shows the current in semiconductor switches for three fault scenarios. In this figure, A, and E represent fault occurrence and removal instances, respectively. Stages B, C and D are explained in subsection 5.2. The current in switches during a fault at bus B_1 are depicted in Fig. 15(a). The results for faults on lines 12 and 13 are shown in Fig. 15(b) and (c), respectively.

Fig. 14(a) shows the current in lines 12 and 13 in presence of the CFC. Fault occurs at time 0 s and consequently the CFC enters into the fault mode for 2.5 s after fault removal. At time 2.505 s, the CFC returns to normal operation mode and regulates the current in line 12. It can be seen in Fig. 14(b) by employing method 1 the capacitor current during fault is limited below 3 kA for all scenarios. Also, Fig. 14(c) shows that the capacitor voltage remains constant during the fault mode and is also limited below 5.5 kV during the transients when the CFC returns to normal operation. Fig. 14(c) can be compared to Fig. 10(b) where the capacitor voltage reaches higher values at and after the fault removal. Note that the capacitor voltage rises slightly before fault mode activation in bus fault scenario. This voltage increase is expected based on analysis from subsection 4.2.3. Fig. 14(d) and (e)

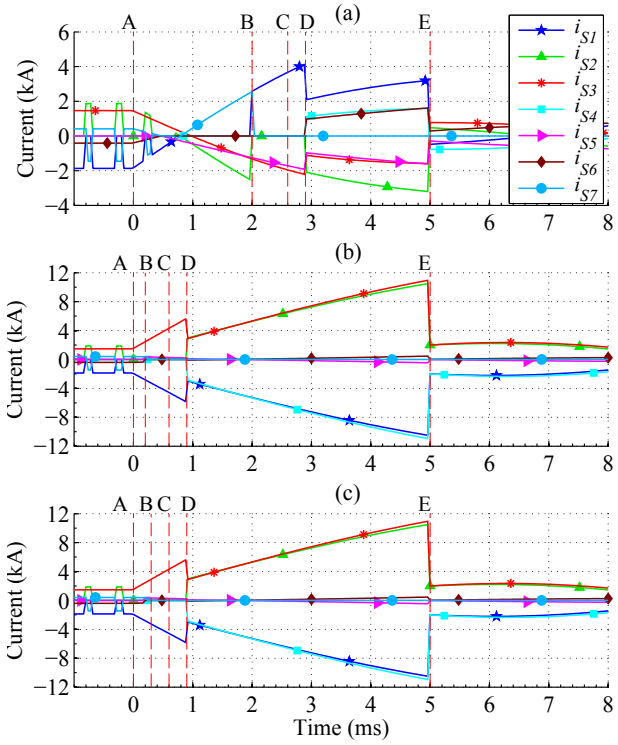

Figure 15: Current in switches of the CFC based on method 2 in three-terminal grid for fault on: (a) bus 1, (b) line 12, (c) line 13

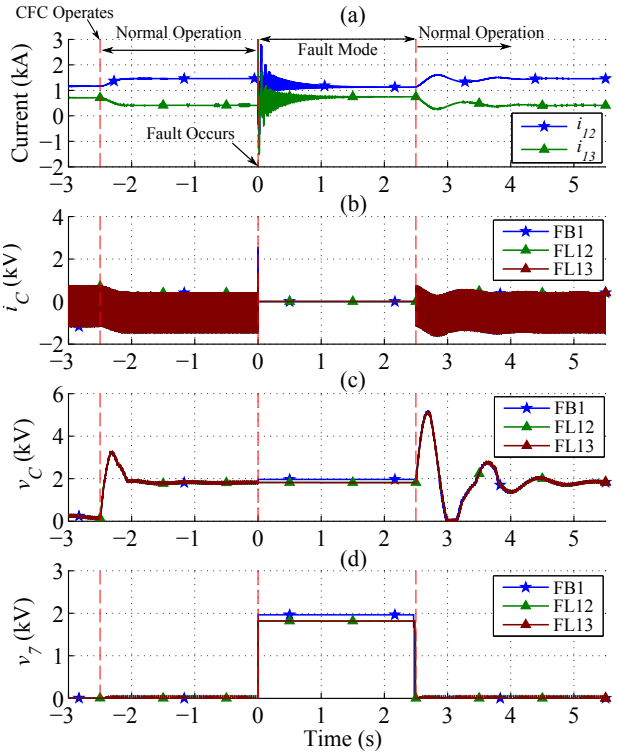

Figure 16: Method 2: (a) line currents, (b) capacitor current, (c) capacitor voltage, (d) S_7 voltage

depict the voltage across S_7 and S_8, respectively. As it is expected the voltage rating of the mentioned switches is equal to the CFC's other switches. Also, S_7 and S_8 are opened at time 2.505 s without any surge voltage since the S_1, S_3 and S_5 have been closed.

6.1.2. Method 2

The current in switches during a fault at bus B_1 are depicted in Fig. 13(a). Fig. 13(b) and (c) depicts the results for fault on lines 12 and 13 , respectively. Fig. 16(a) depicts the currents in lines 12 and 13 in presence of the CFC. The CFC currents for method 1 and 2 are identical from system point of view. It can be seen in Fig. 16(b) method 2 limits the capacitor current below 3 kA during the fault for all scenarios. Also, Fig. 16(c) shows that the capacitor voltage remains constant during the fault mode and is limited below 5.5 kV when the CFC returns to normal operation. Comparing Fig. 16(c) to Fig. 10(b) shows significant improvement in the capacitor voltage behavior. Fig. 16(d) depicts the voltage across S_7. It can be confirmed that the voltage rating of S_7 is equal to that of the capacitor. Moreover, due to zero current switching of S_7 no voltage surge is observed.

6.2. Four-terminal M-HVDC grid model

Fig. 17 shows a symmetric monopole four-terminal M-HVDC grid model. One half-bridge MMC is connected to each terminal of the grid. The grid parameters are illustrated in Table

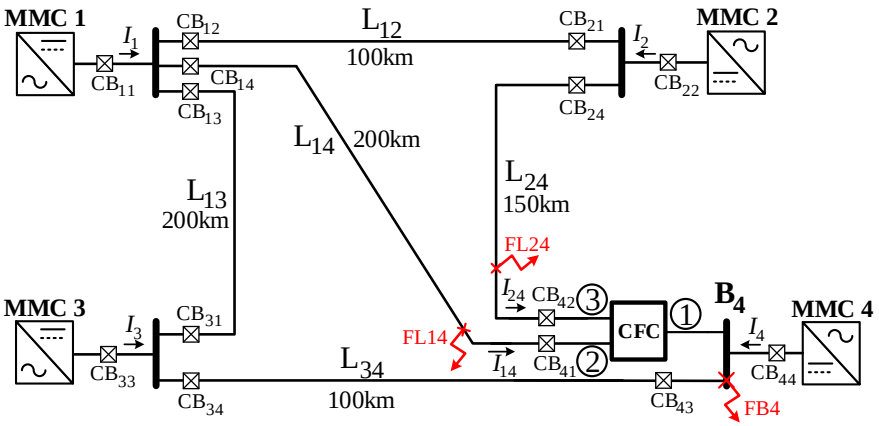

Figure 17: Four-terminal M-HVDC grid equipped with the CFC

.5. Distributed frequency dependent model of XLPE insulated HVDC cable is employed based on physical characteristics, which are illustrated in Table .6 [24]. Due to the system configuration, two CFCs (one for each positive and negative poles) are required. The control system is designed based on lumped parameters of adjacent lines. The lumped cable and the CFC parameters are illustrated in Tables .7 and .8, respectively. The current limiting inductor value for line and converter station DCCBs is set to 50 and 10 mH respectively. The CFC starts its operation at time $t = 4.5$ s and increases I_{14} from 451 A to 745 A. Thereafter, a pole-to-pole fault occurs at time 8 s (Stage A). I_{max} and t_{FMA} are set to 2.8 kA and 2.5 s, respectively. Note that time $t = 8$ s is shifted to $t^{'} = 0$ s in the plotted figures.

Due to the better performance of method 2, the results of three fault scenarios including faults at bus 4 (FB4), line 14 (FL14) and line 24 (FL24) for the CFC based on the mentioned method are presented. The current in switches during a fault at bus B_4 is depicted in Fig. 18(a). Before fault mode activation I_{S1} increases rapidly. Upon fault mode activation the stress on switches is reduced by sharing the fault current between S_1 to S_6. Fig. 18(a) and (b) depict the results for faults on lines 14 and 24 , respectively. At the FL24 removal instance (Stage E in Fig. 18(c)) current in D_6 and S_5 reaches almost 8 kA. Also, current in D_4 and S_3 reaches almost 7.5 kA at the FL14 removal instance (Stage E in Fig. 18(b)).

The current in lines 14 and 24 in presence of the CFC is depicted in Fig. 19(a). As can be seen in Fig. 19(b) the maximum capacitor current is almost 3 kA in all fault scenarios. Fig. 19(c) shows that the capacitor voltage remains constant during the fault mode and its post-fault voltage is limited below 2.2 kV. As it can be seen in Fig. 19(d) the voltage rating of S_7 is equal to that of capacitor and it is turned off without generating surge voltage.

7. Conclusion

In this work, the behavior of H-bridge CFC during dc line and bus short circuit faults is investigated. The system level analysis are carried out based on the system linearized and non-linear models. It is identified that the semiconductor switches of the CFC and its capacitor can be damaged due to the high current and voltage caused by the fault and the

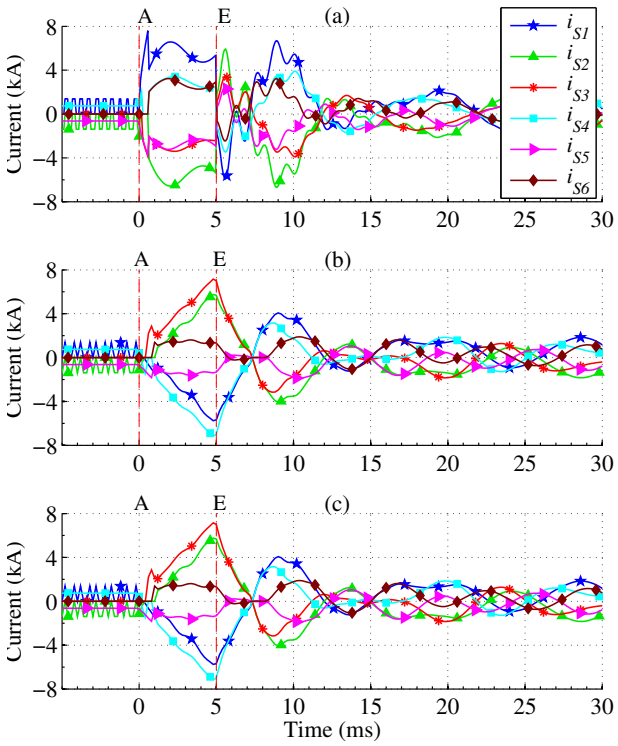

Figure 18: Current in switches of the CFC based on method 2 in four-terminal grid for fault on: (a) bus 4, (b) line 14, (c) line 24

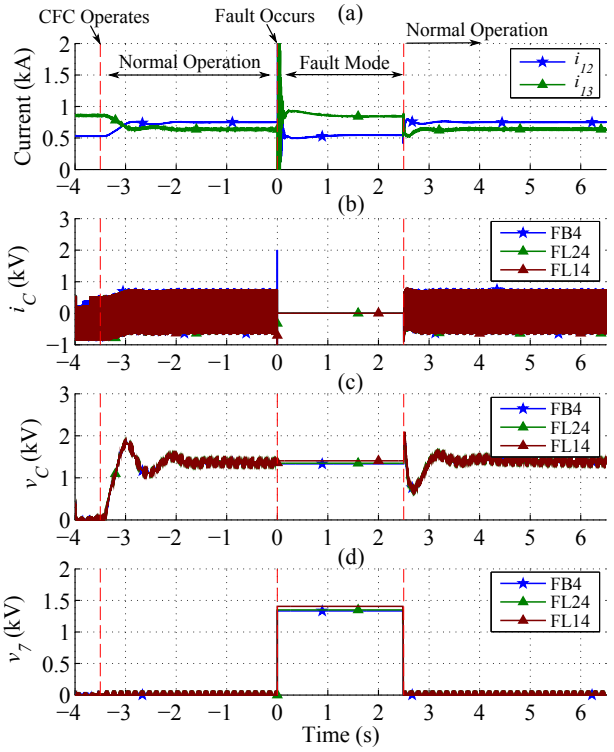

Figure 19: Method 2 (in four-terminal grid): (a) line currents, (b) capacitor current, (c) capacitor voltage, (d) S_7 voltage

CFC control system behavior, even during short action time of fast protection systems (5 ms). It is also found out that the capacitor voltage increases after fault removal when the CFC starts regulating the current due to the controller action. An improved control system, including a fault mode activator is suggested and employed in this paper. Moreover, two circuit level modifications are proposed and compared. Method 1 employs two parallel bypass branches, which are required to be rated for the maximum fault current at CFC terminals. In method 2 the CFC switches are designed for higher current (equal to half of the maximum fault current at CFC terminals) and a low voltage switch is added in series with the capacitor. A comparison between standard and proposed methods shows that method 2 requires less number of switches. The performance of both proposed methods are validated through two sets of simulations based on three-terminal average and four-terminal detailed M-HVDC grid models. The results are in agreement with the analysis and confirm the functionality of proposed methods.

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Appendix

Table .4: Three-terminal test grid parameters

Transmission Lines Parameters			
Lumped T-model Parameters	R [Ω/km]	L [mH/km]	C [μF/km]
	0.01105	3.245	0.382
Length [km]	Line 12	Line 13	Line 23
	100	200	200
VSC Parameters			
Bus	**1**	**2**	**3**
Capacitance [μF]	450	450	450
Power [MW]	1200	-	-
V_i^* [kV]	-	300	300
Droop Constant k_i [A/V]	-	0.05	0.5
CFC Parameters			
Nominal Voltage [kV]	4		
Capacitor [mF]	2		
Switching Frequency [kHz]	2		

Table .5: Four-terminal HVDC system parameters [23]

Parameter	**Converter 1, 2, 3**	**Converter 4**
Rated power	900 MVA	1200 MVA
ac grid voltage	400 kV	400 kV
Converter ac voltage	380 kV	380 kV
Transformer, u_k	0.15 pu	0.15 pu
Arm capacitance C_{arm}	29.3 μF	39 μF
Arm reactor L_{arm}	84.8 mH	63.6 mH
Arm,resistance R_{arm}	0.885 Ω	0.67 Ω
Bus filter reactor L_s	10 mH	10 mH

Table .6: DC cable data [24]

Layer	**Radius (mm)**	**Resistivity (m)**	**Rel. permeability**	**Rel. permittivity**
(1) Core	25.2	1.72×10^{-8}	1	1
(2) Insulator	40.2	-	1	2.3
(3) Sheath	43.0	2.20×10^{-7}	1	1
(4) Insulator	48.0	-	1	2.3
(5) Armor	53.0	1.80×10^{-7}	10	1
(6) Insulator	57.0	-	1	2.1

Table .7: Cable lumped PI-model parameters

	Resistance (Ω/km)	**Inductance (mH/km)**	**Capacitance (μF/km)**
±320 kV XLPE Cable	0.01105	2.945	32.2

Table .8: CFC parameters

	Transfer Function	**Value**
PI	$0.012 + \frac{0.398}{s}$	-
Compensator	$\frac{0.3421s^2+1.2978s+21.5213}{s^2+120.5323s+3207.9071}$	-
Filter	$\frac{1}{0.08s+1}$	-
Capacitor	-	10 mF
Switching frequency	-	2 kHz

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