Design of broadband inductor-less RF front-ends with high dynamic range for G.hn

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A thesis submitted for the degree of

PhilosophiæDoctor (PhD)

year month

Act of qualification of the Doctoral Thesis

Gathered the tribunal consisting of the undersigned to mark the doctoral thesis:

Thesis' title:	Design of broadband inductor-less RF front-ends with high dynamic range for G.hn
Thesis' author:	Xavier Trulls Fortuny

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- ☐ Unacceptable
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Full report of Xavier Trulls Fortuny's PhD thesis
to apply for the title of PhilosophiæDoctor (PhD)

2008-2012
PhD programme "Electronic Engineering"
Electronic Engineering Department
Technical University of Catalonia (UPC)

Abstract

System-on-Chip (SoC) was adopted in recent years as one of the solutions to reduce the cost of integrated systems. When the SoC solution started to be used, the final product was actually more expensive due to lower yield. The developments in integrated technology through the years allowed the integration of more components in lesser area with a better yield. Thus, SoCs became a widely used solution to reduced the cost of the final product, integrating into a single-chip the main parts of a system: analog, digital and memory.

As integrated technology kept scaling down to allow a higher density of transistors and thus providing more functionality with the same die area, the analog RF parts of the SoC became a bottleneck to cost reduction as inductors occupy a large die area and do not scale down with technology. Hence, the trend moves toward the research and design of inductor-less SoCs that further reduce the cost of the final solution.

At the same time, as the demand for home networking high-data-rates communication systems has increased over the last decade, several standards have been developed to satisfy the requirements of each application, the most popular being wireless local area networks (WLANs) based on the IEEE 802.11 standard. However, poor signal propagation across walls make WLANs unsuitable for high-speed applications such as high-definition in-home video streaming, leading to the development of wired technologies using the existing in-home infrastructure. The ITU-T G.hn recommendation (G.9960 and G.9961) unifies the most widely used wired infrastructures at home (coaxial cables, phone lines and power lines) into a single standard for high-speed data transmission of up to 1 Gb/s.

The G.hn recommendation defines a unified networking over power lines, phone lines and coaxial cables with different plans for baseband and RF. The RF-coax bandplan, where this thesis is focused, uses 50 MHz and 100 MHz bandwidth channels with 256 and 512 carriers respectively. The center frequency can range from 350 MHz to 2450 MHz. The recommendation specifies a transmission power limit of 5 dBm for the 50 MHz bandplan and 8 dBm for the 100 MHz bandplan, therefore the maximum transmitted power in each carrier is the same for both bandplans.

Due to the nature of an in-home wired environment, receivers that can handle both very large and very small amplitude signals are required: when transmitter and receiver are connected on the same electric outlet there is no channel attenuation and the signal-to-noise-plus-distortion ratio (SNDR) is dominated by the receiver linearity, whereas when transmitter and receiver are several rooms apart channel attenuation is high and the SNDR is dominated by the receiver noise figure. The high-dynamic-range specifications for these receivers require the use of configurable-gain topologies that can provide both high-linearity and low-noise for different configurations. Thus, this thesis has been aimed at researching high dynamic range broadband inductor-less topologies to be used as the RF front-end for a G.hn receiver complying with the provided specifications.

A large part of the thesis has been focused on the design of the input amplifier of the front-end, which is the most critical stage as the noise figure and linearity of the input amplifier define the achievable overall specifications of the whole front-end. Three prototypes has been manufactured and measured using a 65 nm CMOS process: two input RFPGAs and one front-end using the second RFPGA prototype.

Keywords: *broadband*, *inductor-less*, *RF*, *front-end*, *high dynamic range*, *wired communications*

To my family,

for the continuous support over the years.

Acknowledgements

I would like to thank *Broadcom Corporation* and *Gigle Networks* (prior to acquisition by the former) for the project offer, especially former *Gigle Networks* CTO Jed Hurwitz and Group Manager Keith Findlater for supporting my involvement in this project. I also want to thank the company staff that provided continuous support and valuable insight on how to improve the content, especially my thesis co-advisor Adrià Bofill and fellow co-workers Xavier Redondo and Tomeu Servera.

I thank the Technical University of Catalonia (UPC), the Electronic Engineering Department and especially my university co-advisor Diego Mateo for all the support over the duration of this thesis, as well as fellow university research comrades (in no particular order, Dídac Gómez, Marc Molina, Marc Pons and Enrique Barajas).

I acknowledge that the work presented in this thesis has been partly subsidized by the Spanish Ministry of Industry under the Avanza R&D plan with project number TSI-020100-2009-597.

I also thank *Agilent Technologies* and Lluis Pradell from the RF&MW research group at the Technical University of Catalonia for providing measuring equipment.

Finally, I would like to thank a plethora of friends, close friends and even closer friends who have walked beside me and helped me on this long journey, sharing a lot of unforgettable moments. Thanks to all the people who have shared those moments with me, because as one great literary mind once said, *"[...] ist eine Reise unschtzbar; sie belebt, berichtigt, belehrt und bildet"*.

And, most importantly, to my family, who has always been there for me and deserve much more than a simple acknowledgement.

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Glossary

ACPR Adjacent Channel Power Ratio

ADC Analog-to-Digital Converter

AGC Automatic Gain Control

BER Bit-Error Rate

CTB Composite Triple Beat

DI Double-Input

DSB Double-sideband

F Noise Factor

IF Intermediate Frequency

IIP3 Third-Order Input Intercept Point

IMD Intermodulation Distortion

ITU International Telecommunications Union

LNA Low Noise Amplifier

LO Local Oscillator

MS Multiple-Stage

NF Noise Figure

NPR Noise Power Ratio

OIP3 Third-Order Output Intercept Point

OTA Operational Transconductance Amplifier

PCB Printed Circuit Board

PGA Programmable Gain Amplifier

RF Radio-Frequency

SFDR Spurious Free Dynamic Range

SNDR Signal to Noise plus Distortion Ratio

SNR Signal to Noise Ratio

SoC System-on-a-Chip

SSB Single-Sideband

VCO Voltage Controlled Oscillator

VGA Variable Gain Amplifier

1

Introduction

1.1 Thesis Framework

This thesis has been developed in the framework of industry through a joint fellowship provided by *Broadcom Corporation* (initially *Gigle Networks*, prior to its acquisition) and the *Technical University of Catalonia* (UPC). The research presented in this thesis has been developed based upon the requirements provided by the company and it is focused on the RF front-end part of a receiver for the ITU-T G.hn recommendation (G.9960 [1] and G.9961 [2]) which received final approval in 2010. The recommendation (the ITU's term for standard) defines networking over power lines, phone lines and coaxial cables with data rates up to 1 Gbit/s and contains a bandplan for RF over coaxial cable (RF-coax), where this thesis is focused.

The work presented in this thesis was partly subsidized by the *Spanish Ministry of Industry* under the *Avanza R&D* plan with project number TSI-020100-2009-597.

1.2 G.hn recommendation

As the demand for home networking high-data-rates communication systems has increased over the last decade, several standards have been developed to satisfy the requirements of each application, the most popular being wireless local area networks

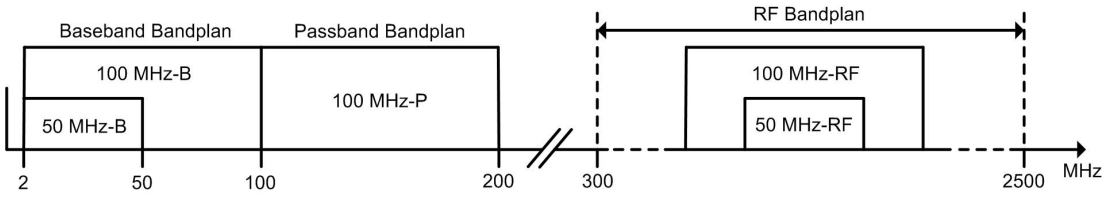

Figure 1.1: G.hn bandplans.

Bandplan	Medium	Number of carriers
50 MHz-B	Powerline	2048
	Phoneline	1024
	Coax	256
100 MHz-B	Powerline	4096
	Phoneline	2048
	Coax	512
100 MHz-P	Powerline	1024
50 MHz-RF	Coax	256
100 MHz-RF	Coax	512

Table 1.1: Physical medium and number of carriers used in each G.hn bandplan.

(WLANs) based on the IEEE 802.11 standard. However, poor signal propagation across walls make WLANs unsuitable for high-speed applications such as high-definition in-home video streaming, leading to the development of wired technologies using the existing in-home infrastructure. The ITU-T G.hn recommendation (G.9960 and G.9961) unifies the most widely used wired infrastructures at home (coaxial cables, phone lines and power lines) into a single standard for high-speed data transmission of up to 1 Gb/s.

The G.hn recommendation defines a unified networking over power lines, phone lines and coaxial cables. The physical medium available and number of carriers used in each bandplan are listed in Table 1.1 and its distribution shown in Fig. 1.1. The RF-coax bandplan, where this thesis is focused, uses 50 MHz and 100 MHz bandwidth channels with 256 and 512 carriers respectively. The center frequency can range from 350 MHz to 2450 MHz. The recommendation specifies a transmission power limit of 5 dBm for the 50 MHz bandplan and 8 dBm for the 100 MHz bandplan, therefore the power spectrum density (PSD) is the same for both bandplans.

Due to the nature of an in-home wired environment, receivers that can handle

both very large and very small amplitude signals are required: when transmitter and receiver are connected on the same electric outlet there is no channel attenuation and the signal-to-noise-plus-distortion ratio (SNDR) is dominated by the receiver linearity, whereas when transmitter and receiver are several rooms apart channel attenuation is high and the SNDR is dominated by the receiver noise figure. The high-dynamic-range specifications for these receivers require the use of configurable-gain topologies that can provide both high-linearity and low-noise for different configurations [3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13].

The minimum value of SNDR depends on the design of each particular application. The G.hn recommendation provides a maximum bit-error rate (BER). The maximum data-rate of a communications system is limited by the maximum bit-error-rate (BER) that is specified to achieve throughput requirements. SNDR, a parameter usually used to define the dynamic range of an analog front-end, is directly related to BER [14, 15, 16]. Therefore, analog front-ends aim at providing a value of SNDR that is above a specified minimum value for a given range of input signal power to comply with the maximum allowed BER of the whole system.

The minimum value of SNDR ultimately depends on the maximum transmission distance that wants to be achieved at a given throughput (as the transmission distance increases, the receiver signal power decreases and thus SNDR decreases) and the maximum throughput that wants to be achieved at minimum distance (as the SNDR increases, the throughput can be increased while maintaining the same transmitted power). The system designer establishes the minimum SNDR of each stage in order to achieve the target value for the whole receiver to comply with the specifications of BER, transmission distance and throughput.

As will be seen in a later subsection, the required specifications for the G.hn front-end provided by the company include a minimum value of SNDR that needs to be achieved for a given range of input power.

1.3 Towards low-cost broadband inductor-less SoCs

System-on-Chip (SoC) was adopted in recent years as one of the solutions to reduce the cost of integrated systems. When the SoC solution started to be used, the final product was actually more expensive due to lower yield. The developments in integrated technology through the years allowed the integration of more components in lesser area with a better yield. Thus, SoCs have become a widely used solution to reduced the cost of the final product, integrating into a single-chip the main parts of a system: analog, digital and memory.

As integrated technology kept scaling down to allow a higher density of transistors and thus providing more functionality with the same die area, the analog RF parts of the SoC became a bottleneck to cost reduction as inductors occupy a large die area and do not scale down with technology. Hence, the trend moves toward the research and design of inductor-less SoCs that further reduce the cost of the final solution.

At the same time, as the demand for home networking high-data-rates communication systems has increased over the last decade, new communication systems using large channel bandwidths such as G.hn have been created to satisfy these needs. Broadband inductor-less design presents a challenge as inductors cannot be used for peaking in order to compensate the parasitic capacitances.

1.4 Research Goals and Contributions

This thesis aims at researching high dynamic range broadband inductor-less topologies to be used as the RF front-end for a G.hn receiver complying with the provided specifications. The main specifications of the RF front-end are defined in Table 1.2.

A large part of the thesis is focused on the design of the input amplifier of the front-end, which is the most critical stage as the noise figure of the input amplifier defines the achievable overall specifications of the whole front-end. Three prototypes have been manufactured in two different runs using a 65 nm CMOS process: two input RF programmable gain amplifiers (RFPGAs) and one front-end using the second RFPGA

Specification	Value
Number of gain settings	8
Output voltage (with 12 dB PAR input signal)	$\geq$0.15 V_{pp}
SNDR	$\geq$35 dB
Power consumption	$\leq$50 mW
Input power dynamic range	$\geq$80 dB
Maximum input power (100 MHz channel)	5 dBm
Maximum input power (50 MHz channel)	2 dBm

Table 1.2: G.hn RF front-end specifications.

prototype.

1.5 Thesis Organization

Chapter 2 contains an introduction to receiver front-end fundamentals. It explains concepts that will be used later on in the design and measurement of the prototypes such as noise, distortion and dynamic range. This chapter also presents available configurable architectures and the reasons behind choosing pre-attenuation based topologies for the design of the front-end.

Chapter 3 contains an introduction to design techniques for high-dynamic-range broadband inductorless RF amplifier circuits. Some of these techniques are used in the design of the amplifier prototypes, such as the active feedback input impedance matching, providing further insight on its design in the proposed prototypes. Other techniques, such as pre-attenuation based amplifiers to provide high dynamic range, are expanded by providing new alternative circuit topologies improving the existing performance.

Chapter 4 contains the design and experimental results of the first RFPGA prototype. The RFPGA is a fully-differential two-stage configurable pre-attenuation based amplifier providing 4 different gain settings. One of the gain settings is provided by by-passing the second amplifier, whereas the other 3 gain settings are provided by using a switchable capacitive attenuation topology at the input. The RFPGA uses 2 different methods of input impedance matching. The prototype has been fabricated in a 65 nm

CMOS technology, packaged inside a QFN and measured on PCB.

Chapter 5 contains the design and experimental results of the second RFPGA prototype. This RFPGA is a fully-differential double-input configurable pre-attenuation based amplifier providing 4 different gain settings with a single stage using a switchable capacitive attenuation topology. The second RFPGA also uses 2 different method of input impedance matching. The prototype has been fabricated in a 65 nm CMOS technology, packaged inside a QFN and measured on PCB.

Chapter 6 contains the design and experimental results of the front-end prototype. The front-end input amplifier uses the double-input (DI) RFPGA presented in Chapter 5. The mixer uses a folded topology composed of a current re-use transconductance amplifier (CR-TCA) and a switching stage. The CR-TCA can be by-passed thus connecting the DI-RFPGA directly to the switching stage, providing another method of configuration. Therefore, the front-end provides a total of 8 different gain settings. The prototype has been fabricated in a 65 nm CMOS technology, packaged inside a QFN and measured on PCB.

Chapter 7 contains the conclusions and suggestions for future research.

2

Receiver Front-End Fundamentals

2.1 Introduction

This chapter presents front-end fundamentals that will be used along the thesis. The chapter starts by introducing the concepts of noise, sensitivity and distortion which are basic measures for both individual circuits and front-ends. These three concepts combine together to obtain the metric of dynamic range, which provides a measure of the circuit's capability to handle a large range of input power while maintaining a minimum signal-to-noise-plus-distortion ratio (SNDR).

We also introduce the noise-power-ratio (NPR) metric which is the process used to measure the front-end dynamic range in Chapter 6. Since the front-end is designed for a multi-carrier system, a metric such as NPR that uses multiple input-tones provides a more reliable measure of circuit distortion than the classical third-order intercept point (IP3). The chapter ends by providing frequency conversion concepts to cover basic mixer specifications.

2.2 Noise and Sensitivity

Noise is a parameter of critical importance in any receiver as it corrupts the desired signal carrying the information resulting in an increase of the bit-error rate (BER). The addition of noise by a circuit is usually characterized by the noise factor (F) or alternatively by the noise figure (NF) when using logarithmic scale, which is defined as how the signal-to-noise ratio (SNR) changes from input to output:

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{2.1}$$

Since the signal of interest spans over a given bandwidth, the noise must be integrated over that bandwidth for the calculations. Noise figure is related to sensitivity in the sense that sensitivity is the minimum signal level the system can detect while providing a minimum value of SNR (which is calculated from the maximum allowed BER). By developing Eq. 2.1 we can define the sensitivity at room temperature as [17]:

$$P_{in_{min}} = -174dBm/Hz + NF + 10logBW + SNR_{min} \tag{2.2}$$

By using the maximum allowed BER of the system, the system designer can extract the minimum SNR value of the front-end. Then, the system designer sets the desired sensitivity of the system which is calculated using the maximum desirable transmission distance (as transmission distance increases, the signal is attenuated by the transmission channel and the received signal power decreases). By using the minimum SNR and the sensitivity and Eq. 2.2, the required NF of the whole front-end is obtained. Finally, the NF of each single stage is established at system level so that the NF of the whole front-end is below the calculated value. The total NF of the front-end can be expressed by the NF and gain of each individual stage [18]:

$$NF_{tot} = 10log\left(F_1 + \sum_{i=2}^{n} \frac{F_i - 1}{\prod_{j=1}^{i-1} G_j}\right) \tag{2.3}$$

Where n is the number of stages and G is the gain of each corresponding stage. This

equation considers equal input and output impedances for each stage. For different output and input impedances, which is usually the case in integrated circuits, the cascaded noise figure can be expressed as [18]:

$$NF_{tot} = 10log\left(F_1 + \sum_{i=2}^{n} \frac{F_i - 1}{\prod_{j=1}^{i-1} G_j^2 \left(\frac{R_{in_j}}{R_{out_{j-1}}+R_{in_j}}\right)^2 \frac{R_{out_{j-1}}}{R_{out_j}}}\right) \tag{2.4}$$

Where R_{in} is the input impedance of each corresponding stage, R_{out} is the output impedance of each corresponding stage and G_v is the voltage gain of each corresponding stage. As can be seen from the equations, the noise figure of each stage is divided by the gain of the previous stages when their contribution to the whole front-end is taken into account. Therefore, the most critical stage in terms of noise figure is the input amplifier since there is no previous amplification.

2.3 Distortion

Ideally, an amplifier device has a linear response from input voltage to output voltage. However, in a practical implementation, the devices have a non-linear response as shown in Fig. 2.1. In a simplified time-invariant model, the response of the amplifying device can be represented as a Taylor series:

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + a_4 v_{in}^4 + ... \tag{2.5}$$

The first term is the output DC voltage of the amplifying device, and the second term is the term of interest corresponding to the amplified input signal. The higher order terms result in unwanted distortion components (intermodulation) which mask the wanted signal reducing the SNR. If *vin* is composed of only one tone, the high-order components are located at frequencies multiple to that of the input tone and the unwanted distortion is located far from the frequency of interest. However, when the input signal contains two or more tones, the high-order components generate harmonics whose frequencies are a combination of the frequencies of the input tones. Some of these

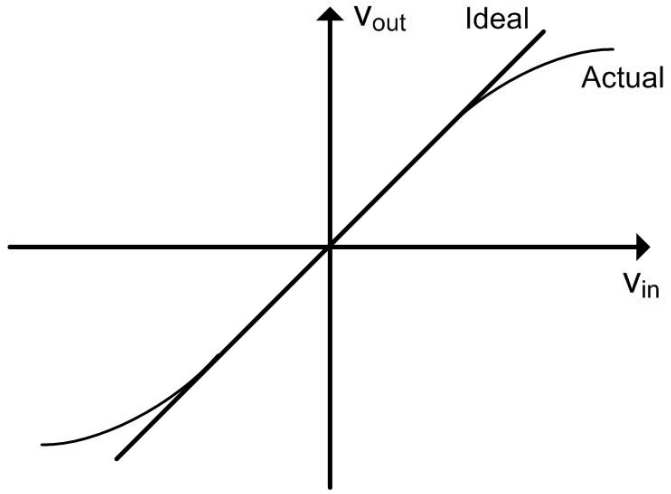

Figure 2.1: Actual versus ideal behavior of an amplifying device.

combinations fall at the frequencies of the input signal, thus adding distortion at the band of interest which decreases the SNR.

The most significant harmonics in terms of amplitude are due to the second-order and third-order non-linearities [19] whose location is shown in Fig. 2.2. Second-order harmonics can be minimized by using a differential topology. However, third-order harmonics are present in both single-ended and differential topologies. Thus, the most common measure of linearity for RF input amplifiers is the third-order input intercept point (IIP3), which provides the value of input power for which the output wanted signal and output unwanted third-order product have the same power, as shown in Fig. 2.3.

The high-order terms have a slope in logarithmic scale equal to that of the order of the polynomial (second-order non-linearities have a slope of 2, third-order a slope of 3, and so on). Therefore, intermodulation distortion is mainly important when handling large values of input power, since for the small values the power of the harmonics is much smaller than that of the signal of interest (Fig. 2.3). Then, as opposed to noise where the required front-end NF is calculated by using the minimum SNDR for the smallest input power signal, the required front-end IIP3 is calculated by using the minimum SNDR for the largest input power signal. The cascaded IIP3, equivalent to

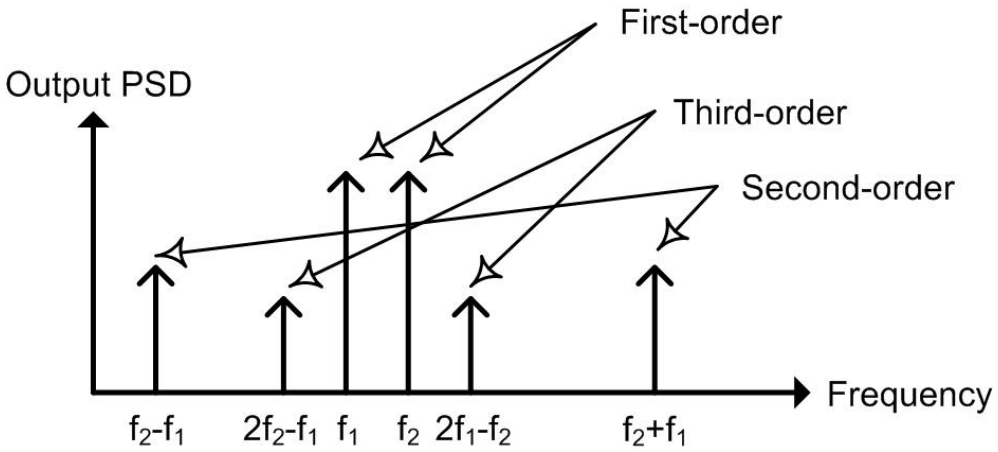

Figure 2.2: Location of second-order and third-order non-linearities.

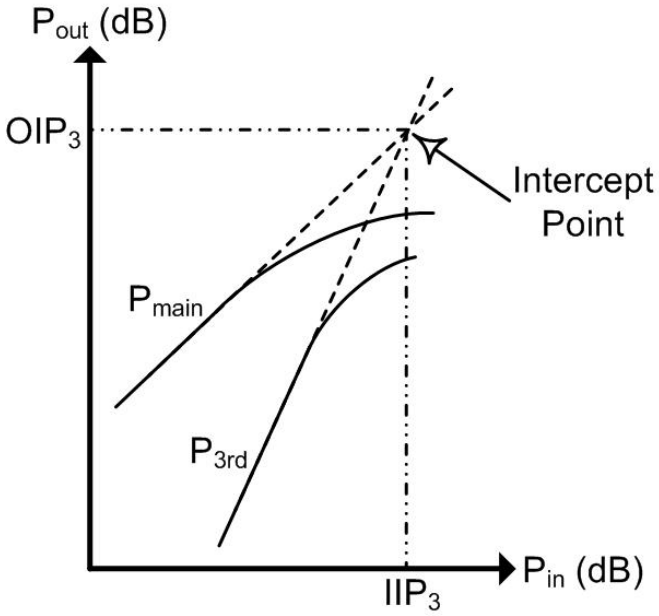

Figure 2.3: Third-order intercept point.

the cascaded noise figure, can be calculated from the IIP3 and gain of each individual stage for equal input and output impedances [18]:

$$IIP_{3_{tot}} = -10log\left(\sum_{k=1}^{n}\frac{\sum_{j=1}^{k-1}G_j^2}{IIP_{3_k}}\right)^{\frac{1}{2}} \tag{2.6}$$

Where IIP_{3_x} is the third-order intercept point of each corresponding stage and G_x is the voltage gain of each corresponding stage. One difficulty in obtaining a closed expression for the front-end cascaded IIP3 is the distortion components of different stages combine between themselves in a way that depends on the phases of each individual component [20]. The previous equation considers the conservative worst-case where all the phases are equal and thus the intermodulation products add directly.

However, the IIP3 metric considers the case of only two input tones. Present broadband communications systems such as G.hn use a large numbers of carriers up to 512 and the theoretical distortion analysis of such a system becomes very complex. The final objective of a distortion measure is to provide a reliable value of intermodulation distortion (IMD) that can be used to calculate the SNDR of the system as shown in Fig. 2.4 for large and small input signal power. Multiple-tone IMD for SNDR calculation can be obtained either by an indirect metric using IIP3 values such as composite triple beat (CTB) [4] or direct metrics such as adjacent channel power ratio (ACPR) and NPR [21, 22] which use a multiple-tone input signal.

As opposed to other communication systems where the distortion and SNDR are based upon the interaction between the signal of interest and out-of-band blockers, in this application there is only one channel with a signal of interest composed of multiple carriers and the out-of-band blockers are filtered with a diplexer. Therefore, the distortion and SNDR are based upon the interaction of all the in-channel carriers between themselves.

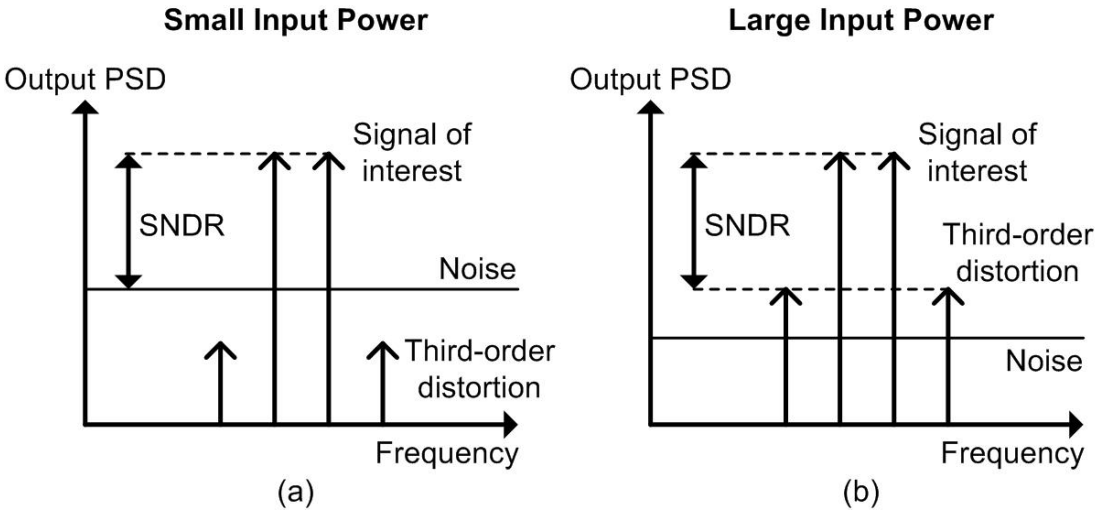

Figure 2.4: SNDR calculation at (a) Small input power (b) Large input power.

2.4 Dynamic Range

Dynamic range is defined as the difference between the maximum power and the minimum power a circuit can handle, where the definition of maximum and minimum power depends on each particular application. In the case of an RF front-end inside of a whole receiver system, the maximum and minimum power the circuit can tolerate is defined by the minimum SNDR the DSP stage needs to provide the required maximum BER. The maximum power is limited by the distortion generated by the circuits whereas the minimum power is limited by the sensitivity. This difference between the minimum and maximum power values is the dynamic range of the system.

Standards such as G.hn require a large dynamic range as they can receive both large amplitude input signals when both transmitter and receiver are connected at the same wall electrical outlet, and very small amplitude input signals when transmitter and receiver are located far from each other at different rooms. Such a large dynamic range requires the use of Automatic Gain Control (AGC) [19]. When not using AGC, a front-end must comply with the noise and distortion specifications simultaneously, which given current CMOS technologies and power consumption constraints is not viable. Therefore, configurable topologies are a common design solution in high dynamic range

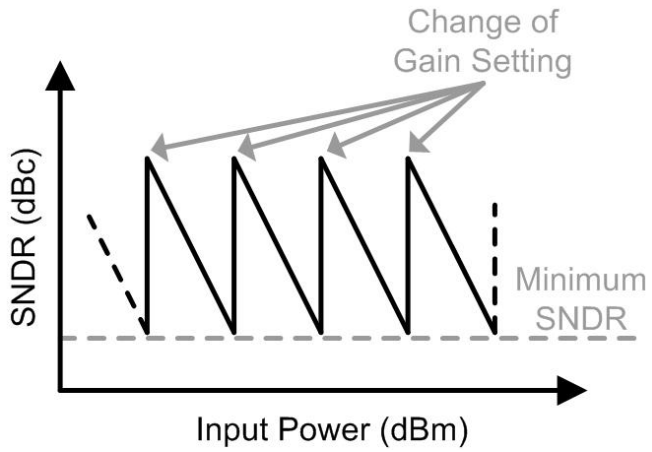

Figure 2.5: SNDR vs input power with constant SNDR steps.

front-ends [3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13].

Configurable topologies provide different gain settings with different specifications of noise and linearity. For the lowest value of input power the front-end is configured at the gain setting which provides the best noise figure, that being the highest gain setting. As the input power increases the minimum SNDR is reached and the front-end is configured at the next gain settings which increasingly provides better linearity, thus resulting in better SNDR as shown in Fig. 2.5, until the maximum input power is reached and the front-end is configured at the last gain setting providing maximum linearity.

The ideal way to perform experimental measures of dynamic range is to use a multiple-tone input signal equivalent to that of the practical application so that the SNDR can be measured directly, instead of measuring separately the noise output power and the distortion output power (through an indirect measure such as using IIP3 to calculate the CTB [4]) and adding them together to find the floor level. This thesis performs the SNDR measurements using the noise power ratio (NPR) metric.

2.4.1 NPR Measurements

NPR is a figure of merit used to measure the SNDR of a given circuit and provides a more reliable value than indirect figures of merit calculated through the IIP3 measured

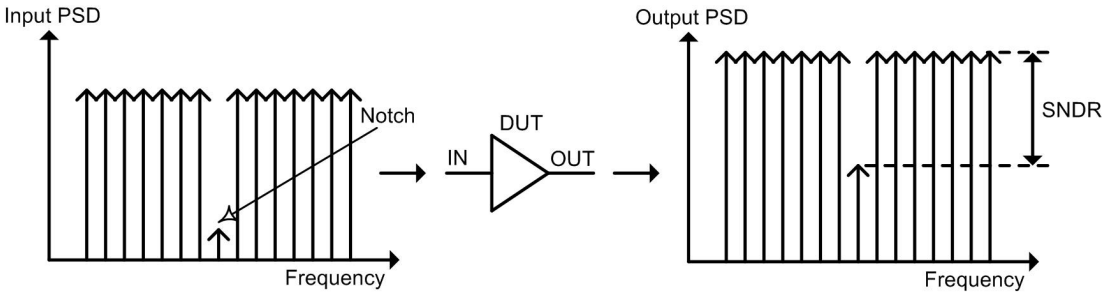

Figure 2.6: NPR measurement process.

values [23]. The NPR measurement is based on creating a broadband input stimulus with power, occupied bandwidth, carrier spacing and spectral shape equivalent to those of the practical case and adding a notch at some frequency location inside the channel. Then, the test signal is fed through the device under test (DUT) and the resulting SNDR is measured at the output using a power spectrum analyzer, as shown in Fig. 2.6.

The important factor in an NPR measurement is for the SNDR at the input between the signal of interest and the notch to be sufficiently below the maximum value of SNDR that wants to be measured at the output. To obtain an input SNDR larger than 60 dB in the front-end measures for this thesis, we use the Agilent Signal Studio for Noise Power Ratio [24]. This method uses a computer, a vector signal generator and a power spectrum analyzer connected via LAN or GPIB as shown in Fig. 2.7. The vector signal generator creates an input signal with the specifications (channel bandwidth, carrier spacing, number of carriers and signal power level) configured by the user and the notch power level is measured using the power spectrum analyzer. If the notch is not low enough, the computer configures the vector signal generator to add pre-distortion to the generated signal in order to decrease the notch power. This process is repeated continuously in a closed loop until the required notch power level is achieved or the maximum number of iterations is achieved. A sample screenshot of input signal after applying pre-distortion zooming into the notch is shown in Fig. 2.8, and a sample screenshot of the resulting signal passing through a front-end including down-conversion is shown in Fig. 2.9.

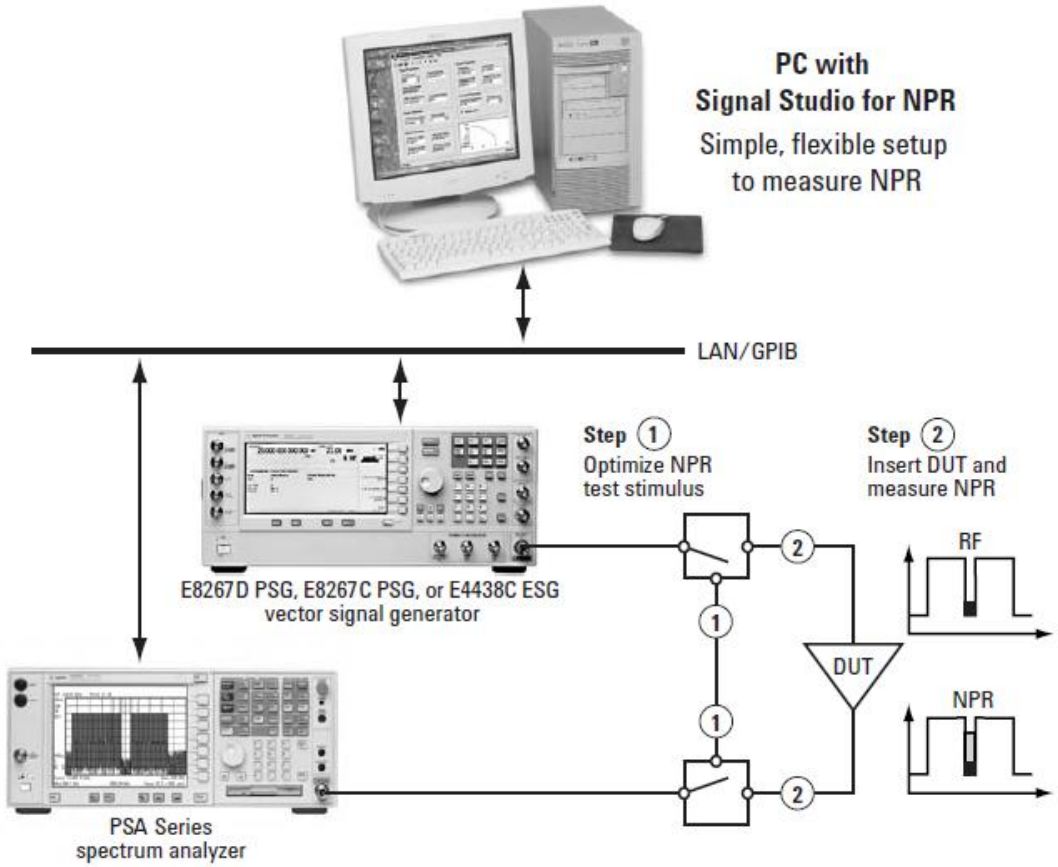

Figure 2.7: Agilent Signal Studio for Noise Power Ratio configuration.

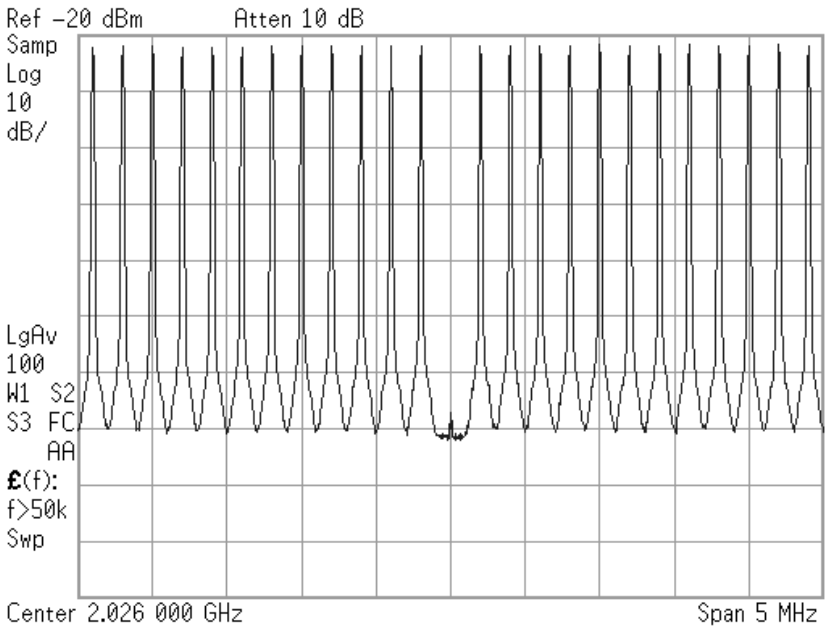

Figure 2.8: Sample screenshot of NPR input signal after applying pre-distortion zooming into the notch.

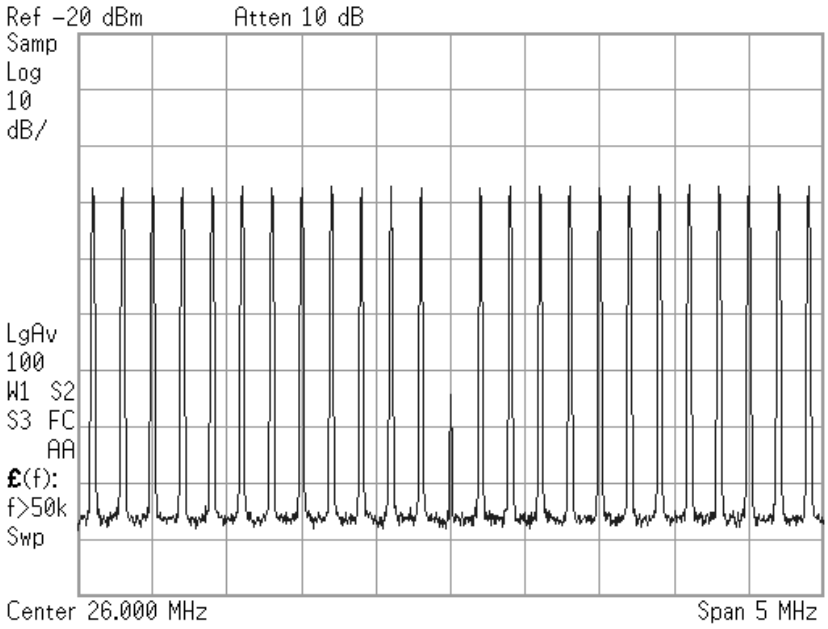

Figure 2.9: Sample screenshot of a front-end output NPR measurement zooming into the notch.

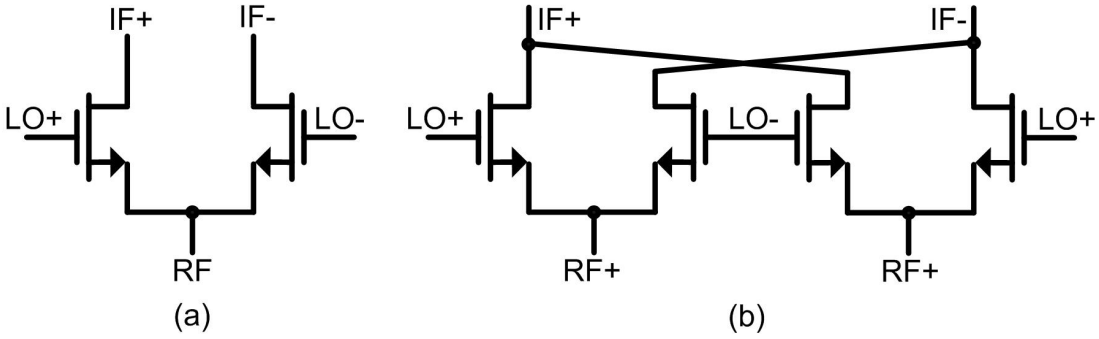

Figure 2.10: Common mixer implementation in CMOS (a) Single-ended (b) Differential.

2.5 Frequency Conversion

The RF signals in a receiver need to be down-converted to a lower frequency before they go into the analog-to-digital converter (ADC) which transforms the waveform into a digital signal. The process of digital conversion is not performed at RF due to the high power consumption of ADCs at high frequencies. The circuit that performs the frequency down-conversion process is called mixer and consists of two inputs, the RF and local oscillator (LO) ports, and one output, the intermediate frequency (IF) port.

The mixer contains a circuit that multiplies the LO signal by the RF signal. The product of these two signals can be decomposed into two components, one of which is the sum of the frequencies of RF and LO and the other is the difference. Therefore, the component of interest at the output (IF port) is the $RF - LO$ term (or $LO - RF$ if LO has a higher frequency than RF) which converts the RF signal to a lower frequency. The LO is usually a sinusoid signal.

The most common mixer topology in CMOS technology uses the structure shown in Fig. 2.10 (single-ended and differential). The RF signal enters through the source of the transistors and the LO signal through the gate. Two instances of LO signal are used, one at 0 phase and the other at 180 phase identified as $LO+$ and LO- respectively. The goal in the design process is to have only half of the transistors on at any given time. The resulting differential signal at the output (the IF port) contains two terms as previously mentioned, at the sum and difference frequency of the LO and RF signals.

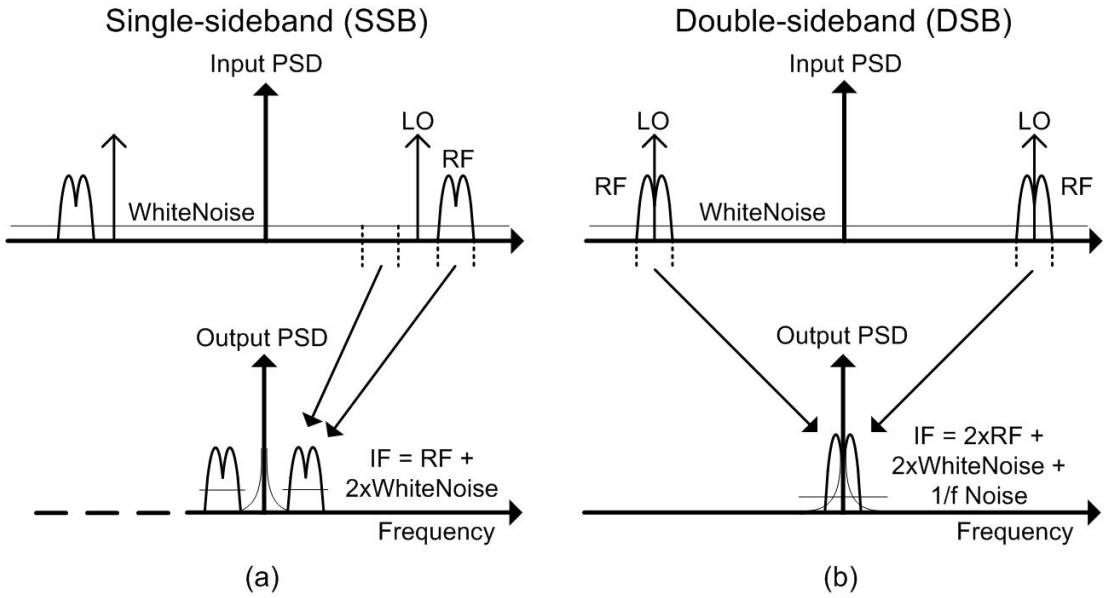

Figure 2.11: SSB and DSB mixer concepts.

The LO frequency can be higher/lower than the RF frequency in which case the mixer topology is called single-sideband (SSB) and is shown in Fig. 2.11a. If the LO frequency is located just in the middle of the RF signal, the mixer topology is called double-sideband (DSB) or direct conversion and is shown in Fig. 2.11b.

In an SSB mixer, the IF signal contains only one instance of the RF signal and two instances of white noise. Thus, the noise figure increases not only due to the noise added by the mixer circuitry itself, but also due to the conversion mechanism. In a DSB mixer, although the IF contains two instances of the RF signal and two instances the white noise, it also contains 1/f noise. In this case, the noise added through the conversion mechanism is due to the 1/f noise. Whether to use a DSB or SSB topology is decided by the system designer. The mixer in this thesis is designed as an SSB topology.

Mixers can be either active (they use a bias current) or passive (they use no biasing current). Passive mixers have losses but generally provide a better linearity than active topologies, whereas active topologies provide gain and thus a better overall front-end noise figure. Although passive mixers have no biasing current, they require large LO

amplitudes to provide a large linearity, indirectly resulting in a considerable increase of the mixer power consumption. Thus, it cannot be considered that the passive mixer has no power consumption. Also, a passive mixer has losses. If these losses need to be compensated at later by adding gain using an amplifier, power consumption will be increased further.

The most important specifications for a mixer are the same than the ones in an amplifier: noise figure, linearity and gain. The mixer, however, has another specification which is of importance, that being the isolation between ports (RF, LO and IF). Isolation can be largely improved by using a differential topology. In the case of a differential mixer, the isolation is ideally infinite although in a practical implementation mismatch results in a finite isolation.

3

High-dynamic-range Broadband Inductor-Less RF Amplifier Techniques

3.1 Introduction

This chapter introduces several techniques used in RF amplifiers to provide high-dynamic-range and broadband behavior without using inductors. Some of the techniques presented in this chapter are used in the design of the prototypes presented in the following chapters. These include parallel resistance and active feedback for input impedance matching, resistive loads and active loads for inductor-less loads and configurable-gain capacitive-attenuation topologies for high linearity. Since these techniques are all used in the design of the three prototypes, they are presented here for ease of reference and to maintain the focus on the core circuit design in the prototype design chapters.

The other techniques presented in this chapter which are not used in the design of the prototypes have been analyzed and tested in schematic design during the thesis but it was decided that they were not the most adequate solution to provide the required

specifications. These techniques, although not used in the prototypes, are presented in order to provide insight on the differences between the techniques used and not used in the prototypes.

We initially discuss input impedance matching techniques that provide broadband matching, including parallel resistance, resistive feedback, common-gate and active feedback. Then, we present amplifier loading techniques that provide broadband gain, including resistive load, active load, active inductors and capacitive peaking. Finally, we present techniques to increase the linearity of an amplifier, including derivative superposition, feedback, noise/distortion cancellation, post-distortion and pre-attenuation.

3.2 Input Impedance Matching

Input impedance matching can be performed either internally or externally. One common approach to internal broadband input impedance matching is performed by using several narrowband amplifiers with inductors tuned at different frequencies for input impedance matching, thereby covering all the required bandwidth [25, 26, 27]. This approach takes a lot of chip space due to the large area occupied by the inductors, which is undesirable in SoC solutions as the total cost increases significantly.

Using external matching (e.g. with an LC ladder [28, 29, 30, 31, 32]) avoids the chip area constraints that forbid the use of integrated inductors. However, external components also result in cost increase due to the additional printed circuit board (PCB) area and the components. Thus, integrated inductor-less input impedance matching is the most adequate solution in cost terms. This section describes how to perform input impedance matching with parallel resistance, resistive feedback, common-gate and active feedback.

3.2.1 Parallel Resistance

The most basic input impedance matching topology is to use a parallel resistance at the input of the amplifier as shown in Fig. 3.1. The value of the parallel resistance

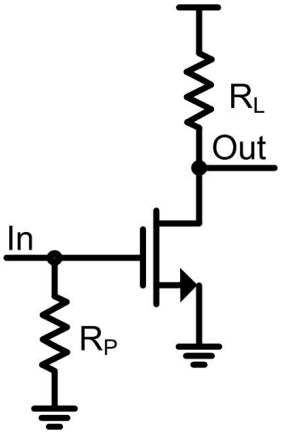

Figure 3.1: Basic topology of the parallel resistance input impedance matching.

R_P has the same value as the source resistance. Using this method, a real impedance component is added to the input impedance, providing broadband input impedance matching.

Besides the simplicity of its design, another advantage of this topology is that it is highly suitable for high linearity circuits. This topology only requires one linear passive component and the input signal is attenuated by half before going through the amplifying transistor, improving the linearity of the whole topology.

This topology, however, results in a very high noise figure. On one hand, the resistor itself generates thermal noise at the input which is added to the signal at the input before any amplification is provided[1]. On the other hand, although attenuating the signal by half results in higher linearity, it also results in higher noise figure.

Thus, the parallel resistor topology is most suitable for high linearity circuits which do not require a low noise figure.

3.2.2 Resistive Feedback

The basic topology of the resistive feedback [27, 33] input impedance matching topology is shown in Fig. 3.2. It is based on using a feedback resistor located between the drain

[1]The increase in noise factor in a whole chain due to a certain circuit or component is divided by the total gain provided before that particular circuit or component. When a circuit or component generates noise before any amplification is provided, the noise factor due to that circuit or component is directly added to the total noise factor of the whole chain.

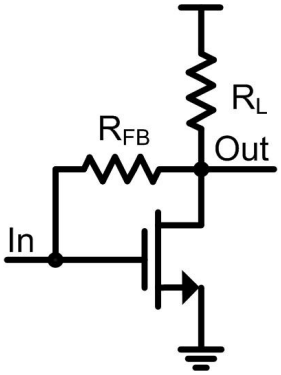

Figure 3.2: Basic topology of the resistive feedback input impedance matching.

and the gate of the amplifying device. By placing this resistor, the input impedance presents a real part that can be used for impedance matching.

As compared to performing input impedance matching by using a parallel resistance, the signal is not attenuated at the input and therefore provides a better noise figure. Nevertheless, the feedback resistor adds thermal noise which, depending on the required value of the resistor to provide input impedance matching, may become a dominant factor in the total noise generated by the amplifier.

When using resistive feedback, reverse isolation is degraded even when using a cascode topology, therefore it is important to ensure that the circuit is stable within the desired frequency range.

The resistive feedback topology provides good broadband impedance matching at frequencies below a few gigahertz, but above that the capacitive component dominates over the real part of the input impedance and the s_{11} is degraded. In this case, the designer is forced to use a mechanism to compensate the imaginary part. The compensation is usually done by using an inductor at the input [34, 35, 36] as shown in Fig. 3.3. [37] proposes a topology using a single compact low-Q on-chip inductor, showing an improved trade-off between performance, power consumption, and die area.

A resistive feedback wideband low-noise amplifier (LNA) with feedforward noise and distortion cancellation is presented in [38] as shown in Fig. 3.4. This topology has no inductors and by using an amplifier between the gate of the main amplifying

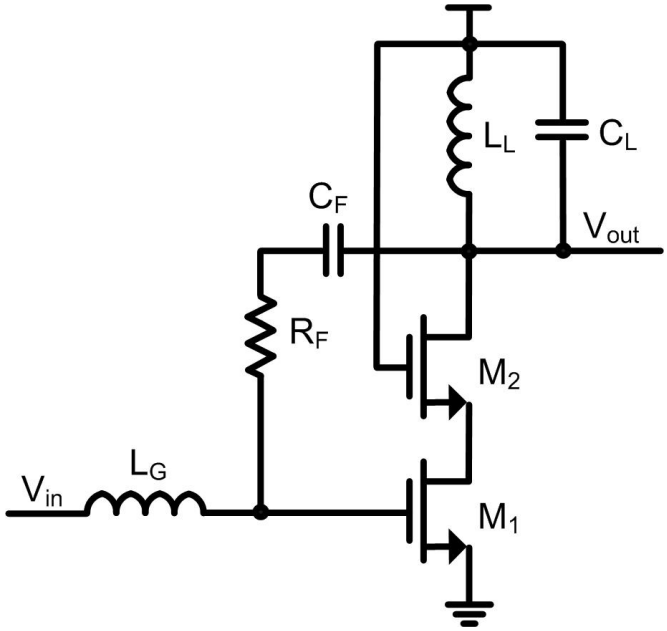

Figure 3.3: Resistive feedback using input inductor.

device and the gate of the cascode transistor is able to provide noise and distortion cancellation.

3.2.3 Common-Gate

The basic topology of the common-gate input impedance matching is shown in Fig. 3.5, which differs from the previous input impedance matching topologies in that the signal enters through the source of the transistor instead of the gate. By using this method, the input signal sees the transistor channel from source to drain, which provides the real part of the input impedance. The input impedance of the common-gate topology is thus the inverse of the transistor transconductance.

The common-gate topology is implemented with a current source at the source of the transistor for applications up to the low gigahertz range [39, 40, 41] and can alternatively use an inductor in place of the current source to enhance the bandwidth of the input impedance matching [42, 43, 44, 45, 46]. The source inductor resonates with the parasitic capacitances of the transistor thus extending the bandwidth.

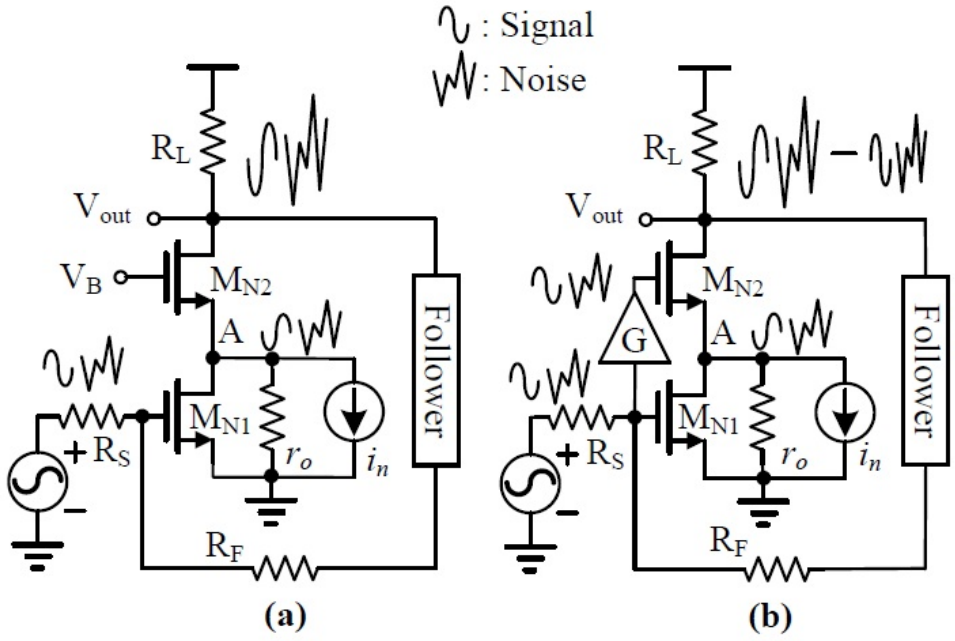

Figure 3.4: Resistive feedback using feedforward noise and distortion cancellation [38] (a) Conventional resistive feedback LNA (b) Resistive feedback LNA using feedforward noise and distortion cancellation.

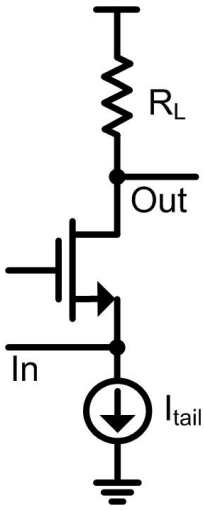

Figure 3.5: Basic topology of the common-gate input impedance matching.

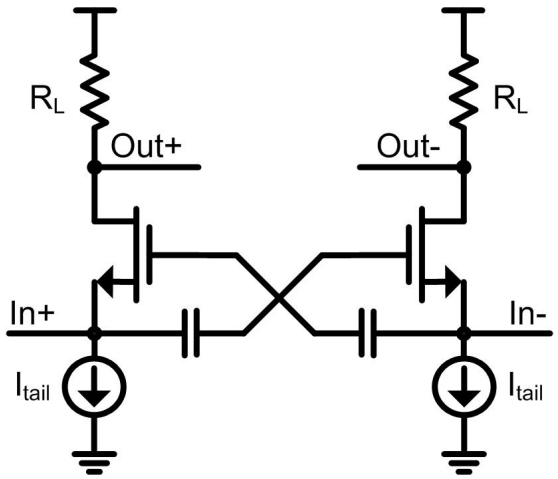

Figure 3.6: Basic topology of the common-gate capacitive cross-coupling input impedance matching.

Although the common-gate topology generally provides better noise figure than the parallel resistance topology, the noise performance of the amplifier cannot be optimized as the transconductance of the input transistor is fixed with a value inverse to the source resistance in order to provide input impedance matching[2] [42, 43]

One way to improve the noise figure of the common-gate topology is to use capacitive cross-coupling [40, 42, 43]. This technique can only be used in differential topologies and is shown in Fig. 3.6. When using this topology the input impedance is now equal to the inverse of twice the transconductance of the amplifying transistor. Thus, for a same value of source resistance, the amplifying transistors using capacitive cross-coupling topology have double the transconductance compared to the case not using it, therefore lowering the noise figure of the amplifier. This topology can be improved by using dual capacitive cross-coupling [41], which further decreases the noise figure by using two additional transistors and two additional capacitors, as shown in Fig. 3.7.

The common-gate topology can be used in conjunction with a common-source topology to provide input impedance matching, single-ended to differential conversion and noise-canceling simultaneously [47, 48, 49, 50]. The topology of such circuit is shown

[2]The noise figure of an amplifier with constant gain composed of a transistor and a load resistance depends on the transconductance of the amplifying device.

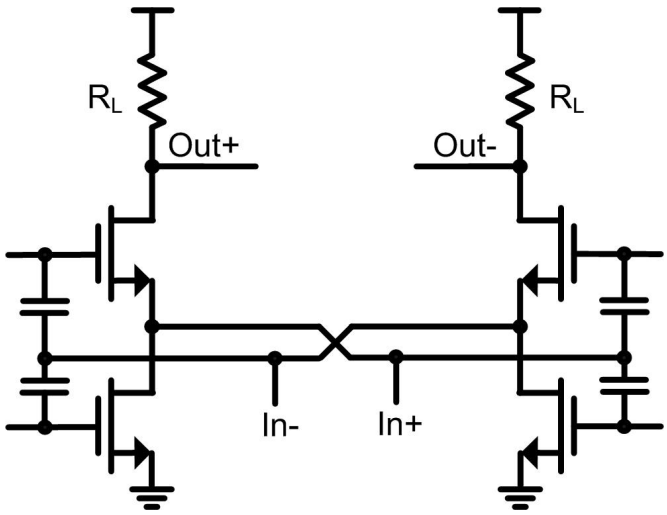

Figure 3.7: Basic topology of the common-gate dual capacitive cross-coupling input impedance matching.

in Fig. 3.8 [47]. The input impedance of this topology at the low gigahertz range is dominated by the resistive part provided by the common-gate transistor. As frequency increases, the input impedance degrades faster than a standalone common-gate topology due to the additional capacitance added by the common-source transistor.

The single-ended to differential conversion is provided by the difference in phase shifting of the two amplifying devices. The common-gate transistor does not change the phase of the input signal after amplification, whereas the common-source inverts the phase of the input signal, resulting in a 180 degree shift. Therefore, the output of the circuit provides a differential signal.

As for the noise-canceling property, it can be understood as follows. The noise generated by the common-gate transistor can be represented by a current source that generates both a voltage at the input node and a fully correlated inverse voltage at the common-gate output. When the input noise due to the common-gate transistor is amplified by the common-source device, it is shifted by 180 degrees. Then, the noise generated by the common-gate transistor appears at both output branches with the same phase as long as both devices provide equal gain. Thus, the noise generated by the common-gate device is canceled and the noise figure is mainly dominated by the

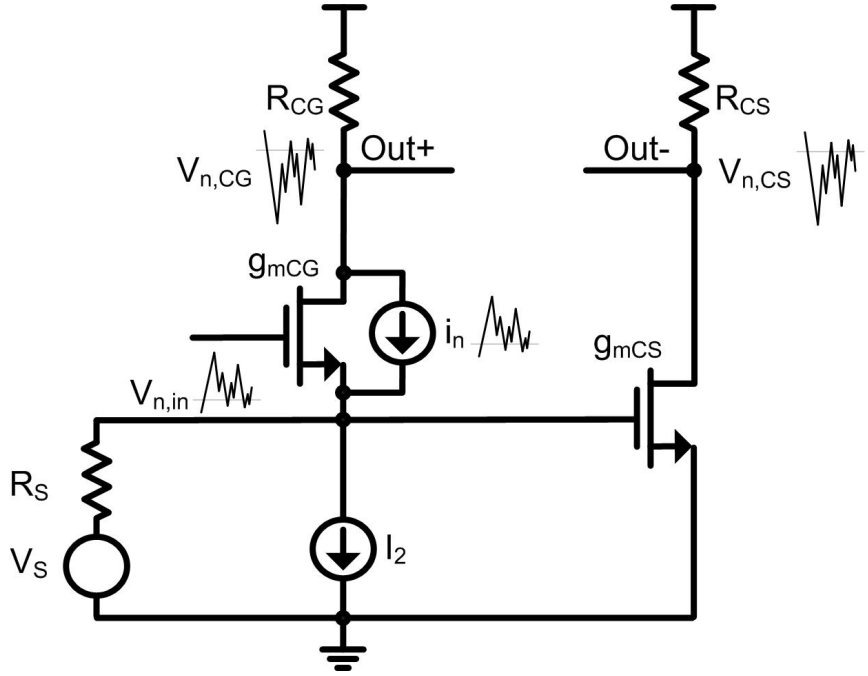

Figure 3.8: Combined common-gate common-source topology providing simultaneous input impedance matching, single-ended to differential conversion and noise-canceling.

common-source transistor.

3.2.4 Active Feedback

The basic topology of the active feedback input impedance matching topology [51, 52, 53] is shown in Fig. 3.9. Input impedance matching can be achieved when the following condition is fulfilled:

$$g_{m2} = \frac{1}{R_S\left(1 + g_{m1}R_L\right) - R_F} \tag{3.1}$$

Where g_{m1} and g_{m2} are the transconductances of the two transistors and R_S is the source impedance the circuit needs to match. The transconductance g_{m2} can be tuned either through the width of M_2 or the biasing current I_F. The equation only applies to positive values of g_{m2}. Therefore, the following condition for the R_F value needs to be complied with:

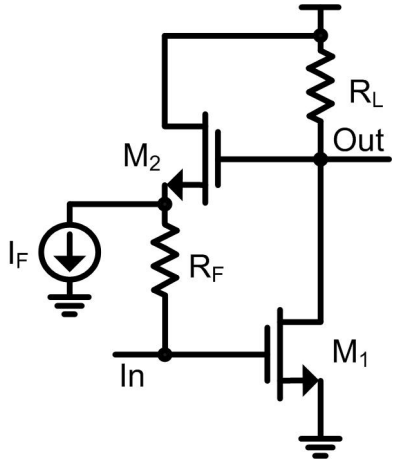

Figure 3.9: Basic topology of the active feedback input impedance matching.

$$R_F \leq R_S\,(1 + A_v) \tag{3.2}$$

Where A_v is the open-loop voltage gain. It can be shown [51] that a higher value of R_F results in a higher noise figure but also higher linearity. Thus, the required value of R_F will depend on the specifications of each particular application.

Several variations can be applied to the active feedback basic topology. Active feedback input impedance matching can be applied to a differential topology [53] by duplicating the basic topology and adding a tail current source as shown in Fig. 3.10a.

The active feedback can also be applied to single-ended to differential conversion. Fig. 3.10b shows such a configuration which, instead of duplicating the active feedback in both branches, combines the active feedback into a single branch achieving higher loop gain bandwidth [54]. Another possible implementation of single-ended to differential conversion with active feedback is shown in Fig. 3.10d. This topology uses a common-gate common-source topology with local feedback. By adjusting the local open-loop gain, the noise figure can be optimized by distributing the power consumption among transistors and resistors based on their contribution to the total noise figure [55]. The basic active feedback topology can also be modified into a dual active feedback topology which provides a higher and flatter broadband response at the cost of

slightly higher noise figure [56, 57].

Another variation is to use AC coupling in the feedback loop [58] as shown in Fig. 3.10c. This variation, although allows for independent biasing of the feedback transistor, adds a high-pass filter at the output node which modifies the circuit operation. The current source in the feedback loop can be eliminated as shown in Fig. 3.10e, which avoids the dependence of the input impedance on R_F [59]. A current sink can also be added at the input node (Fig. 3.10f) to make the input DC voltage level independent of the feedback loop [51].

3.2.5 Implications on the prototype designs

This section has presented the following four input impedance matching topologies:

- Parallel resistance
- Resistive feedback
- Common-gate
- Active feedback

These topologies were tested on schematic in order to analyze their performance and their suitability to the prototype designs. Since the final prototypes are configurable topologies with several gain settings (in depth analysis provided in Chapters 4, 5 and 6), two different input impedance matching topologies are used: parallel resistance and active feedback. Parallel resistance is used at the lower gain settings where non-linearities dominate and higher noise is allowed, thus making this topology more adequate than the other three. At the higher gain settings the active feedback topology was chosen as it provided better noise figure than the other two in the analysis performed on schematic.

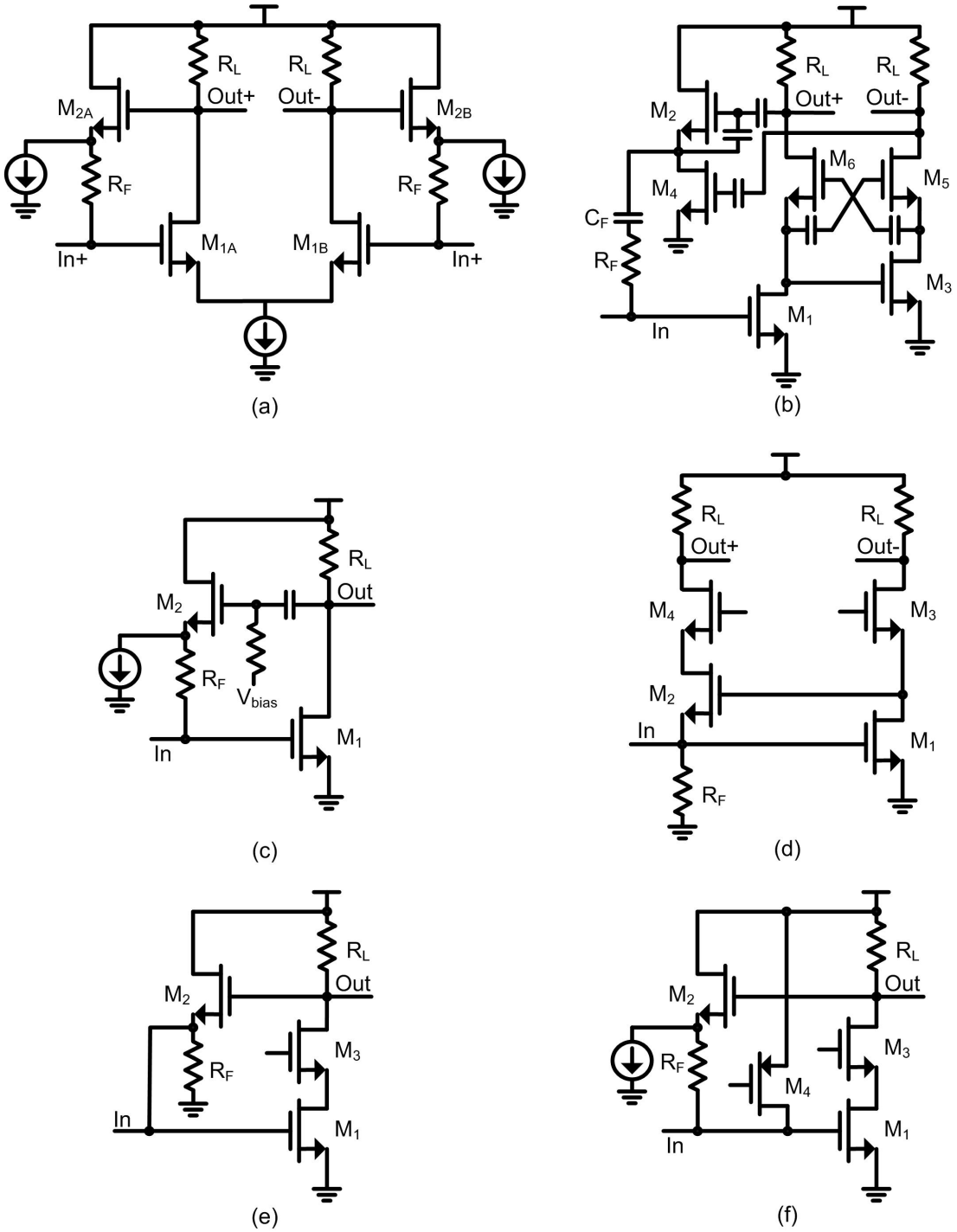

Figure 3.10: Alternative active feedback input impedance matching topologies (a) Differential (b) Single-ended to differential conversion with single-branch active feedback (c) AC coupling at the output (d) Single-ended to differential conversion with local feedback (e) Without current source at the feedback (f) Current sink at the input.

3.3 Inductor-less Loads

The load in an amplifier is responsible for the I-to-V conversion at the output. Traditionally, inductors have been extensively used at the load both as a narrowband solution [60, 61, 62] for applications such as GSM and WiFi (IEEE 802.11) and as a broadband solution [36, 52, 63, 64] for applications such as UWB or DTV. As has been addressed in previous sections, inductors occupy a large area and do not scale down with technology, therefore are cost restrictive for integration in a full SoC using cutting-edge technologies. This section presents several broadband loading topologies without using inductors.

3.3.1 Resistive Loads

The resistive loading is the most basic topology to be used as a load and is shown in Fig. 3.11. It consists on using a resistance at the output which performs the I-to-V conversion. Increasing the resistance value results in higher gain but decreases bandwidth due to the low-pass RC filter effect between the load resistance and the parasitic capacitance. Also, the voltage headroom decreases which worsens linearity.

This topology, although basic, is widely used in broadband amplifier design [4, 5, 6, 7, 8, 9, 10, 11, 12, 13] due to its simplicity and effectiveness. More complex loading techniques are used to improve certain specifications at the cost of worsening other ones, such active loads to provide better noise at the cost of decreased linearity and active inductors to provide higher bandwidth at the cost of higher noise and lower linearity.

3.3.2 Active Loads

The active load topology, as its name implies, uses active devices as the load of a circuit. Fig. 3.12a shows the basic topology of a differential amplifier with active loads implemented using PMOS transistors. An amplifier using active loads provides higher gain and lower noise compared to an amplifier using resistive loads with equal power

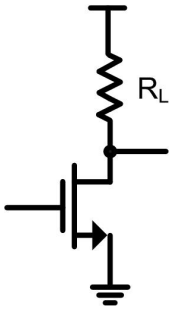

Figure 3.11: Basic topology of an amplifier with resistive load.

consumption [65] and without sacrificing voltage headroom [66]. However, the additional non-linearities due to the transistors result in lower linearity, which is specially important as the signal has already been amplified when it reaches the active loads [25, 67, 68, 69].

Circuits using active loads commonly use a common-mode feedback (CMFB) topology to set the DC voltage value at the output as shown in Fig. 3.12b. In this topology, two large resistors are used at the output to obtain the common-mode voltage, which is fed into an operational transconductance amplifier (OTA) and compared to a reference voltage which is the desired DC voltage level at the output of the main circuit. The middle point between the two resistors is virtually grounded but does not affect the voltage swing headroom [66]. The control voltage at the output of the OTA can be used to control either the tail current source or the gate voltage of the PMOS loads. The resistors can be substituted for transistors operating in the linear region [70].

3.3.3 Active Inductors

Active inductors are topologies which, by using active devices, behave as an inductor under certain operating conditions. Active inductors have several characteristics that differentiate them from passive inductors, offering the following advantages [71]:

- Small area: since they use transistors instead of a metal spiral, active inductors occupy small area and scale down with technology.
- Large and tunable self-resonant frequency: as technology scales down, active

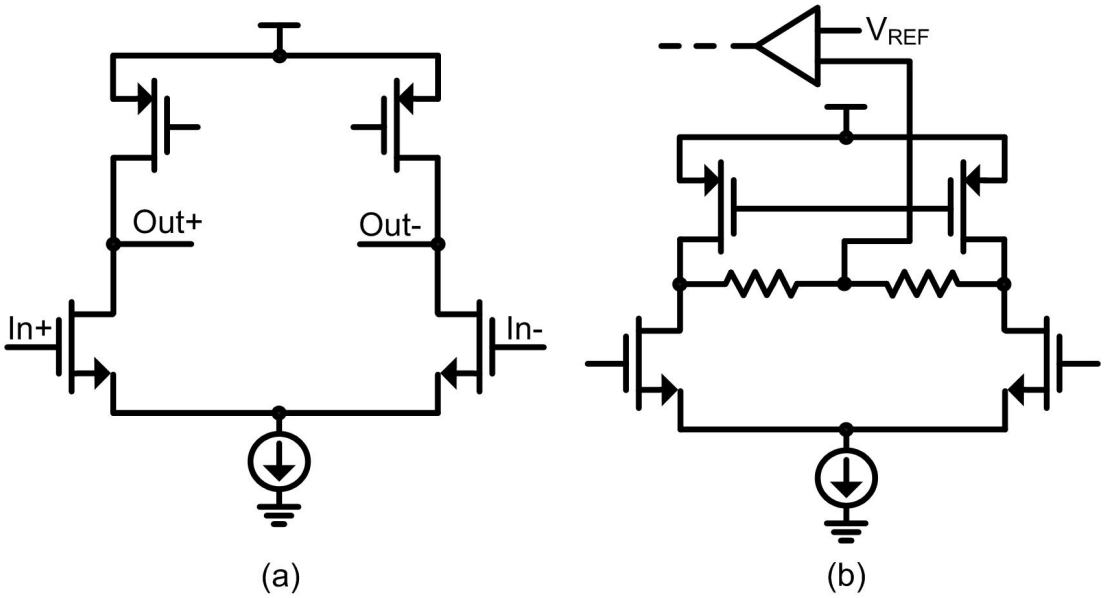

Figure 3.12: Basic topologies of a circuit with active loads (a) Differential amplifier with PMOS loads (b) Differential amplifier with active loads and CMFB.

devices can operate at higher frequencies, which allows the use of active inductors in high frequency applications.

- Large and tunable inductance: the inductance value is inversely proportion to the transconductance of the transistors, therefore large inductances can be obtained with small widths. Also, the inductance is tunable through several parameters depending on each particular topology, such as current consumption or voltage biasing, making active inductors suitable for multi-standard applications.

- Tunable quality factor: as with inductance, the quality factor is also tunable through several parameters of the circuit.

Active inductors, however, also present several disadvantages compared to passive inductors [71]:

- Limited dynamic range: since the active inductor behavior depends on a given biasing of the transistors used in the topology, large-swing signals can take the

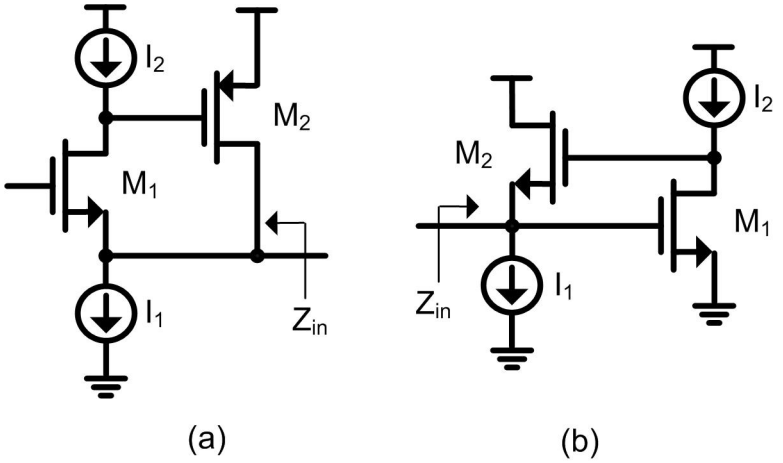

Figure 3.13: Basic topology of an active inductor (a) Using one PMOS and one NMOS transistor (b) Using two NMOS transistors.

transistors operating point outside the margin that guarantees inductive behavior, becoming a resistive topology.

- Increased noise: the transistors in the active inductor topologies add additional noise which may result in a considerable increase of the noise figure of the circuit. This makes them most suitable for implementing loads, as the signal has already been amplified previously and the effect on noise is smaller.

- Vulnerability to process variations and mismatch: active inductors are much more vulnerable to changes in inductance and quality factor due to variations in technological parameters upon manufacturing.

- Reduced linearity: transistors are non-linear devices by nature, therefore using them to implement active inductors results in a severe degradation of linearity. When using active inductors as loads, this degradation becomes very important since the signal has already been amplified.

The most common active inductor topologies are shown in Fig. 3.13. Fig. 3.13a shows the topology using one PMOS and one NMOS transistor [72] and Fig. 3.13b shows the topology using two NMOS transistors [73]. The advantages of using these

topologies are evidently the reduction of chip area and processing cost compared to integrated passive inductors, and the increased tunability. However, their main disadvantage is a low quality factor which also leads to increased noise [71]. The inductance, series resistance and quality factor of the active inductor can be expressed as [74]:

$$L = \frac{C_{gs2}}{g_{m1}g_{m2}} \tag{3.3}$$

$$R_S = \frac{g_{o1}}{g_{m1}g_{m2}} \tag{3.4}$$

$$Q = \frac{1}{g_{m1}\omega L} \tag{3.5}$$

Where g_{m1} and g_{m2} are the transconductances of the transistors, g_{o1} is the output conductance and C_{gs2} is the gate to source capacitance.

The Wu active inductors [75, 76] (Fig. 3.14) are a variation of the basic topology. This topology only uses one current source (I_1) and the second current source (I_1) is provided by the current of the circuit where the active inductor is attached, thus acting as a current re-use topology. The cost of reducing the power consumption in a Wu topology as compared to the basic topology is an increase in the series resistance as given by:

$$R_S = \frac{g_{o1} + g_{o2}}{g_{m1}g_{m2}} \tag{3.6}$$

Another active inductor topology is the Lin-Payne inductor [77, 78] shown in Fig. 3.15a. This topology provides the same inductance, series resistance and quality factor as the basic topology while adding the advantage of requiring a lower minimum supply voltage. The minimum supply voltage of the Lin-Payne topology is $V_T + 2V_{T_{sat}}$ whereas the basic and Wu topologies require $2V_T + 2V_{T_{sat}}$, thus increasing voltage headroom which results in larger signal swing and better linearity.

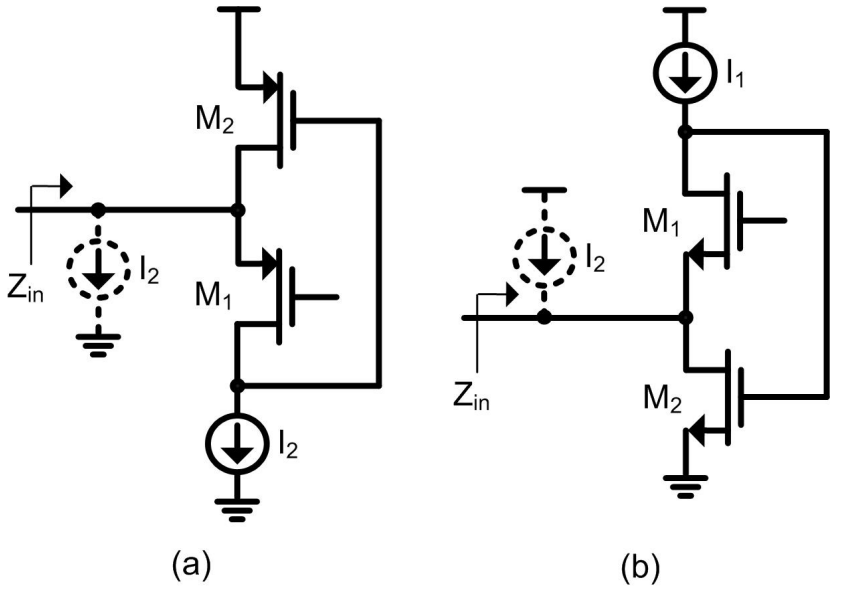

Figure 3.14: Active inductor using the Wu topology (a) PMOS (b) NMOS.

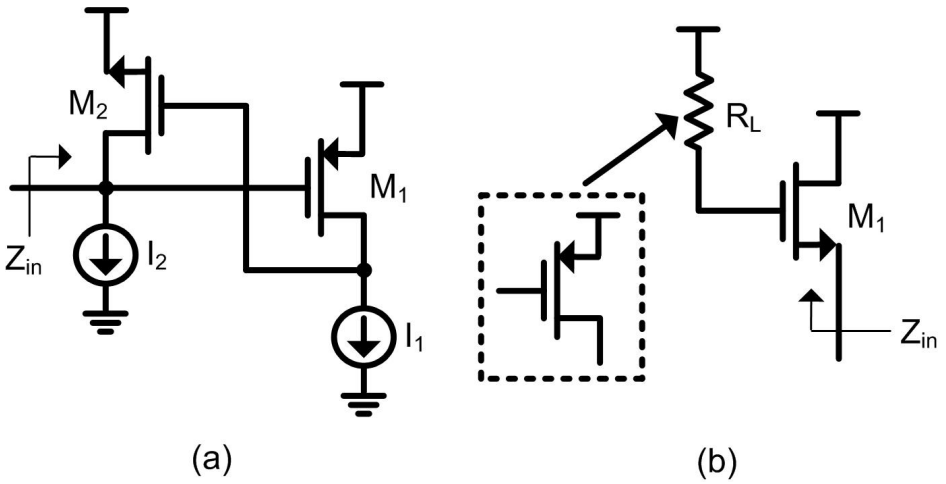

Figure 3.15: Active inductor topologies (a) Lin-Payne (b) Hara.

The most simple implementation of an active inductor in terms of components is the Hara topology [79]. This topology, shown in Fig. 3.15b, is implemented by using one transistor and one resistor. Alternatively, the resistor can be changed for a transistor operating in linear region to provide the required resistance value. The drawback of this topology is the higher value of series resistance as compared with the other topologies. The inductance and series resistance is given by:

$$L = \frac{R_L C_{gs}}{g_m} \tag{3.7}$$

$$R_S = \frac{1}{g_m} \tag{3.8}$$

3.3.4 Capacitive Peaking

Capacitive peaking is an alternative to provide a similar effect to inductive peaking to increase bandwidth [80, 81, 82, 83]. Inductive peaking topologies use a resistor and an inductor in series as the load. Fig. 3.16a shows an amplifier using this structure followed by a mixer stage. The bandwidth extension is provided by the addition of a zero in the gain transfer function due to the inductor.

The same effect can be obtained by substituting the inductor in the amplifier load for a capacitor at the next stage, as shown in Fig. 3.16b. A capacitor and a resistor are placed in parallel at the source of the next stage's transistor, resulting in the same bandwidth extension effect by adding a zero to the gain transfer function of the amplifier.

The gain of the inductive peaking and capacitive peaking can expressed as [84]:

$$A_{iL} = \frac{I_{out}}{I_{in}} = \frac{g_{m1} R_L \left(\frac{sL_L}{R_L} + 1\right)}{s^2 L_L C_{gs1} + sR_L C_{gs1} + 1} \tag{3.9}$$

$$A_{iC} = \frac{I_{out}}{I_{in}} = \frac{\frac{g_{m2} R_L}{1+g_{m2} R_S} (sR_S C_S + 1)}{s^2 \frac{R_S C_S R_L}{1+g_{m2} R_S} + s\frac{C_{gs2} R_S + R_S C_S + C_{gs2} R_L}{1+g_{m2} R_S} + 1} \tag{3.10}$$

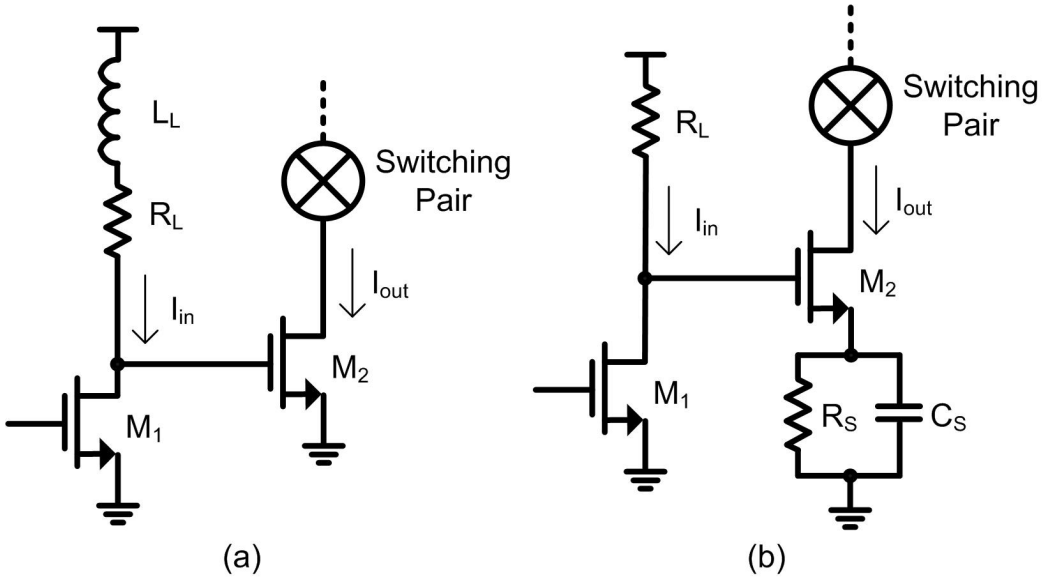

Figure 3.16: Techniques for adding a zero in the gain transfer function (a) Inductive peaking (b) Capacitive peaking.

The capacitive peaking effect can also be explained as follows using the resistive degeneration concept. A resistive degeneration topology results in a decrease of gain as the resistance value at the source increases. When a capacitor is added in parallel to the degeneration resistance the following effect occurs. At low frequencies, the source capacitor provides a large impedance and the impedance at the source is only that of the source resistor. However, as frequency increases the impedance of the capacitor decreases, decreasing the total impedance at the source node and therefore increasing gain as frequency increases.

Due to the added capacitor at the source node of an amplifier, the capacitive peaking topology is prone to have stability issues which requires an in depth analysis to ensure that the designed circuit is stable in all the operating range. Also, this method only adds a zero for a certain range of component values, which may difficult the design.

3.3.5 Implications on the prototype designs

This section has presented the following four inductor-less loads:

- Resistive loads
- Active loads
- Active inductors
- Capacitive peaking

These topologies were tested on schematic in order to analyze their performance and their suitability to the prototype designs. The fabricated prototypes use two different inductor-less loads: resistive and active. Resistive loads are used in the input amplifier and in the switching stage of the mixer since they were found to provide the best trade-off between bandwidth, linearity and noise. Active loads are used in the transconductance stage of the mixer. As will be seen later (in depth analysis provided in Chapters 4, 5 and 6), this stage is by-passable and only used at the higher gain settings, where low linearity is allowed.

After in depth analysis and testing of the presented active inductor topologies, they were found to be not suitable for this thesis' prototypes due to a very low linearity. Capacitive peaking was also discarded in order to avoid stability issues. Also, capacitive peaking provides the zero in the gain transfer function only for a certain range of component values, which further complicated the design of the prototypes since they use several gain settings with different specifications.

3.4 High-Linearity Techniques

As previously presented, the dynamic range of a receiver is limited by noise at the low power range and by linearity at the high power range. This section presents several design techniques to increase the linearity of an amplifier in order to improve dynamic range. Since the work presented in this thesis in based on using differential topologies to provide immunity to the noise coming from the digital part of a SoC, this section focuses on third-order intermodulation products since differential topologies have an inherent high rejection to second-order products.

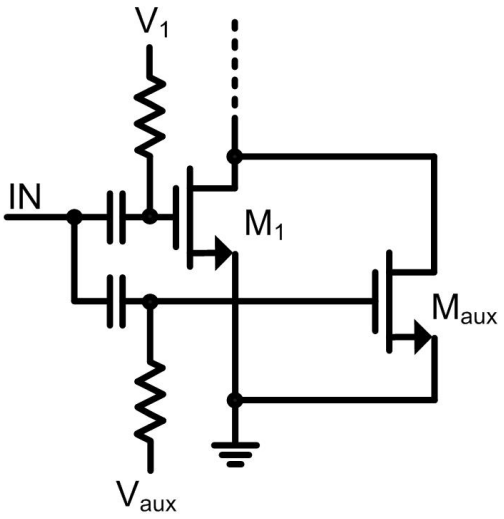

Figure 3.17: Derivative superposition structure.

3.4.1 Derivative Superposition

The derivative superposition method [85, 86, 87, 88] is called as such because it uses the third-order intermodulation products of an auxiliary transistor to cancel the third-order products of the amplifying transistor as shown in Fig. 3.17. This process is explained as follows. The small-signal output current of a common-source MOS transistor can be expressed as a power series of the gate-source voltage [89]:

$$i_d(v_{gs}) = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + ... \tag{3.11}$$

Where g_x are the coefficients defining the strength of each product. The term g_1 corresponds the transconductance of the transistor (g_m) whereas the term g_3 corresponds to the third-order non-linearities. Both coefficients can be calculated as:

$$g_1 = \frac{\delta I_D}{\delta V_{GS}} \tag{3.12}$$

$$g_3 = \frac{1}{6}\frac{\delta^3 I_D}{\delta^3 V_{GS}} \tag{3.13}$$

The dependence of g_3 on V_{GS} is such that the value of g_3 changes from positive

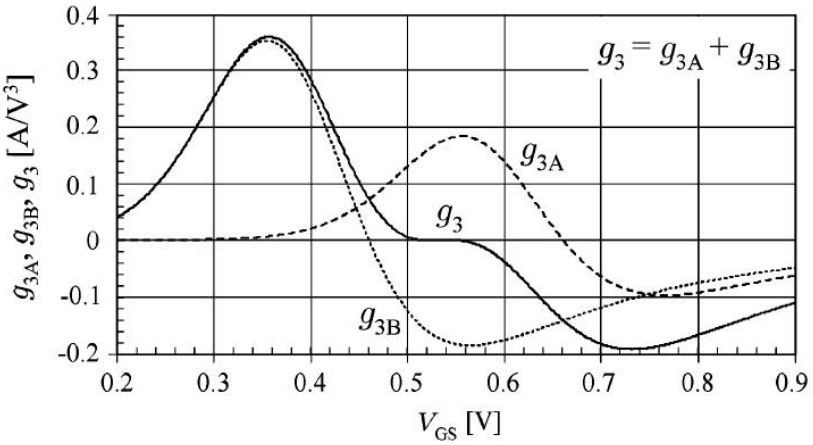

Figure 3.18: Derivative superposition technique [91]: Third-order coefficients of the main and auxiliary transistors in the derivative superposition method.

to negative as the transistor changes between the weak, moderate and strong inversion regions. The sizing and biasing point required to provide high gain and low noise specifications results in a positive value of g_3 [90]. In order to compensate that, the derivative superposition method uses an auxiliary transistor working in weak inversion that provides a g_3 value equal to that of the amplifying transistor but with of opposite sign as shown in Fig. 3.18 [91]. The two third-order derivatives cancel each other and the resulting IIP3 is infinite. The achievable IIP3 in a practical implementation is limited by process variations, mismatch and parasitic capacitances. Since the auxiliary transistor is working in weak inversion, its power consumption, noise and gain contribution are negligible.

Besides the limitation of achievable third-order cancellation in practical implementations due to process variations, mismatch and temperature, this technique is also limited by the weak inversion auxiliary transistor, which may not be able to operate at a sufficiently high frequency and cannot handle large signals as it would result in the device turning off, no longer providing the required g_3 curve [91].

The two curves of g_3 when using an auxiliary transistor are not symmetric, and thus the range of gate-source voltage that provides third-order non-linearity cancellation is very narrow. To increase the voltage range the designer can use several auxiliary

transistor at the cost of degrading gain, noise and bandwidth [92].

3.4.2 Harmonic Termination

The harmonic termination technique is based on adding a termination network to the circuit that modifies the contribution of second-order distortion to the third-order distortion. By tuning the termination impedances at certain frequencies, the amplitude and phase of the second-order interaction terms can be adjusted to cancel the intrinsic third-order distortion term [93].

A Volterra series analysis shows that the two-tone IIP3 of a common-source MOS stage has an inverse dependence on the following term [94]:

$$\varepsilon(\Delta\omega, 2\omega) = g_3 - \frac{2g_2^2}{3}\left[2k(\Delta\omega) + k(2\omega)\right] \tag{3.14}$$

Where ω is the angular center frequency of the two input tones, $\Delta\omega$ is their frequency separation, g_x are the coefficients defining the strength of each product and $k(x)$ is a function that is defined by the circuit gain and the impedances looking into the source and into the load (shown in Fig. 3.19). The term $\varepsilon(\Delta\omega, 2\omega)$ shows that the total third-order distortion depends on both second-order and third-order non-linearities.

This second-order interaction comes from feedback between output and input. The feedback paths allow the second-order non-linearities to be mixed with the fundamental tones resulting in the addition of an additional term to the total third-order distortion. This additional term can be tuned in order to improve the IIP3 of the circuit.

It can be shown [94] that, if the real parts of the terminations impedances are positive (which is the case for a stable amplifier), the term in brackets of Eq. 3.14 has a positive real part. Therefore, $\varepsilon(\Delta\omega, 2\omega)$ can be tuned closer to zero (i.e. no third-order distortion) if g_3 is positive. The amplitude and phase of the second-order term depend on the input and output impedances. The termination impedances can be tuned at the second-order frequency in order to improve IIP3 without modifying the value of the termination impedances at the fundamental frequency to avoid affecting gain and noise

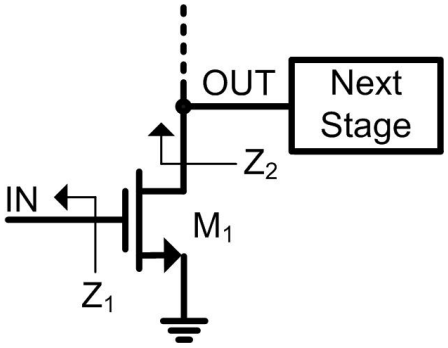

Figure 3.19: Impedances affecting the behavior of the harmonic termination third-order cancellation technique.

figure. The tuning is performed by using resonant LC tanks changing the impedance at the $\Delta\omega$ or 2ω frequencies

The main disadvantage of this technique is the requirement of a positive g_3. In a MOS transistor, g_3 is negative when the transistor is operating in strong inversion region and positive when the transistor is operating in the weak or moderate inversion regions. However, in these latter two regions the transconductance and maximum operating frequency are lower than in strong inversion region, making the technique less suitable than other ones for use in RF applications [95]. Another disadvantage of this technique is the difficulty of implementation in wideband systems since the impedance tuning network needs to be optimized for a large range of frequencies without affecting the behavior at the fundamental frequency.

In a circuit using a MOS in strong inversion, the third-order distortion cannot be canceled but the circuit can be designed in order to decrease the contribution of the distortion due to second-order interaction. A cascode configuration can be used to decrease the impedance looking into the load (Z_2) which improves IIP3 [96]. The use of capacitive cross-coupling further reduces the impedance seen into the output node, resulting in increased IIP3 [43]. However, the improvement provided by these methods are not as good as the harmonic termination, but avoids the use area-consuming inductors and can be applied in wideband circuits.

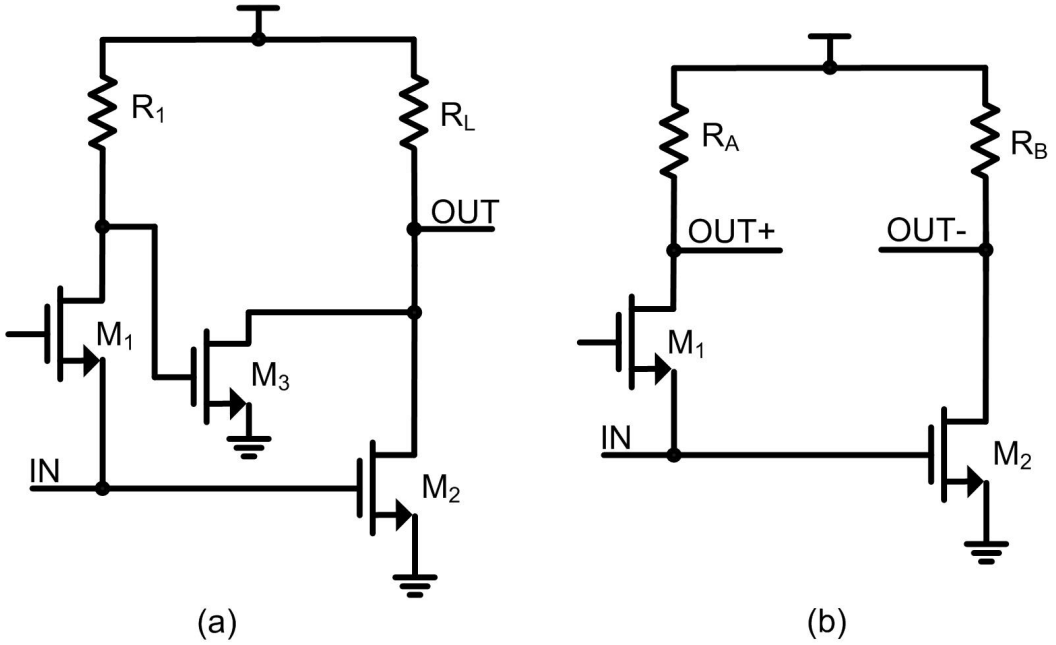

Figure 3.20: Noise/distortion cancellation topologies (a) Single-ended (b) Single-ended to differential conversion.

3.4.3 Noise/Distortion Cancellation

The noise/distortion cancellation technique combines a common-source stage and a common-gate stage to provide input impedance matching and simultaneous noise and distortion cancellation of the matching device (the common-gate transistor). This technique can be applied to a single-ended topology [97] (Fig. 3.20a) or be used to provide single-ended to differential conversion [47, 48, 98] (Fig. 3.20b).

The cancellation property can be understood as follows. The noise and distortion generated by the common-gate transistor can be represented by a current source that generates both a voltage at the input node and a fully correlated inverse voltage at the common-gate output as shown in Fig. 3.21, where the fundamental signal is in solid line and noise/distortion is in dashed line. When the input noise/distortion due to the common-gate transistor is amplified by the common-source device, it is shifted by 180 degrees. Thus, the noise/distortion generated by the common-gate transistor appears at both output branches with the same phase as long as both devices provide equal

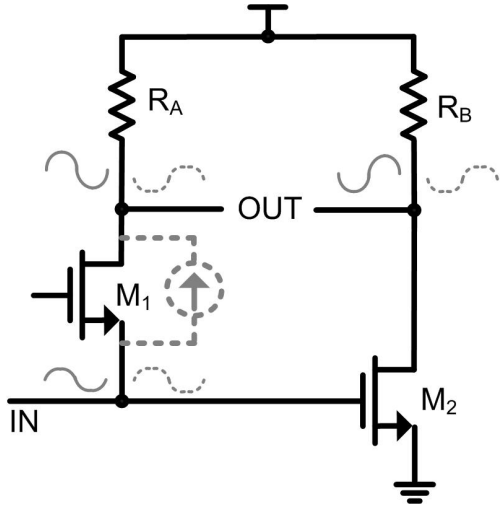

Figure 3.21: Signal phases in the noise/distortion cancellation topology: fundamental signal in solid line and noise/distortion in dashed line.

gain. Thus, the noise/distortion generated by the common-gate device is canceled and the noise figure and IIP3 is mainly dominated by the common-source transistor.

The noise/distortion cancellation technique can be designed using three approaches:

- The transconductances of the CS and CG transistors are equal and the load resistors are also equal [99].
- The transconductance of the CS transistor is n times larger than the CG transistor, and the load resistors are equal [100].
- The transconductance of the CS transistor is n times larger than the CG transistor, and the load resistor of the CS branch is n times smaller than the resistor of the CG branch [47].

The noise figure, voltage gain and gain imbalance of the first approach is independent of the value of n. This approach has a high noise figure due to the low transconductance of the CS branch, since it requires the same transconductance than the CG branch which is fixed by the input impedance matching. The second approach has decreasing noise figure and increasing voltage gain as n increases. However, the gain imbalance also increases with n. The third approach provides decreasing noise figure as

n increases and voltage gain and gain imbalance are independent of n. However, this approach has the challenge of designing a compact layout robust to process variations and mismatch due to the different resistor size.

3.4.4 Post-distortion

The post-distortion technique uses the non-linearities generated by an auxiliary transistor to cancel the linearity of the main amplifying device similar to the derivative superposition method [101, 102, 103]. This technique, however, uses a transistor operating in the saturation region and is connected only at the output of the amplifying device, hence not affecting input impedance matching.

The simplified schematic of the post-distortion technique is shown in Fig. 3.22a with its respective circuit implementation [101] shown in Fig. 3.22b. The drain current of transistor M_1 can be expressed using a Taylor series as follows:

$$i_1(v_{gs}) = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + ... \tag{3.15}$$

Where g_x are the coefficients defining the strength of each product. The term g_1 corresponds the transconductance of the transistor (g_m) whereas the term g_3 corresponds to the third-order non-linearities. The non-linear gate voltage of M_3 ($v_{G_{M3}}$) and the drain current of M_3 (i_3) can be expressed as follows [101]:

$$v_{G_{M3}} = -\frac{\alpha}{g_1} i_1(v_{in}) \tag{3.16}$$

$$i_{out} = \frac{1}{\beta}\left(g_1 v_{G_{M3}} + g_2 v_{G_{M3}}^2 + g_3 v_{G_{M3}}^3 + ...\right) \tag{3.17}$$

Where α and β are the transconductance ratios between M_1 and M_2 and between M_1 and M_3 respectively. Combining Eq. 3.15-3.17, we can define the transconductance and third-order non-linearity of whole topology [101]:

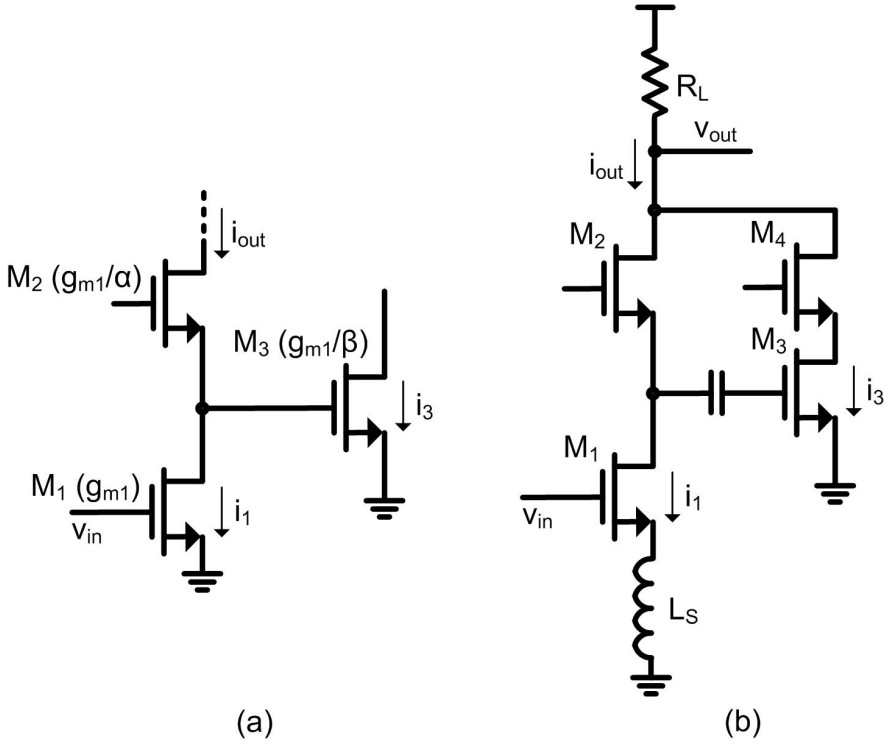

Figure 3.22: Basic topology of the post-distortion technique (a) Core components (b) Implementation in [101].

$$g_{1_{out}} = g_1 \left(1 - \frac{\alpha}{\beta}\right) \tag{3.18}$$

$$g_{3_{out}} = g_3 \left(1 - \frac{\alpha}{\beta} - \frac{\alpha^3}{\beta}\right) + \frac{2(g_2\alpha)^2}{g_1\beta} \tag{3.19}$$

The equations show that the ratios between transconductances α and β affect both the gain (which depends on $g_{1_{out}}$) and linearity (which depends on $g_{3_{out}}$). By choosing adequate values of α and β it is possible to cancel the intrinsic third-order distortion term (due to g_3) and the total third-order distortion is only due to second-order interaction (dependent on g_2). The values of α and β need to be optimized to avoid a large gain loss.

This technique is highly dependent on the transconductances of the transistors and thus highly dependent on biasing conditions, which limits the maximum achievable

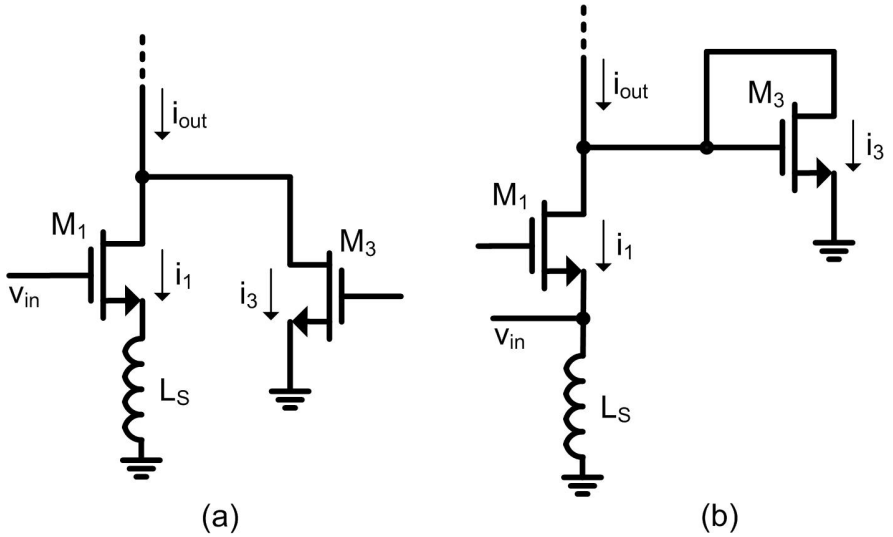

Figure 3.23: Alternative implementation of post-distortion (a) Implementation in [103] (b) Implementation in [102].

IIP3 in practical applications due to process variations, mismatch and temperature. Alternative implementations of the post-distortion technique are shown in Fig. 3.23a [103] and Fig. 3.23b [102].

3.4.5 Configurable-Gain Topologies

As has been explained in the previous chapter, standards such as G.hn require large dynamic range circuits. However, the maximum noise figure and minimum linearity specifications do not need to be complied with at the same time. For large power input signals, higher noise figure is allowed, whereas for small power input signals, lower linearity is allowed. Thus, configurable-gain amplifiers can be used to provide higher linearity by decreasing the gain as the input signal power increases.

Configurable-gain amplifiers are commonly designed by varying the load impedance (Z_L) [9, 10], varying the input transconductance (G_m) [11, 12, 13] or using pre-attenuation based topologies [4, 5, 6, 7, 8], as shown in Fig. 3.24.

In variable-load amplifiers, the value of the load is modified to increase or decrease the gain of the circuit. By decreasing the load value, gain decreases and the output swing is smaller, resulting in the amplification device generating less distortion. How-

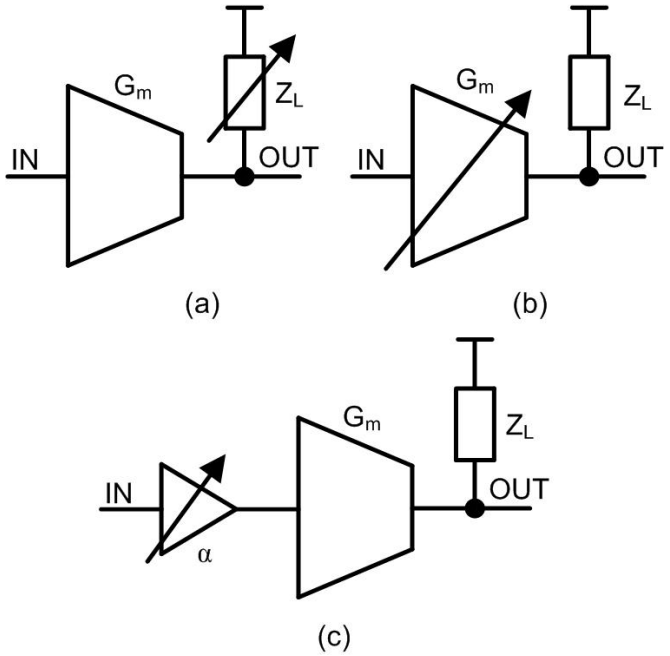

Figure 3.24: Configurable-gain amplifier topologies: (a) Variable-load (b) Variable-G_m (c) Pre-attenuation based.

ever, since the amplification device remains at the same operating point independently of the load value, the linearity enhancement for each dB decrease in gain is less efficient than the other topologies that provide gain configuration by varying the main transconductor operating conditions or pre-attenuating the signal before amplification.

In variable-G_m amplifiers, the operating conditions of the input transconductance are modified to change the specifications. In [11] a common-gate (CG) topology with current steering (Fig. 3.25a) is used to provide gain control. In this topology large degeneration is used to increase linearity performance, however this comes at the cost of a much higher minimum noise figure, requiring the use of an external LNA. In [12] a similar concept is used. In this case a common-source (CS) topology with current steering and source degeneration is used (Fig. 3.25b), also resulting in a significant increase of the minimum noise figure.

Pre-attenuation based configurable-gain amplifiers (Fig. 3.24c) are another option for the design of a high-dynamic-range receiver. These topologies are based on adding

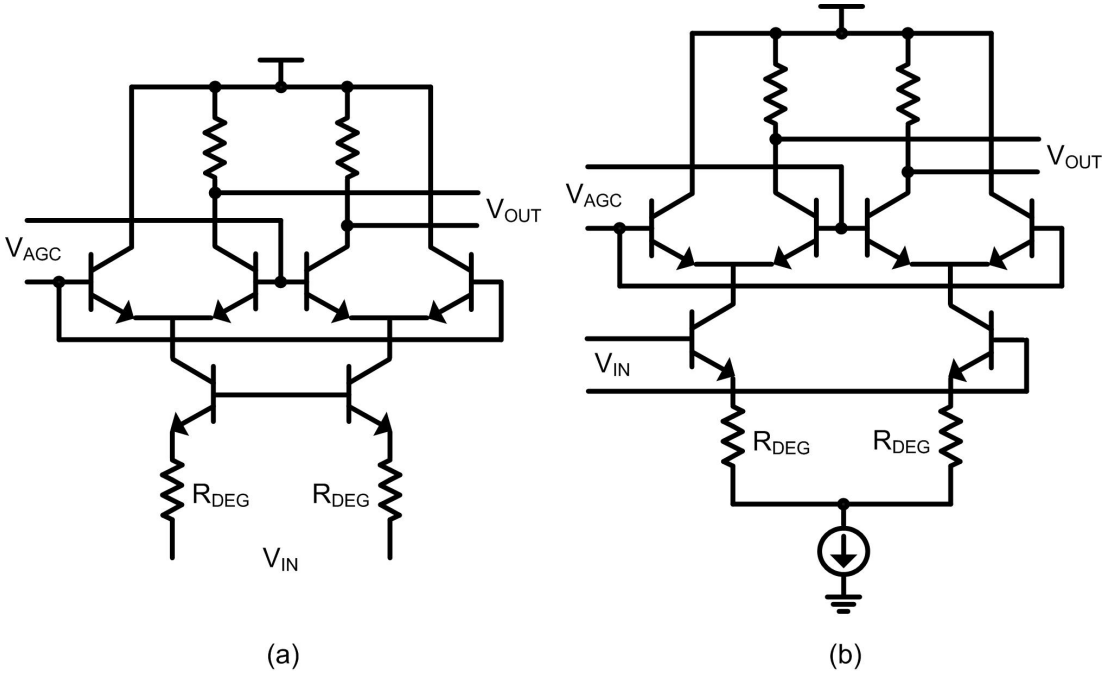

Figure 3.25: Variable-G_m amplifiers with current steering and degeneration: (a) Common-gate (b) Common-source.

attenuation (α) at the input before any signal amplification takes place. By using this topology, the IIP3 of the amplifier core remains the same, but since the signal that reaches the input of the amplifier has been attenuated, the third-order distortion generated by the circuit is smaller. When α equals 0 dB, the received signal is fed directly to the amplifier without adding any noise, avoiding any trade-off between noise and linearity as with variable-G_m amplifiers.

Pre-attenuation based amplifiers can either be implemented with a resistive attenuation topology (Fig. 3.26a) [4] or a capacitive attenuation topology (Fig. 3.26b) [5, 6, 7, 8]. The resistive attenuation circuit provides 6 dB of attenuation per stage along with good impedance matching if resistor values are chosen accordingly. The main drawback of this topology is the high noise figure due to the resistive termination of the amplifier. The capacitive attenuation topology solves this problem by using a ladder based on capacitors [104].

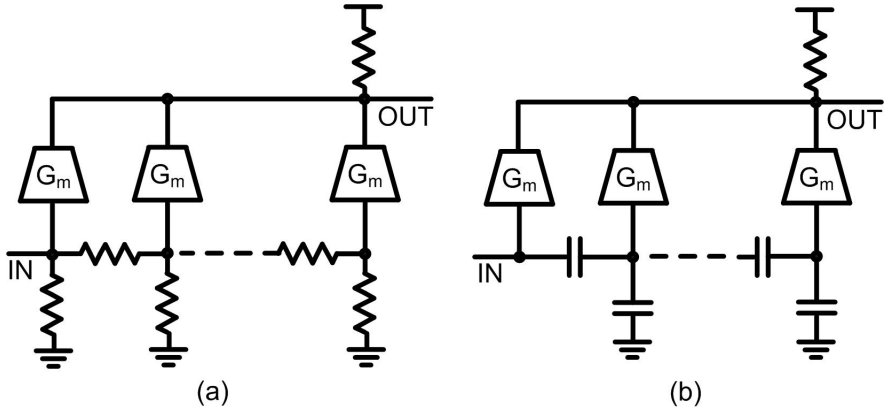

Figure 3.26: Pre-attenuation based amplifier topologies: (a) Resistive (b) Capacitive.

3.4.6 Implications on the prototype designs

This section has presented the following five high-linearity techniques:

- Derivative superposition
- Harmonic termination
- Noise/distortion cancellation
- Post-distortion
- Configurable-gain topologies

Table 3.1 shows a silicon-verified performance comparison of the previously presented high-linearity techniques. This table is not provided to perform a strict comparison between topologies (which is not optimal since the fabrication process, power consumption and bandwidth are different between circuits) but rather to show the achievable values of IIP3 for each technique.

As the table shows, the best IIP3 results are achieved using configurable topologies (configurable-load and pre-attenuation). The large IIP3 values provided by these topologies come at the trade-off of decreasing gain and increasing noise figure by using several configuration settings. In wireless applications where different sets of specifications are not required, such as WiFi or Bluetooth, configurable-gain topologies are

not used. However, for large dynamic range wireline applications such as G.hn that require different sets of specifications, configurable topologies provide better linearity and are more robust to process variations and temperature since they do not depend on a very narrow range of biasing voltages. Also, input-attenuation based configurable-gain topologies such as resistive attenuation and capacitive attenuation can scale by adding more attenuation steps and thus providing higher linearity.

Table 3.1: High-Linearity Techniques Performance Comparison

Topology	**Derivative Superposition**	**Harmonic Termination**	**Noise/Distortion Cancellation**	**Post-Distortion**	**Configurable-Load**	**Pre-Attenuation**
Ref.	**[88]**	**[43]**	**[47]**	**[103]**	**[13]**	**[8]**
IIP3 (dBm)	10	-2.5	0	11.7	-9–6.8	-1.5–27
Voltage Gain (dB)	10	8.6[1]	15.6	11.7[1]	-6–15.1	-17–16
NF (dB)	5.7	1.9	3.5	3.6	2.3–13.9	4.3–35
Frequency (GHz)	0.47–0.86	2.2	0.2–5.2	1.5–8.1	0.47–0.77	0.47–0.87
Power (mW)	5.2	16.2	21	2.6	13.9	22
Supply Voltage (V)	1.8	1.8	1.2	1.3	1.2	1.8
Process	0.18μm	0.35μm	65nm	0.13μm	90nm	0.18μm
Differential	Yes	Yes	Yes	No	No	Yes
Inductorless	Yes	No	Yes	No	No	Yes

[1] s_{21}

4

RFPGA Prototype I: Single-Input Switchable Capacitive Attenuation

4.1 Introduction

This chapter presents the implementation of a 2-stage input-attenuation based radio-frequency programmable gain amplifier (RFPGA) providing 4 different gain settings. We propose the use of a new input-attenuation based topology consisting of a switchable capacitive attenuation circuit over the commonly-used multiple-stage non-switchable capacitive attenuation circuit. The chapter is divided in three sections: design, experimental results and summary.

The design section starts with the core concept of the switchable capacitive attenuation topology and then continues with the full circuit schematic of the topology. After introducing the core topology, the section provides further insight into the input impedance matching topologies used in the RFPGA (active feedback and parallel resistance), the second-stage amplifier and the sizing of the components in the capacitor ladder. The section ends by providing analytical expressions of the noise figure and

input impedance value at the highest-gain setting, where the active feedback input impedance matching is used.

The next section contains the experimental results of the manufactured 2-stage switchable capacitive attenuation RFPGA topology. The circuit has been manufactured using a 65 nm CMOS technology, packaged inside a QFN and solded on PCB. The chapter ends with a summary section providing an overview of the contents presented.

4.2 Design

This sections starts by introducing the concept of the switchable capacitive attenuation topology using basic blocks, without entering into transistor-level design, in order to provide a basic understanding of the topology and its advantages. Then, the schematic of the 2-stage RFPGA using switchable capacitive attenuation is presented, showing the transistor-level design.

The circuit topology subsection of the 2-stage RFPGA is followed by several subsections providing more detail on the two selectable input impedance matching topologies (active feedback and parallel resistance), the second-stage amplifier and the sizing of the components in the capacitive attenuation ladder.

The design section ends by providing analytical expressions of the noise figure and input impedance value at the highest-gain setting. The two subsections focus on the highest-gain setting since this setting is the only one using the active feedback input impedance matching topology, which uses a complex structure with several components that affect the noise performance and input impedance value of the amplifier.

4.2.1 Core Concept

A configurable capacitive attenuation topology is used at the input of the RFPGA to add attenuation to the input signal, thereby increasing the linearity of the circuit. The capacitive attenuation circuit uses linear components (capacitors) to attenuate the signal before it is amplified, as opposed to other topologies where gain is controlled at

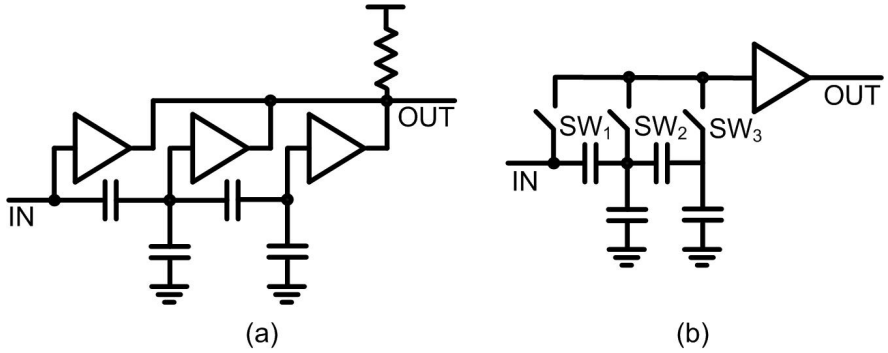

Figure 4.1: Capacitive attenuation topology, (a) Nonswitchable (b) Switchable

the amplification stage [33, 105, 106]. The linearity increase that can be achieved with the capacitive attenuation topology is higher because the signal is attenuated before entering any nonlinear amplifying device.

This chapter introduces a new switchable capacitive attenuation topology that requires only one input amplifying stage (Fig. 4.1b), as opposed to the non-switchable topologies presented in [5, 8] that require multiple input amplifying stages in parallel (Fig. 4.1a). The switches in the switchable capacitive attenuator are implemented using NMOS transistors. Because the contribution to distortion of an NMOS transistor operating as a switch is much higher than the contribution to distortion of the input amplifier, the switches have no influence on the overall linearity of the circuit. The negligible effect of the switches on the overall linearity has been verified through simulation.

By maintaining only one switch closed at any given time (SW_1-SW_3), there is only one low-impedance path available between the circuit input and the amplifying device, which results in the amplifier requiring only one transconductance stage as opposed to one transconductance stage per attenuation step in the non-switchable topology. Hence, the switchable capacitive attenuation topology greatly reduces the total input amplifier area. Such area savings may promote the integration of a complete SoC for multistandard transceivers. Furthermore, a switchable capacitive attenuation topology provides a higher bandwidth than a nonswitchable topology: by requiring only one amplifying stage, the total parasitic capacitance at the output node is independent

of the number of attenuation steps, whereas a nonswitchable topology requires one amplifying stage for each attenuation step, increasing the parasitic capacitance at the output node and thus reducing bandwidth for each attenuation step added to the circuit.

The most important drawback of the switchable capacitive attenuation topology is the increase in noise figure due to the on-resistance of the switches at the circuit input node. This effect, however, can be minimized by choosing an adequate switch size. A larger switch width lowers the on-resistance, thereby reducing noise but slightly decreasing bandwidth due to the increase in input parasitic capacitance. This enhanced parasitic capacitance can be considered part of the capacitive attenuation ladder, reducing the value of the parallel passive capacitances as the switch width (and its parasitic capacitance) increases. It has been verified through simulation that the effect of the nonlinear parasitic capacitances of the switches is negligible compared to the other nonlinearities generated by the circuit.

4.2.2 Circuit Topology

The schematic of the proposed wideband fully differential RFPGA is shown in Fig. 4.2 (biasings omitted). This RFPGA is composed of two stages. The first stage (LNA1) is a configurable tailed-pair LNA with switchable capacitive attenuation. The second stage (LNA2) is a conventional long-tailed pair amplifier with active loads and common-mode feedback (CMFB). The objective of this topology is to obtain a high-dynamic-range RFPGA using three methods of configuration: the new switchable capacitive attenuation circuit, selectable impedance matching topology, and bypassing of LNA2.

The first stage is designed using thick-oxide 0.2 μm minimum channel length transistors so that the input devices can handle very large input amplitudes (0+ dBm) without compromising their reliability. Since the input power level can change at any time from minimum to maximum[1] all the devices in LNA1 must use thick-oxide transis-

[1]The transmitter adjusts its frequency, bandwidth, bit loading and signal power depending on the channel conditions and receiver location to maintain a minimum specified transmission bit-rate. When the channel conditions change (e.g. due to interferers) or a new receiver enter the network, the

tors to ensure the reliability of the whole circuit. If the circuit is configured at high-gain setting and the transmitter changes at a given moment from minimum power to maximum power due to network changes, all the transistors in LNA1 will be exposed to a large power signal for a certain amount of time and, therefore, their reliability can be compromised[2]. The supply voltage in LNA1 is 1.8V. Having a higher voltage supply also allows a larger voltage swing at the output, thereby providing better linearity. The signal level at the input of LNA2 is limited by LNA1, which means thick-oxide transistors are not required. Thus, thin-oxide transistors are used, which allow for lower area, lower power consumption, and a lower noise figure. The supply voltage in LNA2 is 1.2V.

By using these configuration methods, the RFPGA achieves a large dynamic range capable of handling large-amplitude input signals (which require high linearity, as distortion dominates over noise) as well as small-amplitude input signals (which require high gain and low-noise figure, since noise dominates over distortion).

The circuit has two output ports (one from LNA1 and one from LNA2) for measurement purposes. This methodology was followed only for testing purposes in order to measure the LNA1 performance standalone. In a practical application, where the RFPGA is followed by a mixer, the bypass of LNA2 can be implemented by using switches connecting the output of LNA1 to the output of LNA2 and the mixer input as shown in Fig. 4.3. This solution is used in both DTV tuners [107] and wireless receivers [108] to accommodate the high input power requirements and is used in the design of the front-end prototype presented in a later chapter.

transmission re-adjusts itself to maintain the specified bit-rate given the new conditions.

[2]At the time of the circuit fabrication, the G.hn specification was still in early design stages and it was decided that thick-oxide transistors were required given the maximum input power values at that time. Later, when the specification received final approval, it was decided that the thin-oxide transistors could handle the maximum input power levels without compromising reliability. Thus, the second RFPGA prototype was designed only with thin-oxide transistors

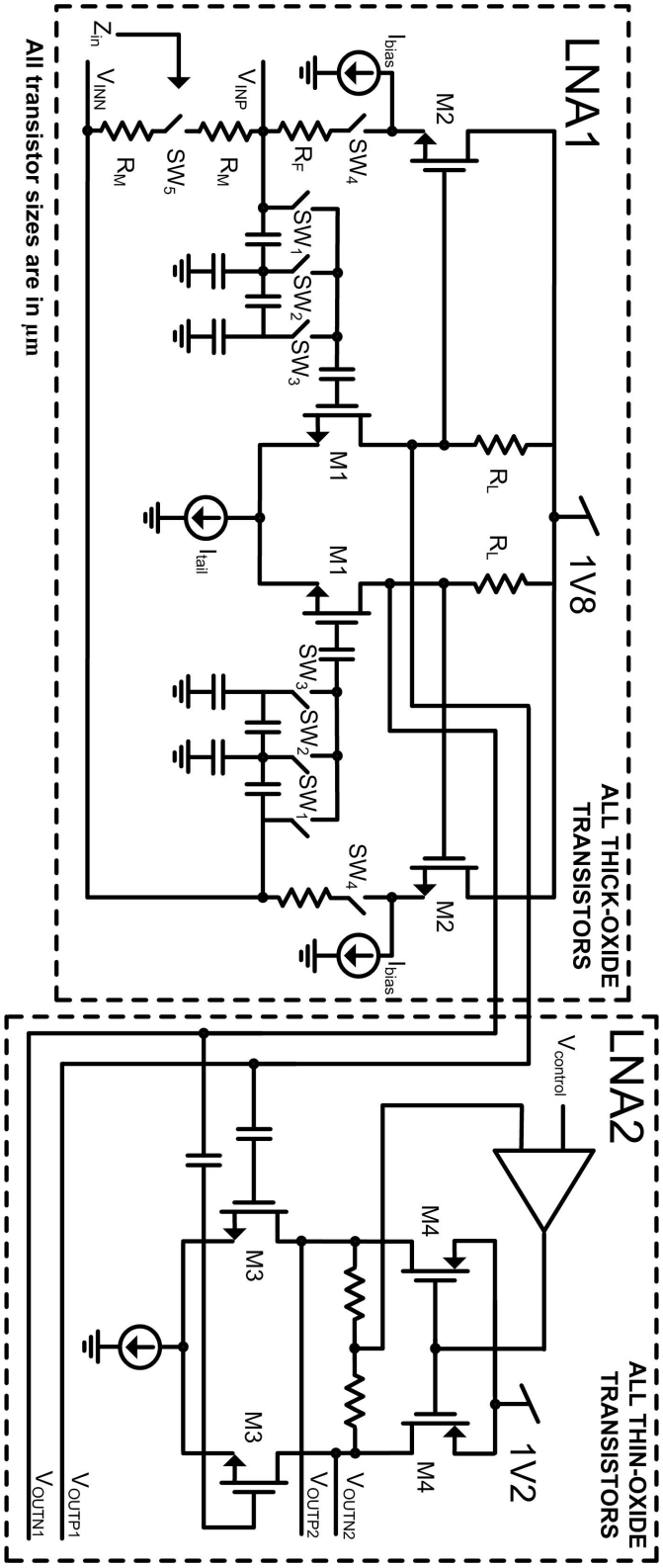

Figure 4.2: Proposed configurable wideband RFPGA schematic.

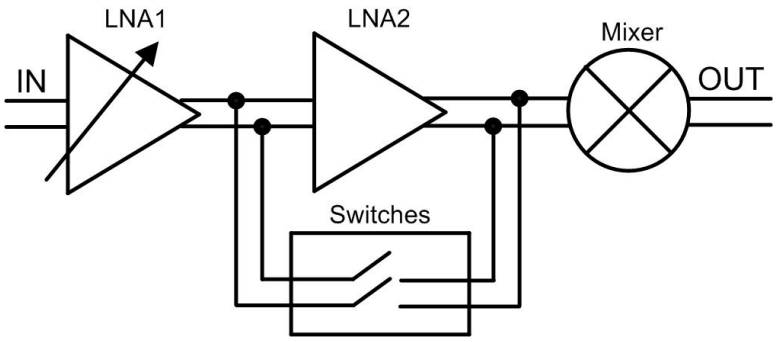

Figure 4.3: Proposed configuration of RFPGA prototype I in a front-end implementation.

4.2.3 Selectable Input Impedance Matching

The input impedance matching, which is performed using two different methods, provides different performance in terms of noise figure and linearity. The two methods are *active feedback* and *parallel resistor*.

The active feedback input impedance matching topology is composed of M_2, SW_4, R_F, and I_{bias}. Because this topology has a small contribution to the overall noise figure of LNA1, it is suitable for input impedance matching in the high-gain modes of the RFPGA, where the circuit is expected to handle small-amplitude input signals, and the SNDR is dominated by the circuit noise figure. This topology, however, has two disadvantages that make it unsuitable for input impedance matching when handling large-amplitude input signals. The first one is related to the linearity issues resulting from the use of nonlinear feedback. It can be shown [51] that a large part of the nonlinearities generated by this circuit are due to the presence of feedback transistor M_2. Nonlinearities generated by the active feedback can be reduced by increasing R_F, although this in turn increases the noise figure of the RFPGA. The reader may note that to maintain a single input impedance matching topology, this issue could be solved by using an array of selectable resistors in place of R_F and selecting higher resistance values as higher linearity is required. This solution, however, has not been implemented because of the second disadvantage of the active feedback topology, which is explained as follows. The input impedance of the RFPGA when using the active feedback circuit

is given by the following expression:

$$Z_{in} = 2\frac{1 + g_{m2}R_F}{g_{m2}\left(1 + A_v\right)} \tag{4.1}$$

In this equation, A_v is absolute value of the open-loop voltage gain of LNA1. As can be seen, the input impedance value has an inverse dependence on the gain of the circuit. When input attenuation is added using the switchable capacitive attenuation circuit to increase linearity, the open-loop gain of the LNA1 (A_v) is lowered, requiring a lower R_F to maintain good impedance matching (generally accepted as an s_{11} below -10 dB), which results in a decrease of linearity. Thus, the active feedback topology is not suited for input impedance matching in low-gain modes, and a second topology (parallel resistor at the input using R_M) intended to handle large-amplitude input signals is added to the circuit. Because the input impedance matching in such low-gain modes is performed using a passive component, linearity is not affected. The only drawback of the parallel resistance method is a larger noise figure, compared to using the active feedback method. The parallel resistor method, however, is used only in low-gain modes to handle large-amplitude input signals, which allows a higher noise figure for a constant output SNDR.

In the designed prototype, input impedance matching is performed with active feedback at the highest-gain setting and with parallel resistance at the other gain settings.

4.2.4 Second Stage and By-Pass

The second stage of the RFPGA is a tailed-pair amplifier using active loads and a CMFB to maintain a constant DC level at the circuit output. The objective of the second amplifying stage is to provide additional gain with a low-noise figure to reduce the effect of the following stages on the overall noise figure of the receiver. This stage is used only in the highest gain configuration mode of the RFPGA, intended for handling small-amplitude input signals that require high gain and a low-noise figure but allow a low linearity. On the other gain modes of the RFPGA, the LNA2 stage is powered

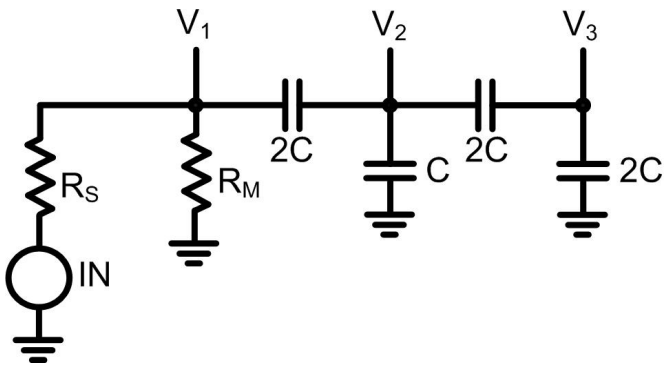

Figure 4.4: Capacitor ladder using a C-2C structure.

down and bypassed, connecting the output of the first RFPGA stage (LNA1) directly to the input of the following circuit.

4.2.5 Switchable Capacitive Attenuation Capacitor Sizing

The capacitors in the capacitive ladder can be sized to obtain different gain steps, the most usual being a C-2C structure [5, 6, 7, 8] as shown in Fig. 4.4. This structure ideally provides 6 dB of attenuation for each step, resulting in an attenuation of 0 dB, 6 dB and 12 dB at the V_1, V_2 and V_3 nodes respectively.

In a system using only one input tone as the signal of interest, the total distortion is mainly dominated by the third-order intermodulation. In this situation, a constant attenuation step with an input power increase equal to the attenuation step (e.g. 12 dB input attenuation and a 12 dB increase in input power) results in the same signal to noise plus distortion ratio (SNDR).

However, in wideband multi-carrier systems the total distortion is also largely affected by the phase of each tone and the peak-to-average ratio (PAR) of the input signal, and can also be affected to a lower degree by intermodulations other than the third-order. Taking these behavior into account, different circuit topologies (such as using active feedback or parallel resistance for input impedance matching) may result in different SNDR for the same input power and voltage gain. Therefore, the design of the gain steps in the capacitor ladder is done in order to comply with certain SNDR

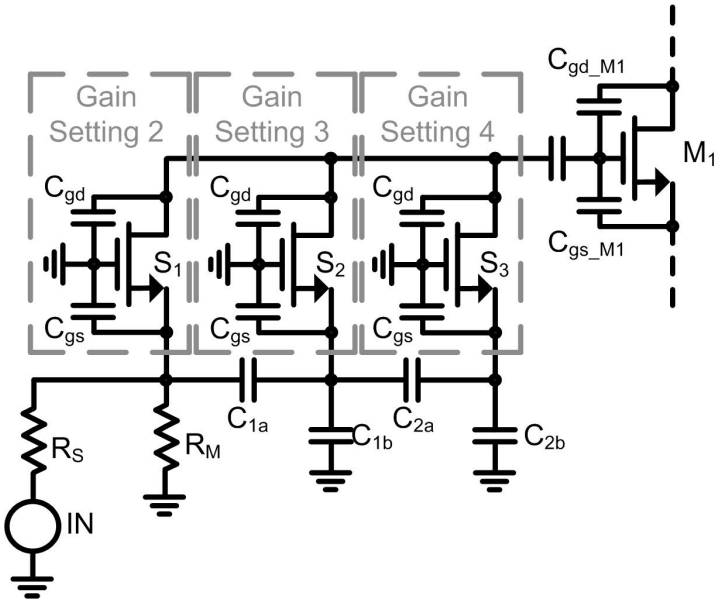

Figure 4.5: Capacitor ladder including the parasitic capacitances of the switches.

specifications which may not result in a constant attenuation step.

The capacitor ladder used in the amplifier provides 3 different attenuation values, one of them being equal to 0 dB (at the V_1 node). Therefore there are 4 available degrees of freedom (the values of the capacitances) to solve a system of 2 equations, therefore 2 capacitor values are fixed and then the values of the other 2 capacitors are calculated. The criteria used to fix the 2 capacitor values is bandwidth. The upper boundary of the capacitances is established by the circuit bandwidth, since larger capacitances decrease the bandwidth. The lower boundary of the capacitances depends on the parasitic capacitances of other components when the practical implementation of the circuit is taken into account.

In a practical implementation there are parasitic capacitances which modify the capacitance structure of the ladder as shown in Fig. 4.5, therefore changing the attenuation at each step. In a non-switchable topology the parasitic capacitances are mainly due to the input amplifying transistor ($C_{gs_{M1}}$ and $C_{gd_{M1}}$), whereas the the switchable topology presented in this chapter also adds the parasitic capacitances due to the switches (C_{gs} and C_{gd}).

By considering that the parasitic capacitances of the switches are connected to an AC ground, the capacitive ladder including parasitic capacitances can be drawn as shown in Fig. 4.6 for each gain setting. The schematics distinguish between ON and OFF capacitances since the NMOS transistors used as switches have different values of parasitic capacitances depending on whether they are in linear region (ON) or cut-off region (OFF). The capacitance C_{M1} is used to identify the parasitic capacitance due to M_1 and during the design stage has been approximated as the sum of $C_{gs_{M1}}$ and $C_{gd_{M1}}$.

These schematics including the parasitic capacitances are used to calculate the required values of the ladder capacitors in order to obtain the required values of gain. As has been previously mentioned, 2 capacitor values are fixed since there are 2 equations and 4 degrees of freedom (4 capacitor values). As the value of the fixed capacitors increases, the circuit bandwidth decreases. However, by decreasing the value of the fixed capacitors it may become impossible to solve the equations as the parasitic capacitances dominate and the range of achievable gains is very narrow. Also, the gain values become more susceptible to process and temperature variations. The final values of the ladder capacitors are obtained after iterating between the analytical model to obtain coarse values and simulations to fine tune the circuit performance.

4.2.6 Optimization of the Active Feedback Impedance Matching

This section analyzes the noise performance and impedance value of the active feedback topology. The noise analysis is performed by first obtaining analytical expressions of the noise figure of the amplifier and then by showing how it can be optimized. The impedance value analysis is performed considering high frequency effects (by adding parasitic capacitances), obtaining an analytical expression of the input impedance value and analyzing how it is affected by different values of total input and output capacitance.

Since the active feedback input impedance matching topology is used only at the highest gain setting of LNA1, where the SNDR is dominated by noise, it is important

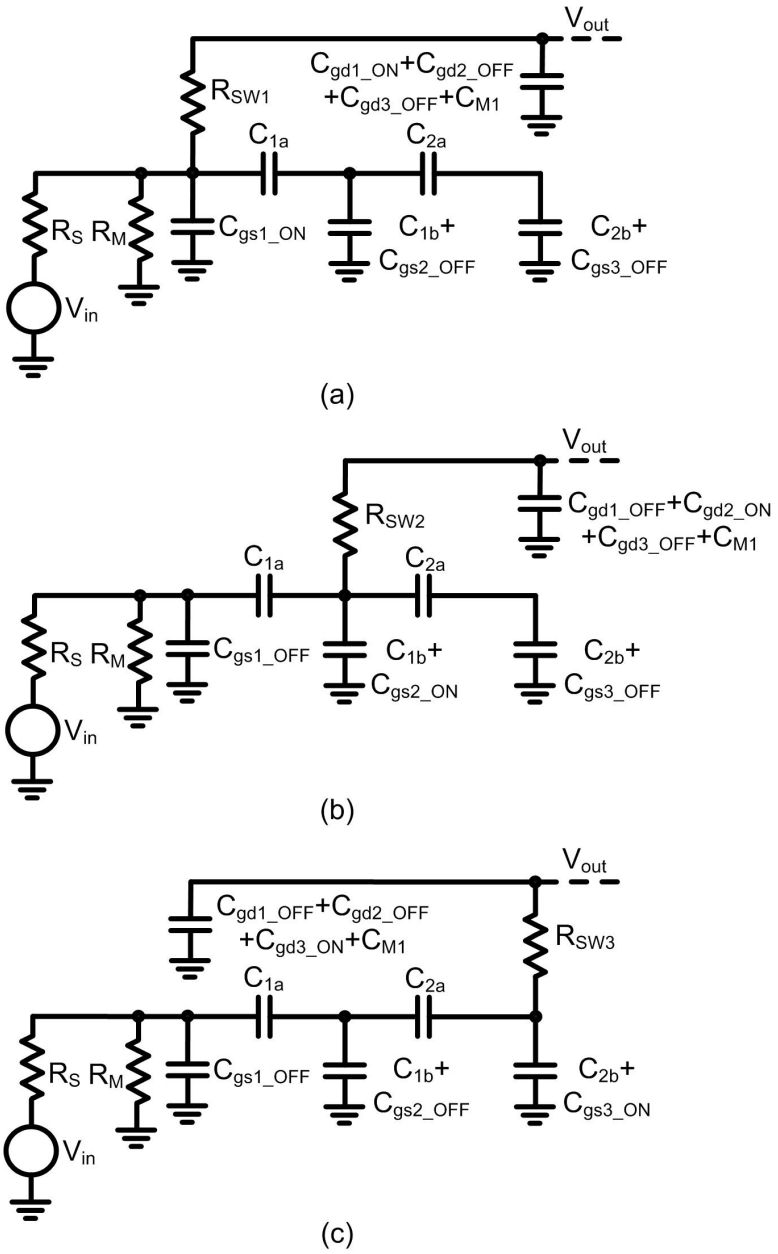

Figure 4.6: Circuit model of the capacitor ladder including switch parasitic capacitances and channel resistance for (a) Gain setting 2 (b) Gain setting 3 (c) Gain Setting 4.

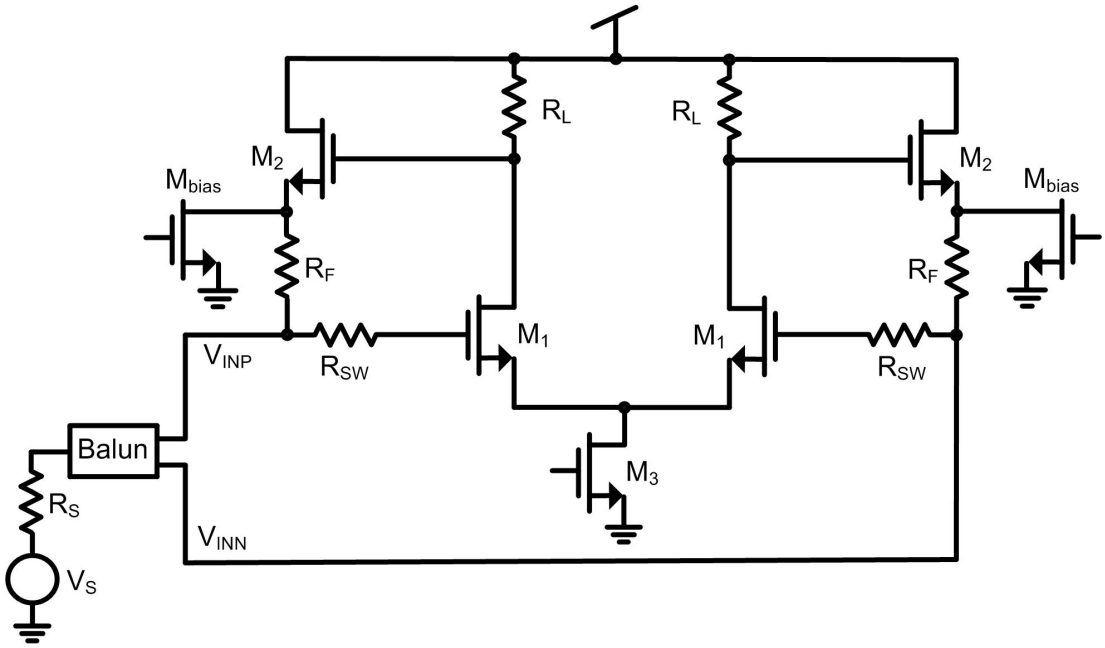

Figure 4.7: LNA1 simplified schematic used for noise optimization calculations.

to optimize the component parameters to obtain the minimum possible noise figure while complying with impedance matching requirements ($s_{11} < -10\ dB$).

4.2.6.1 Noise Optimization

This subsection provides analytical expressions of the noise factor generated by the amplifier at the highest gain setting where the active feedback is used to provide input impedance matching. We obtain the analytical expressions by using a small-signal model of the transistors and then we analyze the dependences of each term, which shows that there exists an optimal value of noise factor.

The equations are calculated using the simplified schematic shown in Fig. 4.7. The simplified schematic does not include the switchable capacitive attenuation ladder and the parallel input impedance matching since both circuits are not used at the highest gain mode. The resistance R_{SW} is the channel resistance due to SW_1.

The noise factor of the amplifier can be expressed as a sum of the noise factor generated by each component [51]:

$$F = F_{R_S} + F_{M_1} + F_{R_F} + F_{SW_1} + F_{M_2} + F_{R_L} + F_{M_{bias}} \tag{4.2}$$

Without taking high frequency behavior due to capacitances into account (C_{in} and C_{out} are negligible) and using simple network analysis, the noise factor of the amplifier can be expressed as follows:

$$\begin{aligned} F = 1 &+ \frac{2\gamma_1 R_X}{g_{m1}} \left[\frac{1}{R_X} + \frac{g_{m2}}{g_{m2}R_F + 1}\right]^2 + 2R_F R_X \left[\frac{g_{m2}}{g_{m2}R_F + 1}\right]^2 + \\ &+ 2R_{SW} R_X \left[\frac{1}{R_X} + \frac{g_{m2}}{g_{m2}R_F + 1}\right]^2 + \frac{2\gamma_2 g_{m2} R_X}{(1 + g_{m2}R_F)^2} + \\ &+ \frac{2R_X}{g_{m1}^2 R_L} \left[\frac{1}{R_X} + \frac{g_{m2}}{g_{m2}R_F + 1}\right]^2 + \frac{2\gamma_{bias} g_{mbias} R_X}{(1 + g_{m2}R_F)^2} \end{aligned} \tag{4.3}$$

In this equation, γ is thermal excess noise factor of each transistor, R_{SW_1} is the switch on-resistance, R_X is half the source resistance, R_L is the load resistance, g_m is the transconductance of each transistor and R_F is the feedback resistance,

Re-writing Eq. 4.1, we can express the required g_{m2} (to obtain input impedance matching) in terms of R_X, R_F and A_v:

$$g_{m2} = \frac{1}{R_X (1 + A_v) - R_F} \tag{4.4}$$

Where A_v is voltage gain of the amplifier and is defined as:

$$A_v = g_{m1} R_L \tag{4.5}$$

When the matching criteria of Eq. 4.4 and the voltage gain definition of Eq. 4.5 are substituted into Eq. 4.3, the noise factor of the amplifier develops into the following expression:

$$F = 1 + \frac{2\gamma_1}{g_{m1}R_X}\left[\frac{2+A_v}{1+A_v}\right]^2 + \frac{2R_F}{R_X\left(1+A_v\right)^2} + \\ + \frac{2R_{SW}}{R_X}\left[\frac{2+A_v}{1+A_v}\right]^2 + \frac{2\gamma_2}{1+A_v}\left[1 - \frac{R_F}{R_X\left(1+A_v\right)}\right] + \\ + \frac{2}{g_{m1}R_X A_V}\left[\frac{2+A_v}{1+A_v}\right]^2 + 2\gamma_{bias}g_{mbias}R_X\left[1 - \frac{R_F}{R_X\left(1+A_v\right)}\right]^2 \tag{4.6}$$

By using the approximation of $A_v \gg 1$ and substituting R_X for $R_S/2$, the resulting noise factor of the amplifier is:

$$F \approx 1 + \frac{4\gamma_1}{g_{m1}R_S} + \frac{4R_F}{R_S A_v^2} + \frac{4R_{SW}}{R_S} + \frac{2\gamma_2}{A_v}\left[1 - \frac{2R_F}{R_S A_v}\right] + \\ + \frac{4}{g_{m1}R_S A_V} + \gamma_{bias}g_{mbias}R_S\left[1 - \frac{2R_F}{R_S A_v}\right]^2 \tag{4.7}$$

Component	**Noise Factor**	**To decrease noise factor**
R_S	1	—
M_1	$\frac{4\gamma_1}{g_{m1}R_S}$	Increase g_{m1}
R_F	$\frac{4R_F}{R_S A_v^2}$	Decrease R_F
SW_1	$\frac{4R_{SW}}{R_S}$	Decrease R_{SW}
M_2	$\frac{2\gamma_2}{A_v}\left[1 - \frac{2R_F}{R_S A_v}\right]$	Increase R_F
R_L	$\frac{4}{g_{m1}R_S A_V}$	Increase g_{m1}
M_{bias}	$\gamma_{bias}g_{mbias}R_S\left[1 - \frac{2R_F}{R_S A_v}\right]^2$	Increase R_F

Table 4.1: Noise factor dependencies of each component of LNA1 at highest gain setting.

Table 4.1 uses the results obtained in Eq. 4.7 to present the parameters that need to be modified to decrease the noise factor of each component. It is taken into account that A_v and R_S are fixed at system level and therefore cannot be modified to decrease

the noise factor. The following conclusions can be extracted:

- By increasing the transconductance g_{m1}, the noise generated by M_1 and R_L decreases. To increase g_{m1}, either M_1 width or channel current can be increased. The limit of the noise optimization is set by the bandwidth and power consumption requirements, usually set at system level.

- By decreasing the channel resistance of the input switch, the noise generated by the switch decreases. To decrease the resistance value, the width of SW_1 should be increased. Since a higher width increases input parasitic capacitance, the limit of the noise optimization is set by the bandwidth requirements.

- By decreasing the resistance value of R_F, the noise generated by R_F decreases. However, by decreasing the value of R_F, the noise generated by M_2 and M_{bias} increases. Therefore, there exists a resistance value of R_F that provides an optimal value of noise factor for the group composed by R_F, M_2 and M_{bias}.

The noise factor generated by R_F, M_2 and M_{bias} is analyzed in Fig. 4.8 using the expressions presented in Table 4.1. Although as has been previously commented A_v and R_S are usually set at system level, the graphical results are provided for different values of A_v and R_S to show their effect on the amplifier performance.

Fig. 4.8a shows the combined noise factor generated by R_F, M_2 and M_{bias} as a function of the resistance value of R_F for 3 different values of voltage gain. As can be seen, there exists a value of R_F that provides an optimal (minimum) value of noise factor. As voltage gain increases, the value of R_F that provides the optimal noise factor increases and the optimal noise factor value decreases. Fig. 4.8b shows the optimal noise factor value as a function of voltage gain and for 4 different values of source impedance. The results show that the optimal noise factor has a small dependence on source impedance and a much larger dependence on voltage gain. The values of R_F and g_{M_2} (transconductance of M_2) that provide the optimal noise figure of Fig. 4.8b are shown in Fig. 4.8c and Fig. 4.8d respectively.

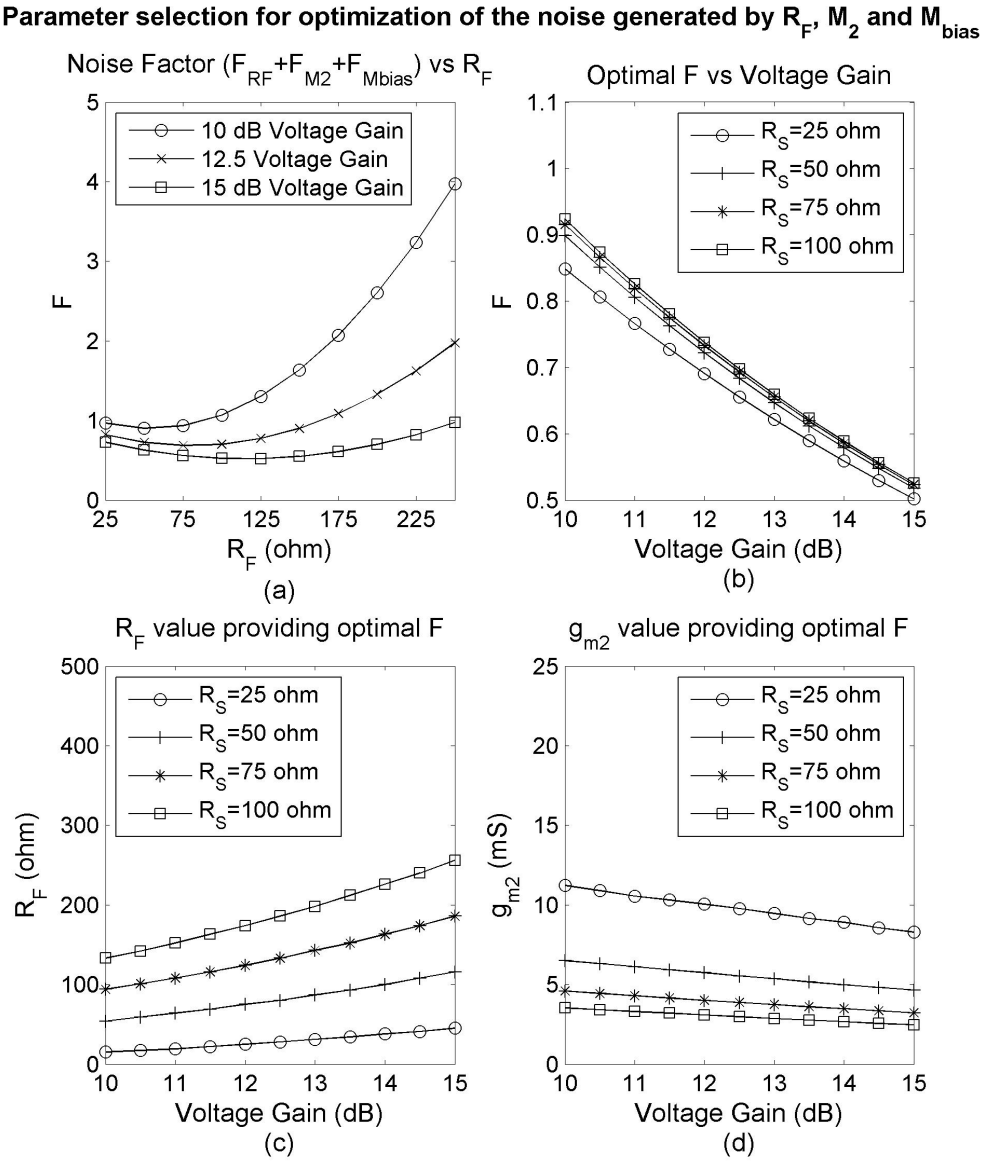

Figure 4.8: Optimization of the noise generated by R_F, M_2 and M_{bias}; (a) Noise factor dependency on R_F and A_v (b) Optimal noise factor for different values of A_v and R_S (c) R_F resistance value that provides optimal noise factor for different values of A_v and R_S (d) M_2 transconductance value that provides optimal noise factor for different values of A_v and R_S.

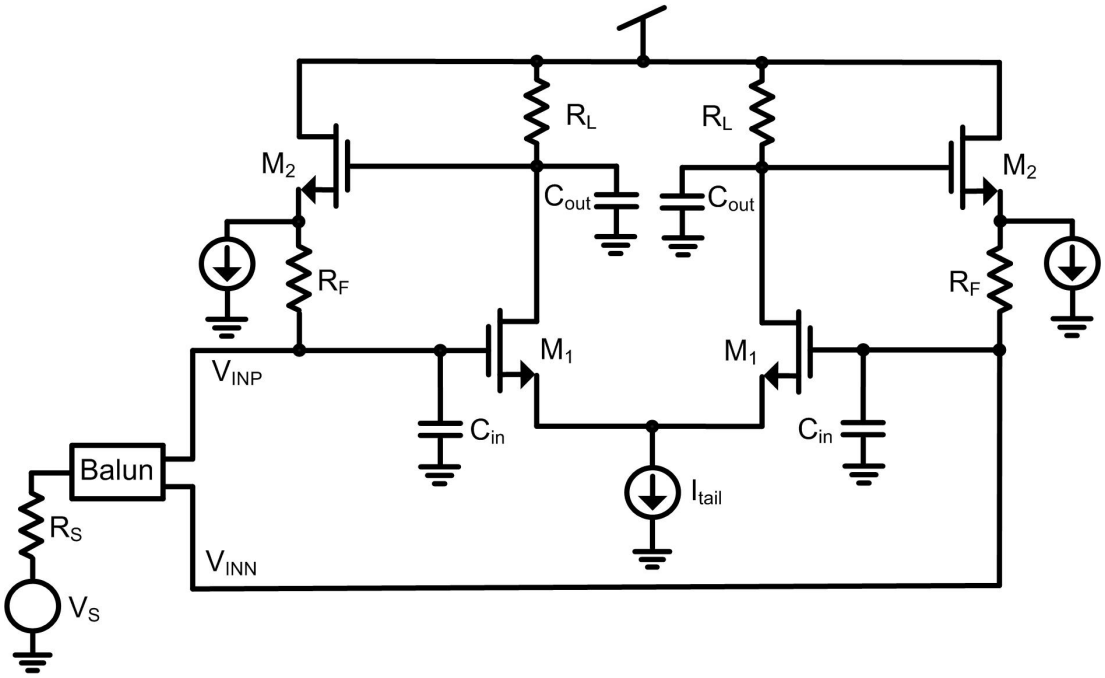

Figure 4.9: LNA1 simplified schematic used for input impedance optimization calculations.

The analytical process presented in this section for noise factor optimization has been used in the design process of the highest gain setting of the RFPGA. The presented noise equations have been used to obtain the approximate values of R_F and g_{M_2} that provide optimal noise factor and then fine tuning through simulation has been performed to choose the final values.

4.2.6.2 High Frequency Behavior

This subsection provides analytical expressions of the input impedance value of the active feedback including parasitic capacitances. We obtain the analytical expression by using a small-signal model of the transistors and using two capacitances, one at the input and one at the output, which represent the total parasitic capacitance at the input and output nodes. The resulting expression of input impedance shows that there is a peaking effect which depends on the value of the capacitances and that can be used to extend the bandwidth of the input impedance matching.

The equations in this section are calculated using the simplified schematic shown in Fig. 4.9. The simplified schematic does not include the switchable capacitive attenuation ladder and the parallel input impedance matching since both circuits are not used at the highest gain mode. The series resistance of the activated switch is neither included in the schematic as it has a negligible influence on the value of input impedance.

To analyze the high frequency behavior it is necessary to include parasitic capacitances, especially at the input and output nodes since they present the highest capacitance loading. The capacitance at the input node is composed by the parasitic capacitances of the switches and the passive capacitors of the capacitance ladder (Fig. 4.6a), whereas the capacitance at the output node is composed by the parasitic capacitances of the amplifying transistors (M_1), the feedback transistors (M_2) and the input capacitance from the next stage. Without loss of generality, the following analysis uses two capacitances, C_{in} and C_{out}, each one representing the total equivalent capacitance at the input and output nodes respectively.

In a general case for amplifiers, increasing the total output capacitance (C_{out}) results in a decrease of the bandwidth of the amplifier, as the bandwidth depends on a low-pass RC filtering effect, where C is the total capacitance seen at the output node. However, due to the behavior of the active feedback input impedance matching at high frequencies, it is possible to increase C_{out} (which is equivalent to allowing a higher input capacitance from the next stage, easing its design) without decreasing bandwidth and improving s_{11}. This effect is explained as follows.

The input structure of a front-end is as shown in Fig. 4.10, including the source resistance and the input amplifier. The voltage gain of an amplifier is given as the quotient between the voltages at the output and input nodes:

$$G_{V_{amp}}(dB) = 20log\left(\frac{V_{out}}{V_{in}}\right) \tag{4.8}$$

However, the input voltage of the amplifier depends on the voltage gain between the source impedance and the input impedance of the amplifier, as given by:

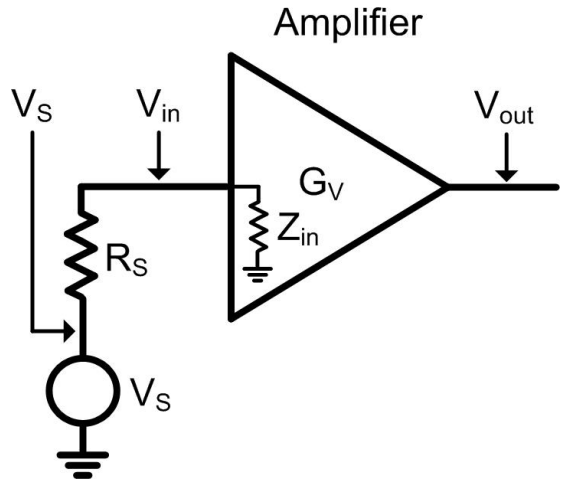

Figure 4.10: Input structure of a front-end.

$$G_{V_{source}}(dB) = 20log\left(\frac{V_{in}}{V_S}\right) = 20log\left(\frac{Z_{in}}{R_S + Z_{in}}\right) \tag{4.9}$$

If the amplifier input impendance (Z_{in}) equals the source resistance (R_S), the impedance matching is ideal (s_{11} equals minus infinite when expressed in dB) and the voltage gain between source impedance and input impedance ($G_{V_{source}}$) is $-6\ dB$. However, in broadband circuits it is generally considered as good input impedance matching an s_{11} below $-10\ dB$. An s_{11} below $-10\ dB$ for an R_S of 50 Ω results in a range of $|Z_{in}|$ values between 26 Ω and 96 Ω (considering no imaginary part). The two $|Z_{in}|$ boundaries result in a respective $G_{V_{source}}$ between $-9.3\ dB$ and $-3.6\ dB$.

In practical broadband applications, Z_{in} is not constant over frequency. Generally, s_{11} is better at the low frequency range than at the high frequency range since the input impedance is designed to be equal to that of the source resistance without including capacitances, providing a very good s_{11} at low frequencies where capacitances have a negligible effect. However, as frequency increases, the total input capacitance starts to affect performance by decreasing the absolute value of Z_{in}, which results in worse s_{11} and decreased $G_{V_{source}}$.

The total voltage gain of the whole structure composed of source resistance and input amplifier (Fig. 4.10) can be defined as:

$$G_{V_{total}}(dB) = G_{V_{source}}(dB) + G_{V_{amp}}(dB) \tag{4.10}$$

Given the previous equation, the bandwidth of the whole structure in a general amplifier case is limited by both the amplifier gain (which decreases as frequency increases due to the output capacitance) and the source gain (which decreases as frequency increases due to the input capacitance).

Now we calculate the input impedance of the active feedback topology as a function of frequency including the total input (C_{in}) and output (C_{out}) capacitances, which is given by:

$$Z_{in}(\omega) = 2\frac{(1 + g_{m2}R_F)(1 + j\omega C_{out}R_L)}{-\omega^2 C_{out}C_{in}R_L(1 + g_{m2}R_F) + j\omega(C_{in} + C_{out}g_{m2}R_L + C_{in}g_{m2}R_F) + g_{m2}(1 + A_v)} \tag{4.11}$$

Due to the complexity of the resulting poles and zeros of the previous equation, graphical results are provided showing the high frequency behavior of the active feedback input impedance matching for certain design parameters. The calculations are made using an open-loop voltage gain (A_v) of 12.5 dB, a source resistance (R_S) of 50 Ω, an input capacitance (C_{in}) of 400 fF, and the R_F and g_{m2} values are calculated to obtain optimal noise factor as defined in the previous section.

For different values of C_{out}, Fig. 4.11a shows the real part of input impedance, Fig. 4.11b the imaginary part of input impedance, Fig. 4.11c the $|s_{11}|$ in dB and Fig. 4.11d the absolute value of input impedance. The figure shows that as C_{out} increases, the absolute value of input impedance gradually shows a peaking at high frequencies. As a result, the s_{11} is better for higher values of C_{out}, therefore a higher output capacitance (which is basically composed of the capacitances added by M_1, M_2 and the next stage input capacitance) can be used to improve the input impedance matching.

Fig. 4.12a shows the source voltage gain ($G_{V_{source}}$) for different values of C_{out}. For a C_{out} value of 150 fF, the input impedance shows no peaking and, as previously explained, $G_{V_{source}}$ decreases as frequency increases. However, for C_{out} values of 250 fF

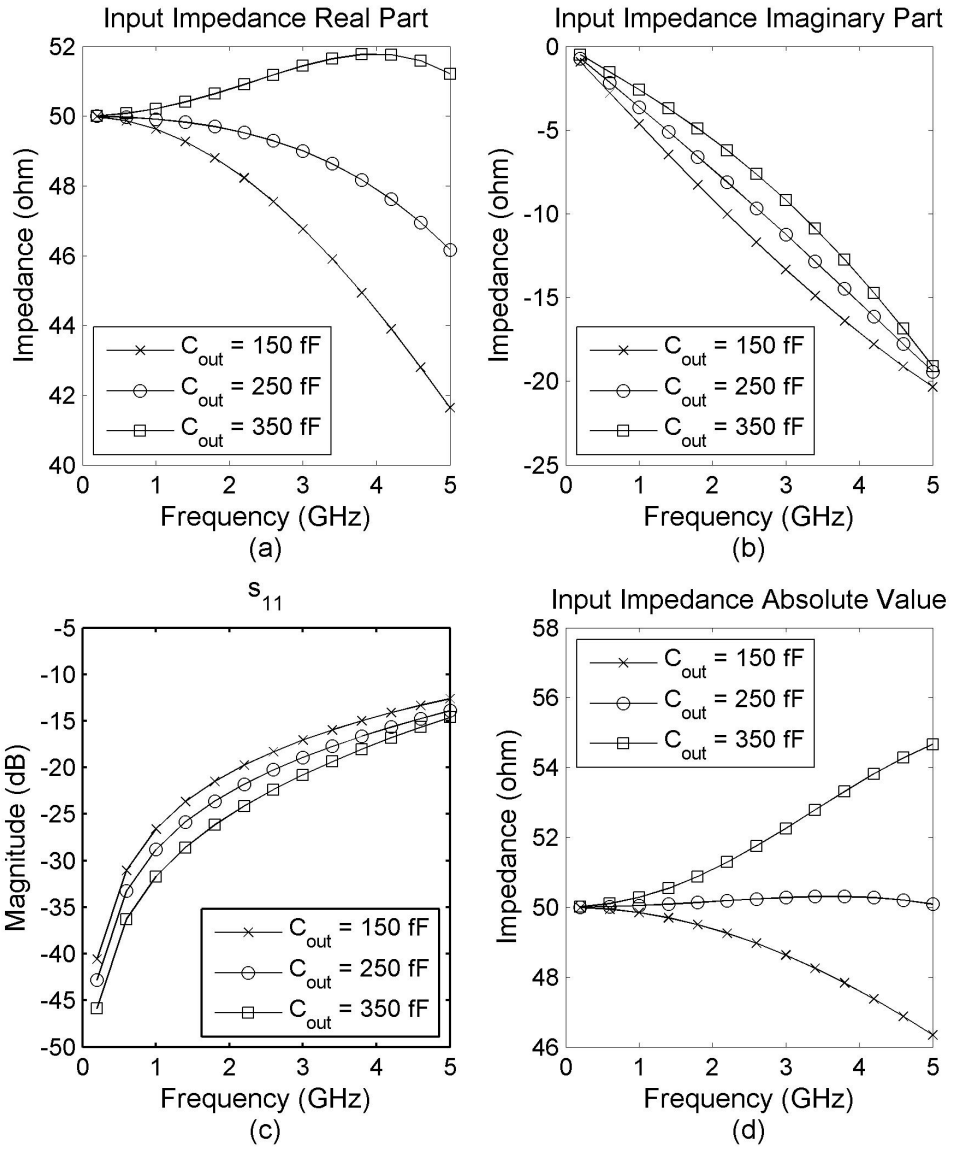

Figure 4.11: High frequency behavior of the active feedback input impedance matching topology for different values of C_{out}: (a) Real part of the input impedance (b) Imaginary part of the input impedance (c) $|s_{11}|$ in dB (d) Absolute value of the input impedance.

and 350 fF, the input impedance peaking at high frequencies results in a source voltage gain increase over frequency. Thus, although a higher value of C_{out} decreases the bandwidth of the amplifier gain, it is offset by the bandwidth increase of the source gain. Fig. 4.12b shows the voltage gain of the whole structure ($G_{V_{total}}$), which is practically the same for the 3 values of C_{out}. Therefore, the active feedback input impedance matching can be designed in order to allow a higher output capacitance while providing better s_{11} and without decreasing the whole circuit bandwidth. This effect has been used in the design of the RFPGA.

4.3 Experimental Results

The proposed fully differential RFPGA is fabricated in a double-oxide 65 nm/0.2 μm minimum channel length CMOS technology (operating supply voltages of 1.2V and 1.8V respectively) and achieves a bandwidth from 500 MHz to 2.5 GHz. The die microphotograph is shown in Fig. 4.14. The circuit is packaged inside a 36-QFN and measured on the PCB with the setup shown in Fig. 4.13. The SMD external baluns are used for single-ended-to-differential conversion, and an on-chip buffer at the output of the RFPGA is used to drive the low-impedance load of the measuring equipment. Both the baluns and on-chip buffer have been de-embedded from the presented results. The PCB tracks have also been de-embedded using SOLT (short-open-load-through) calibration. The first stage, which uses thick-oxide 0.2 μm minimum channel length transistors, occupies an area of 0.028 mm^2 and the second stage, which uses thin-oxide 65 nm minimum channel length transistors, occupies an area of 0.013 mm^2, for a total area of 0.041 mm^2, which includes DC decoupling capacitors. The power consumption varies from 28.8 mW (using only LNA1 with simple resistive termination) to 39.5 mW (using both LNA1 and LNA2 and active feedback impedance matching).

A summary of the RFPGA configuration modes and measurement results is presented in Table 4.2. The RFPGA achieves a total voltage gain range of 30.6 dB, with a maximum gain of 19.9 dB and a minimum gain of -10.7 dB, as shown in Fig. 4.15.

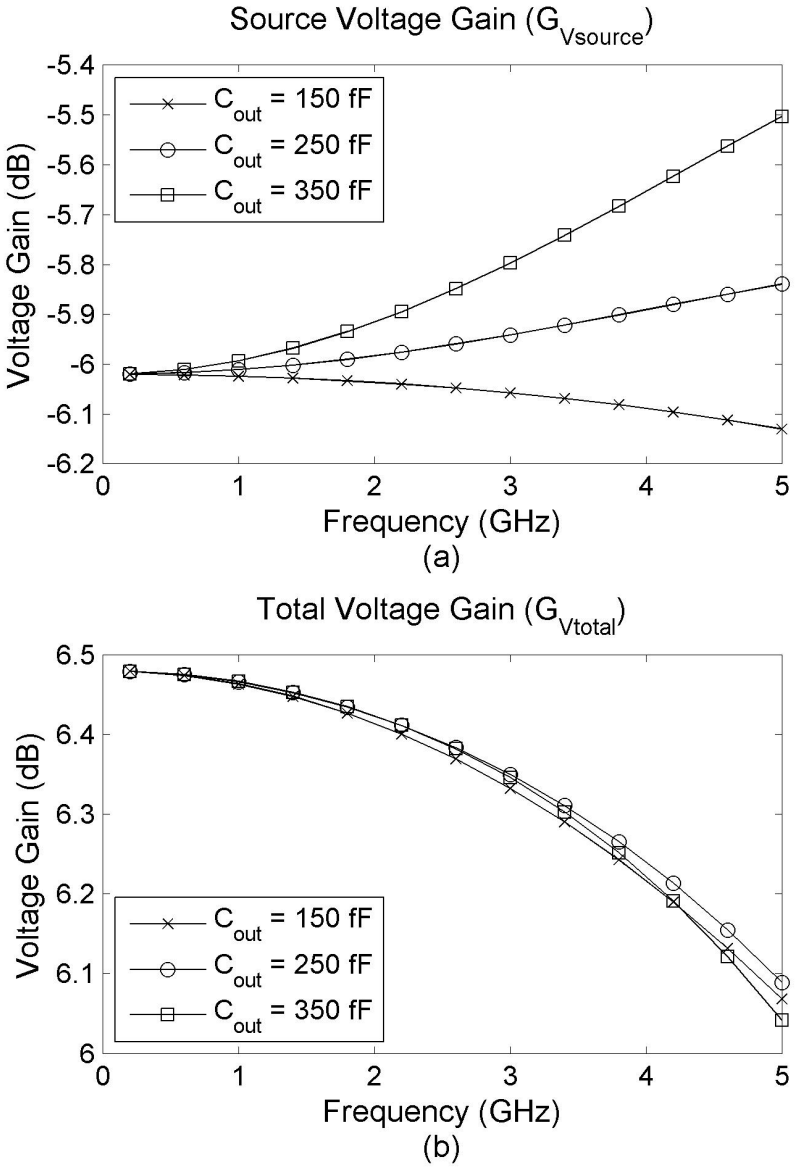

Figure 4.12: Voltage gain using the active feedback input impedance matching topology for different values of output capacitance (a) Source voltage gain (b) Total voltage gain (source plus amplifier).

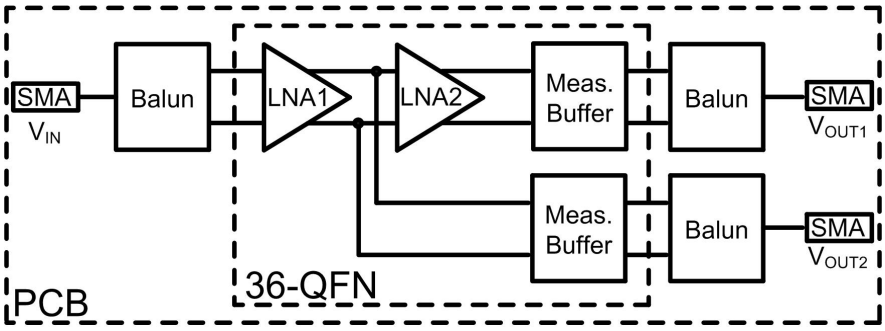

Figure 4.13: PCB measurement setup.

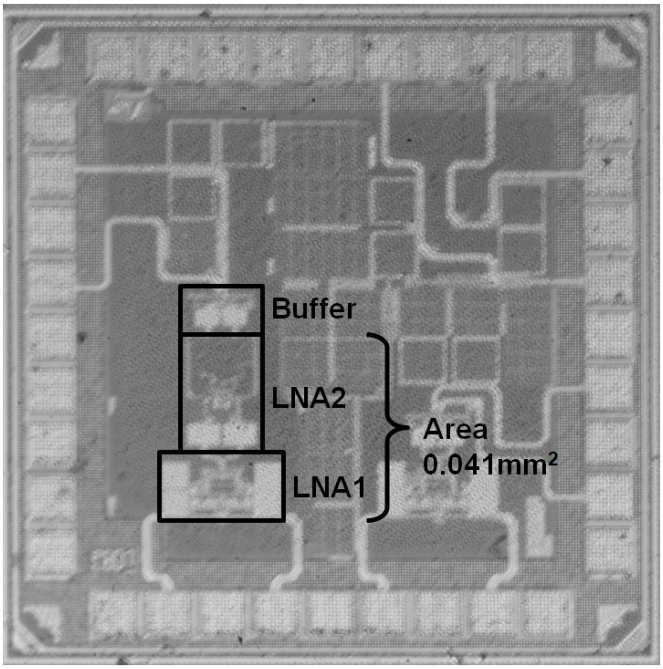

Figure 4.14: Microphotograph of the RFPGA.

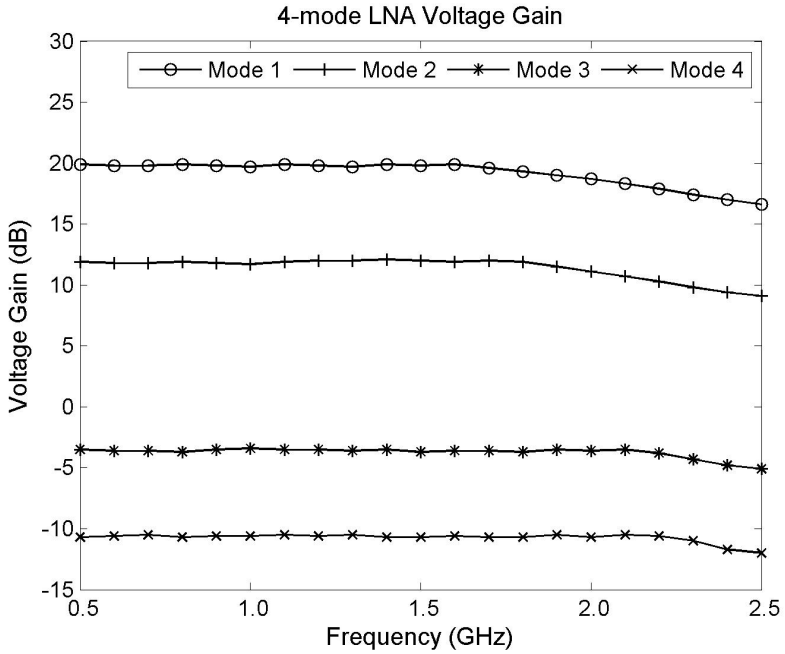

Figure 4.15: Measured voltage gain of the RFPGA four settings.

The s_{11} is below -9.5 dB along the bandwidth in all operating modes, as shown in Fig. 4.16. Fig. 4.17 shows an IIP3 range of 37 dB with a maximum value of 22.8 dBm at the lowest-gain setting. The noise figure (Fig. 4.18) is below 6.1 dB in the maximum-gain setting. The noise figure at gain setting 1 is higher than at gain setting 2. The reason is that gain setting 1 uses LNA1+LNA2, whereas gain setting 2 uses only LNA1, and in both settings LNA1 has the same configuration; hence, it is to be expected that the noise figure at gain setting 1 will be higher than at gain setting 2. However, it should be noted that the RFPGA is designed with the goal of being integrated in a complete SoC where it will drive a mixer, which commonly has a very high noise figure. As system-level design theory dictates, the higher the gain of the LNA stage, the lower the noise figure of the whole receiver. Hence, when integrated in a complete receiver, the use of gain setting 1 will provide a better overall noise figure than gain setting 2, as the higher gain will decrease the effect of the subsequent noisy stages.

The different configuration modes provide a high dynamic range RFPGA that can handle both large amplitude signals (where high linearity is required, and low-noise

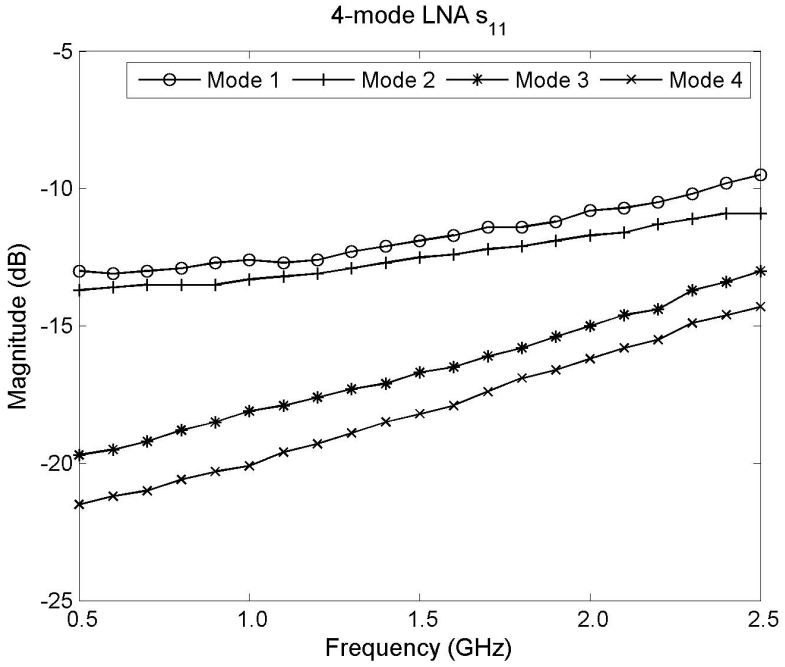

Figure 4.16: Measured s_{11} of the RFPGA four settings.

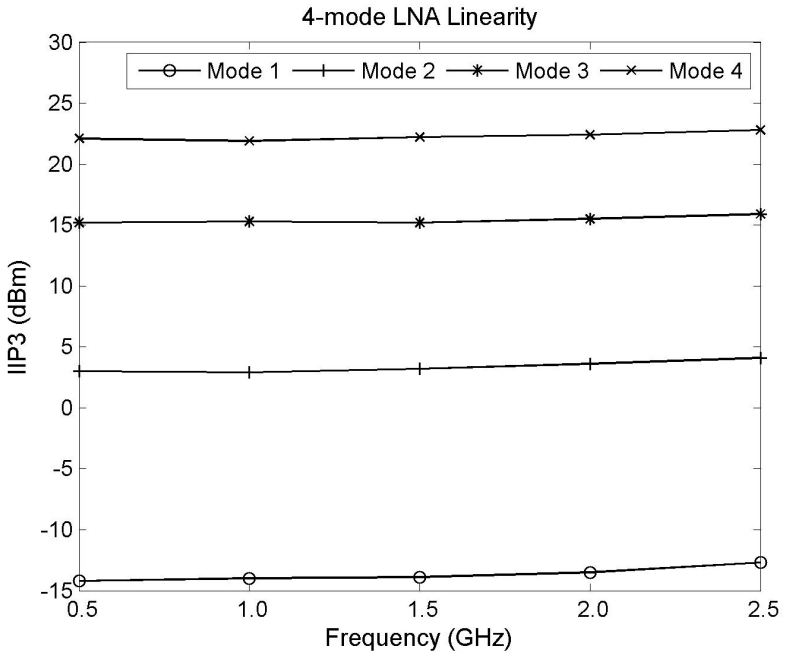

Figure 4.17: Measured IIP3 of the RFPGA four settings.

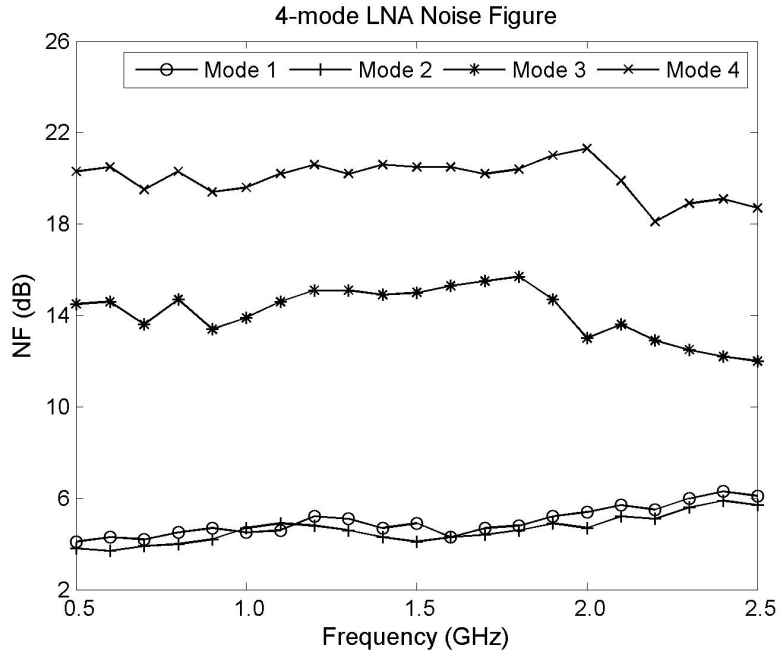

Figure 4.18: Measured noise figure of the RFPGA four settings.

figure is not) and small amplitude signals (where high gain and low-noise figure are required, and high linearity is not). When to switch from one gain setting to another depends on the minimum signal-to-noise-plus-distortion ratio (SNDR) established by the application, which will be ultimately established by the throughput requirements. The switch between gain settings is usually performed by means of an AGC system, which is fairly complex and digitally-controlled in complete SoCs.

Finally, a comparison table with other similar circuits is provided in Table 4.3. The proposed topology improves bandwidth and reduces layout area over a nonswitchable attenuation topology (both capacitive and resistive), making it more suitable for high-frequency applications. The circuits listed in the table provide different gain ranges, so the maximum IIP3 needs to be taken in the context of the minimum gain of each circuit, as higher attenuation results in higher IIP3. Regarding noise figure, the amplifiers in [8, 105, 106] use single-ended topologies. For the same circuit component values and the same operating point of transistors, single-ended topologies provide better a noise figure than differential topologies. A differential topology with external single-ended

to differential conversion was chosen in this design due to its higher immunity to the noise generated by other blocks inside the chip, which is significant in a complete SoC transceiver with analog, RF, and digital blocks. The amplifier in [4] uses a dedicated non-configurable amplifier for the highest gain setting, in parallel with the configurable amplifier, to provide a very low noise figure setting. Finally, the amplifier in [109] uses inductors, which also provide a low noise figure but at the cost of a very large area increase.

Setting	**1**	**2**	**3**	**4**
s_{11} (dB)	<-9.5	<-10.9	<-13	<-14.3
Voltage Gain (dB)	19.9	11.9	-3.5	-10.7
NF (dB)	<6.1	<5.7	<12	<18.7
IIP3 (dBm)	>-14	>3	>15	>22
Power (mW)	39.5	31.1	28.8	28.8
Bypass LNA2	No	Yes	Yes	Yes
ON switches	1 & 4	1 & 4	2 & 5	3 & 5
Impedance matching	Act.	Act.	Res.	Res.

Table 4.2: RFPGA Prototype I experimental results.

4.4 Summary

A two-stage wideband inductorless fully differential RFPGA with high dynamic range has been presented. The first stage of the proposed circuit uses a new switchable capacitive attenuation circuit and two different impedance-matching topologies. The second stage is a tailed-pair amplifier with active loads and CMFB. Hence, the RFPGA can provide different sets of specifications by combining the switchable capacitive attenuation and the impedance-matching topologies, using one or two amplifying stages by powering up or down the second-stage and directly connecting the output of the first stage to the next stage. The presented switchable capacitive attenuation topology reduces the total RFPGA area and improves bandwidth over nonswitchable attenuation topologies, since it only requires one transconductance stage.

Analytical analysis is provided on the switchable capacitive attenuation topology

Table 4.3: RFPGA performance comparison

Ref.	**[106]**	**[8]**	**[105]**	**[4]**	**[109]**	**This work**
Bandwidth (GHz)	0.47∼0.77	0.47∼0.87	0.05∼0.86	0.048∼1	0.47∼0.856	0.5∼2.5
Voltage Gain Range (dB)	−6∼19.6	−17∼16	−18∼14.4[(3)]	−35∼15.4[(3)]	−25∼25	−10.7∼19.9
Minimum NF (dB)[(1)]	1.69	4.3	2.5	2.4[(4)]	1.6	4.1
Maximum IIP3 (dBm)[(2)]	N/A	27	N/A	30	N/A	22.8
Power (mW)	5.3∼13.9	22	19.8	30.6	46.2	28.8∼39.5
Area (mm^2)	0.325	0.32	0.663	0.25	1.5	0.041
Inductorless	No	Yes	Yes	Yes	No	Yes
Differential	No	No	No	Yes	Yes	Yes
Process	90 nm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	2-oxide 65 nm / 0.2 μm

(1) Minimum NF at highest-gain setting
(2) Maximum IIP3 at lowest-gain setting
(3) s_{21}
(4) Uses a dedicated non-configurable amplifier for the highest-gain setting

adding parasitic switch capacitances showing that the capacitor values can be selected in order to provide constant attenuation steps. This chapter also provides analytical analysis on the high-frequency behavior of the input impedance of the active feedback topology and on the noise figure at the highest-gain setting. The high-frequency analysis of the active feedback shows that for certain values of the input and output capacitances the input impedance has peaking behavior and may improve the input matching. The noise analysis shows that there exists a value of feedback resistance that optimizes the noise generated by the active feedback input impedance matching topology.

The fabricated RFPGA achieves a voltage gain range of 30.6 dB with four different gain values and a 3 dB bandwidth from 500 MHz to 2.5 GHz, with a minimum noise figure of 4.1 dB at maximum gain and a maximum IIP3 of 22.8 dBm at minimum gain. The first stage dissipates 31.1 mW, and the second stage dissipates 8.4 mW. The RFPGA is packaged in a 36-pin QFN and occupies a total area of 0.041 mm^2 including the DC decoupling capacitors at each stage.

5

RFPGA Prototype II: Double-Input Switchable Capacitive Attenuation

5.1 Introduction

This chapter presents the implementation of a double-input switchable capacitive attenuation RFPGA (DI-RFPGA) providing 4 different gain settings. We propose the use of a new pre-attenuation based topology consisting of a double-input (DI) switchable capacitive attenuation that provides area, bandwidth and noise improvements over the commonly-used non-switchable multiple-stage (MS) non-switchable capacitive attenuation circuit and the single-input switchable capacitive attenuation circuit presented in Chapter 4. The chapter is divided in three sections: design, experimental results and summary.

The design section starts with the core concept of the DI topology and then continues with the full circuit schematic of the topology. After introducing the topology, the sizing of the various elements in the circuit are analyzed in order to provide the same gain settings than the MS topology and finally and the section ends by providing

an analysis of the noise generated at the different gain settings and compares it to the MS topology under equal gain and power consumption. The comparison is given only with respect to the MS topology since, as has been explained in the previous chapter, it provides lower noise figure than the single-input switchable capacitive attenuation topology.

The next section contains the experimental results of the manufactured DI-RFPGA topology. The circuit has been manufactured using a 65 nm CMOS technology, packaged inside a QFN and solded on PCB. The chapter ends with a summary section providing an overview of the contents presented.

5.2 Design

This sections starts by introducing the concept of the double-input switchable capacitive attenuation topology using basic blocks, without entering into transistor-level design, in order to provide a basic understanding of the topology and its advantages. Then, the schematic of the DI-RFPGA using switchable capacitive attenuation is presented, showing the transistor-level design.

The circuit topology subsection of the DI-RFPGA is followed by a subsection explaining the design of the several gain settings in order to provide the same gain as in the MS topology. By designing both topologies providing the same gain at all settings, a more clear comparison of noise figure performance between topologies can be provided in the next and last subsection. This last subsection finds the analytical expression of the DI topology noise figure as a function of the MS topology noise figure and compares them under different design scenarios.

5.2.1 Core Concept

Typical pre-attenuation based amplifiers with capacitive attenuation use a multiple-stage (MS) G_m structure and a non-switchable capacitor ladder as shown in Fig. 5.1a [4, 5, 6, 7, 8]. This structure has two main drawbacks. On one hand, it requires a

G_m stage for each attenuation step, thus increasing the layout area it occupies as the number of required attenuation steps increases. On the other hand, the load capacitance is largely increased as the output capacitance of each G_m stage is added to the total load capacitance, thereby significantly decreasing the amplifier bandwidth compared to a single-G_m amplifier.

One structural solution to eliminate these two drawbacks is to use a switchable capacitive attenuation topology (Fig. 5.1b) as presented in Chapter 4. This structure adds switches ($S_1 - S_4$) at each attenuation step so that by closing no more than one switch at any given time, only one path is available for the input signal to reach the amplifying stage. Hence, only one G_m stage is required, reducing area and increasing bandwidth as compared to the non-switchable capacitive attenuation topology.

The switchable topology, however, has a higher noise figure. The input switches, which must be implemented using transistors in a CMOS technology, have a non-negligible channel resistance which adds noise at the input node before amplifying the signal. This is especially detrimental at the highest-gain setting which handles the smallest amplitude input signals and therefore requires a very low noise figure.

To eliminate the drawbacks of these two topologies, we have designed a double-input switchable capacitive attenuation topology as shown in Fig. 5.1c. At the highest gain setting, switches $S_1 - S_5$ are open and the circuit behaves as a cascoded common-source amplifier without adding any input signal attenuation. At the other gain configurations, switches $S_4 - S_5$ are closed and only one of the switches $S_1 - S_3$ is closed at any given time to select the desired attenuation step. Thus, transistor $M1$ is cut-off and the circuit operates as a common-source amplifier ($M2$ being the amplifying device) with degeneration (provided by the on-resistance of switch S_4). The voltage gain of the 4 gain settings can be defined as:

$$Av_{set_1} = g_{m1} R_L \tag{5.1}$$

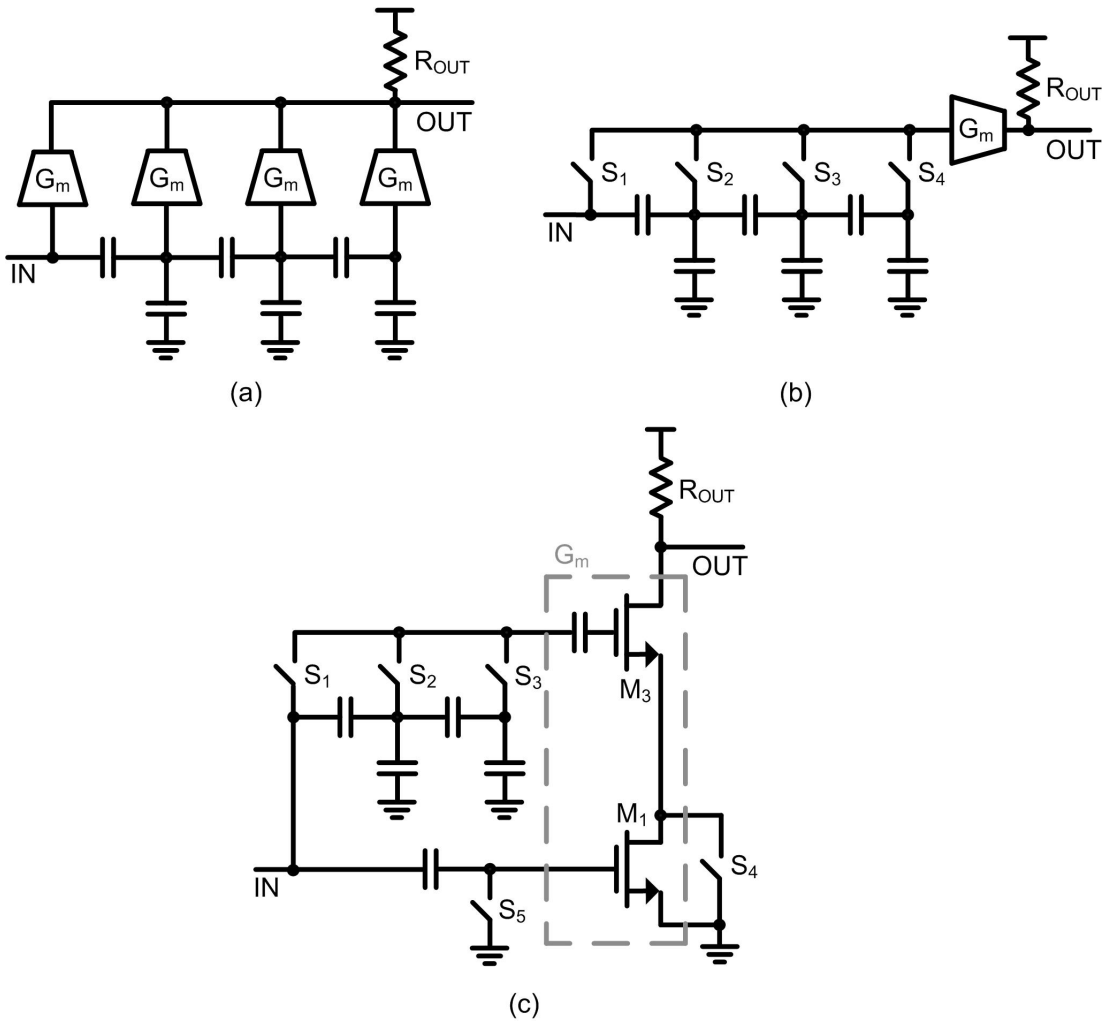

Figure 5.1: Implementations of capacitive attenuation PGAs: (a) Non-switchable (b) Switchable (c) Double-input switchable.

$$Av_{set_x} = \frac{g_{m3}R_L}{\alpha_{set_x}(1 + g_{m3}R_D)} \tag{5.2}$$

Where set_x refers to the gain setting, set_1 being the highest gain setting and set_4 the lowest gain setting, Av_{set_1} is the voltage gain of the highest gain setting (cascoded CS configuration), Av_{set_x} the voltage gain of a non-highest gain setting (degenerated CS configuration, where x can get the values of 2, 3 and 4), α_{set_x} the attenuation added by the capacitive attenuation circuit (which equals 1 for $x = 2$, and is equal to the desired attenuation for $x = 3$ and $x = 4$) and R_D the value of resistance degeneration of S_4. The size of the cascode, the degeneration and the capacitors in the capacitive attenuation topology can be chosen to provide different gain steps, as required for each application, as will be analyzed later. The degeneration provided by the channel resistance of switch S_4 linearizes the transconductance and therefore the amplifier provides better linearity at the gain settings using attenuation, where high linearity is the main requirement.

By using the double-input topology, the DI-RFPGA provides a better performance in terms of bandwidth and area than the MS topology and solves the noise problem at the highest-gain setting due to the switch in series of the single-input switchable capacitive attenuation topology. Also, as will be analyzed in a later section, the DI topology provides better noise figure than the MS topology at all gain settings for most of the practical implementations.

5.2.2 Circuit Topology

The full schematic of the manufactured DI-RFPGA (biasings omitted) is shown in Fig. 5.2. The circuit uses a CMFB to set the output DC voltage level by controlling the tail current. Following the same structure of the previously presented single-input RFPGA in Chapter 4, the DI-RFPGA uses a selectable input impedance matching scheme consisting of an active feedback for the highest-gain setting (gain setting 1) and shunt resistor for the attenuation settings (the term attenuation settings is used to refer to the gain settings other than the highest one, which are numbered as the gain

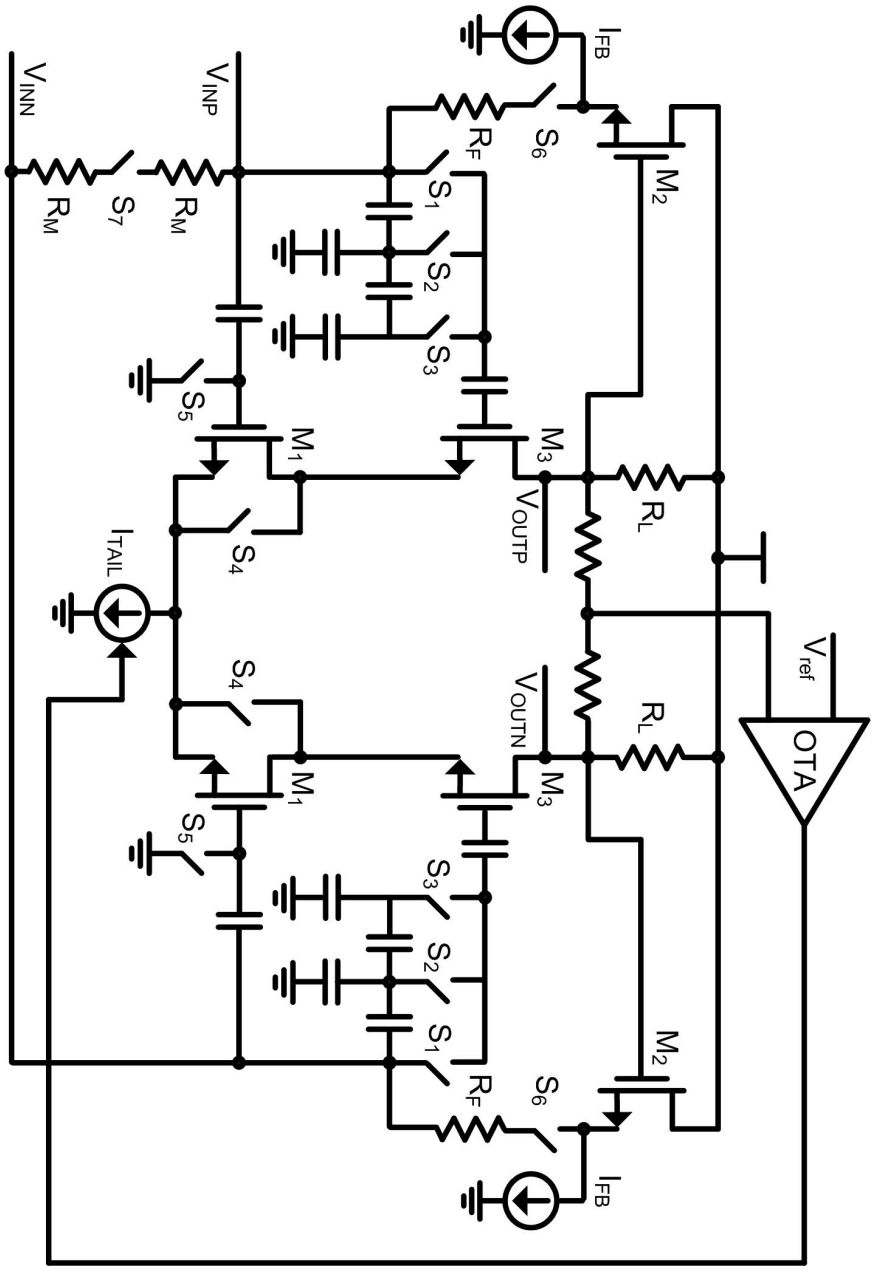

Figure 5.2: Schematic of the differential double-input RFPGA with switchable capacitive attenuation.

settings 2, 3 and 4). The same analysis for input impedance calculation, high-frequency effects and noise optimization can be applied to this topology.

To provide a more clear picture of the components used in each gain setting, Fig. 5.3 (gain settings 1 and 2) and Fig. 5.4 (gain settings 3 and 4) show the full schematic of the DI-RFPGA for each of the 4 gain settings shading in gray the components that are not used in the corresponding gain setting.

5.2.3 Sizing of the Attenuation Steps

The sizing of the various elements in the DI topology are analyzed in order to provide the same gain settings than the MS topology. The reason for this process is to provide a fair comparison (same gain and power consumption) of the noise figure generated by both topologies in the next section. The comparison in this section and the next section is performed only versus the MS topology, as it has been established in the previous chapter that it provides a lower noise figure than the single-input switchable capacitive attenuation topology.

As opposed to the multiple-stage and single-input topologies where the amplification is performed by one circuit topology (common-source) and all the gain settings are provided through the capacitive attenuation circuit, in the double-input topology the amplification is performed by two circuit topologies:

- At gain setting 1, amplification is performed with a cascoded common-source topology (Fig. 5.3a) and the input impedance matching with active feedback.
- At gain setting 2, amplification is performed with a degenerated common-source topology (Fig. 5.3b) and the input impedance matching with parallel resistance.
- At gain settings 3 and onward, amplification is performed with a degenerated common-source topology and the different gain steps are provided by a the capacitive attenuation circuit (Fig. 5.4). Input impedance matching is performed with a parallel resistance.

Therefore, three different design objectives must be taken into account:

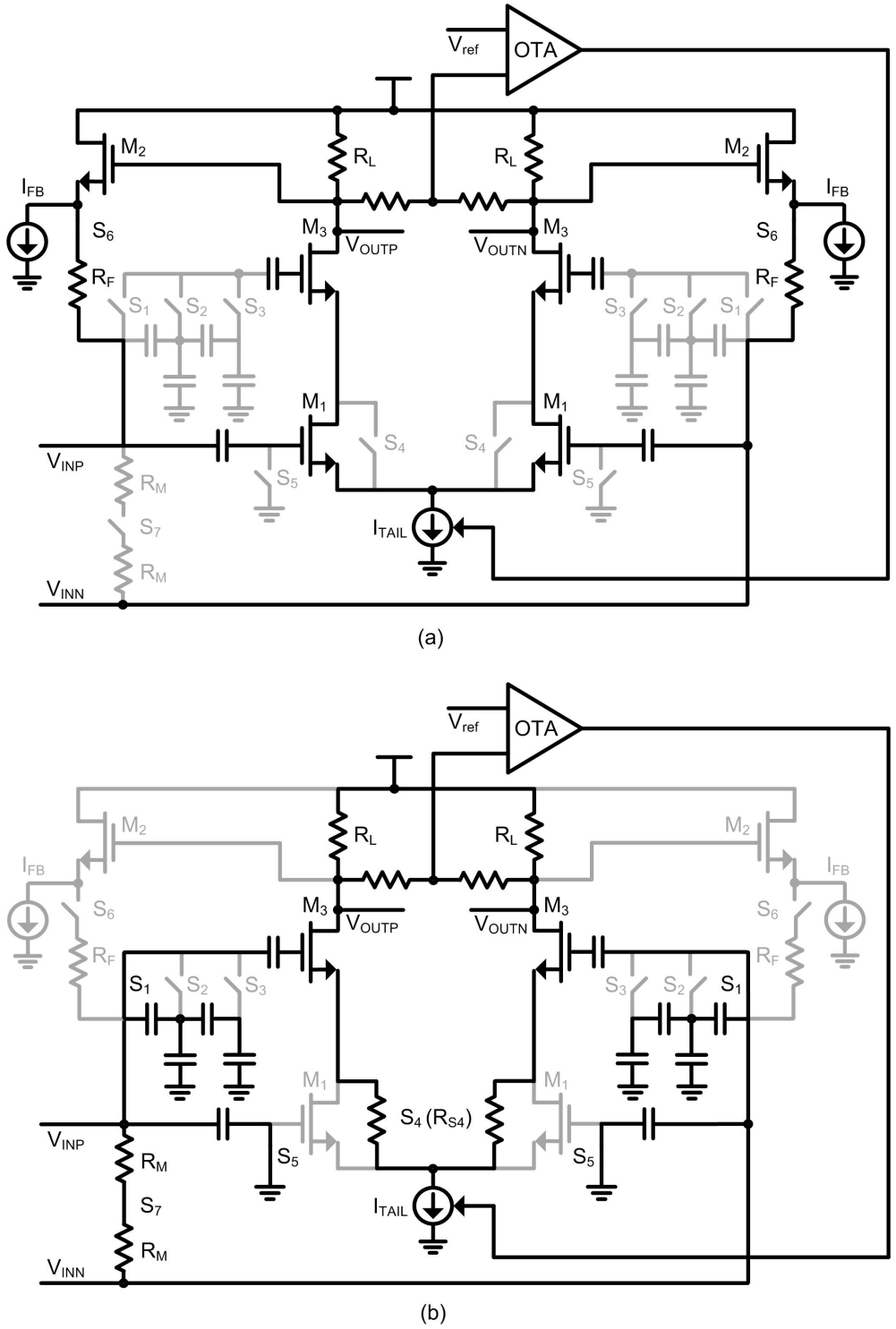

Figure 5.3: Schematic of the differential double-input RFPGA with switchable capacitive attenuation (a) Gain setting 1 (b) Gain setting 2

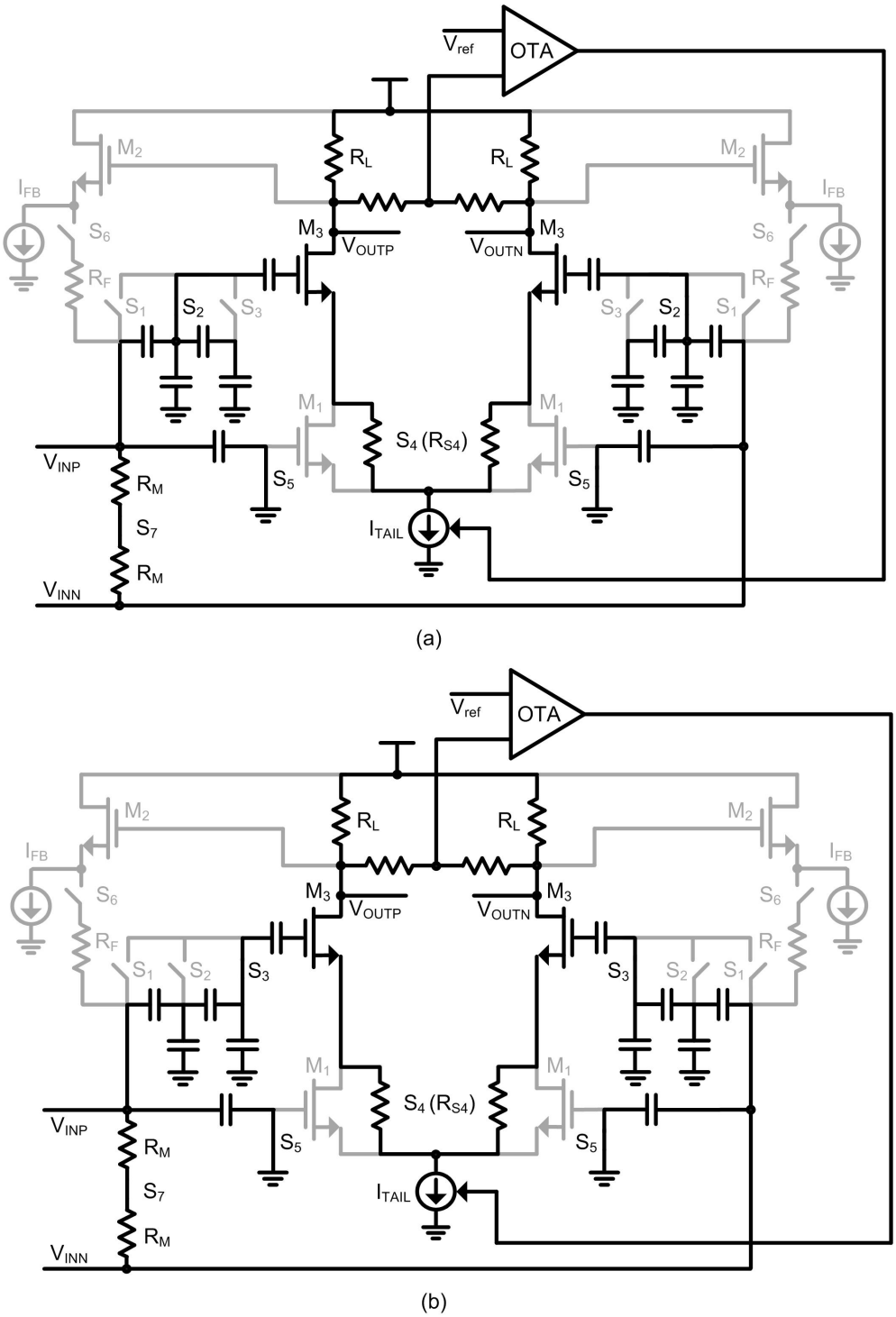

Figure 5.4: Schematic of the differential double-input RFPGA with switchable capacitive attenuation (a) Gain setting 3 (b) Gain setting 4

- How to size the cascoded common-source circuit to obtain the same gain as the common-source circuit in the MS topology and in the single-input topology.
- How to size the degenerated common-source circuit to obtain the same gain as the first attenuation step in the MS topology and in the single-input topology.
- How to size the first attenuation step (and onward) of the DI topology to obtain the same gain as the second attenuation step (and onward) in the MS topology and in the single-input topology.

From here to the end of the chapter, it is considered that the cascode transistor in the DI topology (M_3) is designed with the same transconductance and size (width and length) as the common-source transistor (M_1) for a fair comparison between all the gain settings of the DI and MS topologies.

The DI topology has been presented as requiring one additional transistor compared to the MS topology. However, it should be noted that the MS topologies in the provided literature use a cascode transistor due to its benefits and therefore the DI and MS topologies have the same number of transistors. Still, the analysis from now on considers a cascode-less MS topology to provide a worse case scenario.

The next three subsections analyze the sizing of the components in the DI topology to provide the same gain as the MS topology. First, we compare the first gain setting (highest gain setting) which in the DI topology corresponds to the cascoded common-source topology, then we compare the second gain setting which corresponds to the degenerated common-source without input attenuation and finally we compare the rest of the gain settings which correspond to the degenerated common-source with input attenuation.

5.2.3.1 Cascoded Common-Source Sizing

The highest-gain setting in the DI topology is composed of a cascoded common-source topology whereas in the MS topology it is composed of a cascode-less common-source

topology. As has been previously explained, this provides a worse case scenario compared to the presented literature which uses an MS topology with cascode.

The simplified circuits (omitting input impedance matching and biasings) of the MS topology and the DI topology at the highest-gain setting are shown in Fig. 5.5a and Fig. 5.5b respectively. By using basic circuit theory, we can find the voltage gain of both configurations respectively:

$$Av_{MS-set_1} = g_{m1}R_L \tag{5.3}$$

$$Av_{DI-set_1} = g_{m1}R_L \tag{5.4}$$

Therefore, the cascode transistor M_3 in the DI topology has no effect on the gain and as long as the components in both topologies are designed with the same parameters, both topologies will provide the same voltage gain at the highest-gain setting.

5.2.3.2 Degenerated Common-Source Sizing

The second gain setting in the DI topology is composed of a degenerated common-source topology whereas in the MS topology it is composed of a common-source topology with one step of capacitive attenuation. The simplified circuits (omitting input impedance matching and biasings) of the MS topology and the DI topology at the second gain setting are shown in Fig. 5.5c and Fig. 5.5d respectively. By using basic circuit theory, we can find the voltage gain of both configurations respectively:

$$Av_{MS-set_2} = \frac{g_{m1}R_L}{\alpha_1} \tag{5.5}$$

$$Av_{DI-set_2} = \frac{g_{m3}R_L}{(1 + g_{m3}R_D)} \tag{5.6}$$

The equations take into account the voltage divider effect due to the shunt resistance input impedance matching, which for $R_M = R_S$ adds the term 2 at the denominator.

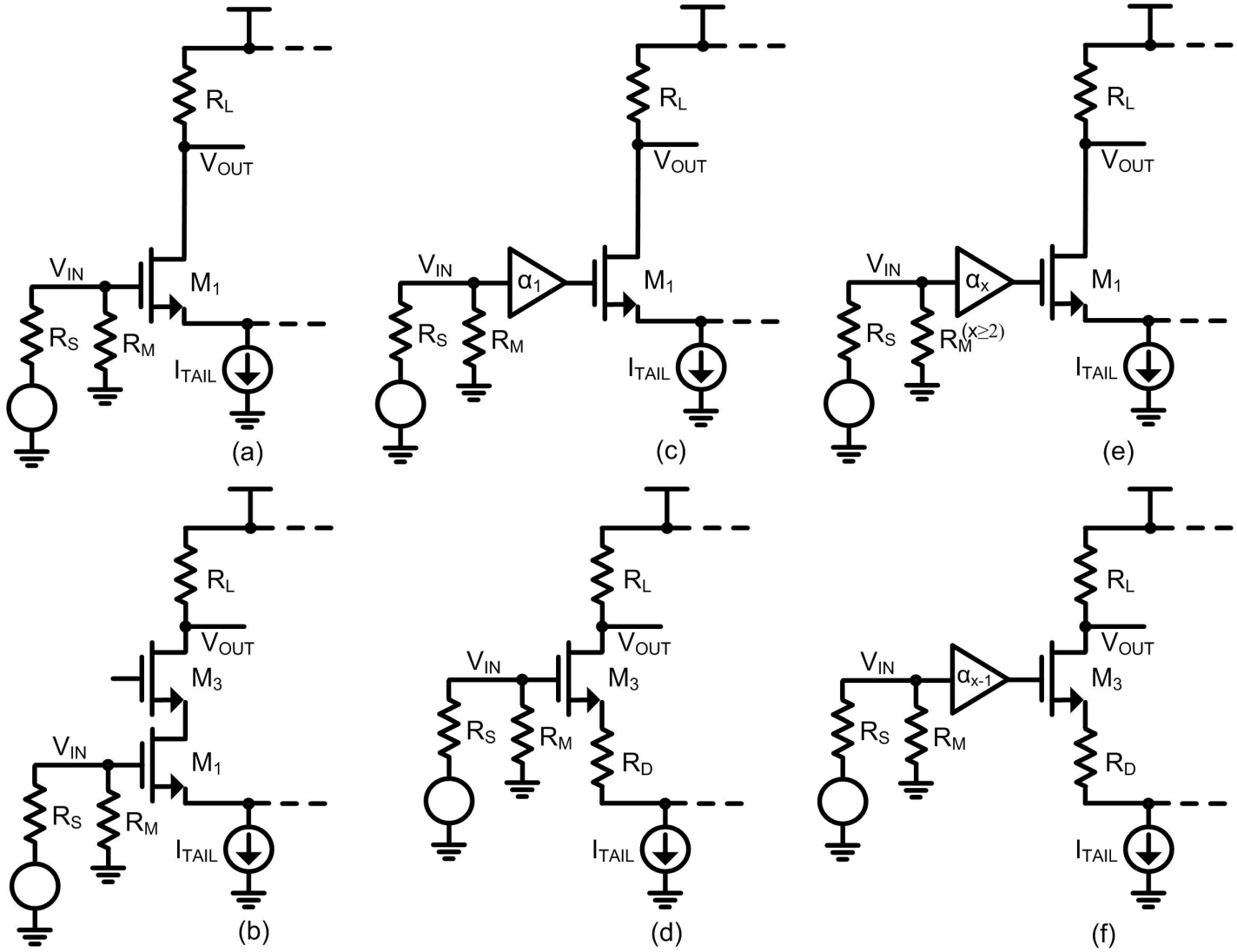

Figure 5.5: Simplified schematics (omitting input impedance matching and biasings) of the MS topology at (a) Gain Setting 1 (c) Gain Setting 2 (e) Gain Setting 3 and onward; and of the DI topology at (b) Gain Setting 1 (d) Gain Setting 2 and (f) Gain setting 3 and onward.

The objective is for the DI topology to provide the same gain as the MS topology, therefore we equal the two expressions:

$$\frac{g_{m1}R_L}{\alpha_1} = \frac{g_{m3}R_L}{(1+g_{m3}R_D)} \tag{5.7}$$

Considering that $g_{m3} = g_{m1}$ and the size (width and length) is the same for $M1$ and $M3$, we can re-write Eq. 5.7 to obtain the required value of degeneration resistance to provide the same gain in both topologies:

$$R_D = \frac{\alpha_1 - 1}{g_{m1}} \tag{5.8}$$

Thus, by using a degeneration resistance equal to the first attenuation step of the MS topology (α_1) divided by the transconductance of the input device (g_{m1}), the second gain setting of the DI and the MS topologies provide the same gain.

It should be noted that considering that $g_{m3} = g_{m1}$ is not optimal and is done only for comparison purposes with equally-sized components. In the DI circuit design, g_{m3} will be chosen in order to provide the required noise and gain specifications independently of g_{m1}.

5.2.3.3 Capacitive Ladder Sizing

The third and fourth gain settings in the DI topology are composed of a degenerated common-source topology with one and two capacitive attenuation steps respectively, whereas in the MS topology it is composed a common-source topology with two and three attenuation steps respectively.

The simplified circuits (omitting input impedance matching and biasings) of the MS topology and the DI topology beyond the second gain setting are shown in Fig. 5.5e and Fig. 5.5f respectively. If the design guidelines provided in the previous section to obtain the same gain in both the DI and MS topologies at gain setting 2 are followed, the only requirement to provide the same gain in gain setting 3 and onward is that the capacitive ladder has a constant attenuation step. Then, both topologies will add the

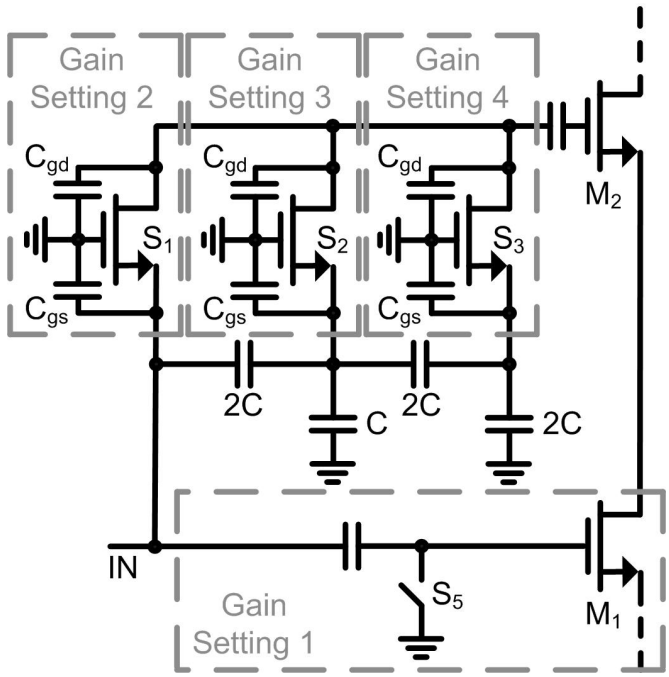

Figure 5.6: Double-input switchable capacitive attenuation using a C-2C ladder and including switch parasitic capacitances.

same attenuation step at each gain setting.

The analysis for the capacitor sizing of the switchable capacitive attenuation for the DI-RFPGA is equivalent to that of the single-input switchable capacitive attenuation RFPGA. Fig. 5.6 shows the input part of the DI-RFPGA substituting the switches for NMOS transistors and adding the corresponding parasitic capacitances. The main path of the circuit corresponding to the gain setting 1 can be neglected as the gate of M_1 is connected to ground and its transconductance and current consumption is negligible at attenuation settings (settings 2, 3 and 4). Therefore, the capacitive ladder of the secondary path in the double-input topology used during attenuation settings is equal to that of the main path in the single-input topology and thus the capacitor values can be tuned to provide constant attenuation steps of the desired value following the analysis in Chapter 4.

Then, as long as the gain of settings 1 and 2 is equal for both the DI and MS topologies by following the guidelines of the previous 2 subsections, the settings of each

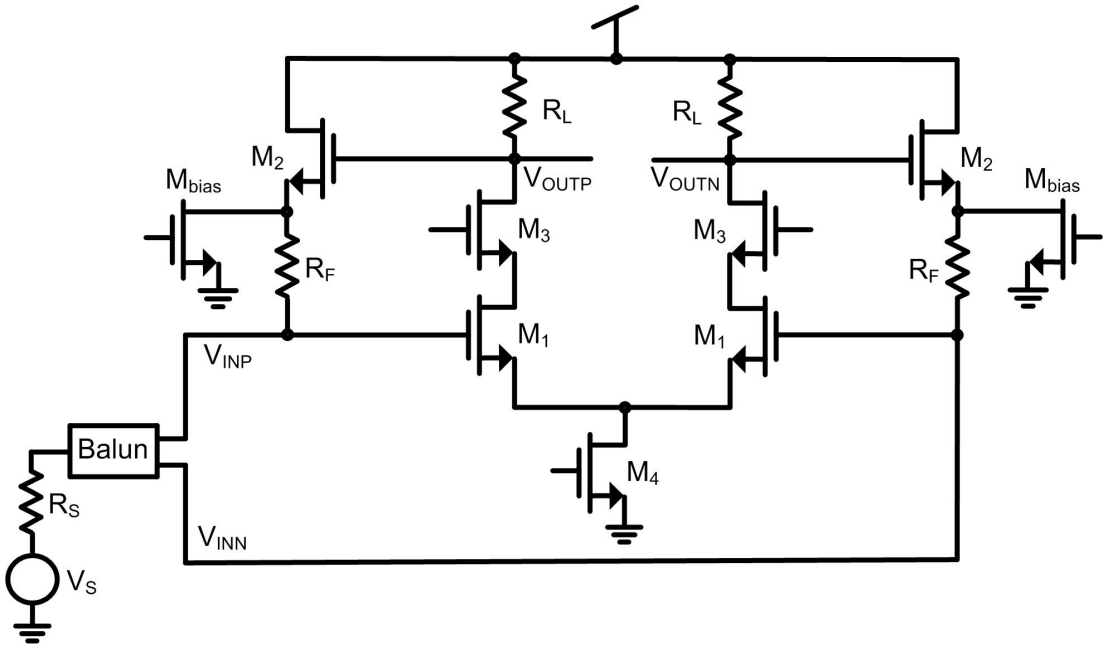

Figure 5.7: DI-RFPGA simplified schematic used for noise calculations at the highest-gain setting.

topology will provide the same gain at settings 3 and 4.

5.2.4 Noise Comparison with the Multiple-Stage Topology

This section compares the noise figure of the DI topology versus the MS topology. The MS topology is used in this section instead of the single-input switchable capacitive attenuation topology presented in Chapter 4 since it provides a lower noise figure. The first section analyzes the noise generated at the highest-gain setting, whereas the second section analyzes the noise generated at the attenuation settings.

5.2.4.1 Noise at Highest-Gain Setting

The equations are calculated using the simplified schematic shown in Fig. 5.7. The simplified schematic does not include the switchable capacitive attenuation ladder and the parallel input impedance matching since both circuits are not used at the highest gain mode.

Component	Noise Factor	
	MS	**DI**
R_S	1	1
M_1	$\frac{4\gamma_1}{g_{m1}R_S}$	$\frac{4\gamma_1}{g_{m1}R_S}$
R_F	$\frac{4R_F}{R_S A_v^2}$	$\frac{4R_F}{R_S A_v^2}$
M_2	$\frac{2\gamma_2}{A_v}\left[1-\frac{2R_F}{R_S A_v}\right]$	$\frac{2\gamma_2}{A_v}\left[1-\frac{2R_F}{R_S A_v}\right]$
R_L	$\frac{4}{g_{m1}R_S A_V}$	$\frac{4}{g_{m1}R_S A_V}$
M_{bias}	$\gamma_{bias}g_{mbias}R_S\left[1-\frac{2R_F}{R_S A_v}\right]^2$	$\gamma_{bias}g_{mbias}R_S\left[1-\frac{2R_F}{R_S A_v}\right]^2$
M_3	—	0

Table 5.1: Noise factor dependencies of each component of MS and DI topologies at highest gain setting.

The noise factor generated by the amplifier can be expressed as a sum of the noise factor generated by each component:

$$F_{DI} = F_{R_S} + F_{M_1} + F_{R_F} + F_{M_2} + F_{R_L} + F_{M_{bias}} + F_{M_3} \tag{5.9}$$

By following the same process used in Chapter 4 in Eq. 4.2—4.7, we can calculate the noise factor contribution of each term, which are summarized in Table 5.1. As can be seen, the noise contribution of the cascode transistor M_3 is 0 and all the other terms are equal for both topologies. Therefore, given the current analysis, the DI has the same noise figure than the MS topology at the highest-gain setting.

The previous analysis has taken into account a small-signal model which does not include channel modulation effects, therefore the channel resistance (R_{DS}) of M_3 is not present, which results in noise current generated by M_3 not appearing at the output. To further expand the analysis to provide a more real effect of the noise due to the cascode transistor M_3, the channel resistances (R_{DS}) of the transistors are placed in the small-signal model in parallel with the noise current sources of each transistor.

Repeating the noise analysis adding the channel resistances, the noise factor due to the cascode transistor is as follows:

$$F_{M_3} = \frac{4\gamma_3 g_{m2}}{g_{m1}^2 R_S} \frac{R_{DS3}^2}{R_{DS1}^2 (1 + g_{m3} R_{DS3})^2} \tag{5.10}$$

By approximating $\gamma_3 \approx \gamma_1$ and $R_{DS3} \approx R_{DS1}$ since M_1 and M_3 are equally sized and have the same current consumption, the equation can be re-written as:

$$F_{M_3} \approx F_{M_1} \frac{1}{(1 + g_{m1} R_{DS1})^2} \tag{5.11}$$

Which provides the relation of noise factor generated by M_3 as a function of M_1. The equation also contains two more variables, which are the transconductance and channel resistance of the transistors. To obtain a more clear relationship between the two noise factors, we need to give typical values to g_{m1} and R_{DS1}.

The content of this thesis is centered on high-frequency wideband inductor-less low-noise amplifiers. Since small output load resistances are required to comply with the high frequency requirement, a large transconductance is required in the amplifying devices to comply with gain specifications. To provide low-noise, a large transconductance in the amplifying devices is also required. This results in a transconductance that is usually in the range of 60 mS to 100 mS.

Channel resistances in this situation are typically of the order of 60 Ω to 120 Ω (obtained through simulation). For the design implementation of this prototype, the values of g_m and R_{DS} are 85 mS and 71 Ω respectively, resulting in the following noise factor due to the cascode transistor:

$$F_{M_3} \approx \frac{F_{M_1}}{49.5} \tag{5.12}$$

Thus, for the design parameters of this prototype, the noise factor due to the cascode transistor is negligible compared to the noise factor of the main transistor, and can be considered that the DI and the MS topologies provide the same noise factor at the highest-gain setting. Also, considering the practical applications of these topologies in

low-noise high-frequency wideband inductor-less amplifiers (by using typical ranges of g_m and R_{DS}), this assertion can be generalized to state that the DI topology provides the same noise figure than the MS topology at the highest-gain setting.

5.2.4.2 Noise at Attenuation Settings

To compare the noise generated by the two topologies at attenuation settings (gain settings 2, 3 and 4) the following methodology is followed. The noise factor of a transistor depends on technology parameters such as γ, which is the thermal excess noise factor of the transistor. At nanometer technologies such as 65 nm it is very difficult to provide typical values for γ and generally it is not provided by foundries. Therefore it is not possible to provide absolute values of noise figure for each topology in order to compare them. In order to compare the two topologies, we are going to calculate the noise figure of the DI topology as a function of the noise figure of the MS topology. As will be seen later, this eliminates the γ parameter from the final equation.

The equations are calculated using the simplified schematics shown in Fig. 5.8a and Fig. 5.8b for the DI and MS topologies respectively. As opposed to the highest-gain setting, the schematics now include the attenuation provided by the capacitive attenuation ladder (α_{DI_x} and α_{MS_x}, where x equals the gain setting) and by the parallel resistance input impedance matching topology (R_M). The active feedback impedance matching is neglected as it is powered-down at attenuation settings.

By following the same process used in Chapter 4 in Eq. 4.2—4.7, we can calculate the noise factor contribution of each component, which are summarized in Table 5.2. As can be seen, the noise generated by the common components in both topologies is the same, and the DI topology has two additional components that add noise (R_{SW} and R_D). However, the attenuation value α is different for each topology, as shown in Table 5.3, where Att_{Step} is the designed attenuation step of the capacitive ladder.

To compare the noise generated by the two topologies at attenuation settings, we start by defining the total noise of the MS topology:

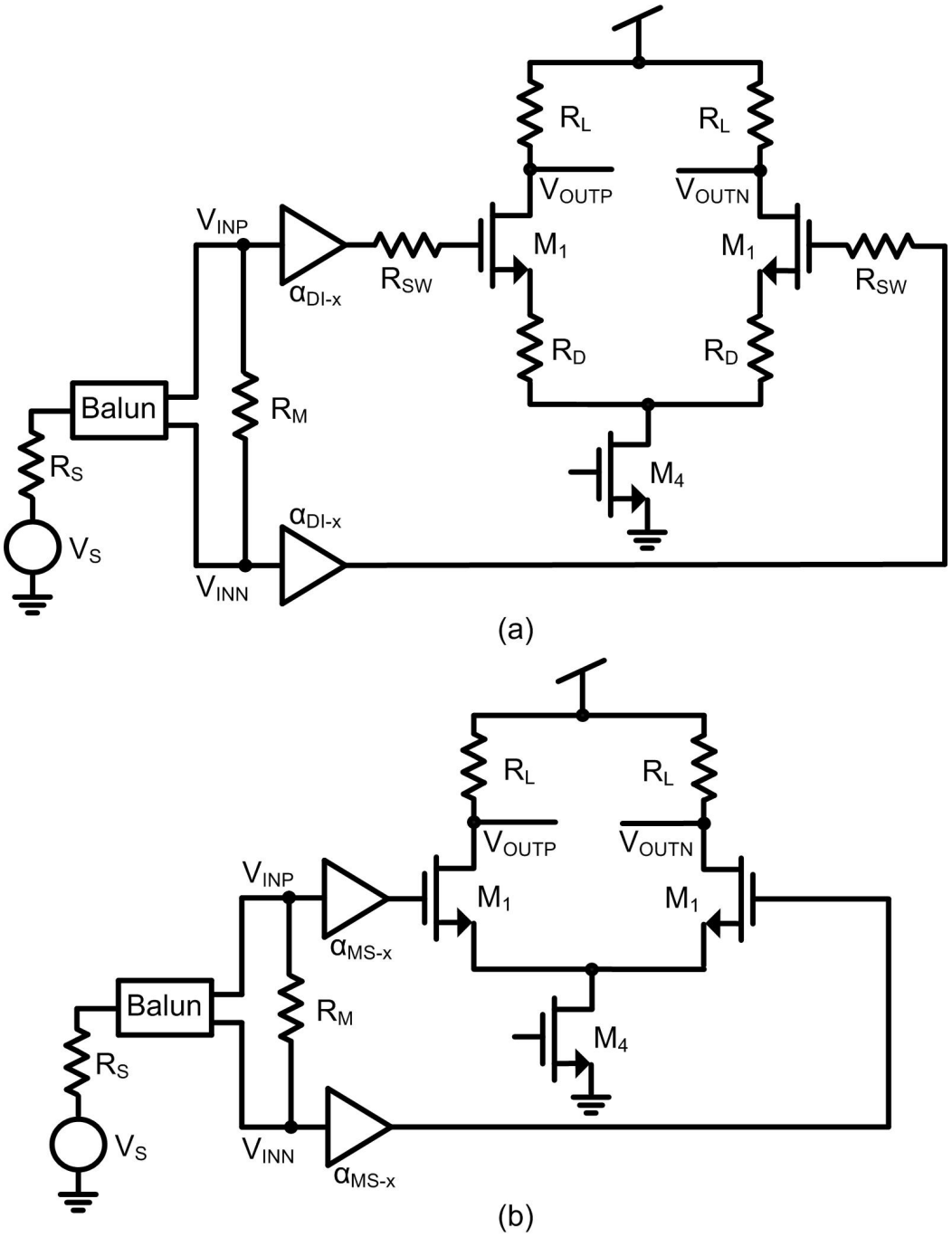

Figure 5.8: Simplified schematics used for noise calculations at attenuation settings (a) DI topology (b) MS topology.

Component	Noise Factor	
	MS	**DI**
R_S	1	1
R_M	1	1
R_{SW}	—	$\frac{8\alpha_{DI}^2 R_{SW}}{R_S}$
M_1	$\frac{8\alpha_{MSx}^2 \gamma_1}{R_S g_{m1}}$	$\frac{8\alpha_{DIx}^2 \gamma_1}{R_S g_{m1}}$
R_L	$\frac{8\alpha_{MSx}^2}{R_S R_L g_{m1}^2}$	$\frac{8\alpha_{DIx}^2}{R_S R_L g_{m1}^2}$
R_D	—	$\frac{8\alpha_{DIx}^2 R_D}{R_S}$

Table 5.2: Noise factor dependencies of each component of MS and DI topologies at attenuation settings.

Gain Setting	α_x	
	MS	**DI**
2	1	Att_{Step}
3	Att_{Step}	$2Att_{Step}$
4	$2Att_{Step}$	$3Att_{Step}$

Table 5.3: Attenuation values for the different settings of the DI and MS topologies.

$$F_{MS} = 2 + \frac{8\alpha_{MS_x}^2 \gamma_1}{R_S g_{m1}} + \frac{8\alpha_{MS_x}^2}{R_S R_L g_{m1}^2} \tag{5.13}$$

We re-write the equation as:

$$F_{MS} = 2 + \alpha_{MS_x}^2 \chi \tag{5.14}$$

Where:

$$\chi = \frac{8\gamma_1}{R_S g_{m1}} + \frac{8}{R_S R_L g_{m1}^2} \tag{5.15}$$

Then we define the total noise generated by the DI topology:

$$F_{DI} = 2 + \frac{8\alpha_{DI_x}^2 \gamma_1}{R_S g_{m1}} + \frac{8\alpha_{DI_x}^2}{R_S R_L g_{m1}^2} + \frac{8\alpha_{DI_x}^2 R_{SW}}{R_S} + \frac{8\alpha_{DI_x}^2 R_D}{R_S} \tag{5.16}$$

We substitute Eq. 5.15 into Eq. 5.16:

$$F_{DI} = 2 + \alpha_{DI_x}^2 \left(\chi + \frac{8R_{SW}}{R_S} + \frac{8R_D}{R_S} \right) \tag{5.17}$$

Then we re-write Eq. 5.14 as:

$$\chi = \frac{F_{MS} - 2}{\alpha_{MS_x}^2} \tag{5.18}$$

And substitute Eq. 5.18 into Eq. 5.17:

$$F_{DI} = 2 + \alpha_{DI_x}^2 \left(\frac{F_{MS} - 2}{\alpha_{MS_x}^2} + \frac{8R_{SW}}{R_S} + \frac{8R_D}{R_S} \right) \tag{5.19}$$

Finally, Eq. 5.8 is substituted into Eq. 5.17 so that the gain of both topologies is the same:

$$F_{DI} = 2 + \alpha_{DI_x}^2 \left(\frac{F_{MS} - 2}{\alpha_{MS_x}^2} + \frac{8R_{SW}}{R_S} + \frac{8(\alpha_{MSx} - 1)}{R_S g_{m1}} \right) \tag{5.20}$$

Using Eq. 5.20 we can get the noise factor of the DI topology for a given noise

factor of the MS topology in order to compare them. The resulting difference between the two noise factors will depend on the attenuation step of the capacitive ladder (see Table 5.3 for the values of α for each topology and each gain setting) and the input transconductance g_{m1}. There are two other parameters in the equation, R_S and R_{SW}. For the noise plots, the source resistance R_S is set to 75 Ω which is the value defined in the G.hn specification. The switch on-resistance R_{SW} is set to 10 Ω. Although the switch on-resistance used in the prototype design is 7 Ω, a higher value is used to provide a less favorable situation for the DI topology and show that it still provide better noise performance than the MS topology in most practical implementations.

The noise figure difference between the DI and MS topologies for the three attenuation settings are provided for gain setting 2 in Fig. 5.9, gain setting 3 in Fig. 5.10 and gain setting 4 in Fig. 5.11. The resulting group of figures provides the noise figure difference between the MS and the DI topologies for different values of transconductance, MS noise figure and attenuation step.

The DI topology provides a better noise figure than the MS topology for the higher range of transconductance. As the transconductance of the circuit decreases, the noise figure difference decreases and the MS topology may even provide a better noise figure than the DI topology. However, the content of this thesis is centered on high-frequency wideband inductor-less low-noise amplifiers. Since small output load resistances are required to comply with the high-frequency requirement, a large transconductance is required in the amplifying devices to comply with gain specifications. To provide low-noise, a large transconductance in the amplifying devices is also required. This results in a transconductance that is usually in the range of 60 mS to 100 mS, where the DI topology provides better performance than the MS topology.

The reader should also note that the results are dependent on the noise figure of the MS topology at each gain setting, which is higher as more attenuation is used. The MS noise figure values in the presented plots have been chosen so as to include within its range typical NF values seen by simulation and in previous publications [5, 6, 7, 8]. It may be possible that the lowest value of MS noise figure in each subplot cannot be

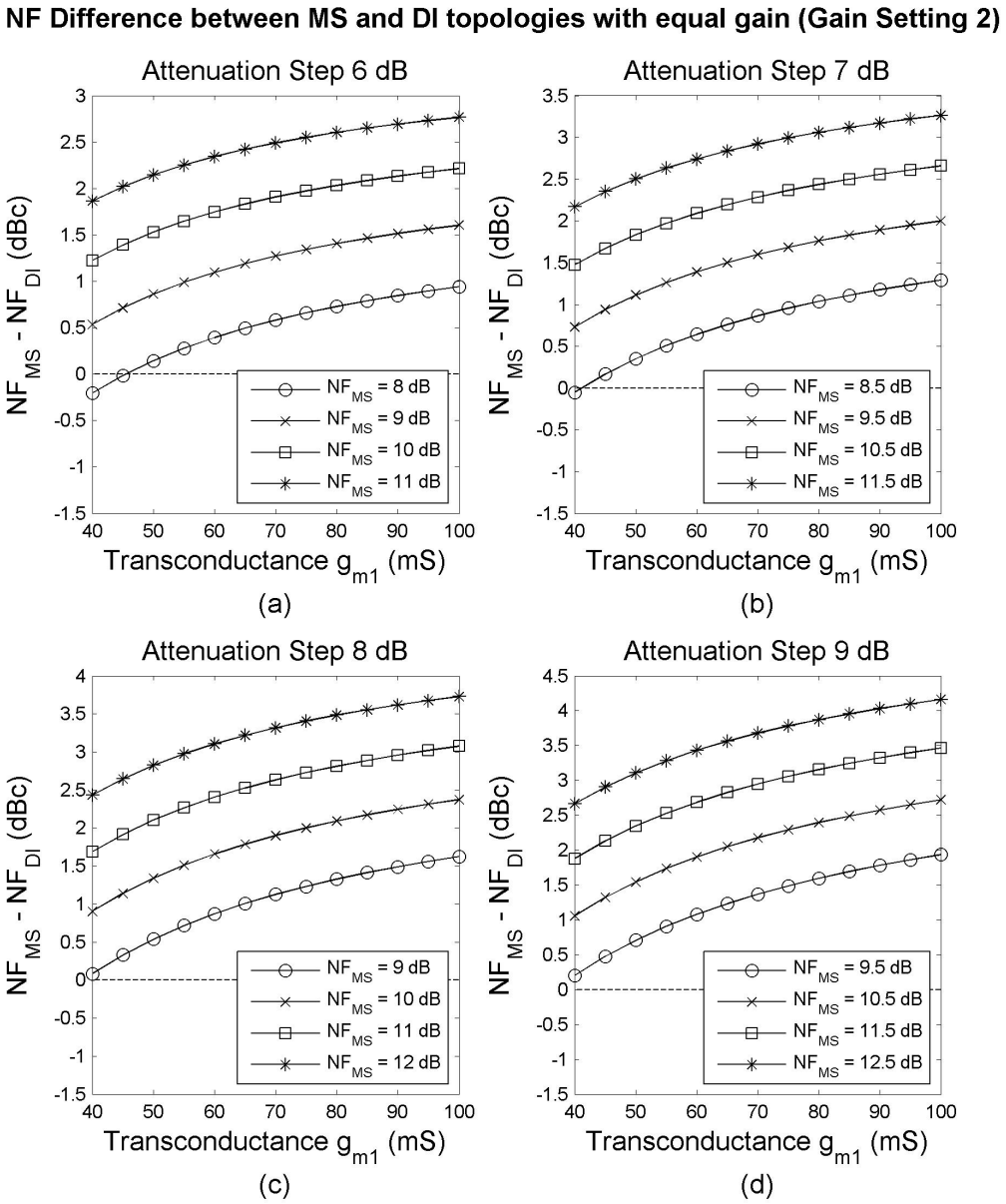

Figure 5.9: Noise figure difference between the MS and the DI topologies (Gain Setting 2) for different values of transconductance, MS noise figure and attenuation step.

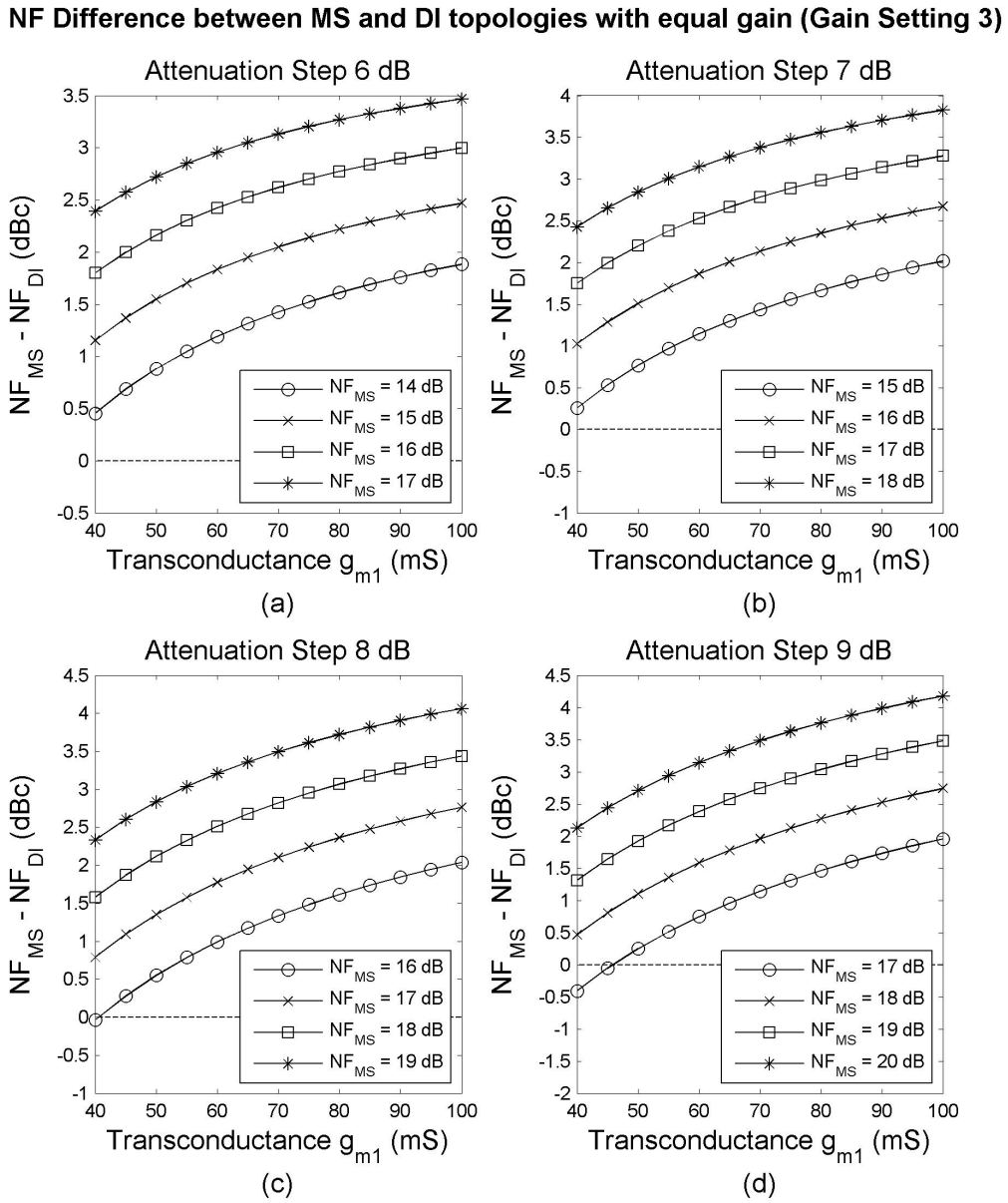

Figure 5.10: Noise figure difference between the MS and the DI topologies (Gain Setting 3) for different values of transconductance, MS noise figure and attenuation step.

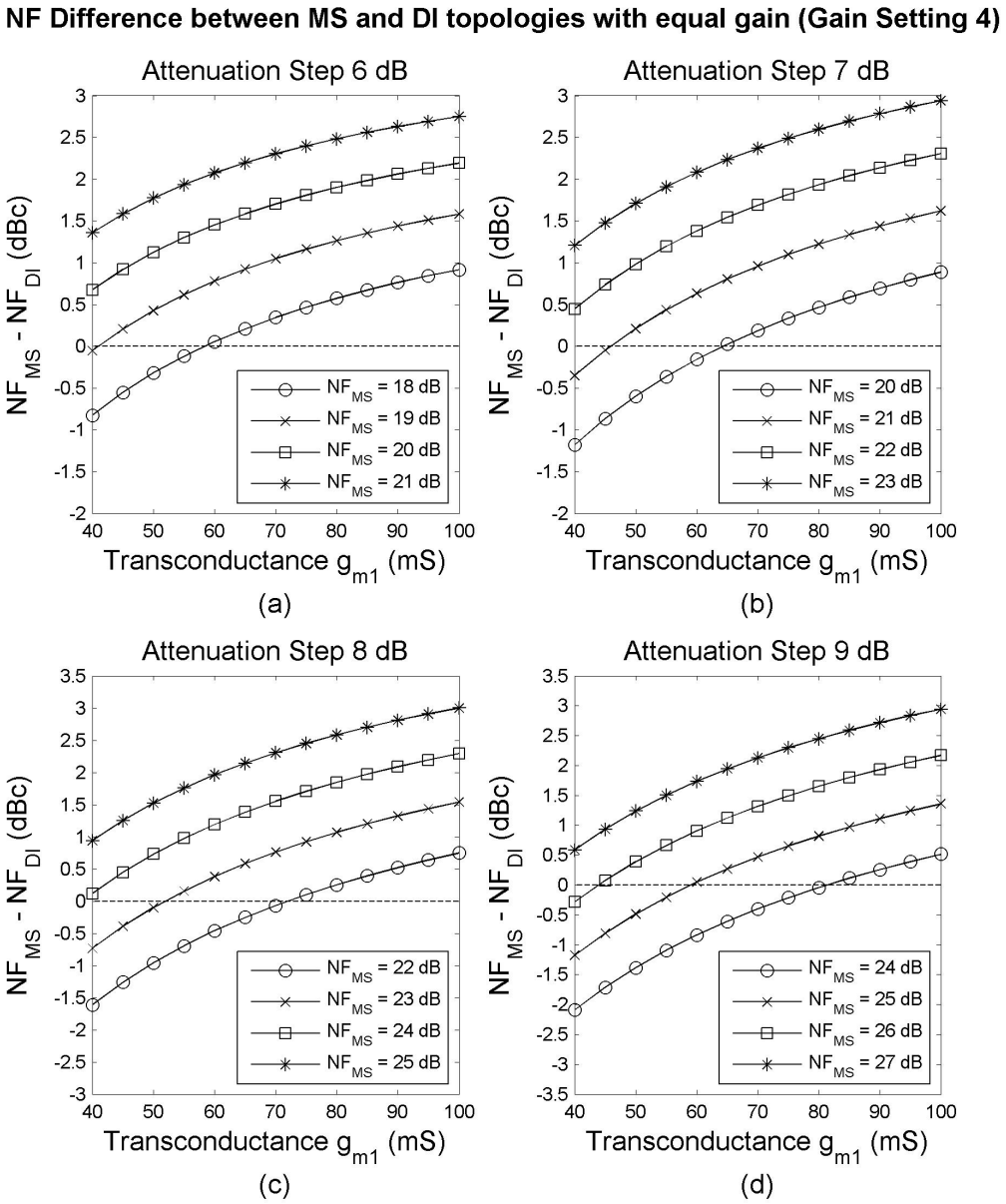

Figure 5.11: Noise figure difference between the MS and the DI topologies (Gain Setting 4) for different values of transconductance, MS noise figure and attenuation step.

Gain Setting	1	2	3	4
s_{11} (dB)	<-12.2	<-13.8	<-15.9	<-15.9
Voltage Gain (dB)	13.4	0.6	-7.9	-16.6
NF (dB)	3.2	10.8	17.7	24
IIP3 (dBm)	-1.8	11.8	20.2	28.9
Power (mW)	24.3	23	23	23
Z_{in} Matching	Active	Passive	Passive	Passive
ON switches	6	1,4,5,7	2,4,5,7	3,4,5,7

Table 5.4: RFPGA Prototype II experimental results.

achieved with current CMOS technologies and power consumption constraints.

Thus, the values for which the MS topology provides better noise figure than the DI topology is for the lower range of transconductances with the lower range of noise figures. The lower range of transconductances is typically not viable in high-frequency inductor-less low-noise amplifiers, and it may not be possible to achieve the lowest values of noise figure with low transconductances. Overall, the DI topology provides better noise figure than the MS topology is most practical implementations.

5.3 Experimental Results

The DI-RFPGA has been fabricated in a 65 nm technology, packaged inside a 40-QFN and measured on PCB. SMD external baluns are used for single-ended to differential conversion, and an on-chip output buffer is used at the output of the front-end to drive the low-impedance load of the measuring equipment. Both baluns and the output buffer have been de-embedded from the presented results. PCB tracks have also been de-embedded using short-open-load-through (SOLT) calibration. The DI-RFPGA occupies a total area of 0.042 mm^2, including DC decoupling capacitors. The very low-area inductor-less designs facilitates the integration of the RF front-end into a complete transceiver SoC. The power consumption varies from 23 mW (at attenuation settings) to 24.3 mW (at highest-gain setting where the active feedback is on) and the bandwidth ranges from 300 MHz to 2.5 GHz.

A summary of the front-end gain settings and measurement results is presented in

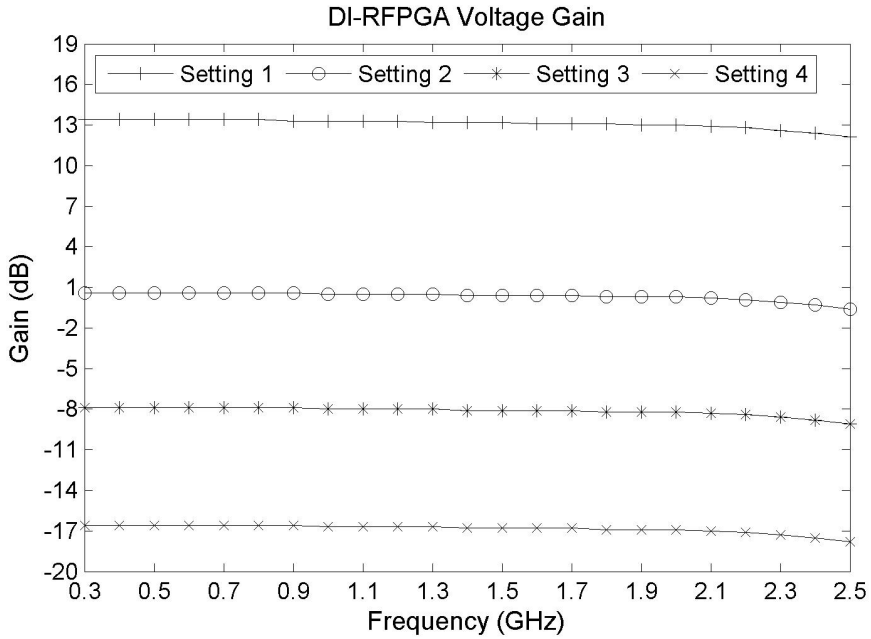

Figure 5.12: DI-RFPGA voltage gain measurement results.

Table 5.4. The front-end achieves a total voltage gain range of 30 dB, with a maximum voltage gain of 13.4 dB and a minimum gain of −16.6 dB, as shown in Fig. 5.12. The s_{11} is below −12.2 dB along the bandwidth (300 MHz — 2.5 GHz) in all operating modes, as shown in Fig. 5.13. Fig. 5.14 shows an IIP3 range of 30.7 dB with a maximum value of 28.9 dBm. The noise figure has a minimum value of 3.2 dB at the maximum-gain setting, as can be seen in Fig. 5.15.

A comparison with other configurable amplifier topologies using input attenuation (either resistive or capacitive) is presented in Table 5.5. The proposed circuit shows a large decrease in chip area with 0.042 mm^2 as compared to 0.25 mm^2, 0.32 mm^2 and 0.325 mm^2 for [106], [8] and [4] respectively. Although our circuit has been fabricated in 65 nm technology, this is still between 6—8 times smaller chip area as compared to 1.4—2.8 shorter length technology.

Also, the presented circuit has an operating frequency up to 2.5 GHz, whereas the other topologies operate up to 1 GHz. In terms of noise figure it is difficult to provide a direct comparison due to differences in structure and bandwidth. The only topology

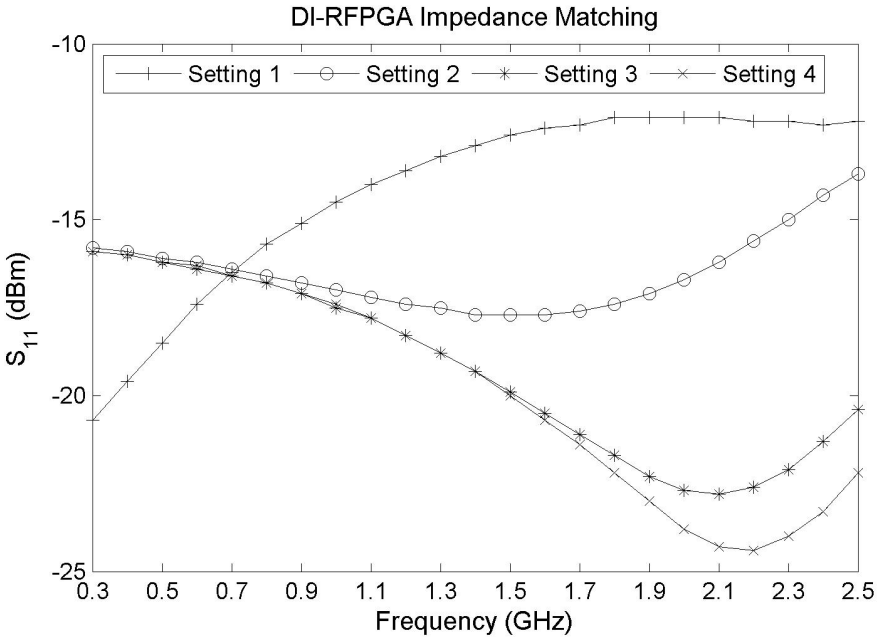

Figure 5.13: DI-RFPGA s_{11} measurement results.

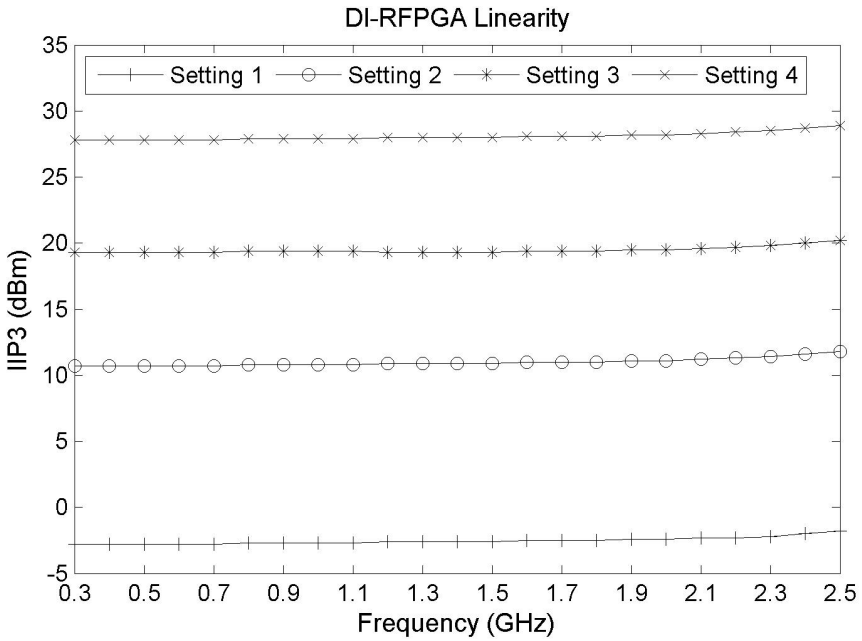

Figure 5.14: DI-RFPGA IIP3 measurement results.

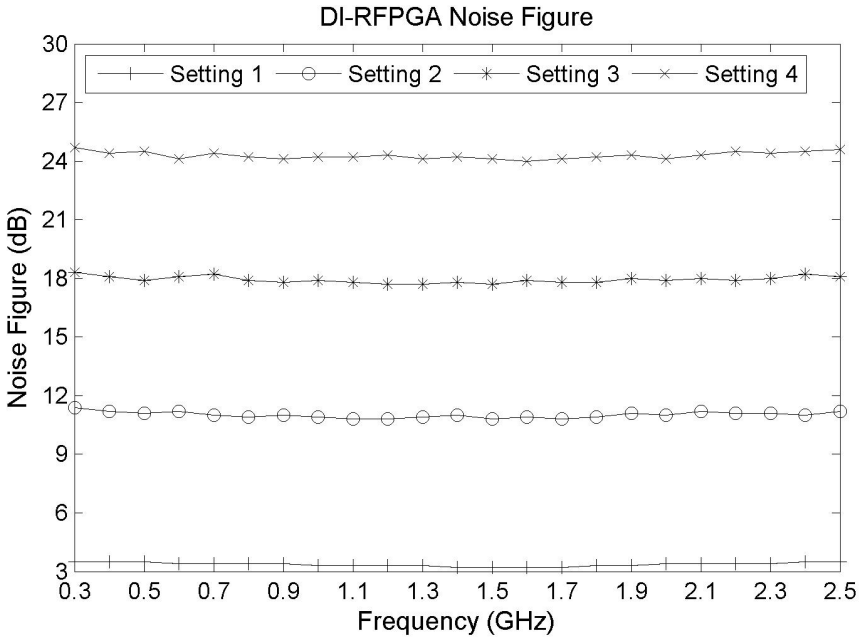

Figure 5.15: DI-RFPGA noise figure measurement results.

besides the one presented in this chapter that is both inductorless and differential is [4], which uses a dedicated non-configurable amplifier optimized for low noise in parallel with the configurable amplifier. [8] and [105] do not use a dedicated amplifier and are inductorless topologies using input attenuation. However, the topologies are single-ended which inherently provide lower noise figure than a differential topology.

Overall, the presented double-input RFPGA topology provides a performance improvement in terms of chip area and bandwidth, while providing comparable performance in terms of noise figure, linearity and power consumption.

5.4 Summary

A wideband inductorless fully differential RFPGA with high dynamic range is presented. The proposed circuit uses a new double-input switchable capacitive attenuation topology and two different input impedance matching topologies. The presented DI-RFPGA maintains the bandwidth and area advantages of the switchable capaci-

Ref.	[106]	[8]	[105]	[4]	[109]	This work
Bandwidth (GHz)	0.47∼0.77	0.47∼0.87	0.05∼0.86	0.048∼1	0.47∼0.856	0.3∼2.5
Voltage Gain Range (dB)	−6∼19.6	−17∼16	−18∼14.4[(3)]	−35∼15.4[(3)]	−25∼25	−16.6∼13.4
Minimum NF (dB)[(1)]	1.69	4.3	2.5	2.4[(4)]	1.6	3.2
Maximum IIP3 (dBm)[(2)]	N/A	27	N/A	30	N/A	28.9
Power (mW)	5.3∼13.9	22	19.8	30.6	46.2	23∼24.3
Area (mm^2)	0.325	0.32	0.663	0.25	1.5	0.042
Inductorless	No	Yes	Yes	Yes	No	Yes
Differential	No	No	No	Yes	Yes	Yes
Process	90 nm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	65 nm

(1) Minimum NF at highest-gain setting
(2) Maximum IIP3 at lowest-gain setting
(3) s_{21}
(4) Uses a dedicated non-configurable amplifier for the highest-gain setting

Table 5.5: DI-RFPGA performance comparison.

tive attenuation presented in Chapter 4 and at the same time reduces the noise at the highest-gain setting by using a double-input topology that eliminates the requirement of a serial switch at the input.

Theoretical analysis shows that the double-input topology can be designed to provide the same gain steps as the single-input switchable capacitive attenuation RFPGA presented in Chapter 4 and the commonly-used non-switchable capacitive attenuation topology. The presented double-input topology also improves the noise figure with equal gain over the non-switchable capacitive attenuation topology at all gain settings for most practical implementation cases.

The DI-RFPGA achieves a total voltage gain range of 30 dB, with a maximum voltage gain of 13.4 dB and a minimum gain of −16.6 dB. The s_{11} is below −12.2 dB along the bandwidth (300 MHz – 2.5 GHz) in all operating modes. The IIP3 range is of 30.7 dB with a maximum value of 28.9 dBm and the noise figure has a minimum value of 3.2 dB at the maximum-gain setting. The DI-RFPGA occupies a total area of 0.042 mm^2, including DC decoupling capacitors. The very low-area inductor-less designs facilitates the integration of the RF front-end into a complete transceiver SoC and the power consumption varies from 23 mW (at attenuation settings) to 24.3 mW (at highest-gain setting where the active feedback is on).

6

Front-End Prototype

6.1 Introduction

This chapter presents the implementation of a full RF front-end providing a total of 8 different gain settings. The input amplifier in the front-end is the DI-RFPGA topology presented in Chapter 5 which provides 4 gain settings by using a double-input topology and a switchable capacitive attenuation circuit. The frequency downconversion is performed by a folded mixer whose transconductance stage can be by-passed. By combining the two methods the front-end provides a total of 8 gain settings. Experimental results of the circuit packaged inside a QFN package and solded on PCB are presented. The chapter is divided in five sections: mixer topology, front-end architecture, circuit design, experimental results and summary.

The mixer topology section starts by explaining the differences between passive and active mixers and justifying the choice for an active mixer, followed by an explanation of the sub-blocks which compose an active mixer and finally proceeds to show how the mixer can be configured to provide different gain settings. This section is then followed by the front-end architecture section which introduces the front-end structure (block diagram) of the manufactured prototype.

Following the presentation of the front-end architecture comes the section that describes in detail the circuits of the front-end blocks. The input amplifier of the front-

end is the double-input RFPGA topology presented in Chapter 5 which has already been analyzed in detail, therefore it is not described in this section. The blocks of the front-end presented in this section are the transconductance amplifier, the switching stage and the buffers.

The next section contains the experimental results of the manufactured front-end. The circuit has been manufactured using a 65 nm CMOS technology, packaged inside a QFN and solded on PCB. Apart from the traditional measures given for any amplifier and front-end, we also provide multi-tone measures that show a more realistic behavior of the circuit linearity in a multiple-carrier wideband application. The chapter ends with a summary section providing an overview of the contents presented.

6.2 Mixer Topology

As has been discussed previously, high dynamic range receivers require both low noise and high linearity although the specifications do not require to be complied with at the same time. When a full front-end with frequency downconversion is taken into account, the decision of which mixer topology is the more adequate arises. Mixers can be classified in two main categories: active and passive. Active mixers are more adequate for small-amplitude input signals as they provide low-noise and high-gain, whereas passive mixers are more adequate for large-amplitude input signals as they provide high linearity.

For the current design, an active mixer topology was chosen since it is more appropriate to comply with the requirements of low-noise and high-gain for the lowest-amplitude input signals (it should be reminded that the higher the gain of the front-end, the less the noise figure of later stages will affect the noise figure of the whole receiver). The structure of an active mixer can be divided into three blocks as shown in Fig. 6.1, which are the transconductance stage, the switching stage and the transimpedance stage.

When using an active mixer topology, the usual problem that arises in high dynamic

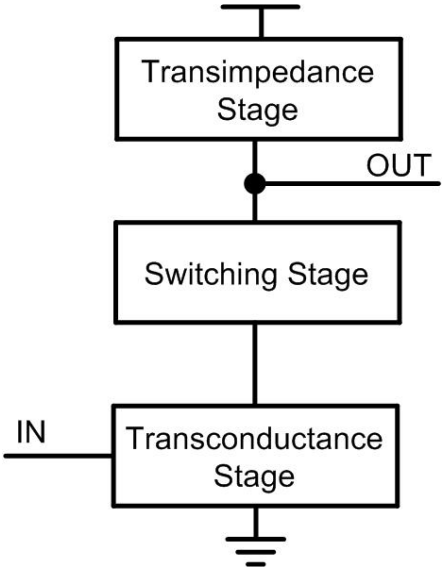

Figure 6.1: Blocks in an active mixer.

range receivers is to comply with the linearity requirements, especially after the LNA has provided amplification. One approach to solve this problem is to use an LNA-less topology, where the LNA stage is eliminated and the received signal enters directly into the mixer stage, which in this case it must be designed to provide input impedance matching. The LNA-less topology, even when using an active mixer, has the disadvantage of higher noise and lower gain, which presents a problem in high dynamic range receivers.

Taking this approach further for configurable high dynamic range front-ends, the receiver can be designed using a by-passable LNA and an active mixer, as shown in Fig. 6.2a. Using this approach, at the highest-gain setting the front-end uses the LNA and mixer, whereas at lower gain settings the LNA can be by-passed and the front-end becomes an LNA-less topology, with the input signal entering directly into the mixer stage. This approach, however, has three important disadvantages:

- If the LNA is designed as a configurable topology providing different gain settings, they can no longer be used as the full stage is by-passed.
- The mixer design must include an input impedance matching circuit for the gain

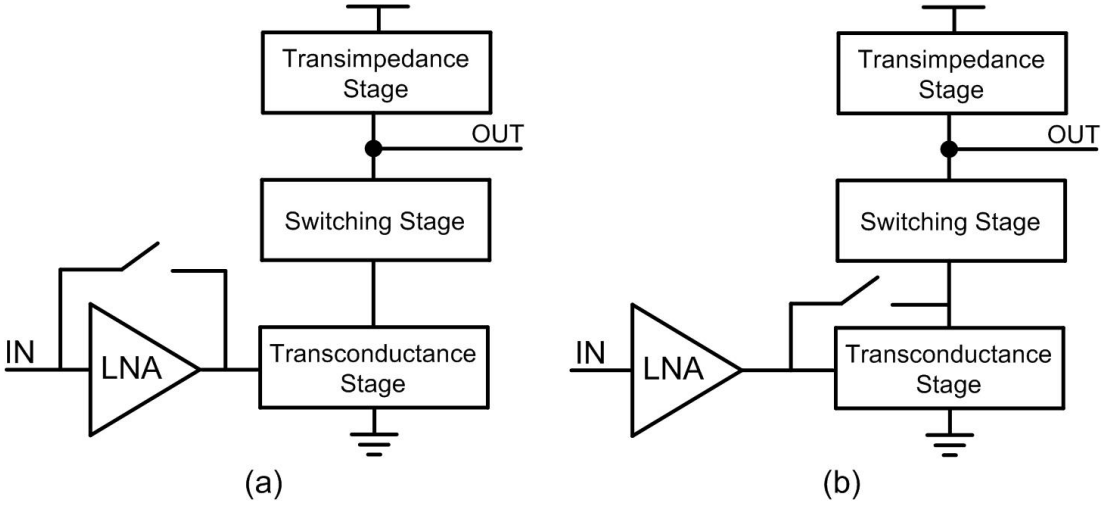

Figure 6.2: (a) Front-end with by-passable LNA and (b) Front-end with by-passable mixer transconductance.

settings where the LNA is by-passed.

- The input switch adds noise that results in a non-negligible increase of the noise figure, as there is no previous amplification. The increase in noise may put further constraints to the noise/linearity trade-off.

In this chapter we propose the use of a front-end architecture that, instead of by-passing the LNA, by-passes the transconductance stage of the mixer and uses the input LNA as the transconductance stage of the mixer as shown in Fig. 6.2b. Therefore, the front-end effectively becomes an LNA-less topology but maintaining the input impedance matching topology and the configurability of the input LNA. Also, the switch is now located at the output of the LNA, and thus it has a much lower influence on the noise figure of the whole receiver as the signal is first amplified by the LNA.

6.3 Front-End Architecture

The implemented front-end architecture is shown in Fig. 6.3. The input LNA of the front-end uses the double-input switchable capacitive attenuation RFPGA presented in Chapter 5 providing 4 gain settings. The DI-RFPGA is followed by a buffer to obtain

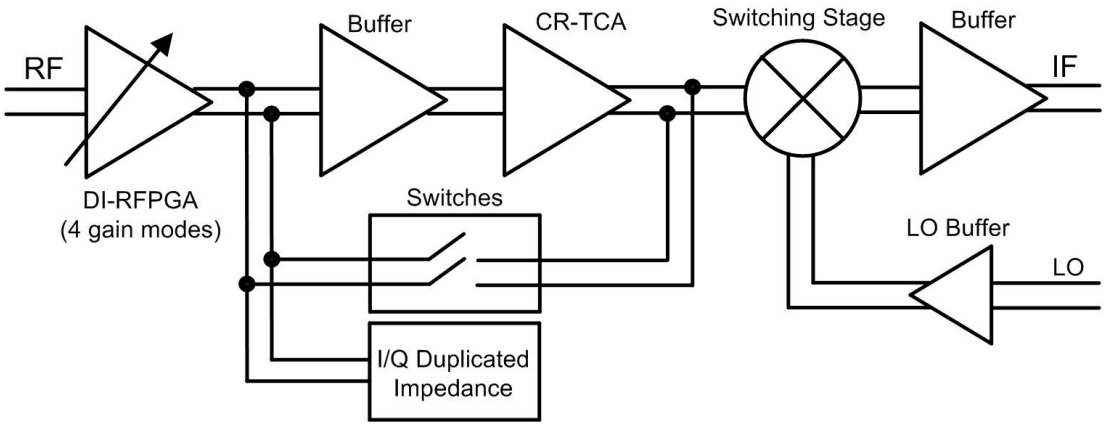

Figure 6.3: Architecture of the implemented front-end.

a better isolation from the LO signal at the mixer stage.

The active mixer uses a folded topology composed of a current re-use transconductance stage (CR-TCA) and a switching stage. As previously mentioned, the transconductance stage of a typical active mixer (which in this front-end design corresponds to the CR-TCA) can be by-passed thus connecting the DI-RFPGA directly to the switching stage and turning the front-end into an LNA-less topology where the DI-RFPGA behaves as the transconductance stage of the mixer. The CR-TCA by-pass adds an additional configuration mode which, combined with 4 DI-RFPGA gain settings, allows the front-end to provide a total of 8 different gain settings.

The function of the buffer at the output of the switching stage is to isolate the mixer from the baseband circuitry and to provide a low capacitive load to the mixer to increase bandwidth, as the G.hn specification establishes channels of up to 200 MHz bandwidth. The LO buffer is used to condition the LO signal to the requirements of the switching stage. In this implementation, the LO signal is fed externally through a signal generator for measurement purposes, whereas in a practical SoC implementation the LO signal would come from a VCO. The switches are implemented using NMOS switches. An additional block is added at the output of the DI-RFPGA to emulate the load seen in a full I/Q receiver where the receiving paths are duplicated beyond the input LNA.

Stage	Power Consumption
DI-RFPGA	23.8 mW
DI-RFPGA Buffer	4 mW
CR-TCA	9.8 mW
Switching Stage	3.2 mW
Switching Stage Buffer	3.1 mW
LO Buffer	3.2 mW
Total	47.1 mW

Table 6.1: Simulated power consumption of each front-end stage.

6.4 Circuit Design

This section presents the various circuits used in the front-end including the current re-use transconductance stage (CR-TCA), the switching stage, the buffers and the by-pass. The DI-RFPGA is not present in this section as the circuit has been analyzed in detail in Chapter 5. For ease of reference along the section, Table 6.1 provides the simulated power consumption of each stage.

6.4.1 Switching Stage

The schematic of the folded mixer is shown in Fig. 6.4, with the switching stage consisting of a double-balanced topology with tail current sources setting the power consumption of the circuit and resistive loads to perform the current-to-voltage conversion. The use of a folded mixer topology allows the use of different currents for the transconductance and switching stages which allows for a better optimization of the circuit, as the transconductance stage requires a high current to provide high gain and low noise, whereas the linearity of the switching stage increases as the current through the switching transistors decreases. The total power consumption of the switching stage is 3.2 mW.

The maximum channel bandwidth defined by the G.hn specification is 200 MHz, and we set the minimum baseband frequency at 10 MHz, therefore the mixer bandwidth must stay between 10 MHz and 210 MHz.

The non-linear time-variant characteristics of a mixer makes the theoretical anal-

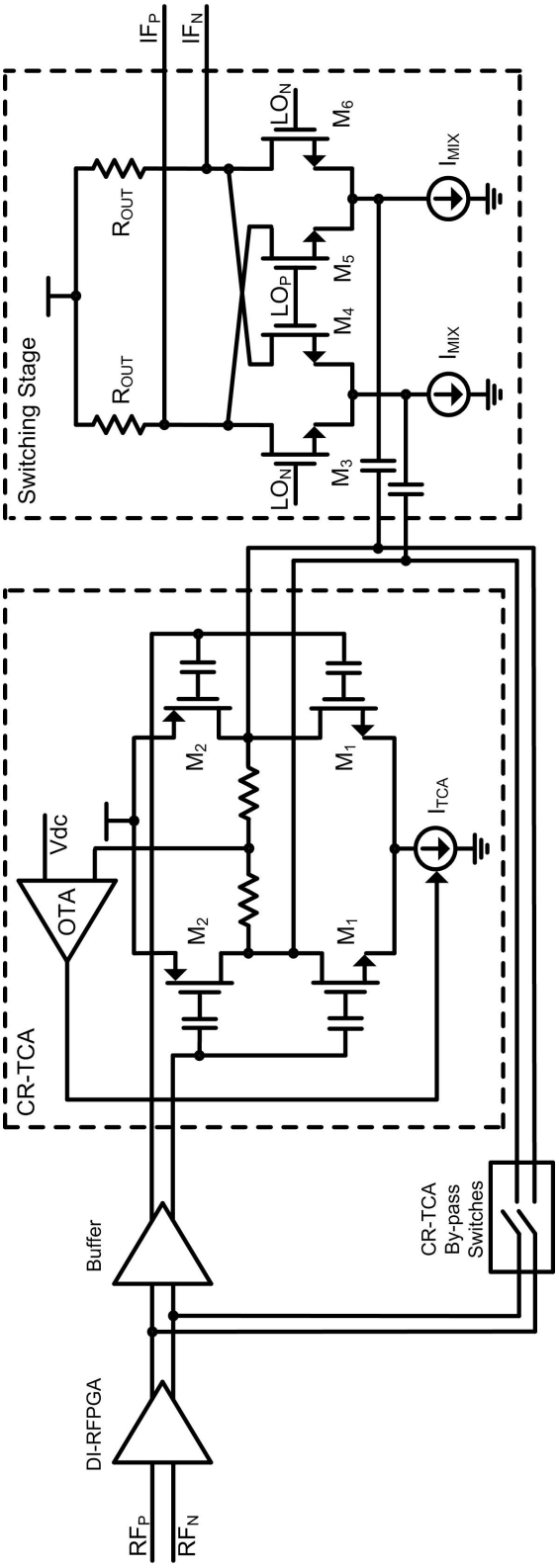

Figure 6.4: Schematic of the CR-TCA and the switching stage.

ysis of the circuit specifications very difficult, requiring the use of Volterra series and several approximations, which is beyond the scope of this thesis. The simulated input impedance of the switching stage for different LO frequencies is shown in Fig. 6.5. The impedance has been obtained using a PSS-PSP simulation. As shown, the impedance value is low, in the range of 100 Ω, which is of the same order as the load resistance R_L of the DI-RFPGA. When the by-pass is not active, the DI-RFPGA sees a large impedance from the following stage (the gate of the buffer's input transistor) whereas when the by-pass is activated, the DI-RFPGA sees a low impedance from the following stage with the same order of magnitude than its load resistance R_L which reduces the gain of the circuit. Thus, when the by-pass is active, the front-end gain is not only lowered by avoiding the CR-TCA, but also by using a lower impedance in the stage loading the DI-RFPGA.

In the measurements, the LO signal is fed externally to the switching stage through an LO driver. Therefore, the LO driver performs input impedance matching to match the output impedance of the signal generator. The LO driver is also in charge of setting the required DC voltage level and amplitude of the LO signal at the output of the driver which is directly connected to the switching transistors. The LO driver is designed as a long-tailed common-source circuit with load resistance and consumes a total of 3.2 mW.

6.4.2 Current Re-Use Transconductance Amplifier

The schematic of the current re-use transconductance amplifier is shown in Fig. 6.4, consisting of a differential NMOS/PMOS structure with common-mode feedback to set the output DC voltage level through the tail current source. The current re-use structure provides higher gain and lower noise figure than a common-source resistive loaded amplifier, therefore this topology is chosen as it allows the front-end to provide a lower noise figure at the highest-gain setting.

The by-pass switches are connected to the output of the CR-TCA, therefore all devices of the transconductance amplifier connected to the output must be powered down during the by-pass settings to provide a high impedance. Then, the only load

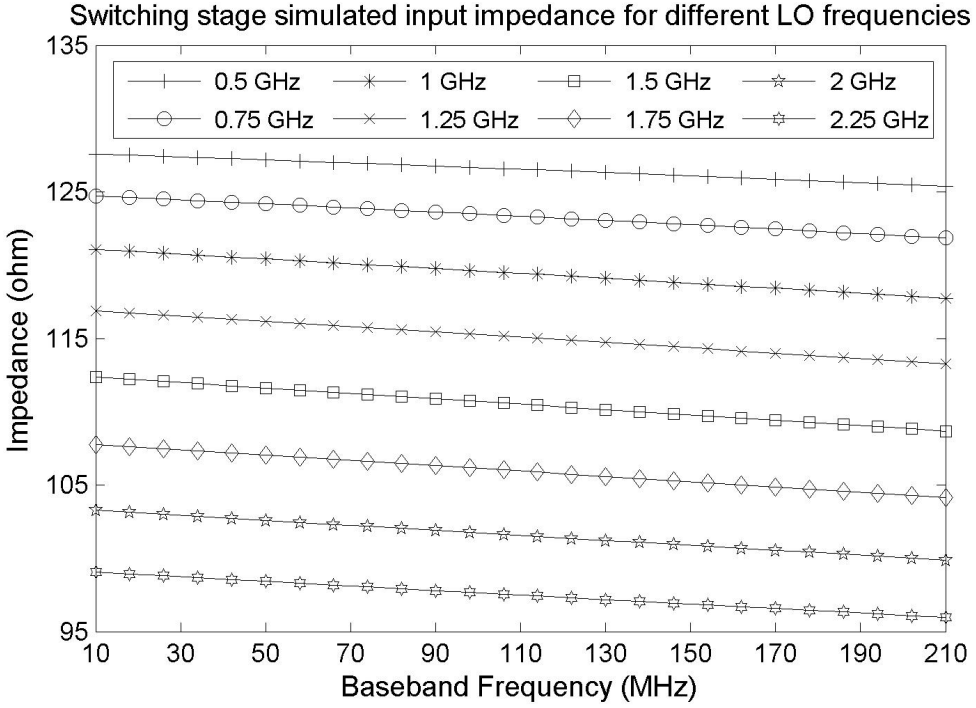

Figure 6.5: Simulated input impedance of the switching stage for different LO frequencies.

impedance seen by the DI-RFPGA is the input impedance of the switching stage as the high output impedance of the CR-TCA can be considered as an open-circuit.

The gain sizing of the CR-TCA depends on how the transition between the different gain settings of the front-end work. The DI-RFPGA standalone provides 4 gain settings with large attenuation steps. The objective when using the by-pass is to provide 4 additional gain settings that are inserted between the gain settings of the DI-RFPGA. as defined in Table 6.2.

When changing from one gain setting to the next the goal is not to provide constant gain steps, but to provide constant SNDR steps as shown in Fig. 6.6. Constant SNDR steps are thus defined as having the same range of input power for each gain setting. When the different gain settings are performed with the same circuit topology by only changing the input attenuation, then constant attenuation steps result in constant SNDR steps, as is the case in the attenuation settings of the DI-RFPGA. However, when the different gain settings are performed with different circuit topologies, con-

Order	DI-RFPGA Gain Setting	By-pass
1	1	No
2	1	Yes
3	2	No
4	2	Yes
5	3	No
6	3	Yes
7	4	No
8	4	Yes

Table 6.2: Order of the front-end gain settings.

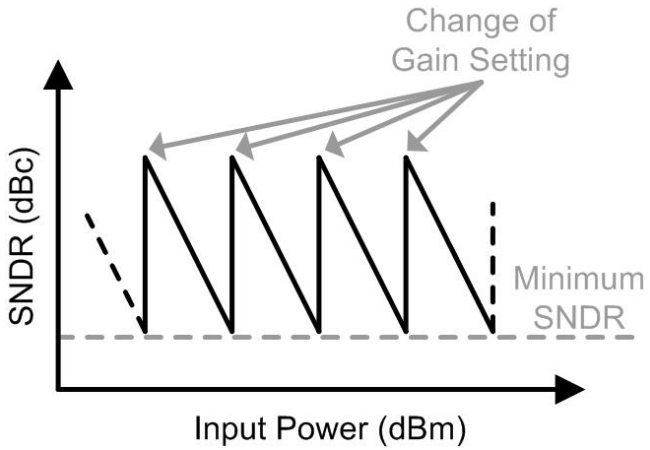

Figure 6.6: SNDR vs input power with constant SNDR steps.

stant attenuation steps may not result in constant SNDR steps as each circuit provides independent specifications of gain and linearity. This is the case for the gain settings of the front-end, where 4 gain settings are provided by changing the input attenuation and the other 4 by changing the front-end topology by-passing the CR-TCA and changing the load impedance seen by the DI-RFPGA. Therefore, when sizing the devices and components in the CR-TCA, it should be done so as to obtain as constant as possible SNDR steps.

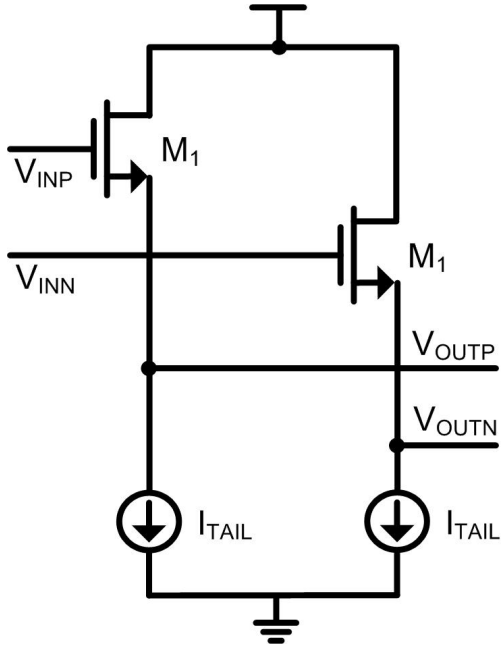

Figure 6.7: Buffers schematic.

6.4.3 Buffers

The buffers used in the front-end are source followers with tail current as shown in Fig. 6.7 and they are used at the output of the DI-RFPGA and at the output of the switching stage. In both cases the buffer isolates the DI-RFPGA and the switching stage from the input capacitance of the following stages, which is of special importance at baseband since the output of the front-end must be able to drive a large capacitance (larger than 4 pF) given the design requirements. The buffers also provide better system stability as source followers provide very good isolation from output to input.

The buffers are designed to provide a high enough linearity so as to avoid affecting the overall front-end linearity and maintaining a reasonable power consumption as compared to the other stages. The sizing of the devices has been done to obtain an IIP3 above 32 dBm with minimum power consumption. The resulting power consumption is 4 mW for the RF buffer and 3.1 mW for the baseband buffer.

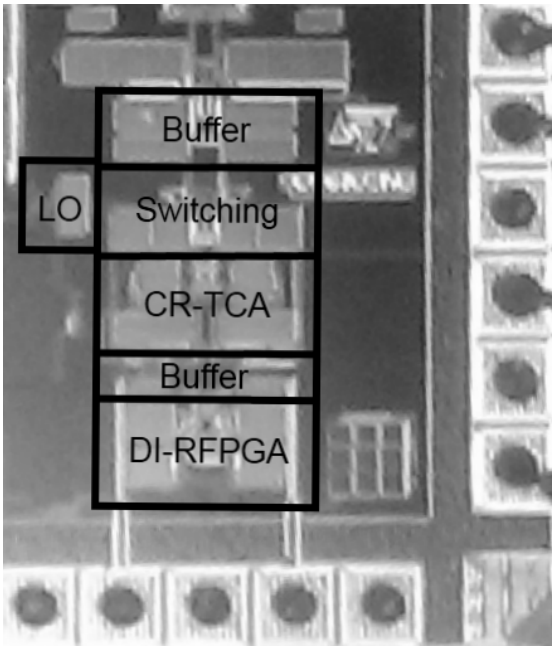

Figure 6.8: Front-end prototype microphotograph.

6.5 Experimental Results

The front-end was fabricated in a 65 nm technology, packaged inside a 40-QFN and measured on PCB. The chip microphotograph is shown in Fig. 6.8. SMD external baluns are used for single-ended to differential conversion, and an on-chip output buffer is used at the output of the front-end to drive the low-impedance load of the measuring equipment. Both baluns and the output buffer have been de-embedded from the presented results. PCB tracks have also been de-embedded using short-open-load-through (SOLT) calibration. The front-end occupies a total area of 0.119 mm^2, including DC decoupling capacitors. The very low-area inductor-less designs facilitates the integration of the RF front-end into a complete transceiver SoC. The power consumption varies from 31.8 mW (at attenuation settings) to 46.8 mW (at highest-gain setting where the active feedback is on) and the bandwidth ranges from 300 MHz to 2.5 GHz.

A summary of the front-end gain settings and measurement results is presented in Table 6.3. The front-end achieves a total voltage gain range of 39.2 dB, with a maximum voltage gain of 25.2 dB and a minimum gain of -14 dB, as shown in Fig.

Gain Setting	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
s_{11} (dB)	<-12	<-9.5	<-13.5	<-13.6	<-15.5	<-15.5	<-15.6	<-15.6
Voltage Gain (dB)	25.2	17.1	13.2	6.9	4	-3.9	-5.9	-14
SSB NF (dB)	5.5	11.1	14.3	19.7	25.3	31.3	33.2	36.2
IIP3 (dBm)	-13.6	-3.9	-1.1	3.6	7.7	13.9	17.9	24.2
Power (mW)	46.8	33.6	45	31.8	45	31.8	45	31.8
Bypass CR-TCA	No	Yes	No	Yes	No	Yes	No	Yes
Z_{in} Matching	Active	Active	Passive	Passive	Passive	Passive	Passive	Passive
ON switches	6	6	1,4,5,7	1,4,5,7	2,4,5,7	2,4,5,7	3,4,5,7	3,4,5,7

Table 6.3: Front-end Prototype experimental results.

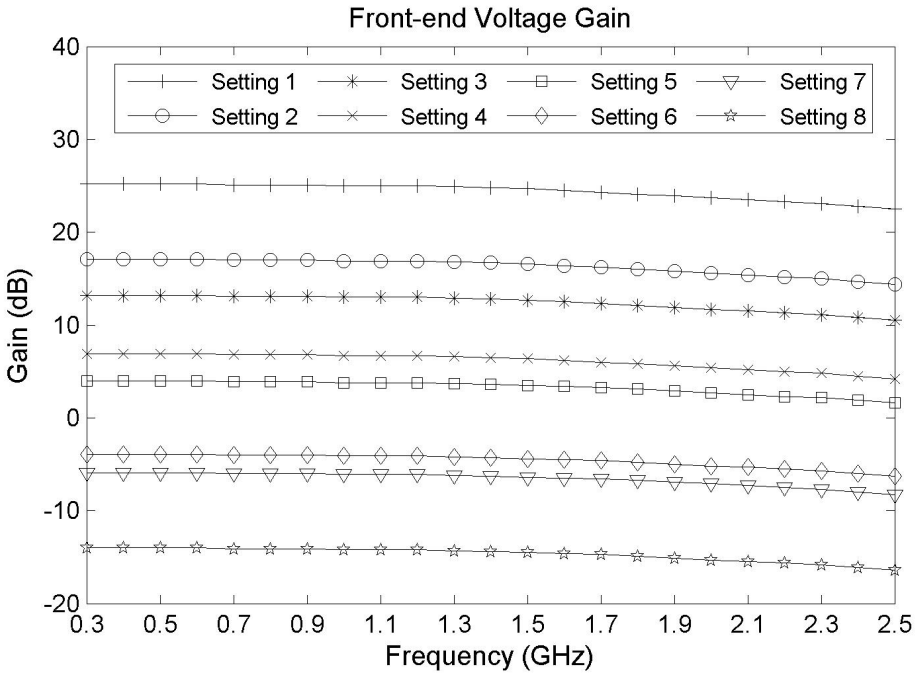

Figure 6.9: Front-end voltage gain measurement results.

6.9. The s_{11} is below -9.5 dB along the bandwidth (300 MHz — 2.5 GHz) in all operating modes, as shown in Fig. 6.10. Fig. 6.11 shows an IIP3 range of 37.8 dB with a maximum value of 24.2 dBm. The single-sideband (SSB) noise figure has a minimum value of 5.5 dB at the maximum-gain setting, as can be seen in Fig. 6.12.

The G.hn specification defines a multiple-carrier system and therefore SNDR measurements with a multiple-carrier input provide a more detailed value of the linearity of the circuit in an application, as the IIP3 measure only uses two input tones. For the SNDR measurements of the front-end we opted for a traditional metric widely used, the noise power ratio (NPR) measurement [23, 24]. The NPR measurement consists in using a multiple-carrier input signal with a single notch at a given point inside the channel and measure the difference between the carriers and the notch at the output. The NPR measures have been performed using the Agilent E4438C ESG Vector Signal Generator [110] and the Agilent Signal Studio for Noise Power Ratio [24]. The latter is a computer software that, through a loop between a computer, the signal generator

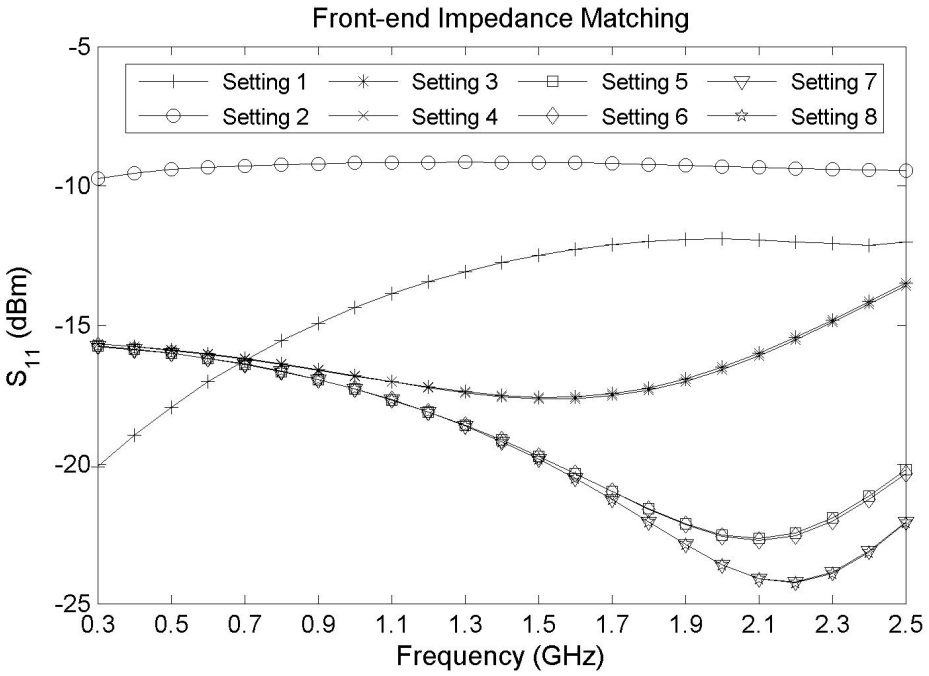

Figure 6.10: Front-end s_{11} measurement results.

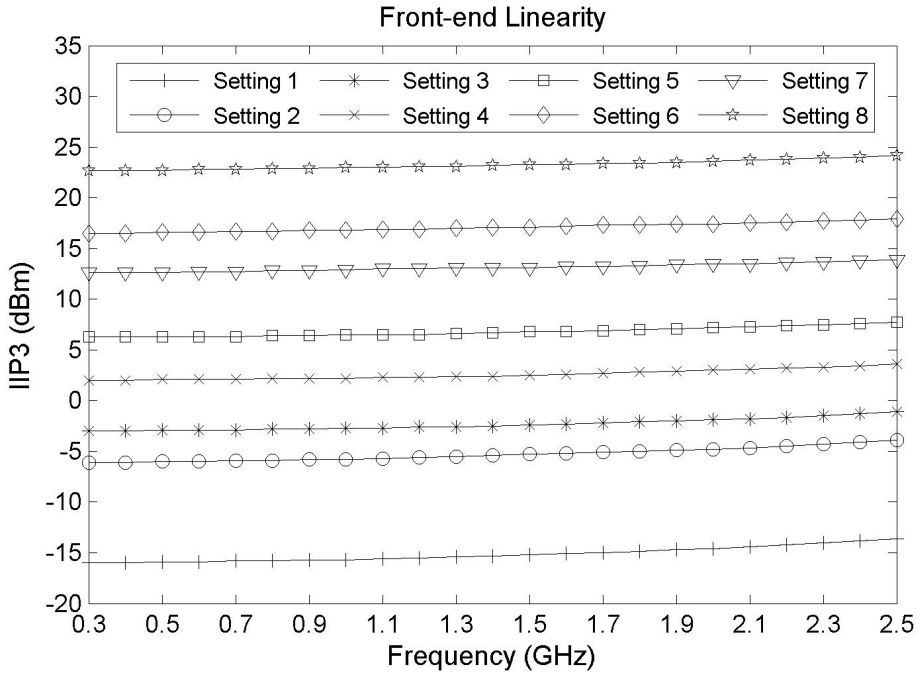

Figure 6.11: Front-end IIP3 measurement results.

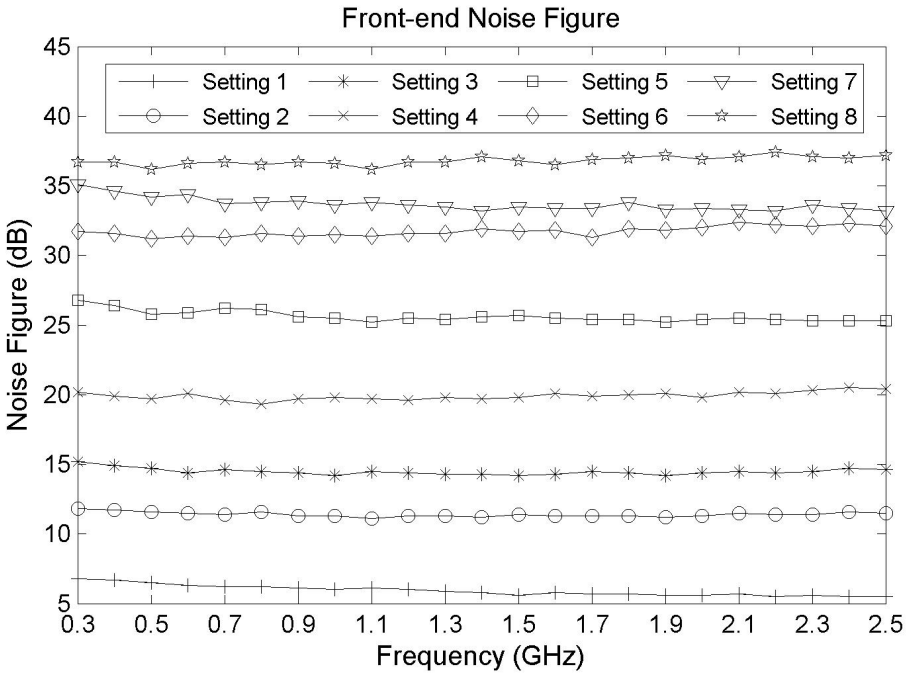

Figure 6.12: Front-end noise figure measurement results.

and a spectrum analyzer, adds pre-distortion to the input signal to obtain higher than -80 dBc notches.

The signal generator is limited to 80 MHz of bandwidth, therefore that is the maximum bandwidth of the generated input signal for the NPR measurements. Each NPR measurement has been performed using a 80 MHz channel bandwidth with 200 kHz carrier spacing, therefore resulting in an input signal with a total of 400 carriers. A frequency sweep for each gain setting has been performed. The NPR measure has been repeated a total of 80 times locating the notch at different frequencies and using random phases for each carrier. The maximum transmitted power defined by the G.hn specification is 8 dBm. In the SNDR measures we use a maximum of 5 dBm power for the input signal, where the 3 dB difference is to account for the minimum losses due to connectors, cables and input diplexer.

The input and output spectra showing the full channel are plotted in Fig. 6.13 and Fig. 6.14 respectively, using 5 dBm input power and the maximum attenuation setting,

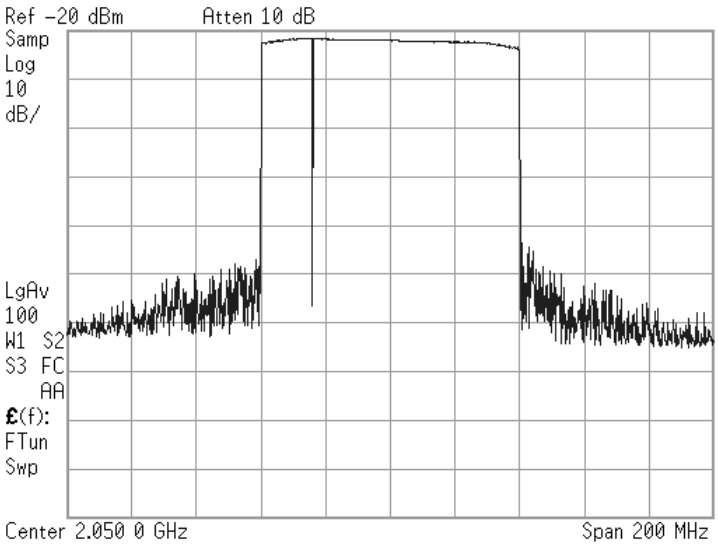

Figure 6.13: Instance of the input signal in an NPR measurement (full channel view). The input signal has a power of 5 dBm and 400 carriers with a 200 kHz spacing centered at 2.05 GHz.

as this is the case which defines the minimum achievable SNDR of the system. It should be noted that the notch value in these plots is higher than the real value, since to plot the entire channel on the screen of the spectrum analyzer requires the use of a high resolution bandwidth. Therefore, the calculation of the power at the notch includes the power of the notch itself and power from the adjacent channels, as the resolution bandwidth is not small enough. These plots are only provided with the intention of showing the full channel and the out of band interferers which, although do not provide exact values, give an idea of the signal PSD shape.

The input and output spectra using a zoom into the channel are shown in Fig. 6.15 and Fig. 6.16 respectively, using 5 dBm input power and the maximum attenuation setting. The figures show a bandwidth of 5 MHz centered at the notch. Using a lower plotted bandwidth allows for a higher resolution bandwidth, and the power at the notch now shows the real value as it does not include power from adjacent channels. The carrier amplitude difference between input and output is larger than the front-end attenuation at gain setting 8 as defined in Table 6.3. This is because, as has been

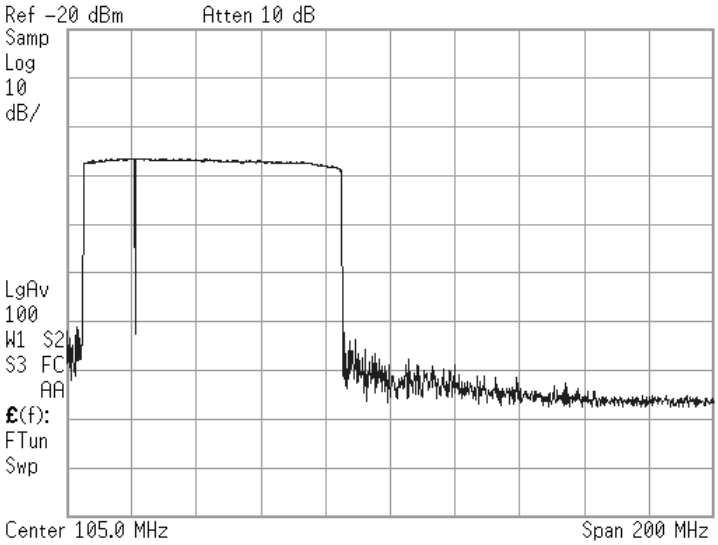

Figure 6.14: Instance of the output signal in an NPR measurement (full channel view). The input signal has a power of 5 dBm and 400 carriers with a 200 kHz spacing centered at 2.05 GHz. The front-end is configured at the lower gain setting with a baseband frequency from 10 MHz to 90 MHz.

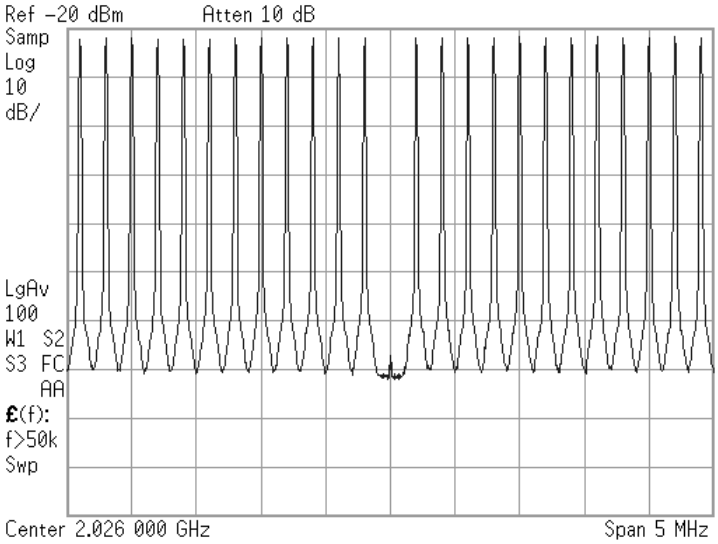

Figure 6.15: Instance of the input signal in an NPR measurement (zoom into the carriers). The input signal has a power of 5 dBm and 400 carriers with a 200 kHz spacing centered at 2.05 GHz with a notch located at 2.026 GHz.

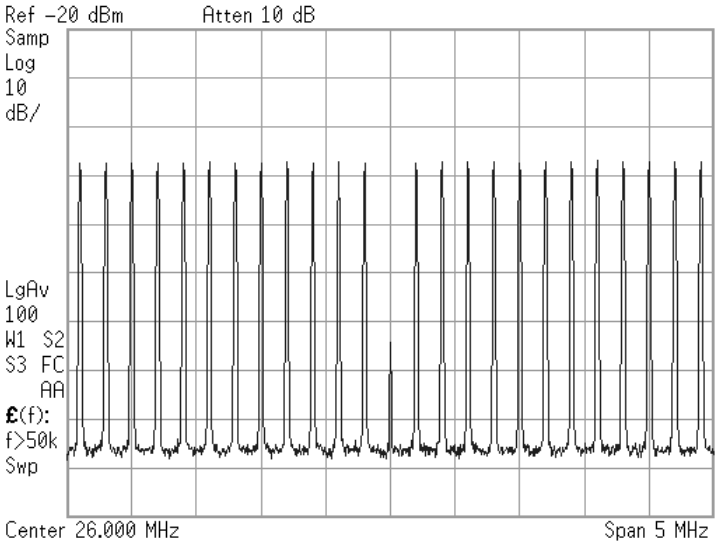

Figure 6.16: Instance of the output signal in an NPR measurement (zoom into the carriers). The input signal has a power of 5 dBm and 400 carriers with a 200 kHz spacing centered at 2.05 GHz. The front-end is configured at the lower gain setting with a baseband frequency from 10 MHz to 90 MHz with a notch located at 26 MHz.

previously explained, the measurement buffer used to drive the 50 Ω measurement equipment has been de-embedded from the gain results, as this buffer is not used in a full SoC product where the front-end will be followed by a high-input-impedance integrated baseband amplifier. The zoomed spectrum figures show that the notch at the input results in a 37 dBc SNDR at the output. Out of the 80 NPR measures at different frequencies, this is the worst measured SNDR value.

Fig. 6.17 shows the evolution of the SNDR through a notch frequency sweep NPR measurement together with the output power versus input power. The minimum value of SNDR was fixed at 37 dBc as this was the worst measured SNDR at maximum input power. Then, once the minimum SNDR was fixed, the SNDR evolution starting at minimum power was measured, switching to the next gain setting as the minimum SNDR was reached.

Fig. 6.18 shows the full channel output spectrum containing all the individual NPR notch measurements. This plot has been created exporting the data points of one NPR

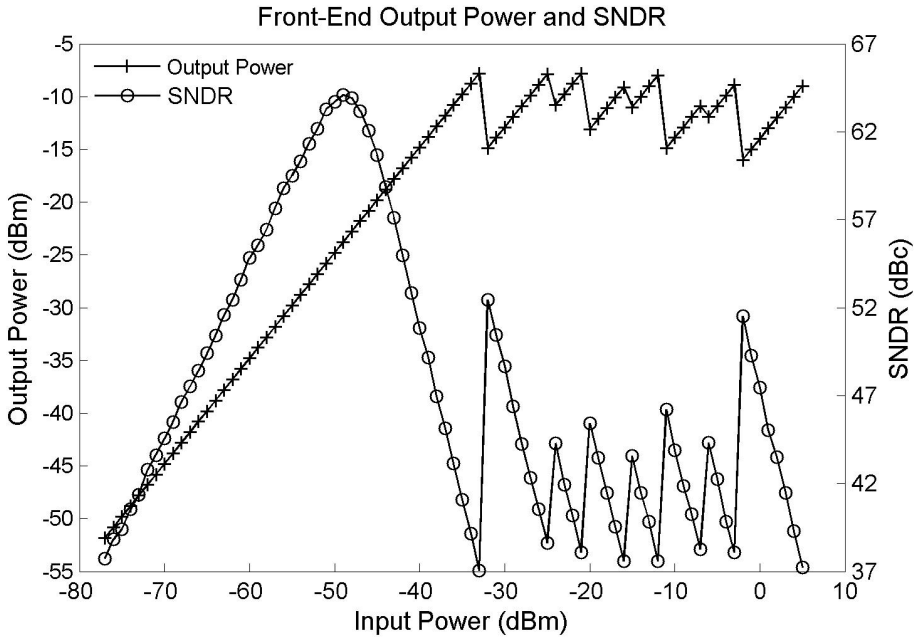

Figure 6.17: SNDR and output power evolution versus input power.

measurement and then adding at the corresponding frequency the notch value measured at each of the 80 NPR measurements. The histogram of the 80 NPR measurements is shown in Fig. 6.19, showing a peak-to-notch with a minimum value of 37 dBc and a maximum value of 55 dBc.

The manufactured front-end achieves the minimum specifications that were specified to comply with the specifications of the G.hn full receiver chain. Table 6.4 shows the required and achieved specifications of the front-end.

6.6 Summary

A wideband inductorless fully differential front-end with high dynamic range is presented. The proposed topology uses the DI-RFPGA presented in Chapter 5 as the input amplifier and a by-passable CR-TCA to provide a total of 8 gain settings. When by-passing the CR-TCA, the DI-RFPGA becomes the transconductance stage of the mixer, thus the front-end behaves as an LNA-less topology.

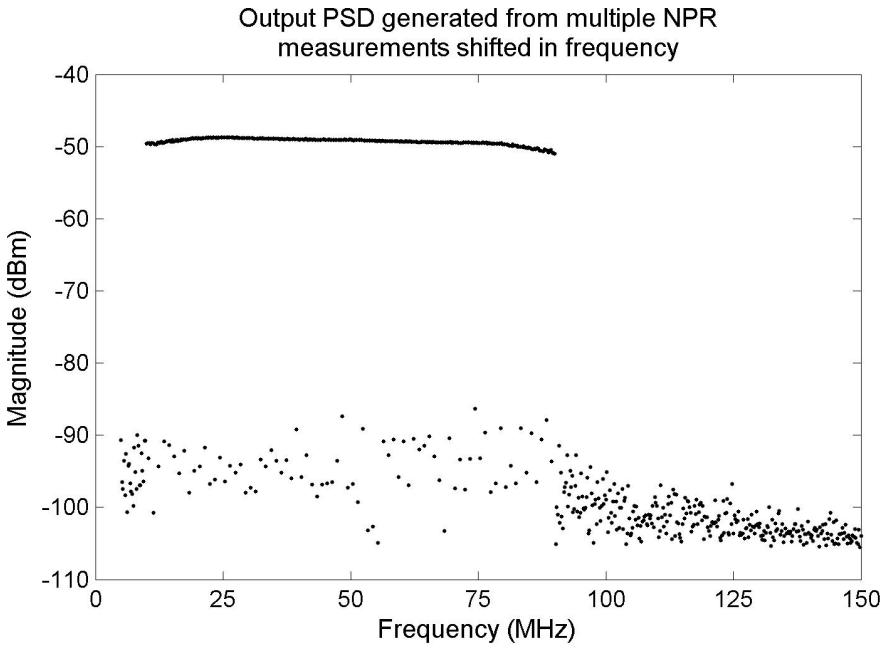

Figure 6.18: Full channel output spectrum containing all the individual NPR notch measurements.

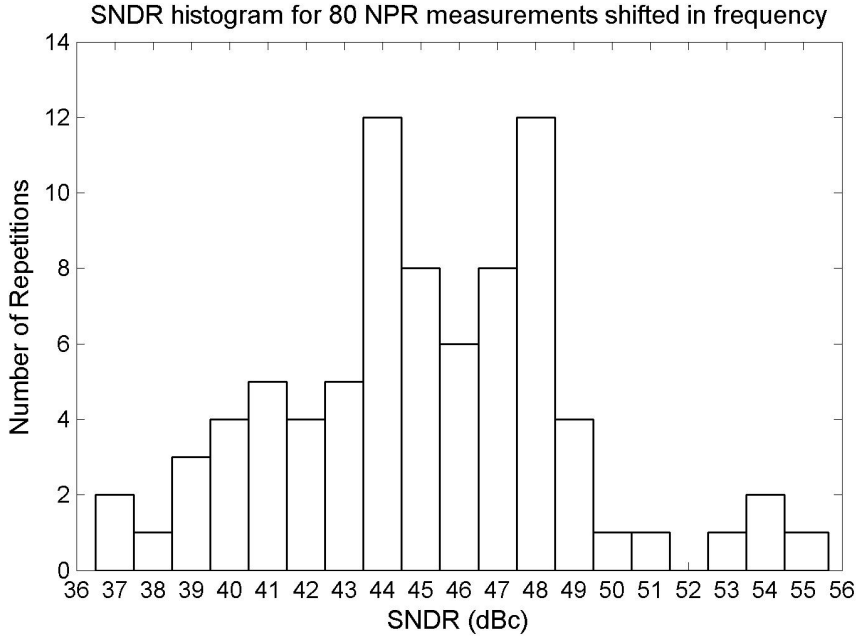

Figure 6.19: Histogram of the NPR notch measurements.

Specification	Required	Front-end
Number of gain settings	8	8
Output voltage (with 12 dB PAR input signal)	$\geq$0.15 V_{pp}	$\geq$0.175 V_{pp}
SNDR	$\geq$35 dB	$\geq$37 dB
Power consumption	$\leq$50 mW	$\leq$47.1 mW
Input power dynamic range	$\geq$80 dB	83 dB
Maximum input power (100 MHz channel)(1)	5 dBm	5 dBm
Maximum input power (50 MHz channel)(1)	2 dBm	2 dBm

(1) Accounts for a minimum loss of 3 dB due to connectors, tracks and diplexer

Table 6.4: G.hn RF front-end specifications.

The front-end achieves a total voltage gain range of 39.2 dB, with a maximum voltage gain of 25.2 dB and a minimum gain of -14 dB. The s_{11} is below -9.5 dB along the bandwidth (300 MHz – 2.5 GHz) in all operating modes. The IIP3 range is of 37.8 dB with a maximum value of 24.2 dBm and the noise figure has a minimum value of 5.5 dB at the maximum-gain setting. The front-end occupies a total area of 0.119 mm^2, including DC decoupling capacitors. The very low-area inductor-less designs facilitates the integration of the RF front-end into a complete transceiver SoC and the power consumption varies from 31.8 mW (at attenuation settings) to 46.8 mW (at highest-gain setting where the active feedback is on). The SNDR of the front-end is 37 dBc when using a 80-MHz 400-carrier input signal with 5 dBm input power.

7

Conclusions and Future Work

7.1 Conclusions

This thesis has been developed in the framework of industry through a joint fellowship provided by Broadcom and the Technical University of Catalonia (UPC), and the work presented has been partly subsidized by the Spanish Ministry of Industry under the Avanza R&D plan with project number TSI-020100-2009-597. The research presented in this thesis has been developed based upon the requirements provided by the company and is focused on the RF front-end part of a receiver for the ITU-T G.hn recommendation (G.9960 [1] and G.9961 [2]) which received final approval in 2010. The recommendation (the ITU's term for standard) defines networking over power lines, phone lines and coaxial cables with data rates up to 1 Gbit/s and contains a bandplan for RF over coaxial cable (RF-coax), where this thesis is focused.

System-on-Chip (SoC) was adopted in recent years as one of the solutions to reduce the cost of integrated systems. When the SoC solution started to be used, the final product was actually more expensive due to lower yield. The developments in integrated technology through the years allowed the integration of more components in lesser area with a better yield. Thus, SoCs have bocame a widely used solution to reduced the cost of the final product, integrating into a single-chip the main parts of a system: analog, digital and memory.

As integrated technology kept scaling down to allow a higher density of transistors and thus providing more functionality with the same die area, the analog RF parts of the SoC became a bottleneck to cost reduction as inductors occupy a large die area and do not scale down with technology. Hence, the trend moves toward the research and design of inductor-less SoCs that further reduce the cost of the final solution.

At the same time, as the demand for home networking high-data-rates communication systems has increased over the last decade, several standards have been developed to satisfy the requirements of each application, the most popular being wireless local area networks (WLANs) based on the IEEE 802.11 standard. However, poor signal propagation across walls make WLANs unsuitable for high-speed applications such as high-definition in-home video streaming, leading to the development of wired technologies using the existing in-home infrastructure. The ITU-T G.hn recommendation (G.9960 and G.9961) unifies the most widely used wired infrastructures at home (coaxial cables, phone lines and power lines) into a single standard for high-speed data transmission of up to 1 Gb/s.

The G.hn recommendation defines a unified networking over power lines, phone lines and coaxial cables with different plans for baseband and RF. The RF-coax bandplan, where this thesis is focused, uses 50 MHz and 100 MHz bandwidth channels with 256 and 512 carriers respectively. The center frequency can range from 350 MHz to 2450 MHz. The recommendation specifies a transmission power limit of 5 dBm for the 50 MHz bandplan and 8 dBm for the 100 MHz bandplan, therefore the maximum transmitted power in each carrier is the same for both bandplans.

Due to the nature of an in-home wired environment, receivers that can handle both very large and very small amplitude signals are required: when transmitter and receiver are connected on the same electric outlet there is no channel attenuation and the signal-to-noise-plus-distortion ratio (SNDR) is dominated by the receiver linearity, whereas when transmitter and receiver are several rooms apart channel attenuation is high and the SNDR is dominated by the receiver noise figure. The high-dynamic-range specifications for these receivers require the use of configurable-gain topologies that can

Specification	Required	Front-end
Number of gain settings	8	8
Output voltage (with 12 dB PAR input signal)	≥0.15 V_{pp}	≥0.17 V_{pp}
SNDR	≥35 dB	≥37 dB
Power consumption	≤50 mW	≤47.1 mW
Input power dynamic range	≥80 dB	83 dB
Maximum input power (100 MHz channel)(1)	5 dBm	5 dBm
Maximum input power (50 MHz channel)(1)	2 dBm	2 dBm

(1) Accounts for a minimum loss of 3 dB due to connectors, tracks and diplexer

Table 7.1: G.hn RF front-end specifications.

provide both high-linearity and low-noise for different configurations.

Thus, this thesis has been aimed at researching high dynamic range broadband inductor-less topologies to be used as the RF front-end for a G.hn receiver complying with the provided specifications. The main specifications of the RF front-end and the achieved results with the manufactured front-end are listed in Table 7.1.

A large part of the thesis has been focused on the design of the input amplifier of the front-end, which is the most critical stage as the noise figure and linearity of the input amplifier define the achievable overall specifications of the whole front-end. Three prototypes have been manufactured in two different runs using a 65 nm CMOS process: two input RFPGAs and one front-end using the second RFPGA prototype.

The first RFPGA prototype is a fully-differential two-stage configurable pre-attenuation based amplifier providing 4 different gain settings. The pre-attenuation circuit uses a new switchable capacitive attenuation topology that increases bandwidth and reduces chip area over a traditional non-switchable capacitive attenuation topology. One of the gain settings is provided by by-passing the second amplifier, whereas the other 3 gain settings are provided by using a switchable capacitive attenuation topology at the input. The RFPGA uses 2 different methods of input impedance matching. The prototype has been fabricated in a 65 nm CMOS technology, packaged inside a QFN and measured on PCB.

The second RFPGA prototype is a fully-differential double-input configurable pre-attenuation based amplifier providing 4 different gain settings with a single stage using

a switchable capacitive attenuation topology. This topology proposes a new structure using double-input and switchable capacitive attenuation topology to increase the bandwidth, decrease the chip area and decrease the noise figure over a traditional non-switchable capacitive attenuation topology. The RFPGA uses 2 different method of input impedance matching. The prototype has been fabricated in a 65 nm CMOS technology, packaged inside a QFN and measured on PCB.

The front-end prototype has been designed using the double-input (DI) RFPGA presented in Chapter 5 as the input amplifying stage. The mixer uses a folded topology composed of a current re-use transconductance amplifier (CR-TCA) and a switching stage. The CR-TCA can be by-passed thus connecting the DI-RFPGA directly to the switching stage, providing another method of configuration. Therefore, the front-end provides a total of 8 different gain settings. The prototype has been fabricated in a 65 nm CMOS technology, packaged inside a QFN and measured on PCB. A summary of the front-end gain settings and measurement results is presented in Table 7.2.

Overall, the two fabricated chips which included three different prototypes have been successful, providing accurate results in the experimental measures relative to the schematic simulations. Also, the front-end prototype complies with the minimum specifications provided by the company.

7.2 Future Work

Although the presented work is rather thorough, there are some issues that can be addressed to provide a more complete work in regards to the commercial implementation of the proposed front-end.

The proposed topologies have been simulated using a large range of temperatures and Monte-Carlo analysis to ensure that a large percentage of the fabricated chips comply with the specifications. However, the designs do not include circuitry to compensate for Process Voltage Temperature (PVT) effects. The inclusion of PVT-compensating circuits that make the proposed design more robust, reduce the variations in specifica-

Gain Setting	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
s_{11} (dB)	<-12	<-9.5	<-13.5	<-13.6	<-15.5	<-15.5	<-15.6	<-15.6
Voltage Gain (dB)	25.2	17.1	13.2	6.9	4	-3.9	-5.9	-14
SSB NF (dB)	5.5	11.1	14.3	19.7	25.3	31.3	33.2	36.2
IIP3 (dBm)	-13.6	-3.9	-1.1	3.6	7.7	13.9	17.9	24.2
Power (mW)	46.8	33.6	45	31.8	45	31.8	45	31.8
Bypass CR-TCA	No	Yes	No	Yes	No	Yes	No	Yes
Z_{in} Matching	Active	Active	Passive	Passive	Passive	Passive	Passive	Passive
ON switches	6	6	1,4,5,7	1,4,5,7	2,4,5,7	2,4,5,7	3,4,5,7	3,4,5,7

Table 7.2: Front-end Prototype experimental results.

tions and are capable of working along all the frequency range should be addressed.

The front-end design uses additional circuitry to replicate the impedance seen by the input amplifier when using an I/Q topology. A complete front-end for commercial implementation requires the design of the VCO and I/Q generation circuits as well as the analysis of mismatch between the two branches.

Also, since the circuits fabricated in this thesis are to be included in a complete SoC using digital blocks, analog blocks and memory, a detailed analysis of the effect of substrate noise and signal coupling due to the other chip blocks is required, as well as proposing mechanisms that make the fabricated designs more robust to those effects.

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