Strategies to enhance the 3T1D-DRAM cell variability robustness beyond 22 nm

E. Amat, C.G. Almudéver, N. Aymerich, R. Canal, A. Rubio

Abstract: 3T1D cell has been stated as a valid alternative to be implemented on L1 memory cache to substitute 6T, highly affected by device variability as technology dimensions are reduced. In this work, we have shown that 22 nm 3T1D memory cells present significant tolerance to high levels of device parameter fluctuation. Moreover, we have observed that when variability is considered the write access transistor becomes a significant detrimental element on the 3T1D cell performance. Furthermore, resizing and temperature control have been presented as some valid strategies in order to mitigate the 3T1D cell variability.

Keywords: Variability, DRAM, Temperature

1. Introduction

Nowadays, the variability influence on device behavior is well reported as one of main drawbacks for electronic devices in nano- meter regime [1], since it leads to a worsening system behavior. Several types of variability coexist, such as Random Doping Fluctua- tion (RDF), Line Edge Roughness (LER), but RDF has the largest impact on bulk CMOS devices performance [1] as it causes the largest threshold voltage (V_T) fluctuation and consequently supposes a deterioration circuit in behavior.

Indeed, memory systems are obviously affected by this varia- bility, and the well established 6T-SRAM cells [2,3] are highly influenced, because a relevant performance lost is manifested in speed reduction and cell instability [3,4]. In this sense, the 3T1D-DRAM is a promising memory cell to substitute it in Very Large System Integration (VLSI) systems. Although, this cell is also affected by the process fluctuations, they do not necessarily impact the operating frequency, unlike 6T [3]. Moreover, 3T1D provides extra benefits: smaller cell area, the non-destructive read process (in contrast to other DRAMs), and large retention time. Thus, the 3T1D-DRAM cell is presented as a suitable memory cell for L1 memory caches [3,5]. In this context, fast access times are required and low retention times are architecturally masked [6]. Note that 3T1D cell is a Dynamic RAM, thus, the memory storage node is a capacitor (the gate capacitance in the gated-diode) and it temporarily stores the data. In order not to lose the contents, a periodic refresh is required to hold data for extended periods [3]. On the other hand, the constant dimension reduction of technologies produces an intolerable increase of leakage current and electric field present in devices. This implies lower carrier mobility and worse reliability [7]. To overcome this problem, the introduction of devices based on high-k dielectrics is a feasible option and it has also allowed a better 3T1D performance beyond 65 nm technology node [2] due to the reduction of the leakage currents. In addition, the introduction of strained channel devices [8] improves carrier mobility.

As a consequence, in this work we carry out an analysis of the variability influence on 3T1D cells for technologies beyond 22 nm node. This work is organized as follows. Section 2 describes the cell scheme and its main parameters analyzed during this work. Moreover, different simulation scenarios (variability and tempera- ture) are carried out. Section 3 illustrates the influence of the device variability on 3T1D-DRAM cell. Furthermore, Section 4 reports some strategies to mitigate the memory cell variability. Next, Section 5 pointed out the performance of a 2 kB memory block when it is based on 3T1D-DRAM cells and it is subjected to variability and high environment temperature. Finally, Section 6 discusses the conclusions obtained from this study about the 3T1D performance.

2. Simulation framework

The schematic structure for a 3T1D-DRAM memory cell is illustrated in Fig. 1. This cell has been simulated using the 22 nm High Performance Predictive Technology Model (HP PTM) [9]. We have implemented the memory cell using the 2.1 PTM models, which it is based on high-k materials as a gate dielectric and with

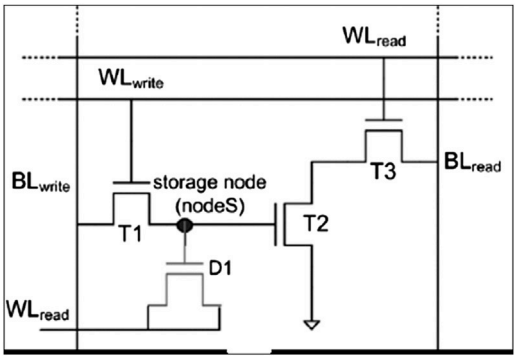


Fig. 1. Schematic structure for a 3T1D-DRAM memory cell. WL: wordline, BL: bitline.

Table 1
Variability scenarios and levels considered for each technology used along this work. (n not considered)

Levels	22 nm	16 nm	13 nm
Moderate (M)	8%	10%	n
High (H)	15%	20%	n
Very high (VH)	30%	40%	58%

strained channel. This involves what involves a lower relevance of the leakage current [10] and higher carrier mobility [8], respec- tively. It is worth noting that the optimal dimensions of all the cell
devices have been extracted from Ref. [4], and a supply voltage (V_{DD}) of 1 V has been applied throughout all this study. Moreover, for comparison, the 3T1D memory cell has been also simulated using two other device models: 16 nm HP PTM [9] and 13 nm TRAMS project model [11]. Note that, all the analysis performed during this work focuses on the following 3T1D-DRAM cell parameters:

(a) *Write Access Time* (WAT) defined as the time elapsed between $V(WL_{write}) ¼ 0.5V_{DD}$ and $V(S) ¼ 0.9(V_{DD} - V_T)$.
(b) *Read Access Time* (RAT) defined as the time elapsed between $V(WL_{write}) ¼ 0.5V_{DD}$ and $V(BL_{read}) ¼ 0.9V_{DD}$.
(c) *Dynamic Power consumption* (PW) obtained by

In order to study the impact of the devices fluctuation on the 3T1D cell parameters, 10,000 Monte Carlo simulations have been performed. The variability influence has been reflected into a variation of the threshold voltage of the on memory cell devices [7]. Table 1 depicts the

we simulate the impact of different variability levels (Table 1), and compare to a non-variability scenario. In this context, Fig. 2 shows how the different level of fluctuation affects the retention time performance. In this sense, the very high process variation level (VH)

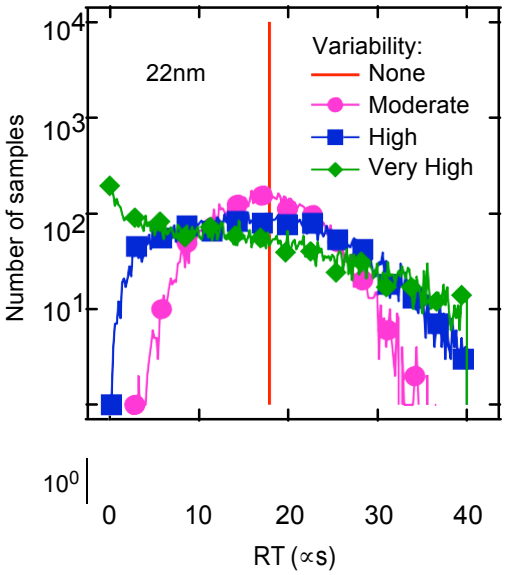
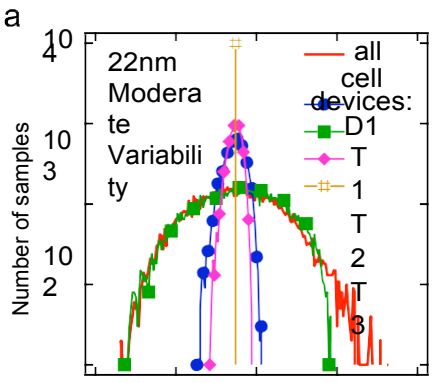


Fig. 2. Influence of the variability on cell performance represented by RT results. The largest fluctuation level means higher impact on cell behavior. These results are obtained for 22 nm cell devices, but similar effect is observed for smaller technologies.



variability levels assumed during this study for all technologies, following TRAMS project statement [
The Gaussian distribution will be spread as the variability level rises and for all the tables the fluctuatic will be analyzed by the 3s/m ratio, expressed as a percentage.

Finally, the influence of the environment tempera

on the 3T1D memory cell behavior has been analyzed as well. For this, the temperature is raised up to 100 1C.

3. Variability influence on 3T1D-DRAM cells

So as to observe the influence of device parameters fluctuation (V_T-variation) on the performance of a 22 nm 3T1D-DRAM memory,

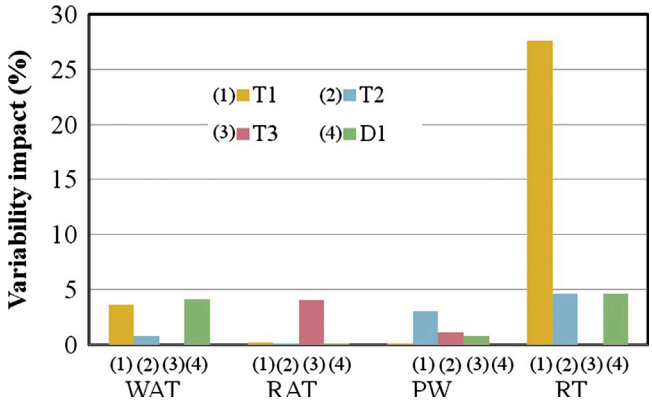


Fig. 3. (a) Influence in RT of each individual transistor on the global cell perfor- mance, based on 22 nm, under a moderate variability. The impact of each device's fluctuation (lineþ symbols) is compared with the observed when all devices present the same variability level (line). (b) Influence on every cell parameter of each 3T1D- DRAM cell transistor variability on global cell behavior. T1 presents the highest impact on retention time (For interpretation of the references to color in this figure, the reader is referred to the web version of this paper.).

presents the largest impact in the analyzed cell parameters, as it is expected. Moreover, the retention time is the cell parameter sub- jected to highest variability relevance.

In order to analyze the previous results in depth, we also study the impact produced by the variability of each individual transistor on the global circuit behavior. For instance, the scenario has been defined in a 3T1D cell based on 22 nm devices with a moderate variability. To do this, we introduce V_T-fluctuation to just one cell device at a time. Fig. 3a compares the global process variation obtained for the retention time, when all devices endure the same level of variability (line) and when only one cell device fluctuates (line þsymbols). In this sense, we observe that the overall cell fluctuation is highly influenced by the variability in T1, since this exhibits the widest distribution (highest impact). Furthermore, Fig. 3b depicts the impact of the variability of each device on the cell's parameters and the highest T1 impact on RT is confirmed, along with a high impact of T1 and D1 on WAT. Hence, the variability in T1 presents the highest impact on the overall cell performance, since it alters the two main 3T1D cell parameters (WAT and RT).

The variability impact on different technologies (22 nm, 16 nm and 13 nm) has been studied in the following paragraphs. But, first, it is worth noting that we have observed a malfunction on 3T1D cell when logic '1' is stored and the technology node is reduced below 22 nm and a very high variability level has been assumed. In this context, Fig. 4a shows that about '" 4% of the 3T1D samples become inoperative, since the stored data are lost when no voltage is applied. For 16 nm and 13 nm, T1 has shown again a high influence on 3T1D cell performance, and it seems to be more critical on the cell behavior than the gated diode [2] for the sub-22 nm nodes. These sub-22 nm examples demonstrate a large susceptibility to variability in T1, since V_{T1} is reduced to very

Fig. 4. Performance of the V_S, during a '1' write operation, obtained from 10,000 Monte Carlo simulations when the 3T1D-DRAM cell is subjected to two scenarios: (a) when a 3T1D cell is based on 22–16–13 nm technology dimensions. Note that a cell malfunction is observed for the smaller nodes when WLw and BLw are not activated. Then, V_S discharge is obtained, due to the small V_{T1} value [12]. (b) When very high variability level only affects one cell device at a time, based on 13 nm node. The variability introduced in T1 is the only one that involves a significant cell malfunction, since the other cell devices show non-significant influence on the overall cell performance.

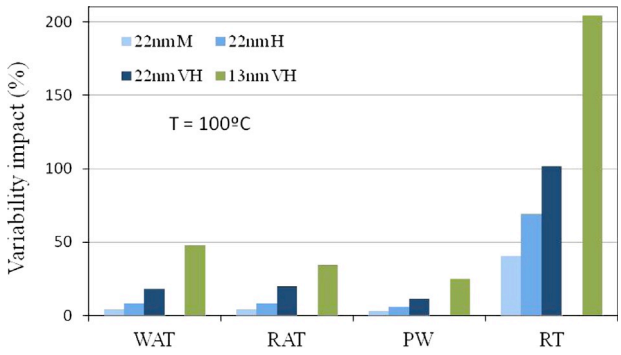
Table 2
Variability impact on 3T1D-DRAM cell parameters for different technologies (22, 16 and 13 nm). Smaller node larger parameter variation.

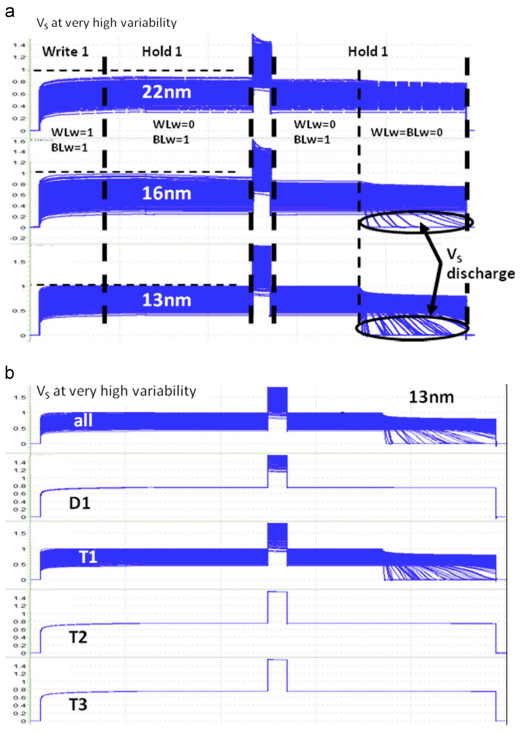
3r/l (%)	Moderate (M)		High (H)		Very high (VH)	
	22 nm	16 nm	22 nm	16 nm	22 nm	16 nm
	22 nm	16 nm	13 nm			
WAT	5.5	6.8	10.4	16	23	40.2	47.3
RAT	4	6.7	7.8	16.9	19.8	32	37.9
PW	3.3	4.4	5.8	10.7	11.3	19	22.2
RT	29.3	33.2	48	59.3	79	101	130

Table 3
Variability impact on a 3T1D cell performance, for 22 nm and 13 nm technologies, when T1 width (W) is enlarged. Larger T1 width results in a lower variability impact on the overall cell behavior.

3r/l (%)	22 nm				13 nm			
	Moderate		High		Very high		Very high	
	2	4	2	4	2	4	2 W	4
WAT	5.3	5.4	10	9.6	21	20	45	42
RAT	4	4	7.9	7.9	18	19	32	32
PW	3.1	2.5	5.5	4.9	11	11	18	15
RT	20.5	16.5	37.7	31.6	71	65.6	110.1	96.4

low values [12], and as a consequence V_S discharges. Thus, storing logic '1' is impossible (i.e. cell fault). To demonstrate it, Fig. 4b shows V_S evolution for a 3T1D cell based on 13 nm node when a high variability is introduced only at one device at a time. Note that the same performance has been observed for cells based on 16 nm devices as well. In this context, we observe that T1 device is the main device that causes the 3T1D-DRAM final bad perfor- mance, since the other cell devices (T2, T3 and D1) do not present any faulty behavior. This result also confirms that the write access transistor (T1) presents a high influence on the global 3T1D memory cell reliability, when the device variability is considered, in contrast to the previous statement od the gate-diode as the principal one at performance level [14]. So then,





taking away the faulty cells, Table 2 shows the impact of variability in sub-22 nm memory cells. The results depict a high increase of the variability as the size of the technology is reduced, as it is expected, and
retention time gets the biggest hit. Furthermore, higher variability level also represents larger amount of cell parameter fluctuation, as it is expected.

4. Mitigation techniques to reduce variability

The process variability has been usually shown to be a detri- mental factor for sub-22 nm 3T1D cells. In this sense, strategies to mitigate the variability are necessary, and thus, in this work, we present two possible solutions in the following sections.

4.1. *T1 resize to mitigate cell variability*

In order to mitigate the effects of variability on 3T1D memory cells, and also to reduce the previous observed cell malfunction, one option could be to increase the dimensions of T1, since we have previously determined this as the most critical cell device in a variability scenario. Then, upsizing T1 dimensions' could reduce the variability impact on the cell performance [15]. Consequently, we have implemented the well-known higher impact of the width resize on device performance [16,17] only on T1. Therefore, the width of cells based on 22 nm and 13 nm nodes will be enlarged by 2 x and 4 x , with an obvious increase of area overhead assumed in order to improve the device robustness against variability. For this, Table 3 demonstrates that this slight device area increase has involved promising results for both technologies. Thus, we could observe that the variability impact on 3T1D cell behavior has been reduced for both, with larger improvement (lower fluctuation) for the 13 nm cells. All the analyzed parameters present an enhance- ment, but the remarkable reduction of variability impact is shown for the retention time. In particular, at a very high variation level an improvement of 13% and 24% is achieved, for both technologies. Thus, a modification of T1 width is a feasible option to mitigate the overall impact of the variability on 3T1D-DRAM cells. However, this would suppose a slight increase of memory cell area.

This improvement of performance is also explained by the higher mean value (m) obtained and similar standard deviation (s),

Fig. 5. Variability impact on 3T1D-DRAM memory cell parameters for 22 and 13 nm technologies and for all variability levels at 100 1C. Worsening performance as the temperature rises up is observed (For interpretation of the references to color in this figure, the reader is referred to the web version of this paper.).

what involves a final lower variability impact on 3T1D behavior. Moreover, the previously observed cell malfunction (Section 3) caused by the bad performance of T1 device on the sub-22 nm nodes is highly reduced ($\sim$ 1%).

4.2. *Temperature influence on cell variability*

On the other hand, the environment temperature is always a relevant factor in the decrease in circuit performance and, thus, its impact on variability has been analyzed in this section, as well. For this, Fig. 5 studies the impact of high temperatures (100 1C) on 3T1D-DRAM cells performance based on 22 and 13 nm nodes and different variability levels. Comparing with room temperature results (Table 2), we observe similar influence on RAT and PW values, whereas RT presents a high increase. This is caused by the V_{Smin} dependence on working temperature that directly affects the leakage current [12]. In particular, higher temperature is more detrimental for the smallest technology node, where an increase of the variability impact on the retention time around 30% is observed. Additionally, WAT shows a slight enhancement, due to the lower variability impact.

5. Yield at memory block architecture

For a more realistic analysis, we have also computed the manufacturing yield of a 2 kB cache memory block based on 3T1D cells. The circuit has been evaluated with a reconfigurable array of 32 cells per column, 512 columns and 24 redundant columns [18]. For yield analysis, we have assumed that a system based on a 3T1D- DRAM cell with a retention time lower than 714 ns is regarded as faulty. This time criteria ensure that the performance IPC loss

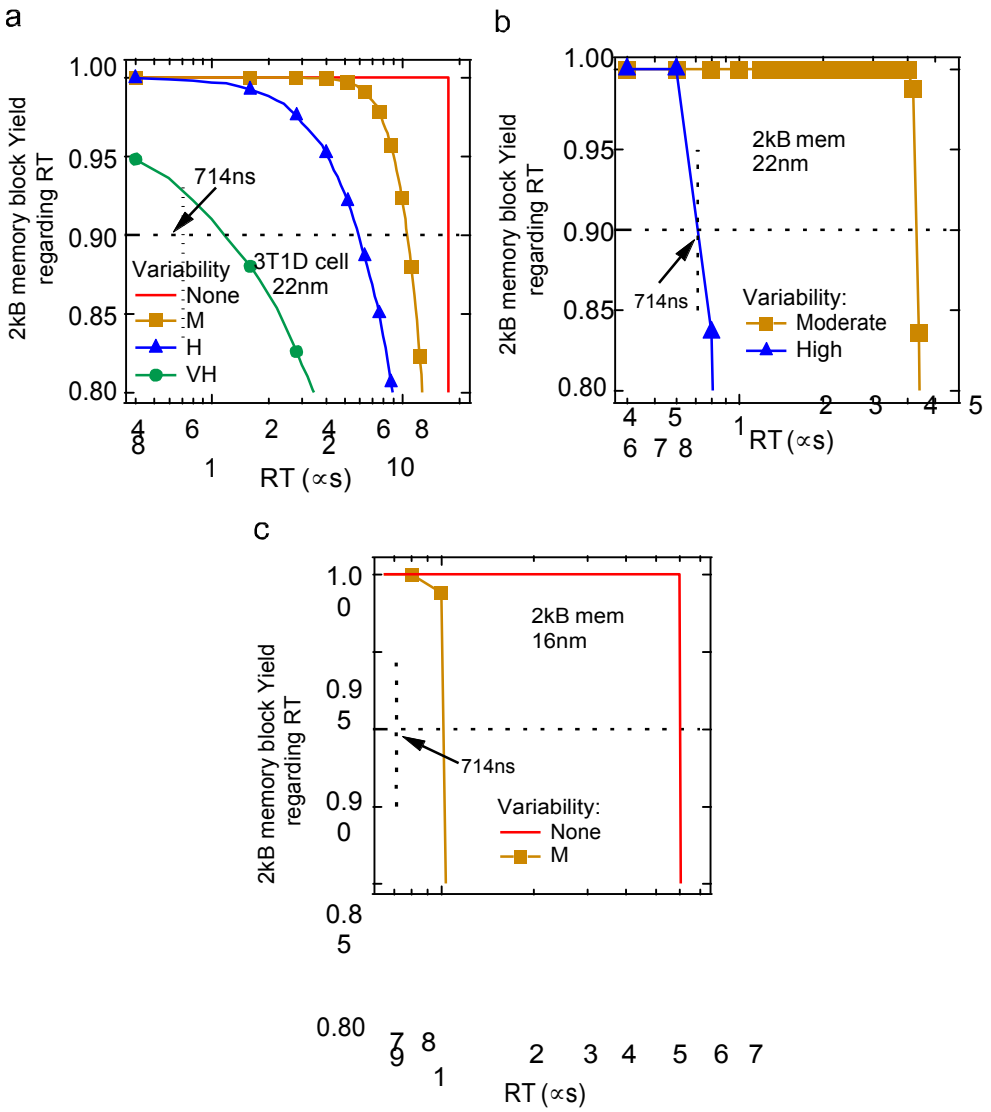


Fig. 6. Yield performance for a 3T1D memory at cell level (a) and at memory block level for 22 nm (b) and sub-22 nm nodes (c). At the 22 nm cell-level, more than 90% of the samples with a high variability level pass the criteria. At memory block level it depends on the technology node, since for 22 nm moderate and high levels pass, but for 16 nm only the moderate exceeds the 714 ns.

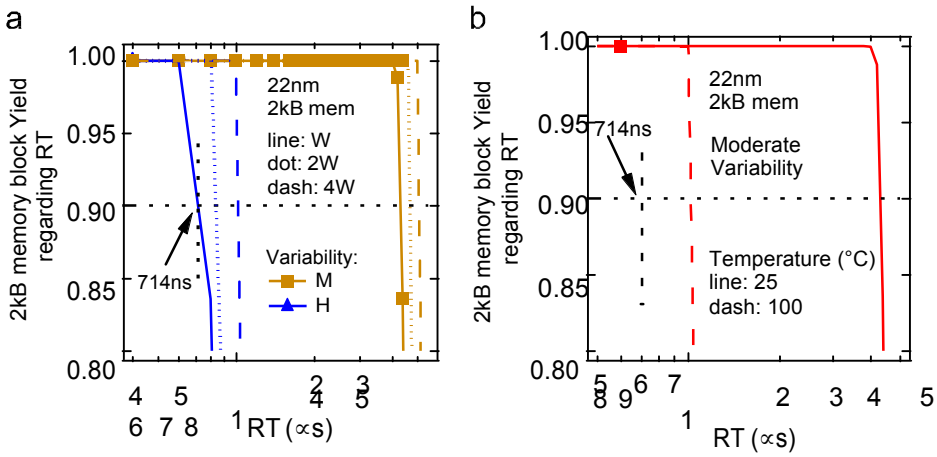


Fig. 7. Yield performance of 2 kB memory blocks based on 22 nm 3T1D cells, when (a) T1 width is resized up and (b) the environment temperature is raised up. The 90% of the memory blocks have larger retention times, improving, then, the cell performance. Meanwhile, for higher temperatures the 3T1D cells present a worsening behavior, since now the 22 nm system only fulfill the retention time

criteria under a moderate variability level.

(Instructions Per Cycle) in a system with 3T1Ds will be only about 2% when comparing with an ideal 6T design [3].

Thus, Fig. 6 shows yield simulations for (a) 3T1D memories based on 22 nm for a single cell, (b) a 22 nm memory block and (c) sub-22 nm one. Fig. 6a shows that, at cell level, more than 90% yield is achieved for 22 nm cells for every variability scenario. Meanwhile, Fig. 6b points out that the 90% yield of 2 kB memory blocks on 22 nm cells can be achieved only with moderate and high variability levels, showing a good performance of the simu- lated 3T1D-DRAM memory cells. Fig. 6c illustrates that for the smaller technologies the performance is more pessimistic, since for instance for 16 nm 3T1D cells is only able to meet the time criteria at moderate variability level.

To complete this analysis, Fig. 7 presents the performance of memory blocks based on 22 nm devices when the two previously presented mitigating scenarios (T1 upsizing and temperature) are assumed. In this sense, Fig. 7a presents a relevant yield enhance- ment when T1 width is enlarged at both fluctuation level (mod- erate and high), since larger retention times are obtained. So then, upsizing T1's width improves the cell performance. On the other

hand, Fig. 7b points out a clear yield reduction when the system temperature is raised up to 100 1C. These results show that the system only fulfills the time criterion at moderate variability level. For this, a control of the environment temperature is a very important aspect to take into account in order to improve the overall system behavior.

6. Conclusions

The 3T1D-DRAM cell performance has been analyzed under different variability scenarios. First, the device fluctuation analysis has pointed out that the effects of variability on write access transistor (T1) have the highest impact on circuit performance, becoming critical for cell device reliability.

In order to mitigate the observed cell variability several strate- gies have been presented and (a) resize the width of the write access transistor, T1, has resulted in a relevant improvement of the cell tolerance to the device variability, and (b) environment tem- perature has shown a cell worsening when is raised up, so, a control and reduction of the cell temperature has to take into account to reduce the device variability impact.

Moreover, the cell fluctuation on a 2 kB memory block based on 22 nm 3T1D cells has shown a yield larger than 90% for moderate and high variability levels, this means a better process variation tolerance than in the case of 6T cells, that it makes a good candidate to become a standard cell for memory caches.

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