Self-Powered Bipolar Gate-Driver Power Supply Circuit for Neutral-Point-Clamped Converters

S. Busquets-Monge, A. Filbà-Martínez, J. Nicolás-Apruzzese, and J. Bordonau
Department of Electronic Engineering
Universitat Politècnica de Catalunya
Barcelona, Spain
sergio.busquets@upc.edu

***Abstract*— The design of gate-driver power supply (GDPS) circuits for multilevel neutral-point-clamped converters is a challenge due to the large number of power switches required and the fact that each device presents a different GDPS reference node. This paper presents a compact self-powered bipolar GDPS circuit, consisting of two subcircuits connected across the power switches, which altogether produce all the positive and negative supply voltages required by the GDs. As these subcircuits essentially contain semiconductor components, they can be integrated with the power switch and gate driver, to produce a compact cell from which obtain a compact converter leg implementation. Overall, this BGDPS design is suitable for all types of NPC multilevel topologies with any type of power transistor, although it is most suitable for moderate device voltage ratings. The good performance of the proposed BGDPS circuit has been confirmed through experiments on a conventional two-level leg, and on three-level and four-level active-clamped converter legs.**

Keywords—gate-driver power supply; multilevel; neutral point clamped, self-powered.

I. INTRODUCTION

The interest in multilevel conversion techniques has been steadily increasing over the last two decades. A number of multilevel converters are already available as commercial products for several applications and it is still a hot research topic [1]. Their advantage is clear in high-power high-voltage applications, but they can also provide benefits at medium or low power and voltage levels. In general, multilevel conversion features improved efficiency, lower harmonic distortion, and lower common mode voltage, compared to conventional two-level conversion.

Among the different multilevel converter topologies, the most popular and widely used is the three-level neutral-point-clamped (NPC) [2]. An *n*-level neutral-point-clamped leg is functionally equivalent to a single-pole *n*-throw switch. The leg ac terminal can be connected to any of the *n* available dc-link points through an arrangement of only power semiconductor devices. The dc-link points are typically generated through a series connection of capacitors. The topology can be regarded as an extension of the two-level half-bridge topology of Fig. 1. Fig. 2 and Fig. 3 show this extension in the case of the passive-clamped (or diode-clamped) and active-clamped (transistor-clamped) versions of the NPC family, assuming that all devices have the same voltage rating, corresponding to a blocking voltage of $v_{dc}/(n-1)$. Although the operation of NPC converters with more than three-levels was initially deemed unfeasible at a wide range of operating conditions, due to the dc-link capacitor voltage balancing problem, several modulation and control techniques are already available today to solve this issue [3]. NPC topologies have a potential for a very compact implementation, because the leg does not require energy storage elements such as capacitors or inductors. However, they require a large number of power switches, especially as the number of levels increases. In addition, each power switch requires ancillary circuitry: basically, a gate driver (GD) and a gate-driver power supply (GDPS). Incorporating a GDPS for each power switch is especially challenging, as the reference node for each switch is in general different.

There are several options to generate the regulated and isolated low voltages necessary to feed each GD. For instance, one can use a set of low-power dc-dc converters with galvanic isolation, bootstrap charge pump circuits, resonant circuits [4], etc. However, these circuits present important drawbacks such as incorporating bulky components (i.e., inductors or transformers), being difficult to integrate, causing electromagnetic interference problems, or being asymmetric from both a topological and operation point of view. Instead, the unipolar GDPS circuit connected across the switch power terminals shown in Fig. 4 and proposed in [5]-[8] offers a very interesting solution for multilevel converters, since the circuit can be monolithically integrated within the power switch, and therefore represents a modular, symmetric, and compact solution. Reference [9] has already demonstrated the operation of this GDPS circuit in a three-level diode-clamped topology. Design guidelines to optimize the performance of this GDPS circuit have been discussed in [10].

The operation of the GDPS circuit presented in Fig. 4 is summarized as follows. Switch S_m represents the main power switch, whose gate driver is to be fed. Capacitor C_s stores the

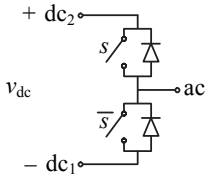


Fig. 1. Two-level half-bridge leg topology.

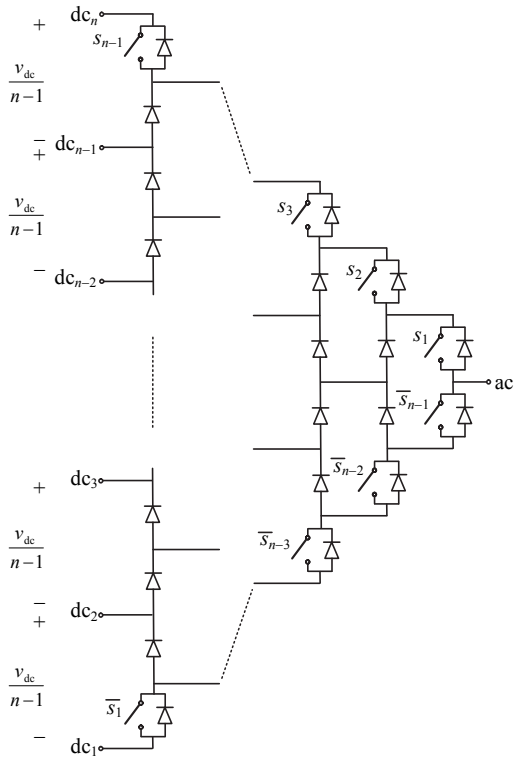


Fig. 2. Multilevel passive-clamped (diode-clamped) NPC topology.

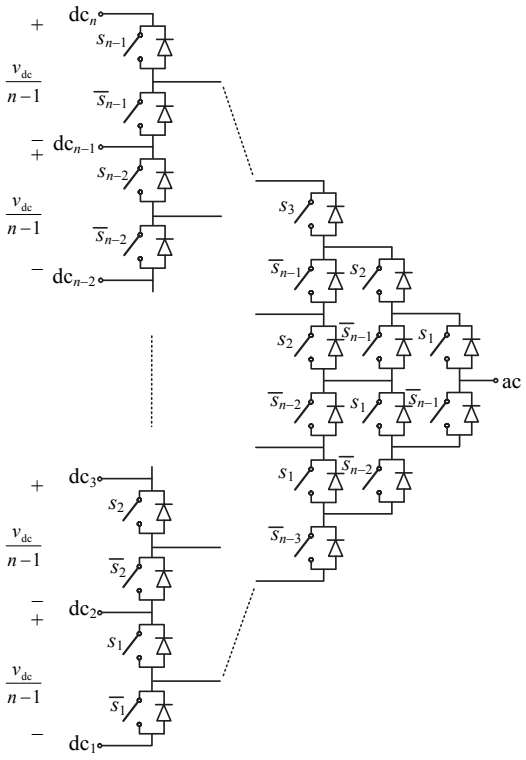


Fig. 3. Multilevel active-clamped (transistor-clamped) NPC topology.

energy necessary to feed this gate driver. Voltage v_{cc} is the generated positive GDPS voltage with reference to the source of S_m. During the S_m turn-off transient with $i_m > 0$, part of the current initially flowing through S_m flows through the auxiliary switch S_a charging capacitor C_s. The zener diode D_z, polarized by diode D_p, limits the value of v_{cc} and the blocking diode D_b prevents the discharging of C_s when S_m is on. S_m and S_a typically share the resulting turn-off loss. Overall, the energy to recharge C_s is obtained from energy that would otherwise be lost during the turn-off transition; i.e., part of S_m turn-off loss is recycled to power the GD. If $i_m < 0$, the energy to recharge C_s is obtained from the dc voltage source connected across the switch during its off state, with lower conversion efficiency. In a discrete implementation of the GDPS circuit, it is convenient to replace D_p by a resistor R_p to better control the polarizing current through D_z.

The self-powered GDPS circuit in Fig. 4 generates a single positive voltage v_{cc} to power the gate driver. However, many power switches (insulated-gate bipolar transistors or field-effect transistors) require a bipolar GDPS to guarantee a safe turn-off transition. Aiming to provide a simple solution for these cases, this paper proposes an extension of the GDPS circuit in Fig. 4 to provide both a positive and a negative GDPS voltage for each switch.

The paper is organized as follows. Section II presents the proposed topology and its operating principle. Section III proves the good performance of the proposed circuit through experiments on several legs with different number of levels. Finally, Section IV outlines the conclusions.

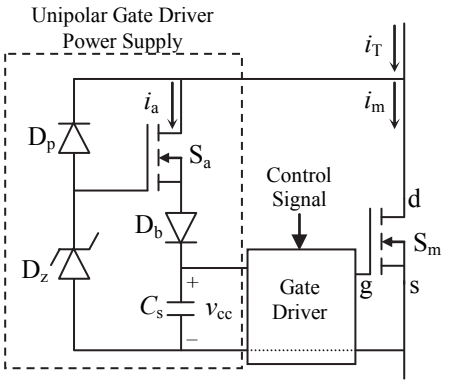


Fig. 4. Self-powered unipolar gate-driver power supply circuit.

II. Bipolar Gate-Driver Power-Supply Topology and Operation Principle

A. Topology

Fig. 5 presents the proposed topology to generate both positive and negative supply voltages to feed the gate driver of the main switch S_m. The GDPS combines two subcircuits: GDPS+ in charge of generating the positive supply voltage v^+_{cc} and GDPS– in charge of generating the negative supply voltage v^-_{cc}. Subcircuit GDPS+ is the original unipolar GDPS circuit depicted in Fig. 4. Subcircuit GDPS– represents a symmetrical extension, incorporating the same components as in GDPS+, except for their parameter values. In addition,

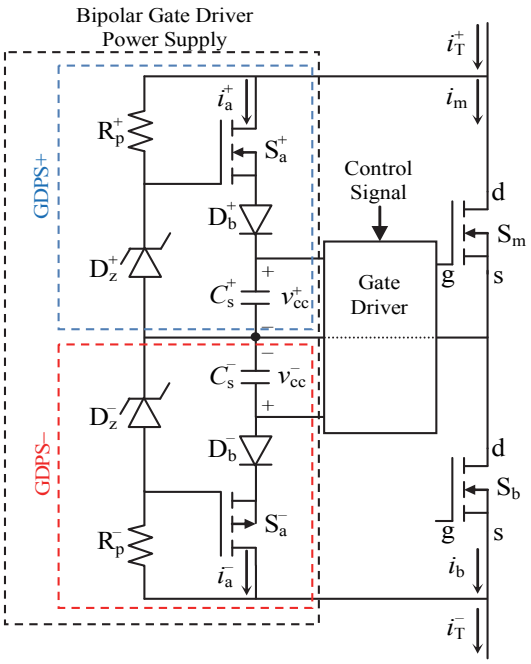


Fig. 5. Proposed self-powered bipolar gate-driver power supply circuit.

transistor S^-_a is a p-channel metal-oxide-semiconductor field-effect transistor (MOSFET) while S^+_a is an n-channel MOSFET. Subcircuit GDPS– must be connected across a bottom power switch S_b, whose drain is connected to the source of the main power switch S_m.

B. Operation Principle

The operating principle of GDPS+ has already been explained in Section I. The operating principle of GDPS– is analogous. Capacitor C^-_s stores the energy necessary to feed the S_m gate driver through the negative power supply. Voltage v^-_{cc} is the generated negative GDPS voltage with reference to the source of S_m. During the turn-off process of S_b with $i_b > 0$, part of the current initially flowing through S_b flows through the auxiliary switch S^-_a charging capacitor C^-_s. The zener diode D^-_z, polarized by resistor R^-_p, limits the value of v^-_{Cs} and the blocking diode D^-_b prevents the discharging of C^-_s when S_b is on. S_b and S^-_a typically share the resulting turn-off loss. Overall, the energy to recharge C^-_s is obtained from energy that would otherwise be lost during the turn-off transition of S_b; i.e., part of S_b turn-off loss is recycled to power the GD. If $i_b < 0$, the energy to recharge C^-_s is obtained from the dc voltage source connected across S_b during its off state, with lower conversion efficiency.

III. Experimental Results

Experimental tests have been conducted to verify the good performance of the proposed bipolar GDPS circuit for NPC converters. A cell composed of a power MOSFET IRFR4510 (100 V, 56 A) and ancillary circuitry (HCPL-316J GD and the proposed bipolar GDPS) has been designed, as a building block to implement converter legs with any number of levels. The selected components for the bipolar GDPS are listed in Table I. Two diodes in series are used to implement D_b in GDPS+ to fine tune the resulting value of v^+_{cc}. Fig. 6 shows a picture of the 30 mm x 35 mm cell, implemented on a printed circuit board.

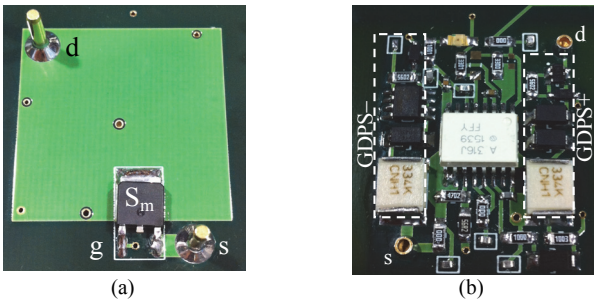
The cell has then been used to implement three different converter legs: a conventional two-level leg (Fig. 7(a)), a three-level active-clamped leg (Fig. 7(b)), and a four-level active-clamped leg (Fig. 7(c)). The GDPS– of each power switch is connected across the power switch right underneath. In cases where two S_b switches are possible, the one right below in the same column is selected. For instance, in Fig. 7(c), when considering the connection of S_{61} GDPS–, there are two S_b candidates (S_{51} and S_{52}) and S_{51} is selected since it belongs to the same column as S_{61}. All power switches present at least one S_b candidate except for S_{11}. To solve this issue, the negative supply voltage of S_{11} has been obtained from an external dc power supply.

The resulting three converter legs have been tested under the experimental test configuration depicted in Fig. 8. A constant dc voltage $V = 50$ V has been forced across nearby dc-link points using independent dc power supplies. The leg is then operated to produce a 10 kHz staircase voltage waveform at the leg ac terminal with equal duty ratios for the connection to all dc-link points. The ac-terminal voltage is applied to a series resistive-inductive load with $L = 8.7$ mH to produce a fairly constant ac-terminal current i_{ac}. The two configurations illustrated in Fig. 8 allow reaching positive and negative i_{ac} values and the load resistance is adjusted to operate with an absolute value of i_{ac} equal to 5 A.

Fig. 9 presents the results of the two-level leg test. All GD supply voltages, switch gate voltages, and the resulting leg ac terminal voltage and current are shown on several synchronized scope captures. Refer to Fig. 7 for the switch nomenclature. All positive and negative supply voltages remain stable at the intended dc value with small ripple. The generated gate voltages of both switches commutate complementarily and

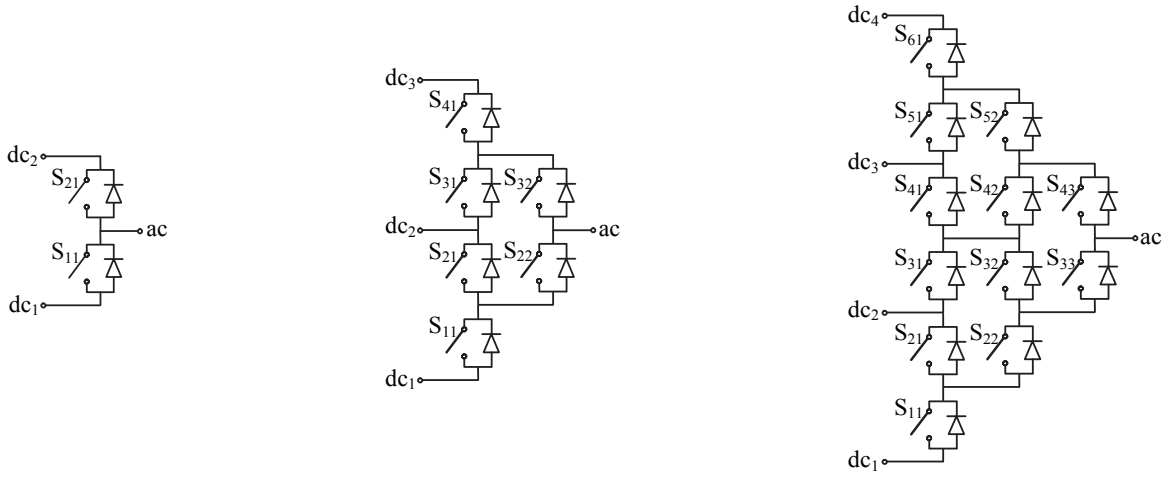
TABLE I
Bipolar GDPS Components

Component	GDPS+	GDPS–
S_a	IRF5802 (150 V, 0.9 A)	IRF6217 (–150 V, –0.7 A)
D_z	DDZ9708 (22 V @ 50 µA)	DDZ9697 (10 V @ 50 µA)
D_b	2xMBRA140 (40 V, 1 A)	MBRA140 (40 V, 1 A)
R_p	56 kΩ	56 kΩ
C_s	330 nF	330 nF



(a) (b)

Fig. 6. Implementation of the bipolar GDPS for each switch of the experimental prototypes. (a) Main power switch on one side of the printed circuit board. (b) Gate driver circuitry and bipolar GDPS on the other side.



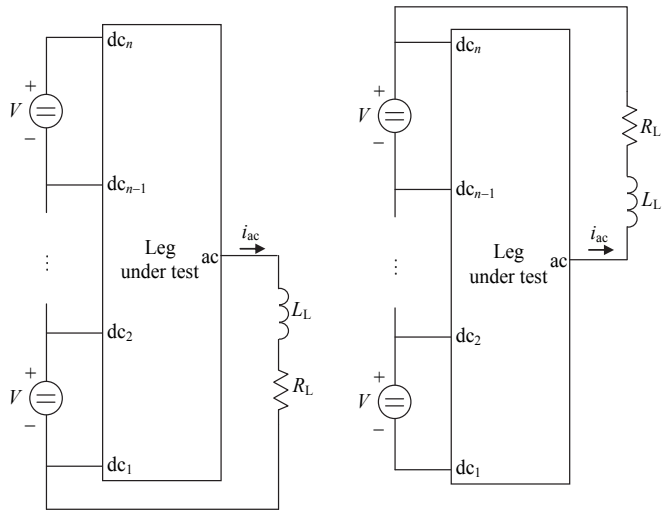
(a) (b) (c)

Fig. 7. Switch nomenclature for the implemented legs. (a) Two-level leg. (b) Three-level active-clamped leg. (c) Four-level active-clamped leg.

with an adequate blanking time between a positive and a negative voltage value in the same manner as would have been occurred with an external GDPS. The resulting ac-terminal voltage presents two levels and the ac-terminal current is fairly constant.

Fig. 10 presents the results of the three-level leg test. All scope captures are again synchronized. All GD supply voltages are regulated at proper voltage values, and the leg generates the expected three-level ac terminal voltage. The spikes appearing in the waveforms are noise captured by the used differential probes.

Fig. 11 presents the results of the four-level leg test. The GD supply voltage waveforms are not displayed for the sake of brevity, but their values can be indirectly observed through the twelve captured switch gate voltages. Again, the leg operates properly to generate the expected four-level ac-terminal voltage.



(a) (b)

Fig. 8. Experimental test configuration. (a) For positive i_{ac}. (b) For negative i_{ac}.

IV. Conclusion

This paper has presented a self-powered bipolar GDPS circuit, consisting of two subcircuits (GDPS+ and GDPS–) connected across the power switches. The proposed bipolar GDPS generates the regulated positive and negative supply voltages necessary to drive the power switch. The energy is partly obtained from recycling switching losses in the power switches. As these subcircuits essentially contain semiconductor components, they can be monolithically integrated within the power switch, with the exception of the power supply capacitors C_s. One GDPS+ circuit and one GDPS– circuit can be integrated with any type of power switch and a GD in order to produce a compact cell from which NPC converter legs with any number of levels can be easily built interconnecting several of these cells. The performance is satisfactory, although a single external dc power supply is necessary for the negative supply voltage of the leg bottom switch. The proposed bipolar GDPS circuit is most suitable for moderate power-switch voltage ratings.

Acknowledgment

This work has been supported by the Ministerio de Economía, Industria y Competitividad, Spain, under Grant DPI2017-89153-P (AEI/FEDER, UE).

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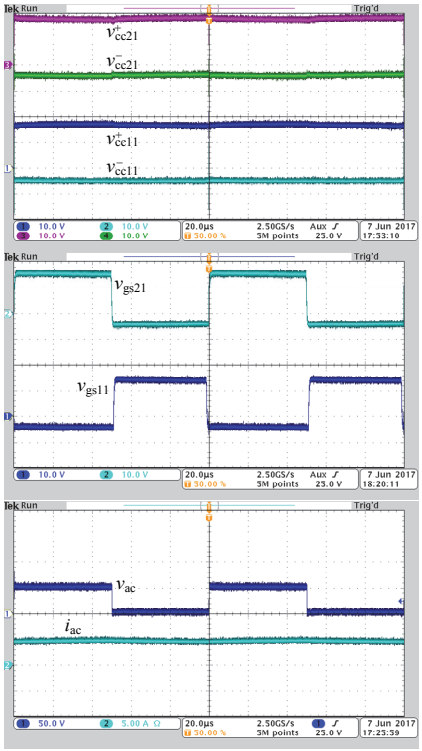
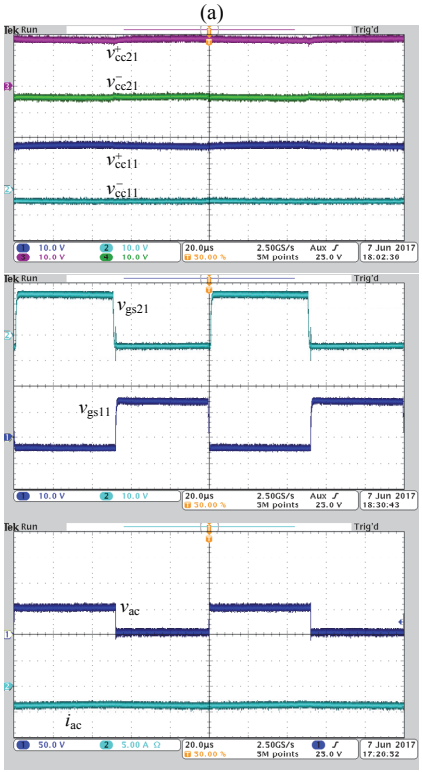
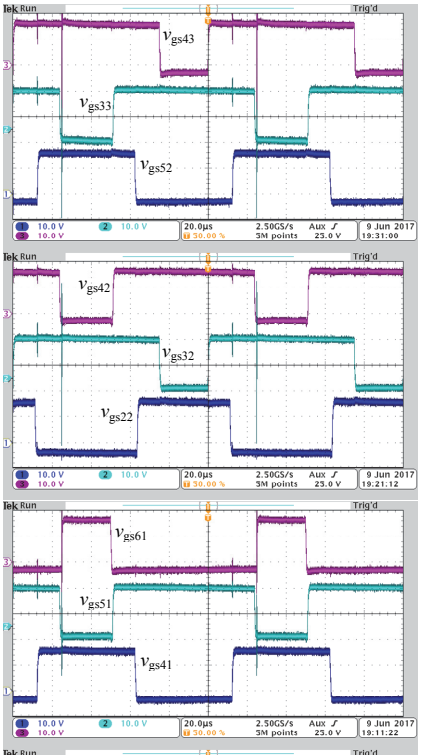


(a)

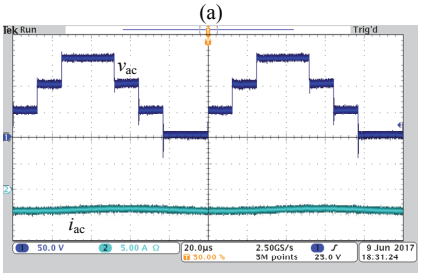


(b)

Fig. 9. Experimental results for a two-level leg. (a) $i_{ac} > 0$. (b) $i_{ac} < 0$.



(a)



(b)

Fig. 11. Experimental results for a four-level active-clamped leg. (a) $i_{ac} > 0$. (b) $i_{ac} < 0$.

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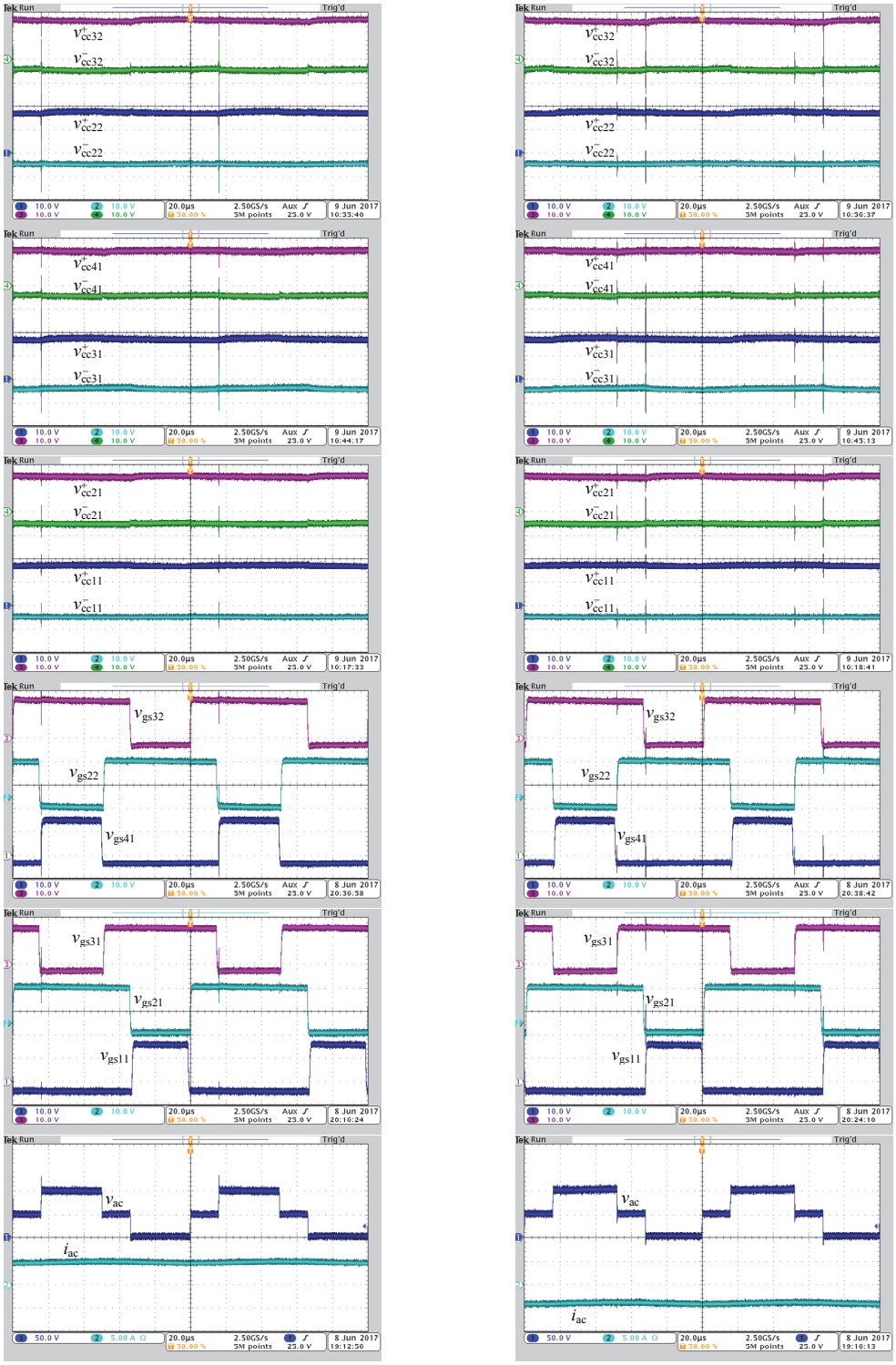

(a) (b)

Fig. 10. Experimental results for a three-level active-clamped leg. (a) $i_{ac} > 0$. (b) $i_{ac} < 0$.

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