Low Power Output-Capacitorless Class-AB CMOS LDO Regulator

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***Abstract*— This paper presents an output-capacitorless class-AB low-dropout (LDO) regulator with load current sinking and sourcing ability. The proposed LDO consists of two complementary pass transistors, controlled using a level shifter technique. The transient improvement section applied to the gates of the pass devices enhances the transient performance of the LDO. The proposed LDO is designed in TSMC 0.18 µm CMOS process with input and output voltages of 1.2-2.5 V and 1 V, respectively, 10 pF output capacitor, and quiescent current of 3.14 µA, and is capable to sink and source maximum load currents of ±100 mA, giving the current efficiency of 99.99%.**

***Index Terms*—low-dropout regulator, class-AB LDO, complementary pass transistors, level shifter, sink and source.**

I. Introduction

Linear-Assisted/LDO-Assisted buck converters become an efficient solution in high speed power management circuits [1-3]. They can provide higher efficiencies rather than linear/LDO regulators and higher speed performance rather than buck converters. One of the main requirements for designing such a structure is utilization of class-AB linear/LDO regulators. Class-AB linear regulators, which are widely used and well known, usually have a push-pull amplifier as their last stage. In contrast, class-AB LDOs have been presented in limited literatures [4, 5]. Since the design of class-AB LDO is a little bit different from its class-A counterpart, due to utilizing two complementary pass transistors (CPTs) in the common-source configuration (n-type and p-type), the design procedure implies the use of extra circuitry to control the PTs. In [4], a class-AB regulator with minimum dropout voltage of 350 mV and large off-chip output capacitor of 30 µF was proposed, which applies two current mirrors to control the operation of the CPTs. Since the upper PT, sourcing the current to the load, has a source follower structure, resulting in a relatively high difference between input and output voltages, it cannot be categorized in the class of LDO regulators, where their power transistors are in common-source configuration. In [5], the design procedure of an external capacitorless class-AB LDO with push-pull common-source power transistors was presented, in which cross-over inverters were utilized to separate and control the gate of CPTs. In addition, a quiescent current reduction circuitry was embedded into the LDO to reduce the quiescent current to a low level of 1.8 µA. However, it suffers from utilizing relatively large on-chip capacitances to improve the performance of the LDO.

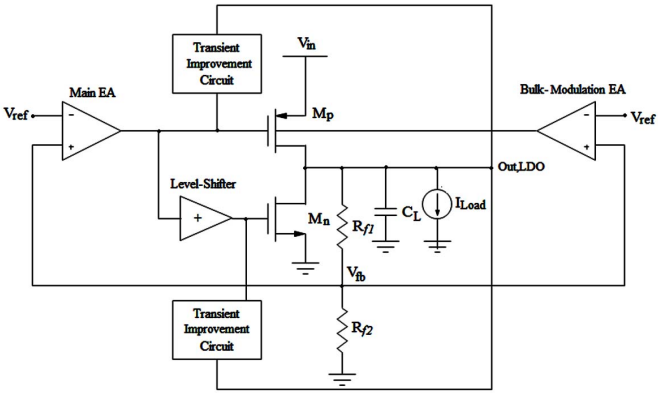

Fig. 1. Block diagram of the proposed class-AB LDO regulator.

In this paper, a new structure is proposed to control the CPTs of a fully on-chip class-AB LDO regulator based on level shifting the gate of n-type PT. Utilizing the transient improvement circuits results in enhancing the transient performance of the LDO. In addition, bulk modulation technique is applied for the p-type PT to further improve the transient behavior during the load step up and down at positive load currents [6]. The rest of the paper is as follows; in section II, the proposed LDO and its performance from the stability and transient points of view are presented. Section III belongs to the results and discussion. Finally, the achievements of the manuscript are concluded in section IV.

II. Proposed Class-AB LDO Regulators

Block diagram of the proposed class-AB LDO regulator is illustrated in Fig. 1. A level shifter stage is used to separate the gate of CPTs. Two transient improvement circuits are exploited to improve the transient response; in addition, the bulk modulation technique is applied for further improving the transient response at load step up and down at positive range.

The circuit level realization of the proposed LDO is shown in Fig. 2. It consists of a recycling folded cascode amplifier, M_1-M_7, as the main EA, which directly drives the PMOS PT, M_p, simple differential amplifier, M_{16} and M_{17}, as the bulk modulation EA, and a level shifter, M_8 and M_9, for driving the NMOS PT, M_n. Transistors M_{18}-M_{29} along with the transient coupling capacitors C_1 and C_2 form the two transient improvement circuits. The rest of the transistors are for bias. C_L and C_C are the on-chip load and compensation capacitors, respectively. R_Z, R_{f1}, and R_{f2} are the compensation and feedback resistors, respectively.

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A. CPT Control Technique: The Level Shifter

A single-ended differential amplifier can be assumed as an amplifier with two inverse outputs. Each output can be used to control the gate of CPTs; the high impedance output is connected to the gate of the p-type PT and the low impedance one to the gate of the n-type PT. However, the low impedance output would not create enough voltage to pull up and down the gate of the n-type pass transistor. Hence, an inverting single-ended amplifier is utilized between the low impedance output node and the gate of the n-type PT. Thus, whole the low impedance output and the inverting amplifier are considered as the level shifter, which indeed shifts the voltage level at the gate of the n-type PT. In this case, the dimensions of the level shifter transistors, M_8 and M_9, determine the different gate voltage levels.

B. Stability Analysis

The small signal block diagram of the proposed class-AB LDO regulator is shown in Fig. 3. In general, there are four left half plane (LHP) poles, three LHP zeros, and two right half plane (RHP) zeros as below:

$$\omega_{p,1}=\frac{1}{R_{eq1}C_{eq1}},\ \omega_{p,2}=\frac{1}{R_{eq2}C_{eq2}},\ \omega_{p,3}=\frac{1}{R_{eq3}C_{eq3}}$$
$$\omega_{p,4}=\frac{1}{R_{out}C_L},\quad \omega_{z,RHP1}=\frac{g_{mp}}{C_{gdp}},\quad \omega_{z,RHP2}=\frac{g_{mn}}{C_{gdn}} \qquad (1)$$
$$\omega_{z,LHP1}=\frac{1}{(R_z-\frac{1}{g_{mn}})C_C},\omega_{z,LHP2,3}=f(\omega_{p,1},\omega_{p,2},\omega_{p,3})$$

where R_{eq1}, R_{eq2}, and R_{eq3} are the resistances seen from the output of the main EA, level shifter, and bulk modulation EA, respectively. R_{out} is the resistance at the output of the LDO ($R_{out}=R_L\,||\,(R_{f1}+R_{f2})\,||\,r_{dp}\,||\,r_{dn}$). G_{m1} and G_{m3} are the transconductance of the main EA and bulk modulation EA, while G_{m2} is the transconductance of the low impedance path of the main EA multiplying by the level shifter transconductance. Transconductance and gate-drain capacitance of the *p*-type and *n*-type PTs are represented by g_{mp}, g_{mn}, C_{gdp}, and C_{gdn}, respectively, generating the RHP zeros, whereas g_{mb} is bulk transconductance of the *p*-type PT. Two LHP zeros are resulted from two parallel paths, and can be described as a function of the LHP poles of corresponding paths, ω_{p1}, ω_{p2}, and ω_{p3}. The other LHP zero comes from the simple Miller compensation technique for the LDO stability achievement. Having four LHP poles and three LHP zeros makes it easier to set the stability of the LDO regulator for every load current.

C. Transient Analysis

Case I- Transients from zero to negative load currents:

When the load current changes suddenly from zero to negative current, the gate of the n-type PT cannot sense the changes immediately. Thus, the current is provided through charging the load capacitance. When the output voltage increases a little bit, the current of M_{25} will be increased, pulling up the gate of M_{27}, allowing more current pass through it. As a consequence, the large current of M_{29} will charge the gate of the n-type PT, resulting in passing more current through it. On the other hand, the main EA keeps off the p-type PT.

Case II- Transients from negative (positive) to zero load currents:

When the load current changes suddenly from negative

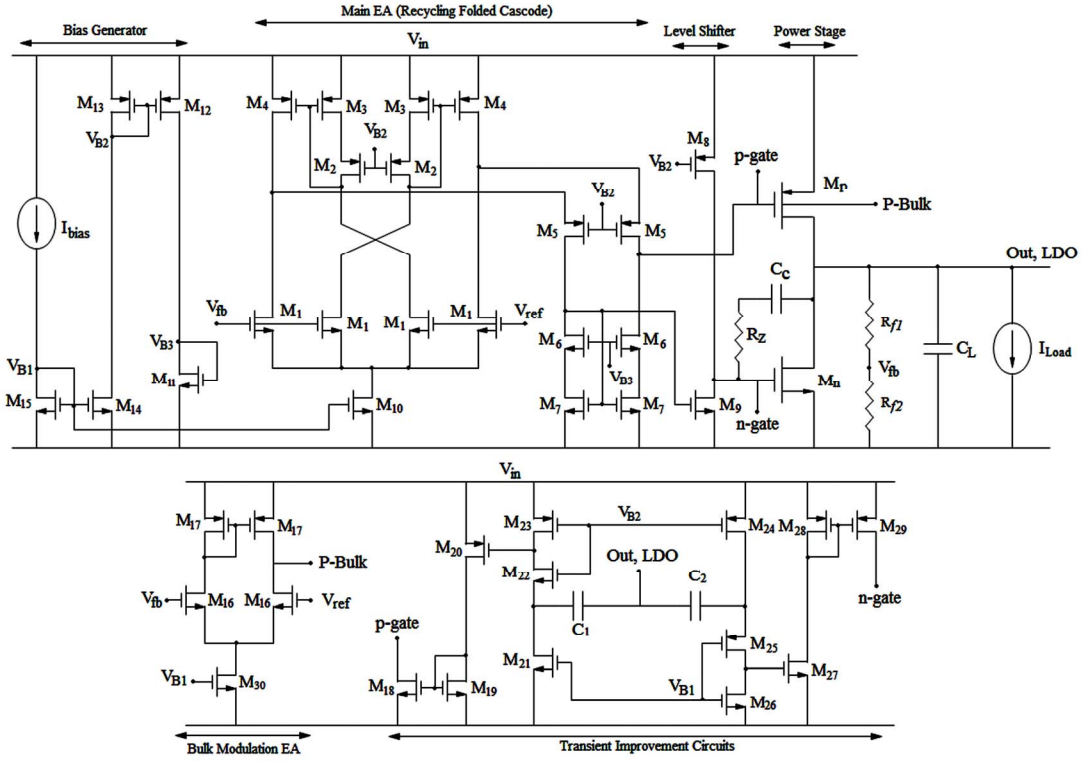

Fig. 2. Circuit level realization of the proposed class-AB LDO regulator.

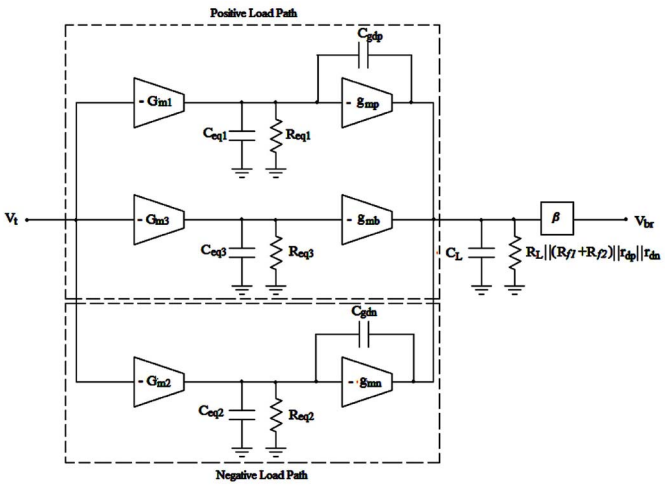

Fig. 3. Small signal block diagram of the proposed class-AB LDO regulator.

(positive) current to zero, first, the current discharges (charges) the load capacitance, decreasing (increasing) the output voltage a little bit. As a consequence, the EA will pull down (up) immediately the gate of the n-type (p-type) PT, and the process is fast enough so that there is no need for any transient improvement circuits

Case III- Transients from zero to positive load currents:

When the load current changes suddenly from zero to positive current, the gate of the p-type PT cannot sense the changes, immediately. Thus, the current is provided through discharging the load capacitance. When the output voltage decreases a little bit, the current of M_{22} and M_{20} will be increased, allowing more current pass through M_{18}. As a result, the large current of M_{18} will discharge the gate of the p-type PT, resulting in pumping more current by it. In addition, the bulk modulation EA will decrease the threshold voltage of the p-type PT, increasing the current passing through it. On the other hand, the main EA keeps off the n-type PT.

III. Results and Discussion

The proposed class-AB LDO regulator is designed and post-simulated using HSPICE in TSMC 0.18 µm CMOS process. The input and output voltages are 1.2 V and 1 V, respectively. The proposed LDO has a wide range of input varying from 1.2 V to 2.5 V. The maximum sink and source load currents of ±100 mA is provided by the proposed LDO, while the quiescent current is equal to 3.14 µA. The capacitors C_L, C_C, C_1, and C_2 are 10 pF, 1 pF, 0.5 pF, and 1 pF, respectively; giving the total on-chip capacitance of 12.5 pF. R_Z, R_{f1}, and R_{f2} are 2 kΩ, 200 kΩ, and 800 kΩ, respectively. The layout of the proposed regulator is shown in Fig. 4. The total core area of the chip is equal to 0.04 mm^2.

Load regulations for two input voltages of 1.2 V and 1.8 V are shown in Fig. 5 (a), which are equal to 23 µV/mA and 15 µV/mA, respectively. Line regulation is provided for three different load currents of 0 and ±100 mA in Fig. 5 (b). It has the amounts of 1.15 mV/V, 0.69 mV/V, and 2.23 mV/V for load currents of 0, 100 mA, and -100 mA, respectively.

Load transient response of the LDO with load current rise and fall times of 1 µs are shown in Fig. 6. The maximum overshoot/undershoot and settling time are 220 mV and 3.6 µs, respectively, while, the minimum ones are 70mV and 2 µs, respectively. In addition, line transients for the load currents of ±100 mA and their corresponding settling times and output voltage deviations are shown in Fig. 7.

Frequency response of the proposed class-AB LDO is shown in Fig. 8 for different load currents. The phase margin varies from 35 to 85 degrees for different currents, indicating a stable treatment of the LDO for all current ranges. Furthermore, power supply rejection ratio (PSR) for different load currents is shown in Fig. 9, which varies between -50 dB

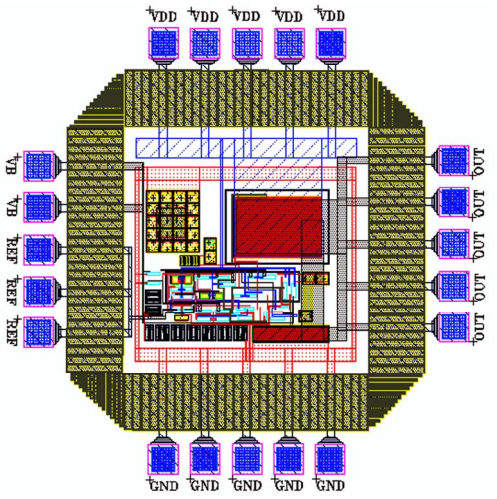

Fig. 4. Layout of the proposed class-AB LDO regulator.

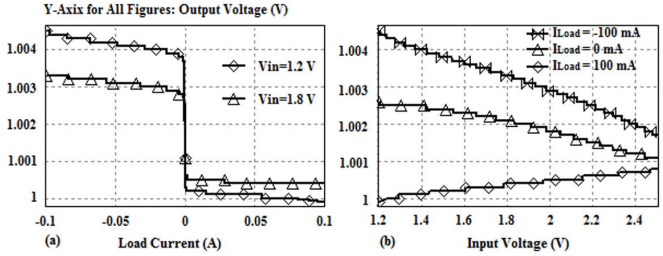

Fig. 5. (a) load regulation and (b) line regulation of the class-AB LDO.

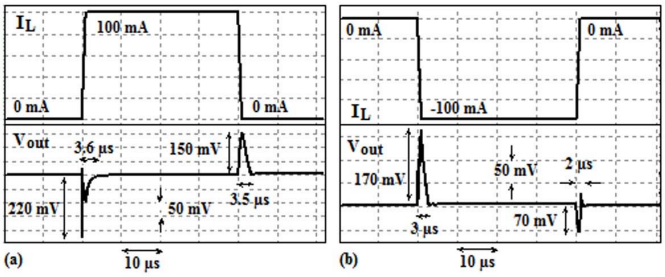

Fig. 6. Load transient behavior of the class-AB LDO for (a) positive and (b) negative loads.

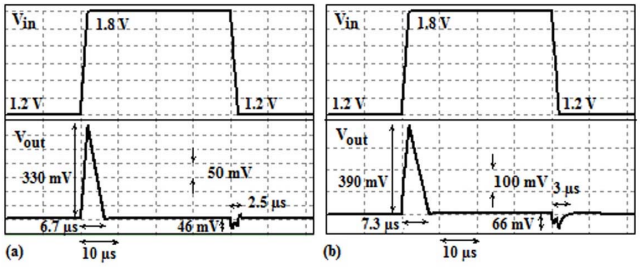

Fig. 7. Line transients for load currents of (a) -100mA and (b) 100mA.

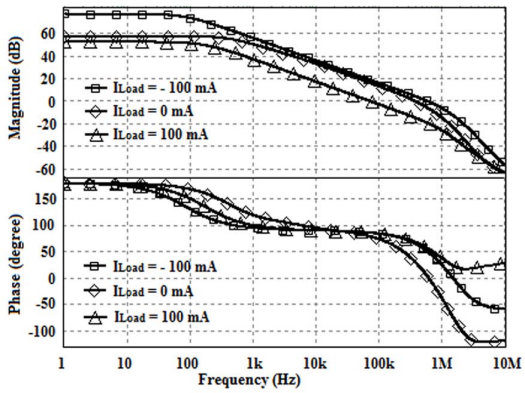

Fig. 8. Frequency response of the class-AB LDO for different load currents.

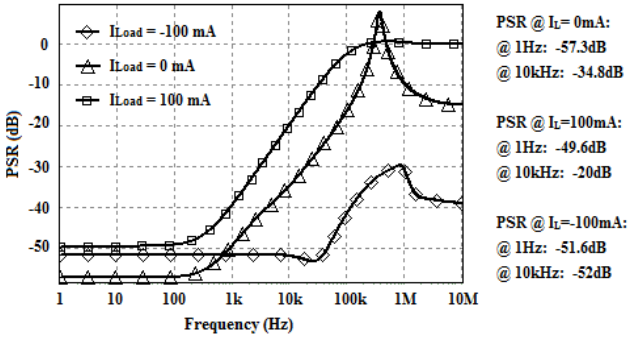

Fig. 9. PSR of the class-AB LDO in different load currents.

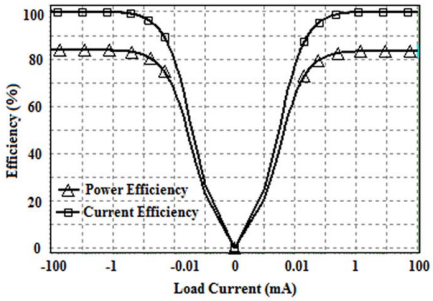

Fig. 10. Current and power efficiencies of the class-AB LDO.

to -40 dB at 1 kHz for different load currents. The current and power efficiencies of the LDO are shown in Fig. 10. The maximum current and power efficiencies of 99.99% and 83.3% are achieved, respectively.

The specifications of some recent works (class-A and class-AB) are provided in table I, to have a benchmark performance comparison with the proposed class-AB LDO regulator. For the proposed LDO, the results are included and the worst case for output voltage variation (ΔV_{out}) and settling time (T_{settle}) is considered. Furthermore, the figure of merit ($FOM = T_{settle}.I_Q/I_{out,max}$) [7] is adopted here to compare the performance of different LDOs. Lower FOMs for LDOs implies better transient performances. Besides the lowest total capacitance and area consumption of the proposed class-AB LDO regulator among all reported LDOs, it has the lowest *FOM* rather than the others. In addition, the proposed LDO has the lowest settling time rather than the other output-capacitorless LDOs, i.e. references [5] and [8], and its output voltage deviation is lower than that in [5]. Although the output deviation of the class-A LDO reported in [8] is lower than the proposed LDO, its settling time and quiescent current is 1.6 and 6.4 times larger than the proposed class-AB LDO.

IV. Conclusion

An output-capacitorless class-AB LDO regulator with maximum load current sinking and sourcing capability of ±100 mA for a stable output voltage of 1 V with a 10 pF output capacitor and 200 mV dropout, consuming a small area and low quiescent current of 3.14 µA is presented. The level shifter-based control technique was applied to control the complementary pass transistors. Additionally, transient improvement circuits were utilized to improve the transient performances of the regulator.

TABLE I. Performance Comparison

Ref.	[4]	[8]	[5]	**This Work**
Data	Exp.	Exp.	Post-Sim.	**Post-Sim.**
Class Type	AB	A	AB	**AB**
Tech (*µm*)	0.5	0.35	0.18	**0.18**
V_{in} (V)	2.4-6	1.8	1.2	**1.2**
V_{out} (V)	0.6-1.3	1.6	1	**1**
I_{out} (mA)	±3000	100	±80	**±100**
I_q (µA)	220	20	1.8	**3.14**
C_{out} (pF)	30×10^6	100	1	**10**
$C_{tot.}$ (pF)	30×10^6	100	100	**12.5**
T_{settle} (µs)	2.8	9	11	**3.6**
ΔV_{out} (mV)	30	97	227	**220**
FOM (*ns*)	0.2	1.8	0.25	**0.11**
Area (mm^2)	1	0.15	0.24	**0.022**

Acknowledgment

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