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The Use of Output-Capacitorless Class-AB CMOS Low-Dropout Regulator for Power Management

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***Abstract*—This article presents the design of a 4.5-*V*, 450-*mA* low drop-out (LDO) voltage linear regulator based on a two-stage cascoded operational transconductance amplifier (OTA) as error amplifier. The aforementioned two-stage OTA is designed with cascoded current mirroring technique to boost up the output impedance. The proposed OTA has a DC gain of 101 *dB* under no load condition. The designed reference voltage included in the LDO regulator is provided by a band gap reference with the temperature coefficient (T_γ) of 0.025 *mV/°C*. The proposed LDO regulator has a maximum drop-out voltage of 0.5 *V* @ 450 *mA* of load current, and has the worst case power supply rejection ratio (PSRR) of [54.5 *dB*, 34.3 *dB*] @ [100 *Hz*, 10 *kHz*] in full load condition. All the proposed circuits are designed using a 0.35 µ*m* CMOS technology. The design is checked in order to corroborate its performance for wide range of input voltage, founding that the circuit design works fine meeting all the initial specification requirements.**

Keywords—Low drop-out (LDO) voltage linear regulator; operational transconductance amplifier (OTA); band gap reference; cascoded current mirror

I. INTRODUCTION

Low-dropout voltage linear regulators (LDO) [1-4] have gained much of importance due to the increased use of battery-powered devices. The main function of the LDO regulator is to provide a reliable, stable and constant voltage, and has been considered as one of the important component in power management of cell phones, laptops, wireless applications, etc., where one of the important issues is the dropout voltage, which plays an important role in these kinds of applications [5].

Fig. 1 shows the overall topology of the proposed LDO regulator. As can be seen, it consists of three main blocks: An error amplifier, a voltage reference and a pass transistor with external load capacitance with small value of internal resistance (ESR) for the frequency compensation. The error amplifier of the LDO regulator, in the negative feedback condition, constantly compares the error signal with the reference voltage and hence maintaining the constant output voltage by varying the gate to source voltage of the pass transistor accordingly. Since the output of error amplifier is used to drive the gate of the pass transistor which is naturally a capacitive load, the best option for the error amplifier would be an operational transconductance amplifier (OTA) [6, 7] with high output impedance (Fig. 2). In addition, it is very easy to model OTA as single pole system because of its high output impedance, which forms a low frequency pole with small load capacitance. Therefore, OTAs are the best components to drive the capacitive loads because of the fact that their output signal is a current controlled by a differential input signal.

The voltage reference is one of the important blocks of the voltage regulators, since it decides the nominal output voltage. The main design issue will be its temperature coefficient, which has to be ideally zero or very near to it. There are many approaches in obtaining the voltage reference. However, one among them, with very low temperature coefficient, is the use of a band gap voltage reference (BGR) [8]. Finally, a pMOS pass transistor, which carries a major part of current in the whole circuit, drives the load. Its dimensions are set such that it is able to withstand the maximum rated current and to achieve the rated low dropout voltage.

The paper is organized as follows: In Section 2, the design of the two-stage cascoded OTA in CMOS technology is carried out. Next, in Section 3, the design of the LDO regulator is discussed, including the design of the error amplifier based on the proposed OTA, and design of the pass transistor in CMOS technology. Finally, in Section 4, simulation results are obtained for both proposed OTA and LDO regulator.

II. DESIGN OF THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

Fig. 3 shows the classical two-stage OTA in CMOS technology [7], where it is operated in $+V_{dd}$ and $-V_{ss}$ power supplies and with an external bias current I_{bias} and having a single ended output. The first stage is the normal *n*-channel differential input pair (m_1 and m_2) with *p*-channel current mirror as its active load (m_3 and m_4). The drain currents of m_1 and m_2 are mirrored to m_6 and m_5, respectively, which is the second (gain) stage through the classical current mirroring technique with the current ratio of 1:α. In Fig. 3, we get:

$$I_a = (I_{bias}/2) - g_{m(2)}v_i \text{, and } I_b = (I_{bias}/2) + g_{m(1)}v_i \qquad (1)$$

The single ended output is taken out from point *P*1, through which a current of:

$$I_o = 2 \cdot g_{m(1,2)} \cdot \alpha \cdot v_i \tag{2}$$

is flowed, where $v_i=(v_+)-(v_-)$ is called the differential input. Therefore, the voltage controlled current source is obtained and the transconductance of this OTA, G_m, is given by the expression:

$$G_m = \frac{I_O}{V_i} = 2 \cdot \alpha \cdot g_{m(1,2)} \tag{3}$$

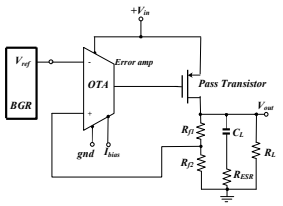

Fig. 1.- Topology of the proposed LDO voltage linear regulator.

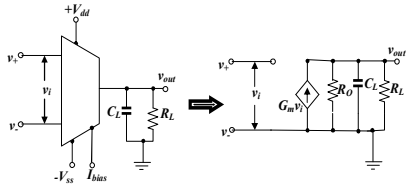

Fig. 2.- Small signal model of an OTA with C_L and R_L.

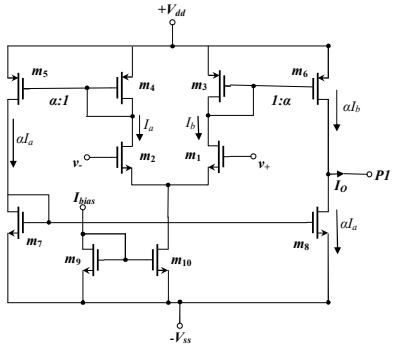

Fig. 3.- Classical two-stage OTA in CMOS technology.

It should be noted that according to the Equation (3), the transconductance of the OTA is dependent on the g_m of the MOS transistors of the input differential pair which is in-turn dependent on the DC current through it, i.e., $\sqrt{I_{bias}/2}$. Therefore, it can be said that it is a current controlled gain OTA. The parameter α is called the gain factor which is modified by varying the ratio W/L of the second stage with respect to the input stage ($W/L_{(6,5)}$:$W/L_{(3,4)}$). The equivalent small signal model representation of the OTA is shown in Fig. 2. According to this figure, the voltage gain ($A_v(s)$) is given by the expression:

$$\frac{V_{out}(s)}{V_i(s)} = A_v(s) = \frac{A_v}{1+\frac{s}{\omega_o}} = G_m . Z_L(s) \tag{4}$$

where G_m is the tranconductance of the OTA which is given by the Equation (3) and the cut-off frequency ω_o is given by:

$$\omega_o = \frac{1}{(R_o \parallel R_L) C_L}, \tag{5}$$

and Z_L(s) is the output impedance of the OTA, which is given by:

$$Z_L(s) = \frac{R_o \parallel R_L}{1+(R_o \parallel R_L) C_L(s)} \tag{6}$$

It should be noted that the OTA has the high output impedance thanks to the common source output configuration which gives the high output impedance $r_o(m_8)\|r_o(m_6)$. The main advantage of the OTA is that, due to the fact of its high output impedance, the frequency compensation is easier. The load capacitance (C_L) will only create the dominant pole. Hence the unity gain bandwidth is varied by varying the load capacitance to obtain the suitable phase margin (PM) according to the application and hence assuring the stability of the system.

Fig. 4 shows the improved two-stage OTA in CMOS technology, adopting the cascoded technique to boost up the output impedance and hence the DC voltage gain (no load) of the classical OTA, taking the proposed OTA into more ideality.

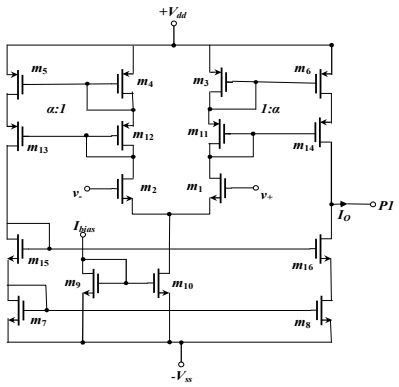

Fig. 4.- Proposed two-stage cascoded OTA in CMOS technology.

In the proposed design ($m_{4,5}$) and ($m_{13,12}$), ($m_{3,6}$) and ($m_{11,14}$), ($m_{15,16}$) and ($m_{7,8}$) form the cascoded pairs with current mirroring. The main design criterion of the proposed OTA is same as the classical OTA design which depends on the Equations (3), (4), and (6). The main advantage here is the boosting up of output impedance by a factor of approximately ($2+ g_{m(8)} \cdot r_o(m_8)$) which is quite significant. Hence the output impedance, R_o, is varied by varying the ratios $W/L_{(6,14,16,8)}$ in-turn varying its g_m. Regarding the other important parameters, the input impedance $R_i \approx \infty$ (since input are at the gate of the MOSFETs), the DC voltage gain of the OTA, from Equations (4) and (6), is given by:

$$A_v = G_m (R_o \parallel R_L) \tag{7}$$

Equation (7) can be used to find the $g_{m(1,2)}$ experimentally by obtaining the AC response of the proposed OTA for $R_L=\infty$, and also obtaining its output impedance plot with respect to frequency. Therefore, the equation for DC gain reduces to:

$$A_v \approx G_m R_o \tag{8}$$

In Section 4, simulation results of classical OTA are compared with proposed OTA by considering some

parameters. In addition, different parameters of the proposed OTA like AC response, DC gain, output impedance, etc. are also presented.

III. Design of the Low Drop-Out (LDO) Voltage Linear Regulator

As mentioned in Section 1, Fig. 1 shows the classical topology of the proposed LDO regulator. It consists of three main blocks, namely *error amplifier* block, *voltage reference* block, and *pass transistor*; and it is biased by means of an external current I_{bias}. In standard voltage regulators, the main difference compared to an LDO is in the pass transistor block. Normally, in a typical voltage regulator, pass transistor element will be an *n*MOS (or *npn*) transistor in source follower (or emitter follower) configuration which has a typical dropout voltage as 2 *V*. However, in a LDO regulator, the pass transistor element is a *p*MOS (or *pnp*) transistor open drain (or open collector) configuration, in which its dropout voltage is nothing but its saturation voltage with typical values as 0.3 ~ 0.5 *V*. One of the handicaps in a LDO regulator is, since a *p*MOS transistor is used as the pass transistor in open drain configuration (Fig. 1), it forms a high output impedance, creating a pole within the unity gain frequency. Since already there are a low frequency pole provided by error amplifier (OTA), there will be extra phase contributed by the pole formed by the high output impedance of the LDO to overall its response by decreasing the phase margin and causing the issue in stability of the system. Therefore, an output capacitance with small R_{ESR} is needed to compensate the above-mentioned pole. R_{ESR} with load capacitance (C_L) together form a zero to compensate the effect of the pole created by the high output impedance of the LDO regulator.

Resistors R_{f1} and R_{f2} in Fig. 1 are the resistors that are used to set the output voltage (V_{out}). The error amplifier forms a negative feedback loop, which constantly compares the error signal at the output with the reference voltage to maintain constant V_{out} by varying the gate voltage of pass transistor, and hence controlling the current flowing through it. Thus, the output voltage is given by:

$$V_{out} = \left(1 + \frac{R_{f1}}{R_{f2}}\right) V_{ref} \tag{9}$$

Thus, by choosing the appropriate values of resistors and reference voltage, output voltage V_{out} is set.

The initial design specifications given for the proposed LDO regulator are shown in Table I. Fig. 5 depicts the complete schematic of the CMOS LDO voltage linear regulator in order to fulfill the performance given by these design specifications. On the other hand, dimensions of the circuit transistors in the proposed LDO voltage linear regulator in Fig. 5 are depicted in Table II.

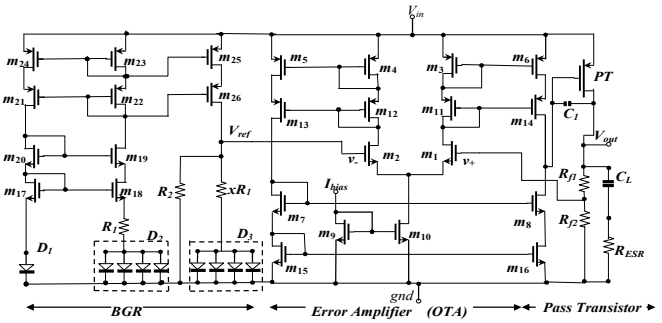

Fig. 5.- Proposed design of LDO voltage linear regulator.

Table I.- Design specifications of the Proposed LDO Regulator.

Design Specification	*Value*
Output voltage (V_{out})	4.5 *V* (1% allowance)
Max. output current ($I_{out,max}$)	450 *mA*
Reference voltage (V_{ref})	650 *mV*
Maximum drop-out voltage (V_{drop}) at I_{out} = 450m*A*	500 m*V*

Table II.- Dimensions of the transistors in the proposed LDO voltage linear regulator in Fig. 5.

Transistor	*Width (W) in* µm	*Length (L) in* µm
m_1 , m_2	500	1
m_3 , m_4 , m_{11} , m_{12}	40	1
m_5 , m_6 , m_{14} , m_{13}	800	1
m_7 , m_8 , m_{15} , m_{16}	800	1
m_9 , m_{10}	100	1
m_{17} , m_{18} , m_{19} , m_{20}	100	1
m_{21} , m_{22} , m_{23} , m_{24}	100	1
m_{25} , m_{26}	100	1
PT (pass transistor)	8000	1

As can be appreciated in Fig. 5, the proposed design has the three aforementioned main parts: (1) the error amplifier, (2) the voltage reference circuit, and (3), the pass transistor and the suitable load capacitance C_L.

A. Design of the Error Amplifier in the Proposed LDO Regulator

The error amplifier in the proposed LDO regulator basically consists of the OTA discussed in Section 2. The OTA as an error amplifier is shown in Fig. 5 and its design criterion is discussed in Section 2. The only difference is that here, it is operated at only positive voltage, i.e., without negative voltage $-V_{ss}$, and instead that point is connected to ground. According to the design, the simulation for open loop AC response is conducted several times with OTA operating at $+V_{dd}$ and *GND* (Fig. 6). Since the OTA is operating in these two potentials, the input terminals must be provided with proper DC bias in order to get the good open loop AC response with high DC gain. Hence the proposed OTA is simulated with different values of offset voltage (V_{offset}) at the input points while obtaining its open loop AC response. Section 4 shows the simulation results for V_{offset}=0 *V*; 0.3 *V*; 0.6 *V*, and 1 *V*. It can be seen that to get the better response the V_{offset}>0.6 *V*. When this OTA is working as the error amplifier in the proposed LDO, V_{offset} is set by the reference voltage (V_{ref}). Thus, the reference voltage has to be greater than 0.6 *V*. As a consequence, in the design

specifications of the LDO regulator, V_{ref}=0.65V. The capacitor C_1 (Miller capacitor) is connected between two high impedance points in the circuit which assures the good phase margin to the proposed design and C_1 is set to 40 pF.

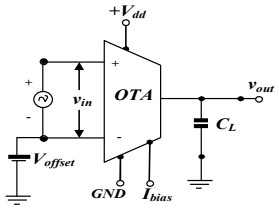

Fig. 6.- Proposed OTA operated in $+V_{dd}$ and GND with input offset.

Error amplifier in the negative feedback condition decides the output voltage (V_{out}) by comparing error signal constantly with V_{ref} that is 0.65V. According to the Equation (9), to get the desired V_{out}=4.5V, R_{f1}=14.8 $k\Omega$, and R_{f2}=2.5 $k\Omega$ are chosen.

B. *Design of the Pass Transistor and Load Capacitance in the Proposed LDO Regulator*

The most of the area in the chip of the LDO regulator is occupied by the pass transistor. It is the element in the circuit that carries the highest current and, hence, the dimensions are set in such a way that in withstand the maximum current according to the design specification given in Table I. The current flowing through the pass transistor is dependent on its dimensions, and the dimensions also influence the drop-out voltage of the proposed LDO. The main advantage of using the MOSFETs as the pass transistor is that, in addition to some gain, it also self protected to short circuit current and hence the additional short circuit protection circuit is not needed to some extent. In the proposed design of LDO regulator shown in Fig. 5, the pass transistor element is the pMOS transistor whose dimensions are set to withstand maximum output current of 450 mA, and also to get the dropout voltage of 0.5V at these maximum loading conditions according the specifications in Table I. Thus, dimensions are W=8000 μm, and L=1 μm. Since the usage of pMOS as pass transistor in open drain configuration, there is an issue in the output impedance being very high, causing a pole within the unity gain frequency, decreasing the phase margin. Therefore, there is needed an external load capacitance (C_L) with small value of internal resistance R_{ESR} so that it forms a zero, nullifying the effect of pole formed by high output impedance. In the considered case, C_L=35nF is chosen. Thus, the proposed LDO regulator has the decent DC gain of 32.6 dB with UGB (gain bandwidth product) equal to 18.68 kHz at no load condition. Simulation results showing important characteristics of the LDO like load regulations, line regulation, PSRR, etc., are also discussed in the Section 4.

IV. Simulation Results and Observations

All the proposed circuit blocks are built in Cadence Hit-Kit V3.70, using a 0.35 μm (c35b4c3) CMOS technology. It is simulated using the Specter software, using the BSIM-3.3 as the MOSFET model.

A. *Operational Transconductance Amplifier*

The proposed OTA as in Fig. 4 is built and simulated with $+V_{dd}$=5 V, $-V_{ss}$=-5 V, and with the bias current I_{bias} = 50 μA. The circuit is simulated in order to obtain some parameters and is compared with the results got by classical OTA shown in Fig. 3. Open loop AC Response of the proposed OTA is plotted and shown in Fig. 7 for the load capacitance C_L=0.4 nF and in the no-load condition. It should be noted that the gain is directly proportional to the small values of load resistance R_L. The results showed that DC gain A_V=101.13 dB, UGB=4.5 MHz with PM=59.17º.

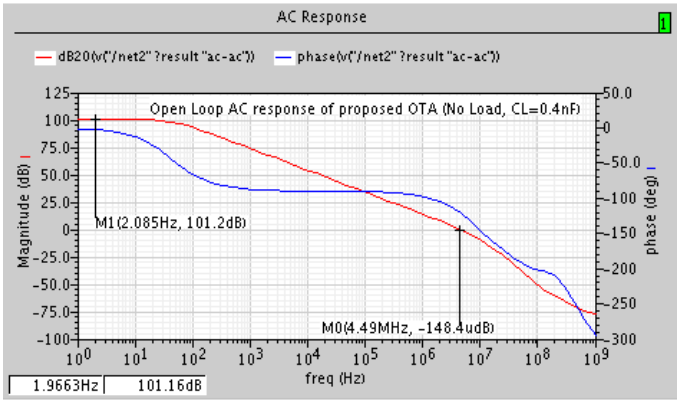

Fig. 7.- AC-Response of the proposed OTA, with C_L=0.4 nF, R_L=∞.

In addition, the proposed OTA circuit is simulated with C_L=1 nF. The DC gain was same, but the UGB=1.98 MHz with PM=75.3º, whereas in the classical OTA, the UGB=2.316 MHz with PM=81.07º. This boosting up of the DC gain in the proposed OTA compared to classical OTA under no load conditions is due to the increase in the output impedance thanks to the cascoded current mirrors in the first one. The DC gain under no load condition matches with Equation (8).

Another important parameter, the output impedance, is evaluated by simulating the circuit with differential inputs grounded and applying an AC-voltage source at the output node, with C_L=1 nF, by finding the current through that voltage source. Fig. 8 shows the output impedance Z_L(s) with R_L=∞, with respect to frequency change in proposed OTA. From this figure, it can be seen that the large signal output impedance (R_O) in the proposed OTA is 1.35 $M\Omega$ which is a good high output impedance, thanks to the cascoded current mirroring technique in proposed OTA.

Another parameter that decides the gain is $g_{m(1,2)}$ of the input differential pair MOSFETs. It is found out experimentally from Fig. 7 and 8, and using Equations (8) and (3) in no load condition. From these figures, the values of R_O and DC gain A_v can be obtained, with a gain factor α set to 20. Substituting appropriate values, it is found that $g_{m(1,2)}$=2.12 mS. This value suits very well with the theoretical value found out using the model file parameters (k_n, V_{tn}) and DC current as I_{bias}/2, i.e., 2.204 mS.

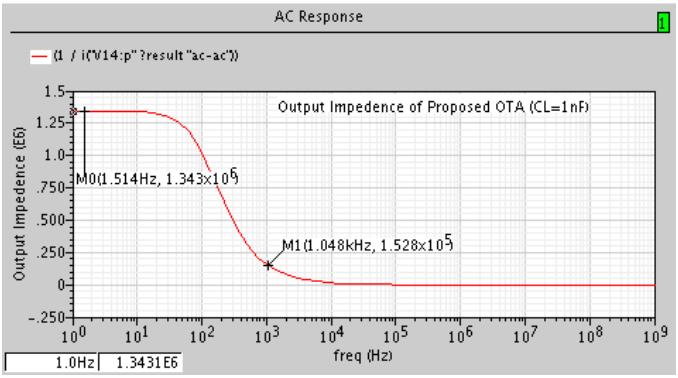

Fig. 8.- Output impedance vs. frequency of the proposed OTA.

B. *LDO Voltage Regulator*

Fig. 5 shows the overall proposed circuit of LDO regulator with three aforementioned main parts: The error amplifier (based on the previously proposed OTA), the band-gap reference circuit and the pass transistor. This circuit was built and simulated with V_{in} ranging from 5V to 20V, I_{bias}=50 µA and it is found that the designed circuit fits to the specifications mentioned in Table I. Tables III and IV show the summary of the simulation results obtained for band-gap reference voltage and LDO regulator circuits respectively.

TABLE III.- SIMULATION RESULTS OF BAND-GAP REFERENCE VOLTAGE CIRCUIT.

Parameters	***Values***
V_{ref} at T=25 °C	653 mV
T_γ	0.025 mV/°C
Line Regulation	0.44 mV/V
Power drawn, V_{in}=5 V	0.54 mW

TABLE IV.- SIMULATION RESULTS OBTAINED FOR THE PROPOSED LDO REGULATOR.

Parameter	***Value***		
	For R_L=∞	***For R_L=10 Ω***	***For R_L=45 Ω***
V_{out} for V_{in}=5 V	4.509 V	4.504 V	4.507 V
I_L for V_{in}=5 V	0 A	450.4 mA	100.1 mA
V_{drop}	0.06 V	0.5 V	0.15 V
Line regulation	3.2 mV/V	3.4 mV/V	3.2 mV/V
Load regulation	0.012 V/A		
V_{out} settling time I_L=0 – 450 mA in 1 µs	4.2 µs		
V_{out} settling time I_L=450 mA – 0 in 1 µs	40 µs		
PSRR (full load)	@ 100 Hz	54.45 dB	
	@10 kHz	34.31 dB	
V_{out} settling time V_{in}=5 V – 20 V in 1 µs	6 µs		
V_{out} settling time V_{in}=20 V – 5 V in 1 µs	4 µs		

The proposed LDO regulator circuit (Fig. 5) was simulated to obtain its most important characteristics and parameters [9] like DC response and line regulation, load regulation, PSRR, open loop AC Response, response for load variations, settling time for load variations, and transient responses for input variations. On the one hand, DC response of the LDO circuit is obtained for the different loading conditions R_L=10 Ω, 45 Ω and ∞. The typical response for R_L=10 Ω and ∞ are shown in Fig. 9. This DC response is used to spot out the drop-out voltage (V_{drop}) of the proposed LDO regulator by spotting the point where the V_{out} just reaches the constant value. Thus, by knowing the corresponding value of V_{in} , dropout voltage can be found. From figures, it can be seen that for R_L=∞, V_{drop}= 0.06V and for the full load conditions (R_L=10 Ω), the dropout voltage V_{drop}=0.5 V. This shows that there is a trade-off between the maximum load and the drop-out voltage, hence the user has to use this proposed LDO regulator according to the application requirements. From the plots of DC response (Fig. 9), the line regulation for corresponding R_L can be found out by considering V_{out} for V_{in}= 5V ~ 20V. Using Equation (15), it can be found out that line regulation for R_L=∞ is 3.2 mV/V, for R_L=10 Ω it is 3.4 mV/V, and for R_L=45 Ω it is 3.2 mV/V. On the other hand, load regulation is obtained by sweeping I_L from 0 A to 450 mA with V_{in}=5 V. From Fig. 10, load regulation is 0.012 V/A.

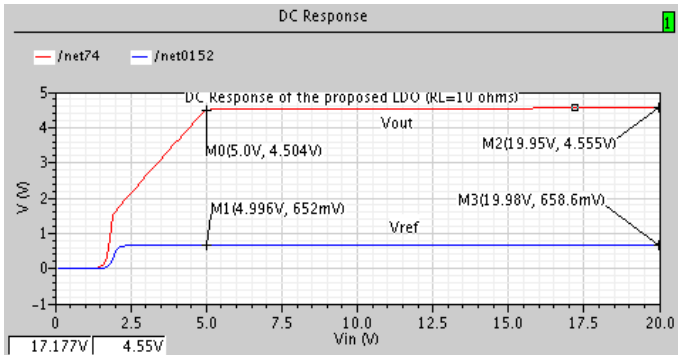

Fig. 9.- DC response of the proposed LDO and band-gap reference for full load condition.

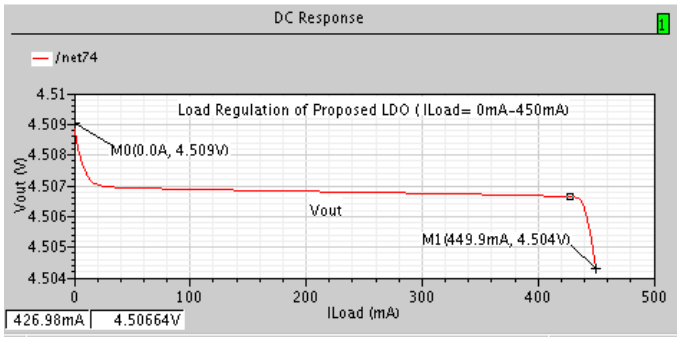

Fig. 10.- Load regulation of the LDO regulator, I_L=0 A – 450 mA.

Being V_{in}=5V, and R_L=∞, the current flowing through the supply is obtained and its value is 1.29 mA, which is usually referred the sum of the current needed to bias whole circuit with the leakage current through the feedback circuit in the error amplifier (quiescent current). This current is small compared to the max output rated current $I_{L(max)}$=450 mA, giving the power efficiency at full load condition as 89.74%. On the other hand, the V_{out}=4.509V for R_L=∞ and V_{out}=4.504V for R_L=10Ω, with satisfying the allowance initial design specifications shown in Table I.

Another important parameter considered is the power supply rejection ratio (PSRR), which decides the ripple rejection capability of the circuit. It is found the PSRR for two load conditions: No load and full load conditions, and it is found that under no load condition at 100 Hz, PSRR=56.26 dB, and at 10 kHz, PSRR=46.53 dB. On the other hand, for full load condition at 100 Hz, PSRR=54.45 dB, and at 10 kHz, PSRR=34.31 dB (Fig. 11). The open loop AC Response of the

LDO regulator is shown in Fig. 12. It can be found that DC gain is 32.56 *dB*, *UGB*=18.68 *kHz* with the *PM* of 91.35º, hence assuring the stability of the circuit.

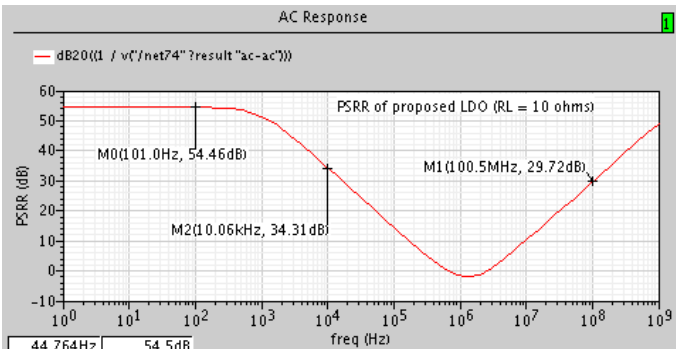

Fig. 11.- PSRR of the LDO regulator, R_L=10 Ω.

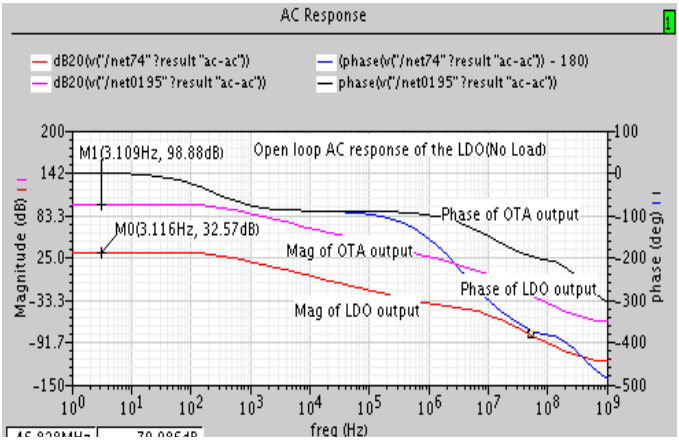

Fig. 12.- Open loop AC response at the LDO and error amplifier outputs.

Finally, response for load variations of the proposed LDO and the settling times for full load variations are depicted in Fig. 13, and transient responses for input variations are given in Fig. 14.

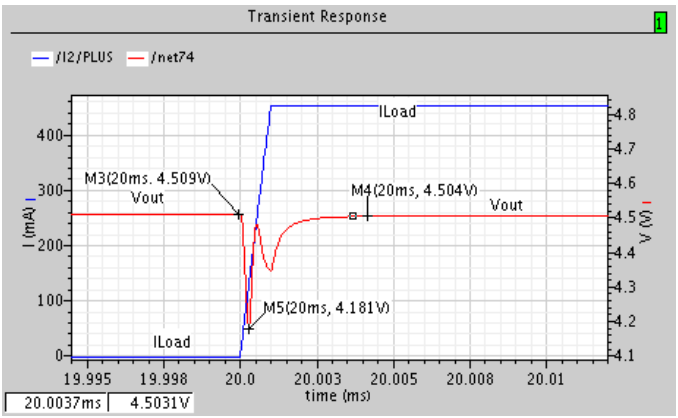

Fig. 13.- Settling time of V_{out} for a step I_L=0 *A* – 450 m*A* in 1 µ*s*.

V. CONCLUSIONS

A low drop-out voltage regulator based on a two-stage cascoded operational transconductance amplifier (OTA) as error amplifier has been designed in a 0.35 µ*m* CMOS technology and simulated in Cadence Spectre software with the MOSFET model of BSIM -3.3. The measured regulated output voltage is 4.5*V* with a maximum current of 450 *mA*. The LDO regulator design has the dropout voltage of 0.5 *V* at full load condition, also with good line and load regulations of 3.2 *mV/V* and 0.012*V/A*, respectively. The PSRR of the design was found out to be 54.45 *dB* at 100 *Hz* and 34.31 *dB* at 10 *kHz* under full load condition. The LDO voltage linear regulator includes a band gap reference circuit that provides the constant reference voltage of 0.653 *V* with a temperature co-efficient (T_y) of 0.025 *mV*/ºC.

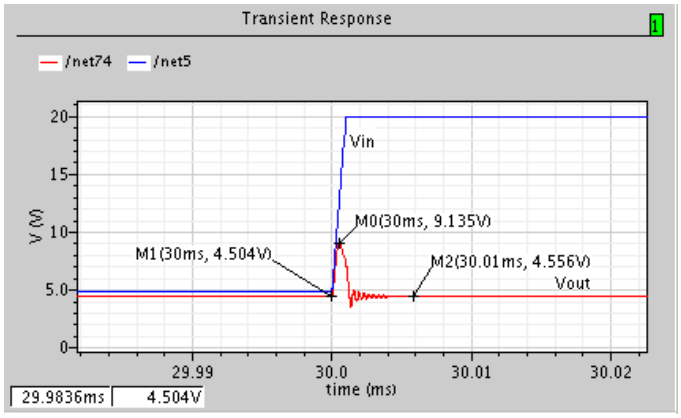

Fig. 14.- Response of V_{out} for V_{in}=5 *V* – 20 *V* in 1 µ*s* for full load.

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