

Approach to the Implementation and Modeling of LDO-Assisted DC-DC Voltage Regulators

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Abstract—This paper presents the design of an LDO-assisted DC-DC voltage regulator in Cadence Virtuoso® based on a 350-nm CMOS technology. This kind of voltage regulator consists of a switching converter together with a classic or LDO (low drop-out) linear voltage regulator. While the linear regulator provides the constant output voltage, the switching converter conducts nearly all the current provided to the output load, and keeping the regulator current close to zero where the higher efficiency is achieved. In addition, this paper shows the modeling in Matlab/Simulink. Notice that, this modeling is mandatory in order to predict and assure the stability of the circuit. In addition, it will help to improve the transient response and performance of the circuit.

Keywords—DC-DC Converters; Low Drop-Out (LDO) Voltage Regulators; Power Electronics; Modeling of Power Converters; Matlab/Simulink.

I. INTRODUCTION

There are substitute renewable energies that are known as cutting-edge technology. They will be fundamental subsystems in electrical energy grids in the future. This is the case, for instance, of high voltage DC (HVDC) transmission. Since they cannot be connected directly, and in order to interconnect these subsystems into the grid to enlarge the possibility of integration, power electronic converters and devices will be required. Because power regulators are quite more flexible in terms of control, have become the most concerning technology for researchers in modern power system.

In fact, DC-DC power regulators are widely used in a significant variety of applications in terms of their high efficiency and low output ripple, such as portable devices, energy-harvesting applications and radio frequency (RF) power amplifiers that are in need of highly efficient and stable power supply [1]–[3].

There are two main approaches for the design of DC-DC power regulators such as using either switching regulators or linear regulators. On the one hand, DC-DC switching regulators could show residual or spurious ripples in the output voltage due to the switching process. Thus, the use of linear regulator would be necessary to eliminate these ripples and

produce the surplus of the current that is not provided by the switching regulators [4].

In general, linear-assisted hybrid voltage regulators usually consist of a switched-inductor (buck or step-down) converter with a linear regulator (standard NPN Darlington pair, LDO or quasi-LDO) in order to provide the desired output current flowing through the load with regulated constant output voltage. Previous researches have been done to minimize the existing impediments such as low efficiency and high power dissipation [5],[6]. Other works have proposed topologies in order to optimize the performance of buck converter or improve the control techniques [7]–[9]. Moreover, other researches have optimized the design using push-pull linear regulator [10].

In this article, a proposal of linear-assisted DC-DC regulator and its modeling is presented to inquire the control loop stability. In fact, in order to carry out the stability study, a model of the whole system is necessary. In particular, on the one hand, an LDO regulator is used that has benefits of maximizing the use of available input voltage and can yet regulate the input voltage while both input/output values are close to each other, minimizing internal power loss. In this structure, the conventional linear regulator is replaced by an LDO in order to obtain the better performance (lower output ripple and better efficiency).

In addition, an approach to the modeling of the circuit is presented in order to analyze the stability based on critical parameters' variation.

II. STRUCTURE OF THE PROPOSED LDO-ASSISTED DC-DC REGULATOR

In the proposed circuit shown in Fig. 1, the switching converter is connected in parallel with an LDO regulator, providing the desired output current and voltage to the load. As it is well known, the LDO regulator, thanks to the feedback loop of the operational amplifier and resistors R_1 and R_2 , continuously compares the reference V_{ref1} and the feedback sample obtained from the output voltage in order to provide a constant output voltage. Therefore, this output voltage, V_{out} , is given by:

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_{ref1} \quad (1)$$

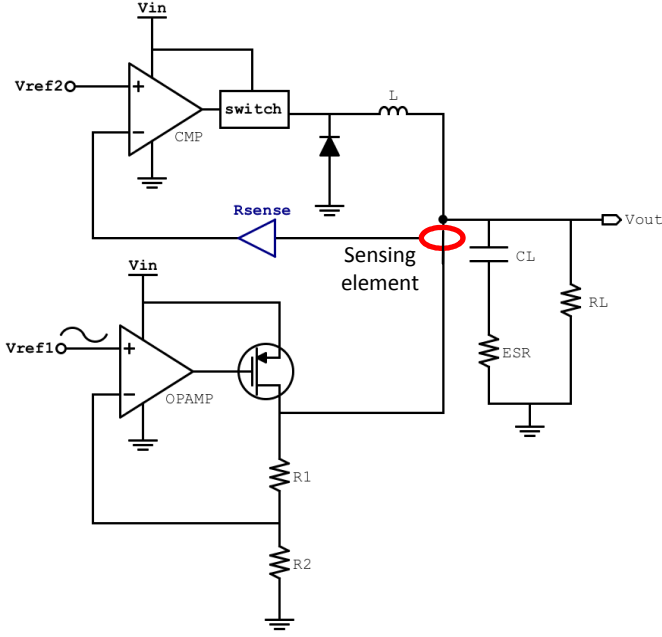


Fig. 1. Proposed schematic of the proposed LDO-assisted DC-DC regulator.

Since the output current is obtained by the sum of both the linear regulator's and the switching converter's currents, and it is constant (in steady state), the conduction and cut off of the switch element is controlled by the comparator (*CMP*) to conduct the majority of the output current by the switching converter. Consequently, the analog comparator compares a reference voltage, V_{ref2} , with the regulator's sensed current flowing through the linear regulator. This reference voltage, V_{ref2} , fixes a boundary current or threshold current, to control the switching frequency, I_γ . In this work, the current sensing through the linear regulator is obtained by a low-value resistor (1Ω in this case), and is defined by the following expression:

$$I_\gamma = \frac{V_{ref2}}{R_{sense}}, \quad (2)$$

where R_{sense} is the transresistance gain of the sense element (current-to-voltage converter).

When the load current is below the threshold current, the output of the comparator will be low and will set the switch off. Thus, the current through inductor L will decrease, and the regulator current will increase to provide all the output current that flows through the load. However, on the other hand, when the load current increases, the comparator will switch to high and turn on the switch of the switching converter. Therefore, the inductor current I_L will increase. This will make the regulator current to decrease linearly as it can be seen in Fig. 2.

In this work, all the simulations are based on a $0.35\text{-}\mu\text{m}$ CMOS technology in Virtuoso Cadence®.

In this simulation, with the input voltage of 3.3 V , a constant value of 1.65 V is obtained at the output terminals, and the load current is fixed at 100 mA that is mostly provided by inductor current. Therefore, it keeps the regulator current close to zero. In Fig. 3, the transient response of the circuit with the variation of V_{in} from 3.3 V to 4.3 V is shown, and it demonstrates a good line regulation as well as the load regulation from 200 mA to 300 mA variation of load current

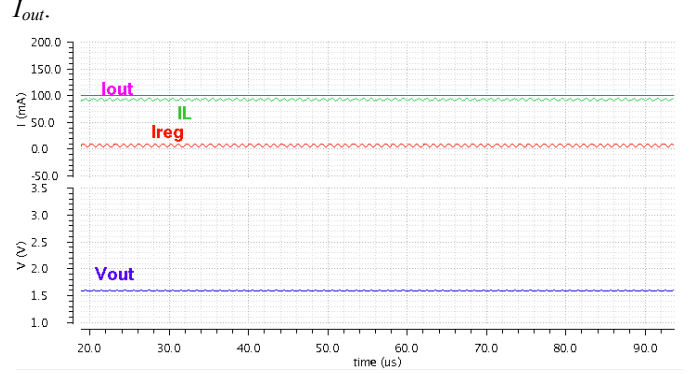


Fig. 2. Transient response of the proposed LDO-assisted DC-DC regulator.

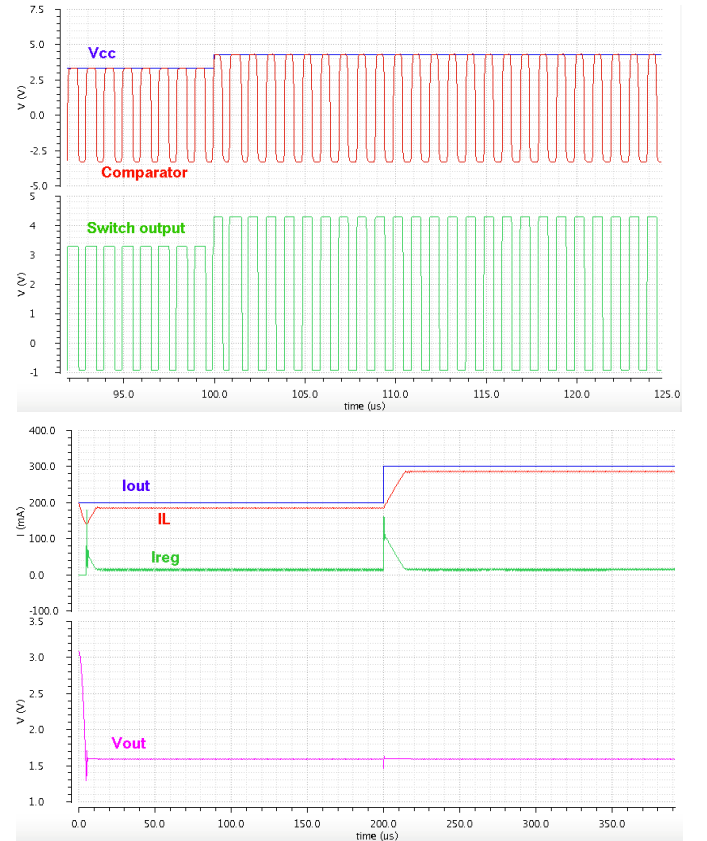


Fig. 3. Transient response for the line and load regulation, respectively, of the proposed LDO-assisted DC-DC regulator.

III. MODELING OF THE PROPOSED LDO-ASSISTED DC-DC REGULATOR

In order to analyze the circuit's behavior (and, of course, its possible instabilities), it is necessary to study the mathematical modeling of the proposed circuit. This modeling will provide the critical parameters of the circuit that affect the global performance (transient response, load and line regulations, etc.), and stability of the whole system.

In Fig. 4, a simplified block diagram model of the LDO-assisted regulator is shown. In this model, the linear regulator current (I_{LIN}) is obtained from the output current, I_{out} , and the switching converter current, I_{sc} :

$$I_{LIN} = I_{out} - I_{sc} \quad (3)$$

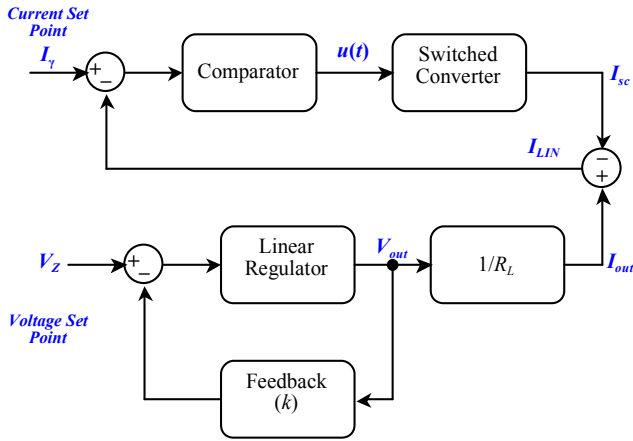


Fig. 4. Basic block diagram of the modeling of the proposed LDO-assisted regulator.

On the one hand, Fig. 5 shows the DC-DC buck (step-down) converter circuit. The buck converter is considered with

an ideal switch that has the switching period of T . When the switch is ON, the current through the inductor (L), load capacitor (CL) and its equivalent series resistor (ESR) is derived from the equations below:

$$i_{sc}(t) = i_L(t) - i_c(t) \quad (4)$$

$$i_L(t) = \frac{1}{L} \int (v_{in}(t) - v_{out}(t)) dt \quad (5)$$

$$v_{out}(t) = v_c(t) + v_{ESR}(t) = \frac{1}{C} \int i_c(t) dt + ESR \cdot i_c(t) \quad (6)$$

$$i_c(t) = C \frac{dv_{out}(t)}{dt} - C \cdot ESR \cdot \frac{di_c(t)}{dt} \quad (7)$$

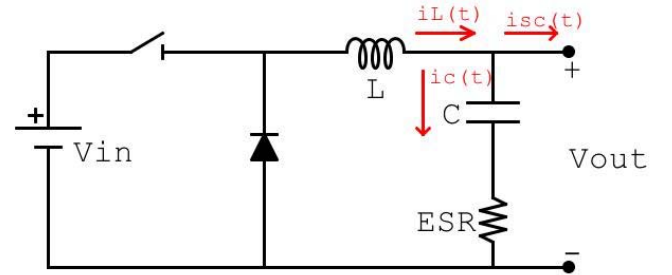


Fig. 5. Basic DC-DC buck converter circuit.

The obtained expressions (5) and (7) are implemented in Matlab/Simulink® as shown in Fig. 6 using linear blocks (summing, gains, etc. blocks) subsequently applied to integrator and derivative blocks in order to obtain the switching converter's output current ($i_{sc}(t)$). In simulations presented in this article, the inductor value used in all the simulation presented is $200 \mu H$.

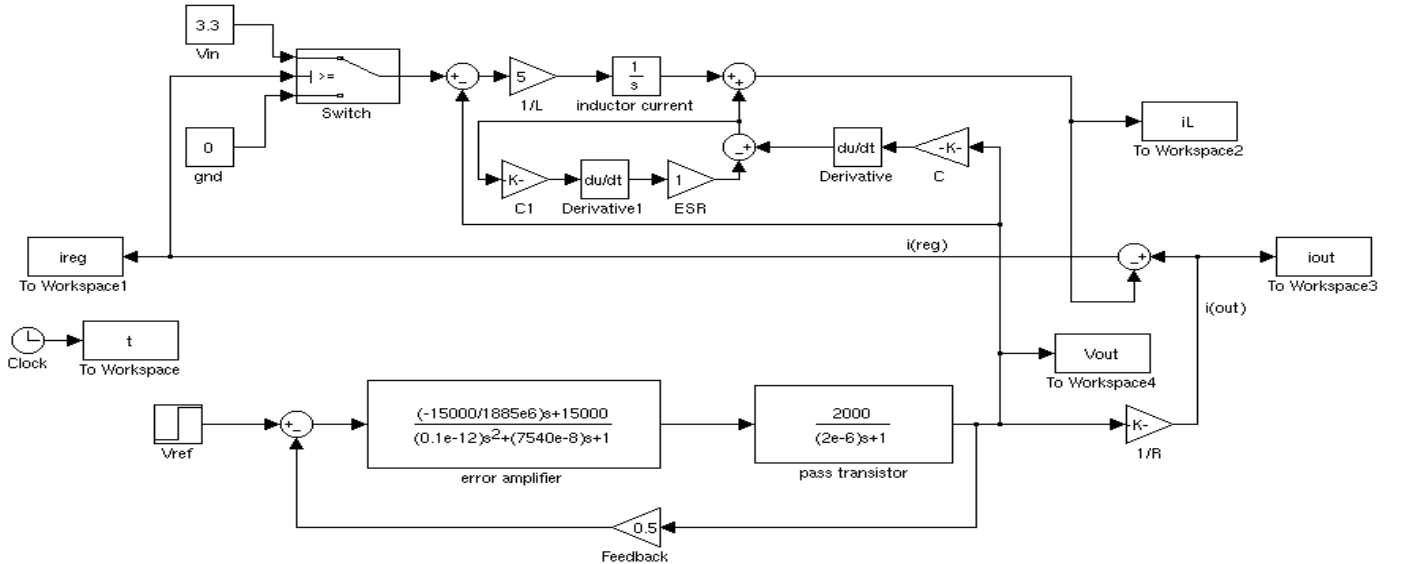


Fig. 6. Proposed modeling diagram of the proposed LDO-assisted DC-DC regulator.

On the other hand, the linear regulator block consists of an error amplifier (Fig. 7), a pass transistor and the feedback loop. To obtain the transfer function for each block, the equivalent circuits are shown below. The transfer function of the operational amplifier is given in equation (8), and it shows two poles (P_1, P_2) and a zero (Z) generated by the Miller capacitor (C_c).

$$H_{oa}(s) = \frac{V_m}{V_{ref}} = \frac{A_{oa} \left(1 - \frac{s}{Z}\right)}{\left(1 + \frac{s}{P_1}\right) \left(1 + \frac{s}{P_2}\right)} \quad (8)$$

$$\begin{cases} A_{oa} = g_{m1} g_{m2} r_{o1} r_{o2} \\ Z = g_{m2} / C_c \\ P_1 = 1 / g_{m2} r_{o1} r_{o2} C_c \\ P_2 = g_{m2} / C_2 \end{cases} \quad (9)$$

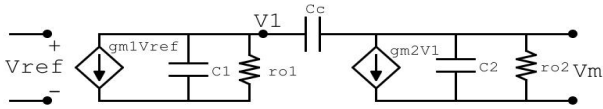


Fig. 7. Operational amplifier's equivalent circuit with Miller effect due to its compensation capacitor (C_c).

On the other hand, Fig. 8 shows the equivalent circuit of the pass transistor. The transfer function of this pass transistor is presented in expression (10), and it depends on the gain of transistor (that is, the product $g_m \cdot r_{pass}$) and its capacitor C_{pass} .

$$H_{pass}(s) = \frac{V_{out}}{V_m} = \frac{g_m r_{pass}}{1 + C_{pass} r_{pass} s} \quad (10)$$

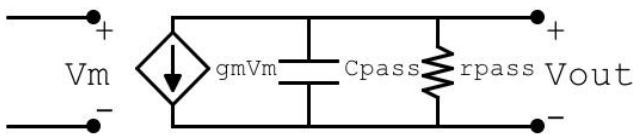


Fig. 8. Pass transistor equivalent circuit.

Finally, the feedback value that was introduced earlier in equation (1) and obtained from the ratio $R_2/(R_1+R_2)$, is applied to the inverting input of the operational amplifier (error amplifier).

IV. SIMULATION RESULTS

The proposed model that is introduced in previous section, guaranties an accurate model for the proposed LDO-assisted DC-DC regulator's behavior. In particular, Fig. 9 shows simulation results of the transient response of the proposed

LDO-assisted DC-DC regulator using the proposed Matlab/Simulink[®] model. In this particular simulation, the desired output voltage is fixed to 1.6 V, providing an output current equal to 100 mA in the steady state, and the maximum output current flowing through the LDO regulator (I_y , according to expression (2)) is fixed to 2 mA.

It is important to highlight that results obtained from the model proposed in this article match with the results obtained from the transistor-level circuit obtained from Virtuoso Cadence[®].

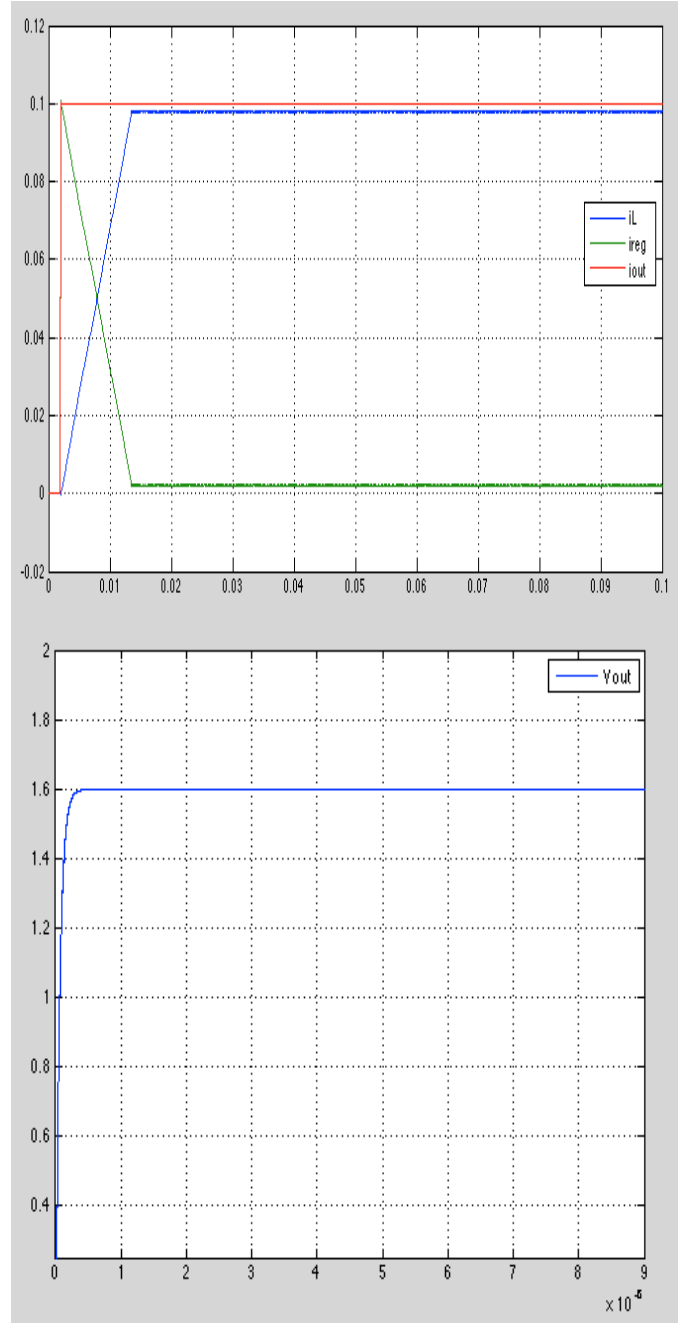


Fig. 9. Transient response of the proposed model in Matlab/Simulink[®] for the LDO-assisted DC-DC regulator.

The circuit could be unstable due to some parameters such as output capacitor (C_L in Fig. 1), and its equivalent series resistor (ESR) connected in parallel with the load resistance. In fact, the existence of these parameters is important in order to predict the transient behavior of the LDO-assisted regulator. Simulation results show that the frequency response of the circuit is also quite sensitive to output capacitor C_L and its corresponding ESR .

In Fig. 10, simulation results for different values of capacitor C_L are obtained. The closed-loop gain is 6 dB since we have an output voltage twice higher than input voltage. For an output capacitor of 100 nF, the gain and phase margin are 59.8 dB and 50 degrees, respectively. In these conditions, the gain margin for $C_L=100$ pF is reduced to 28 dB, and phase margin increased to 114°.

On the other hand, as it is obtained in Fig. 11, for $C_L=10$ μF and $ESR=1$ Ω, gain margin of about 60 dB, and phase margin of 117° is obtained. Otherwise, by changing the ESR to 0.1 Ω, a significant reduction in phase margin is observed, obtaining around 46 degrees. In addition, it is also observed that varying the gain of operational amplifier does not affect the stability of the LDO-assisted regulator.

Since there are just a few capacitors with impedance more than 2 Ω, the upper limit of the ESR can be ignored but for this proposal, the typical lower limit is 0.1 Ω. In this regard, Fig. 12 shows a Bode plot for $C_L=4.7$ μF and $ESR=0.01$ Ω. It shows a phase margin of 5.95° and a gain margin of about 99 dB, which make the system unstable.

V. CONCLUSION

On the one hand, in this paper, the proposal of an LDO-assisted DC-DC regulator based on a 0.35 μm CMOS technology and its simulation results to observe its performance is obtained.

On the other hand, in general, LDO regulators are prone to instabilities due to the position of their poles and zeroes. This is also the case in DC-DC LDO-assisted topologies. Therefore, in addition, the paper shows the modeling in Matlab/Simulink®.

As a consequence, the proposed modeling will help to characterize the critical parameters such as output capacitance and its equivalent series resistance that have influence on these possible instabilities and, in general, in the performance of the DC-DC LDO-assisted voltage regulator. From this modeling the performance of the system could be easily improved by varying the parameters value.

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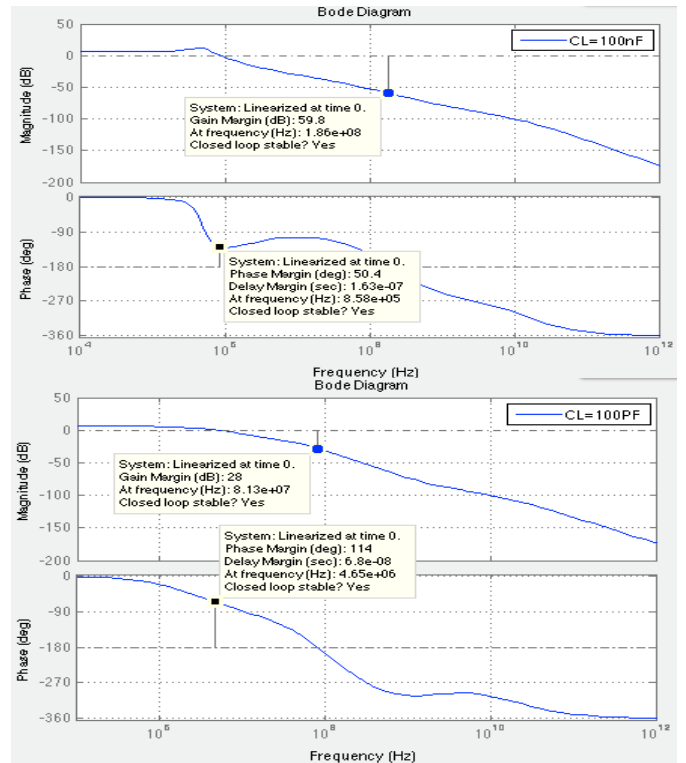


Fig. 10. Bode plot for $C_L=100$ nF and 100 pF.

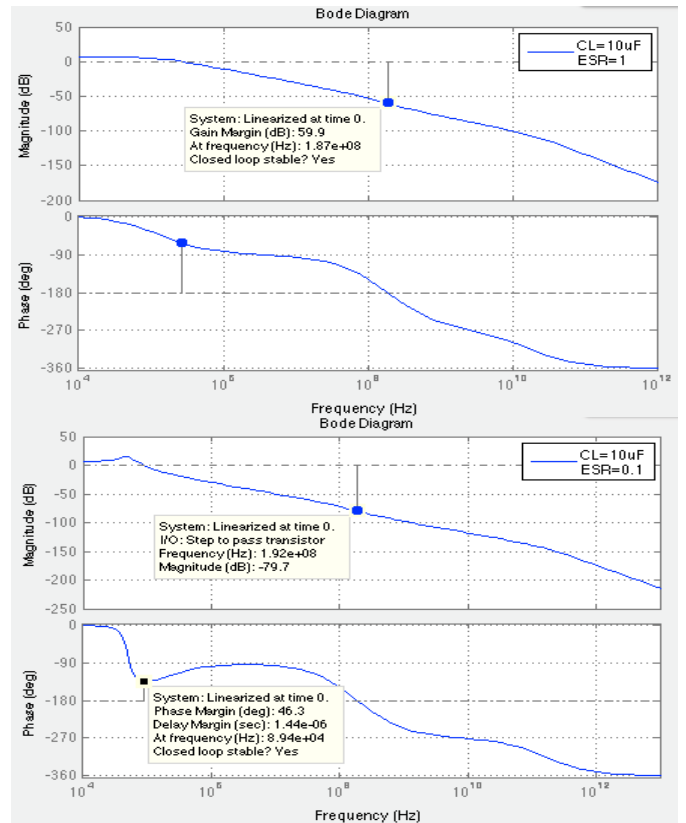


Fig. 11. Bode plot for $C_L=10$ μF, and $ESR=1$ Ω and 0.1 Ω.

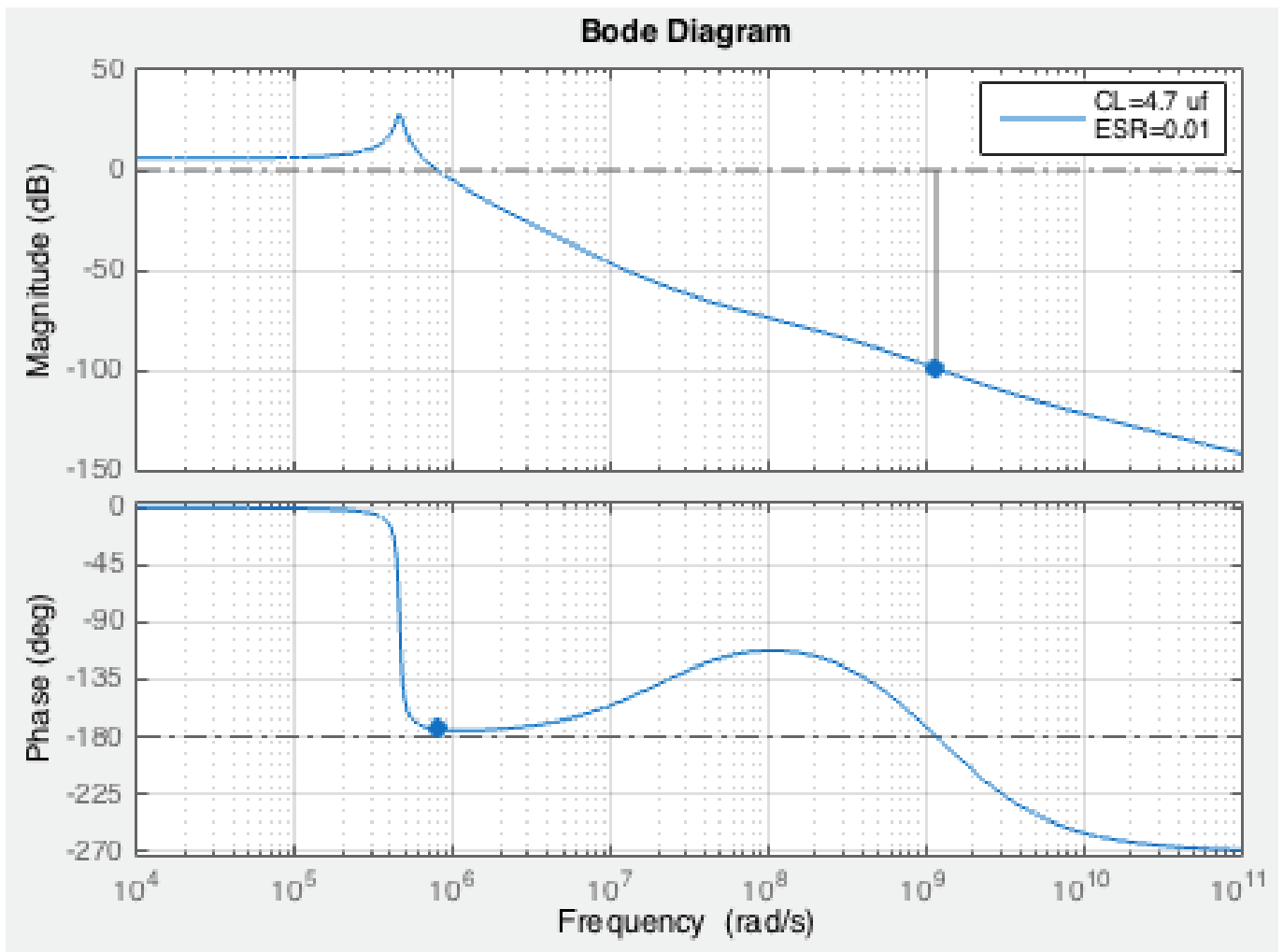


Fig. 12. Bode plot for $C_L=4.7 \mu F$, and $ESR=0.01 \Omega$.

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