A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory

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***Abstract*—The trend in power electronic applications is to reach higher power density and higher efficiency. Currently, the wide band-gap devices such as Silicon Carbide MOSFET (SiC MOSFET) are of great interest because they can work at higher switching frequency with low losses. The increase of the switching speed in power devices leads to high power density systems. However, this can generate problems such as overshoots, oscillations, additional losses and electromagnetic interference (EMI). In this paper, a novel active gate driver (AGD) for improving the SiC MOSFET switching trajectory with high performance is presented. The AGD is an open-loop control system and its principle is based on gate energy decrease with a gate resistance increment during the Miller Plateau effect on gate-source voltage. The proposed AGD has been designed and validated through experimental tests for high-frequency operation. Moreover, an EMI discussion and a performance analysis were realized for the AGD. The results show that the AGD can reduce the overshoots, oscillations and losses without compromising the EMI. Besides, the AGD can control the turn-on and turn-off transitions separately and it is suitable for working with asymmetrical supplies required by SiC MOSFETs.**

***Index Terms*—Driver circuits, electromagnetic interference (EMI), silicon carbide MOSFET, switching losses, switching transients.**

I. Introduction

THE trend in power electronic applications is to reach major power density, higher efficiency, and reliability. In this regard, the power device should be able to work at high frequency with low total losses and work in higher temperature. Nowadays, studies have shown the advantages of wide band-gap power devices in comparison with silicon devices [1]–[3]. The new progress in power devices technology establishes that silicon carbide (SiC) technology, and Gallium Nitride (GaN), are the solutions for the needs faced by power converters nowadays [4]. Accordingly, the SiC devices are a mature technology and they have been used in different applications, such as renewable energy [5], [6], drivers for electrical machines [7], and power converters for Hybrid and Electric Vehicles [8].

The challenges for the new power converters with SiC devices such as BJTs, JFETs, MOSFETs and even IGBTs, are to reach better performance and reliability for hard-switching and even soft switching conditions. In the specific case of the SiC MOSFETs, several studies have shown that despite its advantages, the SiC MOSFETs can present problems in high-frequency operation. When a power SiC MOSFET operates in high frequency, over-voltage and over-current can present due to high switching speed and stray inductances, which produce electromagnetic interference (EMI) and decrease performance [2], [9], [10]. On the one hand, when the PCB layout is optimized, the stray inductances can be reduced. On the other hand, the increment of gate resistance can reduce, even removing this problem, however, efficiency can be affected. Also, snubber circuits have been applied as an alternative [9], [11], [12], but additional components such as inductors or capacitors increase the losses and reduce efficiency of the power converters. Then, the solutions to compensate the switching problems and increase the SiC devices performance are focused on the development of gate driver circuits [13].

This paper presents a new technique design for reducing the overshoots and oscillations provoked by high *di/dt* and *dv/dt* slopes while improving the switching trajectory of SiC MOSFETs with low total losses. The main concept of this approach is to decrease the energy realizing a gate resistance increment during the Miller Plateau effect where the overshoots are commonly present.

The paper is organized as follows: first, a study about gate driver solutions is discussed in section II. The operation principle of the proposed gate driver is presented in section III. Section IV focuses on the AGD design and validation through experimental demonstrations. After that, an analysis and discussion of gate driver performance are realized and a study of losses, costs and electromagnetic interference is developed in section V. Finally, section VI concludes this paper.

II. A Review of Conventional Gate Drivers for SiC MOSFET

A. Gate Drivers Overview for Power Devices

Currently, high switching frequency is required for improving the performances of the power electronics in new applications. Regarding the literature, when a power device works in high frequency the *di/dt* and *dv/dt* slopes are increased due to stray inductances and parasitic capacitances,

which leads to oscillations and overshoots in current and voltage [14]. On the one hand, with a large gate resistor, the overshoots are reduced, but the losses are increased. Besides, if the gate resistor value is small, the losses can reduce but the current and voltage overshoots are increased, which could involve EMI problems and stress in the devices [15], [16]. Several authors have developed studies for the trade-off between loss, stress, and EMI [17]. Other solutions have reached better performance applying snubber circuits in Si and SiC devices [10]. Nevertheless, these circuits can leave high stress in additional components such as inductors, capacitors, and diodes. Additionally, when using a better design of PCB layout the stray inductances are reduced, and consequently the EMI problems can also be lower. Furthermore, many gate driver circuits have been proposed for silicon power devices, such as different variations of resonant gate drivers [18], [19] and AGD [15], [20]. Also, gate drivers for SiC devices such as SiC BJTs [21] and SiC JFETs [22], [12] have been developed. All these techniques could be applied for SiC MOSFET, but these drivers must be adapted due to the differences between the different Si and SiC devices.

B. Gate Drivers as a Solution for Improving the SiC MOSFET Devices Performance

The SiC MOSFET is being widely studied in power electronics systems due to its advantages, but it has low transconductance in comparison with silicon devices such as MOSFET or IGBT. Accordingly, higher gate-source voltage levels are required for turn-on. Moreover, the total pulse of the gate-source voltage is commonly asymmetrical. Therefore, different values of R_g to improve its performance in both turn-on and turn-off transitions are required [13]. The conventional two resistance gate driver is commonly used for controlling the turn-on and turn-off path. Although this configuration controls the turn-on and turn-off path separately, it is limited with regard to the trade-off between efficiency and EMI problems. A boost gate-drive solution was introduced in [23]. The main advantage of this gate driver is the losses reduction. However, the oscillations and overshoots can be kept but cannot be reduced. The same principle was presented in [24]. The structure of the driver circuit is a half-bridge converter using a GaN device. Although the AGD works at high frequency and medium power, it results in a complex circuit.

In [25] a circuit driver for controlling *di/dt* and *dv/dt* for turn-off transition was presented. This driver consists of a close-loop control with an optically switched-drive. Results showed that this driver reduces the losses and overshoots. However, a complex control and laser devices are required. In addition, the turn-on state is not considered.

There are other gate driver circuits for improving the behaviour of the SiC MOSFETs. The resonant gate driver or current gate driver have been developed as efficient and simple solutions. In [26] a resonant gate driver was developed. The driver can work at high frequency and it can reduce the SiC MOSFETs switching losses. However, the EMI was not considered and the gate driver solution adds problems with the switching delay in turn-off. Additionally, a negative gate-source voltage was not considered, which could affect the whole performance. In [27], a complete AGD was developed for suppression of crosstalk of a phase-leg converter, but this driver is focused mainly on problem transition between two devices. Also, an AGD was developed by [28], the results show that the solution can reduce the EMI with high efficiency; however, the close control-loop used is a complex system. In accordance with the previous description, most of the solutions only consider SiC MOSFET losses reduction.

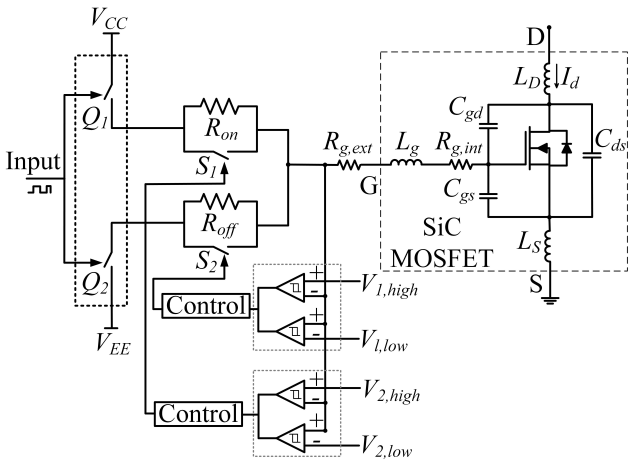

Fig. 1. General scheme of the proposed AGD.

Although several driver circuits face the EMI problems reduction, only a few studies consider reducing both losses and EMI. Accordingly, new techniques or circuit drivers should be developed to compensate for EMI problems and losses reduction in SiC MOSFETs. Taking into account the previous review, if the energy during the time interval where the overshoot and oscillations is decreased, the EMI problems can be reduced. This energy reduction can be reached by changing the R_g resistance around the Miller Plateau effect. Therefore, an AGD design based on a simple open-loop control can be designed. In section III, a new proposal of the AGD is presented and analysed.

III. Proposed Gate Driver and Operating Principle

The general schematic circuit of the proposed AGD is depicted in Fig. 1. The circuit consists of a conventional totem-pole drive and two switches S_1 and S_2 placed in the turn-on and turn-off path with two resistances in parallel. The switches are controlled by two window comparator configurations, which compares the gate-source voltage (v_{gs}) with four reference voltages. Also, a simple control block is on the feedback path for coupling the output signals of the comparators and to generate delays. So, it produces the expected pulses and suitable voltages for switches S_1 and S_2.

In addition to internal resistance ($R_{g,int}$) of the device, an external gate resistance $R_{g,ext}$ is considered because the switches S_1 and S_2 could have a very low on-resistance ($R_{ds(on)}$) and consequently, the power MOSFET could be outside of the safe operation area (SOA) when S_1 and S_2 are carrying current. Therefore, $R_{g,ext}$ is connected in series with

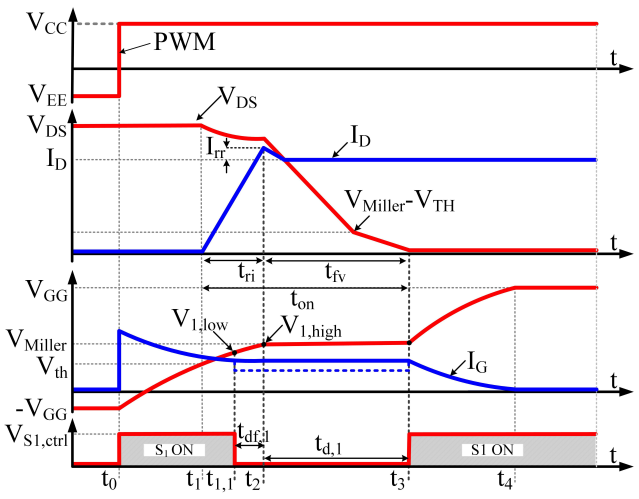

Fig. 2. Turn-on SiC MOSFET waveforms and control signals for S_1 of the AGD.

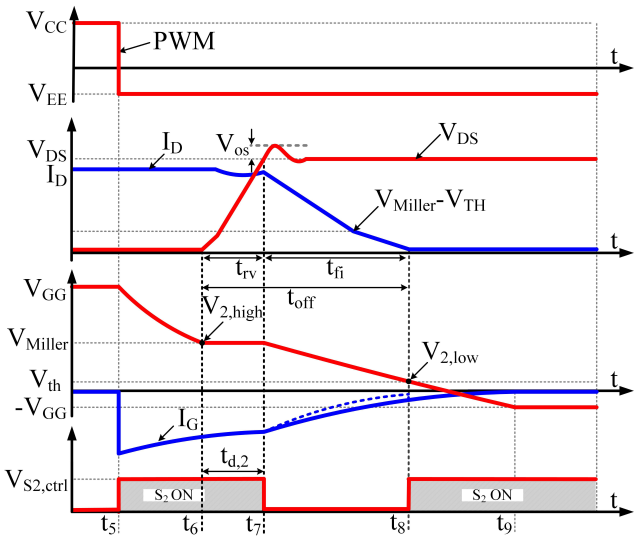

Fig. 3. Turn-off SiC MOSFET waveforms and control signals for S_2 of the AGD.

the driver. It should be worth mentioning that the minimum $R_{g,ext}$ is considered according to the recommended value in the datasheet and it is of 6.3 Ω in this work for the main device studied. On the other hand, $R_{g,int}$ is usually very low and is found in the note application. For this study $R_{g,int}$ was less than 1 Ω.

The AGD principle is to increase the gate resistance value about the Miller Plateau zone of the voltage v_{gs}, in both turn-on and turn-off conditions. Thus, the current and consequently the energy are decreased in the interval where overshoots occur, as shown in Fig. 2 and Fig. 3. Taking into account Fig. 1, the gate resistance is increased due to the switches S_1 and S_2 being off during $t_{1,1} - t_3$ and $t_7 - t_8$ respectively. Therefore, only R_{on} and R_{off} are carrying current during these intervals.

Switching off the S_1 and S_2 switches is reached through a comparison realized by windows comparators that compare four voltage references; $V_{1,high}$, $V_{1,low}$ and $V_{2,high}$, $V_{2,low}$, with v_{gs}. In addition, two delays $t_{d,1}$ and $t_{d,2}$ are applied to reach the expected control signal.

On the one hand, the reference voltage $V_{1,low}$ could be defined at time t_2, where v_{gs} voltage reaches the Miller Plateau voltage. However, the delay $t_{df,1}$ of S_1 control which is the total delay caused by MOSFET, the coupling circuit, and comparators, should be considered for ensuring the timely switching of S_1 and reach the optimal behaviour of the turn-on transition. On the other hand, $V_{2,high}$ is considered in t_6, where the Miller Plateau voltage is reached by v_{gs}, but the delay $t_{d,2}$ define the v_{ds} and i_{ds} slopes behaviour.

The voltages $V_{1,high}$ and $V_{2,low}$ should be properly defined. $V_{1,high}$ is defined as the Miller Plateau voltage, but the delay $t_{d,1}$ keeps the control signal high until the Miller Plateau zone has finished, because it is the point when v_{ds} reaches the minimum value as shown in Fig. 2. On the other hand, $V_{2,low}$ is considered equal to voltage threshold because it is the point where i_d current drops to zero, as shown in Fig. 3. The total delay caused by the S_2 MOSFET, the coupling circuit and the comparators for controlling the turn-off transition is considered, but it has no effect on the output signals.

A. Operating at Turn-on Transition

As depicted in Fig. 2, in t_0 the PWM signal rises to high, Q_1 and S_1 switches are activated, and v_{gs} starts to rise. While a constant I_g is generated to charge C_{gs} capacitance with $R_{g,on} = R_{g,ext} + R_{g,int}$. Then, in t_1 vgs reaches the threshold voltage ($V_{gs(th)}$) and the drain current (i_d) begins to rise. When v_{gs} reaches $V_{1,low}$ the switch S_1 is turned off and R_{on} conducts, therefore I_g decreases with $R_{g,on} = R_{on} + R_{g,ext} + R_{g,int}$. After the $t_{1,1}$, v_{gs} goes beyond $V_{1,low}$ and reaches the Miller Plateau voltage. In this time, i_d current matches the nominal value (I_d) and a peak of current arises due to the freewheeling diode effect. On the other hand, v_{ds} starts to fall, at that time the reference voltage $V_{1,low}$ is also reached and S_1 is turned off, when $t_{d,1}$ is over in t_3. The v_{gs} voltage starts to rise again in t_3. Finally, in t_4 v_{gs} reaches the V_{gg} and SiC MOSFET is in conduction mode. S_1 is active until the PWM signal rises again. The current slope of i_{ds} during turn-on transition is approximated from the following equation:

$$\frac{di_d}{dt} = g_{fs} \cdot \frac{V_{gg+} - V_{gs(th)} - \frac{I_d}{2 \cdot g_{fs}}}{C_{iss} \cdot R_{g,on}}, \tag{1}$$

where g_{fs} is the transconductance and $C_{iss} = C_{gs} + C_{gd}$ is the input capacitance of the SiC MOSFET. On the other hand, the expressions for the i_g current are:

$$i_{g,on} = \frac{V_{gg+} - V_{Miller}}{R_{g,on}}, \tag{2}$$

taking into account that $R_{g,on} = R_{on} + R_{g,ext} + R_{g,int}$ during the interval $t_2 - t_{1,1}$. Moreover, v_{ds} is:

$$dv_{ds}/dt = i_{g,on}/C_{gd}. \tag{3}$$

Regarding the equations (1)-(3), the current and voltage slopes can be controlled varying the values of $R_{g,on}$.

B. Operating at Turn-off Transition

As shown in Fig 3, when PWM input drops to zero in t_5, Q_2 and S_2 are turned on and V_{gs} starts to fall until it reaches the Miller Plateau voltage in t_6. The voltage V_{gs} is approximately constant in t_6 and in this time, v_{ds} starts to rise, $V_{2,high}$ is reached, and S_2 is turned off, after that the delay $t_{d,2}$ is over. Therefore, only R_{off} is carrying current and I_g magnitude decreases with $R_{g,off} = R_{on} + R_{g,ext} + R_{g,int}$. After in t_7 the v_{ds} voltage matches the V_{dc}-bus but an overshoot is created due to the parasitic inductance L_{loop}. At that time, also i_d starts to fall. When $V_{2,low}$ is reached in t_8, S_2 is turned on and it is carrying current until turn-off transition is completed. After t_8, the SiC is in blocking mode. In addition, slope for v_{ds} during turn-on transition is approximated from the following equation:

$$dv_{ds}/dt = i_{g,off}/C_{gd}. \tag{4}$$

On the other hand, the expressions for the i_g current are:

$$i_{g,off} = \frac{-V_{gg-} - V_{Miller}}{R_{g,off}}, \tag{5}$$

taking into account that $R_{g,off} = R_{off} + R_{g,ext} + R_{g,int}$ in the interval $t_7 - t_8$. In addition, v_{ds} slope approximation is:

$$\frac{di_d}{dt} = g_{fs} \cdot \frac{-V_{gg-} - V_{gs(th)} - \frac{I_d}{2 \cdot g_{fs}}}{C_{iss} \cdot R_{g,off}}. \tag{6}$$

Regarding the equations (4)-(6), the current and voltage slopes can be controlled by varying the values of $R_{g,off}$.

IV. AGD Design and Experimental Validation

To evaluate the proposed AGD concept an experimental study has been carried out by using the standard clamped-inductive circuit depicted in Fig. 4. The circuit consists of an inductive load, clamped diode with its parasitic capacitance (C_{D1}), and the SiC power MOSFET with parasitic elements. The L_{loop} represents the parasitic inductance which is created in the loop of the PCB and power devices. Besides, the gate driver circuit was designed and implemented and is shown in Fig. 5. The main experimental tests have been realized by using the N-channel SiC MOSFET SCT2080KE by Rohm Semiconductor and the SiC Schottky diode C3D25170H in hard switching conditions. The load current was 6 A, and the value of L was 87.7 μH. A square signal with 50% of duty cycle and frequency at 100 kHz was applied in the input. The Voltage dc-bus was 400 V and the V_{gg} supply was -5/20 V. The parasitic capacitances were taken from the datasheet and parasitic inductances were measured by considering previous methodologies [15]. The final values for parasitic elements are listed in Table I.

An inductance L_{loop} was connected on the circuit to emulate the oscillations and overshoots. In addition, the maximum values of R_{on} and R_{off} were calculated and the selection of the voltage references were realized.

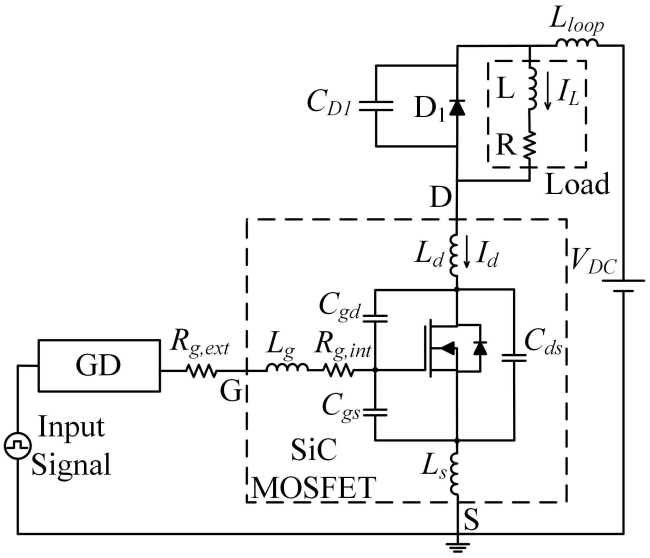

Fig. 4. Parasitic elements representation of the SiC MOSFET, and tests circuit for AGD validation.

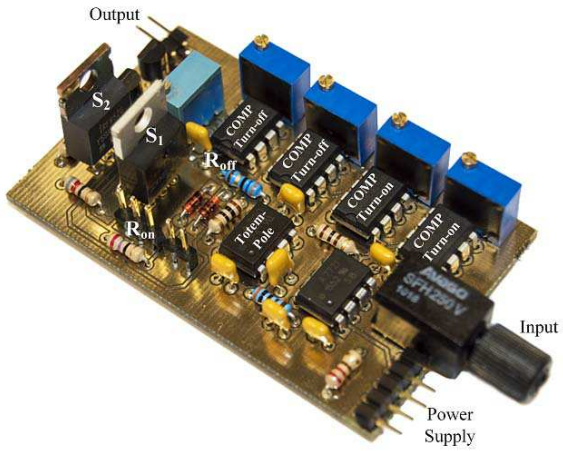

Fig. 5. AGD prototype manufactured.

TABLE I
Parameters for AGD Validation

Parameters	Value
C_{D1}	187.5 pF
C_{gd}	16 pF
C_{gs}	2064 pF
C_{ds}	61 pF
L_d	6 nH
L_g	7 nH
L_s	9 nH
L_{loop}	190.5 nH

A. Calculation of R_{on} and R_{off}

As noted above, the R_g performs an important role in the switching behaviour of the SiC MOSFET. Generally, the resistance R_g can be determined through an analysis in the gate driver path and its respective parasitic elements. Also, based on the presented and validated methods in [9] and [29],

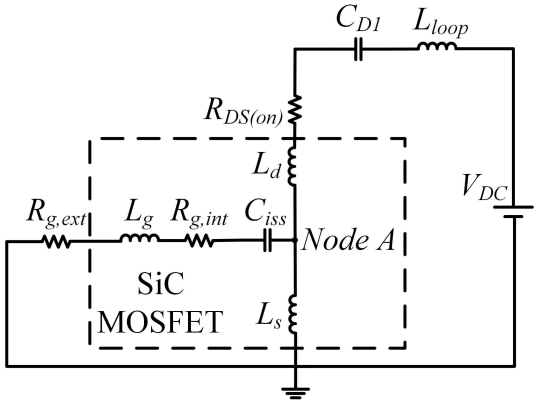

Fig. 6. Parasitic elements representation of the SiC MOSFET in turn-on conditions.

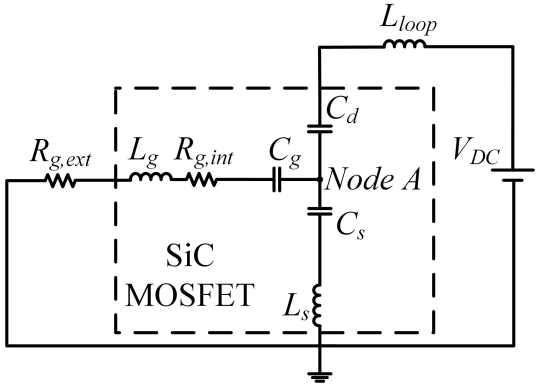

Fig. 7. Parasitic elements representation of the SiC MOSFET in turn-off conditions.

the resistance can be calculated through equivalent circuits of the total parasitic elements. The circuit depicted in Fig. 6 is commonly used to analyse the behaviour of the MOSFET parasitic elements together with the freewheeling diode and its parasitic capacitance C_{D1} for turn-on transition, when the power device is in conduction mode. Whereas, Fig. 7 depicts the equivalent circuit for turn-off conditions when the device is in blocking mode. It is important to mention that the load inductance L is considered as a constant current source due to does not change during switching transients. On the other hand, the parasitic capacitance associated with L is neglected in the models because is commonly lower than the output capacitance and it does not intervene in the resonant effect [30].

Equivalent elements are defined as: $L_{eq} = L_{loop} + L_d$, $R_{g,on} = R_{on}+R_{ext}+R_{int}$, and $R_{g,off} = R_{off}+R_{ext}+R_{int}$. An impedance analysis is developed in the node *A* in both circuit and the final equivalent circuits are represented in Fig. 8.

Regarding Fig. 8, the equivalent resistances $R_{eq,on}$ and $R_{eq,off}$ are obtained as [9]:

$$R_{eq,on} = \frac{(\omega_1 \cdot L_d)^2}{\frac{R_{g,on}+\left(\omega_1 \cdot L_g+\omega_1 \cdot Ls-\frac{1}{\omega_1 \cdot C_{iss}}\right)}{R_{g,on}}}, \tag{7}$$

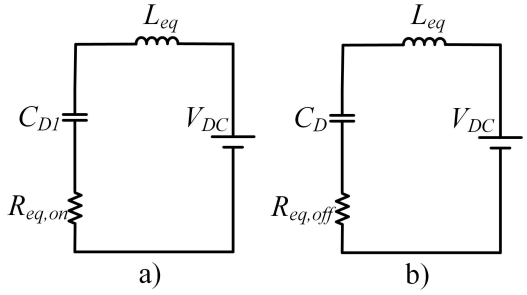

Fig. 8. Final equivalent circuits of SiC MOSFET with parasitic elements. a) Turn-on equivalent circuit and, b) Turn-off equivalent circuit.

$$R_{eq,off} = \frac{(\omega_2 \cdot L_s - \frac{1}{\omega_2 \cdot C_s})^2}{\frac{R_{g,off}+\left(\omega_2 \cdot L_g+\omega_2 \cdot L_s-\frac{1}{\omega_2 \cdot C_g}-\frac{1}{\omega_2 \cdot C_s}\right)}{R_{g,off}}}, \tag{8}$$

where $\omega 1$ and $\omega 2$ are the resonant frequencies of the resulting RLC circuits and are defined by equation (9) and equation (10).

$$\omega_1 = \frac{1}{\sqrt{(L_{eq} + L_s) \cdot C_{D1}}}, \tag{9}$$

$$\omega_2 = \frac{1}{\sqrt{(L_{eq} + L_s) \cdot (C_{gd} + C_{ds}}}. \tag{10}$$

The final circuits, as shown in Fig. 8, are second order systems and can be solved using Laplace domain to obtain the value of $R_{g,on}$ and $R_{g,off}$. However, according to studies in [29], equivalent resistances reach the maximum value when the equations (11) and (12) are fulfilled.

$$R_{g,on} = \left|\omega_1 \cdot L_g + \omega_1 \cdot L_s - \frac{1}{\omega_1 \cdot C_{iss}}\right|, \tag{11}$$

$$R_{g,off} = \left|\omega_2 \cdot L_g + \omega_2 \cdot L_s - \frac{1}{\omega_2 C_g} - \frac{1}{\omega_2 \cdot C_s}\right|. \tag{12}$$

After performing the calculation and replacing the values in each equation, R_{on} and R_{off} were obtained. The final value of R_{on} and R_{off} are 28.3 Ω and 32.1 Ω respectively.

B. Time Interval Calculation

If conventional gate driver (CGD) with fixed resistance is used, the time intervals to define the behaviour of the AGD can be calculated. Regarding the Fig. 2, the time $t_{1,1}$ is calculated as $t_2 - t_{df,1}$ and t_2 is expressed in equation (13), where $t_{df,1}$ is considered constant.

$$t_2 \cong R_{g,on} \cdot C_{iss} \cdot ln\left(\frac{V_{gg} - v_{gs(th)}}{V_{gg} - (\frac{2 \cdot I_d}{g_{fs}}) + v_{gs(th)}}\right). \tag{13}$$

On the other hand, the delay t_{d1} is the interval $t_3 - t_2$ and the time t_3 is expressed as:

$$t_3 \cong Q_{gd} \cdot R_{g,on} / \left(V_{gg} - \left(\frac{2 \cdot I_d}{g_{fs}} + v_{gs(th)}\right)\right), \tag{14}$$

where the Q_{gd} is gain-drain charge. For turn-on transition, the delay $t_{d,2}$ is the interval $t_7 - t_6$ where t_6 and t_7 are determined as:

$$t_6 \cong R_{g,off} \cdot C_{iss} \cdot ln\left(\frac{V_{gg}}{(\frac{2 \cdot I_d}{g_{fs}}) + v_{gs(th)}}\right), \quad (15)$$

$$t_7 \cong Q_{gd} \cdot R_{g,off} / \left(V_{gg} - \left(\frac{2 \cdot I_d}{g_{fs}} + v_{gs(th)}\right)\right). \quad (16)$$

C. Optimal Values for Reference Voltage $V_{1,low}$ and Optimal Delay $t_{d,2}$

As previously mentioned, $V_{1,low}$ and $t_{d,2}$ are the parameters that influence the optimal behaviour of the current i_d and voltage v_{ds}. Accordingly, to reach a better design, $V_{1,low}$ and $t_{d,2}$ are calculated realizing the optimization between losses and switching times. On the one hand, usually the switching losses in both turn-on and turn-off are expressed as:

$$E_{on} = 0.5 \cdot (V_{ds} \cdot I_d \cdot t_{on}) = E_{ri} + E_{fv}, \quad (17)$$

$$E_{off} = 0.5 \cdot (V_{ds} \cdot I_d \cdot t_{off}) = E_{rv} + E_{fi}. \quad (18)$$

On the other hand, a method to characterize the power losses in relation to the rise time and fall time of the current i_d was presented in [31]. This method is used for getting the optimal times for the points $V_{1,low}$ and $t_{d,2}$, when a relation between minimal losses E_{min} expressed in (19), and the energy losses E_{ri} and E_{fi}, is found. In addition, taking into account the overshoots and turn on and turn off delay times.

$$E_{min} = 0.5 \cdot (I_d)^2 \cdot L_{loop}. \quad (19)$$

The rise time losses of the current are calculated by using the expression:

$$E_{ri} = 0.5 \cdot (I_d)^2 \cdot L_{loop} \cdot \left(\frac{1}{\alpha} - 1\right) \cdot (1 + \sigma_1)^3, \quad (20)$$

where α is the relation between di/dt and $[di/dt]_{max}$ according to (21).

$$\alpha = \frac{di_d/dt}{(di_d/dt)_{max}}. \quad (21)$$

The maximum di/dt is defined by equation (22). In general, the maximum di/dt slope is infinite, for this reason in this analysis the maximum value of di_d/dt is considered with the minimum value result calculation of R_g which is 6.3 Ω.

$$(d_{id}/dt)_{max} = V_{dc}/L_{loop}. \quad (22)$$

In addition, σ_1 is the relation between diode reverse recovery current and i_d as shown in equation (23).

$$\sigma_1 = I_{rr}/I_d. \quad (23)$$

The ratio between the losses in t_{rise} and minimal losses is represented by (24).

$$\frac{E_{ri}}{E_{min}} = \left(\frac{1}{\alpha} - 1\right) \cdot (1 + \sigma_1)^3 \quad (24)$$

TABLE II
TURN-ON ENERGY LOSSES AND CURRENT PEAKS

$V_{1,low}$ (V)	di/dt $(A/\mu s)$	α	I_{rr} (A)	σ_1	E_{on} (μJ)	E_{on}/E_{min}
5	14.5	0.47	1.8	0.63	195	2.43
6	15.4	0.50	2.3	0.74	182.3	2.27
7	16.8	0.58	2.7	0.88	163.6	2.03
8	22.4	0.59	3.2	1.05	134.3	1.67
9	27.1	0.63	3.8	1.16	128.2	1.59
10	37.3	0.11	4.2	1.29	115.3	1.43
11	36.8	0.81	4.7	140	95.6	1.19
12	47.2	0.92	5.1	146	88.2	1.1

TABLE III
TURN-OFF ENERGY LOSS AND VOLTAGE OVERSHOOTS

$t_d(ns)$	V_{os}	σ_2	$E_{off}(\mu J)$	E_{off}/E_{min}
200	2	1.00	389.1	1.44
197	15	1.04	345	1.28
156	79	1.19	325.3	1.25
130	88	1.22	292.2	1.2
114	135	1.33	290.6	1.08
96	162	1.145	286.1	1.06
92	189	1.47	283.8	1.05
88	198	1.49	279.5	1.04
81	224	1.56	274.3	1.02

For the case of the losses for fall time of the current, the equation (25) is used.

$$E_{fi} = 0.5 \cdot (I_d)^2 \cdot L_{loop} + 0.5 \cdot (I_d)^2 \cdot L_{loop} \cdot \frac{1}{\sigma_2}, \quad (25)$$

where

$$\sigma_2 = \frac{V_{os}}{V_{ds}} = \frac{L_{loop} \cdot di_d/dt}{V_{dc}}, \quad (26)$$

If the minimal losses are defined by (19), the ratio between t_{fall} losses and minimal losses can be represented by (27).

$$\frac{E_{fi}}{E_{min}} = (1 + \sigma_1). \quad (27)$$

Taking into account the equations (24) and (27), the E_{on} and E_{off} losses were calculated and the optimal t_{rise} and t_{fall} were obtained. Then, times obtained by the equations (13)-(15) were used to calculated $V_{1,low}$ and $t_{d,2}$. The Tables II and III show the variation values when the $V_{1,low}$ and $t_{d,2}$ were finally calculated. In addition, the delay $t_{df,1}$ of 28 ns and minimal losses $E_{min} = 350.4$ μJ (for $R_g = 6$ Ω) were considered.

D. Experimental Validation Analysis of the AGD

With the calculated values in the previous subsection, experimental setup of the AGD for both turn-on and turn-off transitions were developed. Firstly, an evaluation test between AGD and CGD with the minimum fixed $R_{g,ext}$ of 6.3 Ω was carried out. The purpose of this comparison was to analyse the overshoots and oscillations behaviour of the AGD and the

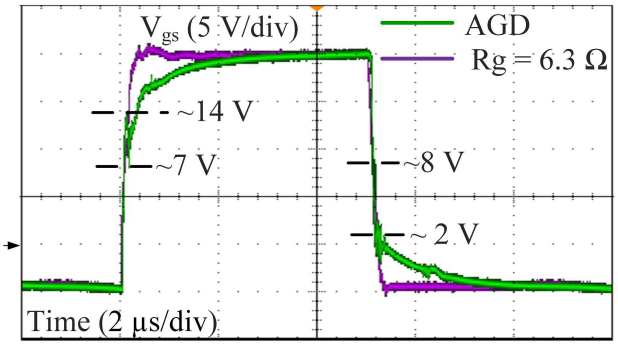

Fig. 9. Experimental results for voltage V_{gs} transitions. $R_g = 6.3\ \Omega$ and AGD with $V_{1,high} = 14$ V and $V_{1,low} = 7$ V and $V_{2,high} = 8$ V and $V_{2,low} = 2$ V.

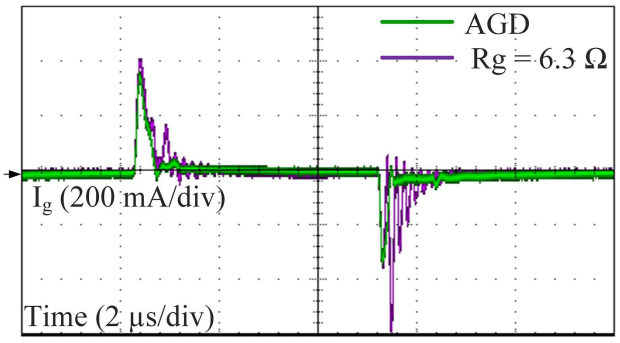

Fig. 10. Experimental results for current I_g transitions. $R_g = 6.3\ \Omega$ and AGD with $V_{1,high} = 14$ V and $V_{1,low} = 7$ V and $V_{2,high} = 8$ V and $V_{2,low} = 2$ V.

CGD with minimal resistance. In addition, for the AGD the initial values of R_g and reference voltages were used according to the values calculated previously. The commercial values $R_{on} = 27\ \Omega$ and $R_{off} = 33\ \Omega$ were used finally.

The value references considered for the study taking into account the results listed in Tables II-III, were $V_{1,hihg} = 14$ V and $V_{1,low} = 7$ V for turn-on transition and $V_{2,hihg} = 8$ V and $V_{2,low} = 2$ V for turn-off transition. On the one hand, Fig. 9 and Fig. 10 show the experimental results of V_{gs} and the I_g respectively. On the other hand, the V_{ds} and I_d impact when the driver is applied are shown in Fig. 11 and Fig. 12 for turn-on and turn-off transition.

According to results, by using the CGD with Rg fixed and minimum value the current oscillations are remarkable with resonant frequency at 5.4 MHz, maximum amplitude 5.8 A and switching speed *di/dt* of 53.2 A/μs. Accordingly, the AGD reduces the current oscillation 31.6% of the maximum amplitude leading a di/dt of 12.3 A/μs. For turn-off transition, voltage oscillations with 5.4 MHz of resonant frequency, an overshoot of 648 V and *dv/dt* of 4.8 k V/μs is presented by using the CGD with fixed resistance of 6.3 Ω. However, the AGD damps the total oscillation and reduces 28.2% of the voltage overshoot with dv/dt of 3.2 kV/μs.

To strengthen the experimental validation of the proposed AGD, an analysis with another SiC MOSFET was performed. Accordingly, the SiC MOSFET C2M0080120D by Cree was evaluated by using the AGD and CGD with the

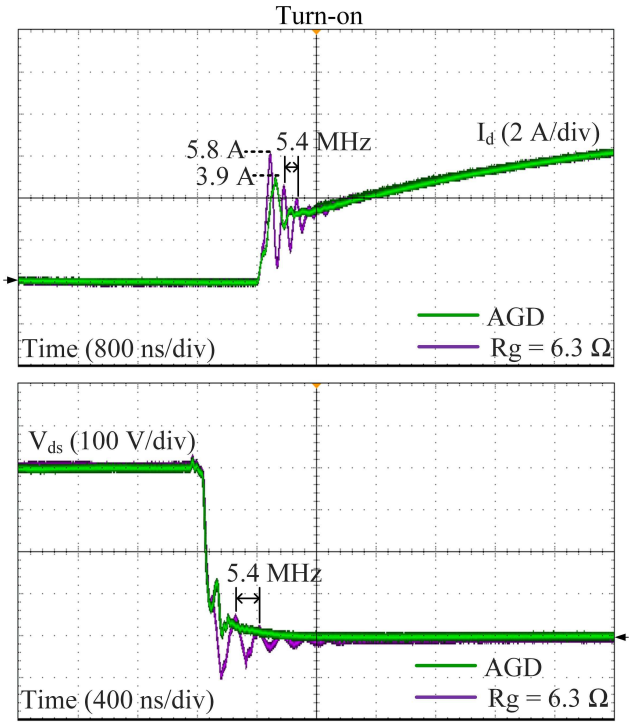

Fig. 11. Experimental results of I_d and V_{ds} for turn-on transition. $R_g = 6.3\ \Omega$ and AGD with $V_{1,high} = 14$ V and $V_{1,low} = 7$ V and $V_{2,high} = 8$ V and $V_{2,low} = 2$ V.

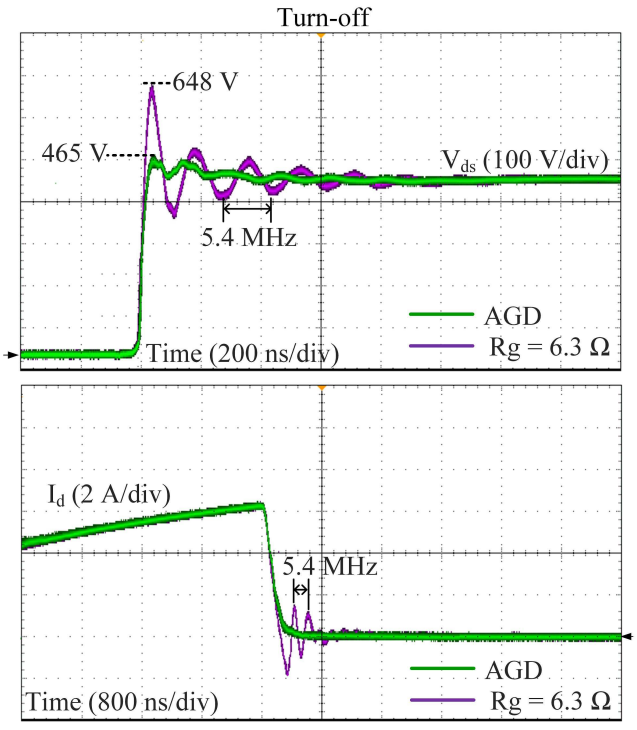

Fig. 12. Experimental results of I_d and V_{ds} for turn-off transition. $R_g = 6.3\ \Omega$ and AGD with $V_{1,high} = 14$ V and $V_{1,low} = 7$ V and $V_{2,high} = 8$ V and $V_{2,low} = 2$ V.

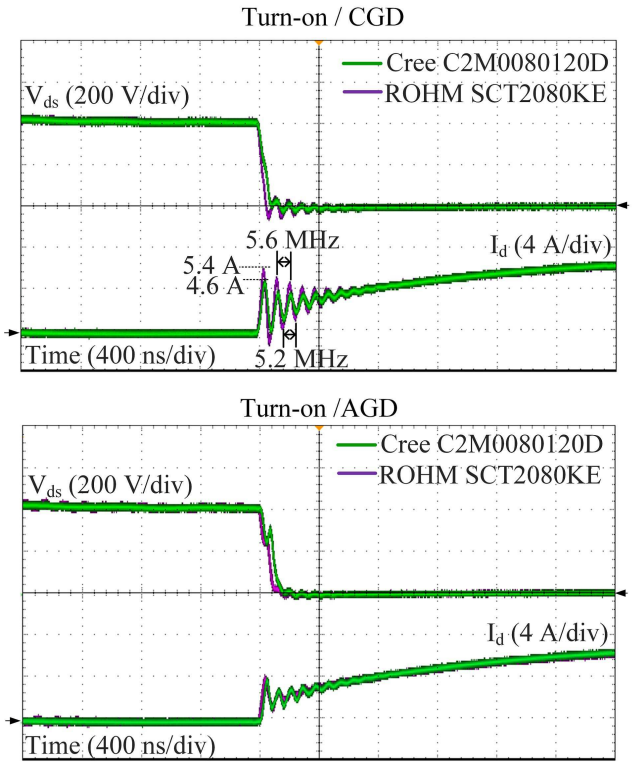

Fig. 13. Experimental results of I_d and V_{ds} for turn-on transition between two SiC MOSFETs.

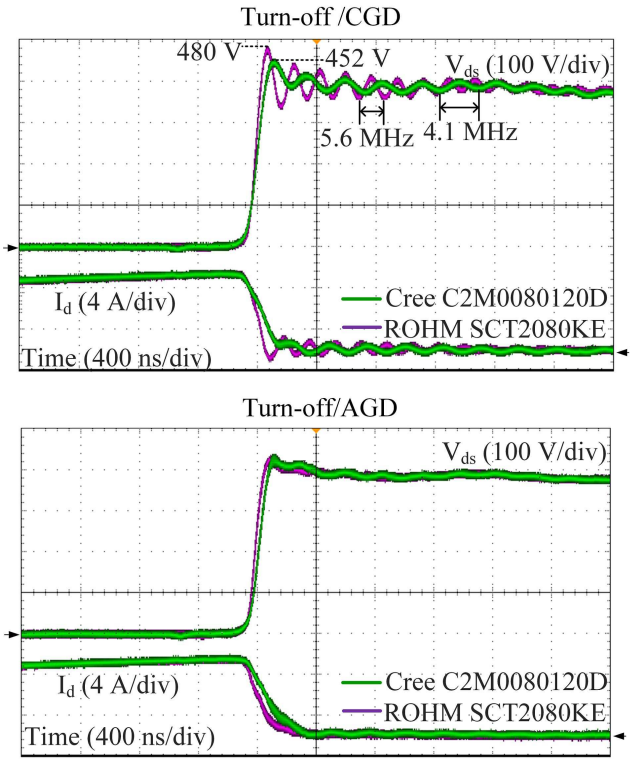

Fig. 14. Experimental results of I_d and V_{ds} for turn-off transition between two SiC MOSFETs.

minimum fixed $R_{g,ext}$ of 2.5 Ω. For realising the analysis with the AGD, the presented method to determinate the gate resistances and reference voltages was used. Regarding the calculation obtained, the gate resistance values for this SiC MOSFET were R_{on} = 33 Ω and R_{off} = 39 Ω. In addition, the voltage references were $V_{1,hihg}$ = 16 V and $V_{1,low}$ = 9 V for turn-on transition and $V_{2,hihg}$ = 10 V and $V_{2,low}$ = 3 V for turn-off transition. The test setup parameters were DC-bus = 400 V, switching frequency at 100 kHz, a load of 6 A and L = 120 μH. Whereas the parasitic elements were considered from the datasheet and previous experiments. The obtained data were compared with the results of a developed study with the SiC MOSFET SCT2080KE under the same operation conditions and AGD parameters used previously for this device. The voltage and current waveforms comparison is shown in Fig. 13 and Fig. 14.

In the figures can be seen that the behavior in both power devices is similar with CGD. Whereas the overshoots in Cree MOSFET are low, the switching delay times are better in Rhom MOSFET. In addition, the frequency oscillations are bigger in the latter. Furthermore, with AGD the oscillations and overshoots are reduced in both devices, despite of the switching time in SiC MOSFET C2M0080120D is longer. Therefore, it can be concluded that the AGD is valid for different MOSFETs and its performance depend on the characteristics of each device and the proper parameters calculation.

TABLE IV
NUMERICAL COMPARISON OF POWER LOSSES

	P_{gate} (W)	P_{cond} (W)	P_{sw} (W)	Total Losses (W)
CGD with minimum R_g	0.233	1.25	35.04	36.5
CGD with large R_g	0.254	2.03	85.4	87.6
Proposed AGD	0.232	1.66	39.1	40.9

V. AGD VIABILITY STUDY

A. SiC MOSFET Performance Analysis with AGD

The aim of the proposed AGD is to reduce the oscillations in both current and voltage but also to reduce total losses. Accordingly, the performance of the AGD was analysed for the SiC MOSFET SCT2080KE, realising a comparison between losses with the AGD and losses with the CGD. The total losses were calculated as:

$$P_{total} = P_{conduction} + P_{switching} + P_{gate}, \tag{28}$$

where

$$P_{conduction} = R_{ds(on)} \cdot (i_{d,rms})^2, \tag{29}$$

and

$$P_{gate} = (V_{gg,on} + |V_{gg,off}|) \cdot Q_{gate}.f_{sw}. \tag{30}$$

Table IV shows the experimental results of switching losses by cycle, with operation conditions of 400 V dc-bus, 6 A on the load, f_{sw}=100 kHz, Q_g =106 nC and $R_{ds(on)}$=125 mΩ (Tj=125°C).

On the one hand, the performance of proposed AGD has been compared with CGD and fixed resistance of 6.3 Ω justified previously. The complete analysis has been realized with the purpose of obtaining the approximation of minimal losses with the minimal considered resistance. On the other hand, an analysis of CGD with large fixed resistance and different values for turn-on and turn-off path has been performed. The considered resistances for this evaluation have been the maximum values calculated and selected previously, which were 27 Ω for turn-on and 33 Ω for turn-off paths.

According to results, the conduction losses are low due to them being dependent on statics characteristics of the SiC MOSFET such as $R_{ds(on)}$ and blocking capabilities. Despite this, the conduction losses have an important variation between the AGD and the CGD with different resistance values. This variation is because of the $i_{d,rms}$ current changes with respect to the maximum and minimum drain current that can have significant differences for each driver.

Besides, in Table IV it can be seen that the conduction losses and losses in the gate are less than the switching losses. Therefore, only the switching losses play an important role. With AGD the switching losses are 4.4 W more than CGD with minimum fixed resistance. However, the switching losses are 40.9 W and are less than CGD with fixed large resistance.

B. Electromagnetic Interference Analysis

The proposed AGD has the capability of reducing the ringing and oscillations in both drain current and drain-source voltage, as shown in Fig. 11 and Fig. 12. In general, the high *dv/dt* is the main parameter of conduced EMI production in power converters. Therefore, although the proposed AGD only reduces the overshoot voltage in 28.2%, the oscillation are eliminated.

The purpose of this EMI study is to have an understanding of the noise provoked mainly by high *di/dt* and *dv/dt*. Therefore, this analysis does not include the total noise but also the main oscillation in the current and voltage waveforms. Accordingly, the effect of oscillations can be characterized considering the current or voltage source as a periodic trapezoidal pulse and FFT analysis. In addition, it is important to consider that the i_d and v_{ds} measures were in common mode (CM) conditions.

Fig. 15 shows an approximation of the spectrum for both v_{ds} voltage and i_d current. These results were obtained from experimental measurement by means of an oscilloscope Tektronix MDO3024 and the spectrum was obtained applying the FFT in MATLAB software after the data were processed. The results show that the AGD can eliminate the noise in v_{ds} voltage and reduce the noise in i_d current with a resonant frequency of 5.4 MHz.

C. AGD Cost Study

As noted above, the SiC MOSFET requires a driver to supply the device, achieve better performance, reliability and even reduce EMI problems. In power converters with a simple gate driver, the snubber circuits are necessary to reduce the

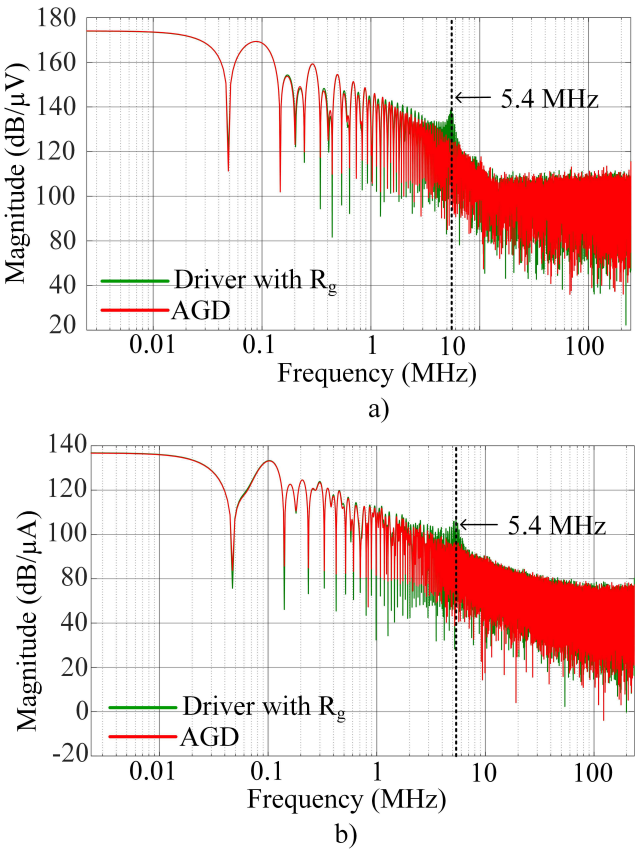

Fig. 15. Spectrum comparison between CGD with Rg=6.3 Ω and AGD for I_d and V_{ds} experimental results. a) Spectrum approximation of V_{ds} and, b) Spectrum approximation of I_d.

EMI problems and overshoots. However, the snubber circuits could reduce the system efficiency.

As an example, the total cost of the driver plus snubber circuit can be considered 100 % and it is obtained regarding the driver components cost. One optocoupler driver HCPL-3120 with 10 % price, one isolated power supply with 54 % of the cost and a snubber network with of 36 % of total cost.

The cost of the proposed gate driver is increased mainly by the high-speed comparators and MOSFETs. Regarding Fig. 1 four high-speed comparators and four MOSFETS are required. For the implementation of the proposed AGD, four ANALOG DEVICES AD8561ANZ comparators were used with a 16 % price per unit. In addition, two N-channel MOSFETS IRF520NPBF and two P-channel MOSFETs IRF9520PBF were used with a price of 3 % per unit. Assuming, that the rest of components have an approximately cost of 36 %, and one isolated power supply of 54 % value; the AGD approximated total cost is 166 %. It is also important to mention that the components cost of this study was consulted for a few components, not for large series. Also, this type of solutions could be integrated into specific gate drivers, reducing, even more, the final cost compared to bulky snubbers.

In Table V a comparison of approximated costs and main characteristics between CGD plus snubber network and proposed gate driver is developed. The comparison shows that

TABLE V
COST AND CHARACTERISTICS COMPARISON OF THE GATE DRIVERS

Drivers	Cost (%)	Efficiency	EMI Reduction	Overshoots Reduction
GD+Snubber	100	Medium	High	High
Proposed AGD	166	High	High	High

the AGD is a good solution and in spite of its cost it has advantages in terms of efficiency, EMI and overshoots reduction.

D. General considerations for the AGD Design

So far, the AGD was designed and validated for a particular case. However, the AGD should be able to work in different load current and tolerate the parameter variations such as the parasitic elements, voltage threshold, and Miller Plateau voltage. Accordingly, for better performance of the AGD in different work conditions, the following assumptions can be established:

- The AGD should be designed for a known application. Therefore, its plant is also known and the expected variations of the system are known.
- The parasitic elements behaviour can be determined through the characterization of the defined system, of studies such as [15], [30], [32] and datasheets specifications.
- The tolerance band for voltage threshold and voltage plateau should be adjusted to guarantee the AGD operation on the variations caused by the temperature and high load currents [32].
- The AGD should be designed for the maximum load current level with the purpose of working in different current loads variations.

Taking into account these considerations, the AGD can offer an extensive operation range of load currents and be insensitive to parasitic elements variations.

VI. CONCLUSIONS

A new AGD has been presented and characterized under hard-switching conditions. The concept of the controller was defined and the main parameters were calculated and optimized. The new gate driver can control the di/dt turn-on and the dv/dt turn- off individually with low switching losses. The proposed AGD has been validated with experimental tests at 100 kHz of switching frequency and 400 V of dc-bus. The results showed that the AGD can reduce the overshoot voltages until 28.2% and until 31.6% of the current peak. The reduction of the overshoots leads total switching losses until about 53.3% less than conventional gate driver with high gate resistance fixed. On the other hand, the AGD cannot only attenuate the current oscillations but also eliminated the voltage oscillations caused by parasitic elements in 5.4 MHz for conditions of this study. In addition, an experimental validation for two different SiC MOSFET has been developed. The two devices evaluation show that the active gate driver can work for any SiC MOSFET. Taking into account all of the above, it has been demonstrated that if the energy on gate-voltage trajectory of the SiC MOSFET is reduced, varying the R_g on a specific interval of v_{gs} around the Miller Plateau zone, the overshoots problems are reduced without compromising performance. Although this driver needs two switching devices and high-speed comparators, it is a good solution due to its control simplicity. In addition, the AGD can be implemented as a closed-loop control with the output signals, just by adding simple analog circuits connected to the load. Therefore, this AGD is a good alternative to snubber circuits and even complex gate circuits presented so far.

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