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Loss Analysis of GaN Based Partial Parallel Isolated Bidirectional Full Bridge Boost Converter

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Abstract—**A theoretical loss analysis is presented for GaN switches, for which conduction and switching losses are considered, and for planar transformers, where winding and core losses are considered. The analysis is then used to make a comparison of the losses in the partial parallel isolated full bridge boost converter and the isolated full bridge boost converter.**

Index Terms—**dc-dc converter, bidirectional, full bridge boost, partial parallel.**

I. Introduction

Renewable energy systems, electrical vehicles and dc microgrids all require flexible and effective reversible dc power flows, making bidirectional dc-dc converters essential [1]–[3]. Often galvanic isolation is a requirement in order to avoid failures propagating through the system, which narrows the plethora of bidirectional dc-dc topologies, and their derivations, down to two common ones; the dual active bridge (DAB) and the isolated full bridge boost/buck (IFBB) [4], [5]. The IFBB is the focus of this paper due to simpler control and ease of calculations than the DAB. The IFBB is a hard switching topology, which leads to relatively high switching losses.

High gain is the hallmark of the isolated topologies [6], and leads to a converter with a high current side, and a high voltage side. Various techniques have been employed to handle the high current, for example the method of directly paralleling semiconductor devices [7]. Paralleling switches complicates circuit layout, and increases parasitic inductance around the switches.

In this paper the high current side of the IFBB will be paralleled, while the high voltage will be connected in series, leading to the partial parallel (PP) IFBB. The losses in the GaN switches and the transformers are then compared.

II. Loss calculation

A. Operation principle

The IFBB converter is shown in Fig. 1, and the PP IFBB is shown in Fig. 2. The two topologies have in common the inductor on the low voltage side and the switches on the high voltage side. Since these are common for the two topologies, their losses will be neglected in this analysis. The switches in the red box of Fig. 2 carry half the current

than those in Fig. 1, but due to a difference in turns ratio between the transformers the same voltage will be seen across the switches on the low voltage side. For the transformers in the blue box of Fig. 2, the current is half of that of Fig. 1, while the voltage on the high voltage side is half for one of the transformers in Fig. 2, giving the same total voltage across both of them as that of the transformer in Fig. 1.

B. Losses in the switches

The losses in the switches can be divided into two categories: switching and conduction losses. The switching
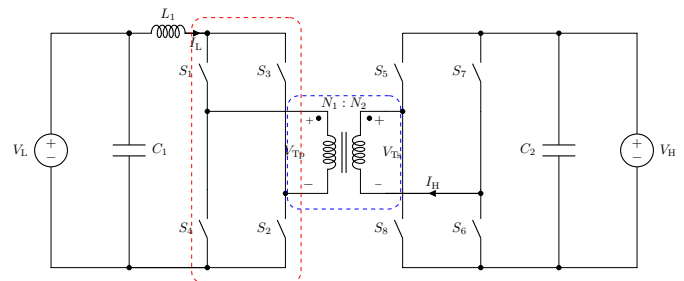

Fig. 1: The isolated full bridge boost converter. The boxes indicates components that are compared.
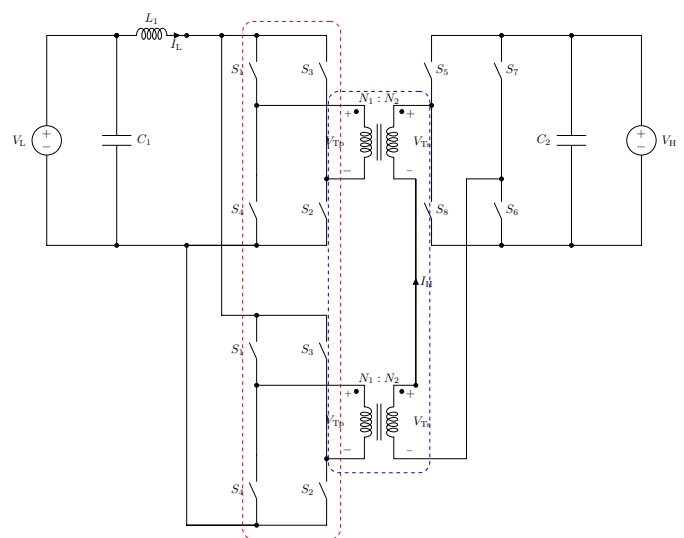

Fig. 2: The parallel in, series out isolated full bridge boost converter. The boxes indicates components that are compared.

losses can be split up into turn-on (P_{ton}) and turn-off (P_{toff}) losses, output capacitance loss (P_{oss}), gate charge loss (P_{G}), reverse conduction loss (P_{SD}), and reverse recovery loss (P_{RR}). Reference [8] has a derivation of the losses, which is only summarized here. The total switching losses thus becomes

$$P_{\text{sw}} = P_{\text{ton}} + P_{\text{toff}} + P_{\text{oss}} + P_{\text{G}} + P_{\text{SD}} + P_{\text{RR}}. \quad (1)$$

The turn-on losses are calculated as

$$P_{\text{ton}} = \frac{V_{\text{BUS}} I_{\text{DS}} f_{\text{sw}}}{2} \left[\frac{Q_{\text{GD}} R_{\text{Gon}}}{V_{\text{DR}} - V_{\text{pl}}} + \frac{Q_{\text{GS2}} \left(R_{\text{Gon}} + R_{\text{CSI}} \right)}{V_{\text{DR}} - \left(\frac{V_{\text{pl}} + V_{\text{th}}}{2} \right)} \right], \quad (2)$$

where

   V_{BUS}: Voltage across the device when the device is off.
   I_{DS}: Current through the device when the device is on.
   f_{sw}: Switching frequency.
   R_{Gon}: Gate on resistance (small internal resistance plus any externally placed resistor).
   Q_{GD}: Charge required to into the gate to change the drain voltage down from blocking state to near zero.
   V_{DR}: Gate drive voltage.
   V_{pl}: Gate plateau voltage at Q_{GD}.
   Q_{GS2}: Charge required to increase gate voltage from the stated threshold voltage of the device to the plateau voltage.
   V_{th}: Gate threshold voltage.
   R_{CSI}: Equivalent impedance of the common source inductance. Since this is layout dependent it will be set to zero for the comparison, but it should be noted it has a significant contribution to the switching losses.

The values corresponding to the system parameters can be found in Table I, while the parameters that are device specific can be found in the corresponding datasheet (the typical value has been used).

Next the turn-off losses are calculated as

$$P_{\text{toff}} = \frac{V_{\text{BUS}} I_{\text{DS}} f_{\text{sw}}}{2} \left[\frac{Q_{\text{GD}} R_{\text{Goff}}}{V_{\text{pl}}} + \frac{Q_{\text{GS2}} \left(R_{\text{Goff}} + R_{\text{CSI}} \right)}{\left(\frac{V_{\text{pl}} + V_{\text{th}}}{2} \right)} \right], \quad (3)$$

where R_{Goff} is the gate off resistance (small internal resistance plus any externally placed resistor).

The loss in the output capacitance can be calculated as

$$P_{\text{oss}} = f_{\text{sw}} E_{\text{oss}} = f_{\text{sw}} \int_0^{V_{\text{BUS}}} v_{\text{DS}} C_{\text{oss}} \left(v_{\text{DS}} \right) \mathrm{d} v_{\text{DS}}, \quad (4)$$

where v_{DS} is the drain source voltage and C_{oss} is the output capacitance at a given v_{DS}.

The gate charge loss is calculated next as

$$P_{\text{G}} = Q_{\text{G}} V_{\text{DR}} f_{\text{sw}}, \quad (5)$$

where Q_{G} is the gate charge.

P_{SD} is zero because of the topology, which has no periods of reverse conduction for the primary switches. P_{RR} is zero because GaN devices have no reverse recovery charge.

Next the conduction losses in the switches are calculated as

$$P_{\text{c}} = I_{\text{DS,rms}}^2 R_{\text{DS,ON}}, \quad (6)$$

where $R_{\text{DS,ON}}$ is the drain source on resistance and $I_{\text{DS,rms}}$ is the rms current through the device. For both the IFBB and the PP IFBB $I_{\text{DS,rms}}$ is given as

$$I_{\text{DS,rms}} = \sqrt{\left(\frac{I_{\text{L}}^2}{4} + \frac{\Delta I_{\text{L}}^2}{48} \right) (3 - 2D)}, \quad (7)$$

where I_{L} is the current through the inductor, ΔI is the ripple in I_{L} and D is the duty cycle of the switches. D is calculated as

$$D = 1 - \frac{V_{\text{L}} n}{2 V_{\text{H}}}, \quad (8)$$

where V_{L} is the low side voltage, V_{H} is the high side voltage and n is the turns ratio between the primary and secondary side of the transformer.

The losses in the IFBB can be expressed as $P_{\text{IFBB}} = 4 P_{\text{sw}} + 4 P_{\text{c}}$, and for the PP IFBB it can be expressed as $P_{\text{PPIFBB}} = 8 P_{\text{sw}} + 8 P_{\text{c}}$. Here it is important to remember that the current in each switch of the PP IFBB is half of that of the IFBB. The calculations of the losses have been done using GaN switches operating close to their maximum voltage and current ratings, i.e. different kind of switches have been used for the PP IFBB (EPC2035) and the IFBB (EPC2020).

The systems specifications can be seen in Table I, and the calculated losses are shown in Fig. 3. Fig. 3a shows that the switching losses for the PP IFBB is higher than for the IFBB, but they are negligible compared to the conduction losses. Fig. 3b shows that the conduction losses are much higher than the switching losses, and that the losses are double for the IFBB compared to the PP IFBB.

C. Losses in transformer

The transformer losses are split into two: core and winding losses. To calculate either of them the first step is to calculate how many turns the transformer should have. For both of the considered topologies the first calculation is to determine the worst case volt seconds (V_{s}) that the transformer will experience as

$$V_{\text{s}} = \frac{V_{\text{H}} \left(1 - D \right)}{f_{\text{sw}} n}, \quad (9)$$

TABLE I: System specification

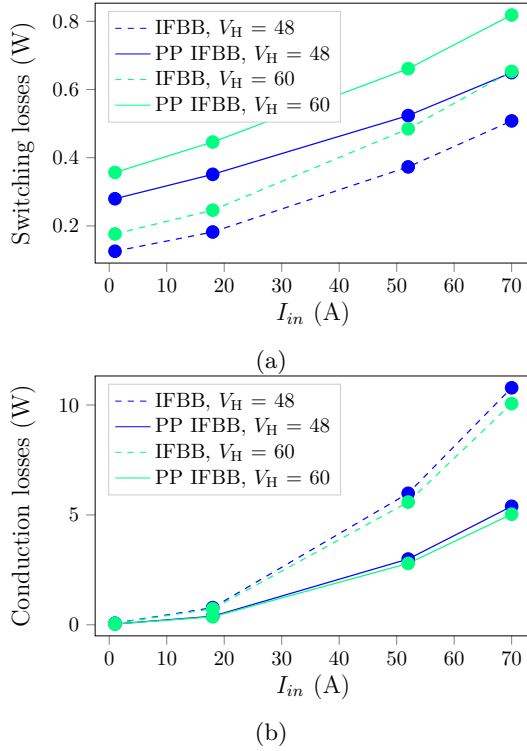| Parameter	Value	Parameter	Value
V_{L}	2 V to 22 V	$I_{\text{DS,IFBB}}$	1 A to 70 A
V_{H}	48 V to 60 V	$I_{\text{DS,PP IFBB}}$	0.5 A to 35 A
V_{BUS}	24 V to 30 V	$\Delta I_{\text{DS,IFBB}}$	20 A
D	0.5 to 1	$\Delta I_{\text{DS,PP IFBB}}$	10 A
f_{sw}	50 kHz	Device IFBB	EPC2020
n	2	Device PP IFBB	EPC2035

Fig. 3: Loss for the primary switches, with switching losses shown in (a) and conduction losses shown in (b).

where the worst case is experienced as the highest V_s. Next the number of primary turns (N_p) can be calculated as

$$N_p = \frac{V_s}{\Delta B A_e}, \tag{10}$$

where ΔB is double the peak flux (B_{pk}) that will stay below core saturation and A_e is the effective area of the core. In case a fractional number is calculated, it is rounded to the next integer in order to physically be able to built it. This rounding of the number of turns leads to a decrease in the flux, which is therefore recalculated with the chosen number of turns as

$$\Delta B_{actual} = \frac{V_s}{N_p A_e}. \tag{11}$$

The core losses per volume (P_v) can be calculated based on the Steinmetz [9] equation

$$P_v = K f_{sw}^\alpha B_{pk}^\beta, \tag{12}$$

where K, α and β are material constants found in the datasheet for the materials. The core losses for the chosen core shape and material can then be found as

$$P_{core} = P_v V_e, \tag{13}$$

where V_e is the effective volume of the core.

The windings are made with planar magnetics, where each turn is made with a layer taking up the full breadth of the core window. The dc resistance (R_{dc}) per layer/turn is thus calculated as

$$R_{dc} = \rho \frac{l}{A_c}, \tag{14}$$

where ρ is the resistivity of copper, l is the mean turn length of the turn and A_c is the area of the conductor. From this the ac resistance (R_{ac}) for planar magnetics, can be found through Dowell's equation [10]–[12], which is expressed as

$$F_r = \frac{R_{ac}}{R_{dc}} = \frac{\xi}{2} \left[\frac{\sinh \xi + \sin \xi}{\cosh \xi - \cos \xi} + (2m-1)^2 \frac{\sinh \xi - \sin \xi}{\cosh \xi + \cos \xi} \right], \tag{15}$$

where ξ is the ratio of the height of the copper (h) to the skin depth of the material (δ), and m is defined as the ratio in

$$m = \frac{F(h)}{F(h) - F(0)}, \tag{16}$$

where $F(h)$ and $F(0)$ are the magneto motive forces (MMFs) at the limits of a layer. With no interleaving of the primary and secondary layers m will get as high as the number of primary or secondary layers, while with full interleaving m is equal to 1, and with other interleaving techniques m can be lower [13]. In general R_{ac} can be calculated as

$$R_{ac} = \sum_{layers} F_{r,layer}(m) R_{dc,layer}, \tag{17}$$

which simplifies to

$$R_{ac} = N_p F_r R_{dc}, \tag{18}$$

if the layers has the same R_{dc} and F_r. The rms current through the transformer is

$$I_{Tp,rms} = \sqrt{\left(2I_L^2 + \frac{\Delta I_L^2}{6}\right)(1 - D)}. \tag{19}$$

Since no dc current is running in the transformer, the winding losses can be calculated as

$$P_{winding} = I_{Tp,rms}^2 R_{ac}. \tag{20}$$

For the comparison of transformers some additional assumptions beyond Table I has been used as follows

- The transformer is based on planar design with cores EELP and EILP 14 to 102.
- Core materials are N49, N87, N92 and N97.
- To have n equal to two for both topologies the PP IFBB has two transformers with $n = 1$ giving a total of $n = 2$.
- Full interleaving is done for the transformers ($m = 1$).
- Copper thickness of the layers is double in the IFBB compared to the PP IFBB, since it has to handle twice the current.
- ΔB is the same for the two transformers in the PP IFBB as in the IFBB.
- Only included cores, where the required number of turns has fitted in the core shape
- I_L is 70 A.

Fig. 4 and Fig. 5 show the core and winding losses, and the volume of the core and the total losses, respectively.

for small cores and bigger core losses for bigger cores.

III. Conclusion

With the choice of letting the GaN switches be driven close to their maximum current, the conduction losses in the switches of the PP IFBB turns out to be half that of the IFBB. Meanwhile switching losses is slightly higher for the PP IFBB, but the switching losses is ten times lower than the conduction losses. So when only considering the switches losses, the PP IFBB is an improvement over the IFBB.

Because of the choice that the copper is twice as thick in the IFBB compared to the PP IFBB, and that the same ΔB is used for both the transformers in the PP IFBB, the losses in the two topologies are almost the same. Therefore the PP IFBB is a good candidate to avoid handling the high currents that can be present in the IFBB.

References

[1] F. Blaabjerg, Z. Chen, and S. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *Ieee Transactions on Power Electronics*, vol. 19, no. 5, pp. 1184–1194, 2004.

[2] Z. Chen, J. M. Guerrero, and F. Blaabjerg, "A review of the state of the art of power electronics for wind turbines," 2016.

[3] Z. Zhang, R. Pittini, M. A. Andersen, and O. C. Thomsena, "A review and design of power electronics converters for fuel cell hybrid system applications," *Energy Procedia*, vol. 20, no. Supplement C, pp. 301 – 310, 2012, technoport 2012 - Sharing Possibilities and 2nd Renewable Energy Research Conference (RERC2012).

[4] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *Ieee Transactions on Industry Applications*, vol. 27, no. 1, pp. 63–73, 63–73, 1991.

[5] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *Ieee Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2745–2760, 2012.

[6] K. L. Jørgensen, M. d. C. Mira Albert, Z. Zhang, and M. A. E. Andersen, "Review of high efficiency bidirectional dc-dc topologies with high voltage gain," *Proceedings of the 52nd International Universities' Power Engineering Conference*, 2017.

[7] R. Ramachandran and M. Nymand, "Effectively paralleling gan fets to achieve ultra-high efficiency in an isolated dc-dc converter," *2016 Ieee International Conference on Renewable Energy Research and Applications, Icrera 2016*, pp. 7 884 476, 956–960, 2016.

[8] A. Lidow, J. Strydom, M. de Rooij, and D. Reusch, *GaN Transistors for Efficient Power Conversion: Second Edition.* Wiley Blackwell, 2014.

[9] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics.* Kluwer Academic Publishers„ 2001.

[10] P. DOWELL, "Effects of eddy currents in transformer windings," *Proceedings of the Institution of Electrical Engineers-london*, vol. 113, no. 8, pp. 1387–, 1966.

[11] J. FERREIRA, "Improved analytical modeling of conductive losses in magnetic components," *Ieee Transactions on Power Electronics*, vol. 9, no. 1, pp. 127–131, 1994.

[12] Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, "Optimal design and tradeoff analysis of planar transformer in high-power dc–dc converters," *I E E E Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2800–2810, 2012.

[13] R. Pittini, Z. Zhang, and M. A. E. Andersen, "High current planar transformer for very high efficiency isolated boost dc-dc converters," *Proceedings of the 2014 International Power Electronics Conference*, pp. 3905–3912, 2014.
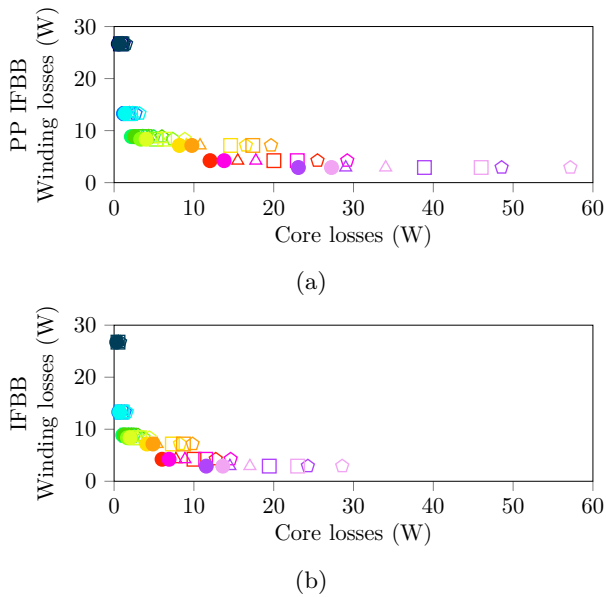
Fig. 4: Calculations on the losses of the transformers in the PP IFBB (a), and the transformer IFBB (b).
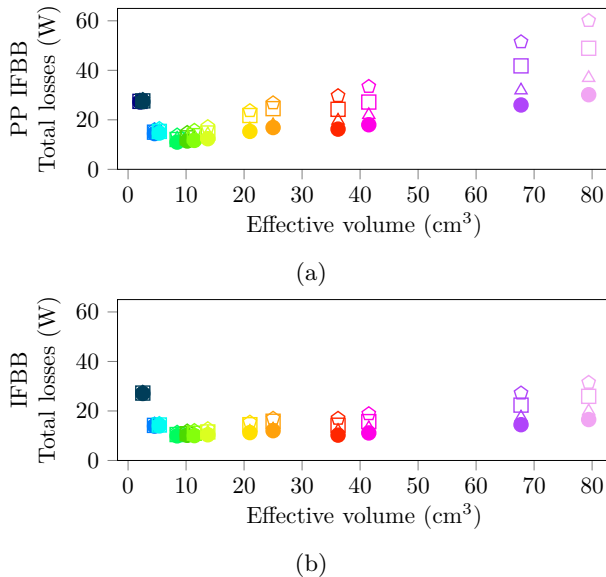

Fig. 5: Calculations on the losses versus volume of the transformers in the PP IFBB (a), and the transformer IFBB (b).

The color of each legend element in each plot is the same core type, while the shape of the legend element is a different core material. Fig. 4 shows that the core losses for the PP IFBB are twice that of the IFBB, which is due to the two topologies having the same ΔB in each core, but there being two of them in the PP IFBB. The winding losses seem to be almost the same for the two configurations, which is due to the double copper thickness of the IFBB, reducing the resistance that the double current runs through. The total losses for both topologies are comparable for small core sizes, while the total losses are much higher for the PP IFBB if larger cores are considered, which is due to the small core losses