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DTU

Integrated Off-Line Power Converter

Lin Fan
PhD thesis
January 2018

DTU Electrical Engineering
Department of Electrical Engineering

DTU

Integrated Off-Line Power Converter

Lin Fan

January 2018

Integrated Off-Line Power Converter

PhD thesis
2018

By
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Preface

This research project of integrated off-line power converter is conducted in the Electronics Group at the Department of Electrical Engineering in the Technical University of Denmark (DTU).

The duration of the research project is 3 years from February 2015 to January 2018. It includes approximately 30 ECTS (European Credit Transfer System) PhD courses study, equivalently 6 months compulsory workload and dissemination requirements such as teaching activities and students supervision, and vacation days with a total amount of officially 18 weeks in addition to public holidays. It also includes an external research stay with Prof. Fred C. Lee and Prof. Qiang Li at the CPES (Center for Power Electronics Systems) at the Virginia Tech (Virginia Polytechnic Institute and State University) in Blacksburg, Virginia, United States for about 3 months from July to September 2017.

The research project is the first project in the Electronics Group starting research on Power IC and/or PwrSoC (Power Supply on Chip). The research topics are multi-disciplinary, and mainly across the fields of integrated circuits, power electronics, and radio frequencies.

The supervisors are Prof. Ivan Harald Holger Jørgensen with a background of integrated circuits and Prof. Arnold Knott with a background of power electronics.

The research project is funded by a grant (No. 67-2014-1) for the TinyPower project from Innovationsfonden, Denmark.

The research project is performed with seven external partners: Niko-Servodan, Nordic Power Converters, Noliac, DTU Danchip, IPU, SimpLight, and Viso Systems.

The detailed acknowledgements are in the last section of this thesis.

Kgs. Lyngby, Denmark, January 2018

Lin Fan
PhD Student

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Abstract (English)

The miniaturization trend of industrial and consumer electronics continuously drives the demand of reductions in size, weight, and cost of power supplies. The examples of such applications considered in this research are light-emitting diode (LED) drivers for intelligent lighting systems and internet of things (IoT). These power supplies convert the mains power of 220-240 Vrms AC in Europe to low DC voltages around 13 V with an output power of 5-20 W. This research focuses on the DC-DC power conversion, with rectified AC mains as input. The size reduction is the direct requirement, and it can only be obtained by simultaneously improving efficiency to maintain thermal limits at maximum losses. However, fundamental trade-off relationships exist between the power density and the efficiency. To achieve both high efficiency and high power density, systematic development is imperative for components, topologies, and architectures.

The research started from integrating active components on a single chip, i.e. integrated high voltage (≥ 100 V) power MOSFETs in a Silicon-on-Insulator (SOI) process. The extreme performances (such as maximum switching speeds and minimum attainable on-resistances) of these devices are jointly determined by the device, layout, package, and PCB parasitic properties. The research highly contributes to the development towards Power Supply on Chip (PwrSoC) regardless of topologies and switching technologies. First, parasitic capacitances of power semiconductors are a part of the key design parameters of power supplies, for both hard-switched and soft-switched converters. A modelling method is proposed to systematically analyse the nonlinear parasitic capacitances of the power MOSFETs in different states, whereas datasheets typically specify capacitances only in transistor off-states. Second, the nonlinear figure-of-merits (FOMs), which might be used for device-to-device comparisons, are systematically analysed and optimized up to 18.3 times for a given device with quasi-zero voltage switching conditions. Third, four layout structures are proposed and their parasitic capacitive coupling effects are analytically compared, which shows that parasitic capacitances of on-chip interconnections could dominate over intrinsic capacitances of power devices. In addition, the parasitic effects of package and PCB are qualitatively analysed.

For topologies and architectures, a two-stage power converter architecture is proposed, where the input stage is a high-voltage switched-capacitor converter and the output stage is a low-voltage inductor-based converter. For the output stage, a buck converter using the integrated power MOSFETs is implemented with measured efficiencies around 93 %. For resonant converters, integrated power stages with parasitic bipolar effects, using piezo elements as resonant tanks, and discrete prototypes of class-DE series-parallel LCLC converters are investigated. The input stage is implemented as 380 V input switched-capacitor converters, using both Gallium Nitride (GaN) and Silicon Carbide (SiC) devices to properly address switching losses at high-voltage low-power levels. For power stages, a 10 W prototype reaches a peak efficiency of 98.6 % and a power density of 7.5 W/cm^3. For converters including driver and its supply, a 21.3 W prototype achieves a full-load efficiency of 97.6 % and a power density of 2.7 W/cm^3. For switching schemes, a concept of Asynchronous-Switched-Capacitor (ASC) is proposed for a 380 V, 4:1 switched-capacitor converter, and a peak efficiency of 95.4 % is achieved with reduced output voltage ripples. All these prototypes demonstrate the switch-capacitor feasibility at higher-voltage (> 200 V) lower-power (< 30 W) levels than previously published ones.

The main conclusions are that this research contributes to the analysis and design of the integrated high voltage power MOSFETs for on-chip integrated power converters, and contributes to the design and implementation of the switched-capacitor based two-stage architecture for discrete off-line power converters. It is concluded that efficient integrated off-line power conversion is currently in its infancy, and this research work fosters the framework and paves the way for future development in this area.

Abstract (Danish)

Miniaturisering tendensen i industriel og konsumer elektronik stiller konstant krav til reduktion i størrelse, vægt og pris på strømforsyninger. I dette forskningsarbejde er der taget udgangspunkt i lysdioder (LED) driver konstruktioner til intelligent belysnings systemer samt til brug i ”internet of things” (IoT). Strømforsyninger i denne kategori konverterer lysnet 220-240V AC Vrms europæisk standart, til lavspænding jævnstrøm (DC) i størrelsesordenen 13V med en effekt på 5-20W. Denne forskning fokuserer på DC-DC konvertere, med ensrettet AC-forsyning. Fysisk størrelses reduktion er kravet, men kan kun opnås samtidig med bedre effektoverførsel for at fastholde termiske grænser og tab. Fundamentale relationer begrænser, i form at afhængigheder imellem energitætheden og effektivitet, for at opnå både høj effektivitet samt høj energitæthed er, systematisk udvikling af udformning, komponenter og arkitekturen, ufravigelig.

Dette forskningsarbejde startede med integration af aktive komponenter på en enkelt ”chip” initialt høj spændings (≥ 100 V) Power MOSFETs på Silicon-on-Insulator (SOI). Den høje ydelse af løsningen er en kombination af, opbygningen, indkapsling og PCB, snylte egenskaber. Forskningen peger imod udvikling med Power Supply on Chip (PwrSoC) uanset opbygning og switch teknologi. Snylte kapaciteter I effekt halvledere er en yderst vigtig konstruktion parameter til strømforsyninger, for både hard-switched og soft-switched konvertere. En modellerings metode bliver fremlagt til systematisk analyse af ikke lineær snylte kapaciteter i Power MOSFETs, i forskellige tilstande, hvor der i datablade typisk specificerer kapaciteten i transistorens off-stadie. Ydermere den ikke lineære godhed (FOMs) som benyttes til sammenligning bliver systematisk analyseret og endvidere optimeret op til 18,3 gange for et givent stykke udstyr med quasi-zero voltage switching drift. Fire forskellige konstruktioner bliver foreslået og deres snylte kapaciteters effekt bliver analytisk sammenlignet, som viser at snylte kapaciteter i on chip konstruktioner kan blive dominerende. Ydermere bliver snylte kapaciteters effekt på både IC og print kvalitativt analyseret.

Opbygning og arkitektur til en to trins effekt-konverter bliver fremlagt hvor indgangs trinnet er en højspændings switched-capacitor kobling og udgangs trinnet er en lav spænding induktions baseret konverter. Udgangstrinnet er en buck konverter som benytter den integrerede power MOSFETs og yder en effektivitet i omegnen af 93 %. Resonans konvertere bliver belyst i forskellige udformninger herunder klasse-DE Seriel-parallel LCLC konverter. Indgangs trinnet er implementeret som 380 V switched-capacitor konverter der benyttes både Gallium Nitride (GaN) og Silicon Carbide (SiC) halvledere for at reducere switching tab ved høj spændings niveauer samt lille effekt. Udgangstrinnet, en 10W prototype opnår en peak effektivitet på 98,6 % og en energi tæthed på 7,5 W/cm^3. En prototype Konverter med effekt på 21,3 W viste en effektivitet på 97,6 % ved fuld belastning og en energitæthed på 2,7 W/cm^3. Valg a switch blev et koncept bestående af asynkron switche kondensatorer (ASC) drift på 380 V, 4:1 switchede kondensator konverter leverede en spids belastning effektivitet på 95,4 % med reduceret ripple. Alle de fremstillede prototyper leverede bedre resultater ved høj spænding (> 200 V) lav effekt (< 30 W) end tidligere publicerede konstruktioner.

Hoved konklusionen er at dette forskningsprojekt bidrager til konstruktion og analyse af integreret høj spændings effekt MOSFET i on-chip integreret strømforsyninger, ydermere bidrager det til konstruktion og implementering af switched-capacitor i to trins arkitektur for diskrete off-line strømforsyninger. Effektive integreret off-line strøm forsyninger er stadig på en spæd stadie, og dette forskningsarbejde baner vejen for fremtidig udvikling på dette område.

1. Introduction

1.1 Background and Motivation

Power supplies that convert universal mains AC power to low DC voltages (e.g. 5 V and 12 V) are essential parts of numerous products of industrial and consumer electronics. The examples of the applications are Solid State Lighting (SSL) products including light-emitting diodes (LEDs), organic light-emitting diodes (OLEDs), and polymer light-emitting diodes (PLEDs). The emerging intelligent systems for internet of things (IoT) are further examples, such as intelligent lighting systems (wall switches and movement sensors), intelligent electronic thermostats, intelligent liquid pumps, and alarm and surveillance systems. The power supplies of the household appliances used in our daily life are common examples, such as power supplies for television and kitchen appliances, and miniature chargers for computers and mobile phones.

As the development of the size reduction of the power supplies in all above examples relatively lag behind the advances of the technology development of other electronic parts in these applications, the power supplies significantly contribute to the overall system sizes of these applications. The miniaturization trend of electronic technologies continuously drives the demand of reductions in size, weight, and cost of power supplies. Among these demands, the size reduction of the power supplies is the direct requirement, and the weight and cost reduction requirement accompany the ministration trend.

The reduction of the sizes of the power supplies can, in principle, be realized from two perspectives, i.e. passive components and active components. The passive components, especially magnetic components, typically dominate the sizes of nowadays power supplies [1]. For the size reduction of passive components, increasing the switching frequency of power supplies can reduce the passive component values and energy storage requirements, and potentially (but not necessarily) reduce the sizes of passive components [1], [2]. The ongoing evolution of very high frequency (VHF) power supplies significantly contribute to the size reduction of passive components [3].

The size reduction of active components benefits and enables the size reduction of passive components. While maintaining other performances, the size reduction (relatively) of active components not only reduces the cost (the device area related) but also reduces on-chip device/layout parasitics and minimizes off-chip package/PCB parasitics, which increases the maximum permissible operating frequency thus enabling small passive components. Therefore, the research and development of active components is one of the important aspects of the miniaturization of power supplies. The integration of power semiconductors on integrated circuits (ICs), e.g. integrated high voltage power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), is hereby considered. This is an emerging research and development area, and directly contributes of the development of to the development towards Power Supply on Chip (PwrSoC), which significantly reduces the sizes of the power supplies. This motivates the first aspect of this research about the investigations of intrinsic properties and layout impacts of integrated power MOSFETs.

With the technologies to reduce the sizes of power supplies, the practical difficulties and challenges reside in the increased power density (output power divided by volume). While the size is reduced, the power density is increased for a given output power, and the thermal density is also increased for a given efficiency. As a result, the power density cannot unlimitedly be increased, in other words, the size cannot be unlimitedly reduced, because the thermal limits of the power supplies have to be maintained for the maximum losses of the power supplies. At the point when thermal limits are reached, further increasing the power density requires simultaneously improving the efficiency. Otherwise, the efficiency becomes limiting the power density, and starts to lower the power density due to additional sizes of heat sinks. Therefore, increasing the efficiency is the primary development goal and the premise of the realization of the size reduction of power supplies. Before the thermal limits are reached, i.e. within a temperature rise constraint, fundamental trade-off relationships exist between the power density and the efficiency. In principle, increasing the efficiency is fundamentally always possible by increasing the volume [4]. To achieve both high efficiency and high power density, systematic development is needed not only for components, but also for topologies, and architectures.

This motivates the second aspect of this research about architectures and topologies that potentially realize the integration of power converters. The switched-capacitor converters are of great considerations for on-chip integration [5] – [9]. The discrete switched-capacitor converters can potentially realize off-line power conversion [10]. One of the main challenges of switched-capacitor converters is the regulation, which can promisingly be resolved by a two-stage architecture, where the input stage is a high-voltage low-frequency switched-capacitor converter that is mainly responsible for power conversion, and the output stage is a low-voltage high-frequency inductor-based converter that is mainly responsible for regulation. The emerging wide band gap semiconductors such as Gallium Nitride (GaN) [11], [12] and Silicon Carbide (SiC) [13], [14] have superior properties and have the potentials to enable both high efficiency and high power density. These devices can also be actively combined to properly address certain topologies and architectures.

1.2 Project Objectives

The primary objective of the project is to investigate ways and feasibility of integrating high voltage active components on integrated circuits that can potentially enable further integration of high voltage off-line power converters. The investigations of topologies and architectures accompany this primary objective with the development goal of achieving both high efficiency and high power density. These are the essential properties to reduce the sizes of power supplies that can find their ways into numerous emerging applications such as power supplies in AC outlets and wall plugs for internet of things (IoT).

Table 1.1 General specifications of the research project.

Parameters	Specifications
Input voltage (AC)	220 – 240 Vrms AC (European mains)
Input voltage (DC)	310 – 340 Vdc (Rectified European mains)
Output voltage	12 – 13 V
Output Power	5 – 20 W

1.3 Scope of the Thesis

The scope of thesis is about the integrated technologies and the utilization of wide band gap semiconductors for the DC-DC power conversion. The focus of the DC-DC power conversion has two areas. One focus area is about integrated power MOSFETs that can potentially realize integrated power converters. This includes the modelling of the nonlinear parasitic capacitances of the power MOSFETs in a Silicon-on-Insulator (SOI) process, the modelling of the parasitic capacitive coupling of on-chip interconnections and the layout structures realization and comparison, and the analysis and optimization of nonlinear figure-of-merits (FOMs). The other focus area is for power stages and their driving circuits that can properly utilize power devices. This includes a two-stage power conversion architecture that is composed of high-voltage switched-capacitor converters and low-voltage inductor-based converters.

The contents of the thesis focus on the research work of related topics within the above scope. A large amount of work has been conducted with partner companies and manufacture foundries. Confidential contents such as information from collaborating companies and PDK (process design kit) information from IC foundries are not included in the thesis, except open access/public information for which references are provided.

1.4 Thesis Structure

The overall thesis structure is shown in Fig. 1.1. The relationships between the chapters and the appendix publications are indicated with the dotted lines. Chapter 1 is the introduction of the thesis, which includes the scope of the thesis, background and motivation, project objectives, and the thesis structure. Chapter 2 is the state-of-the-art, which summarizes the recent advances in components, topologies, and architectures. This chapter is the basis of the research work and to which the following chapters contribute to. Chapter 3 focuses on the integrated power MOSFETs, where both on-chip and off-chip characteristics are described and discussed. Chapter 4 is regarding the low-voltage inductor-based converters, where the implementation of a buck converter using the integrated power MOSFETs and other resonant power stage investigations are presented. Chapter 5 concentrates on the high-voltage switched-capacitor converters, which includes the analysis and design of the power stage, the driving circuit, the complete power converter, and a proposed switching scheme of asynchronous-switched-capacitor and its realization based on GaN and SiC devices. Chapter 6 summarizes and concludes the thesis. Chapter 7 describes the future work.

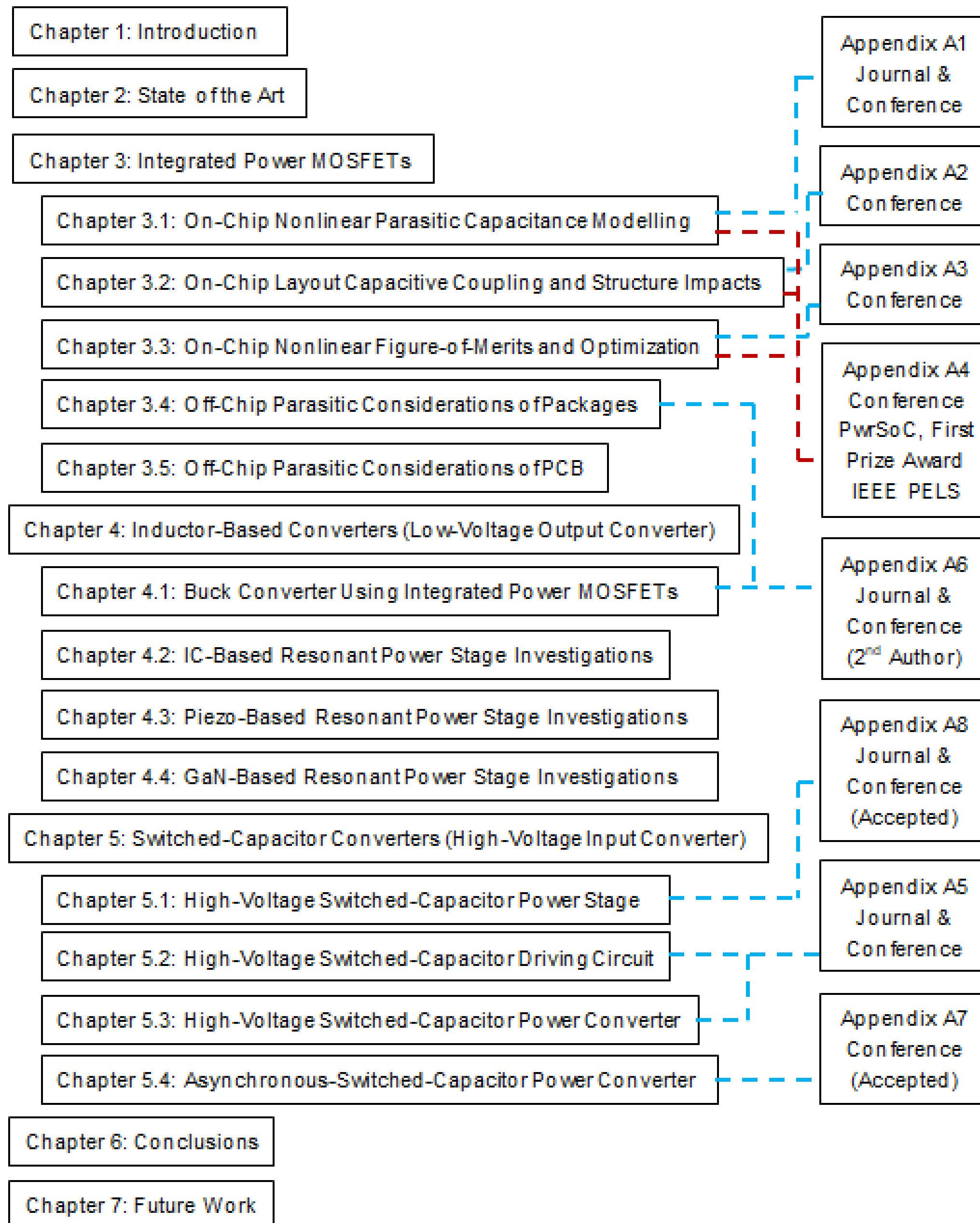


Fig. 1.1 Thesis structure and relations to appendix publications.

2. State of the Art

This chapter summarizes the state of the art of the related research topics and recent advances in components, topologies, and architectures. This formulates the background of the research work and to which the research work contributes to. The initial and original motivation of the technical development of the following chapters is also included.

2.1 Review of Power Supply on Chip (PwrSoC) Workshops

The first aspect of this research work is about the integration of high voltage (≥ 100 V) power MOSFETs. This is tightly related to and contributes to the development towards Power Supply on Chip (PwrSoC). The international workshop on PwrSoC [15], organized by the Institute of Electrical and Electronics Engineers (IEEE) Power Electronics Society (PELS) and the Power Sources Manufacturers Association (PSMA), is the leading workshop in this research field where world-leading companies and universities present cutting-edge advances in integrated power conversion technologies. The selected representative publications in PwrSoC are [16]-[58] for the years from 2008 to 2016. Each of the contributions is state-of the-art and covers a broad range of topics. It is hardly possible to categorize these contributions. Generally speaking, [16]-[28] are switched-capacitor related, [29]-[35] are about system and applications, [36]-[47] are semiconductor technologies related, [48], [49] are about magnetics, [50] is about capacitors, [51], [52] are regarding integration and packaging, [53]-[56] are about topologies and control, [57], [58] are about granular power. A 3 mW micro power supply [59] is composed of an integrated AC-DC converter, an integrated DC-DC converter, and one external capacitor in between. Nearly all of the published work focuses on integrated converters with 48 V and 12 V bus lines or lower intermediate voltages, except discrete prototypes or processes development.

The only four cases of integrated converters that interface voltages above 48 V in [16]-[59] are summarized in Table 2.1. All these reported cases have capacitor-based topologies. The case 1 [23], [60] have a relatively low input voltage, and the case 2 [24], [61] is limited by the level of integration with a two-chips stacking structure and other external components. The case 3 [25], [62] is AC mains interfaced, but most of the chip area is occupied by a single large high-voltage capacitor [62], and this µW-level converter is not easily scalable to higher output power levels unless external components are used [63]. The case 4 [59], [64] uses a directly coupled full wave rectifier combined with two shunt regulators, so the input transistors have to be high-voltage devices that are connected to the mains voltage. Both the case 3 and the case 4 are mains interfaced but the output powers of these converters are in the µW-mW range. This research started with investigations of directly integrating high voltage (≥ 100 V) power MOSFETs on a single chip. The intrinsic nonlinearities and layout impacts of 100 V power MOSFETs in a partial SOI process have been investigated, and this work contributes to the PwrSoC workshop in 2016.

Table 2.1 Only 4 cases of integrated converters that interface voltages above 48 V in [16]-[59].

Case	1 [23]	2 [24]	3 [25]		4 [59]
Year	2010	2014	2014		2016
Prior art	2009 [60]	2013 [61]	2013 [62]		2016 [64]
Contributors	KU Leuven	Columbia University UC Berkeley	KU Leuven		Reutlingen University
Topology	Switched-Capacitor	Switched-Capacitor (Hybrid resonant)	Capacitive AC-DC (Capacitive voltage divider)		Full wave rectifier and Switched-capacitor
Integration	Integrated	**Limited-Integrated**	Integrated	Partly-Integrated	Partly-Integrated
Input voltage	12 Vdc	85 Vdc	230 Vrms	230 Vrms	230 Vrms
Output voltage	70 Vdc	42.5 Vdc	3.3 Vdc	3.3 Vdc	3.3 Vdc
Output power	**320 mW**	17W, 2-chips stacking	**9.5 µW**	**7 mW**	**3 mW**

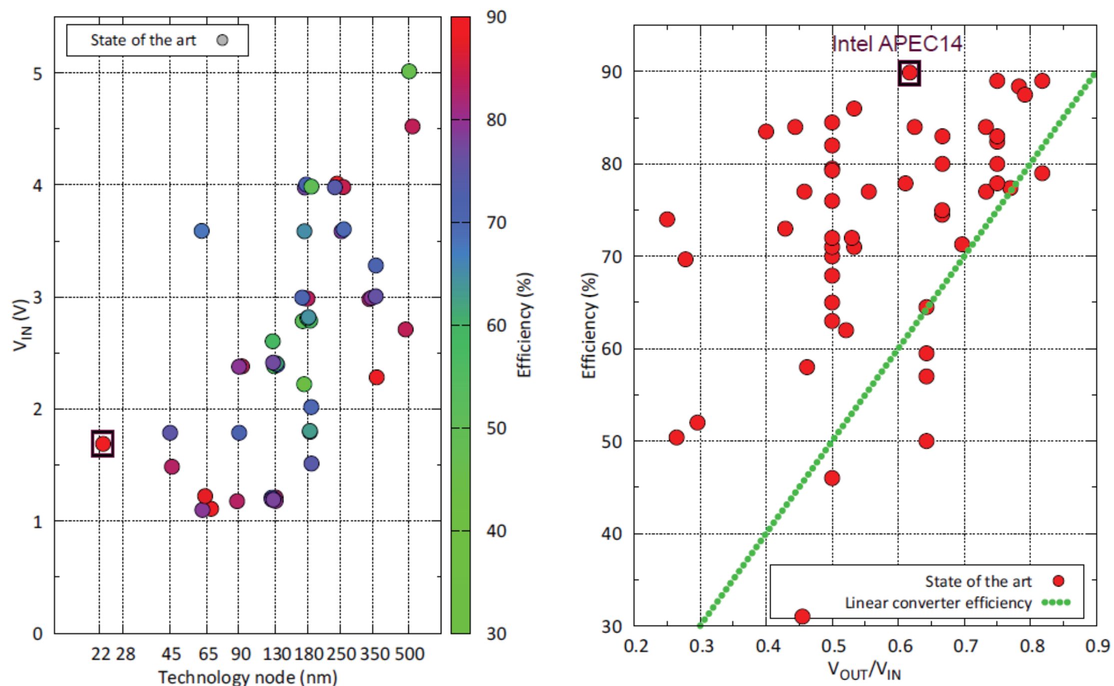


Fig. 2.1 State-of-the-art highly integrated inductive DC-DC converters [33].

In addition to the above high voltage capacitor-based topologies, high frequency inductor-based converters are also of the state-of-the-art considerations [65]-[97]. Generally speaking, the majority of the research combines high frequency operation and multiphase technology to enable small values of passive components [65] so that these components can be integrated on-chip. In addition, advanced topologies are used such as hybrid converters composed of buck converters and regulators [66], [67], three-level buck converters [68], [69], and resonant gate drivers [70], [71]. Special processes are also used such as SiGe [72], GaAs [73], and SOI [74].

Zero voltage switching (ZVS) technology is used in [72], [75]. Customized solutions for specific applications are possible [76]-[78]. Two major research fields are about different ways of packaging and integration [79]-[91] and control technologies [92]-[97] such as frequency control [92], and hysteretic related control [93]-[97].

The state-of-the-art high frequency, highly integrated inductive DC-DC converters are summarized in Fig. 2.1 [33]. The most important thing to note is that the input voltages of these DC-DC converters are limited to 5 V or below. The implementation of on-chip inductors is still the blocking issue for high-voltage power converters. The voltage impacts at high-voltage levels on active components are to be discussed below.

2.2 Power MOSFETs

This section summarizes the recent advances in modelling, layout structures, and figure-of-merits (FOMs) of power MOSFETs. These topics are related to each other and are the areas to which this research work contributes.

2.2.1 Modelling of Power MOSFETs

Inductor-based converters such as resonant converters (resonant converters will be discussed in the section 2.3.1) generally use or tend to use soft-switching technologies. Soft-switching technologies such as zero-voltage switching (ZVS) and zero-current switching (ZCS) are precisely about turn-on and turn-off transients and properties of power switches, e.g. power MOSFETs. Academia and industry have been trying to design, operate, and control power converters as close as soft-switching conditions of power switches. However, difficulties of accurate soft-switching reside on the hard-to-be-determined nonlinear parasitic capacitances of power switches. Conventionally, power switches are characterized in terms of switching time and/or gate charge, which give little insight to the nonlinearities of the parasitic capacitances.

The analyses of the nonlinear parasitic capacitances of the power MOSFETs can benefit power converter designers for getting insight into soft-switching technologies and investigating new topologies such as resonant converters, where parasitic capacitances are a part of the key design parameters. These analyses also benefit hard-switching converters where switching losses and gating losses are determined by the nonlinear parasitic capacitances as well. However, such information is typically not available, and this is particularly due to the fact that industrial datasheets typically specify capacitances only in off-states, e.g. the input capacitance C_{iss} and the output capacitance C_{oss} are provided only at the condition when the gate and the source of the power MOSFETs are shorted [98], [99]. There is no direct information about how the parasitic capacitances behave versus different bias voltages. Further analysis shows that simple extrapolation from the off-state capacitances could sometimes be even misleading. Therefore, this research work intends to establish a proper way to characterize the nonlinear parasitic capacitances of the power MOSFETs, and the nonlinearity analysis will be described in the section 3.1.

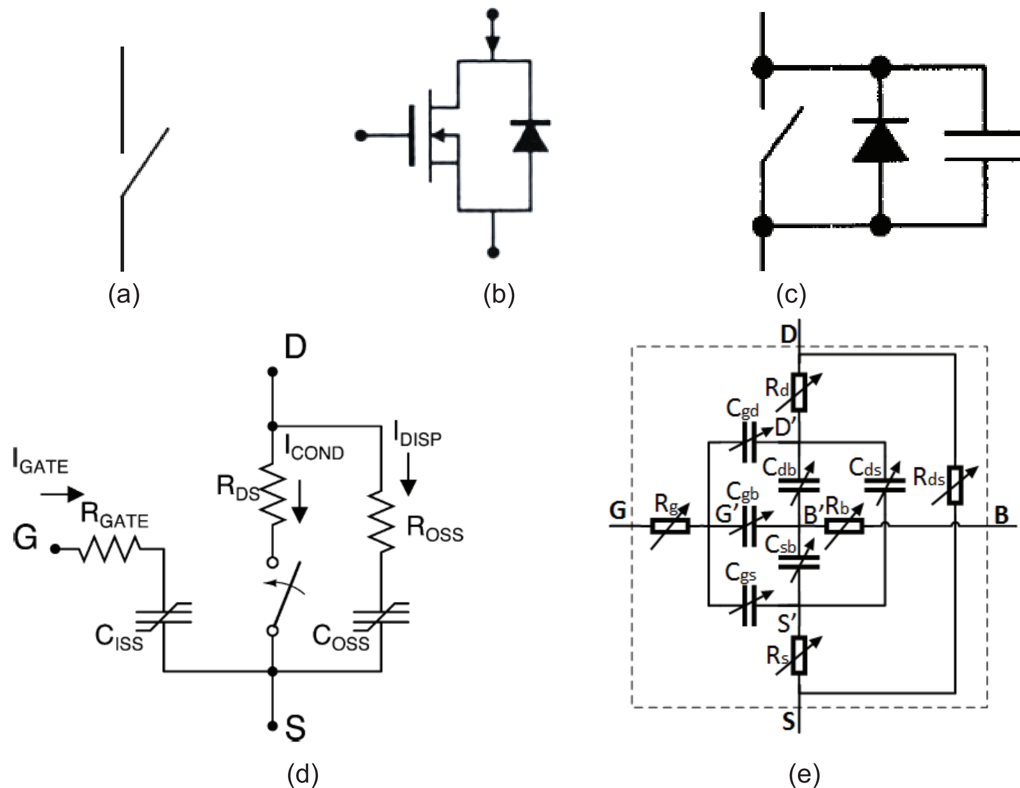


Fig. 2.2 Conventional and state-of-the-art modelling of power MOSFETs. (a) Model used in a Bachelor degree textbook [100]. (b) Model used in a Master degree textbook [101]. (c) Model used in a scientific paper [102]. (d) State-of-the-art loss model by MIT [1], [103], [104]. (e) State-of-the-are small-signal model by this work [Appendix A.1].

The conventional and the state-of-the-art modelling of power MOSFETs are shown in Fig. 2.2. The most simplified model of an ideal switch, with or without on-resistance, is shown in Fig. 2.2 (a). This model is generally used for system level analysis. The model in Fig. 2.2 (b) takes the body diode into account and facilitates basic converter level analysis. For analytical equations development, an ideal capacitor is typically added and assumed, as shown in Fig. 2.2 (c). The state-of-the-art loss model of power MOSFETs is shown in Fig. 2.2 (d). The most important thing to note for this model is that the drain-to-gate capacitance C_{gd} is ignored [103], i.e. the coupling from the output port back to the input port (through C_{gd}) is neglected [1]. Furthermore, for loss analysis purpose, the input and output capacitances in this model are lumped with equivalent linear capacitances. All the above models do not provide the nonlinearities of the parasitic capacitances and are not used for the purpose of analysing the switching transients. The small-signal model in Fig. 2.2 (e), which is proposed by this work and further described in the section 3.1, focuses on the analysis of the nonlinear behaviour of the parasitic capacitances.

2.2.2 Layout Structures of Power MOSFETs

The electrical parameters of on-chip interconnections become the practical bottlenecks of circuit performances [105], and this is especially true for high-power-density converters [106]. The coupling capacitances may be measured directly on-chip but the accuracy of the measurements suffers from the supply noise [107]. Therefore, a modelling/analysis method is needed.

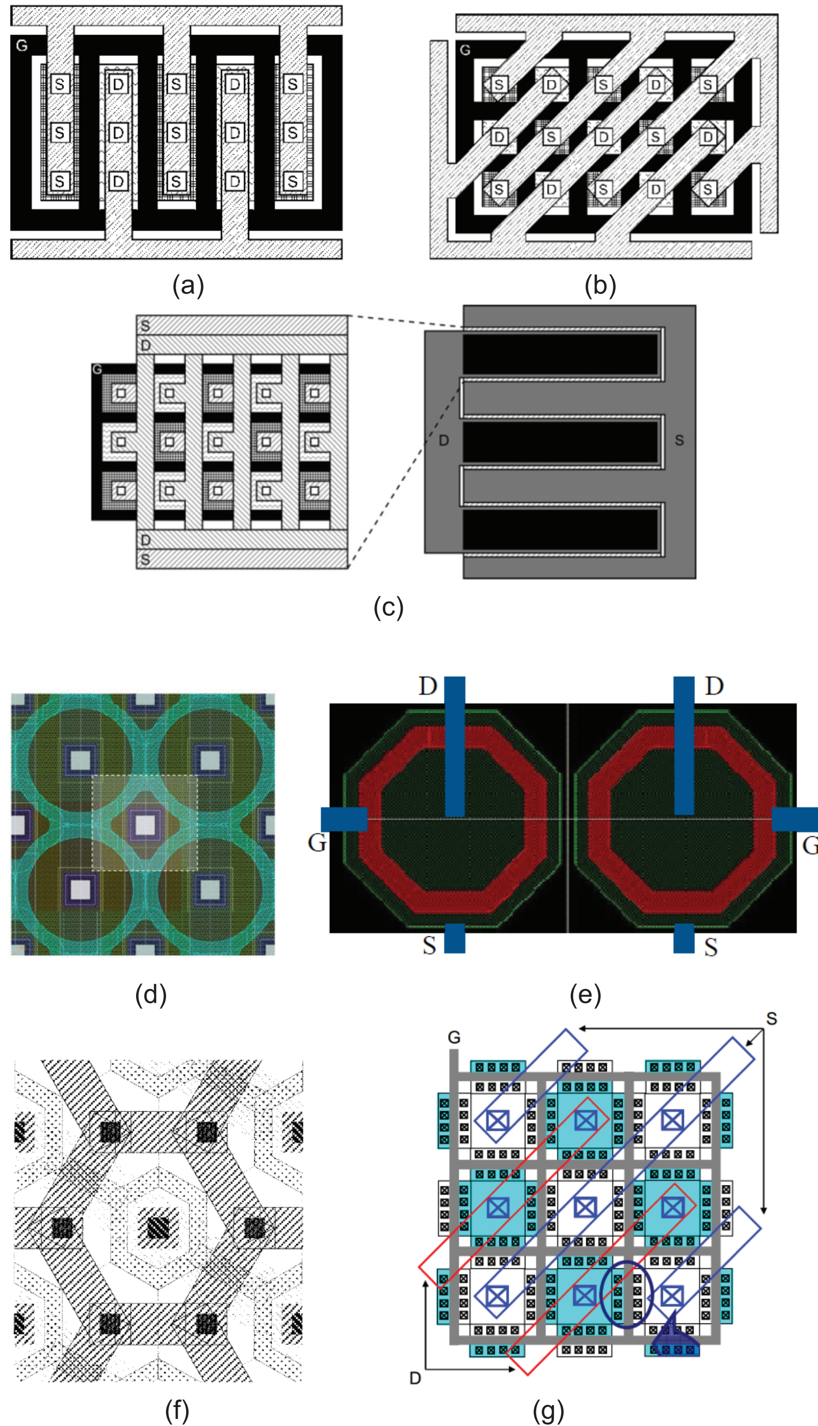


Fig. 2.3 Recent advances in layout structures of power MOSFETs. (a) Linear finger [108]. (b) Waffle-shaped [108]. (c). Modified waffle-shaped [108]. (d) Overlapping circular-gate [109], [110]. (e) Octagonal [111]. (f) Hexagonal [112]. (g). Hybrid-waffle [113].

The capacitive coupling of on-chip interconnections is embedded in the layout structures of power MOSFETs. Accordingly, the layout structures impact the performances of power MOSFETs. The examples of recent advances in layout structures are summarized in Fig. 2.3. In Fig. 2.3 (a), the linear finger structure is shown as a relatively conventional structure. As a

comparison, the waffle-shaped structure is shown in Fig. 2.3 (b). The waffle-layout structure is known of having a reduced overall area in a compact fashion, and hence a high density is the main advantage. In addition, the structure can potentially have low parasitic drain capacitances [108]. However, the 45-degrees routing of the drain and source connections is not optimal for high current applications, due to the current unbalance caused by the angled non-symmetrical connections [108]. In addition, the total width of the drain and source connections is relatively small for handling high peak currents.

Another way of implementing waffle-layout is shown in Fig. 2.3 (c). This modified waffle-layout structure has 90-degrees (vertical and horizontal) drain and source connections, which are located in different metal layers. Note that the drain and the source are connected on both sides, and the space between the waffle-layout structures has to be reserved for substrate contacts and guard rings. On the right side of Fig. 2.3 (c), the overall drain and source connections are implemented in a large metal finger structure. The width of the metal fingers is not only associated with the current handling capability. There is a trade-off to consider, i.e. the wider the metal finger is, the lower the parasitic series resistance becomes, but the parasitic capacitances increase simultaneously. The metal fingers are normally made in upper metal layers, to minimize the parasitic capacitances of drain and source to substrate.

The overlapping circular-gate structure, as shown in Fig. 2.3 (d), is used to improve the power-density of integrated power MOSFETs. Gate overlapping is possible by overlapping the circular gates of the neighboring cells of CGT (Circular-Gate Transistor), which can save up to 30-60 % layout area, as compared to RGT (Rectangular-Gate Transistor) with an equivalent aspect ratio [109]. The lower on-resistance can also be achieved at the same time, due to the higher current stirring capability per active area. The parasitic junction capacitances associated with drain-substrate can also be minimized. One drawback of the overlapping circular-gate structure is that there is a section of gate annulus that does not contribute to the drain current. In addition, the gate overlapping slightly reduces the breakdown voltage, as compared to conventional CGT, but it is still slightly above the breakdown voltage of RGT.

The octagonal structure is shown in Fig. 2.3 (e). It is mainly used to achieve good gate-source voltage matching in the sub-threshold region for low-power applications at very low current levels [111]. The octagonal structure can remove the hump effect, which would otherwise strongly degrade the device matching in the weak-inversion sub-threshold region. For the octagonal structure, the polysilicon gate is already approaching the ring shape. The hexagonal structure is shown in Fig. 2.3 (f). The main advantage of hexagonal structure is the low parasitic drain and source capacitances, due to the very small drain and source area. This hexagonal structure can achieve good matching and small area at the same time [112].

Finally, the hybrid-waffle structure is shown in Fig. 2.3 (g). By comparing the HW (Hybrid Waffle) structure and the conventional MF (Multi Finger) structure, it shows that the hybrid-waffle structure is actually an effective trade-off [113], between the metal width of the diagonal source/drain connections and the active area of the device, which allows effective optimization between conduction loss and switching loss. It also shows that, with large enough area, both reduction in overall on-resistance and smaller total gate charge can be achieved at the same time with the hybrid-waffle structure, compared to the multi-finger structure. Note that the total width of the multi-finger structure is wider than that of the hybrid-waffle structure for the same

chip area, thus the W/L ratio of the hybrid-waffle structure is smaller than that of the multi-finger structure. It means that the hybrid-waffle structure can achieve smaller overall on-resistance with a large enough device area, and it is fundamentally because of the reduction of parasitic resistances due to wide metal connections.

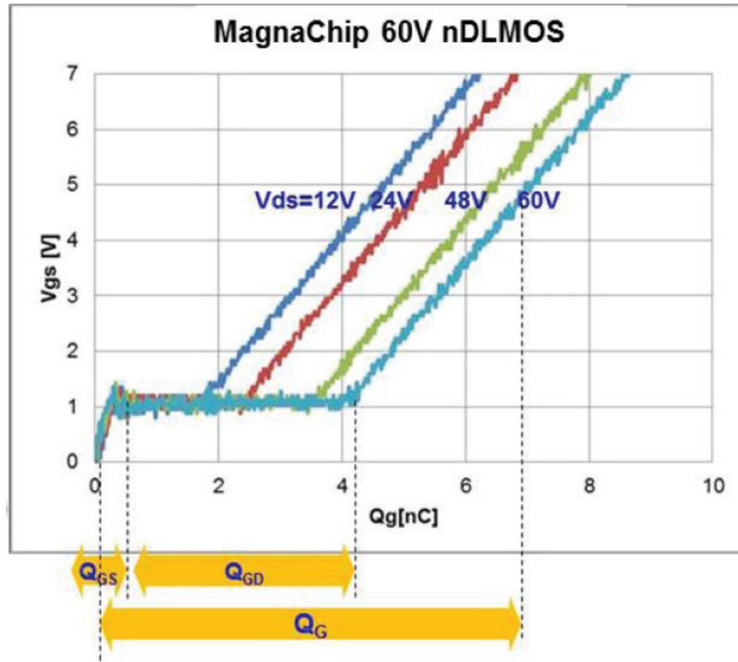
All these layout structures, especially the overlapping circular-gate structure, the octagonal structure, the hexagonal structure, the waffle-shaped structure, and the hybrid-waffle structure actually become obsolete. These layout structures are commonly not permitted in deep submicron processes, due to the polysilicon DRC (Design Rule Check) rules, i.e. the 90-degrees (or other angles) of the turn of the gate polysilicon is generally not allowed in deep submicron processes. The linear finger structure and the modified waffle-shaped structure have the potentials to be further improved to comply with the corresponding DRC rules, e.g. the gate network can be re-distributed in upper metal layers. Furthermore, a high active-area density cannot be a single FOM (Figure of Merit) of a layout structure. The substrate contacts and the guarding rings should also be taken into account between the active-areas. This is especially true when the waffle-shaped structure [114], [115] is actually an effective trade-off between the metal interconnections and the active-area. A common principle of all the structure improvements is about sharing active-areas and/or interconnections in all geometrical directions.

2.2.3 Figure-of-Merits (FOMs) of MOSFETs

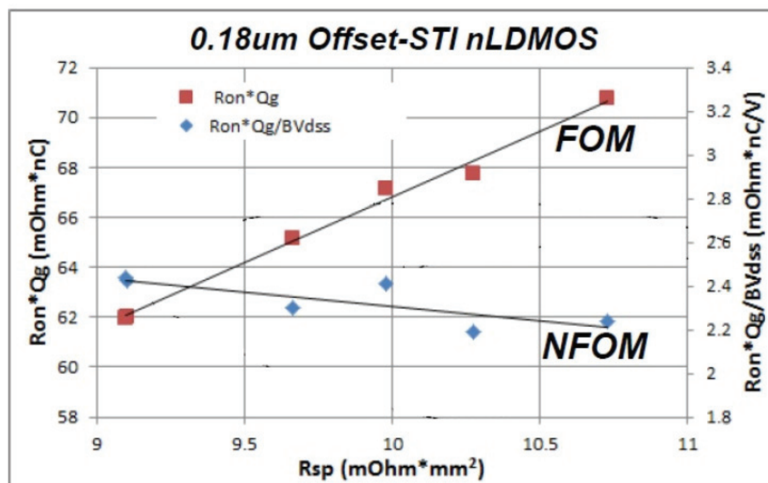
The primary purpose of figure-of-merits (FOMs) in power semiconductor industry is for technology-to-technology comparisons. Different technologies are quantitatively compared using FOMs [12], and a lower FOM index represents a better performance. The second usage of FOMs is for evaluating the overall performance of a power device for a switching application [116]. The conventional BFOM (Baliga FOM) is solely based on the conduction loss minimization [117]. Therefore, the BFOM is not applicable to applications where switching losses are not negligible. Various forms of FOMs exist [12], [42], [43.], [116]. However, it is found that these FOMs are not consistently used [116], [118].

FOMs typically consist of trade-off parameters, e.g. on-resistance and gate charge (or specific parts of gate charge). These trade-off parameters depend on the specific operating conditions. Therefore, the values of the FOMs are fundamentally nonlinear, and application-dependent on voltage and current conditions. A systematic analysis is needed to optimize the nonlinear FOMs in order to fully explore the performance potentials of integrated power MOSFETs.

For the parameters on which FOMs are based, e.g. the gate charge and/or the output charge may be derived by calculating the integration of the parasitic capacitances as a function of an operating voltage such as the drain-source voltage V_{ds} [12], [119], [120]. In fact, the parasitic capacitances depend on not only the drain-source voltage V_{ds} but also the gate-source voltage V_{gs} [Appendix A.1]. Therefore, the calculated results, which take only one of the voltages as a variable for the calculation of the integration, tend to lead to errors.



(a)



(b)

Fig. 2.4 Recent investigations of figure-of-merits (FOMs). The NFOM is defined as Normalized FOM in [43]. (a) Q_g depends on the applied V_{ds}. (b) Different trends of the FOM and the NFOM.

Capacitance values or resistance values cannot be used as standalone indicators for device-to-device comparisons [121]. A device with a higher capacitance value may switch faster than another device with a lower capacitance value [122]. A device with a higher on-resistance value may show a better overall efficiency for a converter, compared to another device with a lower on-resistance value [123]. In addition, a charge parameter may also not correctly reflect switching performances, e.g. the output charge of a device is more than 100 times lower than the output charge of another device, but it turns out that the output charge energies of these two devices are nearly the same [37].

There is no standard test circuit to obtain the gate charge parameters, and different configurations [124]-[134] are compared in this research work for choosing the most appropriate test circuit for the purpose of obtaining the FOMs.

$$\frac{A \cdot R_{on}}{V_B^2} = \frac{k}{\mu_n \cdot \varepsilon_s \cdot E_c^3} = \text{Semiconductor material}^* \text{ figure of merit (FOM)} \qquad (2.1)$$

*process specific for majority carrier devices, e.g. MOSFETs
A = device area
R_{on} = switch on − resistance
V_B = device breakdown votlage
μ_n = electron mobility
ε_s = semiconductor permittivity
E_c = critical electric field (for avalanche breakdown)

The semiconductor material FOM [135], as shown in (2.1), can be applied to majority carrier devices (e.g. MOSFETs) in different semiconductor technologies such as silicon (Si), Silicon Carbide (4H-SiC), Gallium Nitride (GaN), and the element semiconductor diamond (C) [136], [137]. There are two key points of this FOM. First, the wide band gap semiconductors SiC and GaN are superior to the conventional Si technology. This is fundamentally because the critical electric fields E_c of SiC and GaN are about an order of magnitude higher than that of Si. As a result, the FOMs of SiC and GaN are theoretically about three orders of magnitude lower/better than that of Si. Second, this semiconductor material FOM reveals the fundamental theory underneath the common trade-offs such as the gate charge with the switch on-resistance, and the parasitic capacitances with the switch on-resistance. For a given semiconductor technology, the root performance-limiting factor is actually the device breakdown voltage V_B. The product of $A \cdot R_{on}$ is proportional to the square of V_B, i.e. $(A \cdot R_{on}) \propto V_B^2$. For example, if the device breakdown voltage V_B increases 10 times from 10 V to 100 V, the result is that the switch on-resistance R_{on} is increased 100 times for a given device area, or the device area (and the cost) is increased 100 times to keep the same on-resistance R_{on}. This is generally applicable regardless of switching frequencies and hard/soft switching technologies. Therefore, a strategical way of development is to use architectures and topologies that can reduce the voltage stresses of power semiconductors to fully enhance the performances of the devices.

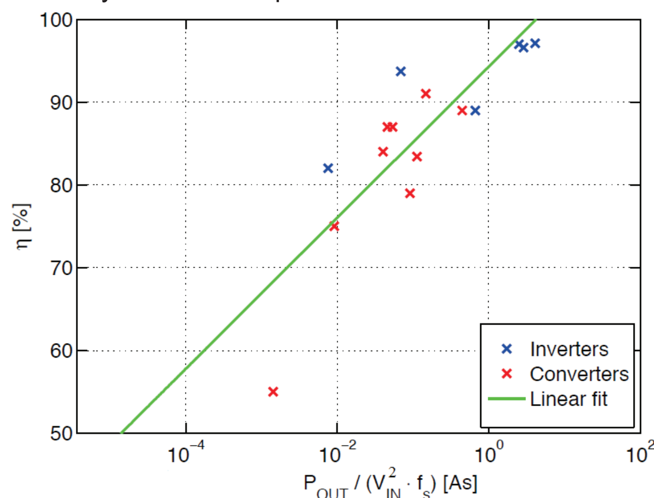


Fig. 2.5 Inspection work [123] [138] of research on resonant inverters and converters.

$$\eta \sim \frac{P_{out}}{V_{in}^2} \cdot \frac{1}{f_s} \quad (2.2)$$

$$f_{s,max} \propto \frac{P_{out}}{V_{in}^2} \quad (2.3)$$

The challenge of the research project is not only about the high input voltage level, it is also about the combination of the high input voltage and the low output power, i.e. it is furthermore challenging for a high-voltage low-power converter design. It is interesting to mention the inspection work [123], [138] of previous research on resonant inverters and converters. It shows that there is a connection between the efficiency η and the ratio of P_{out}/V_{in}^2, as shown in Fig. 2.5. The efficiency η tends to get worse with the square of the input voltage, and it gets even worse for a low output power at a given high input voltage. This is also reflected in (2.2). As an example, the maximum switching frequency of a class-E inverter/amplifier for optimum-efficiency is proportional to the ratio of P_{out}/V_{in}^2 in (2.3) [123]. Early research [139] in 1989 shows the same relationship. Therefore, from an efficiency perspective, the output power needs to track the input voltage, i.e. the constraints to achieve a high efficiency of a high-voltage high-power design or a low-voltage low-power design are generally smaller compared to a high-voltage low-power design.

2.3 Topologies

This section has two parts, i.e. resonant converter topologies, and switched-capacitor topologies. The advanced topologies such as resonant-switched-capacitor topologies are considered as switched-capacitor related in this section.

2.3.1 Resonant Converter topologies

State-of-the-art resonant converters and resonant gate drivers are summarized in Table 2.2.

Table 2.2 Resonant converter related topics and references.

Topics	References
Review of advances in resonant converters	[1], [3]
Nonlinear parasitic capacitances/resistances of power switches impacts on resonant converters	[140]-[145]
Resonant converters use air core PCB inductors	[146]-[148]
Class φ_2/Class EF_2 based inverters/converters	[149]-[155]
Resonant boost converters	[103], [104], [156]-[158]
Resonant rectifier	[152], [160]-[163]
Matching network related	[164], [165]
Resonant SEPIC converters	[166]-[168]
Architectures of resonant converters	[169], [170]
Conventional class E converters	[123], [172]-[175]
Review of half-bridge resonant converts	[176], [177]
Specific class DE inverters/converters	[102], [178]-[186]
Resonant gate drivers related	[152]-[154], [156], [157], [166], [168]-[171], [179], [187]-[197].

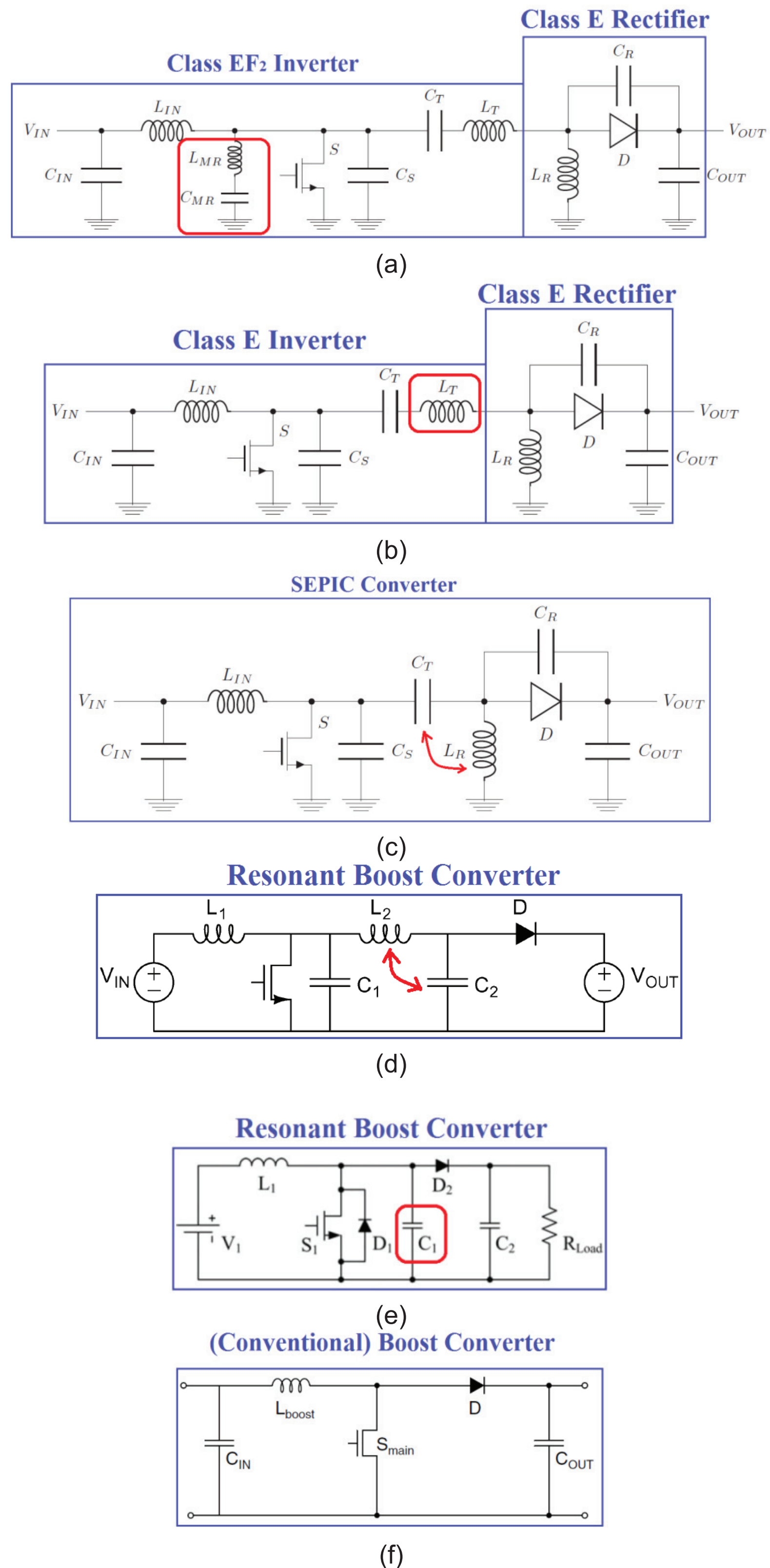


Fig. 2.6 State-of-the-art resonant converters and conventional boost converter.
(a) Class EF_2 inverter and Class E rectifier [167]. (b) Class E inverter and Class E rectifier [167]. (c) SEPIC converter [167]. (d) Resonant boost converter [157]. (e) Resonant boost converter [159]. (f) Conventional boost converter [1].

State-of-the-art resonant inverters/converters commonly use zero voltage switching (ZVS), or use ZVS with further zero dv/dt switching at the switches turn on transients to address the switching losses at the increased switching frequencies. Increase in switching frequency directly reduces the energy storage requirements of power converters [1], thus potentially enabling small passive components and fast transient response. As the switching frequency increases, a design strategy is to either utilize or compensate the parasitics of semiconductor devices. Topologies that absorb device parasitic capacitances as part of the operation are generally preferred. Note that the absorption of the parasitic capacitances is only applicable to the extent that device package inductances are not large and can be ignored [157]. The interconnection inductances of packages and PCB become increasingly contributing to the element impedance as switching frequencies increase. Therefore, topologies that can also absorb device parasitic inductances are further desirable. Several state-of-the-art resonant converter topologies are compared in Fig. 2.6. These topologies are described from a topology derivation point of view.

In Fig. 2.6 (a), class φ_2/EF_2 inverters use low-order lumped network to shape the drain-source voltage waveform to a quasi-trapezoidal voltage waveform across the switch, which aims to lower the peak drain-source voltage value, i.e. lower the voltage stress of the switch. This is achieved by tuning the input impedance of the low-order lumped network to have low impedance at the second harmonic and high impedances at the fundamental and the third harmonic of the switching frequency [150], [151]. Class φ_2/EF_2 inverters are simplified variants of the class φ/EF inverters that use high-order lumped network.

By removing the L_{MR} and C_{MR} in Fig. 2.6 (a), a conventional class E inverter is retrieved in Fig. 2.6 (b). Class E inverters are commonly used but have two main drawbacks. First, class E inverters need large valued (choke) input inductors, which also slow down the setting time of the inverters to the operating points. Second, for the idealized operation of class E inverters with ideal switches at 50 % duty cycle, the peak switch voltage stress is about 3.6 times the input voltage [150], [151]. In practice, the nonlinearities of the device parasitic capacitances have to be taken into account, which further increase the switch voltage stress to about 4-4.4 times the input voltage [150], [151], [153], [154]. By removing the L_r in Fig. 2.6 (b), a SEPIC (Single-Ended Primary Inductor Converter) converter is derived, as shown in Fig. 2.6 (c). The SEPIC converter topology is tightly close to a class E inverter cascaded with a class E rectifier, hence the peak switch voltage stresses of SEPIC converters resemble those of class E converters [166]-[168]. In other words, SEPIC converters do not reduce peak switch voltage stresses as compared to class E converters.

By interchanging the matching network components of C_r and L_R in Fig. 2.6 (c), a resonant boost converter [157] is obtained in Fig. 2.6 (d). Note that in the resonant boost converter, a portion of the power is transferred directly from the input to the output [157], but it shows that the resonant boost converter still suffers from the peak switch voltage stresses about 3.3-3.7 times the input voltage. By replacing the L_2 with the diode D in Fig. 2.6 (d), another resonant boost converter [159] is derived in Fig. 2.6 (e). The resonant boost converter in Fig. 2.6 (e) can also be obtained by adding a capacitor in parallel with the switch of the conventional boost converter [1], [100] that is shown in Fig. 2.6 (f). For both converters in Fig. 2..6 (e) and (f), the rectifier diode transfers the energy stored in the inductor directly to the output [159]. Therefore, the peak switch voltage stresses of these two converters closely track the output voltages.

All the above topologies use (single) ground-referenced switches, which are generally preferred at very high frequencies [1]. Switches that are referenced to switching nodes add challenges of driving circuits to provide desired gate drive waveforms with nonlinear parasitic capacitances tied to the switching nodes. However, a half-bridge class DE converter (class DE converter topologies will be discussed in details in the section 4.4) reduces the peak switch voltage stress to the level of the input voltage. This is a major advantage for high voltage resonant converters, e.g. off-line power converters. The general comparison of the voltage stresses on switches of different resonant converters is summarized in Fig. 2.7. In addition to the resonant inverter/converter topologies that strive to trapezoidal wave-shaping the drain-source voltage of switches, trapezoidal wave-shaping the gate-source voltage of switches also shows better performances for resonant gate drives (e.g. [187]) compared to the conventional sinusoidal or hard-switched gate drives.

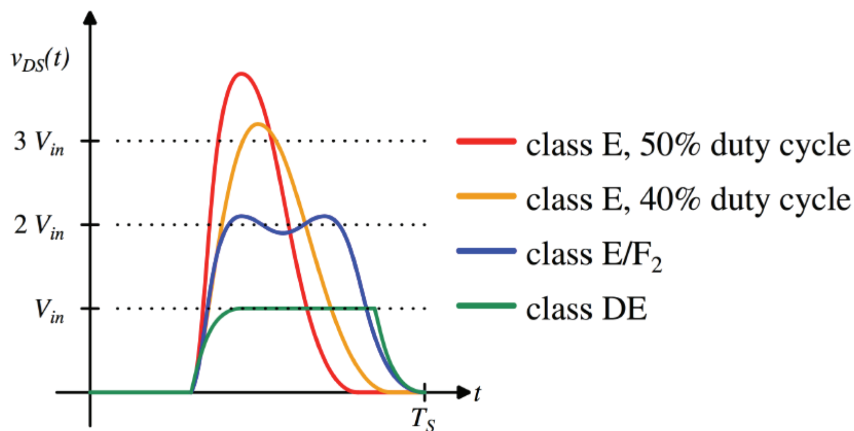


Fig. 2.7 General comparison of voltage stresses of switches in resonant topologies [3], [195]. In practice, nonlinear parasitic capacitances add further voltage stresses on switches, e.g. about 4-4.4 times the input voltage for class E inverters [150], [151], [153], [154].

There are only four cases of on-chip implemented resonant converters in [140]-[197] and the four cases are summarized in Table 2.3. The case 1 [175], the case 2 [184], and the case 3 [185] are simulation results only. The case 4 [186] is implemented in a 130 nm 1.2 V CMOS process with an on-chip spiral inductor and an on-chip MIM capacitor. However, its output power is very low up to 11.6 mW. The development of on-chip resonant converters is still in its infancy, and high voltage ones are further challenging.

Table 2.3 Only 4 cases of on-chip integrated resonant converters in [140]-[197].

Case	1 [175]	2 [184]	3 [185]	4 [186]	
Topology	Class E	Class DE	Class DE	Class DE	
Inverter/Converter	Converter	Inverter Only	Converter	Inverter Only	
Input Voltage	**5 V**	**2 V**	**2 V**	**1.2 V**	
Output Voltage	4.5 V	0.32 V	0.5 V	0. 585 V	0.312 V
Output Power	200 mW	**12.5 mW**	**12.5 mW**	**6.9 mW**	**11.6 mW**
Efficiency	72 %	48 %	N/A	65.2 %	47 %
Comments	**Simulation Only**	**Simulation Only**	**Simulation Only**	Measurement Results	

2.3.2 Switched-Capacitor topologies

With the high-voltage challenge in mind, the on-chip capacitor technologies are reviewed [5], [9], [50] and summarized in Table 2.4. The capacitance densities of these technologies decrease from deep trench capacitors, MOS capacitors, MIM capacitors, to MOM capacitors. For high-voltage integrated converter designs that interface voltages above 48 V, the MOM technology is the only practical choice. However, by comparing the deep trench technology (assume 300 nF/mm^2) and the MOM technology (assume 0.3 nF/mm^2), there is three orders of magnitude difference between the capacitance densities. For the same capacitance that is needed, the capacitor size of a high-voltage design is 1000 times larger than the capacitor size of a low-voltage design. Naturally, the power density of a high-voltage converter design is dramatically lower than that of a low-voltage converter design, if the size of the high-voltage converter is at all acceptable considering that the cost is generally proportional to the chip area. For an intuitive example, if a capacitor with a capacitance value of 3 nF is implemented with the deep trench technology and the MOM technology, respectively, then a 1.5 V, 3 nF deep trench capacitor occupies 0.01 mm^2, whereas a 100 V, 3 nF MOM capacitor would consume 10 mm^2. A chip area of 10 mm^2 for a single capacitor that is 1000 times larger than a deep trench capacitor with the same capacitance is generally not acceptable. Therefore, other approaches are needed for the high-voltage switched-capacitor converters in the chapter 5.

The general comparison of semiconductor technologies is summarized in Table 2.5. It is seen that the emerging wide band gap semiconductors GaN and SiC are superior to the conventional Si technology in the voltage range of hundreds of volts. Therefore, GaN and SiC are of the great considerations to be used for converter designs of this research.

Table 2.4 On-chip capacitor technologies are generally not for high voltage designs above 48 V.

IC Capacitor	Capacitance Density	Examples
Deep Trench	100~300* nF/mm^2=fF/µm^2	~1.5 V [9]
MOS	~10 nF/mm^2=fF/µm^2	~1.8 V/ 5 V
MIM	1~3 nF/mm^2=fF/µm^2	~5 V
MOM	0.2~1 nF/mm^2=fF/µm^2 (decrease with voltage)	~5-50 V

*500~1000 nF/mm^2 in research, e.g. [50]
MOS=Metal-Oxide-Semiconductor
MIM=Metal-Isolator-Metal
MOM=Metal-Oxide-Metal

Table 2.5 General comparison of semiconductor technologies.

	Type 1	Type 2	Type 3	Type 4
Voltage	< ~30 V	~30 V - 600 V	> 600 V	< 200 V
III-V vs. IV	GaAs	GaN	SiC	Si-based
Frequency	High (> 100 MHz)	Medium	Low*	Low (< 1 MHz)
Body Diode	No	No	Yes	Yes

*Compare with Si: lower Electron Mobility, but higher Electron Saturation Velocity

Switched-capacitor circuits have been known and used for long time. Historically, there were up and down periods for the development of switched-capacitor circuits. Many switched-capacitor circuits were rediscovered and revisited, including state-of-the-art advances. In 1873, J. C. Maxwell published the effects of regularly switched condenser (a former name of capacitor) [198]. Research on switched-capacitor converters already commenced since 1930s by Cockcroft and Walton [199]. In 1976, Dickson published switched-capacitor converters for memory applications on IC (Integrated Circuit) [200]. The topology is nowadays known as Dickson converter. It is noted that the Dickson converter has an equivalent circuit to the classical Cockcroft-Walton multiplier, where the capacitors are in parallel instead of in series. The drawback of this converter is that the capacitors have to withstand voltages that are developed along the diode chain. This may not be an issue for on-chip capacitors, because the MOM capacitors can be customized for different voltage ratings, as previously shown Table 2.4. The most important contribution of this work is that efficient multiplication of the switched-capacitor converter is achieved with relatively high on-chip parasitic capacitances. This facilitates the development of on-chip switched-capacitor converters, and the Dickson topology developed in 1970s is still commonly used for state-of-the-art research.

The examples of previously published switched-capacitor converters of 2:1 conversion ratio are summarized in Fig. 2.8. In fact, all the topologies are the same, but they are drawn differently. Similarly, several previously published switched-capacitor converters of 3:1 conversion ratio are shown in Fig. 2.9. These topologies are actually the same and just appear differently. The switched-capacitor converter topologies of 4:1 or 5:1 conversion ratio such as Dickson, Fibonacci, Series-Parallel, and Doubler are summarized in Fig. 2.10. It should be noted that all the above topologies when simplified at 2:1 conversion ratio are actually identical [213], [214].

Previous research on switched-capacitor DC-DC converters has focused on low-voltage and/or high-power applications, compared to the high-voltage and low-power requirements. State-of-the-art on-chip switched-capacitor DC-DC converters either have low input voltages (≤ 12 V) or have low output powers (≤ 2 W) [5]-[9]. To be simultaneously above both practical limits, switched-capacitor converters are commonly implemented with discrete components by industry [204] and academia [206]-[207]. Recent advances in switched-capacitor DC-DC power converters are up to a 200 V input voltage with output powers of 30-53 W [2],[215]. These state-of-the-art high-voltage switched-capacitor converters are summarized in Table 2.6.

Table 2.6 State-of-the-art high-voltage switched-capacitor converters.

	Case 1	Case 2
Year	2015	2015
Reference	[2]	[215]
Conversion ratio	2:1	8:1
Input Voltage	200 Vdc	200 Vdc
Output Power	30 W	53 W
Impedance level	≈ 1333 Ω	≈ 755 Ω
Normalized Impedance level	**1.8x**	**1x**

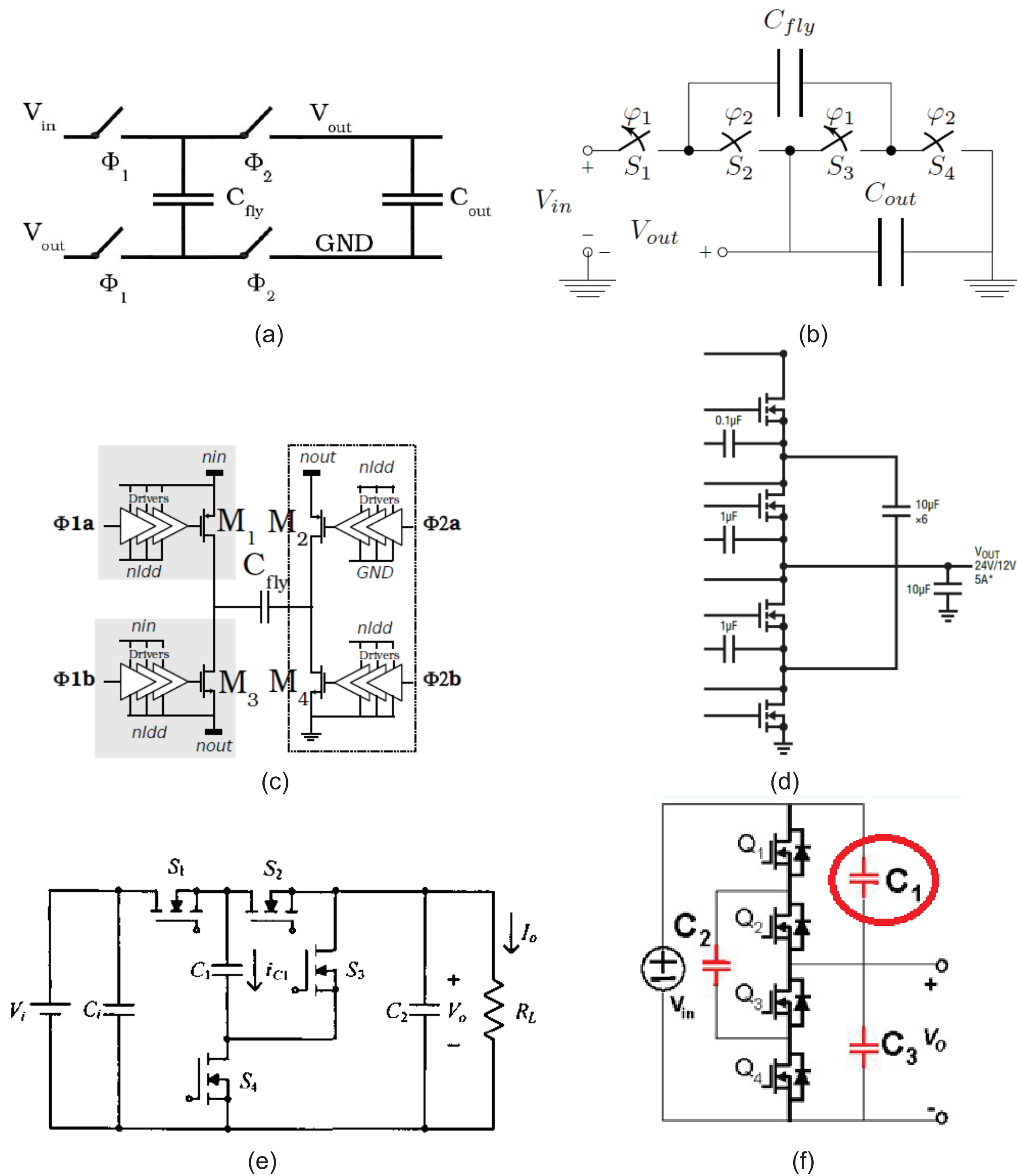


Fig 2.8 Switched-capacitor converters of 2:1 conversion ratio. All topologies are the same, but drawn differently. (a) 2011 [5], [201]. (b) 2016 [202]. (c) 2011 [203]. (d) 2017 [204]. (e) 2004 [205]. (f) 2006-2007 [206]-[209].

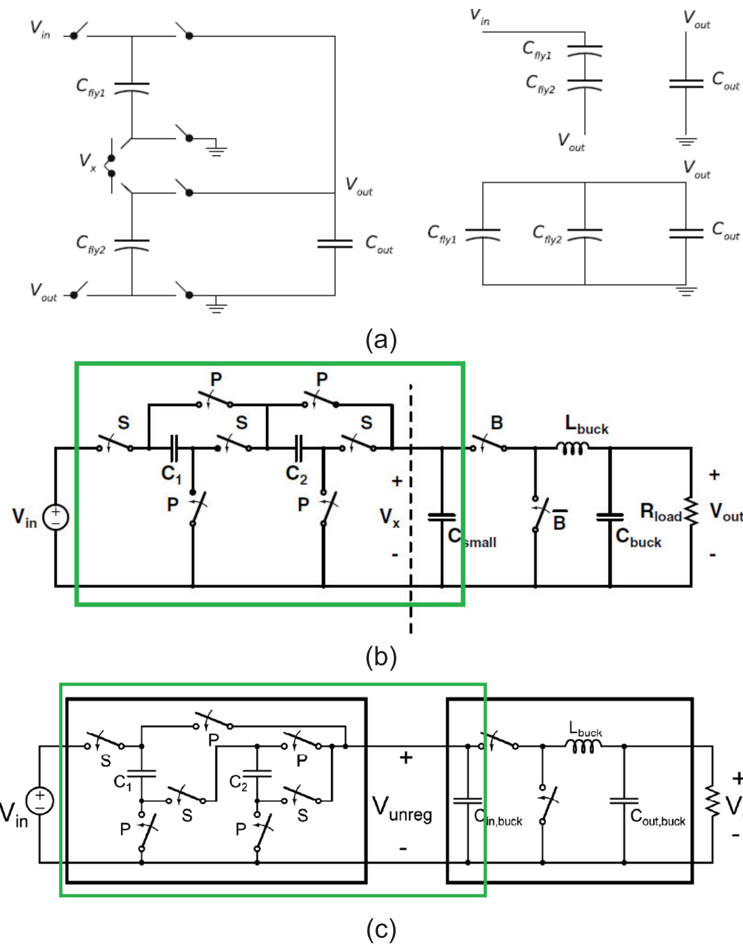


Fig. 2.9 Switched-capacitor converters of 3:1 conversion ratio. All topologies are the same, but drawn differently. (a) 2013 [106]. (b) 2008 [210]. (c) 2011-2012 [7], [211].

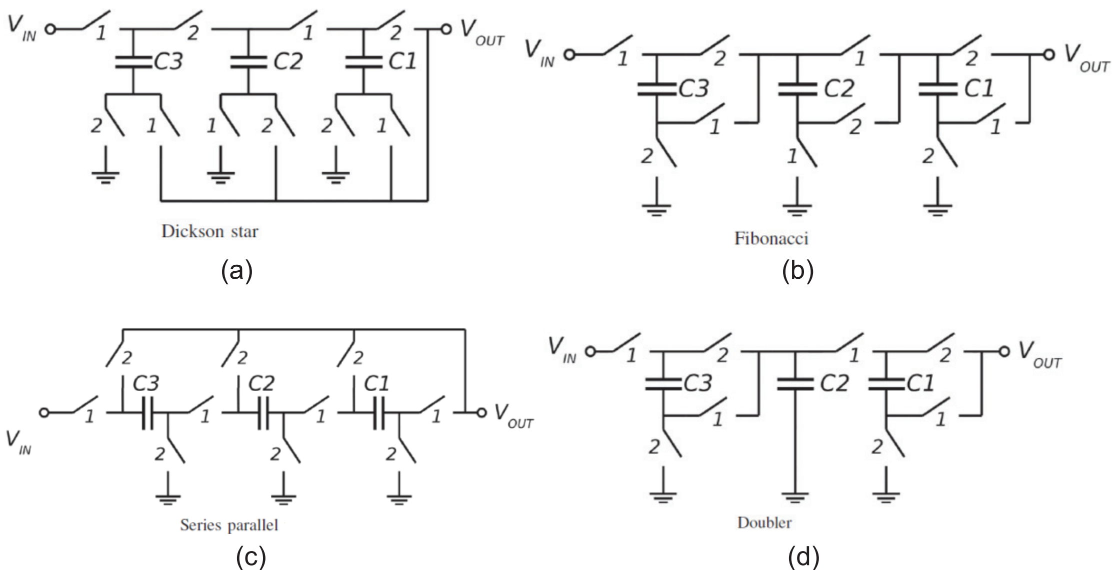


Fig. 2.10 Switched-capacitor converters of 4:1 or 5:1 conversion ratio. [212]. All topologies at 2:1 conversion ratio are actually identical [213], [214]. (a) Dickson 4:1. (b) Fibonacci 5:1. (c) Series-Parallel 4:1. (d) Doubler 4:1.

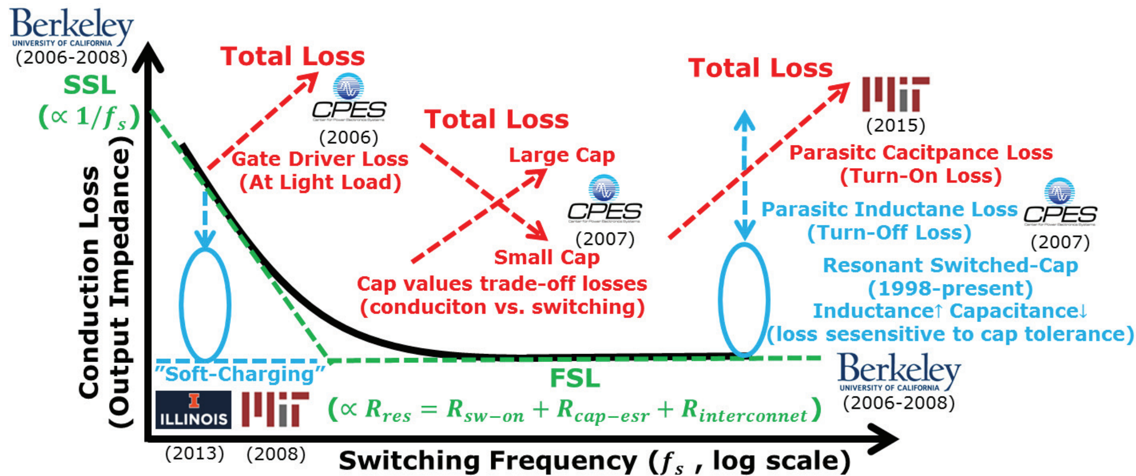


Fig. 2.11 Recent research work on loss analysis of switched-capacitor converters. Summary by the author.

The loss analyses of switched-capacitor converters of the previous research work [2], [7], [205]-[211], [213]-[215] are summarized in Fig. 2.11. The conventional loss modelling of switched-capacitor converters, i.e. the SSL (slow switching limit) and the FSL (fast switching limit) [213]-[214] focuses only on conduction loss. The analysis of solely conduction loss is not adequate for switched-capacitor converters at high-voltage levels [2], where the switching loss related to charging/discharging the output capacitances of the switches becomes significant, compared to the charge transfer loss related to charging/discharging the energy transfer capacitors. At low-power levels, other switching losses such as gate driver losses and losses caused by parasitic inductances also heavily affect the total loss of the switched-capacitor converters [206]-[209]. There are two research trends, i.e. the soft-charging technologies [7], [210], [211], [215] that attempt to reduce capacitor charging/discharging loss, and the resonant switched-capacitor technologies [16]-[22], [205], [216]-[229] that try to reduce switch turn-on/turn-off loss. There are similar mechanisms behind these two technologies, and further merging of the two may lead to advanced topologies. Nevertheless, at high-voltage low-power levels, the design challenges are not the same as low-voltage designs. High efficiency and high power density implementation remains a challenge. Switched-capacitor converters at high characteristic impedance levels (high-voltage and low-current) that are significantly higher than those of other state-of-the-art high-voltage switched-capacitor converters are to be demonstrated in this research wok for potential applications such as LED drivers that are compatible with AC mains.

3. Integrated Power MOSFETs

This chapter summarizes the first aspect of this research work regarding on-chip integrated high voltage power MOSFETs. In section 3.1, the intrinsic nonlinearities of the parasitic capacitances of high voltage power MOSFETs in a SOI process are analysed by a proposed modelling method. In section 3.2, the additional impacts of the parasitic capacitive coupling of on-chip interconnections and layout structures are analysed. In section 3.3, the nonlinearities of the gate charges and the related figure-of-merits (FOMs) are analysed. In section 3.4, the parasitic considerations of packages are qualitatively discussed. In section 3.5, the parasitic considerations of PCB layout are briefly summarized. This chapter focuses on the research on components level that includes device, layout, package, and PCB.

3.1 On-chip Nonlinear Parasitic Capacitance Modelling

In this section, a modelling method is presented to systematically analyze the nonlinear parasitic capacitances of power switches versus different bias voltages. The modelling method is originally proposed for integrated power MOSFETs in a Silicon-on-Insulator (SOI) process, but the principle is general and can be applied to other integrated circuit processes. The existing ways of characterizing the off-state capacitances can be extended by the proposed modelling method that covers all the related operation states: off-state, sub-threshold region, and on-state in the linear region.

High voltage power MOSFETs do not have the relatively simple structures as low voltage MOSFETs, e.g. those in general Complementary Metal-Oxide-Semiconductor (CMOS) processes. Despite that on-chip integrated lateral devices are researched in this work, most of the high voltage power MOSFETs are discrete and vertical devices. High voltage power MOSFETs normally have cellular structures that are composed of parallel connected unit cells [109], [110]. The purpose of the parallelization is to reduce the on-state resistance, not only in nominal operation conditions, but also over high temperatures and low overdriving conditions. The parasitic capacitive coupling effects of the on-chip interconnections and layout structure impacts are discussed in the next section. In addition, the integration of high voltage power MOSFETs is favourable in a SOI process. The name Silicon-on-Insulator does not only mean dielectric isolation in the vertical direction, but also it consists of dielectric isolation in the horizontal direction. The isolation in the vertical direction is achieved with the buried oxide, and the isolation in the horizontal direction is achieved with the Deep Trench Isolation (DTI) and the Shallow Trench Isolation (STI). In this way, it is feasible to integrate high voltage power MOSFETs that operate at different voltage domains. For high voltage operations, the electric field should be properly distributed and the fringing electric field should also be properly terminated, thus handle wafer contacts (connecting different wells and the handle wafer) are needed through the buried oxide, namely a partial SOI process.

A high voltage power MOSFET is firstly designed in a 0.18 µm partial SOI process, and its nonlinear parasitic capacitances are analyzed. The power MOSFET is dielectrically isolated from other MOSFETs and circuits with a full three-dimensional isolation that is form with the combination of the SOI wafer and the deep trench isolation, as previously discussed. It has electrical properties shown in Table 3.1.

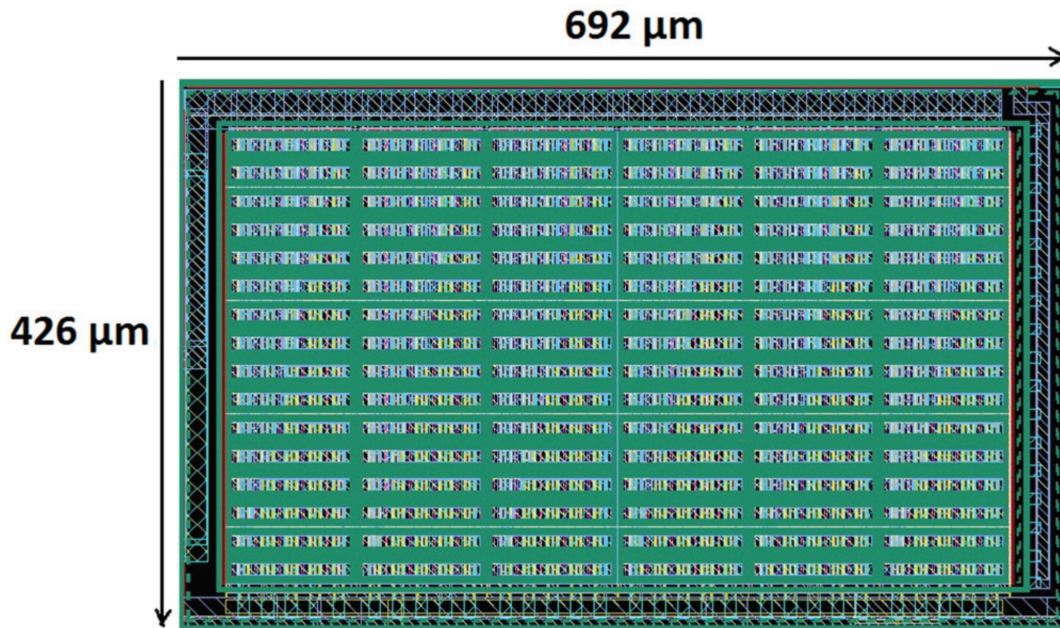


Fig. 3.1 A high voltage power MOSFET in a partial SOI process. Its nonlinear parasitic capacitances are analyzed by the proposed modelling method. [Appendix A.1]

Table 3.1 Electrical properties of the high voltage power MOSFET

Parameters	Values	Comments
Breakdown voltage (between drain and source)	> 110 V	Process [230]
Maximum operating voltage (between drain and source)	100 V	Process [230]
Maximum operating voltage (between gate and source)	5.5 V	Process [230]

The geometrical properties of the high voltage power MOSFET hare summarized in Table 3.2.

Table 3.2 Geometrical properties of the high voltage power MOSFET

Parameters	Values	Comments
Number of rows	16	Design of this work
Number of columns	6	Design of this work
Number of unit cells	96	Design of this work
Gate length of unit cells	0.5 µm	Design of this work
Gate finger width	10 µm	Design of this work
Number of fingers per unit cell	10	Design of this work
Equivalent gate width per unit cell	100 µm	Design of this work
Total length	692 µm	Design of this work
Total width	426 µm	Design of this work
Total die area*	0.2948 mm^2	Design of this work

*Including all unit cells and all deep trench isolation structures, except chip pads and electrostatic discharge (ESD) protection circuits

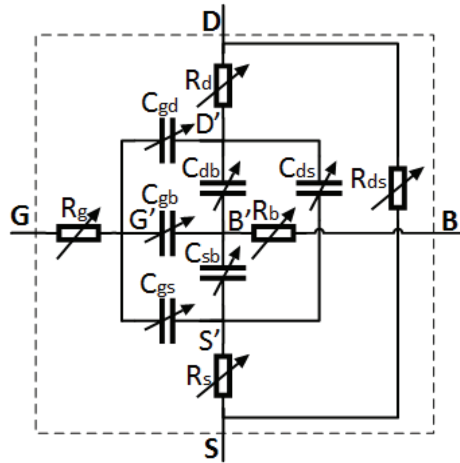


Fig. 3.2 Proposed small-signal model of power MOSFETs. It is applicable for off-state, sub-threshold region, and on-state in the linear region. [Appendix A.1]

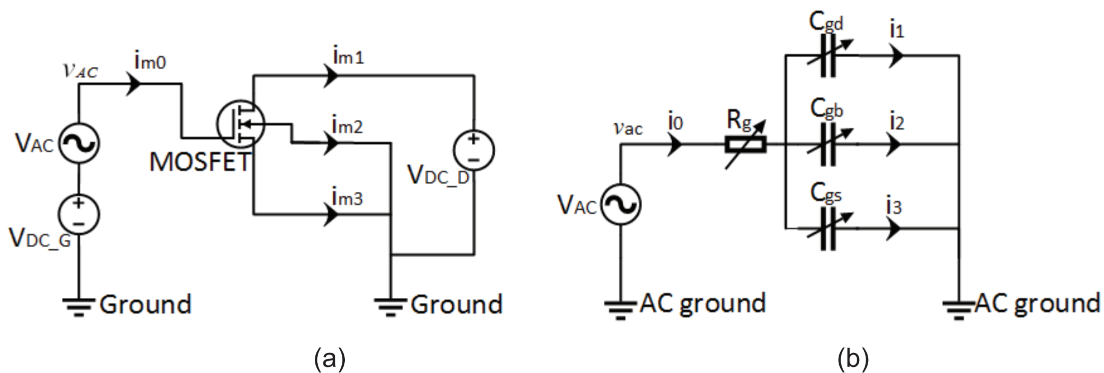
To model the nonlinear parasitic capacitances of the high voltage power MOSFETs, a small-signal modelling method is used and the proposed small-signal model of the power MOSFETs is shown in Fig. 3.2. Note that there is no transistor symbol inside the model, and this should be distinguished from other qualitative analyses where parasitic capacitances are drawn around transistors. There are 4 distinct characteristics of the proposed modelling method:

- The bulk terminal is modelled as a separate terminal. Conventionally, the bulk terminal is shorted to the source terminal, and there is no way to distinguish the gate-source capacitance and the gate-bulk capacitance. The only way to separate the capacitance contributions towards bulk and source is to model the bulk as a separate terminal.
- Rds is modelled as a nonlinear resistance, which depends on the gate-source voltage and the drain-source voltage. And it is included and affects the operation in all states, i.e. the off-state operation, the on-state operation, and the sub-threshold region (nonlinearly). As a comparison, conventional modelling normally includes the resistance only in off-states.
- All components in the model are nonlinear and dependent on DC bias voltages. This means that not only the capacitances but also the resistances are all nonlinear, e.g. the gate resistance may present nonlinear behavior [231], [232].
- Parasitic resistances are specifically included for the drain, source, and bulk terminals. In principle, these parasitic resistances always physically exist and contribute to the nonlinearities, though the resistance values may be small and sometimes negligible.

One of the key points to interpret the modelling of the power MOSFETs is to understand that the model is merely an equivalent circuit. The nonlinear capacitances in the model are not physical [128], [233] even though the model may resemble the physical structures. The real transistor characteristics are much more complex than any simplified model that is composed of lumped components. The parts of the nonlinearities of the real transistor characteristics that are not physically reflected to the limited number of the lumped components have to be incorporated into the simplified equivalent model. As a result, the resulting equivalent values of the lumped components in the model may appear more nonlinear than the corresponding physical characteristics of the part of the structure. The equivalent model is used to reveal and give insight into the electrical behavior of power MOSFETs. Attempting to establish a perfect match between the electrical model and the physical structures would lead to a misconception.

The analyses of the nonlinear parasitic capacitance using the proposed modelling method are classified into 3 categories:
1) Parasitic capacitances looking into the gate terminal
2) Parasitic capacitances looking into the drain terminal with the transistor in off-state
3) Parasitic capacitances looking into the drain terminal with the transistor in on-state in the linear region or in the sub-threshold region

After classifying which terminal of the transistor to look into and what state the transistor is in (off-state, sub-threshold region, or on-state in the linear region), the equivalent circuit model of the transistor can be further simplified when all terminals are biased at fixed DC voltages. As the proposed modelling uses a small-signal method, the characterization of the nonlinearities of the equivalent components uses AC signals, which are superposed on specific DC operating points, as test inputs.



(a) (b)

Fig. 3.3 Evaluation of parasitic capacitances looking into the gate terminal. It is applicable for off-state, sub-threshold region, and on-state in the linear region. [Appendix A.1]
(a) Simulation setup. (b) Equivalent circuit.

To evaluate the parasitic capacitances looking into the gate terminal of the power MOSFET, the simulation of this work is shown in Fig. 3.3 (a). The simulations are based on the high-level models from the process foundry [230]. Under this specific condition, in the small-signal equivalent model, it can be reasonably assumed that the internal nodes D', S', and B' are equivalent AC ground. R_d, R_s, and R_b in reality have very small resistance values, which facilitates this assumption. It is also valid for physical measurements, where the external parasitic resistances and inductances of packages and interconnections do not cause practical influence on the extraction results. Under the conditions that the nodes D', S', and B' are equivalent AC ground, C_{db}, C_{sb}, C_{ds}, and R_{ds} can be removed from the equivalent model. The resulting equivalent circuit is shown in Fig. 3.3 (b), where each component has nonlinear values depending on the bias conditions, and each current (and voltage) has complex values with phase components included. The equivalent nonlinear parasitic capacitances looking into the gate terminal can then be determined [Appendix A.1]. For evaluating the nonlinear parasitic capacitances, an input frequency f_s of 1 MHz is used, and it is the same frequency as used in industrial datasheets [98], [99]. The simulation results of the equivalent nonlinear parasitic capacitances looking into the gate terminal are shown in Fig. 3.4 for $V_D = V_B = V_S = 0$ V. Note that the output capacitance C_{oss}, the drain-bulk capacitance C_{db}, and the drain-source capacitance C_{ds} are fundamentally capacitances looking into the drain terminal instead, and are discussed later in this section and further in the section 3.3.

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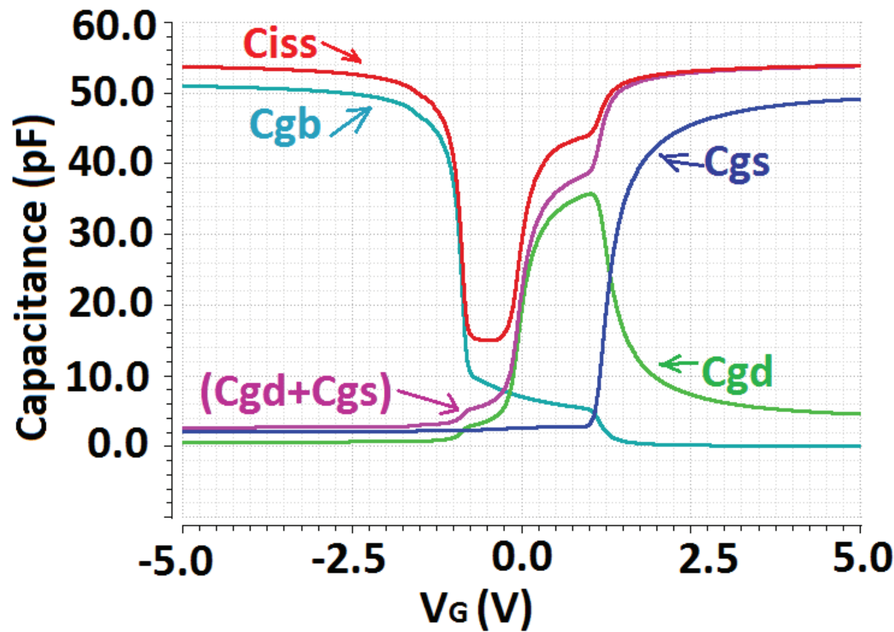


Fig. 3.4 Nonlinear parasitic capacitances looking into the gate terminal. The bias conditions are $V_D = V_B = V_S = 0$ V. [Appendix A.1]

The equivalent input capacitance C_{iss} is dominated by different sub-capacitances in 3 regions:

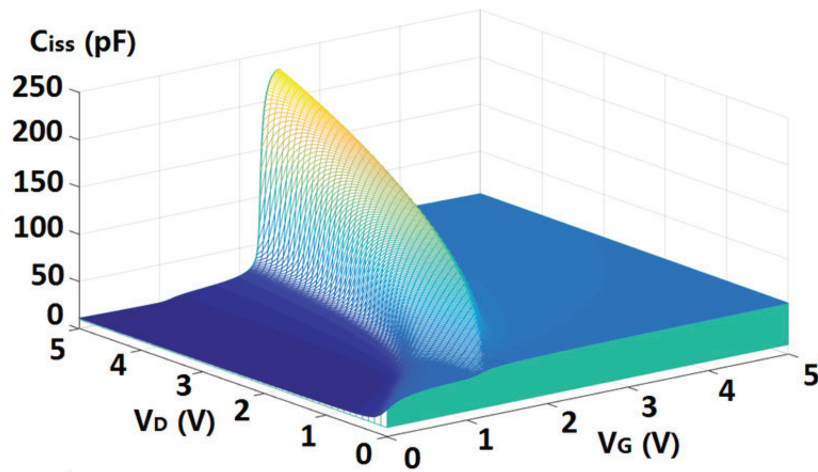
- Dominated by the gate-bulk capacitance C_{gb}, when the fixed DC bias voltage

at the gate terminal VG is negative

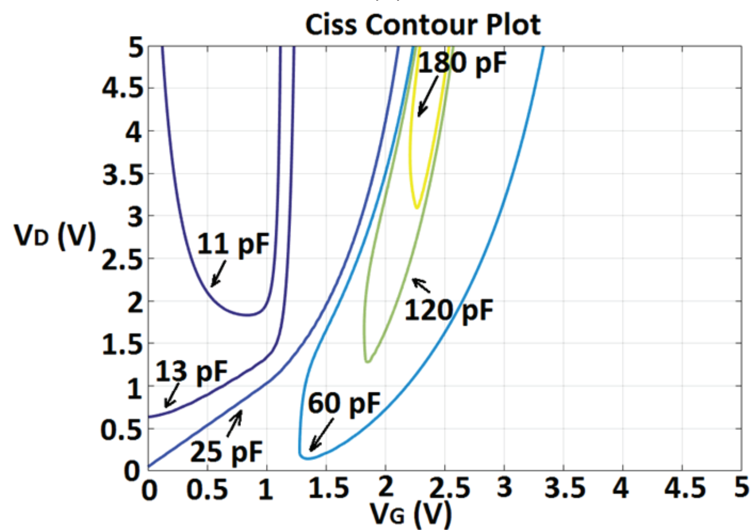
- Dominated by the gate-drain capacitance C_{gd}, when V_G is near 0 V, i.e. the gate and source bias voltages are close to each other
- Dominated by the gate-source capacitance C_{gs}, when V_G is larger than the threshold voltage (Vth $\approx$ 1.1 V for the power MOSFET)

The input capacitance C_{iss}, when the bulk and source terminals are shorted, is not only formed by the gate-source capacitance C_{gs} (and the gate-drain capacitance C_{gd}). It leads to errors and misleading results at negative gate voltages, if the gate-bulk capacitance C_{gb} is ignored. In the case of Fig. 3.4, at V_G = - 5 V, the input capacitance C_{iss} is about 54 pF, whereas the sum of the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} is about 3 pF. It leads to more than 90 % errors if the gate-bulk capacitance C_{gb} is ignored in this case. It also shows that the parasitic capacitances towards the bulk can dominate over the parasitic capacitances towards the source in this lateral device.

The nonlinearities of the equivalent input capacitance C_{iss}, looking into the gate terminal, are shown in Fig. 3.5. It is the combinations of the gate voltage (0-5 V) and the drain voltage (0-5 V). Therefore, the results cover the off-state, the sub-threshold region, and the on-state in the linear region. The input capacitance C_{iss} at the conditions of V_G = 0 V and V_D = 0-5 V monotonically decreases from 28.83 pF to 11.25 pF, and C_{iss} at the conditions of V_G = 5 V and V_D = 0-5 V monotonically increases from 53.82 pF to 55.16 pF. It shows that the nonlinear input capacitance C_{iss} can either increase or decrease at different drain or gate voltages. Therefore, extrapolating input capacitance C_{iss} values based solely on information at a specific drain or gate voltage would be inappropriate. This is one of contributions of this research.



(a)

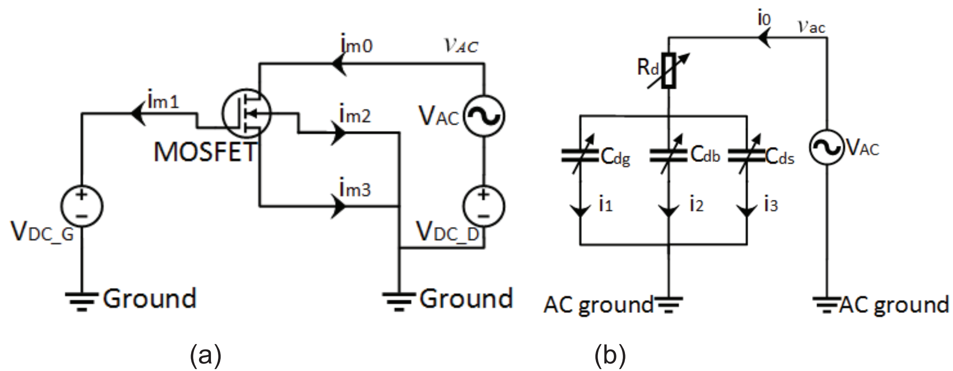


(b)

Fig. 3.5 Nonlinearities of input capacitance C_{iss}. It is applicable for off-state, sub-threshold region, and on-state in the linear region. The bias conditions are VB = VS = 0 V. [Appendix A.1] (a) 3D plot. (b) Contour plot.

The situation is different when looking into the drain terminal, compared to looking into the gate terminal. This is because there is a direct resistive path of the nonlinear resistance R_{ds}, from the drain terminal to the AC ground. When looking into the drain terminal and the transistor is in off-state and the gate voltage is much lower than the threshold voltage, the equivalent R_{ds} is in the MΩ to GΩ range, and thus R_{ds} can be removed from the equivalent model.

To evaluate the parasitic capacitances looking into the drain terminal of the power MOSFET, the simulation test bench is shown in Fig. 3.6 (a). Under this specific condition, in the small-signal equivalent model, the internal nodes G', B', and S' can be reasonably assumed to be equivalent AC ground. Under these conditions, C_{gb}, C_{gs}, and C_{sb} can be removed from the equivalent model. The resulting small-signal equivalent circuit is shown in Fig. 3.6 (b). The equivalent nonlinear parasitic capacitances looking into the drain terminal in off-state can then be determined [Appendix A.1].



(a) (b)

Fig. 3.6 Evaluation of parasitic capacitances looking into the drain terminal. It is applicable for off-state. [Appendix A.1]
(a) Simulation setup. (b) Equivalent circuit.

The simulation results of the equivalent nonlinear parasitic capacitances looking into the drain terminal in off-state are shown in Fig. 3.7 for $V_G = V_B = V_S = 0$ V. The equivalent out capacitance C_{oss} is dominated by the drain-bulk capacitance C_{db}. The drain-source capacitance C_{ds} shows very small values, because in the lateral device in the partial SOI process, the drain diffusion and the source diffusion are separated far apart, and the channel for majority carriers of the transistor is biased in off-state. Note that the situation is different from conventional vertical devices, which have a direct and large junction between the body and the epitaxial layer [134].

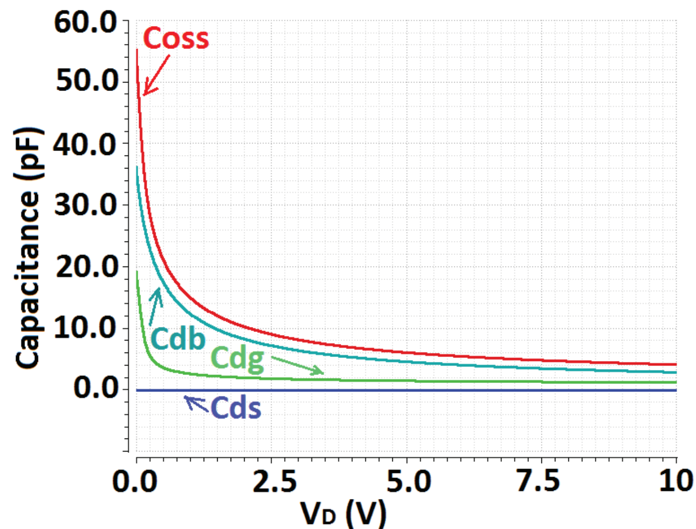


Fig. 3.7 Nonlinear parasitic capacitances looking into the drain terminal in off-state. The bias conditions are $V_G = V_B = V_S = 0$ V. [Appendix A.1]

The nonlinearities of the equivalent out capacitance C_{oss}, looking into the drain terminal, are shown in Fig. 3.8. It is the combinations of the gate voltage (0-700 mV) and the drain voltage (0-5 V). In these voltage ranges, the transistor is in off-state and the gate voltage is much lower than the threshold voltage (Vth ≈ 1.1 V for the power MOSFET). The output capacitance C_{oss} at the conditions of $V_D = 0$ V and $V_G = 0$-700 mV monotonically increases from 55.10 pF to 70.54 pF, and C_{oss} at the conditions of $V_D = 5$ V and $V_G = 0$-700 mV monotonically increases from

6.072 pF to 6.140 pF. Similarly, extrapolating output capacitance C_{iss} values solely based on information at a specific voltage would be inappropriate. Note that R_g is removed from the simplified equivalent circuit in Fig. 3.6 (b) to determine the nonlinear parasitic capacitances when looking into the drain terminal. This corresponds to the common way of the output capacitance C_{oss} measurement [234], where the gate and source terminals are firstly shorted, and then the equivalent capacitances are measured or calculated between the drain terminal and the AC ground [231], [234]. This is equivalent to omitting R_g from the measurement circuit.

The equivalent resistance R_d is nonlinear. This is expected and as previously explained, the nonlinearities of the real transistor characteristics have to be absorbed by the limited number of the lumped components in the equivalent model, which is fundamentally not the same as physical structures. The nonlinearities of the equivalent resistance R_d when looking into the drain terminal are shown in Fig. 3.9. The external series resistance at the gate contributes to the nonlinearities of the equivalent resistance R_d. This is because R_d is the only resistive component in the simplified equivalent circuit in Fig. 3.6 (b) and it has to model the effects resulting from external series resistance at the gate.

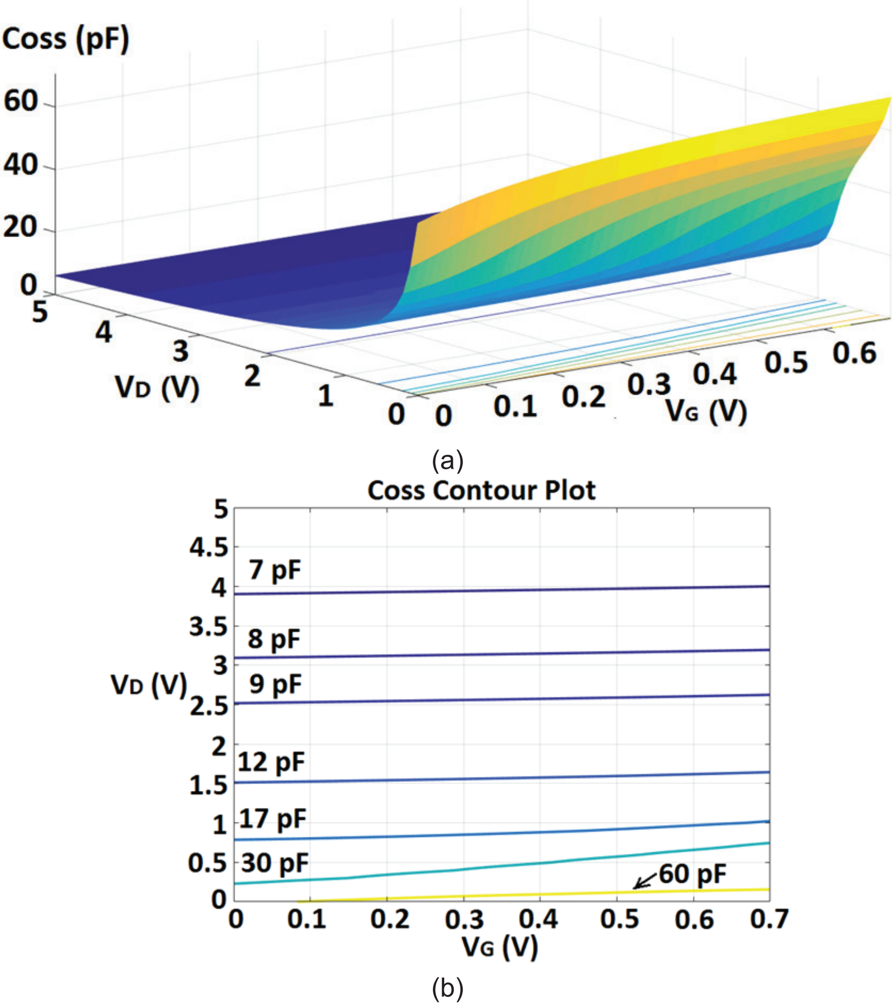


Fig. 3.8 Nonlinearities of output capacitance C_{oss} It is applicable for off-state and the gate voltage is much lower than the threshold voltage. The bias conditions are $V_B = V_S = 0$ V. [Appendix A.1] (a) 3D plot. (b) Contour plot.

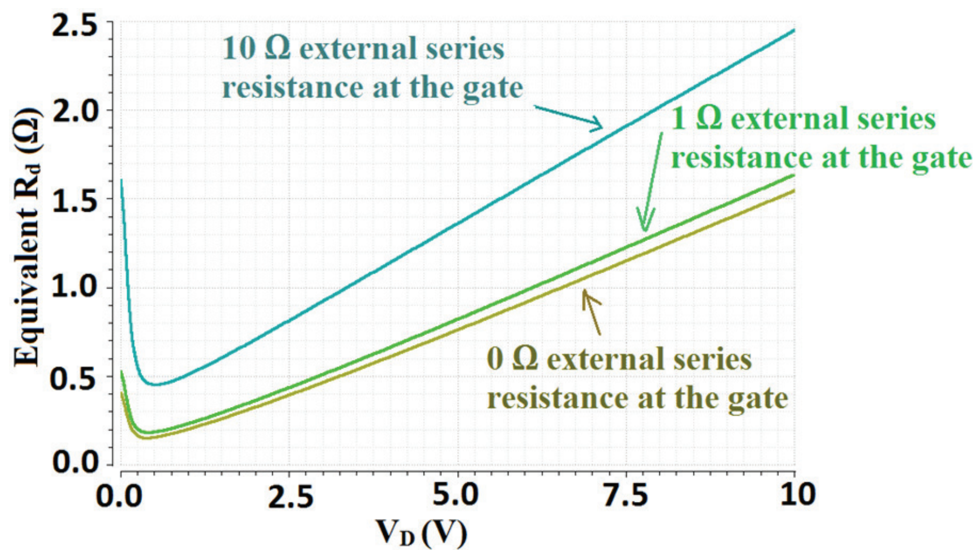


Fig. 3.9 Equivalent resistance R_d when looking into the drain terminal with different external series resistance at the gate. The bias conditions are $V_G = V_B = V_S = 0$ V. [Appendix A.1]

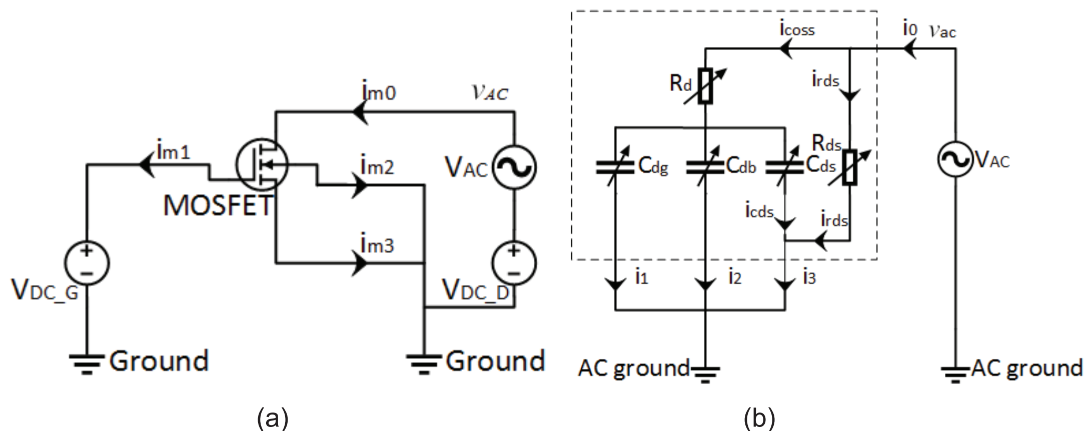


Fig. 3.10 Evaluation of parasitic capacitances looking into the drain terminal.
It is applicable for on-state in the linear region or the sub-threshold region. [Appendix A.1]
(a) Simulation setup. (b) Equivalent circuit.

As previously shown, to evaluate the parasitic capacitances looking into the drain terminal of the power MOSFET, the simulation test bench is shown in Fig. 3.10 (a), which is the same as Fig. 3.6 (a). However, the equivalent circuit is not the same as before. In the sub-threshold region, the equivalent resistance R_{ds} is in the KΩ range or even lower, and its impedance level becomes comparable to the impedance level of the parasitic capacitances, thus R_{ds} cannot be neglected anymore in this case. The equivalent circuit is shown in Fig. 3.10 (b), and the dotted box denotes the boundary of the transistor. The nonlinear parasitic capacitances can then be estimated [Appendix A.1].

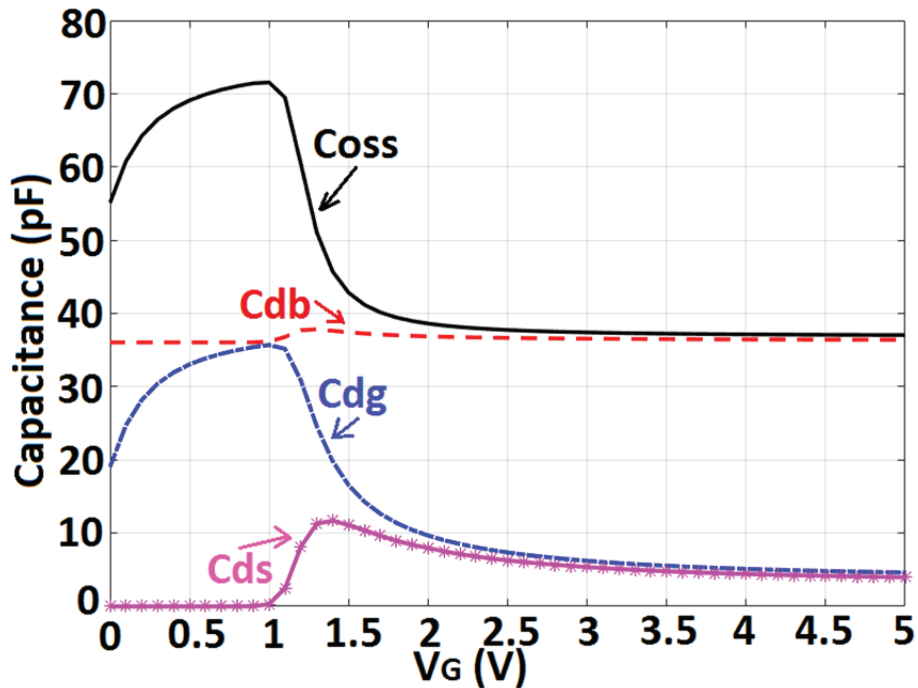


Fig. 3.11 Nonlinear parasitic capacitances looking into the drain terminal in on-state in the linear region or in the sub-threshold region, as well as off-state.
The bias conditions are V_D = 1 µV, V_B = V_S = 0 V. [Appendix A.1]

The simulation results of the equivalent nonlinear parasitic capacitances looking into the drain terminal are shown in Fig. 3.11 when the transistor is in on-state in the linear region or in the sub-threshold region, as well as off-state. The drain voltage V_D has a DC bias value of 1 µV. This is because the nonlinear resistance R_{ds} must be known at each bias point used for the AC simulations. And the drain voltage V_D is kept small to avoid the nonlinear effects at high drain-source voltages. The nonlinearities of parasitic capacitances are not analyzed at high drain-source voltages while the transistor is switched on, because power switches do not normally operate in the saturation region in on-state which causes large losses. The output capacitance C_{oss} in off-state and in the sub-threshold region is dominated by C_{db} and C_{dg}, and C_{oss} in on-state in the linear region is dominated by C_{db}.

The switching behavior and the temperature behavior of the proposed model may be further investigated in one of the following ways.

- Calculate a linear formula or do a two-dimensional numerical simulation of the cell structure [235].
- Use a piecewise linear model or solve a derivatives matrix [236].
- Apply semiconductor physics in different device regions, e.g. accumulation, depletion, weak inversion, moderate inversion, strong inversion saturation, and strong inversion non-saturation [237].

3.2 On-chip Layout Capacitance Coupling and Structure Impacts

The previous section describes the nonlinear parasitic capacitances of the integrated high voltage power MOSFETs, which are the intrinsic properties of the power semiconductors. However, the overall switching performances of the integrated high voltage power MOSFETs are also heavily influenced by the parasitic capacitive coupling of on-chip metal wires, due to the fact that power MOSFETs have prevailing interconnection matrices. The layout capacitance coupling of on-chip metal wires originate from both the side-by-side coupling of metal wires in the same metal layer and the layer-to-layer coupling of metal wires in different metal layers. The mechanism of the side-by-side coupling is generally known, and this research contributes with the systemic analysis of the layer-to-layer coupling and the comparison between the side-by-side coupling and the layer-to-layer coupling.

This section firstly presents a modelling method of parasitic mutual coupling of two on-chip metal wires, and this is to systematically analyze the parasitic capacitances directly coupled between them. It is to be shown that, from 3D field solver analysis, the layer-to-layer coupling can dominate over the side-by-side coupling, and from 2D extraction analysis, the side-by-side coupling dominated structure may perform better than the layer-to-layer coupling dominated structure.

At schematic levels, wires are ideal electrical paths that connect nodes of the same net name. At layout levels, wires in integrated circuit layouts are normally made by metal, and the distances between the on-chip metal wires are generally in the μm range, which results in unavoidable mutual capacitive coupling. The modelling of parasitic mutual coupling of two closely placed on-chip metal wires is shown in Fig. 3.12.

All the components in the modelling circuit result from the parasitic effects of the layouts. The two metal wires are named with wire A and wire B. Wire A connects the node A1 and A2. Wire B connects the node B1 and node B2. The resistance R_A and the resistance R_B are the intrinsic parasitic resistances of wire A and wire B, respectively. The four access resistances R_{access_A1}, R_{access_A2}, R_{access_B1}, and R_{access_B2} represent the parasitic resistances that originate from the physical access pins, whose resistance values are normally less than 1 mΩ. The four substrate capacitances C_{sub_A1}, C_{sub_A2}, C_{sub_B1}. and C_{sub_B2} are the intrinsic parasitic capacitances to the substrate, whose capacitance values increase with the length or width. For the same dimensions, a metal wire located in a lower layer such as Metal1 (abbreviated as M1) presents a higher intrinsic parasitic capacitance to the substrate, than the case if the same metal wire is located in an upper layer. The modelling circuit is symmetrical. The capacitances of interest here are the two direct coupling capacitances $C_{coupling_A1_B1}$ and $C_{coupling_A2_B2}$. Other mutual coupling capacitances $C_{self_A1_A2}$, $C_{self_B1_B2}$, $C_{cross_A1_B2}$, and $C_{cross_B1_A2}$ represent the fact that when the metal wires are very wide but short in length, there could be mutual coupling between the two nodes of the same wire and there could be cross coupling between non-adjacent nodes that cannot be lumped into the capacitances $C_{coupling_A1_B1}$ and $C_{coupling_A2_B2}$. These capacitance values are extracted as well and generally much smaller than the capacitances $C_{coupling_A1_B1}$ and $C_{coupling_A2_B2}$. The capacitances $C_{coupling_A1_B1}$ and $C_{coupling_A2_B2}$ are not lumped together due to the symmetrical structure of the modelling circuit and there are parasitic resistances between them. The average value of the two capacitances $C_{coupling_A1_B1}$ and $C_{coupling_A2_B2}$ is used to represent the average coupling effect.

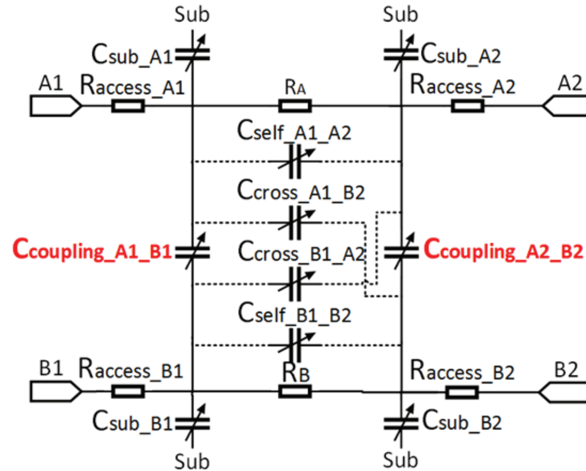


Fig. 3.12 Modelling of two closely placed on-chip metal wires. It is applicable for either side-by-side coupling or layer-to-layer coupling. All components are parasitic. [Appendix A.2]

The layout capacitive coupling between the two metal wires is simulated with the actual layouts using a 2D extraction tool (Calibre xRC) and a 3D field solver (Calibre xACT 3D with high accuracy mode). The simulation results of the side-by-side capacitive coupling are shown on the left side of the Fig. 3.13. It is assumed that there is no power or ground plane above the metal wires, and there is global substrate below the metal wire, such that the simulated results are reproducible and not case-dependent. The dimensions of the side-by-side coupling case are defined in Fig. 3.13 (a). The definitions of the dimensions are summarized in Table 3.3.

Table 3.3 Definitions of dimensions of layout capacitive coupling

Symbol	Definition	Reference value (if not otherwise specified)	Comments
T	metal thickness M_1-M_4 metal thickness M_{top}	555 nm (Public [230]) 975 nm (Public [230])	Process [230] Process [230]
S	spacing distance	0.5 µm	Design of this work
W	common metal width	0.5 µm	Design of this work
L	common metal length	5 µm	Design of this work
D	dielectric thickness	Confidential	Vary between metal layers for the same process
O	offset distance in the vertical direction	0 µm	Design of this work
If the metal wire is located in M3 layer in the used process, then the resulting parasitic resistance is approximately 1 Ω.			

The top metal layer M_{top} of 975 nm [230] is thicker than the other lower metal layers M_1-M_4 of 555 nm [230]. This is to reduce the metal sheet resistance in the top metal layer, but this leads to increased side-by-side capacitive coupling, which is shown in Fig. 3.13 (b). The side-by-side capacitive coupling decreases with increased spacing S between the two metal wires, and it is shown in Fig. 3.13 (c). For side-by-side metal wires with a voltage difference of 100 V, the spacing S in excess of 1 µm is generally recommended for all metal layers. The side-by-side capacitive coupling increases with the width W, while kee/ping the same spacing S, is shown in Fig. 3.13 (d). The 2D extraction results are accurate for small W values, bus as W increases, the 2D extraction results become underestimated compared to the results of the 3D field solver.

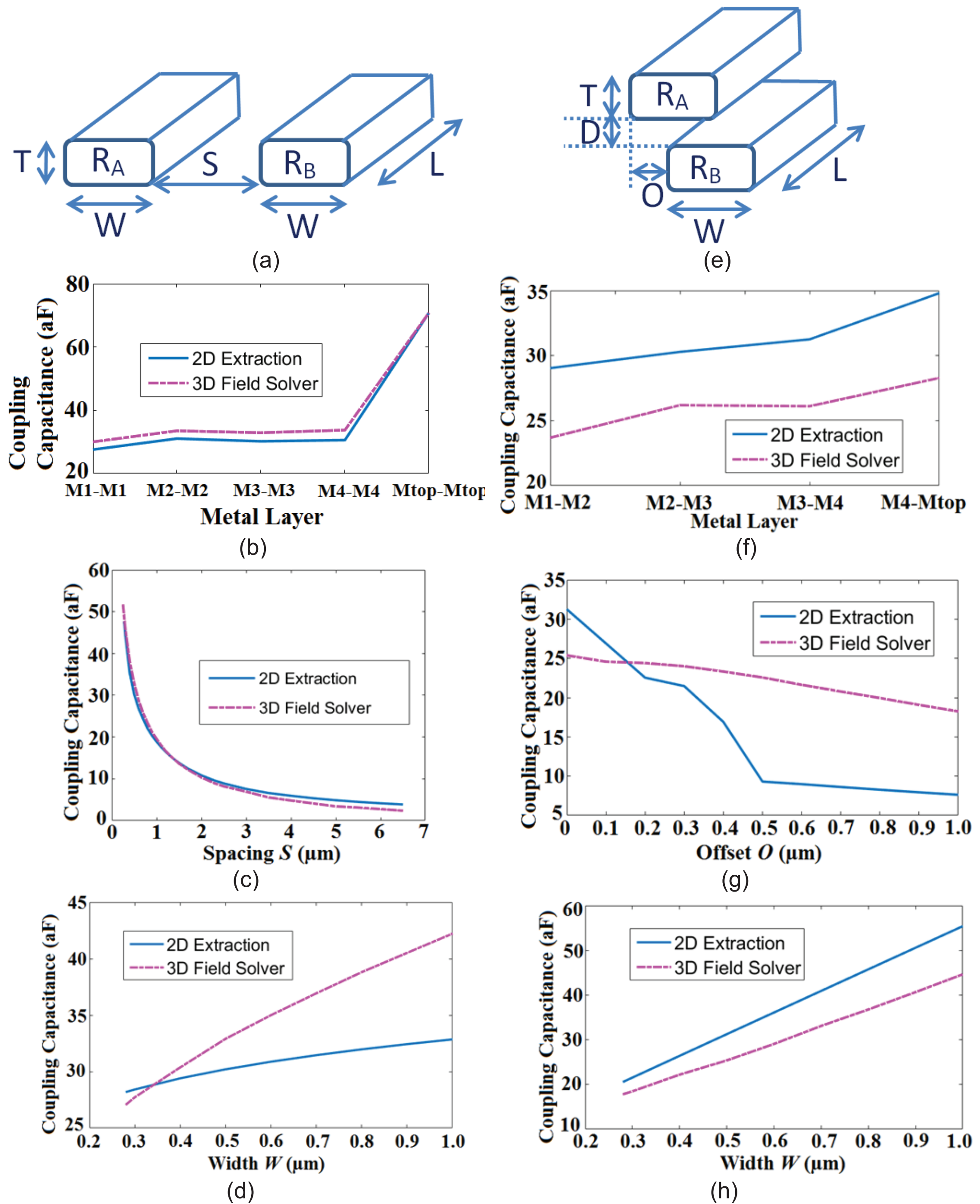


Fig. 3.13 Comparison of side-by-side capacitive coupling and layer-to-layer capacitive coupling. Note that the default dimensions are defined in Table 3.3. [Appendix A.2]
(a) Side-by-side dimensions. (b) Side-by-side coupling versus metal layers. (c) Side-by-side coupling versus spacing S (M3-M3). (d) Side-by-side coupling versus width W (M3-M3). (e) Layer-to-layer dimensions. (f) Layer-to-layer coupling versus metal layers (O = 0). (g) Layer-to-layer coupling versus offset O (M3-M4). (h) Layer-to-layer coupling versus width W (M3-M4).

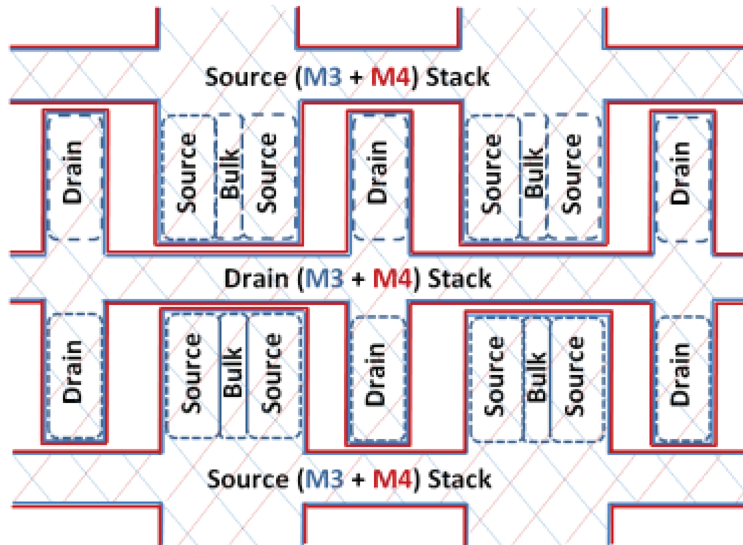
Note that the default dimensions used in Fig. 3.13 are previously defined in Table 3.3. The dimensions are relatively small in the µm range, and the real layout structures are much more complex and are in the mm range. The capacitive coupling effects in Fig 3.13 are only used to show the basic principles and the capacitive coupling effects of the real layout structures are analysed later in this section.

The two metal wires that are located in separate layers can still present capacitive coupling to each other, which is called layer-to-layer capacitive coupling in this work, because the electric field can penetrate the dielectric between the metal layers. The dimensions of the layer-to-layer capacitive coupling case are defined in Fig. 3.13 (e). The simulation results show that the effects of the layer-to-layer capacitive coupling are approximately the same for different metal layers. If the two metal wires have an offset O of zero, it means that the two wires are exactly overlapping each other in the vertical direction, and the layer-to-layer capacitive coupling is strongest in this case. As offset O increases, the layer-to-layer capacitive coupling gradually decreases, and it is shown in Fig. 3.13 (g). The layer-to-layer capacitive coupling becomes stronger as the common width W increases, and this is shown in Fig. 3.13 (h). The 2D extraction results are accurate for small offset O values, and begin to converge with the results of 3D field solver after the two metal wires are moved apart in the vertical direction. The 3D field solver is a more accurate and cost-effective way to investigate the layout capacitive coupling effects. From the 3D field solver results, it shows that the layer-to-layer capacitive coupling is in the same order or even higher than the side-by-side capacitive coupling, when the metal wires and the dielectric have the comparable dimensions. This is one of the contributions of this research work.

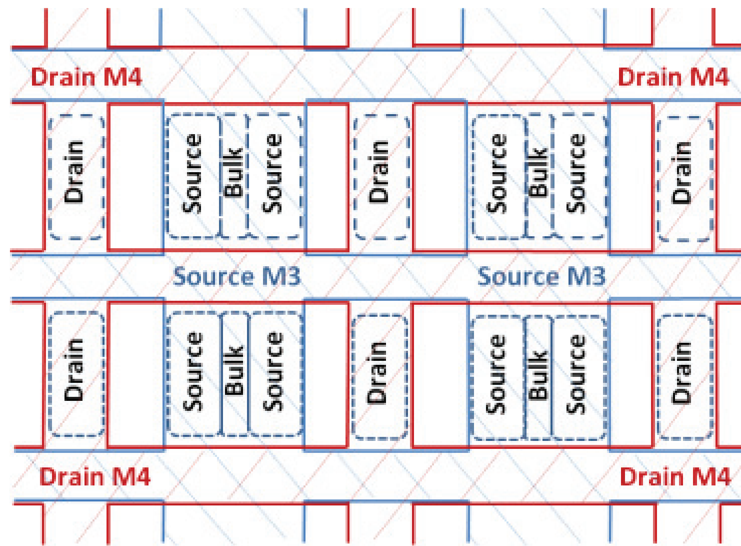
For integrated high voltage (≥ 100 V) power MOSFETs, it is more difficult to achieve a highly compact layout than low-voltage low-power MOSFETs. For high voltage power MOSFETs, there is uniformly distributed voltage potential on the side of the drain diffusion, and the corresponding isolation structures on the drain side can thus be overlapped. However, there is no uniform potential along the side of the device from the drain diffusion to the source diffusion, where the distributed electric field needs to be properly terminated. Therefore, the corresponding isolation structures surrounding these sides cannot be overlapped, and this result in a relatively lower device density of high voltage power MOSFETs, compared to low-voltage low-power MOSFETs.

Four layout structures are proposed for high voltage power MOSFETs and shown in Fig. 3.14. Only the main principles are demonstrated, and the real implementation the layout structures is limited by various DRC rules.

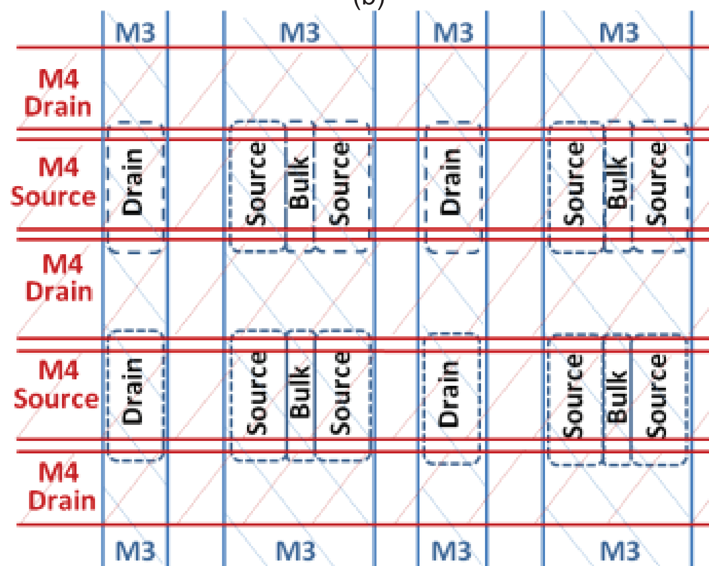
- In Fig. 3.14 (a), the drain/source connections are lateral metal stacks of two adjacent layers (M_3 and M_4), and the capacitive coupling is mainly dominated by the side-by-side coupling mechanism.
- In Fig. 3.14 (b), the drain/source connections are laterally routed in different metal layers (M3 and M4), and the capacitive coupling is mainly dominated by the layer-to-layer coupling mechanism.
- In Fig. 3.14 (c), the drain/source connections are vertically routed and have the perpendicular mesh structure, which can be viewed as a trade-off between the parasitic resistances and the parasitic capacitances. The parasitic effects depend on the specific geometrical dimensions.
- In Fig. 3.14 (d), the drain/source connections are vertically routed, in the same way as Fig. 3.14 (c). The bulk is constructed as a separate terminal that is not shorted to the source.



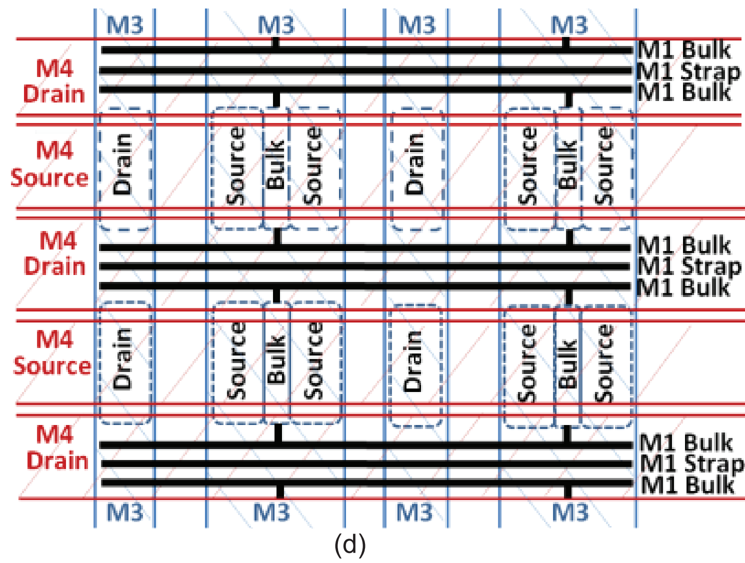
(a)



(b)



(c)



(d)

Fig. 3.14 Proposed layout structures for integrated high voltage power MOSFETs. [Appendix A.2]

(a) Layout a: horizontal D/S connection, metal layers stack, mainly side-by-side coupling.
(b) Layout b: horizontal D/S connection, in separate metal layers, mainly layer-to-layer coupling.
(c) Layout c: vertical D/S connection, perpendicular mesh structure, coupling by geometries.
(d) Layout d: vertical D/S connection, the same as (c) but with the bulk as a separate terminal.

Table 3.4 Comparison of the four proposed layout structures [Appendix A.2]

R/C	**Top chip-level (including chip-pads and ESD protections)**					
	Schematic *a* & *b*	**Post-Layout *a***	**Post-Layout *b***	**Schematic *c* & *d***	**Post-Layout *c***	**Post-Layout *d***
Parasitic	No	2D Extract	2D Extract	No	2D Extract	2D Extract
$R_{ds(on)}$ (Ω)[a]	1.542	2.071	2.250	3.085	3.354	3.295
$C_{g\text{-}sb}$ (pF)[b]	21.3	46.9	49.5	11.5	25.1	26.7
C_{gd} (pF)[b]	38.1	41.4	39.3	19.1	20.6	20.6
C_{iss} (pF)[b]	59.4	92.7	93.2	30.6	48.0	48.9
$C_{d\text{-}sb}$ (pF)[c]	72.1	88.4	85.7	36.0	47.6	48.0
C_{dg} (pF)[c]	38.1	41.4	39.3	19.1	20.6	20.6
C_{oss} (pF)[c]	110.2	132.1	127.6	55.1	69.5	69.8
$R_{ds(on)} \cdot C_{iss}$ (ps)	91.6	192.0	209.7	94.4	161.0	161.1
$R_{ds(on)} \cdot C_{oss}$ (ps)	169.9	273.6	287.1	170.0	233.1	230.0

[a] $V_{G\text{-}SB}$ = 5 V, V_{DS} = 0.1 V, T = 27 C, typical process corner.

[b] Test signals into the gate terminal, $V_G = V_D = V_B = V_S = 0$ V, T = 27 C, typical process corner.

[c] Test signals into the drain terminal, $V_G = V_D = V_B = V_S = 0$ V, T = 27 C, typical process corner.

The comparison of the four proposed layout structures is summarized in Table 3.4. The high voltage power MOSFETs are implemented in a 0.18 μm partial SOI process, which is the same process used in the previous section. The parasitic resistances and parasitic capacitances of the top chip-level post-layout, including the chip pads and the electrostatic discharge (ESD) protection circuits, are extracted using a 2D extraction tool (Calibre xRC). This is because though 3D field solvers are more accurate, they are generally not applicable to complicated layout networks at the top chip-level. 2D extractions are commonly used in industry, and the extracted results are still meaningful for comparison between layout structures. The modeling of the nonlinear parasitic parameters of the high voltage power MOSFETs is described in the previous section and in [Appendix A.1]. A testing frequency of 1 MHz is used and it is the same as the industrial measurement frequency [98], [99]. For each of the four layout structures, the ESD protection circuits add extra nonlinear voltage-dependent parasitic capacitances of 1.3-1.8 pF between the gate terminal and the source terminal.

The main results of the top chip-level post-layout extractions are summarized as follows:

- All post-layout extracted parameters are much worse than the parameters at the schematic level. It means that the overall performances of the high voltage power MOSFETs are heavily impacted or even dominated by the parasitic parameters of the on-chip interconnections, compared to the intrinsic transistor parasitic parameters.

- If $R_{ds(on)} \cdot C_{iss}$ and $R_{ds(on)} \cdot C_{oss}$ are used as indicators, the side-by-side coupling dominated layout a is better than the layer-to-layer coupling dominated layout b, by 9.2% and 4.9%, respectively. $C_{d\text{-}sb}$ of layout b is lower than that of layout a, but $C_{g\text{-}sb}$ of layout b is higher than that of layout a. This is because more metal is used for the source network in M3 layer for layout b, compared to layout a, thus there is more layer-to-layer capacitive coupling between the M_2 layer and the M_3 layer. In addition, the parasitic resistance of layout b is higher than that of layout a.

- Layout c and layout d may be used for high frequency power converters where switching losses dominate. Note that soft-switching converters ideally eliminate the overlap and capacitive discharge switching losses, but gating losses (including sinusoidal gate drive and trapezoidal gate drive) and off-state circulating current losses still exist as frequency-dependent losses and depend on input capacitances and output capacitances, respectively. The low capacitances are one concern. Another concern is that, as the size of the transistor increases, the on-resistance is ideally to be inversely scaling with the size of the transistor. However, in reality, the part of the on-resistance that is contributed by the on-chip interconnections becomes larger, rather than inversely scaling with the size of the transistor. This results in a trade-off between R and C, but the trade-off is not simply with a RC constant. The optimal trade-off between R and C depends on the specific applications.

As discussed, the parasitic coupling capacitances of the on-chip interconnections are always superposed on the intrinsic nonlinear parasitic capacitances of the power MOSFETs. The overall characteristic capacitances are the sum of these parasitic capacitances. After taking into account the parasitic capacitances of the on-chip interconnections, the nonlinearity of the overall total capacitances tends to be reduced. This is because the voltage-dependent variations of the overall total capacitances become relatively less than before. This is actually one of the ways for linearization of the nonlinear parasitic capacitances of the power MOSFETs. The nonlinear parasitic capacitances of the power MOSFETs can be added with on-chip capacitor [41], or can be added with external off-chip capacitors [103], [104]. Note that for conventional class E resonant inverters, the output capacitances of the switches set a maximum frequency limit for a given output power and a given input voltage of a design [3], [123], [138,] [139], or equivalently, the output capacitances of the switches set a minimum output power limit for a given frequency and a given input voltage of a design [150], [151]. Operating either at a switching frequency higher than the maximum frequency limit, or at an output power lower than the minimum output power limit, leaves the optimum operation conditions of the class E inverters and decreases the efficiency. Therefore, the linearization of the nonlinear parasitic capacitances of the power MOSFETs may tighten other operation constraints for power converters. However, topologies that effectively absorb device parasitic capacitances into the switch wave-shaping network, such as class φ_2/EF_2 inverters, break the tight link between the device output capacitance and the output power and the switching frequency [150], [151].

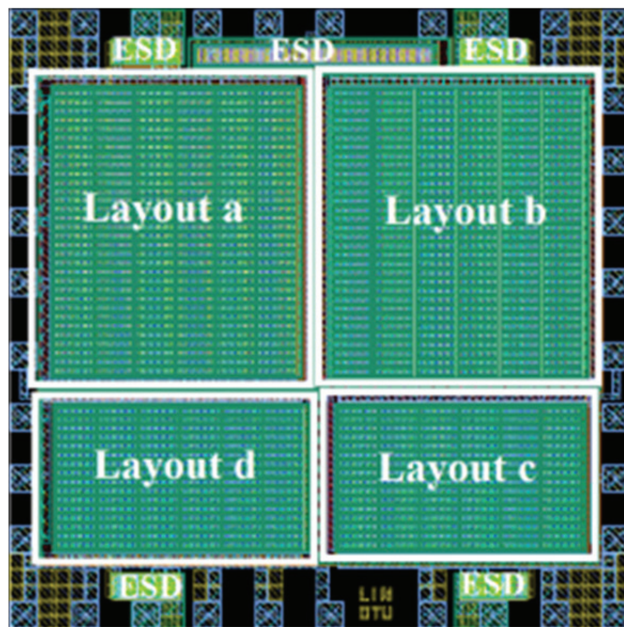


Fig. 3.15 Layout of the chip design. The four proposed layout structures of the high voltage power MOSFETs are highlighted. The chip pads are located on the four edges of the chip and designed according to industrial standards. [Appendix A.2]

The layout of the chip design is shown in Fig. 3.15, and the four proposed layout structures of the high voltage power MOSFETs are highlighted with the white color boxes. The die area is 2.31 mm2, i.e. 1520 μm x 1520μm. The principles of the structures of the layout-a, layout-b, layout-c, and layout-d are previously described in Fig. 3.14.

3.3 On-chip Nonlinear Figure-of-Merits and Optimization

As discussed in the chapter 2, recent research shows that figure-of-merits (FOMs) are not consistently used for device-to-device comparisons. This section presents a systematic analysis of the optimization of the nonlinear FOMs. The analysis is based on a 100 V power MOSFET designed in a 0.18 µm partial SOI process. The parameters of this power MOSFET are summarized in Table 3.5. Note that it is not the same MOSFET that is used in section 3.1.

Table 3.5 Parameters of the the high voltage power MOSFET for optimization of FOMs

Parameters	Values	Comments
Breakdown voltage (between drain and source)	> 110 V	Process [230]
Maximum operating voltage (between drain and source)	100 V	Process [230]
Maximum operating voltage (between gate and source)	5.5 V	Process [230]
Number of rows	**32**	Design of this work
Number of columns	6	Design of this work
Number of unit cells	**192**	Design of this work
Gate length of unit cells	0.5 µm	Design of this work
Gate finger width	10 µm	Design of this work
Number of fingers per unit cell	10	Design of this work
Equivalent gate width per unit cell	100 µm	Design of this work
Total length	**777** µm	Design of this work
Total width	**679** µm	Design of this work
Total die area	**0.5276** mm^2	Design of this work

By using the modelling method presented in section 3.1, for the high voltage power MOSFET in Table 3.5, the nonlinear parasitic capacitances and the nonlinear equivalent resistance R_{ds} versus the gate-source voltage V_{gs} are shown in Fig. 3. 16.

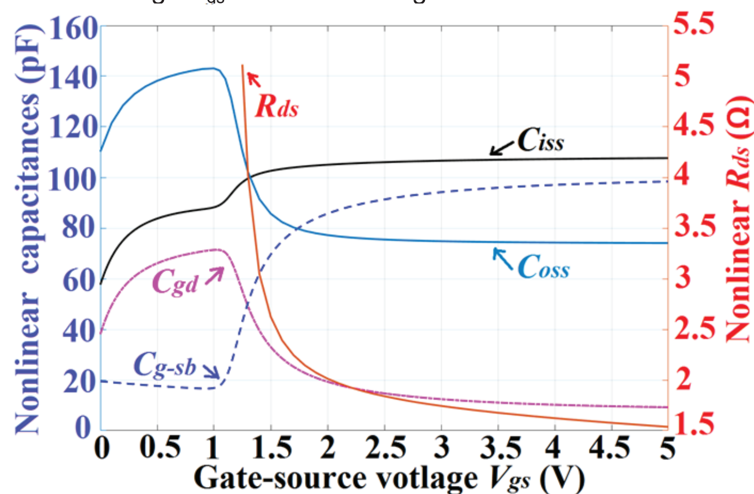


Fig. 3.16 Nonlinear parasitic capacitances and resistances versus gate-source voltage (simulated). This is additional work based on [Appendix A.1] and [Appendix A.3].

The insights into the nonlinearities of the parasitic capacitances are provided by Fig. 3.16. This is especially for the output capacitance C_{oss} when the gate-source voltage V_{gs} is above the threshold voltage (≈ 1.1 V for this power MOSFET). The output capacitance C_{oss} still presents during the on-state of the power MOSFET. This means that there is still energy stored in the output capacitance during the on-state of the power MOSFET, and not all the energy previously stored in the output capacitance before the turn-on of the power MOSFET is dissipated through the on-resistance of the power MOSFET. The nonlinear equivalent resistance R_{ds} is evaluated under the same conditions. This is to highlight the design trade-offs, e.g. the products $R_{ds}\cdot C_{iss}$ and $R_{ds}\cdot C_{oss}$ are not constant, and both $R_{ds}\cdot C_{iss}$ and $R_{ds}\cdot C_{oss}$ decrease when V_{gs} is increased. In Fig. 3.17, the nonlinear parasitic capacitances C_{iss} (input capacitance) and C_{oss} (output capacitance) are shown with C_{dg} (drain-gate capacitance) and $C_{d\text{-}sb}$ (sum of drain-source capacitance C_{ds} and drain-bulk capacitance C_{db}).

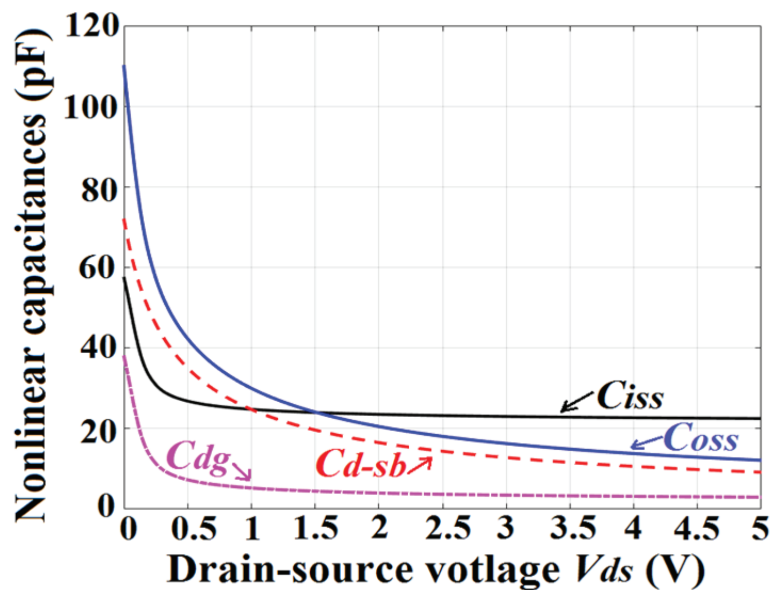
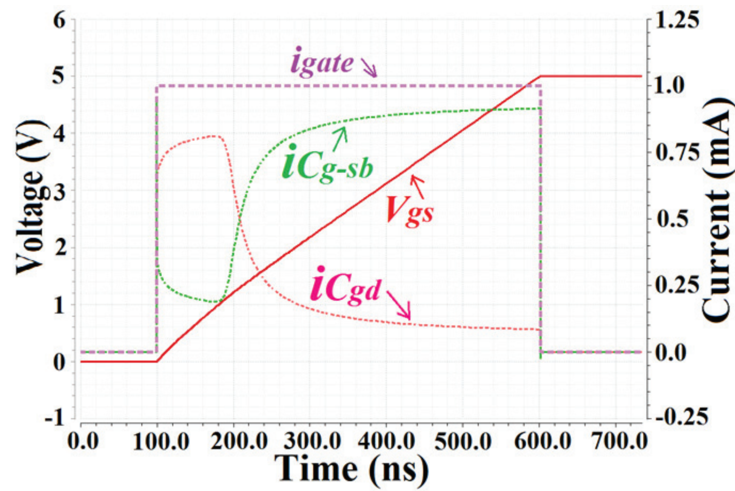


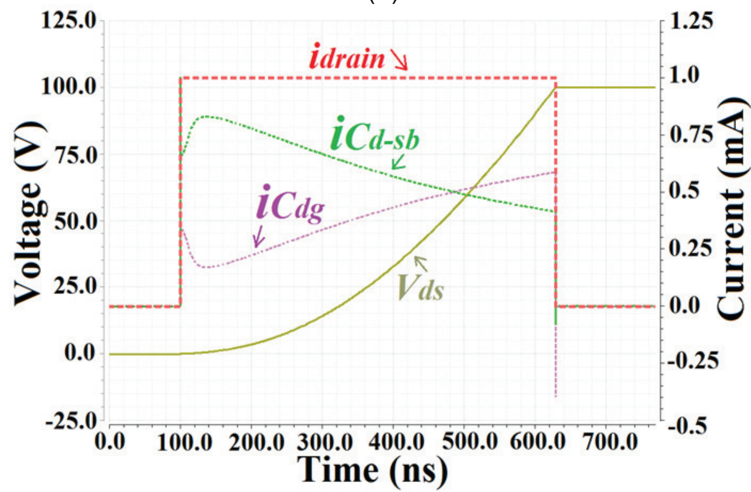
Fig. 3.17 Nonlinear parasitic capacitances versus drain-source voltage (simulated). This is additional work based on [Appendix A.1] and [Appendix A.3].

The gate charge behaviour of the power MOSFET in off-state (charging the gate when drain, source, and bulk are shorted to ground) is simulated and shown Fig. 3.18 (a). A current pulse of 1 mA is applied to the gate from 100 ns. The derivative dv/dt of the resulting V_{gs} decreases. This is because C_{iss} increases with V_{gs}, as shown in Fig. 3.16. Note that the current begins to charge C_{gd} (gate-drain capacitance) rather than $C_{g\text{-}sb}$ (sum of gate-source capacitance C_{gs} and gate-bulk capacitance C_{gb}). This is because C_{gd} is larger than $C_{g\text{-}sb}$ for low V_{gs} values.

The output charge behaviour of the power MOSFET in off-state (charging the drain when gate, source, and bulk are shorted to ground) is simulated and shown Fig. 3.18 (b). A similar current pulse with a different pulse width is applied to the drain. The derivative dv/dt of the resulting V_{ds} increases. This is because C_{oss} decreases as V_{ds} increases, as shown in 3.17. C_{dg} decreases faster than $C_{d\text{-}sb}$ for low V_{ds} values, but C_{dg} decreases slower than $C_{d\text{-}sb}$ for high V_{ds} values. Therefore, the current mainly charges $C_{d\text{-}sb}$ in the beginning and mainly charges C_{dg} in the end.



(a)



(b)

Fig. 3.18 Simulated charge behaviour (off-states).
(a) Gate charge behaviour. (b) Output charge behaviour.
This is additional work based on [Appendix A.1] and [Appendix A.3].

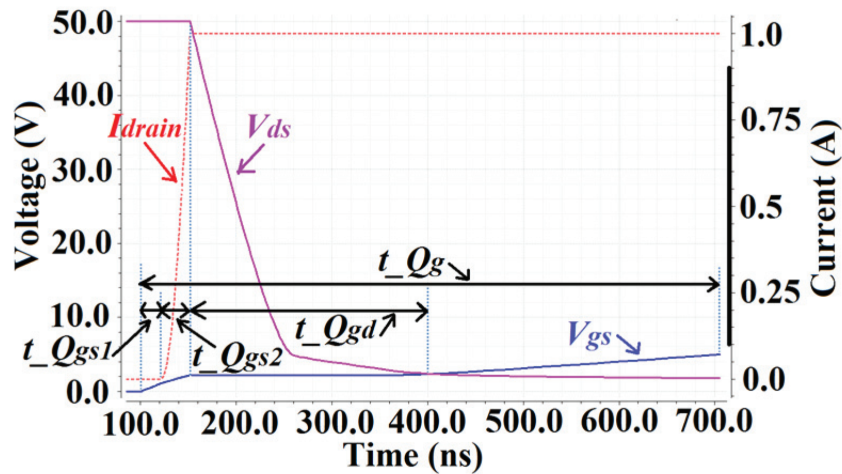


Fig. 3.19 Simulated turn-on waveforms and naming conventions. [Appendix A.3]

There is no standard test circuit to derive gate charges. Numerous test circuits are reviewed and compared in this research work [Appendix A.3], and the switching power-pole configuration is selected for the purpose of deriving different FOMs, especially for those FOMs composed of sub-components of gate charges. The simulated turn-on waveforms are shown in Fig. 3.19 and the naming conventions of the gate charges are also denoted. A current pulse of 1 mA is applied to the gate from 100 ns. The current pulse has a variable pulse width, to charge the gate-source voltage V_{gs} to different voltage potentials. The nonlinear gate charges versus different operating conditions are simulated and shown in Fig. 3.20. The equivalent resistance R_{ds} is derived under the same conditions, as the ratio of the final-state V_{ds} to the final-state I_{drain}. The final-state is defined as the state at the end point of the gate-charge event. The original-state is defined as the state at the start point of the gate-charge event.

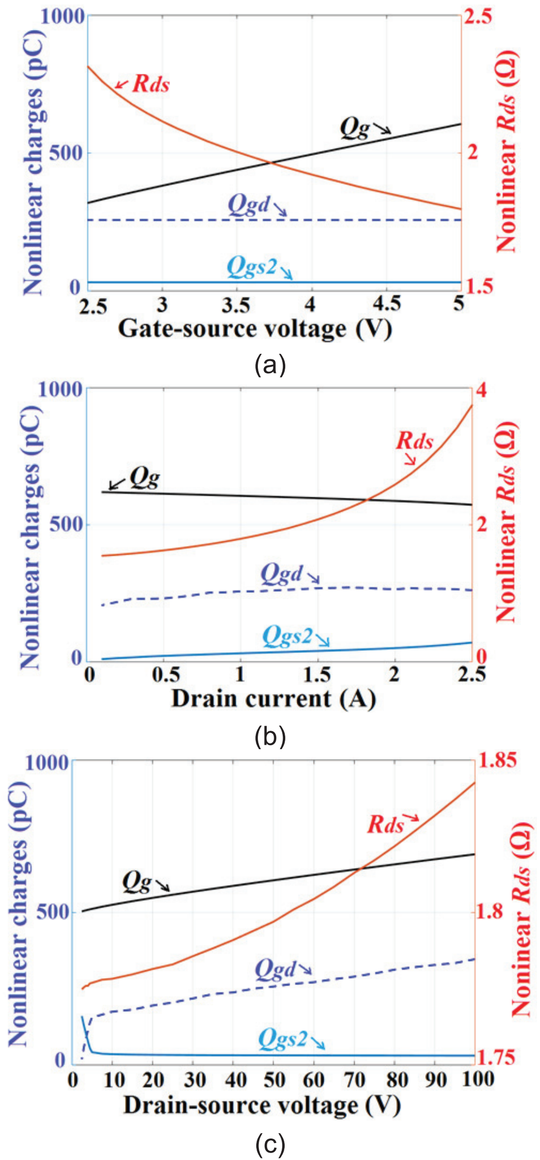


Fig. 3.20 Nonlinear gate charges and equivalent resistances. [Appendix A.3]
(a) Versus final-state V_{gs} (I_{drain} = 1 A, V_{ds} = 50 V).
(b) Versus final-state I_{drain} (V_{gs} = 5 V, V_{ds} = 50 V).
(c) Versus original-state V_{ds} (I_{drain} = 1 A, V_{gs} = 5 V).

The different forms of figure-of-merits in (3.1)-(3.4) are analysed. The output charge Q_{oss} is estimated with the power MOSFET in the off-state, i.e. the same as in Fig. 3.18 (b). For this reason, the output charge Q_{oss} and the soft-switching figure-of-merit $FOM_{soft\text{-}sw}$ are evaluated only versus the drain-source voltage V_{ds}. The derived FOMs versus different operating conditions are shown in Fig. 3.21.

$$FOM_{com1} = R_{ds} \cdot Q_g \tag{3.1}$$

$$FOM_{com2} = R_{ds} \cdot Q_{gd} \tag{3.2}$$

$$FOM_{hard-sw} = R_{ds} \cdot \left(Q_{gd} + Q_{gs2}\right) \tag{3.3}$$

$$FOM_{soft-sw} = R_{ds} \cdot \left(Q_g + Q_{oss}\right) \tag{3.4}$$

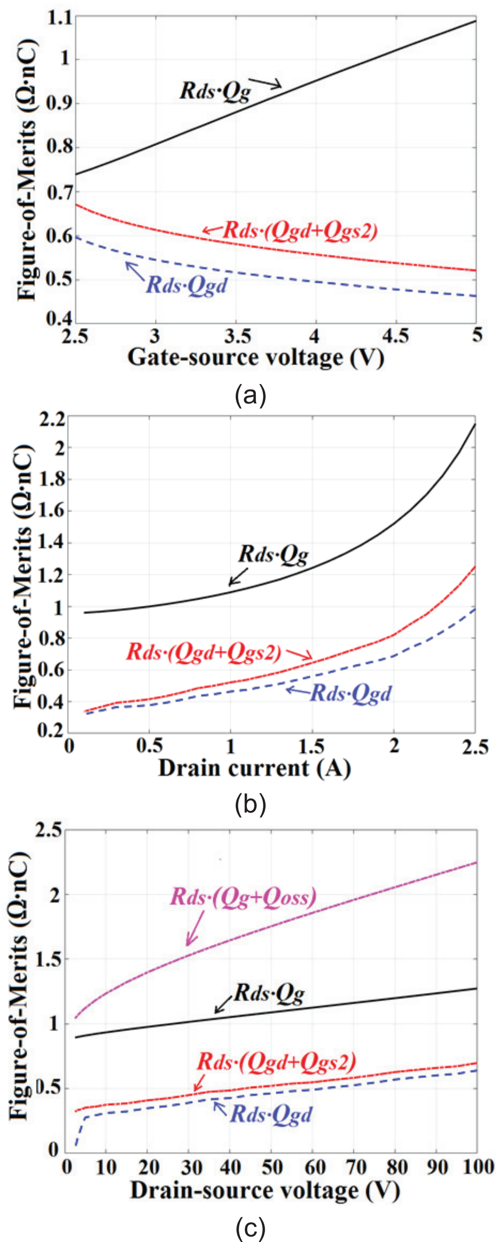


Fig. 3.21 Nonlinear figure-of-merits (FOMs). [Appendix A.3]
(a) Versus final-state V_{gs}. (b) Versus final-state I_{drain}. (c) Versus original-state V_{ds}.

Table 3.6 Optimization of nonlinear figure-of-merits (FOMs) [Appendix A.3]

	Best-case FOM vs. Worst-case FOM FOM is lowered: by times (by percentage)			
	FOM_{com1}	FOM_{com2}	$FOM_{hard\text{-}sw}$	$FOM_{soft\text{-}sw}$
V_{gs}	1.5 (32 %)	1.3 (22 %)	1.3 (22 %)	N/A
I_{drain}	2.2 (55 %)	3.0 (67 %)	3.7 (73 %)	N/A
V_{ds}	1.4 (30 %)	18.3 (95 %)	2.2 (54 %)	2.2 (54 %)

The FOMs at the same operating conditions as Fig. 3.21 are numerically summarized in Table 3.6. The analyses of the nonlinear FOMs are discussed as follows:

- In Fig. 3.21 (a), FOM_{com1} and FOM_{com2} show the contradicting trends. It means that optimization of one FOM may degrade another. There is a trade-off between the FOMs. A common trade-off is between the final-state R_{ds} and the total gate charge Q_g, as shown in Fig. 20 (a).

- In Fig. 3.21 (b), all FOMs are dominated by R_{ds}. The equivalent resistance R_{ds} increases for high I_{drain} values, due to the quasi-saturation effects and the drain current compression effects [235]. The power MOSFET starts to leave the linear region.

- In Fig. 3.21 (c), FOM_{com2} is dominated by Q_{gd}, and it quickly vanishes when the original-state V_{ds} has low values. This occurs when the power MOSFET is in the quasi-saturation region before the gate-charge event, i.e. quasi-zero voltage switching. The operation of the power MOSFET is preferably in the quasi-saturation region with quasi-zero voltage switching, rather than deeply in the linear region before the gate-charge event with absolute zero voltage switching (ZVS). FOM_{com2} is lowered/improved by 95 % (theoretically 100 %) compared to the worst-case in Table 3.6.

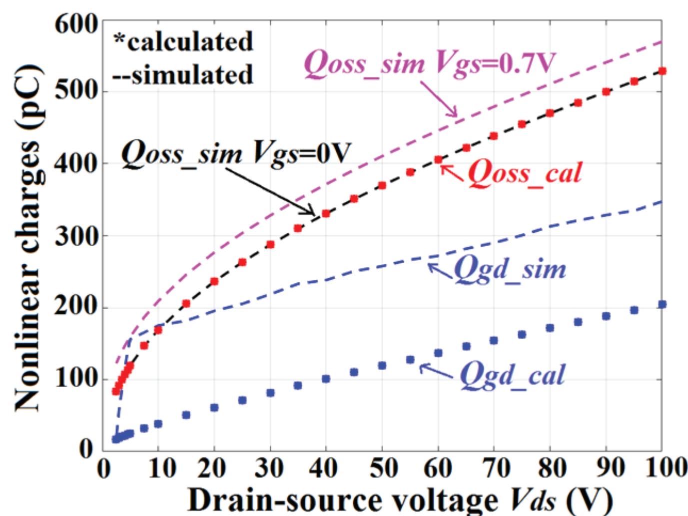


Fig. 3.22 Comparison of calculated and simulated values of gate-to-drain charge Q_{gd} and output charge Q_{oss}. This is additional work based on [Appendix A.1] and [Appendix A.3].

The output charge Q_{oss} and the gate-to-drain charge Q_{gd} may be calculated using (3.5) and (3.6), respectively. And the comparison of the calculated values and the simulated values is shown in Fig. 3.22.

$$Q_{oss} = \int_0^{V_{op}} C_{oss}(V_{ds}) \cdot dV_{ds} \quad (3.5)$$

$$Q_{gd} = \int_0^{V_{op}} C_{gd}(V_{ds}) \cdot dV_{ds} \quad (3.6)$$

The integration in (3.21) starts from 0 V [12] to the operating voltage V_{op}, i.e. the original-state V_{ds}. The integration in (3.21) alternatively starts from the negative barrier potential [120], if the body diode junction capacitance is charged from a negative voltage. The calculated Q_{oss_cal} and the calculated Q_{gd_cal} are based on the C_{oss} and C_{dg} curves of Fig. 3.17, respectively. The simulated Q_{gd_sim} is retrieved from Fig. 3.20 (c). The simulated Q_{oss_sim} is obtained using the same configuration of Fig. 3.18 (b) with different V_{gs} values, separately. From the comparison of the results, the calculated Q_{oss_cal} gets discrepancies when V_{gs} is higher than 0 V. This is due to the fact that the output capacitance C_{oss} also varies versus V_{gs} (as well as Vds), as shown in Fig. 3.16. The calculated Q_{gd_cal} is lower than the simulated Q_{gd_sim}. This is because that the calculation of Q_{gd_cal} does not take into account the nonlinearities of C_{gd} ($C_{g\text{-}sb}$, and C_{iss}) versus V_{gs}.

As a summary, a systematic analysis of the optimization of the nonlinear FOMs is performed. When compared to the worst-case non-optimized FOMs, the nonlinear FOMs are lowered by up to 18.3 times and improved by up to 95 %, for a given power MOSFET. This analysis provides insights into the nonlinearities of the gate charges, the output charges, and hence the FOMs. Because FOMs are nonlinear and can dramatically change for a given device, a device-to-device comparison using FOMs is only meaningful when the comparison is done under the same operating conditions.

3.4 Off-chip Parasitic Considerations of Packages

This section briefly discusses the impacts of packages on the performances of high voltage power MOSFETs. Packages, by themselves, are not a part of on-chip design. However, the extreme performances that can ultimately be achieved by the on-chip power MOSFETs are jointly determined by on-chip device parasitics, on-chip layout parasitics, off-chip package parasitics, and off-chip PCB parasitics, as shown in Fig. 3.2.3. An example is shown in Table 3.7, where the switching speed of a power MOSFETs is limited by the package and circuit parasitics, and the silicon device by itself is not the limiting factor of the switching speed.

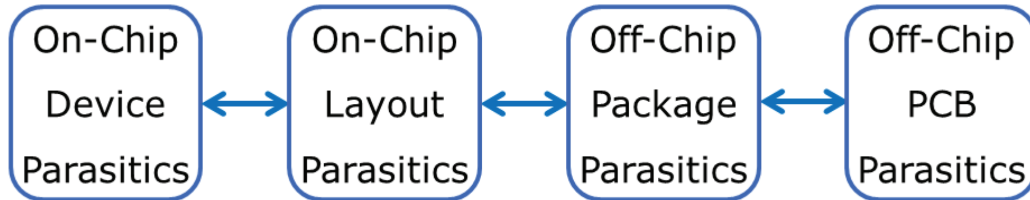


Fig. 3.23 Performances of integrated power MOSFETs are determined by parasitic effects.

Table 3.7 Switching speed is becoming dictated by package and circuit parasitics [41]

	Silicon	Package	Circuit
dI_D/dt	28 A/ns	4 A/nS	5 A/ns
dV_D/dt	13 V/ns	13 V/nS	14 V/ns

*The package is LFPACK (Loss Free Package), and $L_{package}$ = 0.6 nH.
*The circuit dV_D/dt is calculated with an input voltage of 12 V, and a switching frequency of 100 MHz.

The integrated power MOSFETs designed in this research work are lateral devices implemented in a SOI process. The cross sections of these devices are confidential. Therefore, the package impacts are to be elaborated using public power devices. The cross section of a vertical SiC MOSFET from Infineon is shown in Fig. 3.24. The cross section of a lateral GaN FET from EPC is shown in Fig. 3.25. The cross section of a GaN FET from GaN Systems is shown in Fig. 3.26. The most important thing to note is that, for vertical devices, the source terminal and the drain terminal are located on the opposite sides of the die, and for lateral devices, the source terminal and the drain terminal are located on the same side of the die.

The resulting magnetic field through the connection of two vertical MOSFETs (in a half-bridge configuration) is shown in Fig. 3.27. The resulting magnetic field is big [Appendix A.6], and it significantly contributes to the radiated electromagnetic emissions, which may couple into other circuits and compromise the radiated electromagnetic compatibility (EMC).

The resulting magnetic field through the connection of two lateral MOSFETs (in a half-bridge configuration) is shown in Fig. 3.28. The resulting magnetic field is small [Appendix A.6], and the external electromagnetic fields are significantly reduced.

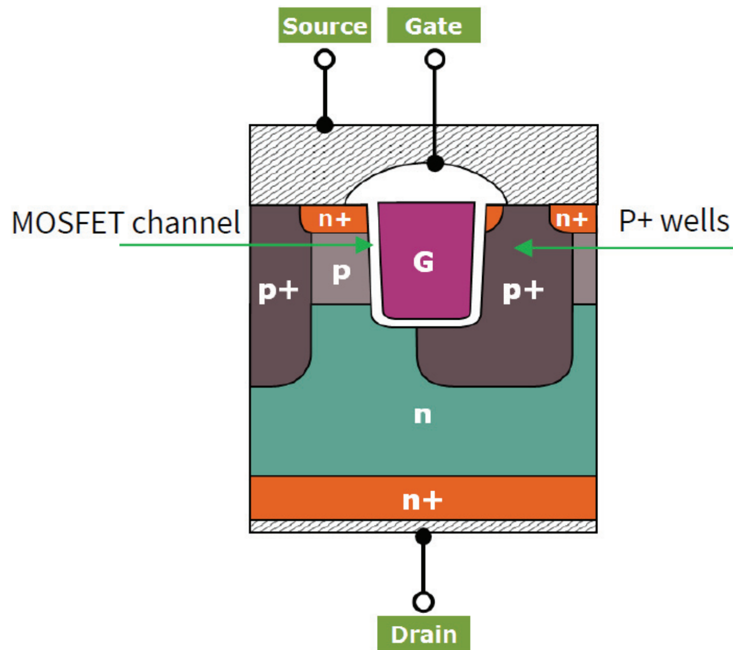


Fig. 3.24 Vertical SiC MOSFET, by Infineon [238].
Lateral SiC MOSFET can be found in [14].

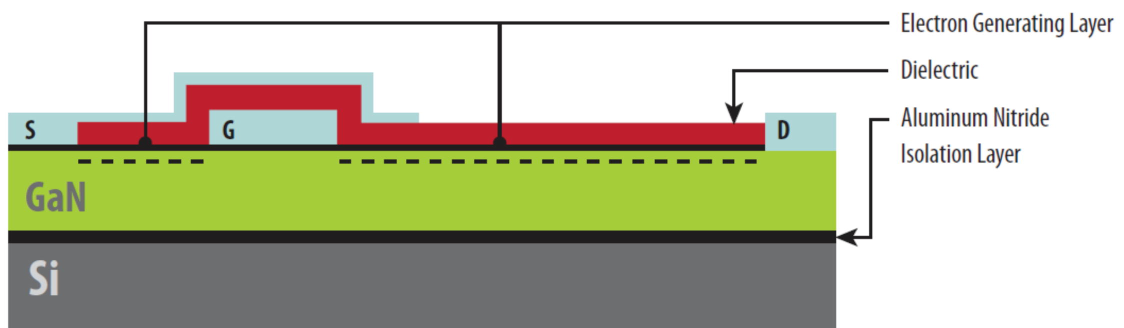


Fig. 3.25 Lateral GaN FET, by EPC [239].

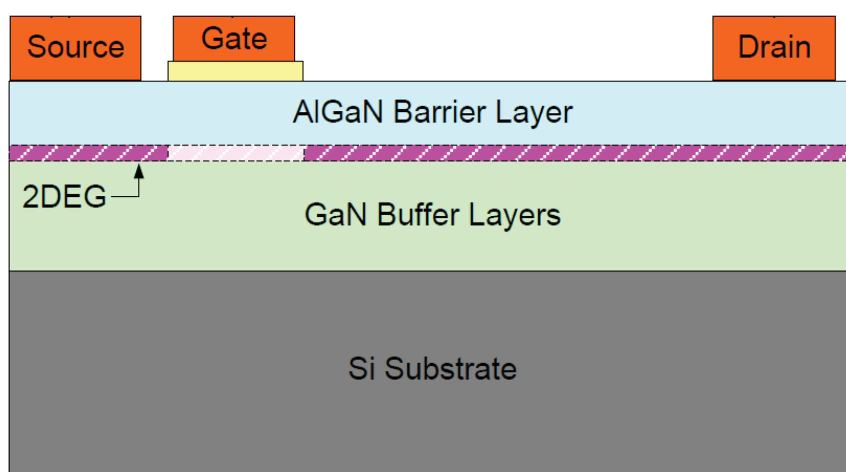


Fig. 3.26 Lateral GaN HEMT, by GaN Systems [240].

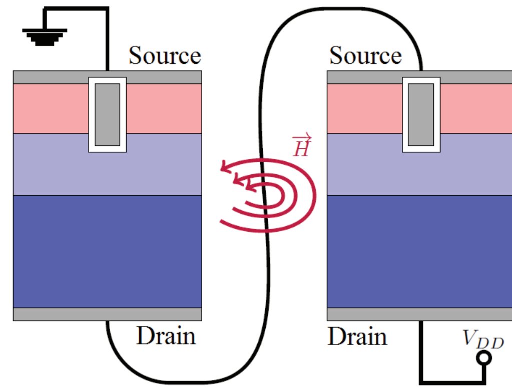


Fig. 3.27 Vertical MOSFETs in a half-bridge configuration, and resulting magnetic field. [Appendix A.6]

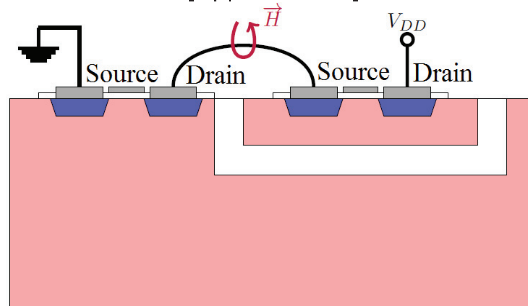
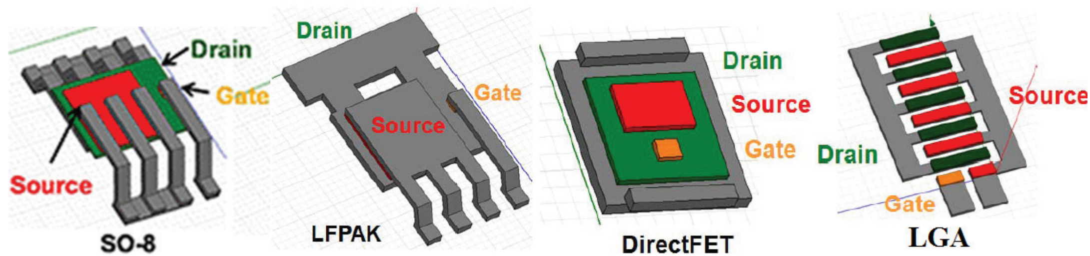


Fig. 3.28 Lateral MOSFETs in a half-bridge configuration, and resulting magnetic field. [Appendix A.6]



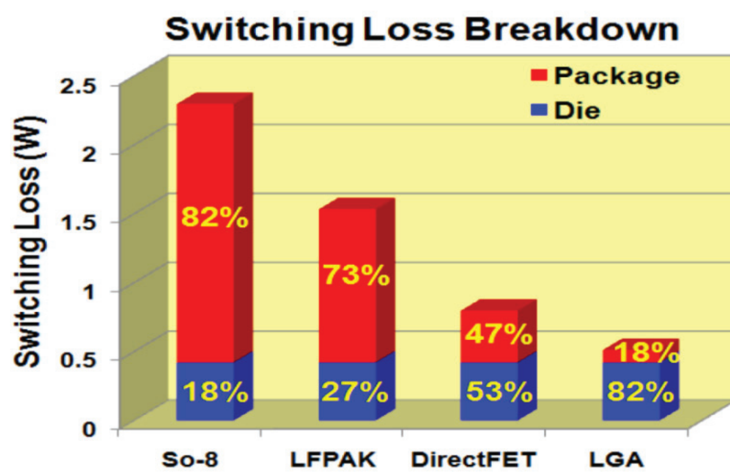


Fig. 3.29 The impact of the package parasitics on power device losses, by Virginia Tech [241]. A buck converter, f_s=1 MHz, V_{in}=12 V, V_o=1.2 V, I_o=20 A, L=150 nH. A loss model [243] is used to break down the switching loss into the contributions of the die and the package.

Package parasitic inductances slower down the turn-on and turn-off switching time of power devices, and cause high switching losses. Four common packages of power devices, i.e. SO (Small Outline), LFPACK (Loss Free Package), DirectFET, and LGA (Land/Linear Gate Array), are shown in Fig. 3.29 [241], [242]. The packages of vertical devices such as SO, LFPAK, and DirectFET require the source/gate pads or the drain pads to be connected to the PCB through external leads and long connections, and thus these packages suffer from high source/gate or drain parasitics. Note that DirectFET packages flip vertical devices to minimize the common source inductance. The packages of lateral devices such as LGA do not require the external leads and long connections, and thus these packages suffer from less switching losses compared to those of vertical devices. LGA packages add the least switching losses that are due to the parasitic inductances of PCB traces, and also add the least unwanted parasitic resistances. This analysis is based on a loss model of a buck converter, manufacturer simulation models, and Maxwell 3D FEA (Finite Element Analysis) parasitic extraction simulations [241]. Further analysis of the loss breakdown in Fig. 3.29 shows that the package parasitics contribute 0.2-4.6 times the switching loss of the power device die.

The packages of the high voltage power MOSFETs designed in this research work use bond wire technology. The bond wire technology, in principle, suffers from more parasitic inductances and resistances than any of the above package types. This is because all the terminals of the source, gate, and drain have to be connected through bond wires from the chip pads to the package pins. The chip pads and bond wires are designed according to industrial standards, such as chip bond pad pitches, chip bond pad opening sizes, and bond wire lengths and angles. The packages, bond wires, and chip pads used in this work are summarized in Table 3.8. The BD (Bonding Diagram) of the design is shown in Fig. 3.30. The photograph of the package of the design is shown in Fig. 3.31.

Table 3.8 Packages, bond wires, and chip pads used/designed in this work.

Package Type	QFN (Quad Flat No-lead)
Package Size	4 mm x 4 mm
Package Lead Number	24 Lead (QFN24)
Package Body	Pre-Molded Air-Cavity Plastic-Package
Package Lead Frame	Copper
Package Lead Finish	Gold-Plate
Package Die Pad	2.300 mm x 2.300 mm
Bond Wire Width	≈ 30 μm
Bond Wire Material	Gold
Physical Die Size	1635 μm x 1635 μm
Design-Area Die Size	1520 μm x 1520 μm
Chip Pad Size	62 μm x 62 μm
Chip Pad Pitch	≥ 150 μm

Note that the physical die size (1635 μm x 1635 μm) is relatively small compared to the smallest available package size (4 mm x 4 mm). This results in the lengths of the bond wires around 650-900 μm. Based on the analysis in [244] and the rule-of-thumb number of 1 nH/mm, each bond wire introduces about 0.65-0.9 nH parasitic inductance. Due to the limited number of package pins, the highest design priority of this work is given to reduce the common source

inductance. Therefore, 3-4 bond wires are used for the same source network of each power MOSFET. The number of bond wires used in the package design is summarized in Table 3.9.

Table 3.9 Summary of number of bond wires used for each power MOSFET

	Source	Drain	Gate	Bulk
Layout a	3	2	1	N/A
Layout b	3	2	1	N/A
Layout c	3	2	1	N/A
Layout d	4	2	1	1
There are 2 other bond wires specially used for the SOI process. There are 4 package pins where 2 bond wires share the same package pin. Total number of bond wires is 28. Total number of package pins is 24.				

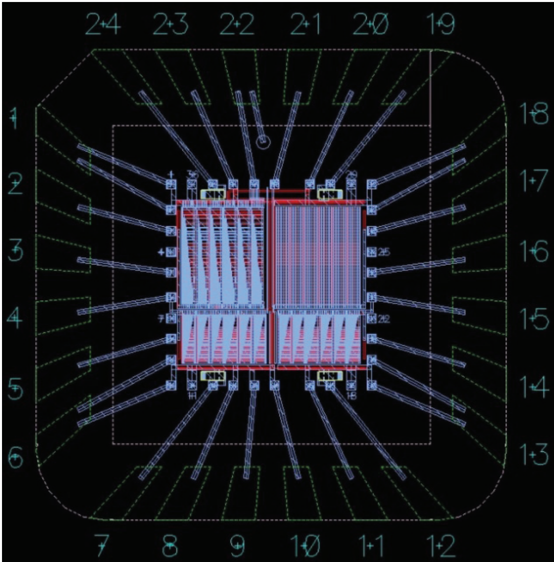


Fig. 3.30 Bonding diagram of the chip pad, bond wire, and package pin design.

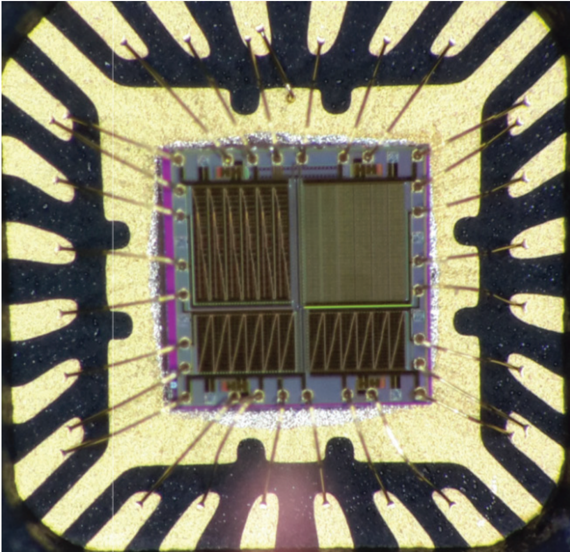


Fig. 3.31 Photograph of the manufactured high voltage power MOSFETs in a QFN package. [Appendix A.6]

3.5 Off-chip Parasitic Considerations of PCB

This section briefly discusses the parasitic effects and considerations of PCB design. The parasitics of packages and PCB are often combined and jointly effective in practice, e.g. the common-source inductance may result from both package parasitics and PCB parasitics. Two undesired turn-on events [239], [245], [246], i.e. dv/dt-induced turn-on and di/dt-induced turn-on, can result from the same parts of the parasitic elements. The parasitics that cause dv/dt and di/dt induced turn-on are summarized in Table. 3.10. The key difference is that dv/dt-induced turn-on is triggered by a positive dv/dt of the drain voltage of an off-state device through the gate-drain capacitance C_{gd}, whereas di/dt-induced turn-on is triggered by a negative di/dt of the drain current of an off-state device through the common-source inductance. From a PCB design point of view, adjusting gate resistances is solely a trade-off between the sensitivities of the dv/dt-induced turn-on and the di/dt-induced turn-on.

Table 3.10 Summary of parasitics that cause dv/dt and di/dt induced turn-on

dv/dt-induced turn-on (of an off-state device)	**di/dt**-induced turn-on (of an off-state device)
Gate-drain capacitance C_{gd} (Device)	Common-source inductance (Package & PCB)
Gate-source capacitance C_{gs} (Device)	
Gate on-chip R_{g_layout} (Layout)	
Gate pad-to-pin R_{g_pak} (Package)	
Gate trace R_{g_trace} (PCB)	
Gate resistor R_{g_res} (PCB)	
Gate pull-down R_{sink} (Driver)	

Table 3.11 Summary of trade-offs of gate resistances

	Gate resistance is small	Gate resistance is big
Pull-up (Turn-on)	• Gate voltage overshoot versus maximum gate voltage with gate loop inductance • Cross-conduction/Shoot-through • Potential gate oscillations	• Slow turn-on • Damping gate overshoot
Pull-down (Turn-off)	• Gate voltage ringing versus threshold voltage with common-source inductance • Drain voltage overshoot • Potential gate oscillations • **Less dv/dt**-induced turn-on • **More di/dt**-induced turn-on Cross-conduction/Shoot-through	• Slow turn-off • Damping gate ringing • **Less di/dt**-induced turn-on • **More dv/dt**-induced turn-on Cross-conduction/Shoot-through
• Adjusting gate resistances is solely a trade-off solution. • An improved solution is to minimize the common-source inductance of package and PCB, e.g. to separate the gate loop and the power loop as close as to the power device. • Package parasitic inductances always contribute to the common-source inductance, i.e. the common inductance of the gate loop inductance and the power loop inductance. A high priority to minimize. Reduce gate loop inductance thus gate voltage overshoot.		

An improved solution is to minimize the common-source inductance, within which reducing the package inductances is the most effective way. This is because package inductances always contribute to the common-source inductance, i.e. package inductances contribute to both the gate loop inductance and the power loop inductance. The trade-offs of the gate resistance design and the considerations of the common-source inductance are summarized in Table 3.11. The parasitic effects of the common-source inductance and the power loop inductance on power loss are calculated for a buck converter [239], as shown in Fig. 3.32. The higher the parasitic inductances become, the higher the power losses are. The improved solution is to minimize the common-source inductance, which is a part of the power loop inductance.

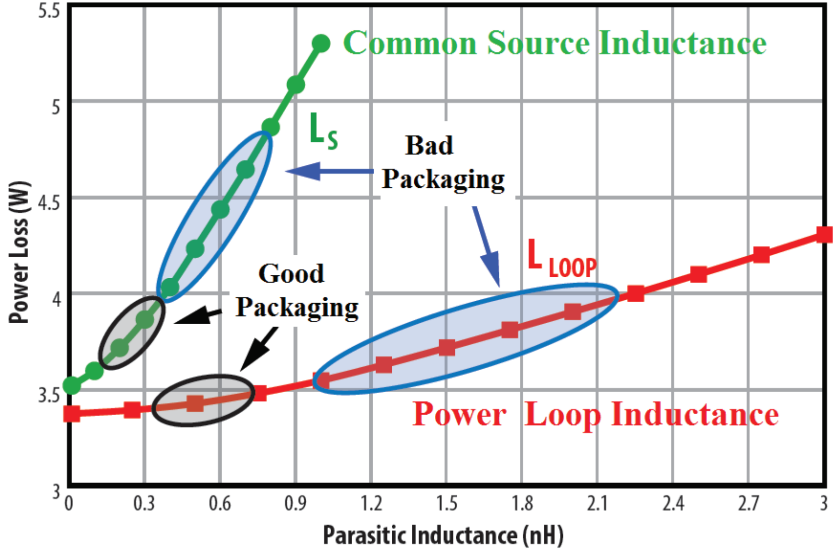


Fig. 3.32 Parasitic inductances impact on power loss [239].
Common-source inductance is controlled by package inductance and PCB inductance. Power loop inductance is also controlled by package inductance and PCB inductance. Power loop inductance includes common-source inductance.

3.6 Summary

The chapter 3 summarizes the research work on the component level of integrated high voltage power MOSFETs. The performances of power MOSFETs (such as maximum switching speeds and minimum attainable on-resistances) are jointly determined by on-chip device parasitics, on-chip layout parasitics, off-chip package parasitics, and off-chip PCB parasitics. Each of these areas is researched in this chapter. First, a modelling method is proposed to systematically analyse the nonlinear parasitic capacitances of power MOSFETs versus different bias voltages. Second, the side-by-side capacitive coupling and the layer-to-layer capacitive coupling of on-chip metal interconnections are analysed, and four layout structures are proposed and compared for integrated power MOSFETs. Third, the nonlinear figure-of-merits (FOMs) are systematically analysed for different voltage and current conditions, and optimized with quasi-zero voltage switching for a given power MOSFET. Fourth, the impact of package parasitics on power devices are analysed and the wire bonding design of this work is presented. Fifth, the PCB design considerations of the dv/dt-induced turn-on and the di/dt-induced turn-on are summarized and the priority to minimize package parasitic inductances (especially the part of the common source inductance) is highlighted, compared to the trade-off of gate resistances.

4. Inductor-Based Converters (Low-Voltage Output Converter)

This chapter addresses the design and investigations of inductor-based converters. These inductor-based converters have low-voltage (≤ 100 V) inputs, and are intended to be used as the output converter of a two-stage power converter architecture. The two-stage power converter architecture is to be discussed and elaborated in more details in the next chapter. This chapter focuses on the low voltage inductor-based converters.

4.1 Buck Converter Using Integrated Power MOSFETs

A synchronous buck converter is designed and implemented using the integrated high voltage power MOSFETs that are designed in a SOI process in the chapter 3. The specifications of the synchronous buck converter are summarized in table 4.1. The schematic of the buck converter is shown in Fig. 4.1. The duty cycle of the buck converter is 25 %.

Table 4.1 Specifications of the buck converter using integrated power MOSFETs.

Parameters	Specifications
Input Voltage	48 V
Output Voltage	12 V
Maximum Output Power	≥ 1 W
Switching Frequency	100 kHz
Output Voltage Ripple	≤ 500 mV
Operation mode	Continuous Conduction Mode (CCM) At Maximum Output Power

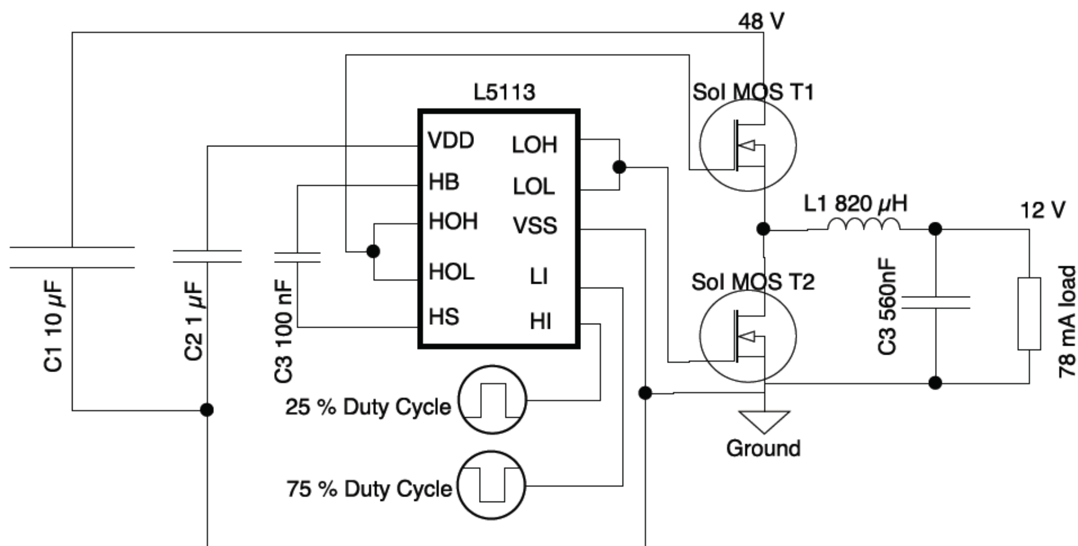


Fig. 4.1 Schematic of the buck converter using integrated power MOSFETs. [Appendix A.6]

For the design [Appendix A.6], [247], the inductor L1 is MSS1278-824KL from Coilcraft (820 μH ± 10 %) with a maximum series resistance of 1.296 Ω. At the maximum output power, the average current of the inductor current is 83 mA, and the peak-to-peak ripple of the inductor current is calculated to be 110 mA. Therefore, the buck converter is operated in Continuous Conduction Mode (CCM). The output capacitor C3 is a 50 V X7R ceramic capacitor (560 nF). The photograph of the buck converter prototype is shown in Fig. 4.2. The chip of the integrated power MOSEFTs is packaged in a QFN24 4 mm x 4 mm package, as described in the previous chapter. The function generator Rigol DG4062 is used for the gate signals, and the electronic load ELA250 from Zentro Elektrik is used as the load. The measured efficiency is above 90 % for 10-100 % of the maximum output power, and the efficiency is around 93 % for 30-100 % of the maximum output power. The thermal image of the buck converter prototype is shown in Fig. 4.3. It shows a temperature rise of less than 10 °C from an ambient temperature of 25.7 °C.

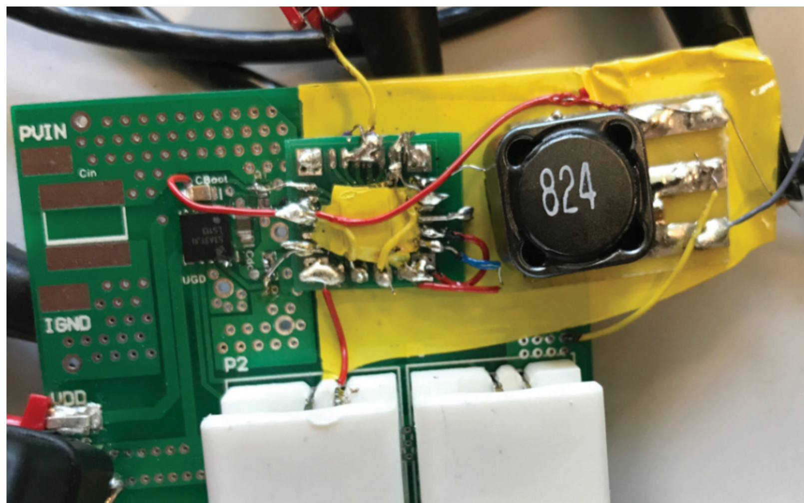


Fig. 4.2 Photograph of the buck converter prototype. The test chip composed of the integrated power MOSFETs is under the yellow isolation tape. The output inductor is on the right side. [Appendix A.6]

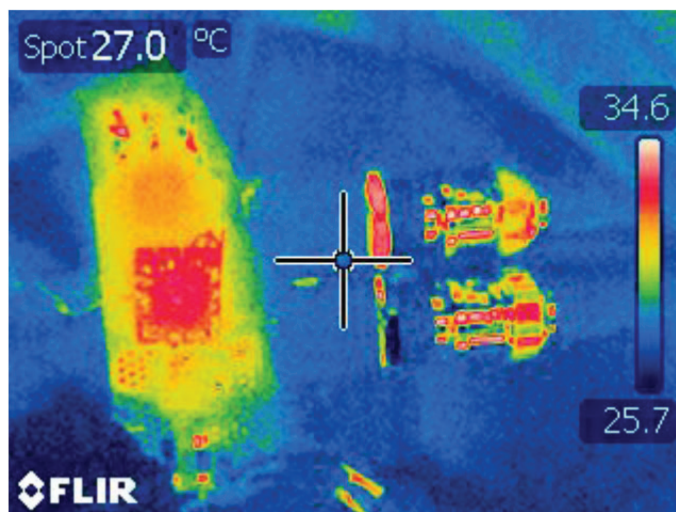


Fig. 4.3 Thermal image of the buck converter prototype. [Appendix A.6]
The image is taken with a 90° left-turn of the Fig. 4.2.

4.2 IC-Based Resonant Power Stage Investigations

This section focuses on the discussions of the resonant operation of a half-bridge configuration (e.g. class DE resonant inverters/converters) in common high voltage CMOS processes. Compared to a SOI process, a standard CMOS process has no buried oxide layer between the active layers and the substrate. The simplified cross section of an N-channel MOSFET in common high voltage CMOS processes is shown in Fig. 4.4. The structure of the N-channel MOSFET is well known. However, there are parasitic bipolar transistors that are embedded in the N-channel MOSFET structure. These parasitic bipolar transistors are often not modelled, and they are of the most importance for the resonant operation of the high voltage MOSFETs.

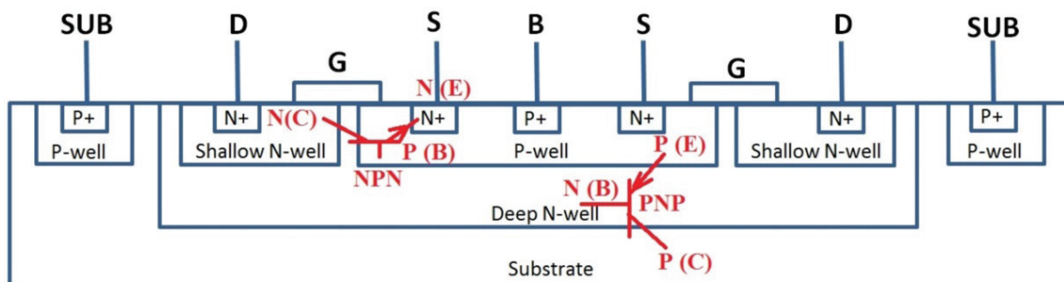


Fig. 4.4 Parasitic PNP and NPN bipolar transistors in a lateral N-channel MOFSET.
The cross section is simplified and representative for common high voltage CMOS processes.
This work is additional to the appendixes.

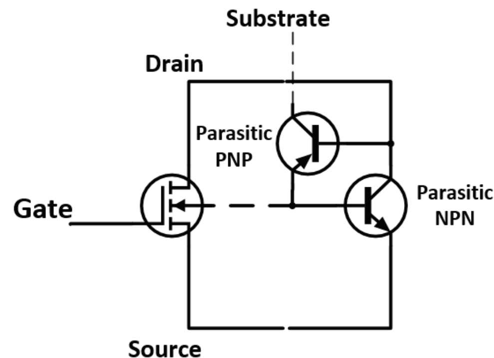


Fig. 4.5 Equivalent circuit of Fig. 4.4 with parasitic PNP and NPN bipolar transistors.
This work is additional to the appendixes.

The equivalent circuit of Fig. 4.4 with the parasitic PNP and NPN bipolar transistors is shown in Fig. 4.5. Resonant converters that are composed of a half-bridge configuration typically have inductive loads at the switching frequency to achieve soft-switching conditions. For zero voltage switching, the body diodes of the high voltage MOSFETs are commonly used to clamp the drain-source voltages before switches turn on. This applies to the body diodes of both the high-side switch and the low-side switch in a half-bridge configuration. If the body diode of the N-channel MOSFET in Fig. 4.4 is conducted, i.e. the bulk-drain diode is conducted, there are two scenarios to consider. The first scenario is shown in Fig. 4.6 and its equivalent circuit is shown in Fig. 4.7. The bulk-drain diode can be used as a conducting element, but it also causes parasitic current pulled from substrate, i.e. the substrate-drain diode is then also conducted and the substrate-drain diode is not intended to be used as a conducting element. In this case, an external Schottky diode may be used to prevent the substrate current and the conduction of the

substrate-drain diode. The second scenario is shown in Fig. 4.8 and its equivalent circuit is shown in Fig. 4.9. The substrate-drain diode is reversely biased in this case. However, the parasitic vertical PNP structure is still enabled. For a PNP bipolar transistor, when the base–emitter junction (i.e. drain-bulk in the structure) is forward bias, and the base-collector junction (i.e. drain-substrate in the structure) is reverse bias, the PNP transistor is in forward-active operation mode. Therefore, parasitic current is pushed from the bulk to the substrate. In both of the above scenarios, there is parasitic current either pulled from or pushed to the substrate. This causes unwanted effects such as changing the voltage reference potentials of the substrate across the die, or even worse coupling into other circuits on the same chip which results in distortions and degradations of signal integrity. The conclusion is that it is unlikely to achieve resonant converters with soft-switching conditions in common high voltage CMOS processes, unless the substrate current issue can be properly addressed. It needs to mention that the advanced isolation structure such as deep P-well is not available in this research work.

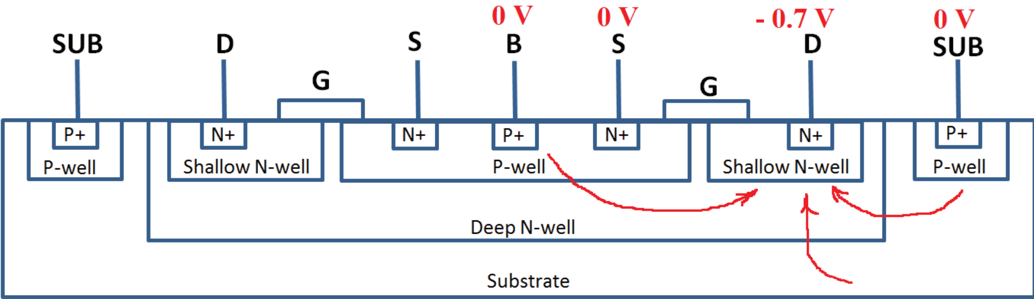


Fig. 4.6 Parasitic current is pulled from substrate
if $V_{bulk} = V_{sub}$ = 0V and body diode (bulk-drain) is conducted.

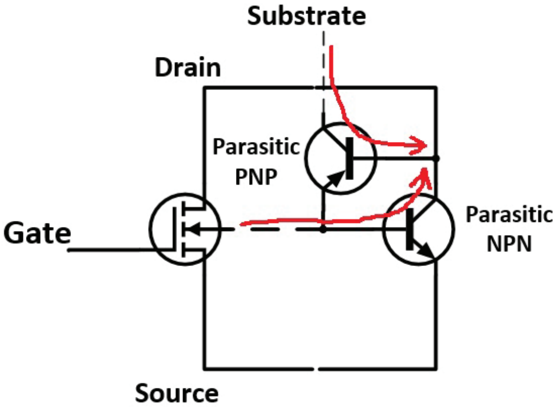


Fig. 4.7 Equivalent circuit of Fig. 4.6 with parasitic current pulled from substrate.

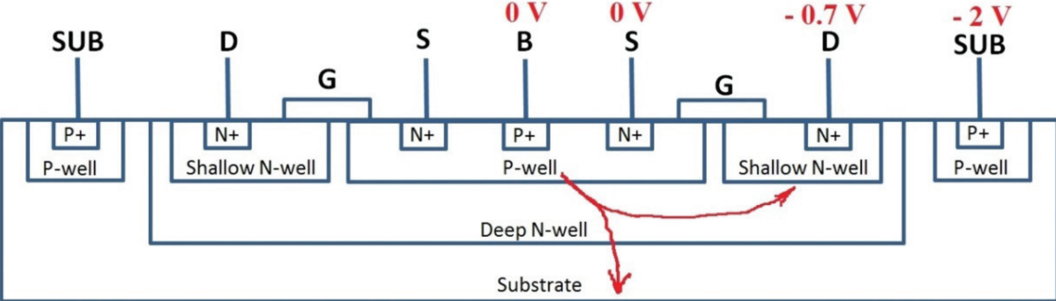


Fig. 4.8 Parasitic current is pushed to substrate if V_{bulk} = 0 V and V_{sub} = -2 V
(or equivalently V_{bulk} = 2 V and V_{sub} = 0 V) and body diode (bulk-drain) is conducted.

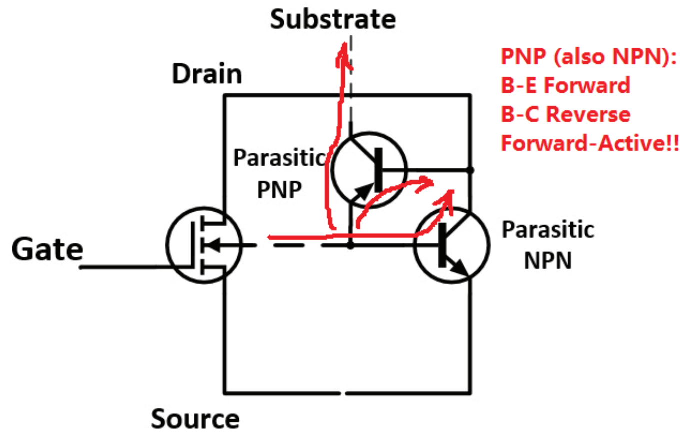


Fig. 4.9 Equivalent circuit of Fig. 4.8 with parasitic current pushed to substrate.

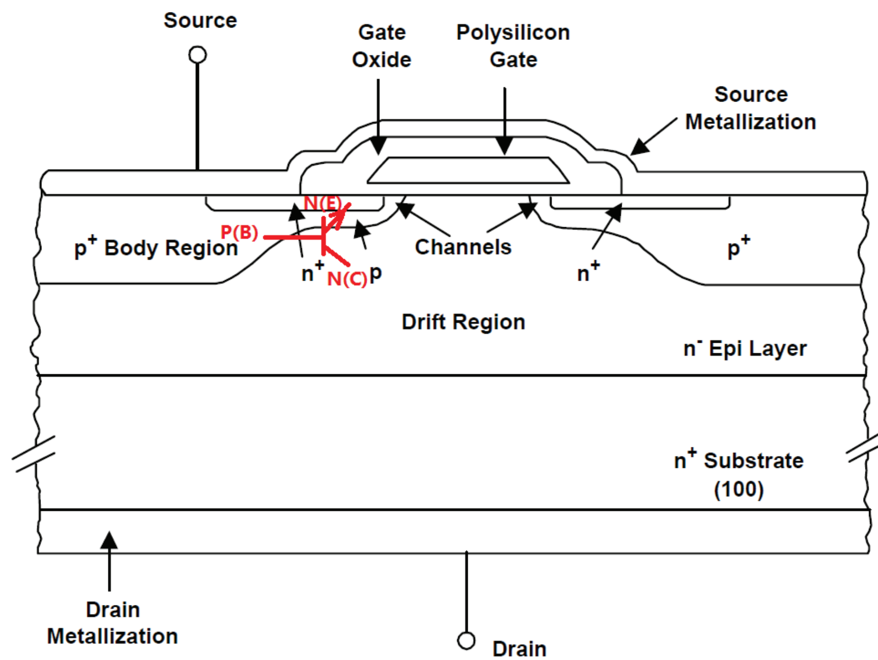


Fig. 4.10 Parasitic NPN bipolar transistor in a vertical N-channel MOFSET.
The cross section is based on the work [121].

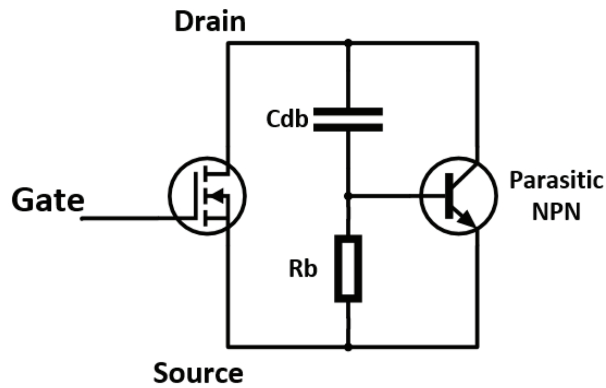


Fig. 4.11 Equivalent circuit of Fig. 4.10 with parasitic NPN bipolar transistor.
The equivalent circuit is based on the work [121].

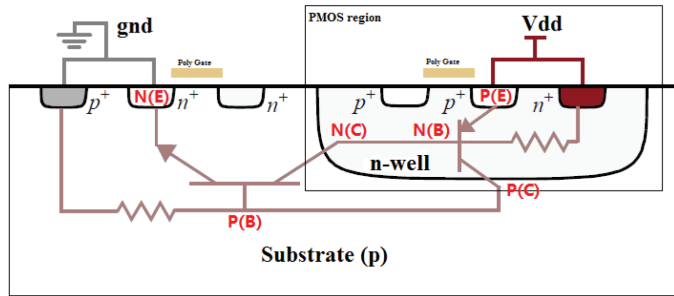


Fig. 4.12 Parasitic PNP and NPN bipolar transistors in standard CMOS processes (Latch-up). The cross section is based on the work [248].

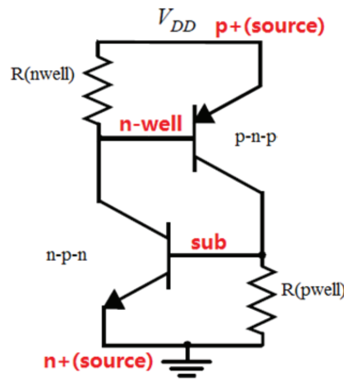


Fig. 4.13 Equivalent circuit of Fig. 4.12 with Parasitic PNP and NPN bipolar transistors. The equivalent circuit is based on the work [248].

The parasitic NPN transistor in a vertical device is shown in Fig. 4.10, and the equivalent circuit is shown in Fig. 4.11. The parasitic NPN transistor can cause dv/dt-induced turn-on [121], in addition to the mechanism discussed in the section 3.5. The parasitic N-P-N-P latch-up structure in a standard CMOS process is shown in Fig. 4.12, and the equivalent circuit is shown in Fig. 4.13. If triggered, the positive feedback between the parasitic NPN and PNP transistors can cause overcurrent and circuit failure [248]. This research work on the parasitic PNP and NPN bipolar transistors in lateral high voltage n-channel MOSFETs is often confused with the above two cases. Therefore, the comparison of these mechanisms is summarized in Table 4.2.

Table 4.2 Comparison of parasitic bipolar transistors of different mechanisms

	High Voltage CMOS (this work)	Vertical MOSFET (conventional)	Standard CMOS (latch-up)
Structure	Lateral	Vertical	Lateral
Device	Integrated	Discrete	Integrated
Parasitic BJTs	**Vertical PNP** (and Lateral NPN)	**Vertical NPN**	**Vertical PNP** **Lateral NPN**
Trigger	Single-BJT	Single-BJT	Two-BJTs
Condition	**No resistance needed**	**Bulk-resistance**	**Bulk-resistance** **Substrate-resistance**

4.3 Piezo-Based Resonant Power Stage Investigations

This section elaborates the investigations of using piezo elements for resonant power stages. An alternative way to implement inductor-less switch mode power supplies is to use piezo elements, e.g. piezoelectric transformers (PT) are used to replace conventional magnetic transformers [249]-[252]. The advantages of using piezo elements in power supplies are due to their low electromagnetic interference (EMI), small size, light weight, low cost, and potentially high power density and high efficiency. Ceramics are inorganic non-metallic materials. The operating principle of the piezoelectric ceramic elements is based on the electromechanical energy conversion. For piezoelectric transformers, as shown in Fig. 4.14, there is electromechanical coupling between the primary side and the secondary side. The primary side acts as a piezoelectric actuator and the secondary side acts as a piezoelectric transducer [249] coupled by mechanical vibrations. In contrast to the piezoelectric transformers in Fig. 4.14, in this research work, piezo elements with two terminals are investigated. The lumped parameter model of the investigated piezo elements is shown Fig. 4.15. The mechanical design of the piezo elements is confidential and done by the partner company Noliac [253]. The theoretical estimations of the lumped parameters are summarized in Table 4.3.

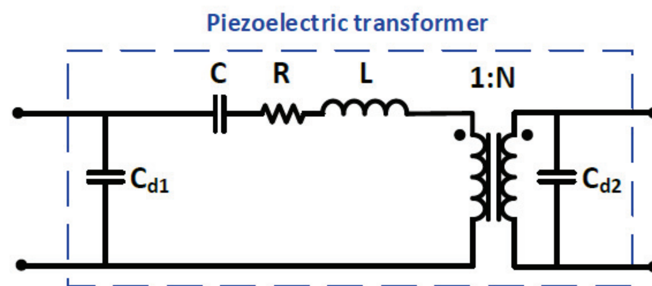


Fig. 4.14 Lumped parameter model of a piezoelectric transformer (PT) [249].
It is valid close to the resonance frequency of the operating resonance mode.
(i.e. one of the resonance modes, usually the most pronounced mode)

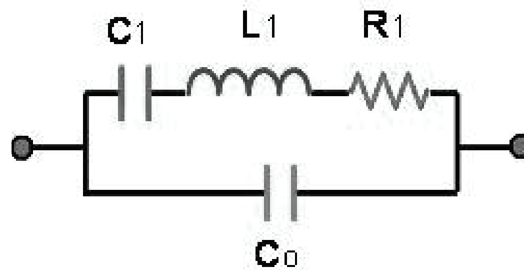


Fig. 4.15 Lumped parameter model of a piezo element in this research work [253].

Table 4.3 Theoretical estimations of the lumped parameters using the model of Fig. 4.15 [253]

Parameter	Comment	Estimated
C_0	Shunt Capacitance	3.190 nF
C_1	Motional Capacitance	0.810 nF
L_1	Motional Inductance	0.469 µH
R_1	Motional Resistance	0.030 Ω

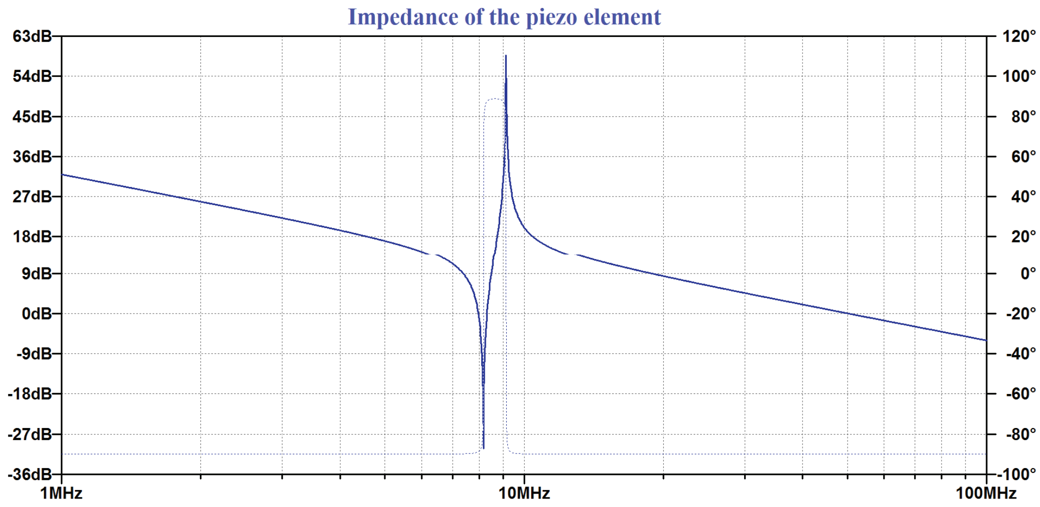


Fig. 4.16 Simulated impedance of the piezo element in Table 4.3.

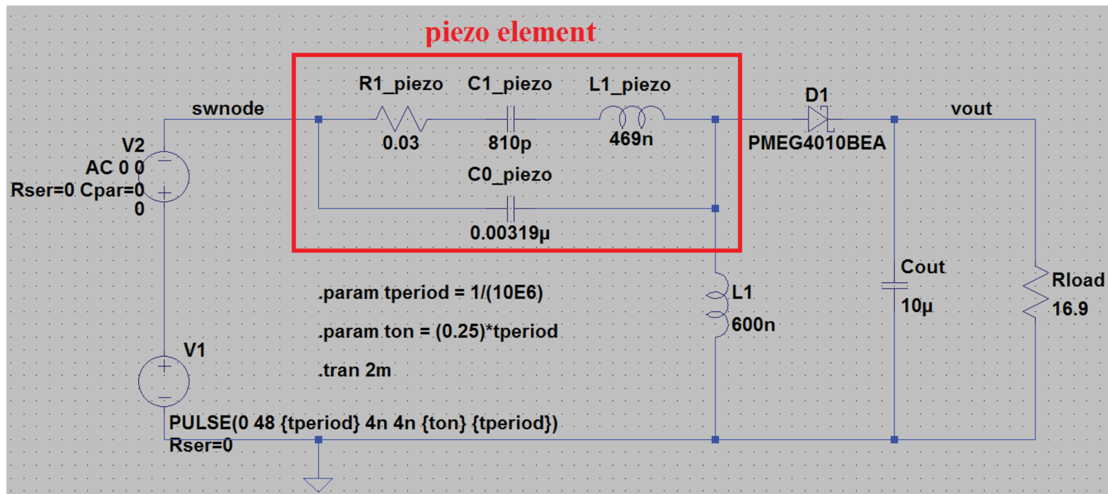


Fig. 4.17 Principle simulation of using the piezo elements in a proposed resonant converter. (Switching Frequency 10 MHz, Input voltage 48 V, Output voltage 13.6 V, Output power 10 W)

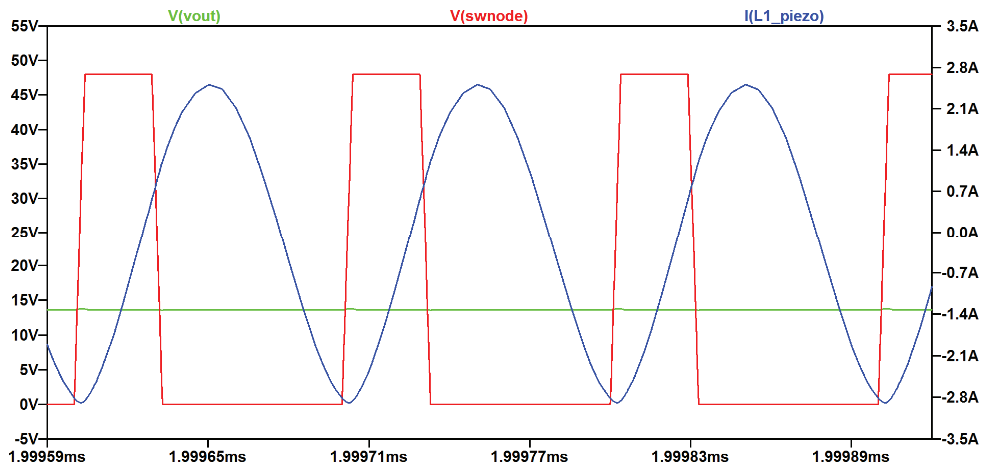


Fig. 4.18 Simulated waveforms of the proposed resonant converter in Fig. 4.17.

The simulated impedance of the piezo element in Table 4.3 is shown in Fig. 4.16. Note that the piezo element appears inductive between the two resonant frequencies. The piezo element is further simulated in a proposed resonant converter with a switching frequency of 10 MHz. The simulation configuration and the simulated waveforms are shown in Fig. 4.17 and Fig. 4.18, respectively. Afterwards, the piezo elements are manufactured, and the photograph of the samples is shown in Fig. 4.19. The equivalent electrical parameters of these samples are measured using a spectrum analyser, and the measurement results are summarized in Table. 4.4. The piezo elements show resonant frequencies around 8 MHz, as expected. However, the equivalent resistances are rather high and about an order of magnitude higher than the theoretically estimated value. Therefore, it is deemed that these piezo elements would cause high losses and may not be suitable for power converters in the scope of the research project.

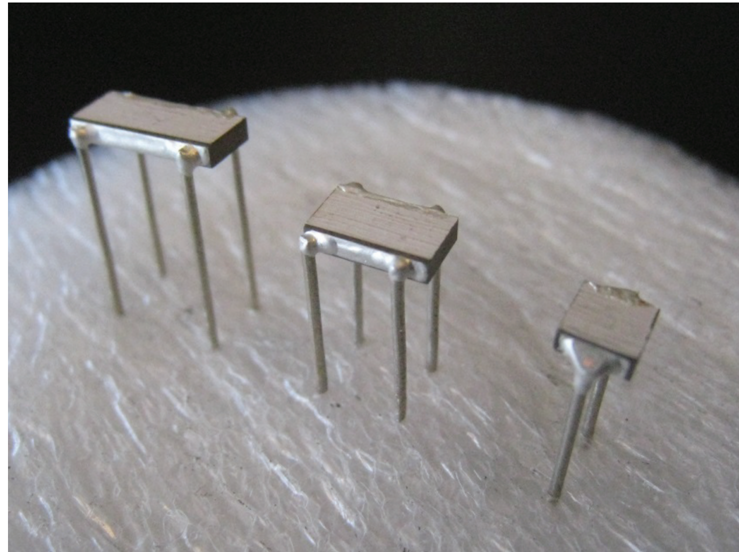


Fig. 4.19 Photograph of the manufactured piezo elements by Noliac [253].

Table 4.4 Measured equivalent parameters of the manufactured piezo elements by Noliac [253]

Dimensions	Sample No.	R1 (Ω)	L1 (nH)	C1 (pF)	C0 (nF)
Type 1	2	**3.70**	860	426	1.90
	3	**1.10**	1208	305	1.50
	4	**1.80**	882	411	2.10
	5	**1.34**	1400	260	1.40
	6	**1.17**	1440	256	1.50
Type 2	**11**	**0.35**	**529**	**680**	**3.52**
	12	**0.32**	**463**	**792**	**3.80**
	13	**0.25**	**456**	**818**	**3.79**
	14	**0.28**	**475**	**781**	**3.66**
	15	**0.28**	**456**	**800**	**3.86**
Type 3	21	**0.22**	244	1550	6.51
	22	**0.26**	302	1222	5.55
	23	**0.31**	291	1250	6.10
	24	**0.22**	263	1420	6.2

4.4 GaN-Based Resonant Power Stage Investigations

This section elaborates the investigations of new topologies of class DE converters. Class DE converters, in principle, have lower voltage stresses on the power switches compared to class E and class φ_2/class EF_2 converters. A conventional class DE converter topology is shown in Fig. 4.20. The DC input voltage is inverted into an AC current, and the AC current is then rectified back to a DC output voltage. There is a current interface between the inverter and the rectifier. By further analysis, the input impedance of a class DE rectifier that is composed of only diodes and capacitors appears basically capacitive for all frequencies, as shown in Fig. 4.21. However, to achieve zero voltage switching for the class DE half-bridge power stage, the impedance at the switching node looking backwards to the load is preferable to be inductive at the switching frequency. This means that the inductor in the resonance tank needs to provide the inductance not only for the inverter but also for the impedance matching of the rectifier. Since for a given switching frequency, more inductance is needed for the complete converter compared to what is needed for the inverter assuming a resistive rectifier at the switching frequency, the inductor used in the resonance tank tends to be physically large. The power density of the converter tends to be low, as inductors generally have lower energy densities than capacitors. Therefore, alternative class DE topologies are looked for. An initial design of a class DE converter with a voltage interface instead of a conventional current interface is shown in Fig. 4.22. This topology can be viewed as a class DE series-parallel inverter with a class E voltage-driven rectifier.

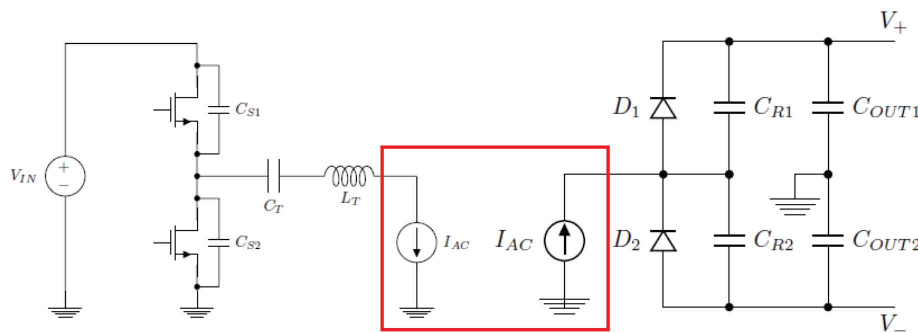


Fig. 4.20 A conventional class DE converter with a current interface [179].

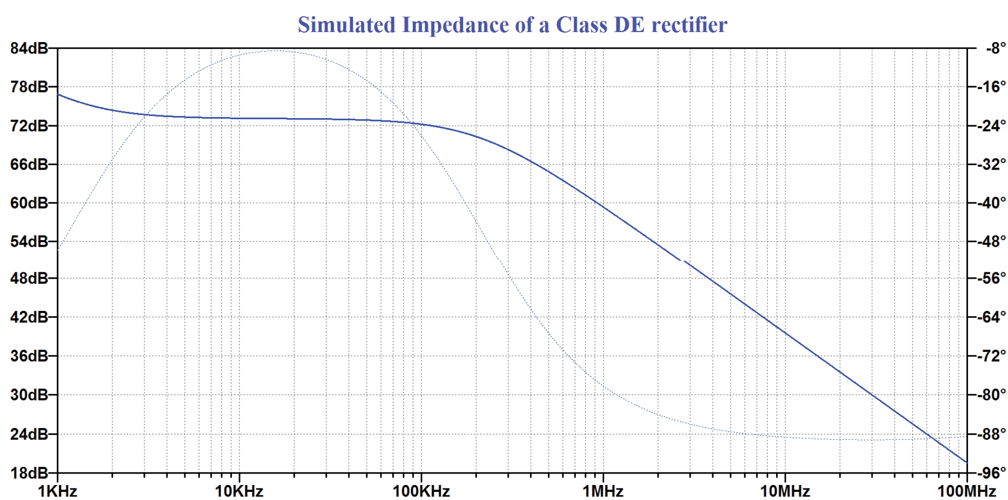


Fig. 4.21 Simulated input impedance of a class DE rectifier. The models used are NXP PMEG4010BEA diodes, KEMET 15 nF, 25 V, X7R, C_{OUT} capacitors, and 160 Ω load.

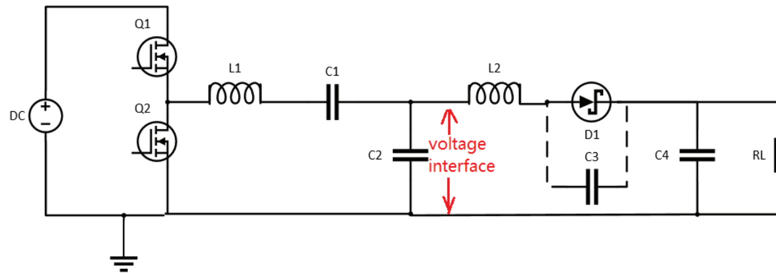


Fig. 4.22 An initial design of a class DE converter with a voltage interface.

For the initial design in Fig. 4.22, the voltage at the anode of the rectifier diode needs to be higher than the output voltage for the diode to be conducted. For an output voltage of 13 V, this requires high resonant voltages to be clamped at the anode of the rectifier diode, and it results in a generally low duty cycle of the rectifier diode, which causes high peak currents when the diode is conducted to deliver an average output power of 10 W. This means that the rectifier diode needs to handle both peak reverse voltages and peak forward currents. However, in practice, diodes have trade-offs between the voltage ratings and the current ratings. A workaround solution is to use multiple diodes in parallel to increase the current handling capability, but this lowers down the power density of the converter. Further practical trade-offs of didoes are shown in Table 4.5. This analysis is based on about 200 Schottky diodes on market with the same ratings of 40 V and 1A. Note that different manufacturers may specify at different operating conditions, and the Table 4.5 is made at the same conditions for fair comparison. The forward voltage and the total capacitance of Schottky diodes are typically with trade-off specifications. The top two Schottky diodes in Table 4.5 are finally chosen for the class DE converters design in this section.

Table 4.5 Top 3 selected 40 V, 1 A Schottky diodes
(Based on ≈200 diodes datasheets on market, last one is reference for general performance)

Manufacturer	Part No.	Peak Reverse Voltage	Average Rectified Current	Forward Voltage **At 1 A (Max)**	Total Capacitance **At 10 V (Typ)**	Remark
DIODES	1N5819HW	40 V	1 A	**450 mV**	**30 pF**	**tradeoff**
PANASONIC	DB2W40100L	40 V	1 A	**390 mV**	50 pF	**lowest**
TOSHIBA	CUS10S40	40 V	1 A	500 mV	**15 pF**	**lowest**
NXP	PMEG4010EP	40 V	1 A	490 mV	50 pF	general

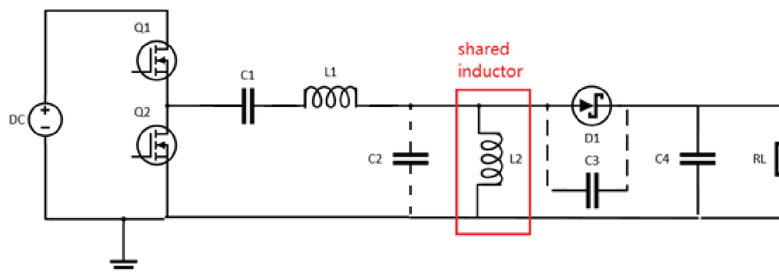


Fig. 4.23 Implemented design of a class DE series-parallel LCLC converter.

The implemented class DE converter uses a series-parallel LCLC topology, as shown in Fig. 4.23. This topology can be viewed as a class-DE series-parallel LCC inverter with a class E resonant rectifier, or it can be viewed as a class-DE LLC inverter with a shared-inductor with a class E resonant rectifier. A class DE inverter combines the advantages of a class D inverter and a class E inverter. A series-parallel resonance tank combines the advantages of a series-resonant tank and a parallel-resonant tank. The design specifications of this class DE series-parallel LCLC converter are shown in Table 4.6. The simulated waveforms are shown in Fig. 4.24 with zero voltage switching for both the high-side and low-side switches. The photographs of the implemented prototypes are shown in Fig. 4.25.

Table 4.6 Design specifications of the class DE series-parallel LCLC converter.

Parameters	Specifications
Input Voltage	48 V
Output Voltage	13 V
Output Power	10 W
Switching Frequency	5 MHz

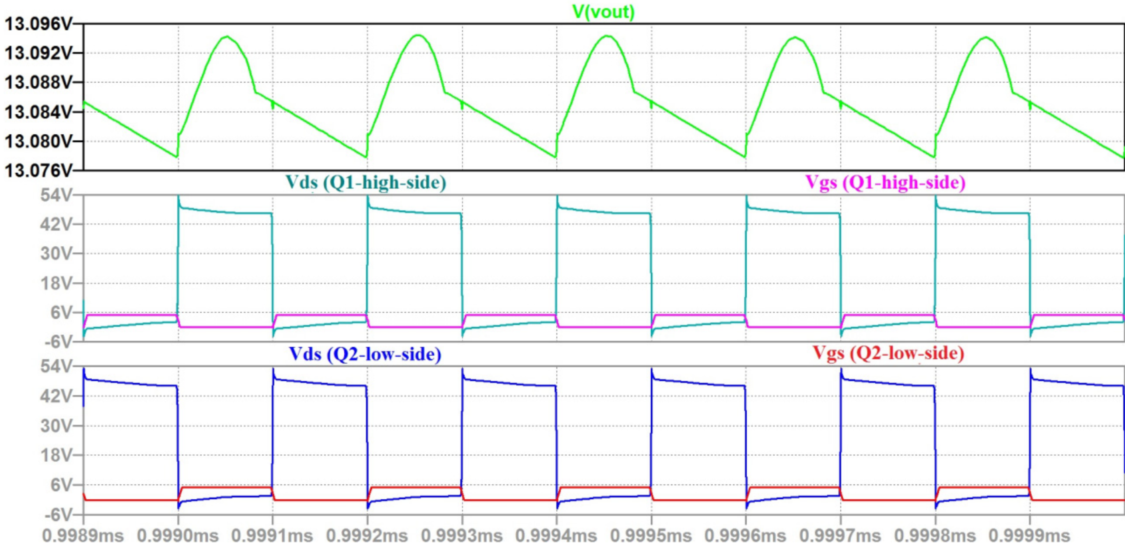


Fig. 4.24 Simulated waveforms of the class DE series-parallel LCLC converter. Zero voltage switching (ZVS) is shown for both high-side and low-side switches.

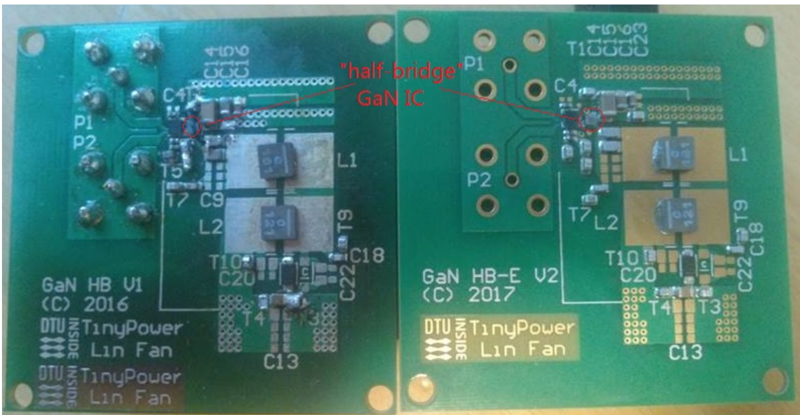


Fig. 4.25 Photograph of the implemented class DE series-parallel LCLC converters.

The engineering samples of EPC2107 were used for the prototypes. Experimental work was performed during the end of the year 2016. Through debugging processes and using the 2210-LS probe station, it was found that the FETs were not connected on-chip, whereas indicated in the datasheet. In Jan 2017, EPC confirmed that the block diagram in the datasheet was wrong, as shown Fig. 4.26. Further development of the class DE converter prototypes was generally stopped after the time delay caused by the fact that a "half bridge" die became a "dual" die.

Table 4.7 Selected key components for implementing the prototypes.

Components	Values	Comments
Q1/Q2 (2016)	100 V, 320 mΩ, 1.7 A EPC2107	Engineering sample "Half Bridge" was used. Datasheet was wrong, confirmed by EPC, Jan 2017.
Q1/Q2 (2018)	100 V, 390 mΩ, 1.7 A EPC2107	Final product "Dual with Sync Boot" on market. Block diagram has been corrected in datasheet.
Driver	100 V, LM5113	1.2 A source, 5 A sink, half bridge gate driver, TI
C1 (initial)	(3.9 nF ± 2 %) x 2	50V, NP0, 0805, Murata
C1 (tuning)	1.0 nF ± 1 %	50V, NP0, **0603**, Murata
C2 (tuning)	3.9 nF ± 2 %	50V, NP0, 0805, Murata
C2 (tuning)	1.0 nF ± 1 %	50V, NP0, **0603**, Murata
C3 (tuning)	3.9 nF ± 2 %	50V, NP0, 0805, Murata
C3 (tuning)	1.0 nF ± 1 %	50V, NP0, **0603**, Murata
C4 (initial)	10 µF ± 10 %	25 V, X5R, 0805, Murata
C4 (tuning)	2.2 µF ± 10 %	25 V, X5R, **0603**, Murata
L1 (initial)	**180 nH ± 20 %**	XFL4015-181, Coilcraft, Composite Core
L1 (tuning)	72-300 nH ± 20 %	XEL3515, XEL4014, XEL4020, Composite Core
L1 (tuning)	90-300 nH ± 5.2 %	2222SQ, Coilcraft, Square Air Core
L2 (initial)	**120 nH ± 20 %**	XFL4012-121, Coilcraft, Composite Core
L2 (tuning)	72-300 nH ± 20 %	XEL3515, XEL4014, XEL4020, Composite Core
L2 (tuning)	90-300 nH ± 5.2 %	2222SQ, Coilcraft, Square Air Core
D1 (initial)	40 V, 1A	390 mV, 50 pF, DB2W40100L, PANASONIC
D1 (tuning)	40 V, 1A	450 mV, 30 pF, 1N5819HW, DIODES
Cin (initial)	**10 µF** ± 10 %	50 V, X5R, **1206**, Murata, Input Decoupling Cap
Cin (initial)	**2.2 µF** ± 10 %	50 V, X5R, **0805**, Murata, Input Decoupling Cap
Cin (initial)	**0.47 µ** ± 10 %	50 V, X7R, **0603**, TDK, Input Decoupling Cap
Cin (tuning)	**10 nF** ± 5 %	50 V, X7R, **0402**, Murata, Input Decoupling Cap

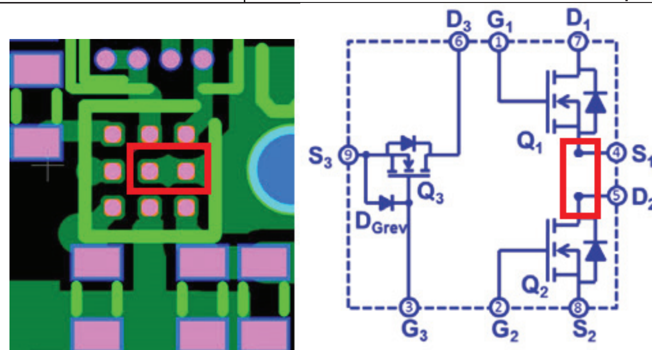


Fig. 4.26 EPC confirmed that the two pins were separated on-chip of EPC2107, and had to be connected externally. Block diagram was wrong in datasheet. Jan, 2017.

4.5 Summary

The chapter 4 summarizes the research work on the inductor-based low voltage converters. These converters are intended to be used as the output stage of a two-stage power converter architecture. First, a synchronous buck converter is implemented using the integrated high voltage power MOSFETs designed in the previous chapter. Second, the substrate current issues caused by the parasitic bipolar transistors in the lateral power MOSFETs in high voltage CMOS processes are investigated for resonant operations. Third, the piezo elements with two terminals are manufactured and investigated for potential operations as resonant tanks of resonant converters. Fourth, the design and implementation of the class-DE series-parallel LCLC resonant converters using the integrated GaN devices are presented.

5. Switched-Capacitor Converters (High-Voltage Input Converter)

This chapter concentrates on the design and implementation of high-voltage switched-capacitor converters. The high-voltage switched-capacitor converters are intended to be used as voltage conversion stages in a two-stage power converter architecture. The two-stage power converter architecture is shown in Fig. 5.1. This is a bi-directional architecture, and switched-capacitor converters are proposed to be in high voltage domains for both step-down and step-up power conversion, i.e. for a step-down converter, the input stage is a switched-capacitor converter and the output stage is an inductor-based converter. For a step-up converter [10], the two stages are interchanged, i.e. the input stage is an inductor-based converter and the output stage is a switched-capacitor converter. The thesis focuses on the step-down power conversion in the former case. The two-stage architecture combines the advantages of switched-capacitor converters and inductor-based converters. The hybrid-advantages are summarized in Table 5.1. The architecture separates the voltage conversion and the regulation [1], and exploits power switches into two categories [2], [7], [210], [211], [254], [255] i.e. slow high-voltage devices and fast low-voltage devices. The scaling of power devices versus voltages is previously discussed in chapter 2. At high impedance levels, the large and bulky magnetic components are avoided by using switched-capacitor converters, and high power density and high efficiency are both realized. At low impedance levels, the regulation function is handled by an inductor-based converter that can operate at high switching frequencies at low voltage levels. The high frequency operation reduces the passive component values and energy storage requirements, especially minimizes the demands upon magnetic components, thus a high power density can also be achieved in the output stage.

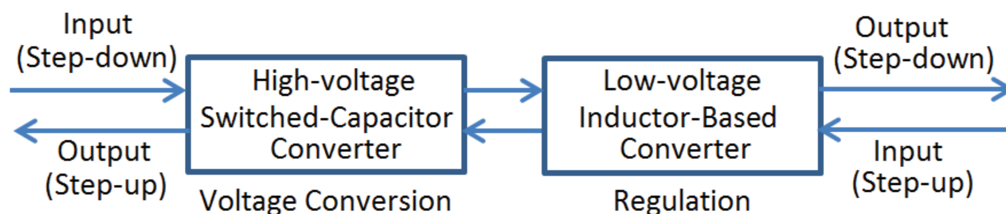


Fig. 5.1 Two-stage power converter architecture (bi-directional).

Table 5.1 Hybrid-advantages of the two-stage power converter architecture.

Two-stage power converter architecture (Step-down)	
Input/first stage	Output/second stage
High-voltage switched-capacitor converter	Low-voltage inductor-based converter
Voltage conversion	Regulation
Slow high-voltage devices (low-frequency)	Fast low-voltage devices (high-frequency)
High power density No magnetics (inductors/transformers)	High power density Small passive components (inductors/capacitors)
High efficiency	High control bandwidth
High impedance level (avoid using magnetics components)	Low impedance level (minimize magnetics components requirements)
The two stages are interchanged for setup-up power converters, i.e. input stage is low-voltage inductor-based and output stage is switched-capacitor based.	

5.1 High-Voltage Switched-Capacitor Power Stage

The goal of the switched-capacitor power stage design is to achieve both high efficiency and high power density at high-voltage low-power levels. This is in contrast to the previous research which focused on low-voltage and/or high-power levels. The design challenges of high-voltage switched-capacitor converters are not the same as low-voltage ones, e.g. especially switching losses become significant. The specifications of the 380 V, 10 W switched-capacitor converter prototypes are shown in Table 5.2. The characteristic impedances of the converter are considerably high (high-voltage low-current). The co-development of components, topologies, and architectures is necessary to achieve both high efficiency and high power density. The power stage proposed and used in this research work is shown in Fig. 5.2. The power stage consists of only 8 components, i.e. 2 transistors, 2 diodes, and 4 capacitors. The transistors and the diodes work in pairs (Q1/D1 and Q2/D2) to facilitate the energy transfer capacitor C2. The load current is primarily supplied by charging/discharging the capacitor C2.

Table 5.2 Specifications of 380V, 10 W switched-capacitor converter prototypes.

Parameters	Specifications
Input voltage	300 V - 380 V
Voltage conversion ratio	2:1
Maximum output power	10 W
Output voltage ripple	< 5 %
Efficiency	> 95 % above half rated power
Power density	> 4 W/cm^3

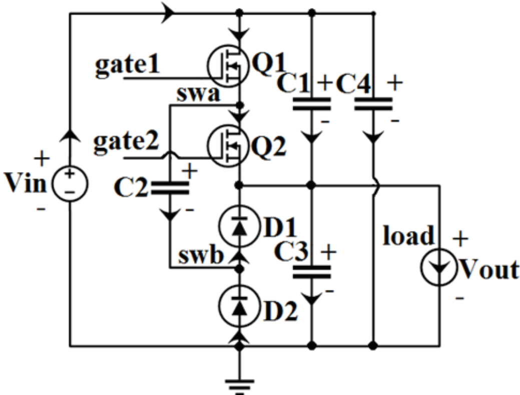


Fig. 5.2. The power stage of a 2:1 switched-capacitor DC-DC converter. [Appendix A.5]
For high-voltage low-power applications, with both high efficiency and high power density.

For implementing the design, wide band gap semiconductors of GaN and SiC devices are actively combined and utilized to improve both efficiency and power density. GaN switches are used for transistors implementation, and SiC diodes are used for diodes implementation. Analytical analyses of the comparison of GaN switches and SiC diodes are provided in [Appendix A.8], for conduction losses, switching losses, gating losses, land patterns, and total footprint areas. A key point is to understand that for the high-voltage low-power converters under consideration, the switching losses and the gating losses are significant, so the design needs to address the total loss rather than the conduction losses only. Another key point is that it is the total footprint area that is targeted, rather than the land patterns at the component levels.

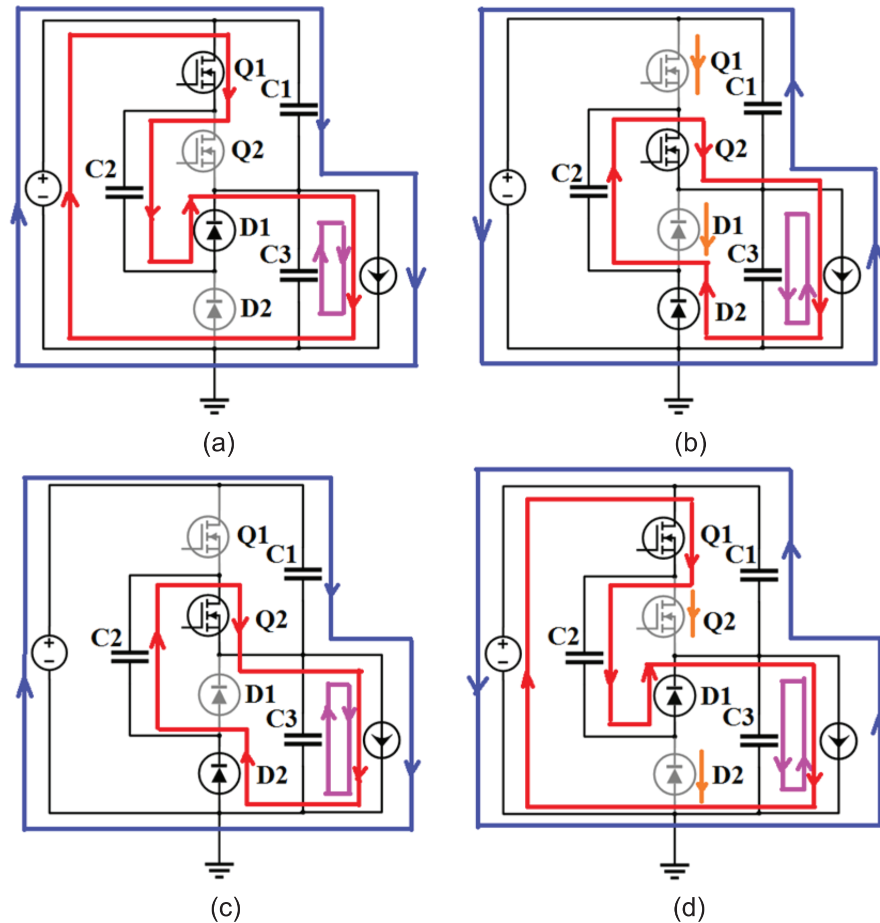


Fig. 5.3 Four states of the switched-capacitor power stage. [Appendix A.8]
Red is current loop of C2. Blue is current loop of C1. Pink is current loop of C3.
Orange is the small amount of current to charge the output capacitances of Q1/D1 or Q2/D2.
(a) Stage S1. (b) State S2. (c) State S3. (d) State S4.

Table 5.3 Summary of the four states operation of the power stage.
The output voltage ripple is at the double frequency of the switching frequency.

State	S1	S2	S3	S4
Q/D	Q1/D1 on	Q2/D2 turning on	Q2/D2 on	Q1/D1 turning on
C2	Charges	Discharges	Discharges	Charges
C1	Charges	Discharges	Charges	Discharges
C3	Discharges	Charges	Discharges	Charges
Vout	**Decreases**	**Increases**	**Decreases**	**Increases**

The operation of the switched-capacitor power stage is identified with four operating states S1-S4, as shown in Fig. 5.3. The charging/discharging operations of the capacitors C1-C3 are also summarized in Table 5.3. Note that the output voltage of the power stage equals to the voltage of the capacitor C3. For each of the 50% switching cycles (e.g. S2/S3 and S4/S1), the capacitor C3 charges and then discharges, so the output voltage increases and then decreases. The main contribution of this four states analysis is that with detailed charge/discharge transfer behaviours for each of the capacitors, it reveals that the output voltage ripple of the power stage is at the double frequency of the switching frequency of the control switches Q1 and Q2.

Three variant designs of the power stage are implemented. The final trade-off between conduction loss and switching loss is experimentally optimized with switching frequencies, as shown in Fig. 5.4. Then the efficiencies (without driver losses) versus the output powers are measured and shown in Fig. 5.5. Finally, the trade-off between the efficiency and the power density is validated, for which the peak efficiencies versus the power densities of the three variant designs are shown in Fig. 5.6. A peak efficiency of 98.6% and a power density of 7.5 W/cm^3 (123 W/inch^3) are achieved without heatsink or airflow at the room ambient temperature.

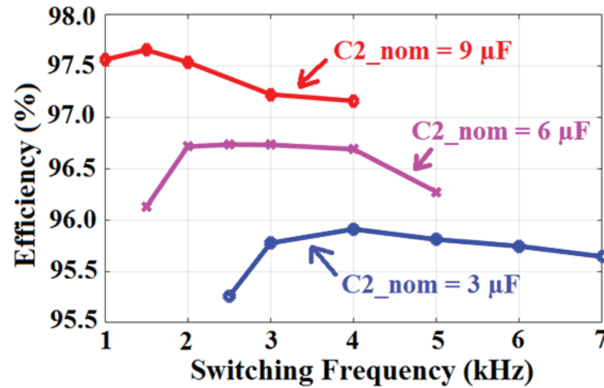


Fig. 5.4 Optimization of switching frequencies, i.e. trade-off between conduction loss and switching loss. 374 V input voltage, 10 W output power. [Appendix A.8]

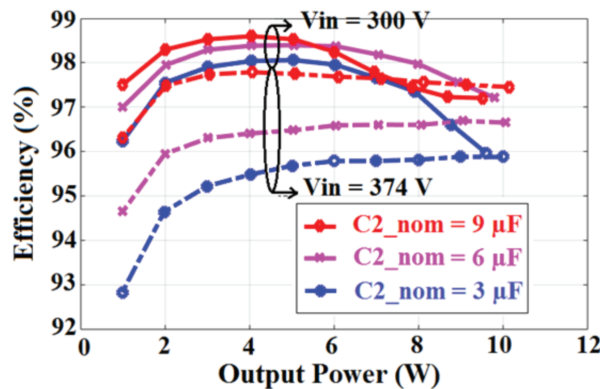


Fig. 5.5 Efficiency vs. output power. Three variant designs with optimized switching frequencies, i.e. 3 µF/4 kHz, 6 µF/2.5 kHz, 9 µF/1.5 kHz. [Appendix A.8]

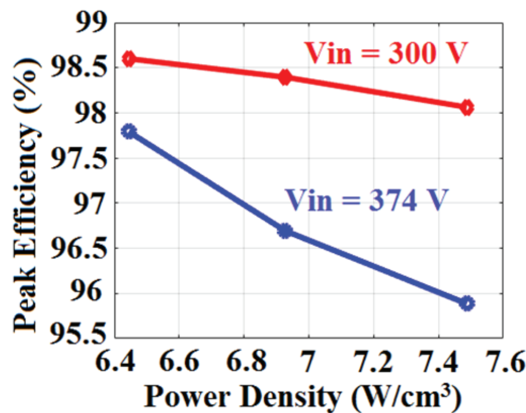


Fig. 5.6 Peak efficiency vs. power density, i.e. trade-off between efficiency and power density. [Appendix A.8]

5.2 High-Voltage Switched-Capacitor Driving Circuit

After the power stage is designed, driving the two high-side GaN switches also has challenges. First, conventional bootstrap circuits are not suitable for the power stage, because there are no low-side switches (other than D1 and D2) to charge the high-side bootstrap capacitors. Though the load current might be used in the charge path to charge a high-side bootstrap capacitor, recall that the switched-capacitor converter is for high-voltage low-power operations, the load current is relatively low, so the load current may not ensure an adequate gate-drive voltage. Second, three possible driving circuits are shown in Fig. 5.7. In Fig. 5.7 (a), digital isolators are used in series with conventional low-side gate drivers, as the case shown, 6 components are required for the driving circuit. In Fig. 5.7 (b), two single-channel isolated gate drivers are used, as the case shown, 4 components are used for the driving circuit. In Fig. 5.7 (c), an isolated half-bridge gate driver is used with an isolated supply with dual independent outputs for the individual outputs of the gate driver. The driving circuit uses only 2 components and is proposed.

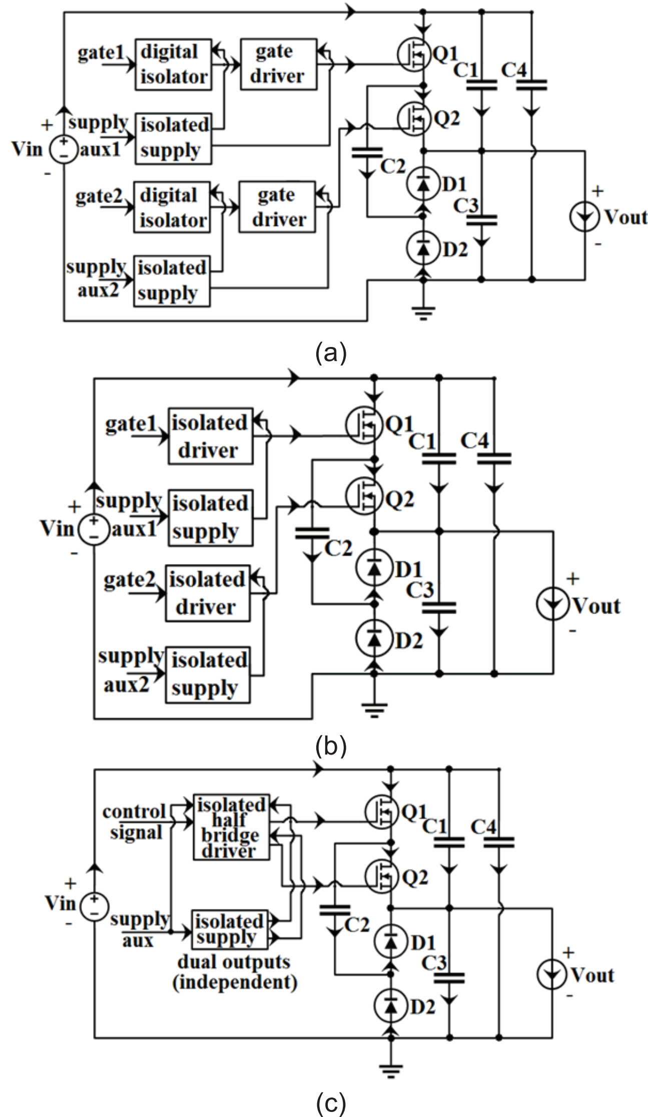


Fig. 5.7. Driving circuits for the power stage. (a) Digital isolators with low-side gate drivers. (b) Two single-channel isolated gate drivers. (c) Single isolated half-bridge gate driver. [Appendix A.5]

5.3 High-Voltage Switched-Capacitor Power Converter

From simulations [Appendix A.8] (and also later measurements), the peak dv/dt slew rates of the switching transients of the GaN and SiC devices can reach 100 V/ns level. Therefore, the capacitive-coupled gate driver Si8274GB1 with a minimum CMTI (Common Mode Transient Immunity) rating of 150 V/ns is selected, to prevent the control signals from losing signal integrity. The supply of the driver is transformer-based thus also isolated. The fully isolated high-voltage switched-capacitor converter is shown in Fig. 5.8. The measured efficiencies of the power stage and the total converter (including the power consumptions of the gate driver and the isolated supply) are shown in Fig. 5.9. The thermal image of the switched-capacitor converter measured after one hour full-power operation is shown in Fig. 5.10. For the power stage, a full-load efficiency of 98.3 % and a power density of 7.9 W/cm^3 (130 W/inch^3) are achieved. For the total power converter (including driver and supply), a full-load efficiency of 97.6 % and a power density of 2.7 W/cm^3 (45 W/inch^3) are achieved.

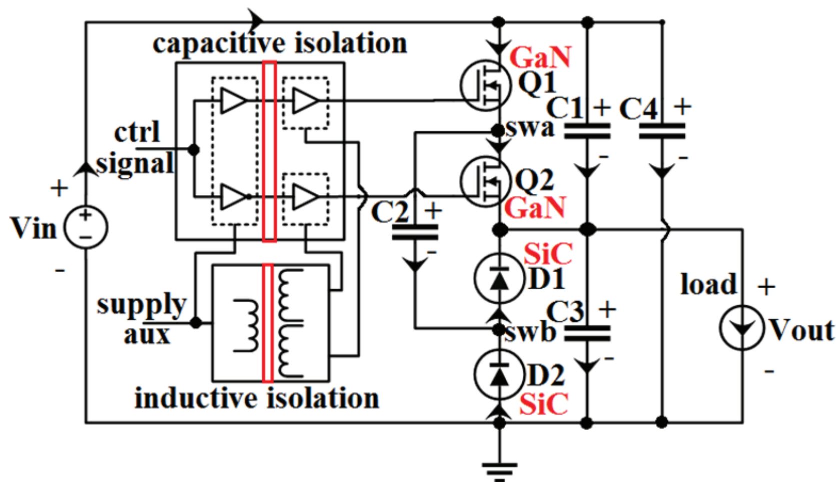


Fig. 5.8 A high-voltage switched-capacitor DC-DC converter. [Appendix A.8]
For high-voltage low-power applications, with both high efficiency and high power density.

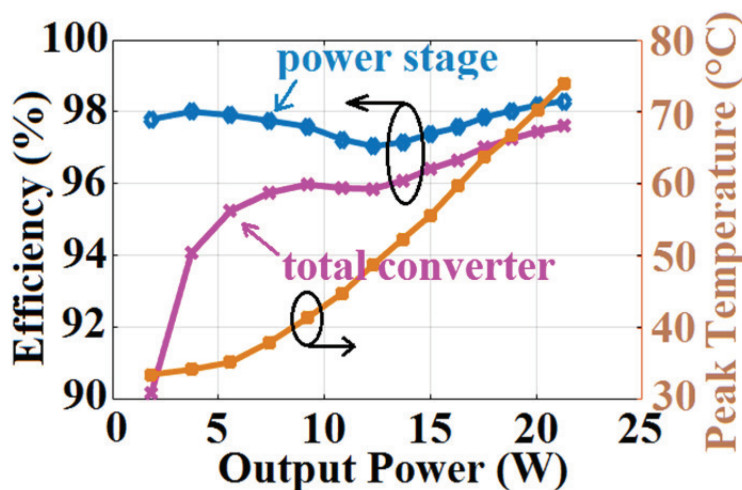


Fig. 5.9 Efficiencies of the power stage and the total converter (including gate driver and isolated supply) versus output powers. And peak temperatures of the hottest spot on PCB. [Appendix A.5]

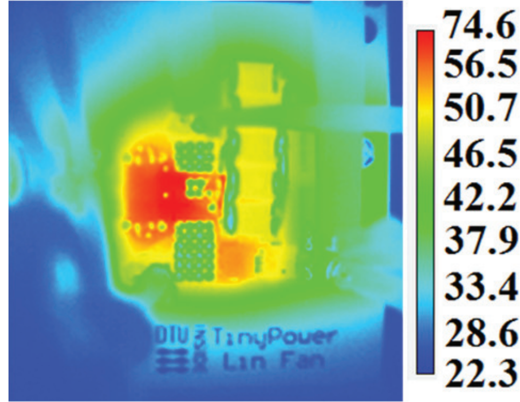


Fig. 5.10 Thermal image (°C). 380 V input voltage, 21.3 W output power.
No heatsink, no airflow, measured after one hour full-power operation. [Appendix A.5]

5.4 Asynchronous-Switched-Capacitor Power Converter

As previously discussed, for high-voltage low-power switched-capacitor converters, switching losses become a major concern and challenge. New design concepts are anticipated to emerge. An example is the concept of Asynchronous-Switched-Capacitor (ASC) proposed in this research work [Appendix A.7]. The ASC operation is named when the switches can be operated with uncorrelated frequencies, with unnecessary phase/clock synchronization of the control signals. A 380 V input voltage, 6 W output power, 4:1 conversion ratio switched-capacitor converter is shown in Fig. 5.11 and used to experimentally validate the concept. In this switched-capacitor converter, the total switching loss of the switches (Q1-Q4) related to charging/discharging the output capacitances C_{oss} is calculated in (5.1). For the conventional switching scheme, all the switches (Q1-Q4) are operated with a single common frequency, and it shows that the switching losses are not evenly distributed. If the switches are of the same type, the switching losses of the switches Q1 and Q2 are more than two times of the switching losses of the switches Q3 and Q4, which takes the nonlinearities of the output capacitances C_{oss} into account as well.

$$P_{sw_Coss_total} \cong f_{Q1_Q2} \cdot V_{IN} \cdot \int_0^{V_{IN}/2} C_{oss}(v_{DS}) \cdot dv_{DS} + f_{Q3_Q4} \cdot \left(V_{IN}/2\right) \cdot \int_0^{V_{IN}/4} C_{oss}(v_{DS}) \cdot dv_{DS} \quad (5.1)$$

Furthermore, for a given switched-capacitor converter design, the optimal switching frequencies for the minimal total losses (switching losses and conduction losses) depend on the operating current levels, hence depend on the specific characteristic impedance levels. Therefore, the conventional switching scheme does not optimally address the switching losses (hence the total losses), which are significant for high-voltage low-power switched-capacitor converters. For an optimal efficiency of the converter, the switches are preferably operated at different frequencies, and if the switching frequencies are not necessarily correlated or the phases/clocks are not necessarily synchronized, it also mitigates the timing requirements of the control signals with high tolerance of phase-shifts. This concept of Asynchronous-Switched-Capacitor is experimentally validated with measurement results. The measured efficiencies versus the switching frequencies of the switches Q3 and Q4 are shown in Fig. 5. 12, while the switching frequency of the switches Q1 and Q2 is kept constant at 1 kHz. It shows that the total efficiency is improved by 4 %, if the switches Q3 and Q4 are operated with a switching frequency of 3.5 kHz. The ASC switching scheme is also compared with the conventional switching scheme with

or without phase-shifts between the control signals, and the measured efficiencies versus the output powers are shown in Fig. 5.13. The proposed ASC switching scheme significantly improves the efficiencies across the output power range compared to the conventional switching scheme, with an efficiency improvement of 4 % at the full-power of 6 W. In addition, the ASC switching scheme also reduces the peak-to-peak output voltage ripple by 39 % compared to the conventional switching scheme. A peak efficiency of 95.4 % is achieved for the 380 V, 6 W, and 4:1 conversion ratio switched-capacitor DC-DC converter.

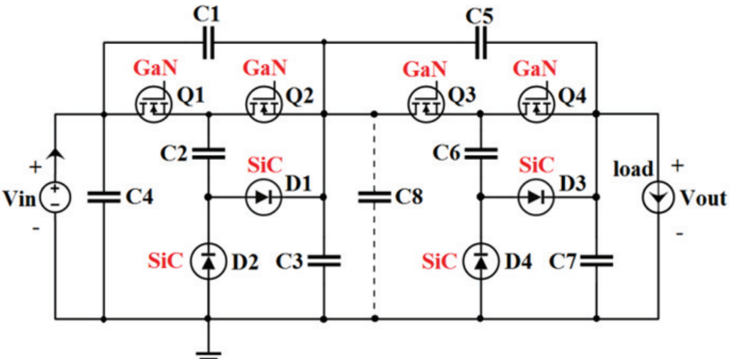


Fig. 5.11 An asynchronous-switched-capacitor DC-DC converter.
380 V input voltage, 4:1 voltage conversion ratio. Dotted line means optional. [Appendix A.7]

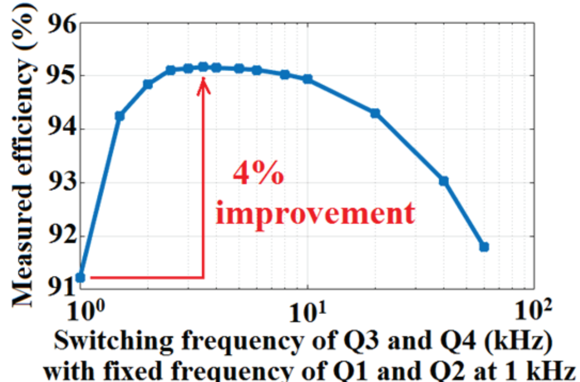


Fig. 5.12 Efficiency versus the switching frequency of Q3/Q4.
The switching frequency of Q1/Q2 is fixed at 1 kHz. [Appendix A.7]

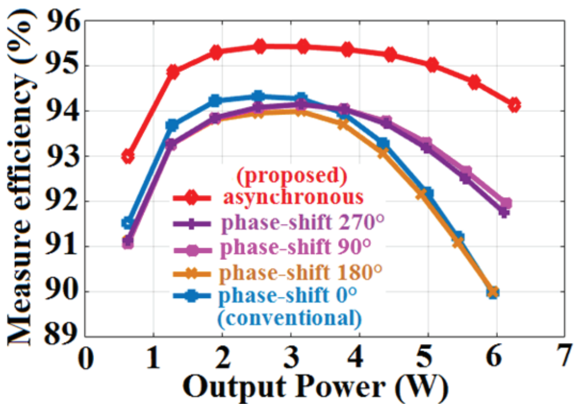


Fig. 5.13 Efficiency versus output power. [Appendix A.7]
The phase-shift is defined as Q3/Q4 referred to Q1/Q2, when Q1-Q4 have the same frequency.

5.5 Summary

The chapter 5 summarizes the research work on the high voltage switched-capacitor converters. A two-stage power converter architecture is proposed and the high voltage switched-capacitor converters are intended to be used as the input stage of the two-stage power converter architecture. First, a switched-capacitor power stage using both GaN and SiC devices is designed and implemented, and the four states analysis reveals that the output voltage ripple is at the double frequency of the switching frequency. The trade-off between the conduction loss and the switching loss and the trade-off between the efficiency and the power density are experimentally validated. Second, different isolated driving circuit topologies for the power stage are compared and a compact isolated half-bridge driving circuit is proposed. Third, a total power converter including its driver and isolated supply achieves a full-load efficiency of 97.6 % and a power density of 2.7 W/cm^3 based on the boxed volume. Fourth, a concept of Asynchronous-Switched-Capacitor (ASC) is proposed, which improves the efficiencies of the power converter for the entire power range and reduces peak-to-peak output voltage ripples.

As previously discussed in the chapter 2, the design challenge is the combination of the high-voltage and low-power requirements, i.e. a converter with a higher characteristic impedance level is more challenging to design than a converter with a low characteristic impedance level. The switched-capacitor converters designed in this research work have about an-order-of-magnitude higher characteristic impedance levels than the state-of-the-art high-voltage switched-capacitor converters. The comparison of these converters is summarized in Table 5.4.

Table 5.4 Comparison of state-of-the-art high-voltage switched-capacitor converters.

	Case 1	Case 2	Case 3	Case 4	Case 5
Year	2015	2015	This work		
Reference	[2]	[215]	Appendix A.8	Appendix A.5	Appendix A.7
Conversion ratio	2:1	8:1	2:1	2:1	4:1
Input Voltage	**200 Vdc**	**200 Vdc**	**380 Vdc**	**380 Vdc**	**380 Vdc**
Output Power	30 W	53 W	10 W	21.3 W	6 W
Impedance level	≈ 1333 Ω	≈ 755 Ω	≈ 14440 Ω	≈ 6779 Ω	≈ 24066 Ω
Normalized Impedance level	**1.8x**	**1x**	**19.1x**	**9.0x**	**31.9x**

6. Conclusions

The size, weight, and cost reductions of power converters are continuously driven by the demand of industrial and consumer electronics, while the performances such as the efficiency and the power density are simultaneously driven high. The state-of-the-art research shows that the development of the efficient integrated off-line power conversion is currently in its infancy. This research work focuses on the DC-DC power conversion, and a systematic development on components, topologies, and architectures has been conducted.

For components development, 100V integrated power MOSFETs are analysed, designed, and implemented in a SOI process. A small-signal modelling method is proposed to systematically analyse the nonlinear parasitic capacitances of the power MOSFETs in different states, i.e. off-state, sub-threshold region, and on-state in the linear region. It is found that the parasitic capacitances (from either the gate or the drain) towards the bulk can dominate over the parasitic capacitances towards the source for the lateral power MOSFETs. The nonlinear figure-of-merits (FOMs) are also systematically analysed for different operating conditions. It shows that for a given power MOSFET, the FOMs are lowered by 1.3-18.3 times and improved by 22-95 % by optimizing the voltage and current conditions with quasi-zero voltage switching. Four layout structures are proposed and analytically compared for the layout parasitic capacitive coupling effects. It shows that parasitic capacitances of on-chip interconnections could dominate over intrinsic capacitances of power devices. The analysis also shows that the layer-to-layer capacitive coupling could dominate over the side-by-side capacitive coupling. In addition, package and PCB parasitics are qualitatively analysed and summarized. The analysed examples show that the package parasitics contribute 0.2-4.6 times the switching loss of a power device die, and that di/dt-induced turn-on, dv/dt-induced turn-on, gate voltage overshoot, gate voltage ringing can be simultaneously mitigated by minimizing package and PCB parasitics (e.g. the common-source inductance), which also reduces converter power losses.

For topologies and architectures development, both inductor-based and switched-capacitor converters are investigated, designed, and implemented, and a two-stage power converter architecture is proposed. The inductor-based converters are low voltage output converters. A synchronous buck converter is implemented using the integrated power MOSFETs with efficiencies around 93 %. For resonant power stages in high voltage CMOS processes, there are substrate current issues caused by the parasitic bipolar transistors in the lateral power MOSFETs. For potential operations as resonant tanks of resonant converters, the piezo elements with two terminals are manufactured and investigated. The class-DE series-parallel LCLC resonant converters using integrated GaN devices are investigated. The switched-capacitor converters are high voltage (up to 380 V) input converters. Both GaN and SiC devices are utilized to address the significant switching losses at high-voltage low-power levels. A 10 W power stage design shows a peak efficiency of 98.6 % and a power density of 7.5 W/cm^3. Different isolated driving circuit topologies are analysed and compared, which contributes to a 21.3 W completed power converter with a total efficiency of 97.6 % at the full-load and a power density of 2.7 W/cm^3 based on the boxed volume. An Asynchronous-Switched-Capacitor (ASC) switching scheme is proposed, with which a 380 V, 6 W, 4:1 conversion ratio switched-capacitor converter reaches a peak efficiency of 95.4 % and reduces peak-to-peak output voltage ripples.

The research work contributes to the analysis and design of the integrated high voltage power MOSFETs for on-chip integrated power converters, and contributes to the design and implementation of the switched-capacitor based converters and the inductor-based converters with a two-stage power conversion architecture for discrete off-line power converters. Future work towards the Power Supply on Chip (PwrSoC) and the efficient integrated off-line power conversion is anticipated.

7. Future Work

The power supply industry is currently at an inflection point with a clear move away [256] from conventional power converter modules towards products based more directly on semiconductor and IC technologies. The greater integration and higher power density motivated by space-constrained and miniaturized applications are now beginning to be delivered in integrated hardware based on Power Supply in Package (PSip) and its evolution, i.e. Power Supply on Chip (PwrSoC) [15], as replacements for conventional printed circuit board (PCB) power supply configurations [256]. This research work is just a little part of the power supply evolution. There are multiple fields of future work that is related to this work. The future development of the work is closely related to components and topologies, with advanced architectures still to emerge.

Device Parasitics: The modelling and characterization of transistors from Very High Frequencies (VHF) to Ultra High Frequencies (UHF) and other frequency bands above 1 GHz definitely contribute to the development towards increasing switching frequencies. Industrial datasheets typically do not specify parasitic parameters or only specify limited parasitic capacitance values that are normally measured at 1 MHz. Research work on modelling and characterization of transistors is already in GHz ranges [232], [257]-[260]. By using S-parameters, characterization of transistors can be up to 220 GHz [257]. The characterization of nonlinear gate resistances [232] is of top interest for resonant gate drivers of resonant converters. The circuit-oriented utilization of nonlinear parasitic capacitances in power converters is recently reported and worth attention [261]. The nonlinear parasitics are the essential parts of loss modelling of power transistors [262].

Package Parasitics: The parasitic inductances and resistances of packages are one of the limiting factors of increasing switching frequencies. The future work on the characterization of transistors also relies on the characterization of packages. It is worthy to mention that one of the 2017 first place winners of “IEEE Transactions on Power Electronics Prize Paper Award” is regarding to research on packaging, i.e. “A New Package of High-Voltage Cascode Gallium Nitride Device for Megahertz Operation” [263] which was carried out by CPES, Virginia Tech.

Audio Power IC: Audio power amplifiers [264] are one of the potential application areas of power ICs. Compared to off-line power converters that are targeted in this research project, integrated or partly integrated audio power amplifiers normally have relatively lower input voltages but dramatically higher maximum output powers (with high dynamic ranges between the lowest and highest output powers). Note that the recent advances in audio power ICs [265]-[271] including high voltage (> 10 V) level shifters [272] are typically not published in the field of power electronics. The processes commonly used are SOI processes [265], [266], [269], [270] with supply voltages of 30-85 V, and BCD (Bipolar-CMOS-DMOS) processes [267], [268], [271] with supply voltages of 30-40 V. In the December 2016 issue of the IEEE JSSC (Journal of Solid-State Circuits), a research work on audio power IC [268] reported a part of similar substrate current issues as what is investigated in the chapter 4.2. In this publication, the “extra-large substrate noise problem” was carefully dealt with guard rings and isolation structures. In this research project, isolation structures were also heavily investigated and implemented for the SOI process used in the chapter 3, but due to confidential process information they are not included in the thesis.

GaN IC: 200 MHz half-bridge DC-DC converters are already reported in 2013 [273], [274]. With the high thermal conductivity of silicon-carbide (SiC) substrates, GaN-on-SiC processes are later used for half-bride DC-DC converters [11], [275]-[280], and a 400 MHz half-bridge DC-DC converters with a 20 V input voltage is reported [277]. The applications of GaN ICs are for example wireless power transfer [280] and smartphone chargers [281]. During 2015-2016, in this research project, a Master thesis project [282] with the author as one of the supervisors conducted research on “Resonant Power Converter Implemented in a Gallium Nitride Foundry Process” using a 100 nm, 25 V GaN-on-Si (in 2015), 40 V GaN-on-SiC (in 2020) process [283]. The maximum drain-source voltage of 25 V of the process is considerably low for off-line converters in this project, but for future research projects, it may be worthy of considerations.

Advanced Switched-Capacitor Converters (e.g. bi-directional, multi-port, set-up, PFC): Theoretically, the fundamental switched-capacitor converters are bi-directional converters. There are potentially many applications for the bi-directional feature. For example, switched-capacitor converters may be adopted into three-port converters [284], [285], or power factor correction circuits [286], [287]. Stacked switched-capacitor [288], [289] and/or switched-capacitor power combining converters [290], [291] are opening other degrees of the applications.

Hybrid Converters (e.g. Resonant-Switched-Capacitor): Many state-of-the-art resonant-switched-capacitor converters are already summarized in the chapter 2, e.g. [16]-[22], [205], [216]-[229]. In March 2017, Google [229] proposed a switched-capacitor based power conversion architecture. This has brought tremendous attention of researchers in the field of magnetics-oriented converters. In the December 2017 issue of “IEEE Power Electronics Magazine”, the discussions of the switched-capacitor based power conversion are heavily reported [292]. In fact, resonant-switched-capacitor converters were already published in 1998 [217]. Additionally, resonant gate drivers for switched-capacitor converters were also published in 1998 [293]. Nevertheless, hybrid structures of switched-capacitor and magnetics are predicted as one of the future research trends by Prof. J. W. Kolar from ETH [216] in 2017.

Regarding VHF (Very High Frequency): VHF is defined as the frequency band of 30-300 MHz [294], by both IEEE (Institute of Electrical and Electronics Engineers) and ITU (International Telecommunication Union). Numerous DC-DC converters in this frequency band were reported, and some of the converters are summarized in the chapter 2. Beyond this frequency band, there are also many publications, e.g. a 400 MHz half-bridge DC-DC converter as mentioned above, a 660 MHz fully integrated DC-DC converter [75], and a 480 MHz multi-phase interleaved buck DC-DC converter which was already reported in 2004 [94]. In 1999, a 4.5 GHz microwave frequency DC-DC power converter was published almost two decades ago [35], [295]. The switching frequency, by itself, is not an indicator of converters performance. There are many other aspects of practical trade-offs, e.g. input voltage (range), output power (range), efficiency (loss), power density (volume), weight, cost, reliability (failure rate), design procedure (time to market), and so on. For switched-capacitor converters, switching frequencies can be increased with resonant operations, e.g. resonant-switched-capacitor converters, as discussed above. The attention is that the additionally introduced inductance(s) for resonant operations are not expected to make the volume and the power density worse or induce additional power losses, considering that switched-capacitor converters already have high efficiencies. PCB and/or package parasitic inductances are of research interest to realize resonant operations of switched-capacitor converters with minimum impacts on power densities.

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Appendix A Publications

A.1. Publication (journal and conference)

This is the final published version, also known as the version of record. It is based on the open access policy: the journal provides immediate open access to its content on the principle that making research freely available to the public supports a greater global exchange of knowledge.

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And

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Nonlinear Parasitic Capacitance Modelling of High Voltage Power MOSFETs in Partial SOI Process

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Abstract—**State-of-the-art power converter topologies such as resonant converters are either designed with or affected by the parasitic capacitances of the power switches. However, the power switches are conventionally characterized in terms of switching time and/or gate charge with little insight into the nonlinearities of the parasitic capacitances. This paper proposes a modelling method that can be utilized to systematically analyse the nonlinear parasitic capacitances. The existing ways of characterizing the off-state capacitance can be extended by the proposed circuit model that covers all the related states: off-state, sub-threshold region, and on-state in the linear region. A high voltage power MOSFET is designed in a partial Silicon on Insulator (SOI) process, with the bulk as a separate terminal. 3D plots and contour plots of the capacitances versus bias voltages for the transistor summarize the nonlinearities of the parasitic capacitances. The equivalent circuits in different states and the evaluation equations are provided.**

Index Terms—**Nonlinear circuits; parasitic capacitance; power MOSFET; silicon-on-insulator.**

I. INTRODUCTION

Reductions in size, weight, and cost of power supplies are continuously being demanded by the miniaturization trend of industrial and consumer electronics [1]. The reduction of size can in principle be achieved from two perspectives: passive components and active components. Reducing the size of the passive components is related to circuit topologies with increased switching frequencies. Resonant power converters such as class DE inverters that have been developed over the years [2], [3] contribute to the size reduction of passive components, and to further reduce the size of power supplies, integrating the active components on-chip must also be considered:

First, high voltage power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) used as main switches in power converters normally have a cellular structure composed of a mesh with parallel connected unit cells [4] to satisfy the stringent on-state resistance requirements over high temperatures and low overdriving conditions. Modern discrete power devices are constructed using a vertical channel structure where the drain and source terminals are placed on the opposite sides of a wafer, so that the distance between the two terminals can be reduced to improve the electrical performance. However, these vertical devices are not suitable for monolithic integration [4] and lateral devices where both drain and source are placed on the top side of a wafer are still the major trend for integrating the power devices with control and driver circuits on the same die. The conventional Complementary Metal–Oxide–Semiconductor (CMOS) technologies are not suitable for integrating power switches whose bulk terminals may operate at highly different voltage potentials. Silicon on Insulator (SOI) processes can take advantage of the buried oxide for dielectric isolation in vertical direction, together with the Deep Trench Isolation (DTI) and the Shallow Trench Isolation (STI) technologies for dielectric isolation in horizontal direction, so that integrating power devices at different voltage domains becomes feasible. To relax the distribution of the electric field in a pure SOI process and lead the fringing electric field to proper termination, handle wafer contacts are needed through the buried oxide for high voltage power devices. In Section II, a high voltage power MOSFET is designed as an array of parallel connected unit cells in a partial SOI process.

Second, nonlinearity analyses of the parasitic capacitances of the power MOSFETs can benefit power converter designers when investigating new topologies such as resonant power converters where the parasitic capacitances affect or participate in the operation of the resonant tank. The dynamic characteristics of power MOSFETs are often evaluated in terms of switching time and gate charge, and one of the reasons for this is the difficulties of analysing the nonlinearities of the parasitic capacitances. Industrial datasheets typically specify the input capacitance C_{iss} and the output capacitance C_{oss} with gate shorted to source [5], [6]. However, such information is very difficult to utilize and sometimes even misleading because the power MOSFETs normally operate under different conditions in real applications. Therefore, establishing a proper way to characterize the nonlinear parasitic capacitances is imperative. In Section III, a small-signal modelling method is proposed to address the nonlinearity analysis that is applicable for different transistor states: off-state, sub-threshold region, and on-state in the linear region. The detailed nonlinear parasitic capacitance analysis using the

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proposed transistor model is divided into 3 sub-cases. In Section IV, the parasitic capacitances looking into the gate terminal are investigated. In Section V, the parasitic capacitances looking into the drain terminal with the transistor in off-state are investigated. In Section VI, the parasitic capacitances looking into the drain terminal with the transistor in on-state in the linear region or in the sub-threshold region are investigated. Section VII provides the conclusions of this paper.

II. A POWER MOSFET IN PARTIAL-SOI PROCESS

The high voltage power MOESFET modelled in this paper is designed in a 0.18 μm partial SOI process from X-FAB Silicon Foundries. One of the most important advantages of this process is that the SOI wafer can be combined with the deep trench isolation, forming full 3D (three-dimensional) isolation (dielectrically) between on-chip power switches.

The selected type of power MOSFET has a breakdown voltage between drain and source in excess of 110 V, a maximum operating voltage between drain and source of 100 V, a maximum operating voltage between gate and source of 5.5 V, and a minimum channel length of 0.5 μm.

The high voltage power MOSFET is designed as follows: it is composed of 96 unit cells which are connected in parallel, and each unit cell has an equivalent gate width of 100 μm, calculated as 10 fingers, each of which has a gate finger width of 10 μm. The gate length is 0.5 μm for all cells. The total of the 96 parallel connected unit cells (16 rows and 6 columns) constitutes a single, large, high voltage power MOSFET. The layout of the cell array is shown in Fig. 1. The die area is 0.2948 mm^2: the length is 692 μm and the width is 426 μm. This area includes all transistor unit cells and all deep trench isolation structures, but the associated chip pads and the electrostatic discharge (ESD) protection circuits are not shown here and are not included in the area. The silicon design has been sent to fabrication.

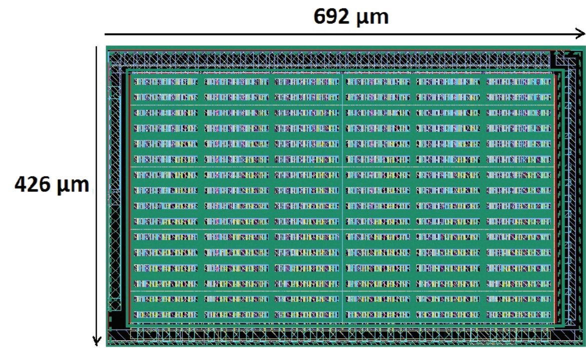

Fig. 1. A high voltage power MOSFET designed in a partial SOI process.

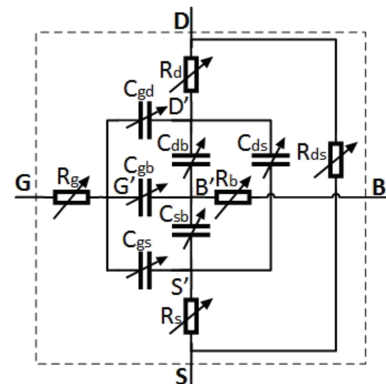

Fig. 2. Proposed small-signal model of power MOSFETs (off-state, sub-threshold region, and on-state in the linear region).

III. MODELLING OF POWER MOSFETS

For modelling the high voltage power MOSFETs in a partial SOI process, especially the nonlinearities of the parasitic capacitance, a small-signal modelling method is used and the proposed small-signal model of the power MOSFETs is shown in Fig. 2.

There are 4 distinct characteristics of the proposed model. First, the bulk terminal is modelled as a separate terminal. A conventional power MOSFET normally shorts the bulk terminal to the source terminal, and the corresponding gate capacitance is the sum of the gate-source capacitance and the gate-bulk capacitance.

The only way to separate the contributions of the nonlinearities of the capacitance towards bulk and source is to model the bulk as a separate terminal. Second, the proposed model includes R_{ds} as a nonlinear resistance (depending on the gate-source voltage and the drain-source voltage), both in the off-state operation and in the on-state operation, including the nonlinear behaviour in the sub-threshold region, whereas conventional modelling of power MOSFETs normally includes the nonlinear capacitances only in the off-state operation.

Third, every single component in the proposed model is nonlinear (dependent on DC bias voltages). This does not only apply to the nonlinear capacitances but also apply to the nonlinear resistances. For example, the gate resistance may present nonlinear behaviour [7]. Fourth, the parasitic resistances are specifically included for drain, source, and bulk terminals. Although the values may be very small and can sometimes be neglected, in principle, the parasitic resistances always physically exist and contribute to the nonlinearities.

IV. NONLINEAR CAPACITANCES LOOKING INTO THE GATE TERMINAL

One of the key points in evaluating the nonlinearities in the modelling of power MOSFETs is to understand that the model is merely an equivalent circuit, and nonlinear capacitors in the model are not physical capacitances [8], [9], although the model may resemble the physical structures. The real transistor characteristics are much more complex than any simplified model with lumped components, and certain parts of the nonlinearities of the real transistor characteristics which do not correspond directly to the lumped components in the circuit model have to be incorporated into the descriptions of the components in the simplified equivalent model. Therefore, the resulting equivalent values of the components in the model may appear more nonlinear than the physical characteristics of a certain part of the structure. The equivalent model is used to understand and give insight into the electrical behaviour of power MOSFETs, and trying to establish a perfect match between the electrical model and the physical structures would lead to a misconception.

When all terminals of the power MOSFET are biased at fixed DC voltages, the equivalent circuit model of the

transistor shown in Fig. 2 can be further simplified in different ways, depending on which terminal of the transistor to look into, what state the transistor is in (off-state, sub-threshold region, or on-state in the linear region), and at what frequency to evaluate the model. The proposed model uses a small-signal method, and the characterization of the nonlinearities of the equivalent components uses AC signals that are superposed on certain stationary DC operating points.

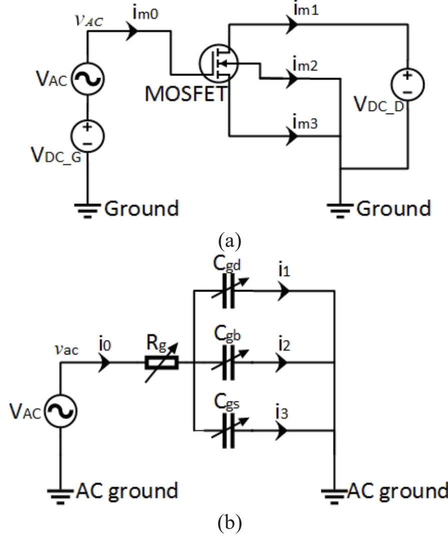

Fig. 3. Evaluation of parasitic capacitances looking into the gate terminal (off-state, sub-threshold region, and on-state in the linear region): (a) simulation setup; (b) equivalent circuit.

To evaluate the parasitic capacitance looking into the gate terminal of the power MOSFET, the simulation test bench circuit is shown in Fig. 3(a). The corresponding equivalent circuit can be derived as follows: when looking into the gate terminal of the equivalent model with drain, source, and bulk biased at fixed DC voltages, it can be assumed that the internal nodes D', S', and B' are equivalent AC ground. This is valid because R_d, R_s, and R_b in reality have very small resistance values. The assumption still holds true for physical measurements, where the external parasitic resistances and inductances from packages and interconnections do not cause practical impact. Under the conditions that the nodes D', S', and B' are equivalent AC ground, C_{db}, C_{sb}, C_{ds}, and R_{ds} can be removed from the equivalent model, and the resulting small-signal equivalent circuit is shown in Fig. 3(b). Note that each component has nonlinear values depending on the bias conditions, and that each current (and voltage) has complex values with phase component included. From Ohm's law, it is found that the equivalent nonlinear parasitic capacitance value of C_{iss} can be mathematically solved by using (1), and that C_{gd}, C_{gb}, and C_{gs} can afterwards be determined by using (2)–(4).

In (1), the imaginary part of the impedance is taken into account for calculating the capacitance value of C_{iss}, because as the input frequency f_s increases, the magnitude of the imaginary part of the impedance decreases, so that the magnitude of the resistive part of the impedance becomes comparable to the magnitude of the imaginary part of the impedance. Therefore, estimating the capacitance values using the total impedance would lead to huge errors or even wrong results at high frequencies:

$$c_{iss} = c_{gd} + c_{gb} + c_{gs} = \frac{1}{2\pi \times f_s \times \left|\mathrm{Im}\left(v_{ac} / i_0\right)\right|}, \quad (1)$$

$$c_{gd} \cong \frac{|i_1|}{|i_0|} \times c_{iss}, \quad (2)$$

$$c_{gb} \cong \frac{|i_2|}{|i_0|} \times c_{iss}, \quad (3)$$

$$c_{gs} \cong \frac{|i_3|}{|i_0|} \times c_{iss}. \quad (4)$$

For evaluating the nonlinear parasitic capacitance, an input frequency f_s of 1 MHz is used, as it is the industrial standard measurement frequency [5], [6]. At higher frequencies, the equivalent series resistance associated with the physical capacitive structures may influence the results. Since it is a distributed capacitive structure, it is a non-trivial task to include the physically distributed parasitic resistance in the transistor model (*e.g.* as equivalent series resistances to C_{gd}, C_{gb}, and C_{gs}). Using a model with a lumped capacitor C_{iss}, the distributed physical nature of the structure may cause the equivalent lumped capacitor value of C_{iss} to show a decrease with increasing frequency. Simultaneously, the equivalent lumped capacitor values of C_{gd}, C_{gb}, and C_{gs} may show either an increase or a decrease, depending on the unbalance of the distributed parasitic resistances of the drain, bulk, and source.

The simulation results of the equivalent nonlinear parasitic capacitances when looking into the gate terminal are shown in Fig. 4 for $V_D = V_B = V_S = 0$ V. The simulations are based on the HiSIM-HV models [10] for the SOI process used for fabricating the chip.

From the simulation results in Fig. 4, it is worth noting that the equivalent capacitance C_{iss} is dominated by different sub-capacitances in 3 regions: when the fixed DC bias voltage at the gate terminal V_G is negative, C_{iss} is mainly dominated by the gate-bulk capacitance C_{gb}; when V_G is near 0 V, implying that the gate and source bias voltages are close to each other, C_{iss} is mainly dominated by the gate-drain capacitance C_{gd}; when V_G is larger than the threshold voltage of the power MOSFET ($V_{th} \approx 1.1$ V), C_{iss} is mainly dominated by the gate-source capacitance C_{gs}.

The gate input capacitance C_{iss} (when bulk shorts to source) does not originate solely from the gate-source capacitance C_{gs} (and the gate-drain capacitance C_{gd}). Ignoring the gate-bulk capacitance C_{gb} would give huge errors at negative gate voltages, though at positive gate voltages, the difference may be rather small.

The nonlinear behaviour of the equivalent capacitance C_{iss} looking into the gate terminal is shown in Fig. 5 with different combinations of the gate voltage (0 V–5 V) and the drain voltage (0 V–5 V). This covers all the transistor states that power switches normally work in, i.e. the off-state, the sub-threshold region, and the on-state in the linear region.

The curve at the edge for V_D = 0 V and V_G = 0-5 V in Fig. 5(a) shows the same curve of C_{iss} for the same voltage range as shown in the right part of Fig. 4. (Note that the x-axes are different). The curve at the edge for V_G = 0 V and V_D = 0-5 V shows a monotonically decreasing function from 28.83 pF to 11.25 pF. The curve at the edge for V_G = 5 V and V_D = 0-5

V shows a monotonically increasing function from 53.82 pF to 55.16 pF with very small derivatives. From the 3D plot in Fig. 5(a), it is clear that extrapolating the nonlinear C_{iss} values based solely on a 2D plot at a certain drain or gate voltage would be inappropriate, because the nonlinear C_{iss} can either increase or decrease at different drain or gate voltages. From the contour plot in Fig. 5(b), it can be observed that at a fixed drain voltage, as the gate voltage increases, the nonlinear capacitance C_{iss} has either a large range of small capacitance values at the foot of a narrow and big mountain (high V_D), or a smaller range of small capacitance values at the foot of a wide and small hill (small V_D).

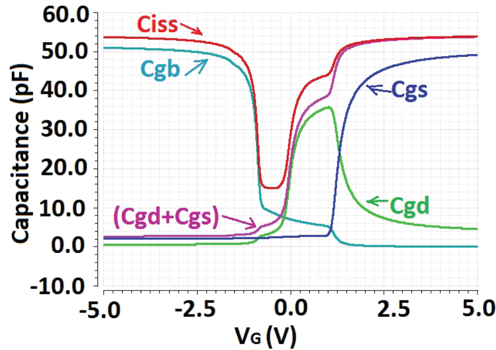

Fig. 4. Nonlinear parasitic capacitances looking into the gate terminal ($V_D = V_B = V_S = 0$ V).

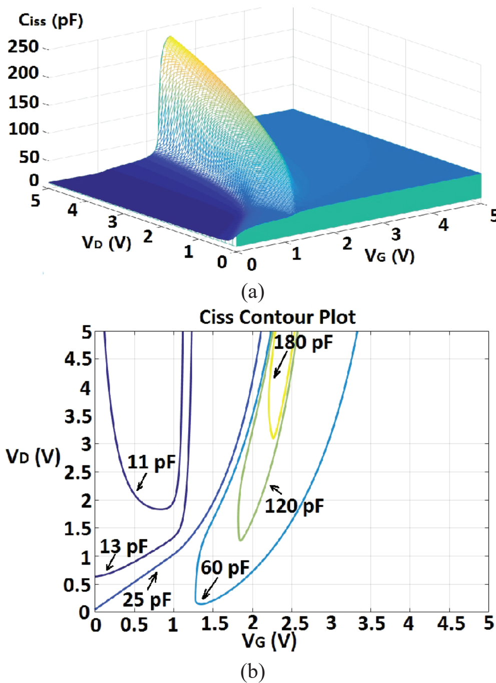

Fig. 5. Nonlinearities of C_{iss} (off-state, sub-threshold region, and on-state in the linear region, $V_B = V_S = 0$ V): (a) C_{iss} in 3D plot; (b) C_{iss} in contour plot.

In the simplified equivalent circuit in Fig. 3(b), it has been assumed that R_d in the small-signal model of power MOSFETs (in Fig. 2) has a very small resistance value and can be removed from the model when looking into the gate terminal. To evaluate the actual impact of R_d, an effective way is to add an external series resistance to the drain terminal and then determine the equivalent capacitances using the same modelling method. The simulation results of the equivalent capacitances versus the external series resistance value at the drain terminal are shown in Fig. 6(a).

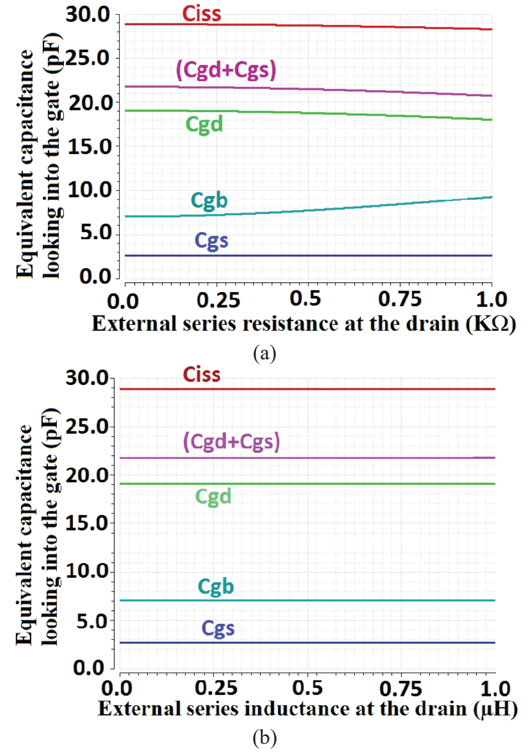

Fig. 6. Equivalent capacitances looking into the gate with external series resistance or inductance at the drain ($V_G = V_D = V_B = V_S = 0$ V): (a) external series resistance at the drain; (b) external series inductance at the drain.

All the equivalent capacitances change very little with increasing external resistance, and the gate-bulk capacitance C_{gb} is most affected. When the external resistance is about 360 Ω, C_{gb} increases by 5 %. When the external resistance increases from 0 KΩ to 1 KΩ, C_{gb} increases by 31.07 % from 7.08 pF to 9.28 pF. Similarly, an external series inductance can be added to the drain terminal, leading to the simulation results shown in Fig. 6(b). When the external inductance increases from 0 μH to 1 μH, the equivalent capacitances almost do not change (< 0.4 %). Therefore, it can be concluded that even the simplified circuit model works very well in practical conditions.

V. NONLINEAR CAPACITANCES LOOKING INTO THE DRAIN TERMINAL AT OFF-STATE

To determine the corresponding equivalent nonlinear parasitic capacitances, the situation is different when looking into the drain terminal, compared to looking into the gate terminal. This is because there is a direct resistive path from the drain terminal towards AC ground through the nonlinear resistance R_{ds}. The situation is divided into two sub-cases: 1) when the transistor is in off-state and the gate voltage is much lower than the threshold voltage, and 2) when transistor is in on-state in the linear region or in the sub-threshold region.

For the first case, R_{ds} between the drain terminal and the source terminal has an equivalent resistance in the MΩ to GΩ range, implying that R_{ds} can be removed from the equivalent model. In this case, the situation is very similar to the situation in the previous section. To evaluate the parasitic capacitances looking into the drain terminal, the simulation test bench circuit is shown in Fig. 7(a). The corresponding equivalent circuit can be derived as follows: when looking into the drain terminal of the equivalent model with the gate, bulk, and

source terminals biased at fixed DC voltages, the internal nodes G', B', and S' can be assumed to be equivalent AC ground. Then C_{gb}, C_{gs}, and C_{sb} can be removed from the equivalent model, and the resulting small-signal equivalent circuit is shown in Fig. 7(b).

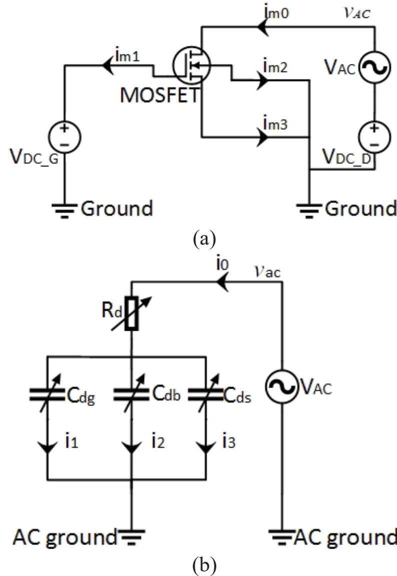

Fig. 7. Evaluation of parasitic capacitances looking into the drain terminal (off-state): (a) simulation setup; (b) equivalent circuit.

The corresponding nonlinear parasitic capacitance values can be determined by the following equations (5)–(8):

$$c_{oss} = c_{dg} + c_{db} + c_{ds} = \frac{1}{2\pi \times f_s \times \left|\mathrm{Im}\left(v_{ac} / i_0\right)\right|}, \quad (5)$$

$$c_{dg} \cong \frac{|i_1|}{|i_0|} \times c_{oss}, \quad (6)$$

$$c_{db} \cong \frac{|i_2|}{|i_0|} \times c_{oss}, \quad (7)$$

$$c_{ds} \cong \frac{|i_3|}{|i_0|} \times c_{oss}. \quad (8)$$

The simulation results of the equivalent nonlinear parasitic capacitance when looking into the drain terminal are shown in Fig. 8 for $V_G = V_B = V_S = 0$ V. The equivalent capacitance C_{oss} is mainly dominated by the drain-bulk capacitance C_{db}. The drain-source capacitance C_{ds} shows very small values, because the transistor is biased in off-state with the gate voltage of 0 V, and there is no channel for majority carries formed in the lateral device: in a partial SOI process, the drain diffusion and the source diffusion are separated far apart.

Therefore, the situation is very different from the situation that there is a direct and large junction between the P-body and N$^-$ epitaxial layer in conventional vertical devices [11].

The nonlinear behaviour of the equivalent capacitance C_{oss} looking into the drain terminal is shown in Fig. 9 with different combinations of the gate voltage (0 mV–700 mV) and the drain voltage (0 V–5 V). Note that in these voltage ranges, the transistor is in off-state and the gate voltage is much lower than the threshold voltage ($V_{th} \approx 1.1$ V). The curve at the edge for $V_G = 0$ V and $V_D = 0$-5 V in Fig. 9(a) shows the same curve of C_{oss} for the same voltage range as shown in the left part of Fig. 8. The curve at the edge for $V_D = 0$ V and $V_G = 0$-700 mV shows a monotonically increasing function from 55.10 pF to 70.54 pF. The curve at the edge for $V_D = 5$ V and $V_G = 0$-700 mV shows a monotonically increasing function from 6.072 pF to 6.140 pF with very small derivatives. This phenomenon can be observed from the contour plot of C_{oss} in Fig. 9(b) as well.

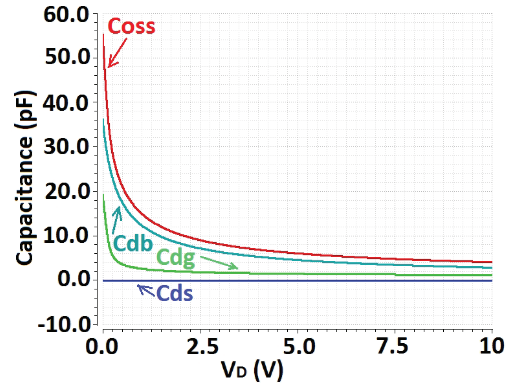

Fig. 8. Nonlinear parasitic capacitances looking into the drain terminal (off-state, $V_G = V_B = V_S = 0$ V).

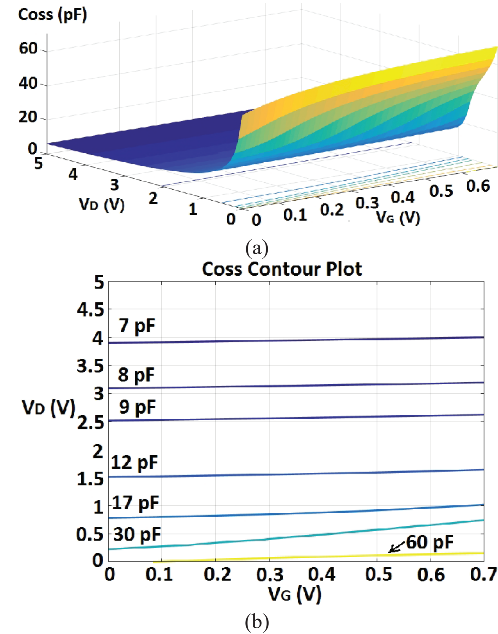

Fig. 9. Nonlinearities of C_{oss} (off-state and the gate voltage is much lower than the threshold voltage, $V_B = V_S = 0$ V): (a) C_{oss} in 3D plot; (b) C_{oss} in contour plot.

It may be noticed that R_g has been removed from the simplified equivalent circuit in Fig. 7(b) to determine the nonlinear parasitic capacitances when looking into the drain terminal. This corresponds to the industrial standard way [12] of measuring C_{oss} by directly shorting the gate terminal to the source terminal, and then measuring or calculating the equivalent capacitance between the drain terminal and AC ground [7], [12]. This is equivalent to omitting R_g from the measurement circuit.

To evaluate the actual impact of R_g, an effective way is to add an external series resistance to the gate terminal and then determine the equivalent capacitances using the same modelling method. The simulation results of this evaluation are shown in Fig. 10(a). The equivalent capacitances almost

do not change (< 0.6 %) with increasing external resistance, except for the drain-gate capacitance C_{dg}. When the external resistance increases from 0 KΩ to 1 KΩ, C_{dg} looking into the drain terminal decreases by 1.52% from 19.06 pF to 18.77 pF. Again, an external series inductance can be added to the gate terminal, leading to the simulation results shown in Fig. 10(b).

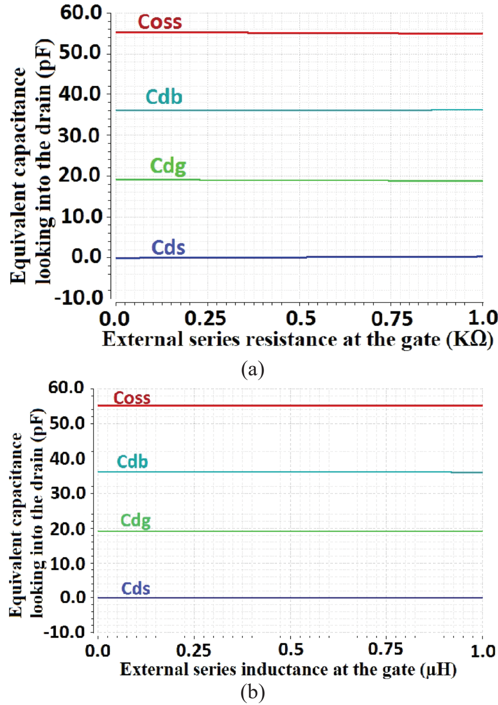

Fig. 10. Equivalent capacitances looking into the drain with external series resistance or inductance at the gate ($V_G = V_D = V_B = V_S = 0$ V): (a) external series resistance at the gate; (b) external series inductance at the gate.

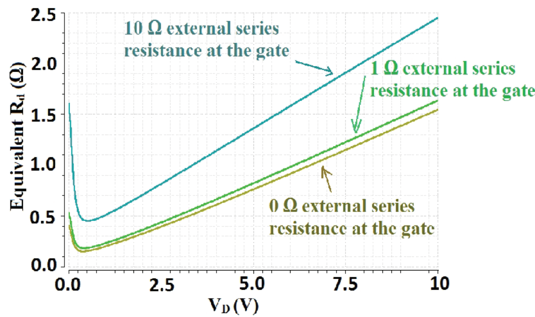

Fig. 11. Equivalent R_d looking into the drain with different external series resistance at the gate ($V_G = V_B = V_S = 0$ V).

When the external inductance increases from 0 μH to 1 μH, the equivalent capacitances almost do not change (< 0.2 %). Therefore, it can be concluded that the simplified circuit model also works very well in practical conditions, when evaluating the nonlinear parasitic capacitances looking into the drain terminal.

The nonlinear equivalent resistance R_d that is determined using the equivalent circuit in Fig. 7(b) when looking into the drain terminal is shown in Fig. 11. It shows that the external series resistance at the gate indeed contributes to the nonlinearities of the equivalent resistance R_d, and this is because R_d as the only resistive component in the simplified equivalent circuit has to model all the effects resulting from a finite value of the total resistance at the gate.

VI. NONLINEAR CAPACITANCES LOOKING INTO THE DRAIN TERMINAL IN ON-STATE IN THE LINEAR REGION OR IN THE SUB-THRESHOLD REGION

As discussed in the previous section, the second sub-case is when the transistor is in on-state in the linear region or in the sub-threshold region. The simulation test bench circuit is the same one as shown in Fig. 7(a). For the sub-threshold region, the equivalent resistance R_{ds} is in the KΩ range or even lower, so it cannot be neglected compared to the impedance of the parasitic capacitances. The equivalent circuit can be derived from Fig. 7(b) by adding R_{ds} directly between the drain and the source terminals. The resulting equivalent circuit is shown in Fig. 12, where the dotted box denotes the transistor boundary.

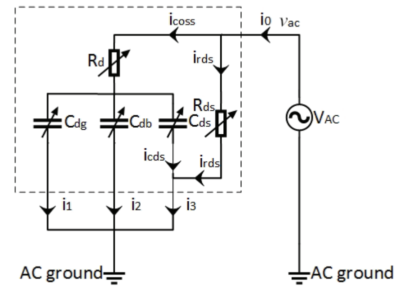

Fig. 12. Equivalent circuit looking into the Drain terminal (on-state in the linear region or in the sub-threshold region).

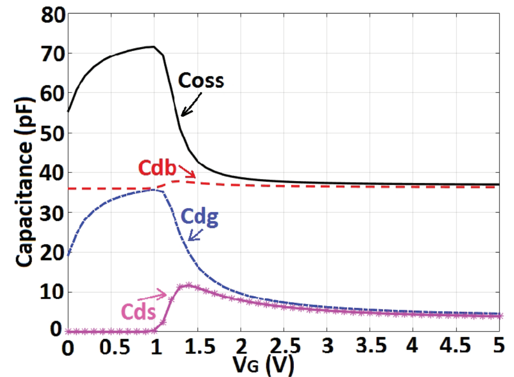

Fig. 13. Nonlinear parasitic capacitances looking into the drain terminal (on-state in the linear region or in the sub-threshold region, as well as off-state, $V_D = 1$ μV, $V_B = V_S = 0$ V).

The nonlinear resistance R_{ds} can be measured at DC using a small DC bias voltage for the drain voltage. With the value of R_{ds} in place, the nonlinear parasitic capacitance values can be estimated by the following equations (9)–(13) (recall that each AC current has its phase included, and the minus sign is not simple subtraction of magnitudes):

$$i_{rds} \approx \frac{v_{ac}}{R_{ds}}, \tag{9}$$

$$c_{oss} = c_{dg} + c_{db} + c_{ds} = \frac{1}{2\pi \times f_s \times \left|\mathrm{Im}\left(v_{ac} / \left(i_0 - i_{rds}\right)\right)\right|}, \tag{10}$$

$$c_{dg} \cong \frac{|i_1|}{|i_0 - i_{rds}|} \times c_{oss}, \tag{11}$$

$$c_{db} \cong \frac{|i_2|}{|i_0 - i_{rds}|} \times c_{oss}, \tag{12}$$

$$c_{ds} \cong \frac{|i_3 - i_{rds}|}{|i_0 - i_{rds}|} \times c_{oss}. \quad (13)$$

Finally, the nonlinear parasitic capacitances looking into the drain terminal are shown in Fig. 13 for the case when the transistor is in on-state in the linear region or in the sub-threshold region. The equivalent circuit for these conditions works for the off-state as well, and the part of the C_{oss} curve for V_G = 0-700 mV in Fig. 13 matches exactly with the C_{oss} curve for the same voltage range in Fig. 9(a), even though the results are achieved using different equivalent circuits with and without R_{ds}. Note that the drain voltage has a DC bias value of 1 μV because the nonlinear resistance R_{ds} must be found for the bias point used for the AC simulations, and the drain voltage has to be kept as small as possible to avoid the nonlinear effects at higher drain voltages. The nonlinearities are not analyzed at the high drain voltages when the transistor is switched on, because power switches do not normally operate with a high drain voltage in on-state as this causes large losses. C_{oss} in off-state and in the sub-threshold region is dominated by the parasitic capacitances C_{db} and C_{dg} together, and C_{oss} in on-state in the linear region is mainly dominated by C_{db}. The parasitic capacitance C_{ds} has its peak value when the gate voltage is slightly above the threshold voltage.

VII. CONCLUSIONS

A high voltage power MOSFET with a drain to source breakdown voltage above 100 V is designed in a 0.18 μm partial SOI process. It is composed of 96 parallel connected unit cells with a gate length of 0.5 μm, and the die area is 0.2948 mm² for the transistor array.

The power MOSFET is modeled using a small-signal modeling method, with the bulk as a separate terminal. The proposed circuit model is applicable for all the relevant transistor states: off-state, sub-threshold region, and on-state in the linear region. The nonlinearity analysis is divided into 3 sub-cases, which are analyzed separately. The input capacitance C_{iss} and the output capacitance C_{oss} are separated into sub-components, and it is found that the parasitic capacitances towards the bulk can dominate over the parasitic capacitances towards the source in this lateral device. The 3D plots and the contour plots reveal the overall nonlinear dependencies of the parasitic capacitances on the bias voltages.

FUTURE WORK

The switching behavior and the temperature behavior of the proposed small-signal model can be further investigated as future work. The theoretical behavior might be derived in one of the following ways: 1) calculate a linear formula or do a two-dimensional numerical simulation of the cell structure [13], 2) use a piecewise linear model or solve a derivatives matrix [10], or 3) apply semiconductor physics in different device regions (*e.g.* accumulation, depletion, weak inversion, moderate inversion, strong inversion saturation, and strong inversion non-saturation) [14].

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A.2. Publication (conference)

This is the post-print version of the publication.

Lin Fan, Arnold Knott, Ivan Harald Holger Jørgensen, “Layout Capacitive Coupling and Structure Impacts on Integrated High Voltage Power MOSFETs”, in 12th Conference on PhD Research in Microelectronics and Electronics, 2016.

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Layout Capacitive Coupling and Structure Impacts on Integrated High Voltage Power MOSFETs

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***Abstract*—The switching performances of the integrated high voltage power MOSFETs that have prevailing interconnection matrices are being heavily influenced by the parasitic capacitive coupling of on-chip metal wires. The mechanism of the side-by-side coupling is generally known, however, the layer-to-layer coupling and the comparison of the layout impacts have not been well established. This paper presents modeling of parasitic mutual coupling to analyze the parasitic capacitance directly coupled between two on-chip metal wires. The accurate 3D field solver analysis for the comparable dimensions shows that the layer-to-layer coupling can contribute higher impacts than the well-known side-by-side coupling. Four layout structures are then proposed and implemented in a 0.18 µm partial SOI process for 100 V integrated power MOSFETs with a die area 2.31 mm^2. The post-layout comparison using an industrial 2D extraction tool shows that the side-by-side coupling dominated structure can perform better than the layer-to-layer coupling dominated structure, in terms of on-resistance times input or output capacitance, by 9.2% and 4.9%, respectively.**

Keywords*—*integrated circuit interconnections; layout; mutual coupling; parasitic capacitance; power MOSFET

I. Introduction

The miniaturization trend of power electronics requires reductions in size [1], and one of the principle approaches is to integrate active components on-chip, such as power MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) in SOI (Silicon on Insulator) processes [2] or in nonstandard high-voltage CMOS (Complementary Metal-Oxide-Semiconductor) processes [3]. As the process technologies keep developing, the electrical parameters of on-chip interconnections are becoming the real bottleneck of circuit performances [4], especially for high-power-density converters [5]. The coupling capacitance can be measured on-chip but the accuracy suffers from the supply noise [6]. Section II presents modeling of parasitic mutual coupling of on-chip metal wires, from which the capacitive coupling directly between the wires is specifically analyzed with post-layout 2D extractions and 3D field solvers.

The capacitive coupling of interconnections is embedded in the layout structures of high voltage power MOSFETs. The previously investigated structures such as overlapping circular-gate structure [7], octagonal structure [8], hexagonal structure [9], waffle-shaped structure [10], and hybrid waffle structure [11] are commonly not permitted by the polysilicon DRC (Design Rule Check) rules in deep submicron processes. The waffle-shaped structure with the angled non-symmetrical connections leads to current unbalance and is therefore not optimal for high current applications [10]. Taking into account the substrate contacts and the guarding rings between the active areas, especially when the waffle structure is actually an effective trade-off between the metal interconnections and the active area [11], the high active area density cannot be a single FOM (Figure of Merit) of a layout structure. Nevertheless, a common principle underneath all the structure improvements is about sharing active areas and/or interconnections in all geometrical directions. In section III, four layout structures are proposed and implemented in a 0.18 µm partial SOI process for 100 V power MOSFETs. In Section IV, the post-layout results are compared and discussed. Section V concludes the paper.

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II. Layout Capacitive Coupling

A. Modeling of Parasitic Mutual Coupling

At the schematic level, wires are ideal electrical paths connecting different nodes that have the same net name. However, the wires in integrated circuit layouts are normally made by metal (polysilicon is another example with high sheet resistance), and the distances between the on-chip metal wires are generally in µm range, resulting in unavoidable mutual capacitive coupling. The modeling of two closely placed on-chip metal wires (*A* and *B*) is shown in Fig. 1. All the components result from the parasitic effects of the layouts.

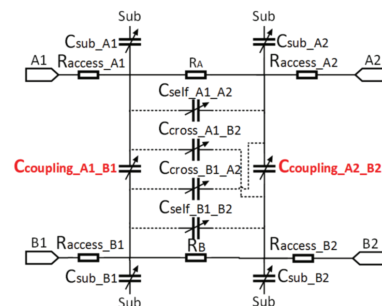

Fig. 1. Modeling of two closely placed on-chip metal wires (mutual coupling from either side-by-side or layer-to-layer). All components are parasitic.

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Wire A is connecting the nodes $A1$ and $A2$, and wire B is connecting the nodes $B1$ and $B2$. R_A and R_B are the intrinsic parasitic resistance of each metal wire. The four R_{access} represent the parasitic resistance coming from the physical pins to access the real metal wires, where the resistance values are normally less than 1 mΩ. The four C_{sub} are the intrinsic parasitic capacitances to the substrate, where the capacitance values are growing with increased length or width. It can also be shown that for the same dimensions, a metal wire located in a lower layer such as *Metal1* (abbreviated as *M1* and for the rest of the paper) presents higher intrinsic parasitic capacitance to the substrate, than the associated one if the same wire is located in an upper layer. The modeling in Fig. 1 has a symmetrical structure. The main focus of this paper is the two direct coupling capacitors $C_{coupling}$. There are other mutual coupling capacitors C_{self} and C_{cross}, which are illustrated with dash lines, representing the fact that when the metal wires are very wide but short in length, there could be mutual coupling between the two nodes of the same wire and cross coupling between non-adjacent nodes that cannot be lumped into $C_{coupling}$. These capacitance values are extracted as well and generally much smaller than $C_{coupling}$.

B. Side-by-Side Capacitive Coupling of Metal Wires

The coupling capacitors $C_{coupling_A1_B1}$ and $C_{coupling_A2_B2}$ (in Fig. 1) are not lumped due to the symmetrical structure and the parasitic resistance in between. To reflect the coupling effect, the average value of the two is used. The capacitive coupling between the two side-by-side metal wires located in the same layer has been simulated with the actual layouts using a 2D extraction tool and a 3D filed solver (i.e. Calibre xRC and Calibre xACT 3D with high accuracy mode, respectively), and the corresponding results are shown in Fig. 2. Note, it is assumed that there is no power/ground plane above the metal wires (much more expensive to possess on-chip compared to PCB case), and there is global substrate underneath, so that the results are reproducible and not case-dependent. The dimensions of the side-by-side metal wires are defined in Fig. 2(a). T is the metal thickness. S is the spacing distance. W is the common metal width. L is the common metal length. The reference dimensions of a single metal wire are T of 555 nm, W of 0.5 µm, L of 5 µm, and S of 0.5 µm, if not otherwise specified. If the metal wire is located in *M3* layer in the used process, then the resulting parasitic resistance is approximately 1 Ω. There are 5 metal layers available to use with the chosen process modules. The top metal layer *Mtop* is generally thicker than the other lower layers to reduce the metal sheet resistance (the *Mtop* thickness used is 975 nm), however, this leads to increased capacitive coupling which is shown in Fig. 2(b). The capacitive coupling decreases with increased spacing between the two metal wires, and it is shown in Fig. 2(c). The 2D extraction results are flat out for very small spacing values, due to the extractions limited by the DRC rules. For 100 V side-by-side operations, the spacing S in excess of 1 µm is generally recommended for all metal layers. The capacitive coupling increases with the width W, while keeping the same spacing S, as shown in Fig. 2(d). The 2D extraction results are accurate for small W values, however, as W increases, $C_{coupling}$ becomes more underestimated, mainly because C_{self} of the same metal wire is increasingly overestimated instead.

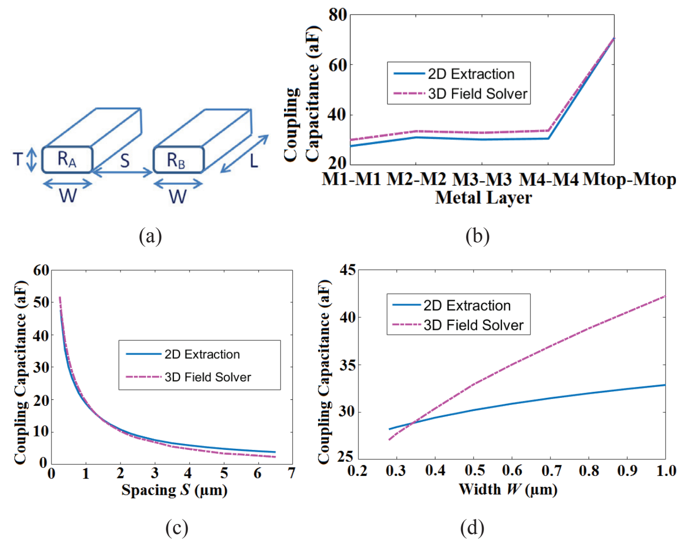

Fig. 2. Side-by-side capacitive coupling. (a) Definition of dimensions. (b) Versus metal layers. (c) Versus S (*M3-M3*). (d) Versus W (*M3-M3*).

C. Layer-to-Layer Capacitive Coupling of Metal Wires

The two metal wires that are located in separate layers can still suffer from capacitive coupling to each other, because of the electric field penetrating the dielectric between the metal layers. The definitions of the dimensions in this case are shown in Fig. 3(a). T is the metal thickness and D is the dielectric thickness. O is the offset distance in the vertical direction. W and L are the common metal width and length, respectively. The values of T and D can vary between different metal layers even for the same process. The D values are confidential for the used process. Fig. 3(b) shows that the capacitive coupling resulting from the layer-to-layer effects is approximately the same for different metal layers. When the two metal wires have zero offset O meaning that they are exactly overlapping each other in the vertical direction, the capacitive coupling is strongest in this case, then as O increases, the capacitive coupling gradually decreases, as shown in Fig. 3(c).

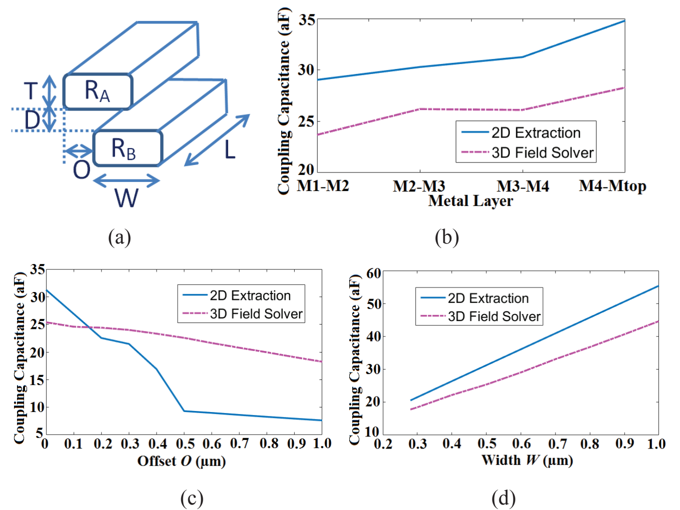

Fig. 3. Layer-to-layer capacitive coupling. (a) Definition of dimensions. (b) Versus metal layers (O = 0). (c) Versus O (*M3-M4*). (d) Versus W (*M3-M4*).

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The capacitive coupling directly between the two metal wires in *M3* and *M4* becomes stronger as the common width *W* increases, and this is shown in Fig. 3(d). In Fig. 3, the common discrepancies between the results of the 2D extraction and the 3D field solver are mainly due to the fact that the 2D extraction tool tends to have unbalanced solutions for the mutual coupling capacitance C_{self} in the layer-to-layer coupling case and have discontinuous solutions for certain geometrical dimensions. Despite this, the 2D extraction results are still accurate for small offset values and start to converge with the 3D field solver results after the two metal wires are actually moved away in the vertical direction. The 3D field solver is the most accurate and cost-effective way to investigate the capacitive coupling effects, and by comparing the results, it shows that the layer-to-layer capacitive coupling is in the same order or even higher than the side-by-side capacitive coupling, when the metal wires and the dielectric have the comparable dimensions.

III. PROPOSED LAYOUT STRUCTURES

For the layout structures of integrated high voltage power MOSFETs, a highly compact layout is more difficult to achieve, compared to low-power MOSFETs. On the side of the drain diffusion, the voltage potential is uniformly distributed, thus the corresponding isolation structures can be overlapped. However, there is no uniform potential along the side of the device from the drain diffusion to the source diffusion, and the distributed electric filed needs to be properly terminated. Therefore, the associated isolation structures surrounding these edges result in a less achievable device density.

The four proposed layout structures for high voltage power MOSFETs are shown in Fig. 4. The main principles are demonstrated and the real layout implementation is limited by various DRC rules. The gate network is mainly routed in *M2* layer and the power distribution is basically achieved in *Mtop* layer. These two and other nearly forty layers are left out on purpose, so that the major capacitive coupling structure between the drain network and the source network can be shown for clarity. In Fig. 4(a), the drain/source connections are lateral stacks of two adjacent metal layers, i.e. *M3* and *M4*, and the capacitive coupling is mainly dominated by the side-by-side coupling mechanism. The drain/source connections in Fig. 4(b) are laterally routed on different metal layers (*M3* and *M4*), thus the capacitive coupling is mainly induced by the layer-to-layer coupling mechanism. The perpendicular mesh structure in Fig. 4(c) can be viewed as a trade-off between parasitic resistances and capacitances, and the resulting parasitic effects depend on the specific geometrical dimensions. Fig. 4(d) serves as a layout structure where the bulk is constructed as a separate terminal, and the Nwell metal strap connections need to be chopped into pieces to make the bulk network route through and reach the chip pad.

IV. POST-LAYOUT COMPARISONS AND DISCUSSIONS

The comparison of the four proposed layout structures is summarized in Table I. The high voltage power MOSFETs are implemented in a 0.18 μm partial SOI process. The maximum operation voltage between the drain and the source is 100 V, and that between the gate and the source is 5.5 V.

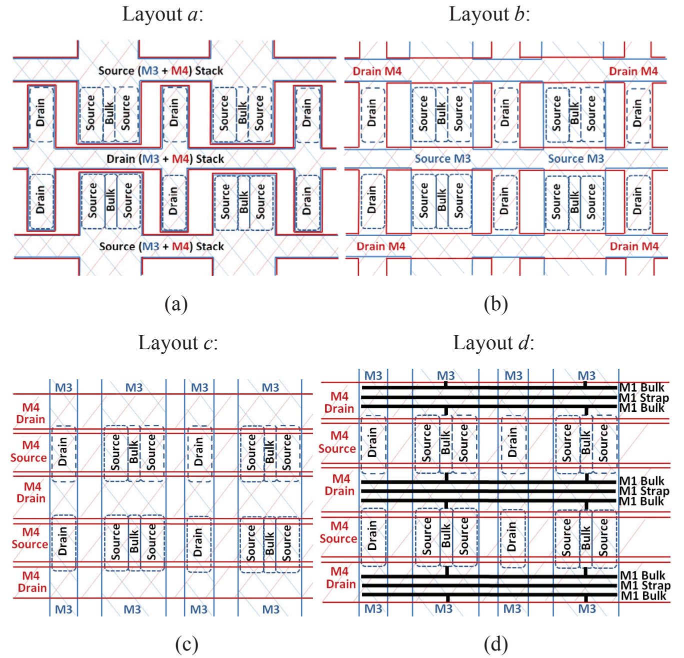

Fig. 4. Proposed layout structures for integrated high voltage power MOSFETs. (a) Drain/source horizontal connection, metal layers stack, mainly side-by-side coupling. (b) Drain/source horizontal connection, on separate metal layers, mainly layer-to-layer coupling. (c) Drain/souce vertical connection, perpendicular mesh structure, coupling by geometries. (d) Drain/souce structure the same as (c) but with the bulk as a seperate terminal.

$$\left(\frac{W}{L}\right)_a = \left(\frac{W}{L}\right)_b = 2\cdot\left(\frac{W}{L}\right)_c = 2\cdot\left(\frac{W}{L}\right)_d = 38400 \qquad (1)$$

TABLE I. LAYOUT STRUCTURES COMPARISION

R/C	Top chip-level (including chip-pads and ESD protections)					
	Schematic *a & b*	**Post-Layout *a***	**Post-Layout *b***	**Schematic *c & d***	**Post-Layout *c***	**Post-Layout *d***
Parasitic	No	2D Extract	2D Extract	No	2D Extract	2D Extract
$R_{ds(on)}$ (Ω)[a]	1.542	2.071	2.250	3.085	3.354	3.295
$C_{g\text{-}sb}$ (pF)[b]	21.3	46.9	49.5	11.5	25.1	26.7
C_{gd} (pF)[b]	38.1	41.4	39.3	19.1	20.6	20.6
C_{iss} (pF)[b]	59.4	92.7	93.2	30.6	48.0	48.9
$C_{d\text{-}sb}$ (pF)[c]	72.1	88.4	85.7	36.0	47.6	48.0
C_{dg} (pF)[c]	38.1	41.4	39.3	19.1	20.6	20.6
C_{oss} (pF)[c]	110.2	132.1	127.6	55.1	69.5	69.8
$R_{ds(on)}\cdot C_{iss}$ (ps)	91.6	192.0	209.7	94.4	161.0	161.1
$R_{ds(on)}\cdot C_{oss}$ (ps)	169.9	273.6	287.1	170.0	233.1	230.0

a. $V_{G\text{-}SB}$ = 5 V, V_{DS} = 0.1 V, T = 27 C, typical process corner.

b. Test signals into the gate terminal, $V_G = V_D = V_B = V_S$ = 0 V, T = 27 C, typical process corner.

c. Test signals into the drain terminal, $V_G = V_D = V_B = V_S$ = 0 V, T = 27 C, typical process corner.

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The designed (W/L) ratios of the four layout structures are according to (1). W is the effective total gate width, and L is the channel length. The minimum channel length of 0.5 µm is chosen for the used process. The top chip-level post-layout parasitic resistances and capacitances are extracted using an industrial 2D extraction tool (Calibre xRC). The 3D field solver is generally not applicable to complicated layout networks, due to its demanding computational requirements. Therefore, the 2D extractions are commonly used in industry, and the extracted results are still meaningful for comparison between topologies. The full details of the modeling, simulation, and extraction of the equivalent nonlinear parasitic parameters of the high voltage power MOSFETs can be found in [2]. A testing frequency of 1 MHz is used as it is the industrial standard measurement frequency [12], [13]. For each structure, the electrostatic discharge (ESD) protection circuits add 1.3-1.8 pF extra parasitic capacitance between the gate and the source terminals (nonlinear voltage dependent).

First, all of the post-layout parameters are much worse than those at the schematic level, which means that the overall performances are heavily impacted or even dominated by the parasitic parameters of the interconnections, rather than the intrinsic transistor parameters. Second, using the products of on-resistance and input or output capacitance as indicators, the side-by-side coupling dominated layout *a* is actually better than the layer-to-layer coupling dominated layout *b*, by 9.2% and 4.9%, respectively. Even though $C_{d\text{-}sb}$ of layout *b* is lower, more metal is spent for the source on *M3* thus $C_{g\text{-}sb}$ is higher due to the layer-to-layer coupling with *M2*, and the parasitic resistance is higher than the metal stack layout *a*. Third, the layouts *c* and *d* may better fit the high frequency converters where the switching loss is dominated. The lower capacitance is one concern. The part of the on-resistance contributed by the interconnections becomes larger as the transistor sizes increase, rather than inversely scaling with the transistor sizes, i.e. it is a trade-off between R and C, but not simply with a RC constant.

The parasitic coupling capacitance of the interconnections is always superposed on the intrinsic nonlinear parasitic capacitance of the power MOSFETs, and the nonlinearity of the overall total capacitance tends to be reduced in terms of the voltage-dependent capacitance variations becoming relatively less. This kind of linearization may benefit high frequency switching applications, and it is previously investigated with on-die capacitor [14] and external capacitor [15].

The layout of the entire chip design is shown in Fig. 5, and the four proposed layout structures are highlighted with the white color boxes. The die area is 2.31 mm^2 (1520 µm x 1520 µm). The silicon design has been sent to fabrication.

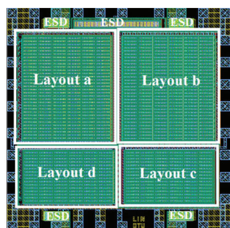

Fig. 5. Layout of the chip design (proposed structures are highlighted).

V. Conclusions

The modeling of parasitic mutual coupling of on-chip metal wires is presented, and the capacitive coupling is specifically analyzed for different geometrical dimensions with post-layout 2D extractions and 3D field solvers. It shows that the layer-to-layer coupling can have more impacts than the side-by-side coupling. Four layout structures for 100 V integrated power MOSFETs are proposed and implemented in a 0.18 µm partial SOI process. The post-layout performances reveal that the side-by-side coupling dominated structure can improve $R_{ds(on)}{\cdot}C_{iss}$ by 9.2% and $R_{ds(on)}{\cdot}C_{oss}$ by 4.9%. The trade-off between R and C depends on the specific applications.

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A.3. Publication (conference)

This is the post-print version of the publication.

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Optimization of Nonlinear Figure-of-Merits of Integrated Power MOSFETs in Partial SOI Process

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Abstract – **State-of-the-art power semiconductor industry uses figure-of-merits (FOMs) for technology-to-technology and/or device-to-device comparisons. However, the existing FOMs are fundamentally nonlinear due to the nonlinearities of the parameters such as the gate charge and the output charge versus different operating conditions. A systematic analysis of the optimization of these FOMs has not been previously established. The optimization methods are verified on a 100 V power MOSFET implemented in a 0.18 μm partial SOI process. Its FOMs are lowered by 1.3-18.3 times and improved by 22-95 % with optimized conditions of quasi-zero voltage switching.**

Keywords – **Figure of Merit, Gate Charge, Output Charge, Power MOSFET, Silicon-on-Insulator**

I. Introduction

One of the main challenges for state-of-the art very high frequency (VHF, 30-300 MHz) converters to be effectively used in industrial products is the selection of active components, i.e. power semiconductors [1]. For discrete power devices, the Wide Band Gap (WBG) semiconductors such as GaN and SiC are of consideration [2]. For integration of power devices with control and driver circuits on the same die, one promising way is to use Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) at different voltage domains in Silicon-on-Insulator (SOI) processes [3].

Conventionally, different transistor technologies are compared quantitatively using figure-of-merits (FOMs) [4]. Another usage of the FOMs is to evaluate the overall performance of a power device for a switching application [5]. The technology or device that has a lower FOM index value is deemed to have a better performance. The early-developed FOM such as Baliga FOM (BFOM) is solely based on the conduction loss minimization [6], and therefore does not apply to high frequency applications where the switching losses are not negligible. As technologies keep developing with emerging devices, different forms of FOMs are proposed in [4], [5], [7], [8]. However, recent researches show that these FOMs are not consistently used [5], [9]. This is because the FOMs typically consist of trade-off parameters such as on-resistance and gate charge (or certain parts of the gate charge), and these contributing parameters depend on the specific operating conditions. As a result, the FOMs are fundamentally nonlinear and application-dependent on voltage and current conditions. A systematic analysis to optimize the nonlinear FOMs has not been previously established, but it is needed to fully explore the performance potentials of the integrated power MOSFETs, especially for partial SOI processes. In Section II, different evaluation methods are reviewed, and the most suitable test circuit for deriving FOMs is selected and implemented. In Section III, the nonlinearities of the gate charge and its different sub-components are analyzed. In Section IV, the FOMs are then synthesized by using the gate charge and other corresponding parameters. Optimization methods of the FOMs versus specific operating conditions are summarized and discussed. Section V concludes the paper.

II. Selection and Implementation of Test

Before composing the FOMs of a power MOSFET, the key parameters such as the gate charge and its sub-components have to be known. The first way to obtain various charge parameters is to calculate the integration of the parasitic capacitances as a function of an operating voltage such as the drain-source voltage [4], [10], [11]. However, the calculated results inherently lead to errors. These errors come from the fact that the parasitic capacitances depend on not only the drain-source voltage but also the gate-source voltage [3], which is not taken into account as a variable for the integration calculation. Note that the parasitic capacitances themselves do not provide direct and accurate device-to-device comparisons [12], e.g. a device with a higher capacitance value in [13] switches faster than another device with a lower capacitance value. In addition, a device with a higher on-resistance value in [14] shows a better overall efficiency for a converter, compared to another device with a lower on-resistance value. Therefore, a more accurate way to obtain the gate-charge parameters is needed, particularly for designing a gate-driver circuit [15] as well as calculating the FOMs.

The second way is to simulate the gate-charge behavior during switching transients. There is no standard test circuit for this, and different configurations are compared for choosing the most appropriate test circuit for the purpose of composing the FOMs. Some possible test circuits for evaluating the gate-charge behavior in the transistor turn-on process are shown in Fig. 1. The simplest configuration is to use a resistive load [5], [16], [17], as shown in Fig. 1(a). The configuration that uses a clamped inductive load [18]-[20] is shown in Fig. 1(b). The same circuit in Fig. 1(b) can be reused for a double pulse test (DPT) circuit. By

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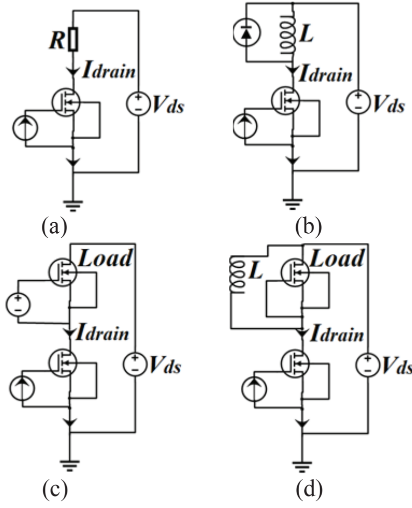

Fig. 1. Several test circuits for gate charge. (a) Resistive load. (b) Clamped inductive load. (c) Active load (simplified bias circuit). (d) Active load combined with an inductive load.

replacing the current source with a voltage-pulse source [21], the transistor turn-on and turn-off energy losses are measured, instead of the gate-charge parameters. For both test circuits in Fig. 1(a) and (b), the voltage transition and current transition occur simultaneously when charging the gate of the transistor. As a result, the sub-components of the gate charge cannot be accurately extracted from the gate-charge curve. Therefore, these test circuits cannot be used for deriving the FOMs that are composed of sub-components of the gate charge.

The configuration that uses an active load [13], [22], [23] is shown in Fig. 1(c) with a simplified bias circuit for the load. Another alternative test circuit is to use a gate-source-shorted active load combined with an inductive load [24], as shown in Fig. 1(d). For both test circuits in Fig. 1(c) and (d), the gate-charge curves are affected by the parasitic capacitances of the active loads as well as the device under test (DUT). Therefore, the resulting gate charge cannot be accounted for solely by the DUT.

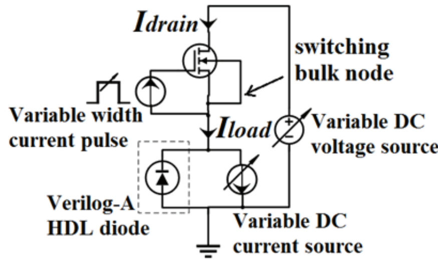

Fig. 2. Selected test circuit for gate charge (for deriving FOMs).

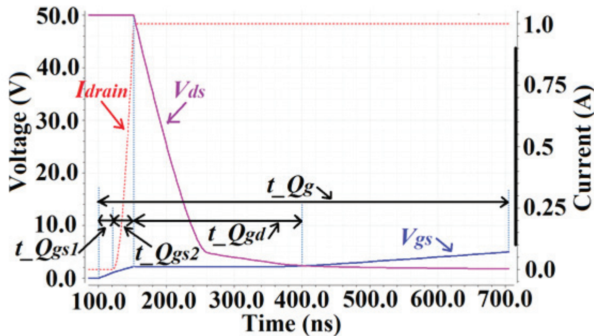

Fig. 3. Simulated transient waveforms and naming conventions.

The principle of the switching power-pole configuration [25] that uses a transistor and a diode is adopted and used for the purpose of deriving different FOMs. With the setup shown in Fig. 2, the voltage and current transitions are separated apart, which results in clear definitions of the sub-components of the gate charge. Provided that the diode is ideal, it is basically equivalent to interchange the positions of the power MOSFET and the load part of the circuit [12], [26]. The bulk terminal of the power MOSFET is connected to the on-chip switching node. This can be done by utilizing the vertical and horizontal dielectric isolation of a partial SOI process. The diode is implemented using the Verilog-A Hardware Description Language (HDL), and it is deliberately modeled with no reverse current and no forward voltage drop. The drain current I_{drain} is always equal to the load current I_{load}.

The DUT is a 100 V power MOSFET implemented in a 0.18 μm partial SOI process with a die area of 0.5276 mm^2. The maximum operating gate-source voltage is 5.5 V. The HiSIM-HV models that are provided by the process foundry are used, which are complete surface-potential-based models based on the drift-diffusion theory [27]. In contrast, the model that is conventionally from a discrete-transistor manufacturer such as [22] uses the most basic Schichman-Hodges model, which is often used for initial manual analysis without considering mobility degradation and an inaccurate model for sub-micron technologies [28]. Using the setup in Fig. 2, the parasitic resistance and/or inductance at the gate terminal do not affect the gate-charge results because the constant-amplitude current pulse is used. The parasitic inductance at the source terminal causes slight errors due to the resulting ringing of the drain current and the drain-source voltage. The results especially for the sub-components of the gate charge are most affected by the parasitic resistance at the source terminal, which is equivalent to adding an extra resistive load to the DUT, as previously discussed for Fig. 1(a).

The simulated transient waveforms are shown in Fig. 3. A current pulse of 1 mA is applied to the gate at 100 ns. The current pulse has a variable pulse width so that the gate-source voltage can be charged to different voltage potentials. The naming conventions are also shown in Fig. 3 and defined as follows: the time interval t_Q_{gs1} starts (t_Q_g starts) when the gate-source voltage V_{gs} starts to increase (i.e. at 100 ns when the current pulse to the gate is applied). The time interval t_Q_{gs2} starts (t_Q_{gs1} ends) when the drain current I_{drain} starts to increase. The time interval t_Q_{gd} starts (t_Q_{gs2} ends) when the drain-source voltage V_{ds} starts to decease. The time interval t_Q_g ends when the final-state (i.e. the state at the end point of the gate-charge event) V_{gs} is reached. The end point of t_Q_{gd} generally has no strict definition, and it is often stated as the point when the final-state V_{ds} or the final-state drain-source resistance R_{ds} (provided that the final-state V_{gs} is high enough to turn the transistor on, the final-state R_{ds} is also called on-resistance) is reached [5], [13], [16], [20], [23], [26]. In fact, both during and after the time interval t_Q_{gd}, V_{gs} still continuously increases (slightly), and the resulting V_{ds} (thus R_{ds}) keeps decreasing, until the final-state V_{gs} is reached. In this paper, the end point of t_Q_{gd} is defined as the intercept point of the extended lines of the V_{gs} curves during and after the time interval t_Q_{gd}.

After the time intervals are obtained, the corresponding charges are calculated as the time intervals multiplied by the gate-charge current. The time interval t_Q_{gs2} multiplied by 1 mA gives so-called Q_{gs2}. The time interval t_Q_{gd} multiplied by 1 mA gives so-called Q_{gd}. The time interval t_Q_g multiplied by 1 mA gives the total gate-charge Q_g.

III. Nonlinearities of Gate Charge

Using the evaluation methods in the previous section, the nonlinearities of the total gate-charge Q_g and its sub-components Q_{gd} and Q_{gs2} versus different operating conditions are shown in Fig. 4. The equivalent R_{ds} is evaluated under the same conditions, and it is derived as the ratio of the final-state V_{ds} to the final-state I_{drain}.

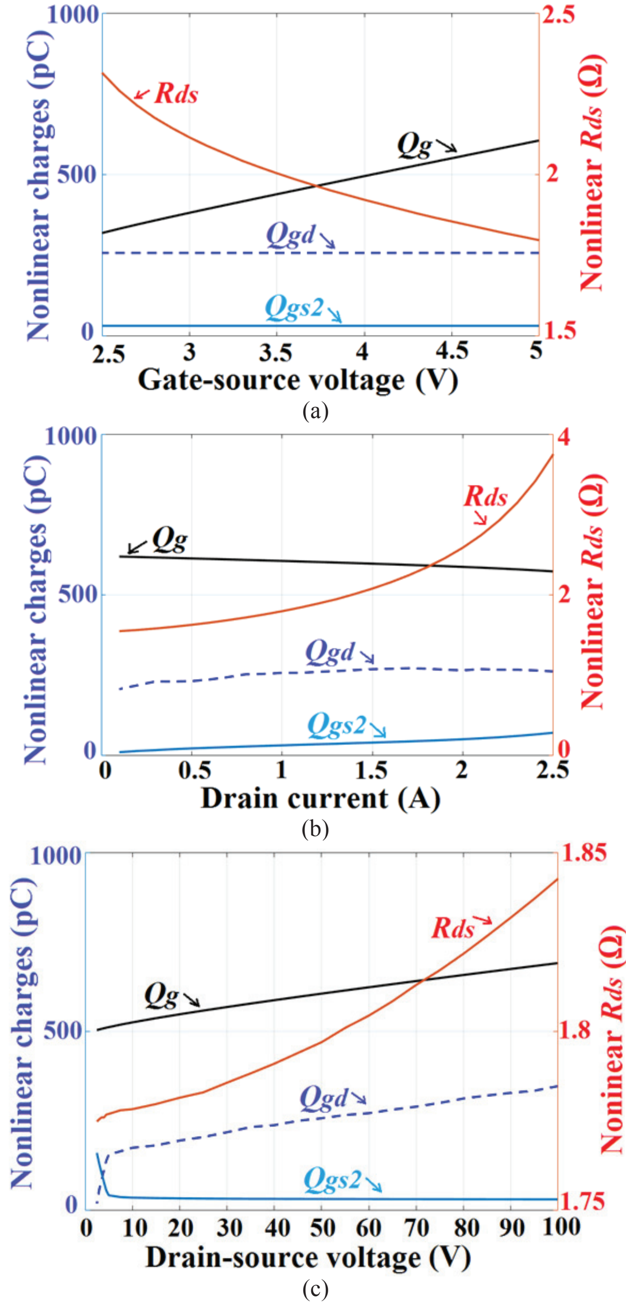

Fig. 4. Gate charge Q_g, its sub-components Q_{gd} and Q_{gs2}, and final-state R_{ds} (simulated). (a) Versus final-state V_{gs} (I_{drain} = 1 A, V_{ds} = 50 V). (b) Versus final-state I_{drain} (V_{gs} = 5 V, V_{ds} = 50 V). (c) Versus original-state V_{ds} (I_{drain} = 1 A, V_{gs} = 5 V).

IV. Optimization of Nonlinear FOMs

The FOMs in (1)-(4) are to be evaluated. FOM_{com1} is commonly used [5], [7]-[9]. FOM_{com2} is also widely accepted [5], [7]. $FOM_{hard\text{-}sw}$ and $FOM_{soft\text{-}sw}$ are proposed in [4] for hard-switching application and soft-switching application, respectively. The soft-switching here generally refers to zero-voltage switching (ZVS) for transistor turn-on transition and/or zero-current switching (ZCS) for transistor turn-off transition.

$$FOM_{com1} = R_{ds} \cdot Q_g \quad (1)$$

$$FOM_{com2} = R_{ds} \cdot Q_{gd} \quad (2)$$

$$FOM_{hard-sw} = R_{ds} \cdot \left(Q_{gd} + Q_{gs2}\right) \quad (3)$$

$$FOM_{soft-sw} = R_{ds} \cdot \left(Q_g + Q_{oss}\right) \quad (4)$$

The output charge Q_{oss} in (4) is analyzed as follows: for

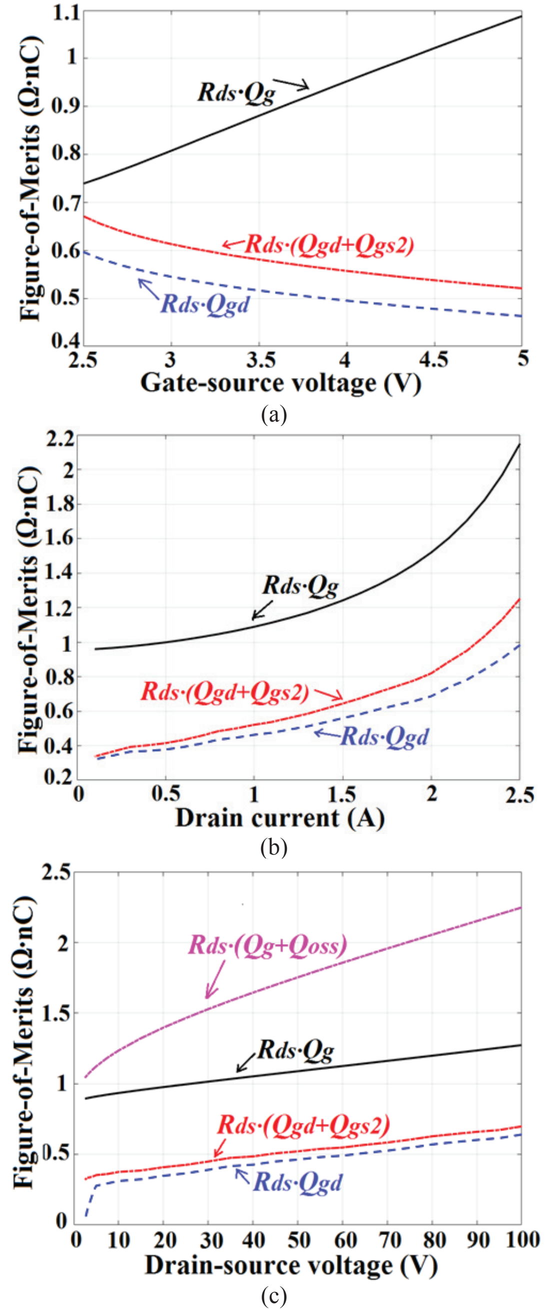

Fig. 5. Nonlinear FOMs (simulated). (a) Versus final-state V_{gs}. (b) Versus final-state I_{drain}. (c) Versus original-state V_{ds}.

TABLE 1. OPTIMIZATION OF NONLINEAR FOMS

Same as in Fig. 5	Best-case FOM vs. Worst-case FOM FOM is lowered: by times (by percentage)			
	FOM_{com1}	FOM_{com2}	$FOM_{hard\text{-}sw}$	$FOM_{soft\text{-}sw}$
V_{gs}	1.5 (32 %)	1.3 (22 %)	1.3 (22 %)	N/A
I_{drain}	2.2 (55 %)	3.0 (67 %)	3.7 (73 %)	N/A
V_{ds}	1.4 (30 %)	18.3 (95 %)	2.2 (54 %)	2.2 (54 %)

the transistor turn-off process, the output capacitance of the power MOSFET is charged to the supply voltage by only a portion of the load current. Therefore, it is difficult to dynamically determine Q_{oss} during the switching transients. Instead, Q_{oss} is estimated with the transistor in the off-state. The gate, source, and bulk terminals are shorted to ground, and the output-charge current is applied to the drain terminal. For the same reason, Q_{oss} (thus $FOM_{soft\text{-}sw}$) is only evaluated versus the drain-source voltage V_{ds}.

The FOMs in (1)-(4) are then derived versus different operating conditions, with the results shown in Fig. 5. The results are also quantitatively summarized in Table 1, versus the same operating conditions as in Fig. 5.

First, the contradicting trends of FOM_{com1} and FOM_{com2} are observed in Fig. 5(a). Another trade-off is between the final-state R_{ds} and the total gate-charge Q_g, as shown in Fig. 4(a). Second, all FOMs in Fig. 5(b) are dominated by R_{ds}. The equivalent R_{ds} increases for high I_{drain} values, due to the quasi-saturation effects and the drain current compression effects [29]. This means that the transistor starts to leave the linear region. Third, Q_{gd} in Fig. 4(c), which dominates FOM_{com2} in Fig. 5(c), quickly vanishes when the original-state (i.e. the state at the start point of the gate-charge event) V_{ds} has a low value (comparable to the V_{gs} values during the time interval t_Q_{gd}). This occurs when the transistor is in the quasi-saturation region before the gate-charge event, with quasi-zero voltage switching. In contrast, if the transistor is forced to be in the linear region, which is closer to the real ZVS, it may not be able to deliver the required final-state I_{drain} or it can deliver the current only after the time interval t_Q_{gd}. Therefore, the operation of the transistor is optimal in the quasi-saturation region rather than deeply in the linear region before the gate-charge event. The maximum improvement of 95 % (theoretically 100 %) is achieved for FOM_{com2}. It indicates that the power MOSFET is suitable for resonant and soft-switching converters (quasi-ZVS is preferred to ZCS).

V. CONCLUSION

A systematic analysis of the optimization of the nonlinear FOMs is performed for a 100 V power MOSFET implemented in a 0.18 μm partial SOI process. The FOMs (compared to the worst-case non-optimized FOMs) are lowered by 1.3-18.3 times and improved by 22-95 % with optimized quasi-zero voltage switching conditions.

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A.4. Publication (PwrSoC, First Prize Award, IEEE PELS)

This is the post-print version of the publication.

Lin Fan, Arnold Knott, Ivan Harald Holger Jørgensen, “Intrinsic Nonlinearities and Layout Impacts of100 V Integrated Power MOSFETs in Partial SOI Process”, in 5th International Workshop on Power Supply on Chip (PwrSoC), 2016.

The final published version is available:
http://pwrsocevents.com/pwrsoc-2016-e-poster-presentations/

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Intrinsic Nonlinearities and Layout Impacts of 100 V Integrated Power MOSFETs in Partial SOI Process

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Abstract

Parasitic capacitances of power semiconductors are a part of the key design parameters of state-of-the-art very high frequency (VHF) power supplies. In this poster, four 100 V integrated power MOSFETs with different layout structures are designed, implemented, and analyzed in a 0.18 μm partial Silicon-on-Insulator (SOI) process with a die area 2.31 mm^2.

A small-signal model of power MOSFETs is proposed to systematically analyze the nonlinear parasitic capacitances in different transistor states: off-state, sub-threshold region, and on-state in the linear region. 3D plots are used to summarize the intrinsic nonlinearities of the power devices. The nonlinear figure-of-merits (FOMs) are lowered by 1.3-18.3 times and improved by 22-95 % with optimized conditions of quasi-zero voltage switching. The layout impacts of the on-chip interconnections are analyzed with post-layout comparisons.

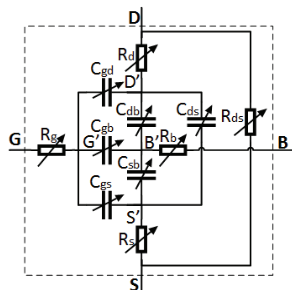

Figure 1. Proposed small-signal model of power MOSFETs (off-state, sub-threshold region, and on-state in the linear region)

Intrinsic Nonlinearities in Frequency-Domain

(Nonlinear Capacitances @ 1 MHz)

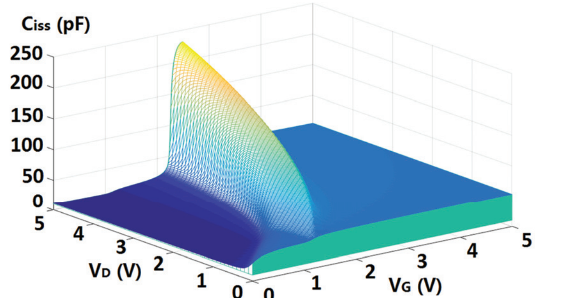

Figure 2. Nonlinearities of C_{iss} (off-state, sub-threshold region, and on-state in the linear region)

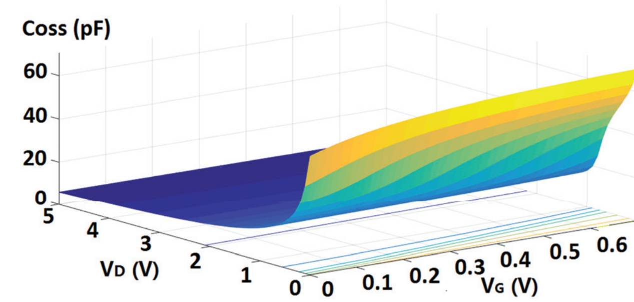

Figure 3. Nonlinearities of C_{oss} (off-state and the gate voltage is much lower than the threshold voltage)

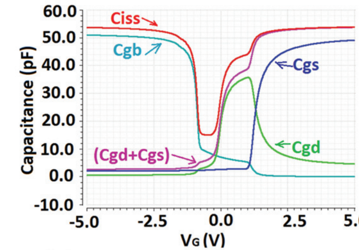

Figure 4. Nonlinear parasitic capacitances looking into the gate terminal ($V_D = V_B = V_S = 0$ V)

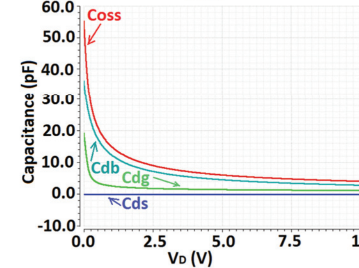

Figure 5. Nonlinear parasitic capacitances looking into the drain terminal (off-state, $V_G = V_B = V_S = 0$ V).

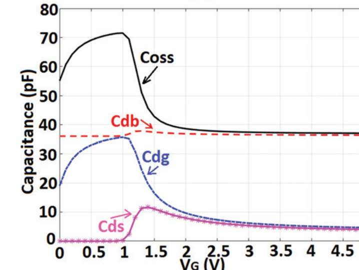

Figure 6. Nonlinear parasitic capacitances looking into the drain terminal (on-state in the linear region, or in the sub-threshold region, as well as off-state, $V_D = 1$ μV, $V_B = V_S = 0$ V).

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Intrinsic Nonlinearities in Time-Domain

(Nonlinear Gate Charges and FOMs)

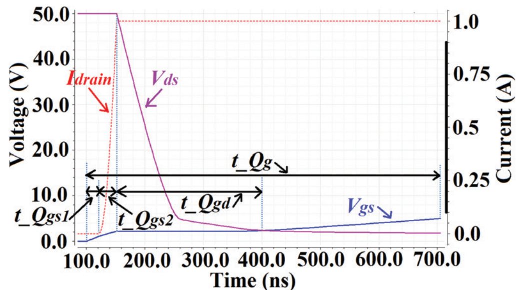

Figure 7. Simulated transient waveforms and naming conventions.

$$FOM_{com1} = R_{ds} \cdot Q_g \quad (1)$$

$$FOM_{com2} = R_{ds} \cdot Q_{gd} \quad (2)$$

$$FOM_{hard-sw} = R_{ds} \cdot (Q_{gd} + Q_{gs2}) \quad (3)$$

$$FOM_{soft-sw} = R_{ds} \cdot (Q_g + Q_{oss}) \quad (4)$$

Same as in Fig. 9	Best-case FOM vs. Worst-case FOM FOM is lowered: by times (by percentage)			
	FOM_{com1}	FOM_{com2}	$FOM_{hard-sw}$	$FOM_{soft-sw}$
V_{gs}	1.5 (32 %)	1.3 (22 %)	1.3 (22 %)	N/A
I_{drain}	2.2 (55 %)	3.0 (67 %)	3.7 (73 %)	N/A
V_{ds}	1.4 (30 %)	18.3 (95 %)	2.2 (54 %)	2.2 (54 %)

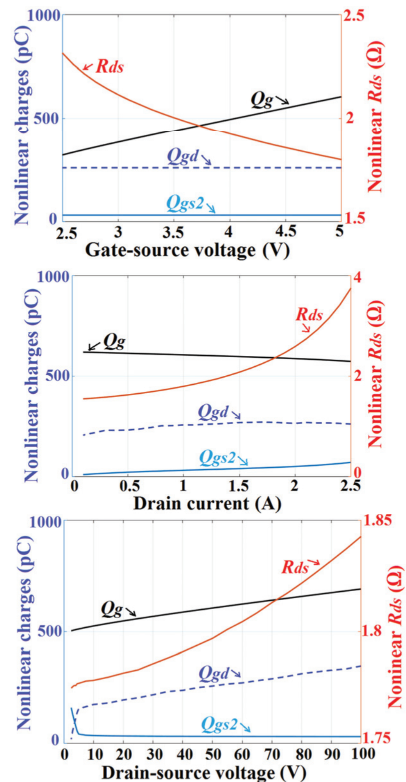

Figure 8. Gate charge Q_g, its sub-components Q_{gd} and Q_{gs2}, and final-state R_{ds} (simulated).
(a) Versus final-state V_{gs}
(b) Versus final-state I_{drain}
(c) Versus original-state V_{ds}

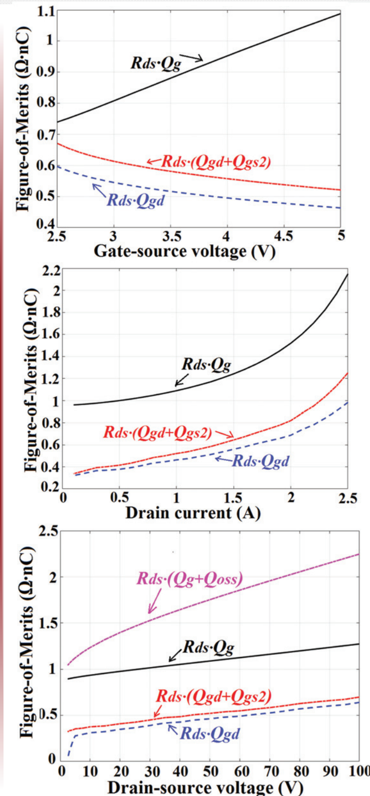

Figure 9. Nonlinear FOMs (simulated).
(a) Versus final-state V_{gs}.
(b) Versus final-state I_{drain}.
(c) Versus original-state V_{ds}.

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Layout Structure Impacts

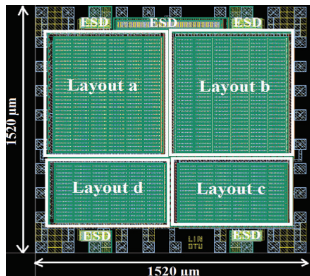
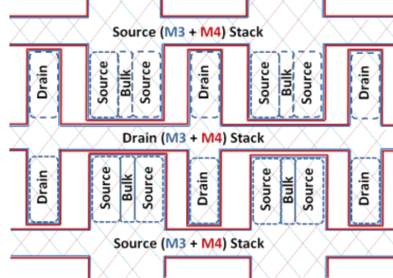


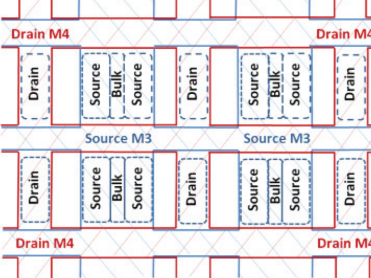
Figure 10. Layout of the chip design (proposed structures are highlighted)

R/C	Top chip-level (including chip-pads and ESD protections)					
	Schematic *a* & *b*	Post-Layout *a*	Post-Layout *b*	Schematic *c* & *d*	Post-Layout *c*	Post-Layout *d*
Parasitic	No	2D Extract	2D Extract	No	2D Extract	2D Extract
$R_{ds(on)}$ (Ω)^a	1.542	2.071	2.250	3.085	3.354	3.295
$C_{g\text{-}sb}$ (pF)^b	21.3	46.9	49.5	11.5	25.1	26.7
C_{gd} (pF)^b	38.1	41.4	39.3	19.1	20.6	20.6
C_{iss} (pF)^b	59.4	92.7	93.2	30.6	48.0	48.9
$C_{d\text{-}sb}$ (pF)^c	72.1	88.4	85.7	36.0	47.6	48.0
C_{dg} (pF)^c	38.1	41.4	39.3	19.1	20.6	20.6
C_{oss} (pF)^c	110.2	132.1	127.6	55.1	69.5	69.8
$R_{ds(on)}$-C_{iss} (ps)	91.6	192.0	209.7	94.4	161.0	161.1
$R_{ds(on)}$-C_{oss} (ps)	169.9	273.6	287.1	170.0	233.1	230.0

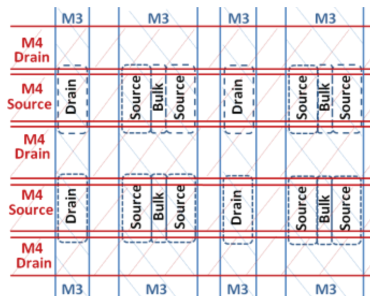
Layout *a*:
Drain/Source horizontal connection,
Mainly side-by-side coupling.



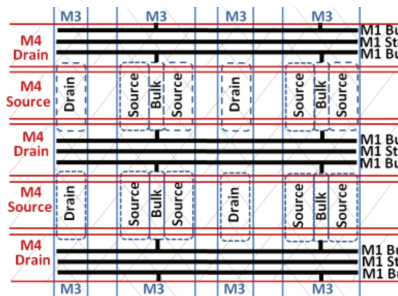
Layout *b*:
Drain/Source horizontal connection,
Mainly layer-to-layer coupling.



Layout *c*:
Drain/Souce vertical connection,
Perpendicular mesh structure



Layout *d*:
Drain/Souce structure the same as *c* *but* Bulk as a seperate terminal.



Key Contributions

1) Systematically analyzed the nonlinear parasitic capacitances of integrated high voltage power MOSFETs in a partial SOI process.
2) A modeling method is proposed for analyses in different transistor states, whereas industrial datasheets typically specify only off-states.
3) Parasitic capacitances towards bulk can dominate over parasitic capacitances towards source.
4) The nonlinear FOMs are lowered by 1.3-18.3 times and improved by 22-95 % with optimized quasi-zero voltage switching conditions.
5) Parasitic capacitances of on-chip interconnections could dominate over intrinsic capacitances of power devices.
6) Side-by-side coupling dominated layout structures may perform better than layer-to-layer coupling dominated layout structures.

Acknowledgment:
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[1] **L. Fan**, A. Knott, and I.H.H. Jørgensen, "Nonlinear parasitic capacitance modeling of high voltage power MOSFETs in partial SOI process," ISI-indexed Research Journal Elektronika ir Elektrotechnika, Vol. 22, No. 3, pp. 37-43, June 2016.
[2] **L. Fan**, A. Knott, and I.H.H. Jørgensen, "Layout capacitive coupling and structure impacts on integrated high voltage power MOSFETs," IEEE PRIME conference, June 2016.
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A.5. Publication (journal and conference, accepted)

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And

Lin Fan, Arnold Knott, Ivan Harald Holger Jørgensen, “A 380 V High Efficiency and High Power Density Switched-Capacitor Power Converter using Wide Band Gap Semiconductors”, in 16th International Conference on Renewable Energies and Power Quality, 2018.

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Renewable Energy and Power Quality Journal (RE&PQJ)
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A 380 V High Efficiency and High Power Density Switched-Capacitor Power Converter using Wide Band Gap Semiconductors

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Abstract. State-of-the-art switched-capacitor DC-DC power converters mainly focus on low voltage and/or high power applications. However, at high voltage and low power levels, new designs are anticipated to emerge and a power converter that has both high efficiency and high power density is highly desirable. This paper presents such a high voltage low power switched-capacitor DC-DC converter with an input voltage up to 380 V (compatible with rectified European mains) and an output power experimentally validated up to 21.3 W. The wide band gap semiconductor devices of GaN switches and SiC diodes are combined to compose the proposed power stage. Their switching and loss characteristics are analyzed with transient waveforms and thermal images. Different isolated driving circuits are compared and a compact isolated half-bridge driving circuit is proposed. The full-load efficiencies of 98.3% and 97.6% are achieved for the power stage and the complete power converter, without heatsink or airflow. The corresponding power densities are 7.9 W/cm^3 and 2.7 W/cm^3, based on boxed volumes, respectively.

Key words

Switched capacitor circuits, DC-DC power converters, Gallium nitride, Silicon carbide, Wide band gap semiconductors.

1. Introduction

Industrial and consumer electronics keeps demanding smaller and lighter power supplies [1]. One of the principle approaches is to design power converters that consist of switches and capacitors. Research on switched-capacitor circuits has been commenced since 1930s [2]. Afterwards, switched-capacitor converters have been investigated for memory applications on IC (Integrated Circuit) in 1970s [3]. Research on state-of-the-art switched-capacitor DC-DC converters has focused on low voltage and/or high power applications, majority of which are implemented on ICs [4]-[6]. For switched-capacitor power converters that have voltage and power levels above 12 V and 2 W, discrete power converters are commonly implemented by academia [8],[9] and industry [10]. Recent advances in switched-capacitor DC-DC power converters are up to a 200 V input voltage with output powers of 30-53 W [11],[12]. Switched-capacitor DC-DC power converters at further higher input voltage and lower output power level are anticipated to emerge. This paper presents a 380 V input voltage (compatible with European 220-240 Vrms AC operation with ±10% tolerance) switched-capacitor DC-DC power converter, which is intended to be used as the voltage conversion stage for LED (light-emitting diode) drivers. This paper focuses on the high efficiency and high power density design of the complete power converter (i.e. the power stage with the driving circuit included). For high voltage, low current applications, the switching loss becomes significant. The wide band gap semiconductors, i.e. GaN (Gallium Nitride) switches and SiC (Silicon Carbide) diodes are combined to properly address both conduction loss and switching loss, in order to achieve both high efficiency and high power density.

This paper presents a switched-capacitor DC-DC power converter that consists of a power stage and its driving circuit. The target is to achieve both high efficiency and high power density for the complete power converter. In section 2, the proposed power stage and its basic operation principle is introduced. The consideration of the off-state leakage is also elaborated and discussed. In section 3, different driving circuit topologies are analyzed and compared. An isolated half-bridge driving circuit is chosen to achieve high power density. In section 4, the complete power converter is implemented. The choice of the components and the PCB design considerations are illustrated. In section 5, the proposed power converter is experimentally validated. The measurement methods and results are presented. Thermal images and oscilloscope waveforms are used to analyze and compare the behavior of the wide band gap semiconductors. The measured efficiency and power density of the prototype converter are summarized. Section 6 concludes the paper.

2. Power Stage

The power stage is the core design of the complete power converter. The proposed power stage is shown in Fig. 1.

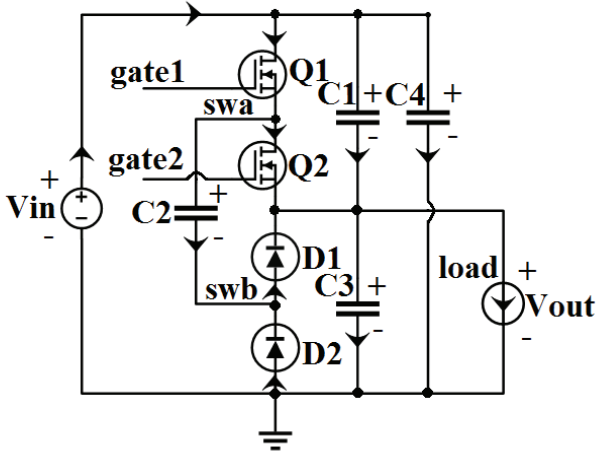


Fig. 1. Proposed power stage of switched-capacitor DC-DC converter for high voltage low power applications

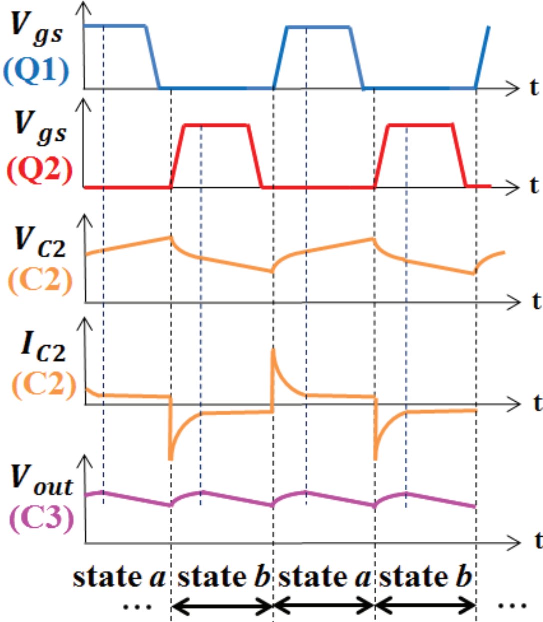


Fig. 2. Key waveforms of the proposed power stage (two main operation states are annotated with state *a* and stage *b*)

The power stage has a DC-DC voltage conversion ratio of 2:1 from the input voltage to the output voltage. It consists of two switches (*Q1*, *Q2*), two diodes (*D1*, *D2*), and four capacitors (*C1*-*C4*). The switches *Q1* and *Q2* are the main control devices. The diodes *D1* and *D2* facilitate the charge transfer to and from the capacitor *C2*, with *Q1* and *Q2*, respectively. The capacitors *C1* and *C3* serve as both input and output capacitors while balancing the charge transfer loops. The capacitor *C4* adds further decoupling capability (in addition to *C1* and *C3*) to filter out high frequency noise of the input supply. This topology is in contrast to the conventional all-transistors switched-capacitor DC-DC converters. For high characteristic impedance (high voltage, low current) applications, by analyzing the direction of the current flow, some of the switches may suitably be implemented with diodes, which reduces switching loss and gating loss while constraining conduction loss. Therefore, high efficiency and high power density can be achieved with the proposed power stage, while the ultimate trade-off between the efficiency and the power density depends on the components used to implement the power converter and the PCB design.

The waveforms of the proposed power stage are shown in Fig. 2. The power stage operates with complementary fixed 50% duty cycle gate-source signals for the two switches *Q1* and *Q2*. There is a slight dead time between the two gate-source signals. The optimal dead time is tuned for optimizing the efficiency. The dead time cannot to be too long, to avoid the transient period when the output current is solely provided by the output capacitors (*C1*, *C3*), which further reduces the efficiency of the energy transfer of the power stage. A too short dead time is also not desired, to prevent shoot-through loss. An undesired shoot-though condition can also be triggered by improper dead time timing, together with the parasitic capacitances, resistances and inductances of the transistors, gate drivers, packages and PCB layout, where a switch under turning-off transients can suffer from the dv/dt-induced turn on and the di/dt-induced turn on [13].

The basic operation principle of the power stage is identified with two operating states (state *a*, state *b*). In state *a*, the pair *Q1*/*D1* is on and the pair *Q2*/*D2* is off, the energy transfer capacitor *C2* is charged while providing the load current. In state *b*, the pair *Q2*/*D2* is on and the pair *Q1*/*D1* is off, the energy transfer capacitor *C2* is discharged to supply the load current. The capacitors *C1* and *C3* always charge and discharge in opposite ways because the sum of their voltages equals to the input voltage. During each of the state *a* and the state *b*, *C3* charges then discharges while *C1* discharges then charges. Therefore, the output voltage ripple of the power stage is at the double frequency of the switching frequency of the switches *Q1* and *Q2*. Due to the charge balance of the energy transfer capacitor *C2* in steady state, the average current of *C2* equals to zero.

$$I_{C2} = \frac{1}{T_s}\int_0^{T_s} i_{C2} \cdot dt = 0 \tag{1}$$

However, the current flows through C2 in opposite directions for each of the 50% duty cycles. The average of the absolute current of *C2* equals to the DC output current.

$$\left|I_{C2}\right|_{avg} = \frac{1}{T_s}\int_0^{T_s}\left|i_{C2}\right| \cdot dt = \frac{1}{T_s/2}\int_0^{T_s/2}\left|i_{C2}\right| \cdot dt = I_{out} \tag{2}$$

Considering the current of *C2* conducts through either the pair *Q1*/*D1* or the pair *Q2*/*D2* during a 50% duty cycle period, the average current of these devices is half of the output DC current.

$$I_{Q1} = I_{D1} = I_{Q2} = I_{D2} = \frac{1}{T_s}\int_0^{T_s/2}\left|i_{C2}\right| \cdot dt = I_{out}/2 \tag{3}$$

Then the peak-to-peak voltage ripple of *C2* can be calculated, which is shown to be inversely proportional to the capacitance of *C2* and the switching frequency, and it is proportional to the output load current.

$$\Delta V_{C2} = \frac{1}{C2}\int_0^{T_s/2}\left|i_{C2}\right| \cdot dt = \frac{\left(I_{out}/2\right) \cdot T_s}{C2} = \frac{I_{out}}{2 \cdot C2 \cdot f_s} \tag{4}$$

It may seem that if designers choose *C1* and *C3* to have an equal capacitance value, then at no load condition when all switches are off, the capacitor divider of *C1* and *C3* may automatically balance the output voltage to be half of the input voltage. However, this does not happen in practice due to the leakage of the devices (in the µA range).

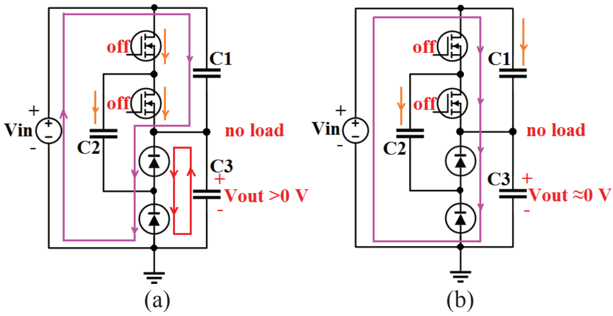


Fig. 3. Leakage current paths at no load condition when all switches are off (e.g. before start-up, or after turn-off). (a) *C3* is not fully discharged. (b) C3 is fully discharged.

The main leakage paths are shown in Fig. 3 when an input voltage is applied to the circuit under discussion. In Fig. 3(a), there are still residual charges stored on *C3*, and these charges on *C3* are mainly discharged by the reverse current of the diodes. When *C3* discharges, *C1* is charged by the input supply, and the charge current also flows through the reverse biased diodes. The drain-source leakage current of the switches and the leakage current of *C2* are relatively small and may be negligible in this case. In Fig. 3(b), C3 is fully discharged, and the majority of the leakage current passes through the switches and the diodes. These devices individually carry different leakage current and the bottom diode carries the highest leakage current. In either case of Fig. 3(a) and Fig. 3(b), the capacitor *C1* is eventually charged to the input voltage and has to withstand it. Therefore, the voltage rating of the capacitor *C1* (without adding extra component or circuitry) is determined by the input voltage, rather than its steady state operating voltages.

3. Driving Circuit

After the power stage is designed, designing its driving circuits is another challenge. The conventional bootstrap circuits are not suitable for the proposed power stage. First, the diodes *D1* and *D2* are utilized in the power stage to complete the charge transfer loops, and there are no conventional low-side switches that can be used to charge the high-side bootstrap capacitors. Second, though the load current might be used in series with the charge path of a bootstrap capacitor, the voltage of the highest bootstrap capacitor suffers most from the voltage drop of the bootstrap diodes [10], which may not ensure an adequate gate-drive voltage or even trigger an under-voltage lockout by its voltage ripple, which is in turn caused by transistor gate charge, driver supply bias current, transistor gate leakage, diode reverse leakage, and other leakage current [14].

The possible driving circuits for the proposed power stage are shown in Fig. 4. In Fig. 4(a), digital isolators are used in series with conventional low-side gate drivers [11],[15], to provide isolated high-side gate signals to the switches *Q1* and *Q2*. If each switch has its own digital isolator and gate driver, then 4 components are needed to drive 2 switches. In addition, if one pair of digital isolator and gate driver shares the same isolated supply, as shown in Fig. 4(a), then in total 6 components are required to complete the driving circuit.

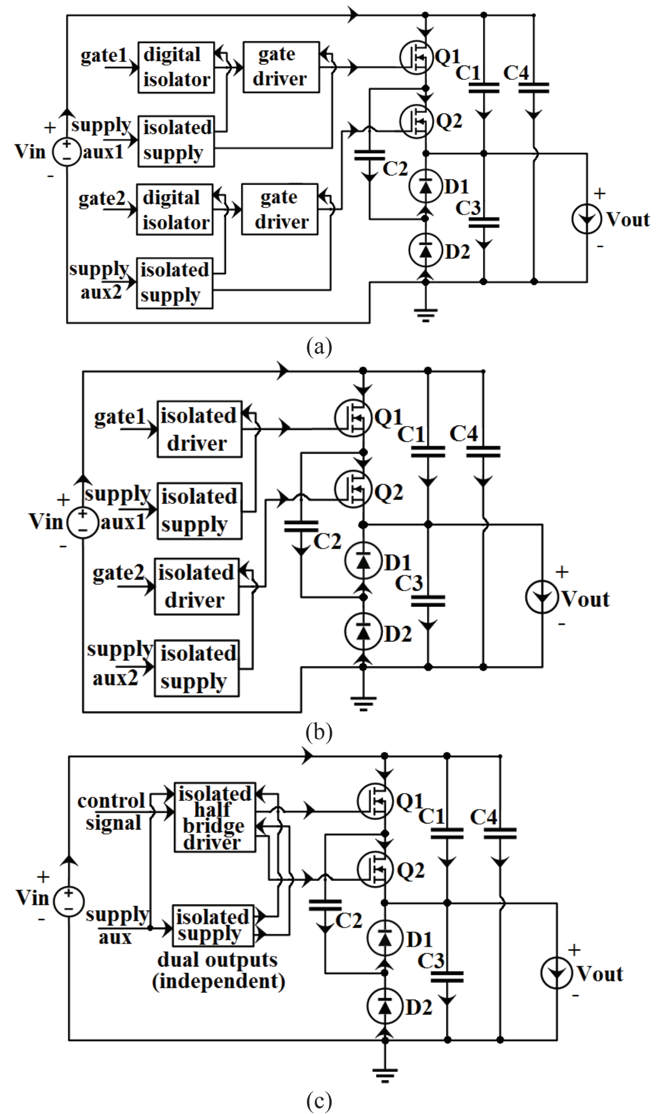


Fig. 4. Possible driving circuits for the power stage. (a) Using digital isolators with conventional low-side gate drivers. (b) Using single-channel isolated gate drivers. (c) Proposed driving circuit, using a single isolated half-bridge gate driver.

In Fig. 4(b), two single-channel isolated gate drivers are used to replace the corresponding two pairs of digital isolator and gate driver [16]. In this case, if each isolated gate driver has its own isolated supply, then in total 4 components are used to compose the driving circuit. To further improve the integration level thus the power density of the converter, the driving circuit in Fig. 4(c) is proposed. Because the switches *Q1* and *Q2* are driven complementary with fixed 50% duty cycle, as discussed in the previous section, the driving circuit for these two switches is suitable for implementation with an isolated half-bridge gate driver. Furthermore, an isolated supply with dual independent outputs is used to provide supplies for the individual outputs of the gate driver. As a result, with only 2 components the driving requirements of the power stage are fulfilled and high power density is thus achieved.

4. Implementation of Complete Converter

The complete power converter can now be synthesized with the power stage and the driving circuit.

Table I. Components for the prototype converter

Component	Technology	Specification
Switches *Q1*, *Q2*	Gallium Nitride (GaN)	EPC2012C, EPC 200 V, 5 A, 100 mΩ
Diodes *D1*, *D2*	Silicon Carbide (SiC)	C3D1P7060Q, CREE 600 V, 3.3 A, 4 nC
Capacitors *C1*, *C3*	Multi-Layer Ceramic Capacitor (MLCC)	450 Vdc, 1 μF, ±10% X7T, TDK
Capacitor *C2*	Multi-Layer Ceramic Capacitor (MLCC)	250 Vdc, 10x 1 μF, ±10% X7T, TDK
Capacitor *C4*	Multi-Layer Ceramic Capacitor (MLCC)	450 Vdc, 0.22 μF, ±20% X7T, TDK
Gate Driver	Capacitive-isolated (with dies)	SI8274GB1-IM, 4 A, 2.5 kVrms, Silicon Labs
Driver Supply	Inductive-isolated (with transformer)	R1DA-3.30505, 1 W, 1 kVdc, RECOM Power

A prototype of the switched-capacitor power converter is implemented with the key components listed in Table I. The switches *Q1* and *Q2* are GaN devices. The diodes *D1* and *D2* are SiC devices. The capacitors *C1*-*C4* are all ceramic capacitors. The isolated gate driver has pull-down transistors with 1.0 Ω equivalent on-resistance, and pull-up transistors with 2.7 Ω equivalent on-resistance, resulting in peak output current of 4.0 A and 1.8 A, respectively. It has a minimum CMTI (Common Mode Transient Immunity) rating of 150 V/ns, to facilitate the fast dv/dt transients of the GaN and SiC devices. The isolated power supply has dual independent outputs. Each of the outputs has a maximum output current rating of 100 mA, which is excessively over-designed for the converter and causes unnecessary low efficiencies operating at light load conditions, and the choice is due to the availability of the components.

All components are SMD (Surface-Mount Devices). The PCB of the prototype converter is designed with 2-layers (industry-standard conductor track widths, conductor spacing distances, and through hole diameters), where the components are mounted on both sides of the PCB, to minimize the charge transfer loops and the power loops. The thickness of the PCB is 1.0 mm, with trade-offs between parasitic inductance of vias, heat dissipation capability, cost and mechanical reliability. A copper thickness of 2 oz is used to trade-off conduction loss and solder joint reliability. The surface finish of ENIG (Electroless Nickel Immersion Gold) is used to improve the planarity and the fine-pitch capability of the copper pads for the LGA (Land Grid Array) devices, e.g. the isolated gate driver.

5. Experimental Results

The experimental setup of the test bench is shown in Fig. 5. The digital multimeters 34401A are employed for the efficiency measurements. For the highest accuracy of 34401A, the full 6½ digits resolution and the manual ranging are used. The prototype of the power converter under test is shown in Fig. 6. The default ground leads of the oscilloscope probes are not used because of the signal-ground loop inductances. Instead, local ground connections are custom-made to minimize the loops for more accurate transient measurements.

The measured efficiency of the power stage and the complete power converter is shown in Fig. 7, with a switching frequency of 1 kHz for the switches *Q1* and *Q2*. The total efficiency includes the power consumption of the driving circuit (i.e. the gate driver and the isolated supply), which is about 153-159 mW. All the efficiency measurements are made at the room ambient temperature, without any heatsink or any airflow. The full-load power stage efficiency is 98.3%, and the efficiency of the complete power converter at the full-load is 97.6%. The efficiency of the complete power converter at the 10%-100% load range is always above 90%. The efficiency is measured up to an output power of 21.3 W, which is limited by the multimeters rather than the converter itself. The reading accuracy of 34401A measuring a DC current with the 1 A range (0.1 Ω shunt resistor) is 5 times worse than with the 100 mA range (5 Ω shunt resistor) [17]. The accuracy of the measurement of the input and output power is highly demanded for the resulting maximum absolute error in the efficiency, where the losses are determined indirectly. A direct measurement of losses by means of a calorimeter [18] may be of consideration for high efficient power converters.

The measure peak temperature of the hottest spot on the PCB is also shown in Fig. 7. The efficiency increases with the output power at high temperatures. This is mainly caused by the temperature effects of the SiC diodes. SiC diodes typically have positive temperature coefficient at high current levels. However, at low current levels (as in the proposed high voltage low current power converter), the temperature coefficient of the SiC diodes becomes negative [19],[20], i.e. for a given forward current, the forward voltage becomes less at a higher temperature. This phenomenon happens for a limited low-forward-current range of the SiC diodes, and it contributes to reduce the conduction loss, which is the dominated loss at high output power levels for the proposed power converter.

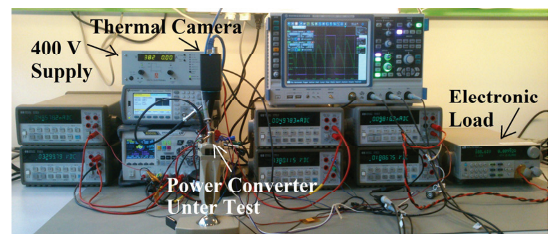


Fig. 5. Experimental setup of the test bench

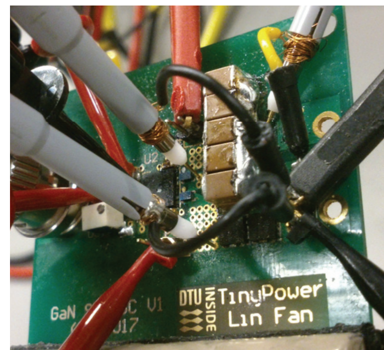


Fig. 6. Prototype converter under test (local ground connections are custom-made for oscilloscope probes)

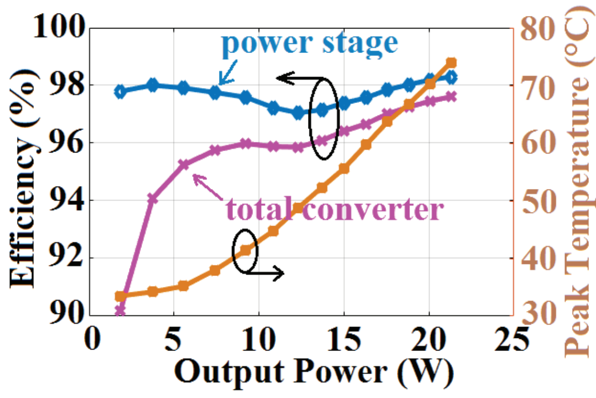
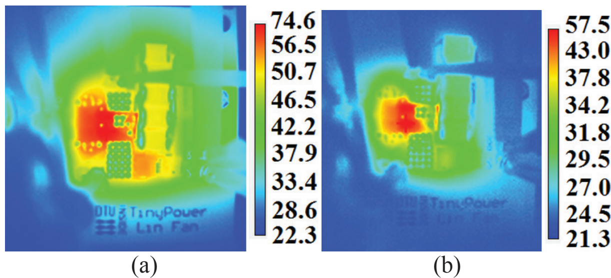


Fig. 7. Measured efficiency of the power stage and the complete power converter (including gate driver and isolated supply) vs. output power. No heatsink, no airflow, with the peak temperature of the hottest spot on the PCB.

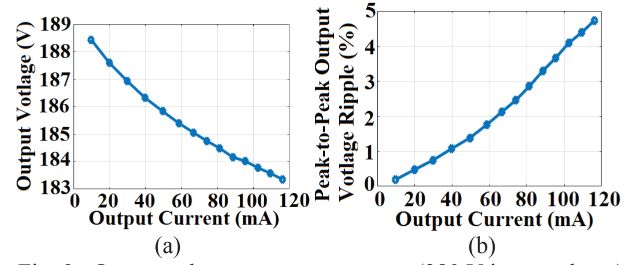
This is further experimentally validated with thermal measurements. The thermal images of the power converter operating at 380 V input voltage and 21.3 W output power are shown in Fig. 8. In Fig. 8(a), the thermal image is measured after one hour full-power operation without any airflow. The peak temperature is 74.6 °C and the measured efficiency of the power stage is 98.3%. After adding forced airflow, the thermal image is measured again and shown in Fig. 8(b). The peak temperature is 57.5 °C, and the measured efficiency of the power stage is 97.8%. For the same constant load current of the power stage, the negative temperature coefficient of the SiC diodes increases the forward voltage drop at a low temperature, which increases the conduction loss and decreases the resulting efficiency.

The measured DC output voltage and the peak-to-peak output voltage ripple with respect to it versus the output current are shown in Fig. 9(a) and Fig. 9(b), respectively. As the output current rises, the conduction loss increases accordingly and the DC output voltage decreases for a given implementation of the power converter at a fixed switching frequency. The peak-to-peak output voltage ripple (thus the corresponding percentage with respect to the DC output voltage) rises as the output current increases, as expected, because the same amount of capacitance is loaded with more current for a fixed switching period. The waveform of the peak-to-peak voltage ripple measured at a worst-case full-load current of 116 mA is shown in Fig. 10. The 3.3 V control signal is shown as a reference signal for the switching period. The output voltage ripple has a double frequency of the control signal frequency, as previously discussed.



(a) (b)

Fig. 8. Thermal images (°C) measured at 380 V input voltage, 21.3 W output power. (a) No airflow, measured after one hour full-power operation. (b) With forced airflow.



(a) (b)

Fig. 9. Output voltage vs. output current (380 V input voltage). (a) DC output voltage. (b) Peak-to-Peak output voltage ripple.

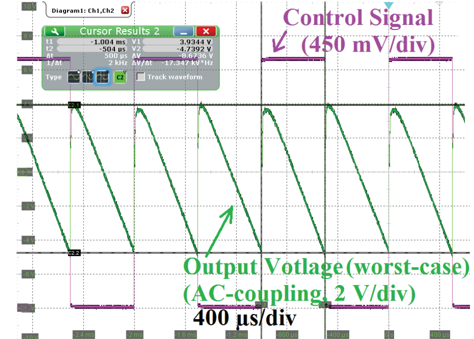


Fig. 10. Waveforms of peak-to-peak output voltage ripple (at a double frequency of the control signal)

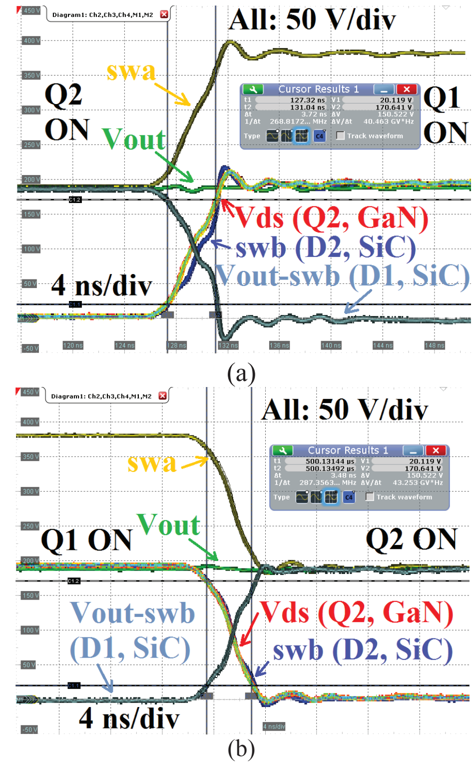


Fig. 11. Measured waveforms of switching transients, with comparisons of GaN device and SiC device. (a) *Q1*-on/*Q2*-off transient. (b) *Q2*-on/*Q1*-off transient.

Table II. Volumes and power densities of the prototype

	Power Stage	Total Power Converter
Dimension as Cuboid	14.55 mm 21.70 mm 8.50 mm	27.70 mm 21.70 mm 13.00 mm
Boxed Volume	2.68 cm^3	7.81 cm^3
Power Density	7.9 W/cm^3 (130 $W/inch^3$)	2.7 W/cm^3 (45 $W/inch^3$)

The waveforms of the switching nodes (*swa*, *swb*, as shown in Fig. 1) are measured using the probes with the custom-made local ground connections (as shown in Fig. 6). The results are summarized in Fig. 11. The average slew rate of the switching signals is about 40-43 V/ns. The GaN switch (*Q2*) is switching at a similar dv/dt rate as the SiC diode (*D2*), with slightly faster rise and fall time (<0.2 ns). The GaN device and the SiC device are combined and shown to work well in the proposed power converter.

The attainable power density of the power converter depends on the PCB layout design as well as the circuit topology and the realizing components. The volumes and the power densities of the power stage and the complete power converter of the implemented prototype are summarized in Table II. The power density of the power stage achieves 7.9 W/cm^3, and the power density of the complete power convert is 2.7 W/cm^3. The boxed volume is used to calculate the power density and it is mainly limited by the height of the energy transfer capacitor *C2* for the power stage and the height of the isolated supply for the complete power converter. The boxed volume of the prototype has further improvement possibilities.

6. Conclusion

This paper presents a switched-capacitor DC-DC power converter with an input voltage up to 380 V and an output power experimentally validated up to 21.3 W. The wide band gap semiconductor devices of GaN switches and SiC diodes are combined to compose the proposed power stage for high voltage low power applications. Different isolated driving circuits are analyzed and compared and an isolated half-bridge driving circuit is proposed to achieve high power density. Switching and loss characteristics of the wide band gap semiconductors are analyzed with transient waveforms and thermal images. The full-load efficiency of the complete power converter (including driver and supply) is 97.6%, without heatsink or airflow, and the power densities of the power stage and the complete power converter are 7.9 W/cm^3 and 2.7 W/cm^3, respectively.

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A.6. Publication (journal and conference, accepted, second author)

This is the post-print version of the publication.

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And

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Renewable Energy and Power Quality Journal (RE&PQJ)
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Evaluation of custom-designed lateral power transistors in a silicon-on-insulator process in a synchronous buck converter

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***Abstract*—Most of todays power converters are based on power semiconductors, which are built in vertical power semiconductor processes. These devices result in limited packaging possibilities, which lead to physically long galvanic connections and therefore high external electromagnetic fields. These fields compromise power quality significantly. Therefore this paper examines the possibility to use lateral silicon-on-insulator power MOSFETs and uses the custom-made devices in a 48 V to 12 V synchronous buck converter in continuous conduction mode. The converter is designed based on custom made power transistors, implemented and verified by experimental results. The resulting efficiency of the 1 W converter is around 93 % across a wide load range and its temperature rise is less the 10 °C. This leads to the conclusion, that modern lateral silicon-on-insulator power processes allow high integration of power stages and therefore promise lower emissions, leading to higher power quality.**

***Index Terms*—power semiconductors, vertical semiconductor process, lateral semiconductor process, silicon-on-insulator process, buck converter**

I. Introduction

Modern power semiconductor transistors are often constructed as vertical devices. [1]–[3] The advantage of vertical devices are very low on-resistances $R_{DS_{on}}$ in combination with low gate charges Q_g, therefore resulting in a low figure of merit FOM, where $FOM = R_{DS_{on}} \cdot Q_g$. The FOMs of several processes can be compared to each other for a given maximum device voltage, as a bigger gate area increases the width of the channel, therefore effectively reducing its $R_{DS_{on}}$, but negatively affecting the gate charge Q_g due to the increased plate areas of the gate facing the channel. These plates effectively create the input capacitance C_{iss} and represent the gate charge Q_g.

Within all other integrated circuit design areas, such as Complementary Metal Oxid Semiconductors (CMOS), such as [4]–[7], lateral devices are state-of-the-art. Figure 1 shows a simplified representation of a vertical and a lateral Metal Oxid Semiconductor Field Effect Transistor (MOSFET).

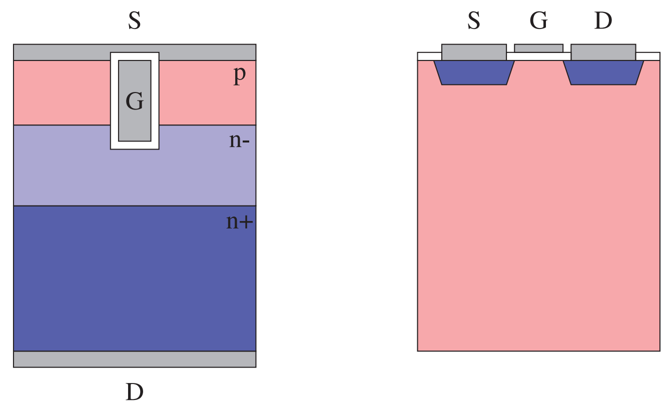

Fig. 1. Simplified example of crosssection of the die of a vertical (left side) and a lateral (right side) power n-channel MOSFET, where D is drain, G is gate and S is source. The coloring and n+, n- and p are indicating the doping of the semiconductor. The bulk connection in the lateral device is neglected.

The vertical n-channel device on the left side of Fig. 1 is using the whole die thickness and the n-doped wafer provides plenty of electrons to be flushed into the channel, when attracted by a positive potential applied between gate (G) and (S) source, hence a low resistance between drain (D) and source (S), i.e. low $R_{DS_{on}}$.

The lateral device on the right side of Fig. 1 is built on a p-doped wafer, where the number of free electrons to be attracted to the channel between drain (D) and and source (S) are rather low. However in this case, the backside of the die - called bulk (B) - has no electrical function and is typically tied to the lowest potential of the implemented circuit, which is the

source of the power MOSFET in this case.
For building a power stage, many power converter topologies, such as synchronous buck, synchronous boost, half-bridge and full-bridge, require two stacked power transistors. These stacked power transistors are the power stage inside those topologies and are called half-bridge or switching pole. Figure 2 shows such a half-bridge configuration.

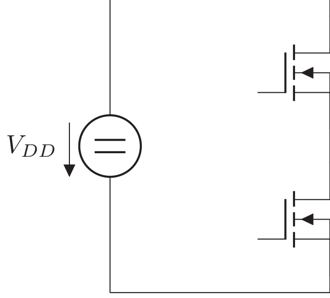

Fig. 2. Half bridge switch-mode power stage realized with two n-channel MOSFETs.

When connecting two vertical MOSFETS in such a half-bridge configuration, the top-metallization of the low-side device is connected to ground and the backside metallization of the other die is connected to the supply voltage V_{DD}. Furthermore, the backside of the die of the low-side MOSFET needs to be shorted to the topside of the high-side MOSFETs die. This node is the switch node, which is carrying a high $\frac{dI}{dt}$ and $\frac{dV}{dt}$. Figure 3 is visualizing these connections.

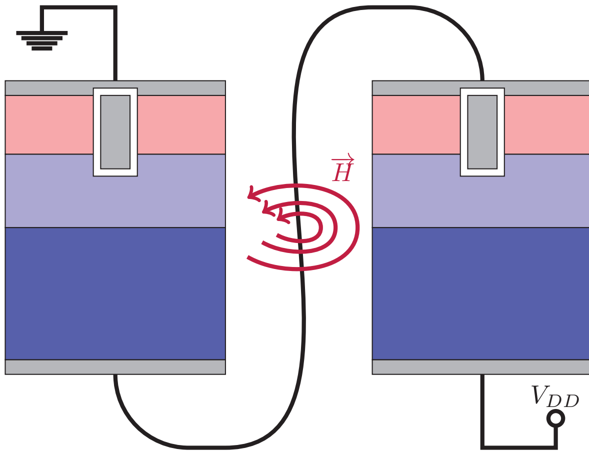

Fig. 3. Parasitics inductance and resulting magnetic field through connection of two vertical MOSFETs in a half bridge configuration

Especially the $\frac{dI}{dt}$ running in this connection generates a magnetic field $\vec{H}$, which is defined by equation 1:

$$\vec{H} = \oint \frac{dI}{dt} dl. \quad (1)$$

If the path l, which the alternating current (AC) is flowing along, is long, the area between the forward and the return path of the loop is big and therefor the integral on the right side of the equation is big.
In the case of vertically implemented MOSFETs, the physical path, where this current flows is rather large, as it consists of a number of mechanical connections:

- drain connection of die of low-side device
- package
- printed circuit board
- source pin of high-side device
- lead frame of high side device
- source bonding wire of high-side device
- routing in metal of high-side source

Therefore the resulting $\vec{H}$-field is rather big, which results in a significant contribution to radiated electromagnetic emissions, which can potentially couple into other circuits in the same system [8] or even worse getting emitted outside the mechanical enclosure of the system. This compromises the radiated electromagnetic compatibility (EMC) significantly and therefore compromises the power quality of the system.
When connecting lateral power devices in a half-bridge configuration as provided in Fig. 2, the high-side device needs to be isolated from the die-substrate, the bulk, which is accomplished by modern silicon-on-insulator processes (SOI). Such an arrangement is visualized in figure 4.

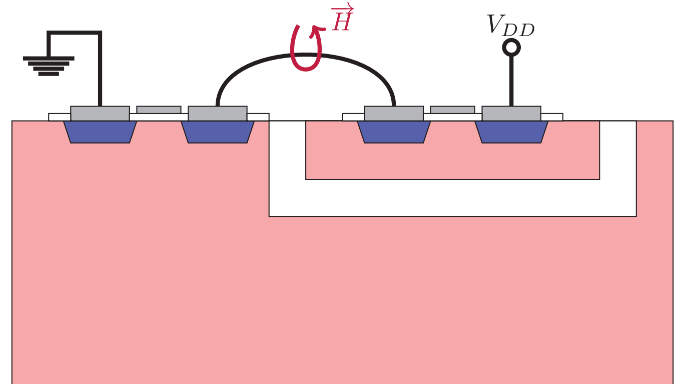

Fig. 4. Parasitics inductance and resulting magnetic field through connection of two lateral MOSFETs in a half bridge configuration

Compared to the routing of the switch-node in vertical devices, the alternating current in the lateral configuration only needs to be routed inside the metallization layers on top of the active silicon and does neither leave the package nor the die. Therefore the forward and the return path of the loop, penetrated by the alternating current is rather short, resulting in a significantly reduced $\vec{H}$-field.
As initially mentioned, the increased on-resistance of the vertical devices compared to the vertical counterparts, is their largest drawback. Therefore this paper focuses on the usability of lateral devices in power converters with respect to achievable efficiency. Section II introduces the custom made lateral SOI devices used in section III in a synchronous buck

converter design. Section IV shows the achieved experimental results and section V concludes the paper.

II. Custom made lateral power devices in silicon-on-insulator process

The design procedure and layout extracted results for the four designed lateral power MOPSFETs in a 180 nm SOI high voltage process is given in [9] and [10]. The resulting on-resistances of the two bigger devices are in the 2.5 Ω-range and the two smaller devices achieve around 3 Ω. Figure 5 provides the top-view of the designed devices, revealing their aspect ratio and their relative sizes. Furthermore, the bonding diagram is included in Fig. 5.

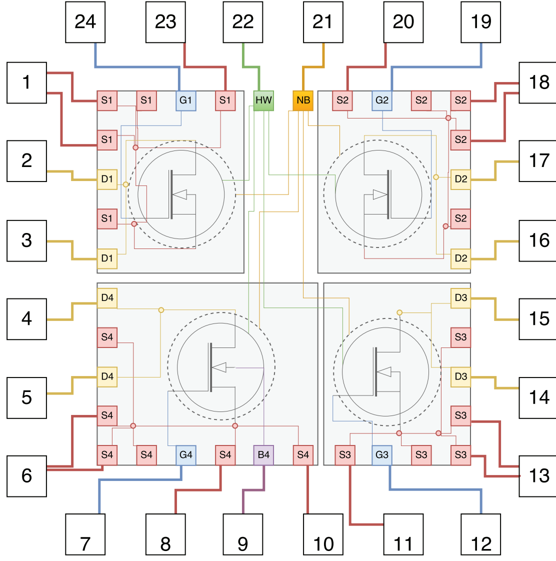

Fig. 5. Bonding diagram and top-view of the layout of the test MOSFETs

Figure 6 shows the packaged devices with open lid after soldering on a test printed circuit board (PCB). Here the aspect and size ratio of the two uper MOSFETs compared to both lower MOSFETs is even more visual, corresponding to the approximately 0.5 Ω difference in on-resistance between the respective drain and source connections, when the gate-source voltage is above the devices threshold voltage.

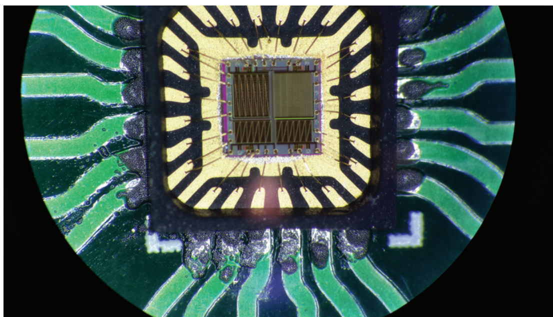

Fig. 6. Die photograph, when mounted on a printed circuit board (PCB).

III. Design of synchronous buck converter

The synchronous buck converter is designed to fullfil the specifications given in table I.

TABLE I
SPECIFICATIONS FOR SYNCHRONOUS BUCK-CONVERTER BASED ON THE SOI MOSFETs

Parameters	Value
Input Voltage V_{in}	48 V
Output Voltage V_{out}	12 V
Maximum output power $P_{out_{max}}$	≥ 1 W
Switching frequency f_{sw}	100 kHz
Output voltage ripple ΔV_{out}	≤ 500 mV
Operation mode	continuous at $P_{out_{max}}$

These specifications result in an output current I_{out} of

$$I_{out_{max}} = \frac{P_{out_{max}}}{V_{out}} = 83 \text{ mA}, \tag{2}$$

which results in an equivalent load resistance R_{load} of

$$R_{load_{min}} = \frac{V_{out}}{I_{out_{max}}} = 144 \ \Omega. \tag{3}$$

To keep the converter in continuous conduction mode [11] at the maximum power level $P_{out_{max}}$, the output inductor L_{out} must fullfil

$$L_{out} \geq \frac{(1-d)R_{load_{min}}}{2 \cdot f_{sw}} = 540 \ \mu\text{H}, \tag{4}$$

where d is the duty cycle of the buck converter in continuous conduction mode, derived as $d = \frac{V_{out}}{V_{in}} = 0.25$. The 820 µH inductor MSS1278-824KL with ±10 % tolerance and a maximum series resistance of 1.296 Ω from Coilcraft satisfies the design criteria. The contribution of the inductors DC resistance to the losses in the converter is therefore limited to 9 mW and an inductor ripple current $\Delta I_{L_{out}}$ of

$$\Delta I_{L_{out}} = \frac{(1-d)V_{out}}{f_{sw} \cdot L_{out}} = 110 \text{ mA}. \tag{5}$$

The contribution of the switching losses of the inductor are estimated in the approximate same range to 10 mW.
To keep the output ripple within the requirement an output capacitor C_{out} of

$$C_{out} \geq \frac{\Delta I_{L_{out}}}{4 \cdot f_{sw} \cdot \Delta V_{out}} = 550 \text{ nF} \tag{6}$$

is needed, where the design choice for C_{out} is a 590 nF ceramic X7R capacitor with 50 V rating. The losses in the equivalent series resistance of the output capacitor are negligible.
The half-bridge needs a gate driver. Here the design choice is an L5113 with a maximum power dissipation of 15 mW.
The completed design results in full schematic in Fig. 7 including all decoupling capacitors and the inputs to the gate driver.

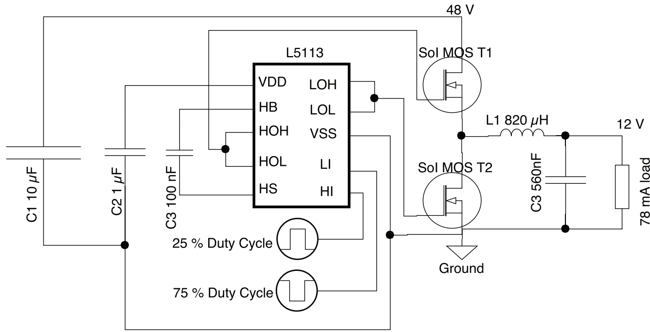

Fig. 7. Total schematic of the implemented synchronous buck converter.

Figure 8 shows a picture of the implemented prototype.

Fig. 8. Photograph of the implemented synchronous buck prototype with the test chip under yellow isolation take, the gate drive signals fed through the white BNC connectors at the bottom and the output inductor on the right side.

IV. Experimental Results

The block diagram of the experimental verification setup is provided in Fig. 9.

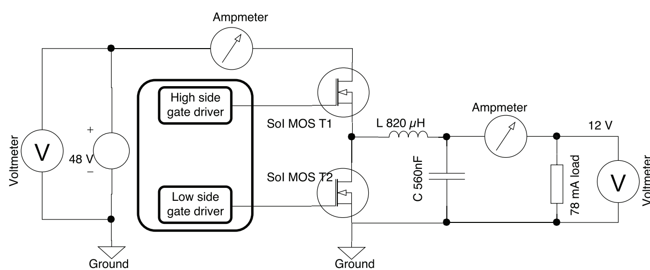

Fig. 9. Block diagram of setup to verify the usability of lateral SOI-based MOSFETs in the designed synchronous buck converter.

Figure 10 shows the laboratory setup, where the function generator Rigol DG4062 provides the gate signals and the active load ELA250 from Zentro Elektrik functions as the load resistor.

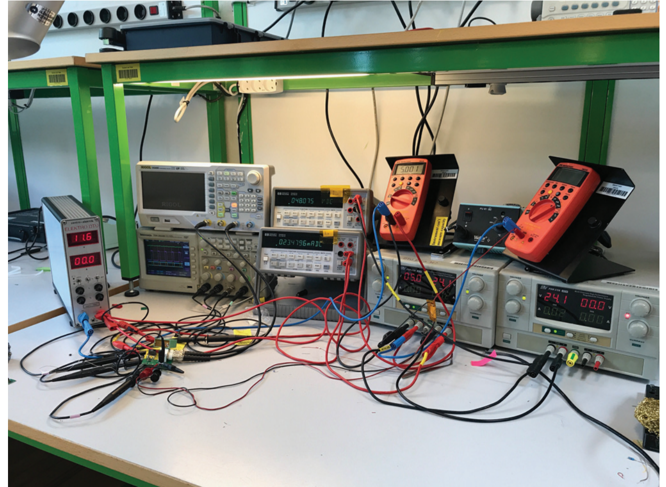

Fig. 10. Photograph of laboratory setup including - from left to right - the active load, the prototype, the function generator, the multimeters and the supplies for the input voltage as well as the auxiliary supply for the gate driver.

The correct operation of the buck converter is confirmed by measuring the switch node, e.g. the connection of the low-side MOSFETs drain to the high-side MOSFETs source, while monitoring the output voltage. Fig. 11 shows a screenshot of the oscilloscope measurement. The output voltage V_{out} is 12.0 V, the average voltage of the switching node is 12.5 V, while the converter is operating at 100.0 kHz. The overswing on the switch-node are an artifact of the applied measurement technique, resulting from the coupling of magnetic fields into the loop of the ground clip of the oscilloscopes probe.

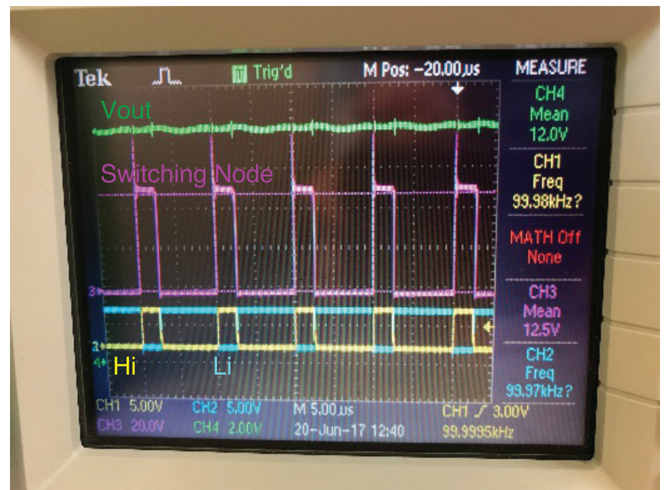

Fig. 11. Verification of the operation of the synchronous buck converter based on custom made lateral SOI power MOSFETs. From top to bottom: output voltage (green, 2 V/div), switch node (purple, 20 V/div), low-side input to the gate driver (cyan, 5 V/div) and its high-side input (yellow, 5 V/div) with a time base of 5 $\mu\mathrm{s}/div$

The most important parameter to verify the usability of lateral power MOSFETs in switch-mode power stages to reduce the

external fields and therefore improve the overall power quality of the converter is its achievable efficiency. The losses in the passive components, i.e. the output inductor and the output capacitor, as well as the losses in the gate drive are minimized by design. This leaves the switching and conduction losses in the power devices as the determining factor of efficiency, as the parasitic capacitances of the power devices are responsible for the switching losses and the on-resistance dominates the conduction losses. Hence the definition of the FOM. Figure 12 represents the final quantitive representation of the losses in the converter.

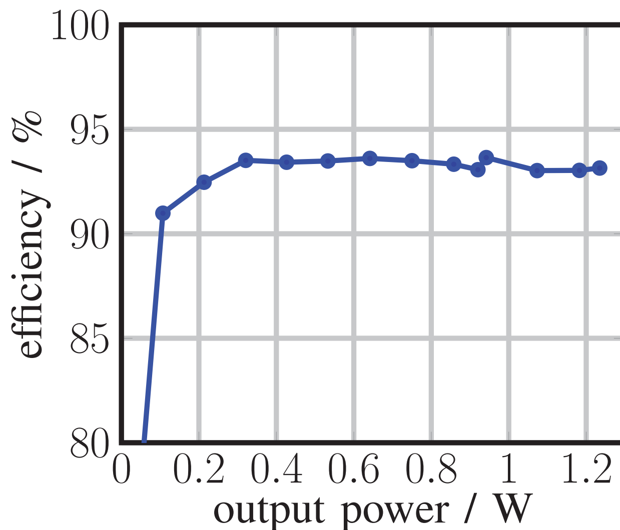

Fig. 12. Measured efficency of the implemented buck converter

Over a wide power range (from 10 % of $P_{out_{max}}$ to $P_{out_{max}}$), the converter operates above 90 % and at more than 300 mW the efficiency is around 93 %. This leaves about 70 mW to losses, of which 34 mW have been accounted for in the gate driver (15 mW) and the output inductor (19 mW) by design above. The remaining 36 mW of losses are expected in the power semiconductors.

The thermal image of the converter confirms the power semiconductors as the highest components with the highest temperature. Given their physical volume and the fact that they dissipate about half of the total losses, this is expectable. As the highest temperature of the converter in thermal equilibrium is 34.6 °C, only 8.9 °C above the ambient temperature of 25.7 °C, the overall performance of the converter is acceptable for many applications. Given a maximum operating temperature of silicon devices at 150 °C and adding a small safety margin, this design can be qualified up to an ambient temperature of 140 °C, which is enough for most consumer, industrial, automotive and space applications.

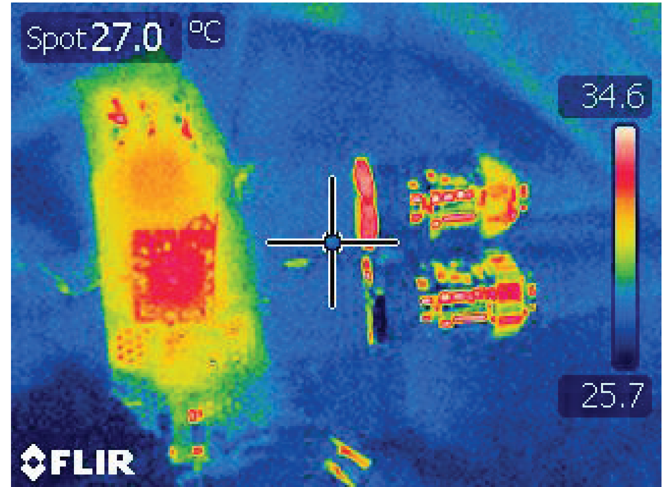

Fig. 13. Thermal image of the synchronous buck converter under operation: the highest temperature rectangle to the left of the cursor represents the tested custom made lateral SOI power MOSFETs, whereas the hot spots to the right of the cursor are the BNC connectors - which might represent a wrong temperature due to the reflective nature of their surface with respect to the infrared cameras measurement technique.

V. Conclusion

Lateral power semiconductors are proposed as a method to reduce emitted magnetic fields compared to the widely used vertical power devices. To check the feasibility of the lateral devices, their useability in power converters needs to be examined. This paper used custom made silicon-on-insulator lateral power MOSFETs to determine the applicability of the selected process in power electronics. A 48 V to 12 V, 1 W synchronous buck converter was designed and experimentally verified. The experimental results show a high efficiency (around 93 %) over a wide load range and a temperature rise of less than 10 °C, proofing that lateral silicon-on-insulator power MOSFETs are a serious alternative to vertical devices.

Acknowledgements

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A.7. Publication (conference, accepted)

This is the accepted version of the publication.

Lin Fan, Arnold Knott, Ivan Harald Holger Jørgensen, “An Asynchronous-Switched-Capacitor DC-DC Converter Based on GaN and SiC Devices”, in IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia, 2018.

An Asynchronous-Switched-Capacitor DC-DC Converter Based on GaN and SiC Devices

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Summary

For the state-of-the-art switched-capacitor DC-DC converters at high-voltage low-power levels, switching loss becomes a major concern and challenge. Existing switching schemes operate power semiconductors at a signle common frequency, which does not optimally address the switching losses, especially for a high-conversion-ratio design. This paper presents a concept of Asynchronous-Switched-Capacitor (ASC), which is applied to the GaN switches that are combined with the SiC diodes to improve the efficiency and the power density. The ASC operation is named when the switches can be operated with uncorrelated frequencies, with unnecessary phase/clock synchronization of the control signals. A 380 V, 6 W, 4:1 conversion ratio converter experimentally validates the concept. The efficiency is improved by 4% and the peak-to-peak output voltage ripple is reduced by 39%, with the proposed ASC switching, compared to the conventional switching. A peak efficiency of 95.4% is achieved.

Motivation

Switched-capacitor DC-DC converters are commonly implemented on integrated circuits (IC)[1]. Theses converters are either limited by the input voltage (≤ 12 V) and/or the output power (≤ 2 W). Recent research demonstrates switched-capacitor converters using discrete components with an input voltage up to 200 V and output powers of 30-53 W[2, 3]. At higher characteristic impedance (higher-voltage, lower-current) levels, new designs and concepts are anticipated to emerge. This paper presents a 380 V input voltage, 6 W output power, 4:1 conversion ratio switched-capacitor DC-DC converter (see Fig. 1), and proposes the concept of Asynchronous-Switched-Capacitor (ASC). The switching losses of the switches related to charging and discharging the output capacitances are calculated as follows. It shows that the switching losses are not evenly distributed with the conventional switching at a single common frequency. Furthermore, the optimum switching frequencies depend on the current level hence the characteristic impedance level, for a given energy transfer capacitance. This motivates the proposed ASC concept, which mitigates the requirements of the control signals with high tolerance of phase-shifts.

$$P_{sw_Coss_total} \cong f_{Q1_Q2} \cdot V_{IN} \cdot \int_0^{V_{IN}/2} C_{oss}(v_{DS}) \cdot dv_{DS} + f_{Q3_Q4} \cdot \left(V_{IN}/2\right) \cdot \int_0^{V_{IN}/4} C_{oss}(v_{DS}) \cdot dv_{DS}$$

Results

A high-voltage low-power switched-capacitor DC-DC converter experimentally validates the proposed ASC switching. The efficiency (see Fig. 2 and Fig. 3), the thermal performance (see Fig. 4) and the output voltage ripple (see Fig. 5) are improved. The measured peak slew rates of the GaN (EPC2012C) and SiC (C3D1P7060Q) devices in the operating converter (see Fig. 6) are about 90 V/ns and 80 V/ns, respectively, which also enhance the performance of the converter, with switching frequencies as low as 1 kHz. All experimental work is finished and will be presented in the final paper.

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Figures

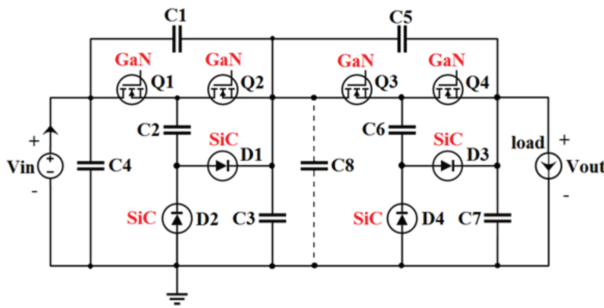

Fig. 1: Proposed asynchronous-switched-capacitor DC-DC converter (4:1 conversion ratio). Wide-bandgap devices are highlighted.

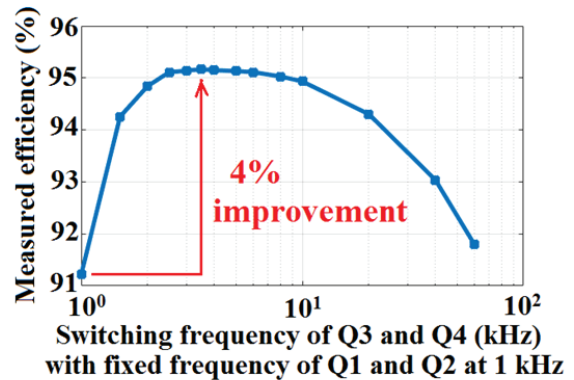

Fig. 2: Measured efficiency versus switching frequency of Q3 and Q4, while Q1 and Q2 are operated with a constant frequency of 1 kHz.

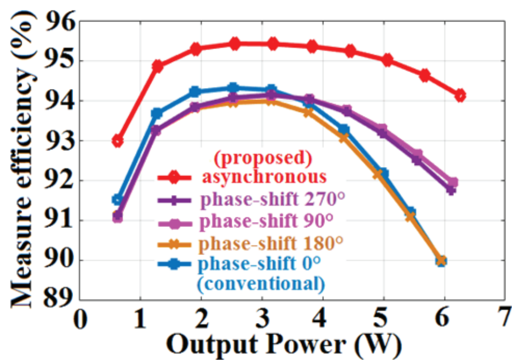

Fig. 3: Measured efficiency versus output power. The phase-shift is defined as Q3/Q4 referred to Q1/Q2 when Q1-Q4 have the same frequency. The asynchronous is measured with Q3/Q4 at 4 kHz and Q1/Q2 at 1 kHz (unnecessarily multiple times of each other).

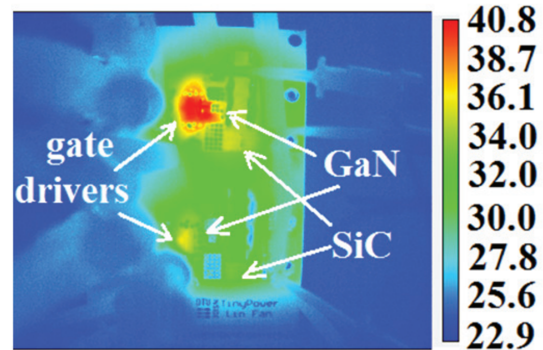

Fig. 4: Thernal image (°) of the prototype asynchronous-switched-capacitor converter. Measured after one hour full-power operation, without heatsink or airflow.

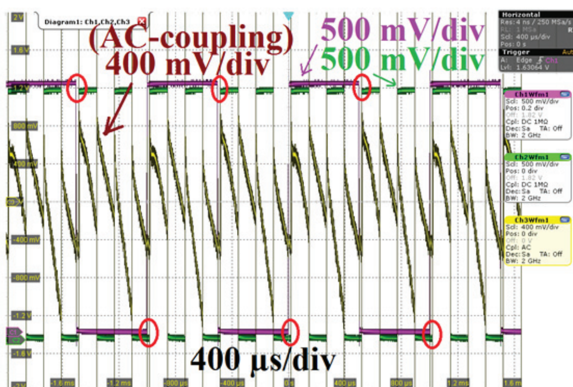

Fig. 5: Waveforms of the output voltage (AC-coupling) versus the asynchronous control signals.
The phases/clocks are not necessarily synchronized.
The peak-to-peak output votalge ripple is reduced by 39% compared to conventional switching.

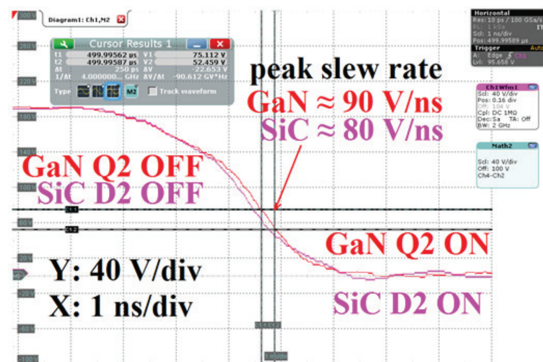

Fig. 6: Measured turn-on transients. Peak slew rates of GaN Q2 and SiC D2 are about 90 V/ns and 80 V/ns, respectively. RTO-1024 2 GHz oscilloscope, RT-ZP10 500 MHz probes, and 1 kHz switching frequency.

A.8. Publication (journal and conference, accepted)

This is the accepted version of the publication.

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And

Lin Fan, Arnold Knott, Ivan Harald Holger Jørgensen, "A High-Voltage Low-Power Switched-Capacitor DC-DC Converter Based on GaN and SiC Devices for LED Drivers" in 22th International Conference ELECTRONICS 2018.

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A High-Voltage Low-Power Switched-Capacitor DC-DC Converter Based on GaN and SiC Devices for LED Drivers

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***Abstract*—Previous research on switched-capacitor DC-DC converters has focused on low-voltage and/or high-power ranges, where the efficiencies are dominated by conduction losses. Switched-capacitor DC-DC converters at high-voltage (> 100 V) and low-power (< 10 W) levels with high efficiency and high power density are anticipated to emerge. This paper presents a switched-capacitor converter with an input voltage up to 380 V (compatible with rectified European mains) and a maximum output power of 10 W. The converter is intended for LED drivers. GaN switches and SiC diodes are analytically compared and actively combined to properly address the challenges at high-voltage low-current levels, where switching losses become significant. Further trade-off between conduction losses and switching losses is experimentally optimized with switching frequencies. Three variant designs of the proposed converter are implemented, and the trade-off between efficiencies and power densities is validated with measurement results. A peak efficiency of 98.6% and a power density of 7.5 W/cm^3 are achieved without heatsink or airflow. The characteristic impedance level of the converter is an order of magnitude higher than previously published ones.**

***Index Terms*—DC-DC power converters, Gallium nitride, Silicon carbide, Switched capacitor circuits, Wide band gap semiconductors.**

I. INTRODUCTION

The demand for high efficiency and high power density power converters has been progressing along with advances in industrial and consumer electronics, power conversion architectures, converter circuit topologies, and wide band gap semiconductor technologies. The size, weight, cost reduction demands of power supplies are the major drivers in the continuing miniaturization trend [1]. However, the decrease in volume could be attained only by a simultaneous increase of the efficiency to maintain thermal limits at maximum losses [2]. Therefore, increasing the efficiency is the primary development goal and the premise of the realization of smaller and lighter power supplies.

The applications such as light-emitting diode (LED) drivers for intelligent lighting systems and miniature chargers for internet of things (IoT) are examples driving a continuous demand of the reduction in volume of power converters. The converters driving LEDs are typically inductor-based converters, with operation ranges in voltage from a few volts [3] to tens of volts [4]. The power densities of these converters can potentially be increased by integrating power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) on integrated circuits (IC) [5]. For the LED drivers interfacing with rectified AC mains in the range of hundreds of volts, voltage conversion is needed to step-down the high-voltage level to a suitable level, with which the LED drivers can properly work. A possible way of achieving the voltage conversion is by stacking power converters or stacking certain parts of power converters, e.g. the inverter stages [6]. This paper is to present another approach, i.e. the voltage conversion is achieved with a high-voltage low-power switched-capacitor converter, which has not been previously demonstrated in the voltage and power levels.

The switched-capacitor approach has been shown as an alternative way with respect to the inductor-based converters [7]. State-of-the-art switched-capacitor DC-DC converters that are implemented on IC chips are either limited by input voltages (≤ 12 V) or limited by output powers (≤ 2 W) [7]–[10]. To be simultaneously above both practical limits, low-voltage (≥ 12 V) high-power (≥ 100 W) switched-capacitor converters are commonly implemented with discrete components [11], [12]. However, at high-voltage (≥ 100 V) low-power (≤ 10 W) levels, the design challenges are not the same as low-voltage designs, and high performance implementation remains a challenge. The conventional modelling of switched-capacitor converters [13] focuses only on conduction losses and is not adequate to analyse switched-capacitor converters at high-voltage levels [14], where the switching loss related to charging and discharging the output capacitances of the switches becomes significant, compared to the charge transfer loss related to charging and discharging the energy transfer capacitors. Recent research shows switched-capacitor DC-DC converters with input voltages up to 200 V and output powers in the range of 30–53 W [14], [15]. Switched-capacitor converters at much higher characteristic impedance levels (higher voltage and lower current) with high efficiency and high power density are to be demonstrated for potential applications such as LED drivers

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that are globally compatible with AC mains.

This paper presents a high input voltage (up to 380 V, e.g. compatible with European 220-240 Vrms AC operation with ±10 % tolerance) and low output power (up to 10 W) switched-capacitor DC-DC converter. To address the aforementioned challenges, wide band gap semiconductor devices, i.e. Gallium Nitride (GaN) switches and Silicon Carbide (SiC) diodes are combined and utilized to achieve high power density while obtaining high efficiency by trade-off between conduction loss and switching loss at high characteristic impedance (high-voltage and low-current) levels. Section II presents the proposed switched-capacitor DC-DC converter and its operation principle. Section III presents the design procedure and considerations. Section IV presents the experimental results of the converter with three variant designs, i.e. a high power density design, a high efficiency design, and a trade-off design between the other two. The optimization of the switching frequencies and the trade-off between the efficiency and the power density are experimentally validated. Section V concludes the paper.

II. SWITCHED-CAPACITOR DC-DC CONVERTER

The proposed high-voltage low-power switched-capacitor DC-DC converter is shown in Fig. 1. The converter has a voltage conversion ratio of 2:1 from the input to the output. The power stage of the converter consists of only eight components, i.e. two switches (Q1, Q2), two diodes (D1, D2), and four capacitors (C1–C4).

The operation of the switched-capacitor converter is distinguished in four states (S1–S4), as shown in Fig. 2. The contribution of this analysis is that the conventional two-states analysis is not adequate to analyse the behaviour of the output voltage ripple, whereas the four-states analysis reveals that the output voltage ripple is at the double-frequency of the switching frequency with the detailed charge/discharge behaviour of the energy transfer capacitor C2.

The switching waveforms are shown in Fig. 3. The two switch/diode pairs Q1/D1 and Q2/D2 are in complementary operation with a fixed 50% duty cycle. In general, the load current is primarily supplied by either charging or discharging the energy transfer capacitor C2. The sum of the voltages of the capacitors C1 and C3 equals to the input voltage, as a result, the capacitors C1 and C3 are always charged and discharged in the opposite directions.

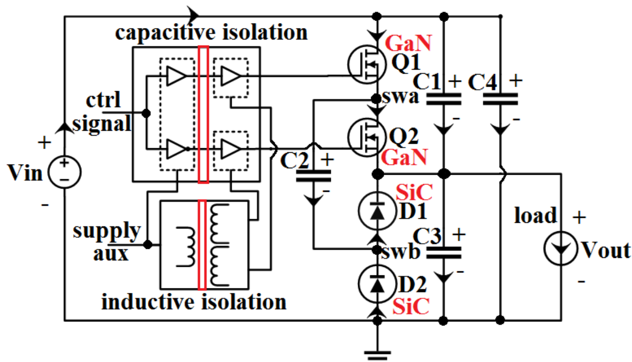


Fig. 1. Proposed switched-capacitor DC-DC converter, for high-voltage low-power applications with high efficiency and high power density.

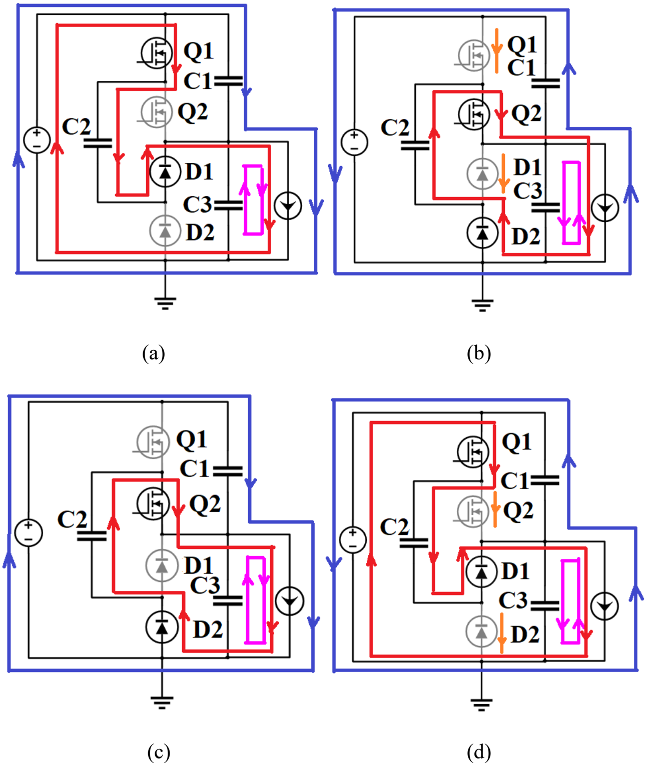


Fig. 2. Four operation states of the switched-capacitor DC-DC converter. (a) State S1. (b) State S2. (c) State S3. (d) State S4.

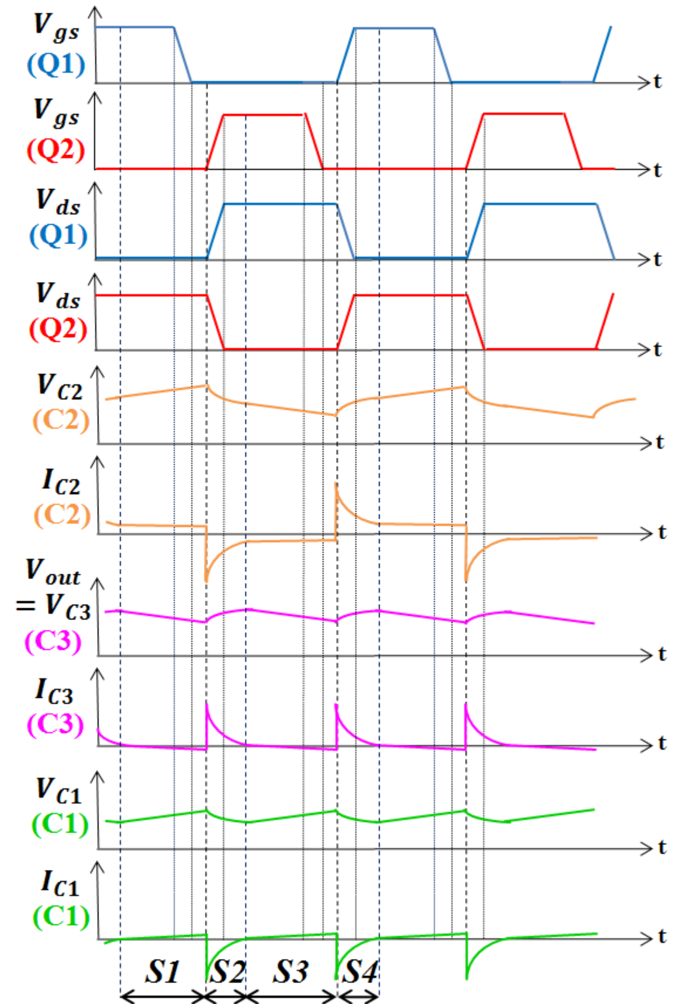


Fig. 3. Switching waveforms of the switched-capacitor converter (four operation states are indicated with S1-S4).

The operation principle of the four states (S1-S4) is elaborated as follows:

State S1: The switch/diode pair Q1/D1 is on. The input current mainly charges C2 and also charges C1, and C3 is discharged, thus the output voltage decreases.

State S2: The switch/diode pair Q2/D2 starts turning on. A small amount of current is needed to charge the parasitic output capacitances of Q1/D1. C2 is discharged to provide the load current and also charges C3, and C1 is discharged, thus the output voltage increases.

Stage S3: The switch/diode pair Q2/D2 is on. The load current mainly discharges C2 and also discharges C3, and C1 is charged, thus the output voltage reduces.

Stage S4: The switch/diode pair Q1/D1 starts turning on. A small amount of current is needed to charge the parasitic output capacitances of Q2/D2. C2 is charged while providing the load current and also charges C3, and C1 is discharged, thus the output voltage rises. Then next cycle begins.

The output voltage of the converter increases and then decreases for each 50 % switching cycle when either Q1/D1 or Q2/D2 starts turning on. Thus the output voltage ripple shows a frequency f_{Vout_ripple}, which is twice the switching frequency f_{sw} of the control signals for driving Q1 and Q2.

$$f_{Vout_ripple} = 2 \times f_{sw} \tag{1}$$

For the energy transfer capacitor C2, in steady state, the average current of C2 (I_{C2}) is zero. However, the average of the absolute current of C2 ($|I_{C2}|_{avg}$) equals the output DC current I_{out}. These two currents I_{C2} and $|I_{C2}|_{avg}$ are distinguished in (2) and (3), where T_s is the period of the control signals, i.e. $1/f_{sw}$.

$$I_{C2} = \frac{1}{T_s}\int_0^{T_s} i_{C2} \cdot dt = 0 \tag{2}$$

$$|I_{C2}|_{avg} = \frac{1}{T_s}\int_0^{T_s} |i_{C2}| \cdot dt = I_{out} \tag{3}$$

This is because the current of C2 (i_{C2}) is in opposite directions for each 50 % duty cycle, i.e. in one 50 % duty cycle, C2 is discharged to provide the load current, and in the other 50 % duty cycle, C2 is charged while providing the load current, as discussed above. To reduce the conduction loss, it is the root mean square (RMS) current of C2 (I_{C2_RMS}) to be minimized, while the average of the absolute current of C2 ($|I_{C2}|_{avg}$) is kept constant as the DC load current.

$$I_{C2_RMS} = \sqrt{\frac{1}{T_s}\int_0^{T_s} (i_{C2})^2 \cdot dt} \tag{4}$$

The peak-to-peak voltage ripple of C2 (ΔV_{C2}) is calculated, and it is reversely proportional to the capacitance of C2 and the switching frequency f_{sw} of the control signals [16]. The capacitance and the switching frequency are major design parameters of the switched-capacitor converter, and discussed in more details in the next section.

$$\Delta V_{C2} = \frac{1}{C2}\int_0^{T_s/2} |i_{C2}| \cdot dt = \frac{I_{out}}{2 \times C2 \times f_{sw}} \tag{5}$$

From a generalized DC model of switched-capacitor converters [13], [17], [18], the output voltage of the converter V_{out} can be expressed as follows in (6). Therefore, the output voltage directly depends on the output load current.

$$V_{out} = V_{in}/2 - I_{out} \times R_{out} \tag{6}$$

R_{out} is the equivalent (resistive) output impedance of the converter (only taking conduction losses into account), and it also depends on the two major design parameters, i.e. the capacitance and the switching frequency.

III. Design Considerations

A. Converter Specifications

The specifications of the DC-DC converter are shown in Table I. From the specifications, the characteristic impedance level of the converter is considerably high (high-voltage and low-current), which is proportional to the square of the voltage for a given power. Note that both high efficiency and high power density are required for the converter. As previously discussed, a high efficiency is the primary development goal and the premise of a high power density. However, the requirement of the power density needs to be kept in mind through the development process. This is because higher efficiencies are fundamentally always possible by increasing the volume of the converter [2]. A good practice is to design with components and architectures that can address high efficiency and high power density at the same time. The characteristic impedance level of the converter is an order of magnitude higher than those of previously published switched-capacitor DC-DC converters with high efficiency and high power density, and this is summarized in Table II.

B. GaN switches and SiC diodes

The emerging wide band gap semiconductors have superior properties, which have the potentials to enable both high efficiency and high power density. The components considered here are GaN switches and SiC diodes, for the specified voltage range of the converter.

First, the purpose of the diodes is to replace some of the transistor-switches in the switched-capacitor converter. This is theoretically analysed, i.e. by analysing the direction of the current flow in an all-transistor-switches switched-capacitor converter, a general switching-device that conducts negative current and blocks positive voltage may be suitable for diode implementation [13], instead of using a transistor-switch.

TABLE I. SPECIFICATIONS OF THE CONVERTER.

Parameters	Specifications
Input voltage	300–374 Vdc
Voltage conversion ratio	2:1
Maximum output power	10 W
Output voltage ripple	< 5 %
Efficiency	> 95 % above half rated power
Power density	> 4 W/cm^3

TABLE II. COMPARISON OF HIGH-VOLTAGE SWITCHED-CAPACITOR DC-DC CONVERTERS.

	Reference [14]	**Reference [15]**	**This work**
Input voltage	up to 200 Vdc	up to 200 Vdc	up to 380 Vdc
Output power	up to 30 W	up to 53 W	up to 10 W
Impedance level	≈ 1333 Ω	≈ 755 Ω	≈ 14440 Ω
Normalized impedance	**1.8 x**	**1 x**	**19.1 x**

Second, the need of using both GaN switches and SiC diodes becomes clear when the comparison of the two devices is demonstrated with conduction loss, switching loss, gating loss, land pattern and total footprint area. The SiC diodes are non-controlled devices, and a fictitious all-diode-switches switched-capacitor converter is not feasible. Therefore, to implement the converter, it only needs to compare the two cases of either using all-transistor-switches or using the combination of switches and diodes.

The comparison of the selected GaN switch and SiC diode is summarized in Table III. The comparison mainly contains four parts: conduction loss, switching loss, gating loss, and footprint area. They are described as follows.

Conduction loss: for low-voltage high-power applications, where conduction loss is the dominated loss, diodes may be considered to be replaced by synchronous rectification (SR) actively-controlled transistors to reduce the conduction loss and thus improve the total efficiency. However, the converter under discussion is for high-voltage low-power applications, and switching loss and gating loss are the major concerns. Table III shows that the SiC diode indeed incurs higher conduction loss compared to the GaN switch, but under high-voltage (≥ 100 V) and low-current (≤ 100 mA) operation conditions, the conduction loss introduced by the forward voltage drop of the diode can be constrained at a minimal level. The loss of the converter under discussion is not conduction loss dominated.

Switching loss: from the datasheets, the GaN switch has an output charge of 10 nC and an output capacitance of 64 pF at 100 V, whereas the SiC diode only exhibits a total capacitive charge of 1.8 nC and a total capacitance of 10 pF at 100 V. Further calculated and estimated comparison is shown in Table III. SiC diodes largely reduce the output-capacitance related switching loss, and facilitate fast switching transients, compared to the case if the converter is implemented solely with GaN switches. Note that SiC diodes as majority carrier devices need close-to-zero reverse recovery charge.

Gating loss: the SiC diode implementation eliminates the driver circuits (and the associated supply circuits) that are needed for driving GaN switches, thus the gating loss and the power consumption of the driver circuits are saved, and a high power density can also be achieved.

Footprint area: at the component level, as shown in Table III, the SiC diode occupies more footprint area than the GaN switch. However, the development goal is to achieve a high power density of the total converter, rather than a single component. In fact, the GaN switch together with its driver circuits takes much larger footprint area than the SiC diode that does not need any driving circuits. From a total-converter point of view, the SiC diode can greatly save the footprint area and thus improve the overall power density.

As a result of the comparison of the GaN switch and the SiC diode, the combination of using both GaN switches and SiC diodes is preferred and proposed to achieve high efficiency and high power density of the switched-capacitor converter for high-voltage low-power applications.

The peak current handling capability of the GaN switches and the SiC diodes may be of concern and is briefly discussed as follows.

TABLE III. COMPARISON OF GAN SWITCH AND SIC DIODE.

Parameters	GaN switch	SiC diode
Manufacturer	Efficient Power Conversion (EPC)	Wolfspeed (Cree)
Part Number	EPC2012C	C3D1P7060Q
On-Resistance (Equivalent)	70 mΩ (at 5 V V_{GS})	260–880 mΩ (estimated)
Conduction Loss	$I_{RMS}^2 \times R_{on}$	$I_{RMS}^2 \times R_{on}$
Conduction Loss (Calculated)	0.11 mW* (at 40 mA I_{RMS})	0.42–1.41 mW* (at 40 mA I_{RMS})
Output Capacitance	50 pF (at 200 V V_{DS})	7 pF (at 200 V V_R)
Output Charge	15.7 nC (at 200 V V_{DS})	2.7 nC (at 200 V V_R)
Switching Loss (Capacitance Loss)	$Q_{OSS} \times \left(V_{in}/2\right) \times f_{sw}$	Zero (assume zero reverse leakage current)
Switching Loss (Calculated)	7.46 mW** (at 2.5 kHz f_{sw})	Zero (assume zero reverse leakage current)
Gate Charge	1.1 nC (at 200 V V_{DS})	Zero (no gate terminal)
Gating Loss	$Q_G \times V_{DRIVE} \times f_{sw}$	Zero (no gate terminal)
Gating Loss (Calculated)	0.01 mW** (at 2.5 kHz f_{sw})	Zero (no gate terminal)
Driver and Isolated Supply Loss	78.79 mW* (average value of measured prototype)	Zero (no driver or isolated supply needed)
Reverse Recovery Charge	Zero (no body diode)	Zero (majority carrier diode)
Total Loss (without Driver)	7.58 mW*	0.42–1.41 mW*
Total Loss (with Driver and Isolated Supply)	86.37 mW* (each GaN switch)	0.42–1.41 mW* (no driver or isolated supply needed)
Package Dimensions	1.711 mm × 0.919 mm = 1.57 mm^2	3.3 mm × 3.3 mm = 10.89 mm^2
Land Pattern (without Driver)	1.711 mm × 0.919 mm = 1.57 mm^2	3.6 mm × 3.6 mm = 12.96 mm^2
Land Pattern (with Driver and Isolated Supply)	1.57 + 5.00 × 5.00/2 + 15.24 × 12.00/2 mm^2 = 105.51 mm^2 ***	12.96 mm^2 (no driver or isolated supply needed)

*Depends on frequency, capacitance, load current, input voltage, output power, and parasitic resistances and inductances of packages and layout.
**Depends on frequency (to be experimentally optimized in next section).
***Half of driver and isolated supply land pattern is counted for each GaN switch for fair comparison, but additional footprint is further needed for local decoupling capacitors and dead time circuits for driving GaN switches.

From the analysis and simulations, high peak currents conduct through the switches (and the corresponding diodes) to and from the energy transfer capacitor right after each switching event. The high peak currents get worse when low equivalent on-resistance devices such as the GaN switches and the SiC diodes are employed to reduce conduction loss. For this reason, the selected GaN and SiC devices have high ratios of peak-current to continuous-current ratings. The high forward surge current handling capability of the SiC diodes is enhanced by the Merged PIN Schottky (MPS) structure [19], evolved from the Junction Barrier Schottky (JBS) design.

C. Switching Frequency and Dead Time

As shown in Table III, the conduction loss, the switching loss, the gating loss, and hence the total loss of the converter depend on the switching frequency. The calculations and estimations in Table III serve as the initial design guide of the

converter, and the switching frequency is to be experimentally optimized in the next section. The conduction loss is considered as frequency dependent here. This is because from the RMS-current point of view, the RMS currents through the switches and the diodes depend on the switching frequency. In the frequency range of interest (about a few kilohertz), the switched-capacitor converter is insensitive to the dead time between the complementary control signals for driving the GaN switches. Therefore, the dead time may firstly be optimized or tuned, and then the optimization of the switching frequency is performed afterwards.

D. Capacitors Design

The design of the capacitors of the switched-capacitor converter starts with the capacitors C1 and C3. The voltage ratings of C1 and C3 need to be higher than the maximum input voltage, rather than the steady-state operation voltages. During the initial start-up phase, C3 may be fully discharged and/or not properly charged, and then C1 has to withstand the input voltage. By doing further failure analysis, if either the switch Q1 or Q2 breaks down as a short circuit, C3 has to withstand the input voltage, instead of the output voltage. C1 and C3 are firstly chosen to have a 450 V rating with a nominal capacitance value of 1 μF. The sum of the capacitances of C1 and C3 needs to be designed high enough to keep the output voltage ripple at low levels, while considering that the effective capacitance of the 450 V ceramic capacitors operating at 200 V is about the half of the nominal capacitance at zero DC bias voltage.

The design of C2 is to be shown as a trade-off between the efficiency and the power density, and its capacitance value is chosen to be several times larger than those of C1 and C3 to achieve a high efficiency. To demonstrate the trade-off, C2 is designed with three capacitance values, i.e. 3 μF (high power density), 9 μF (high efficiency), and 6 μF (trade-off between the other two), all of which has a voltage rating of 250 V. In addition, C4 is a 0.22 μF 450 V capacitor to filter out higher-frequency noise of the input supply than the decoupling capability partly provided by C1 and C3.

After the voltage ratings and the capacitance values are determined, the quality factor and the energy density of the ceramic capacitors may be further improved by the trade-off with temperature specifications [20], e.g. X7R (+125 °C ±15 %) may be relaxed to X6S (+105 °C ±22 %) or X7T (+125 °C +22/-33 %). All capacitors C1–C4 are chosen to be X7T type.

E. Driver and Isolated Supply

The power state design is now completed. However, driving the GaN switches in the proposed high-voltage converter is another challenge. From simulation results, the highest peak dv/dt of the switching transients may research 100 V/ns level. High dv/dt immunity is required for the high-side gate drivers of the GaN switches, to prevent the control signals from losing signal integrity and/or unexpectedly changing logic states. For a GaN switch above 100 V, more than 50 V/ns immunity is typically needed [21]. The state-of-the-art junction-coupled drivers, opto-coupled drivers, and transformer-coupled drivers have Common Mode Transient Immunity (CMTI) specified up to 50 V/ns (minimum) [22]. Therefore, the capacitive-coupled gate driver (Si8274GB1) with a CMTI of 150 V/ns (minimum) is selected. The capacitive isolation is achieved with the semiconductor-based isolation barrier of the three-die architecture, and the control signals are transmitted in the form of RF on/off keying modulated signals [23]. Because the isolated output drivers are actually located on individual dies, independent supplies are needed for these driver outputs, and the inductive-isolated supply with dual independent outputs (R1DA) is used to fulfil this purpose. The comparison of different driver circuit topologies is analysed in [16]. The gate driver circuitry can be viewed as a floating half-bridge gate driver that is superposed on the converter output voltage.

IV. EXPERIMENTAL RESULTS

The prototype of the proposed converter is implemented with 2-layers PCB, which has 1 mm PCB-thickness and 2 oz copper-thickness. The PCB is designed complying with industry standard specifications such as track widths, spacing distances, and through-hole diameters. The components are located on both sides of the PCB, as shown in Fig. 4, to minimize the charge transfer loops and the power loops.

The measurement test bench is shown in Fig. 5. The digital multimeter 34401A and the power analyzer PPA5530 are compared by calculating the sum of the reading error and the range error. For an input at 300 V and 20 mA, the total error of 34401A is ±12 mV, ±6 μA, ±0.034 % (ΔP/P), and the total error of PPA5530 is ±136 mV, ±11.6 μA, ±0.103 % (ΔP/P). For an output at 150 V and 40 mA, the total error of 34401A is ±9 mV, ±8 μA, ±0.026 % (ΔP/P), and the total error of PPA5530 is ±106 mV, ±30.8 μA, ±0.148 % (ΔP/P). The maximum absolute error of the efficiency measurement ($\Delta\eta$) is then calculated [2].

$$\Delta\eta = \eta \times \left(\Delta P_{out} / P_{out} + \Delta P_{in} / P_{in} \right) \quad (7)$$

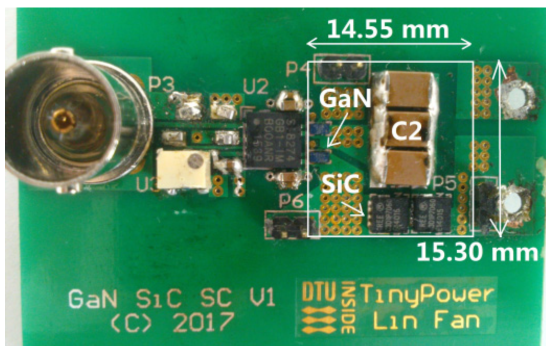
Assume an expected efficiency of 98 %, the maximum absolute errors of the efficiencies measured using 34401A and PPA5530 are 0.059 % and 0.246 %, respectively. Therefore, 34401A digital multimeters are used for the efficiency measurements. For the highest accuracy, the full 6½ digits resolution and the manual ranging of 34401A are used. For the low-power converter with high efficiencies, the measurement results are sensitive to the surrounding airflow. All efficiencies are measured at the room ambient temperature without any heatsink or airflow. The measurements are repeated for multiple times under the same conditions, and the measurement results are only counted when the data are reasonably repeatable.

Three variant designs with different nominal capacitance values of C2 (C2-nom) are experimentally optimized for switching frequencies. The measured efficiencies versus switching frequencies with an input voltage of 374 V and the maximum output power of 10W are shown in Fig. 6. The optimization of switching frequencies is essentially the trade-off between the conduction loss and the switching loss (mainly the output-capacitance related switching loss of the

GaN switches), as discussed in the previous section.

After the switching frequencies are optimized for each design, the efficiencies of the power stages (without driver losses) are measured versus output powers and input voltages, as shown in Fig. 7. The efficiencies are generally higher with higher capacitance values. However, higher capacitance values mean larger volumes, and this fundamentally results in a trade-off between the efficiency and the power density.

The voltage conversion ratios are measured versus output powers and input voltages, and the results are shown in Fig. 8. The measurements are under the same conditions as the efficiency measurements in Fig. 7. The voltage conversion ratios are close to 2:1, as expected. The voltage conversion ratios increase with the output power and it is because the output voltages decrease with the output load current for given capacitance values and fixed switching frequencies. The theoretical relation is (6) in the previous section.



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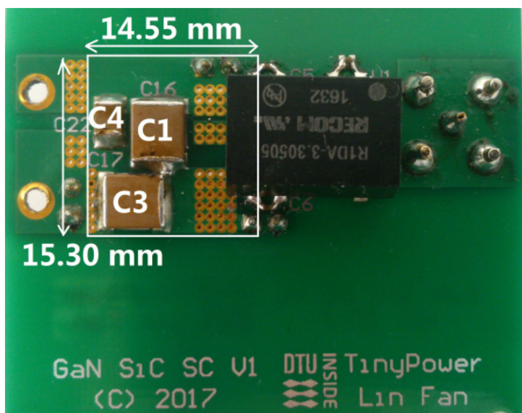


(b)

Fig. 4. Prototype converter. Power stage components are highlighted. (a) Top side. (b) Bottom side.

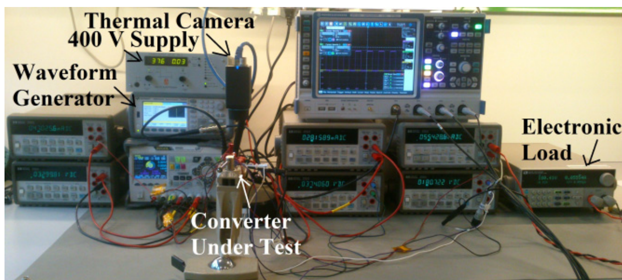


Fig. 5. Measurement test bench. Keysight 33622A waveform generator is used for generating control signals. Delta Elektronika SM400-AR-4 power supply is used for input voltages. ITECH IT8812B electronic load is used for load currents. FLIR A35 thermal imaging temperature sensor is used for taking thermal images of the prototype converter.

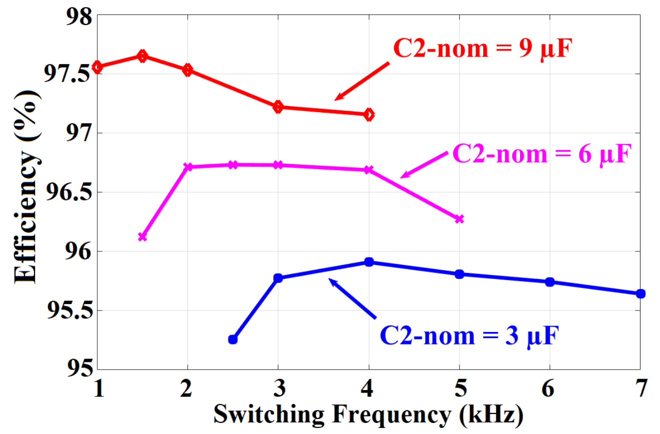


Fig. 6. Experimental optimization of switching frequency (trade-off between conduction loss and switching loss). Measured with 374 V input voltage and 10 W output power.

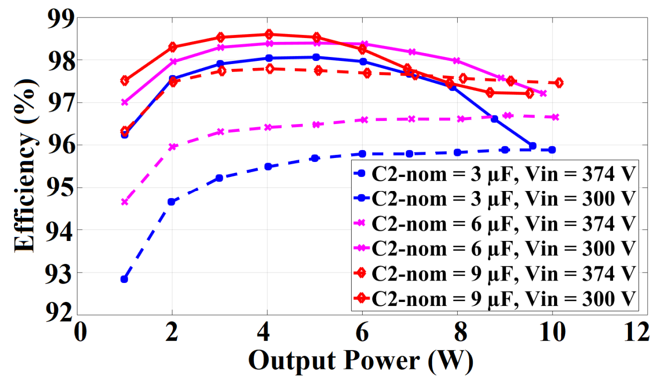


Fig. 7. Measured efficiency vs. output power (three variant designs with optimized switching frequencies: 3 μF/4 kHz, 6 μF/2.5 kHz, 9 μF/1.5 kHz).

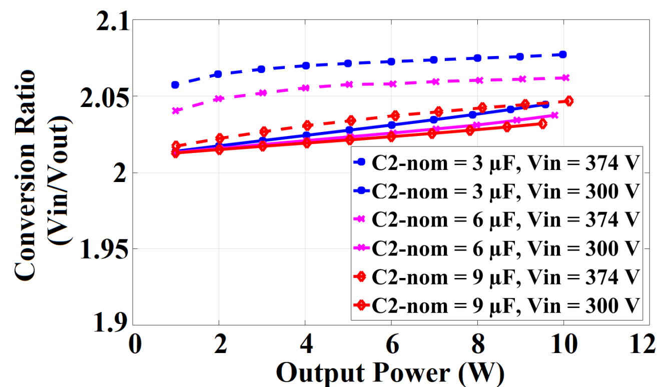


Fig. 8. Measured voltage conversion ratio vs. output power (three variant designs and the legends are the same as Fig. 7).

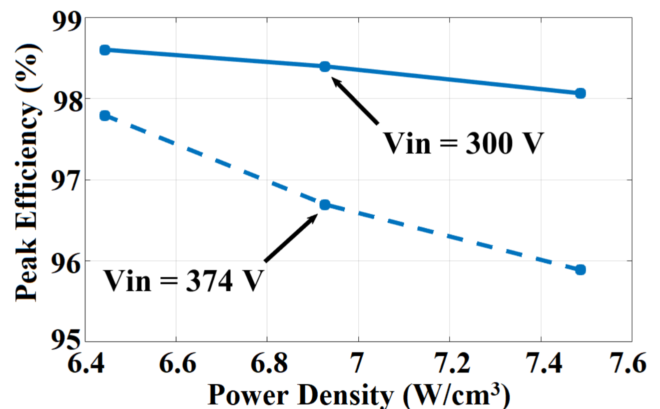
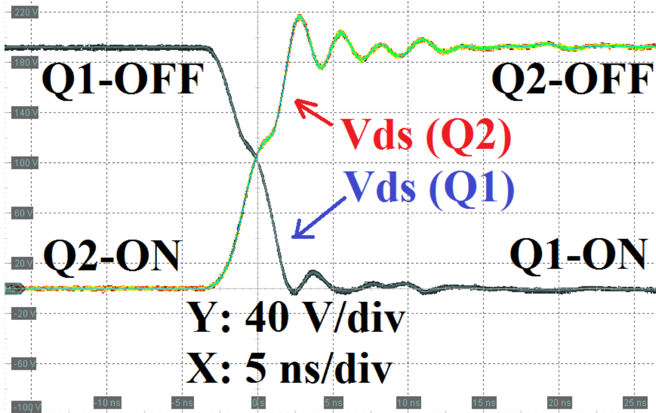


Fig. 9. Peak efficiency vs. power density (three variant designs).

TABLE IV. PEAK-TO-PEAK OUTPUT VOTLAGE RIPPLE (MEASURED VOLTAGE AND CALCULATED PERCENTAGE).

Output Power 10 W (Worst-Case)	Vin	Switching Frequency		
		1.5 kHz	2.5 kHz	4 kHz
C2-nom = 9 µF	300 V	**3.085 V (2.06 %)**	1.835 V (1.22 %)	0.896 V (0.60 %)
	374 V	**2.030 V (1.09 %)**	0.922 V (0.49 %)	0.371 V (0.20 %)
C2-nom = 6 µF	300 V	4.180 V (2.79 %)	**2.325 V (1.55 %)**	1.955 V (1.30 %)
	374 V	2.840 V (1.52 %)	**1.420 V (0.76 %)**	0.806 V (0.43 %)
C2-nom = 3 µF	300 V	5.630 V (3.75 %)	3.580 V (2.39 %)	**2.125 V (1.42 %)**
	374 V	4.400 V (2.35 %)	2.295 V (1.23 %)	**1.056 V (0.56 %)**



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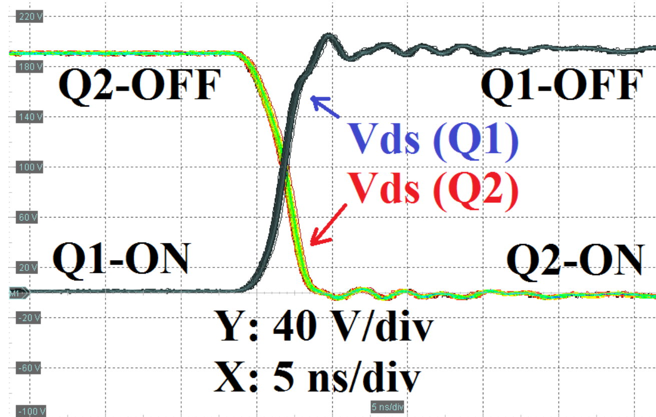
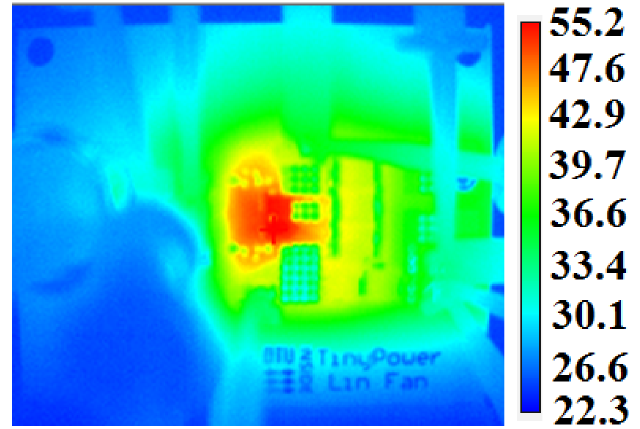


(b)

Fig. 10. Measured waveforms. Input voltage of the converter is 380 V. Both Q1 and Q2 are high-side switches. The ringing is partly reduced by the custom-made local ground connections for the oscilloscope probes. Due to the high density of the converter with double-side mounted components, the ringing is not completely removed when differential signals are measured with interactive signal-ground loops. The ringing is mainly parasitic effect and does not show up when single-ended signals are separately measured. (a) Q1-turn-on/Q2-turn-off transient. (b) Q2-turn-on/Q1-turn-off transient.

The peak efficiency versus the power density of the power stage is summarized in Fig. 9 for the three variant designs. The peak efficiencies of the high efficiency design (C2-nom, 9 µF) are 98.6 % and 97.8 % at 300 V and 374 V input voltages, respectively. The high power density design (C2-nom, 3 µF) reaches a power density of 7.5 W/cm^3 (123 W/inch^3), which is based on the boxed volume of the power stage (the white-boxes as shown in Fig. 4).



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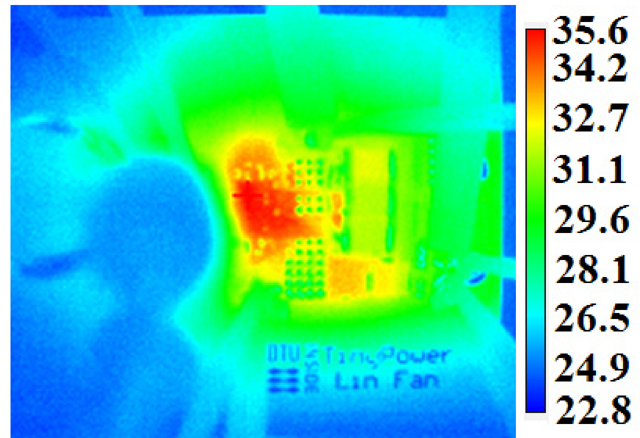

(b)

Fig. 11. Thermal images (°C) measured after one hour full-power operation, no heatsink, no airflow (annotated with output power, input voltage, nominal capacitance of C2, and switching frequency). (a) 10 W, 374 V, 3 µF, 4 kHz. (b) 10 W, 300 V, 9 µF, 1.5 kHz.

The peak-to-peak output voltage ripples are measured at the worst-case condition of the maximum output power of 10 W, for the three variant designs with different input voltages and switching frequencies. The results are summarized in Table IV, and the bold numbers in green colour are measured when the designs are operated with the optimized switching frequencies. The worst-case peak-to-peak output voltage ripples are between 0.56 % and 2.06 % at the full load conditions. For a given design, the peak-to-peak output voltage ripples are higher with the input voltage of 300 V compared with the input voltage of 374 V, and it is because the load current is higher in the case of 300 V input voltage for a given output power of 10 W.

For the measured waveforms shown in Fig. 10, the Rohde & Schwarz RTO-1024 2-GHz oscilloscope and the RT-ZP10 500-MHz single-ended passive probes are used for the measurements. The measured average slew rates of the high-side GaN switches (Q1 and Q2) are about 40–50 V/ns.

The thermal images of the prototype converters are shown in Fig. 11, at the maximum output power of 10 W after one hour operation without heatsink or airflow. The heat density is high around the GaN switches due to the limited available copper area connecting the small land patterns of the devices to conduct currents and heat.

V. CONCLUSIONS

A high-voltage low-power switched-capacitor DC-DC converter is designed, implemented and validated with experimental results. The GaN switches and the SiC diodes are analysed, combined and utilized to properly address the challenges at high-voltage and low-power levels. The trade-off between the conduction loss and the switching loss is optimized with switching frequencies. Three variant designs with the trade-off between the efficiency and the power density are experimentally validated. A peak efficiency of 98.6 % and a power density of 7.5 W/cm^3 (123 W/inch^3) are achieved, without any heatsink or airflow. The converter is intended for applications such as LED drivers.

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