Rajaguru, P. and Bailey, Christopher and Aliyu, Attahir Murtala and Castellazzi, Alberto and Pathirana, V. and Udugampola, N. and Trajkovic, T. and Udrea, F. and Mitchelson, P.D. and Elliot, A.D.T. (2017) Co-design/simulation of flip-chip assembly for high voltage IGBT packages. In: 23rd International Workshop on Thermal Investigations of ICs and Systems, THERMINIC 2017, 27-29 September 2018, Amsterdam, Netherlands.

Co-Design/Simulation of Flip-Chip Assembly for High Voltage IGBT Packages

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Abstract

This paper details a co-design and modelling methodology to optimise the flip-chip assembly parameters so that the overall package and system meets performance and reliability specifications for LED lighting applications. A co-design methodology is employed between device level modelling and package level modelling in order enhance the flow of information. As part of this methodology, coupled electrical, thermal and mechniacal predictions are made in order to mitigate underfill dielectric breakdown failure and solder interconnect fatigue failure. Five commercial underfills were selected for investigating the trade-off in materials properties that mitigate underfill electrical breakdown and solder joint fatigue.

1. Introduction

LED lighting products are rapidly taking the lead position in domestic, industrial and display markets. A significant portion of these products need to be highly compact, for example to fit into a GU10 bulb housing (see Fig. 1). Compactness can be achieved by increasing the switching frequency, but this is not a trivial task since improved electrical performance posees challenges in terms of thermal management, EMC, and reliability.

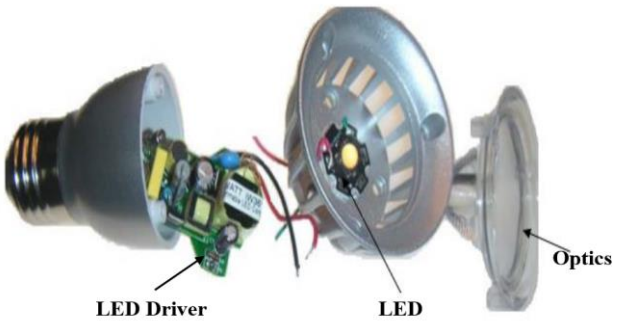

Fig 1: LED driver inside a GU10 housing

At present, most LED driver systems are based on vertical MOSFET devices. The vertical design of the Power MOSFET, where high voltage terminal is at the back of the die and low voltage terminals are at the front, imposes a major barrier for monolithic integration, co-packing or even Chip On Board (COB) assembly. Moreover, very high dV/dt and dI/dt seen in MOSFET switching transients pose significant challenges with EMC as they cause excessive voltage spikes at turn-off and current spikes at turn-on.

To address these issues, additional components such as snubbers must be used thus cancelling out potential size benefits of increased frequency.

Replacing the vertical MOSFET by lateral IGBTs (LIGBT) for LED driver can provide significant advantages as these LIGBTs are more than ten times smaller compared to vertical MOSFETs at these current and voltage ratings and have all terminals on the front side of the die allowing area-efficient flip-chip packaging as in Fig 2. Moreover, they have much smoother switching transients compared to MOSFETs with breakdown voltages in excess of 800V and avalanche capability [1, 2] allowing to eliminate snubbers and avalanche protection circuits hence resulting in a reduction in overall number of system components.

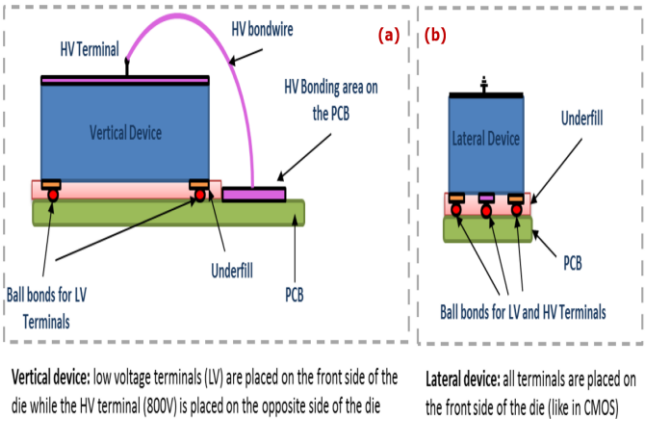

Fig 2. (a) COB assembly using a vertical device and (b) a lateral device for the same power level.

The layout of the LIGBT package considered in this work is shown in Fig.3. The size of the device is 744µm x 1345µm with deposited solder balls that has a radius of around 75µm.

The layout of the fabricated LIGBT developed in 0.6µm/5V bulk silicon technology is shown in Fig. 4(a), and 3 dimensional schematic of the LIGBT device structure presented in Fig. 4(b). The PCB package design for an effective cooling of the LIGBT is presented in Fig.3 (a). The package is designed for optimal thermal performance using vias linking the device solder balls and top PCB copper layer to the base which can be used for cooling. An additional copper foil is used as a heatsink to extract heat from the backside of the device and the PCB copper layer. Solder is used to attach the copper foil to the device backside to improve thermal performance.

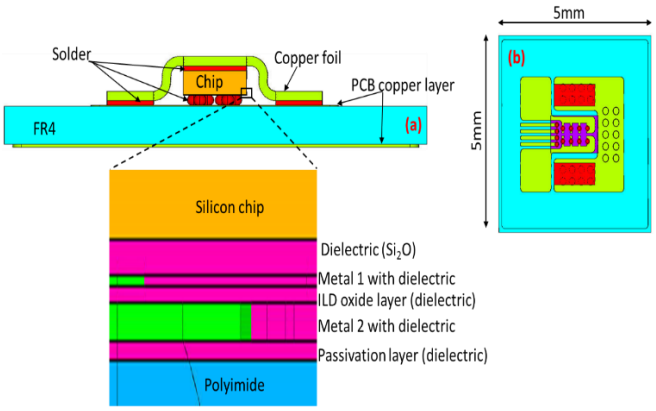

Fig 3: (a) Layout of the LIGBT package in side view, (b) top view of the package

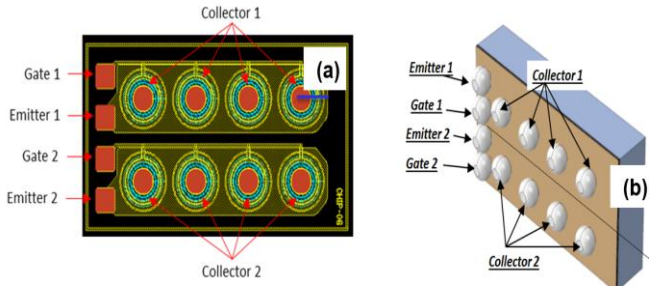

Fig.4: (a) Fabricated LIGBT in 0.6µm bulk silicon technology layout (b) Terminal layout of two identical LIGBTs with a fully populated solder ball matrix on a silicon based substrate

2. Co-Design Methodology

At present design simulation for electronic packaging can generally be classified as:

- Single physics/component/user
- Lot of point analysis tools
- Few design points investigated

Co-design is inclusive, encompassing collaborative, co-operative, concurrent research in any design objective. The aim of co-design is to

- Foster communication between academic researchers and industry practitioners concerned with collaborative design;
- Model and simulate the coupon between different physis: Electrical, Thermal, Mechanical
- Encourage a flow of information across the boundaries of the disciplines (device, package and system level) resulting into a collaborative optimised design product

In this project, both TCAD (at device level) and finite element (at package level) models are used to characterise the electrical and thermo-mechanical behaviour of the lateral IGBT devices and their packaging using flip-chip assembly techniques.

At the device level, TCAD models provide electrical results in terms of voltages and currents. The predicted voltages are then used as boundary conditions to predict the electric field across the package and the electric field strength throughout the underfill.

It is important to understand the behaviour of the underfill and optimise its properties in terms of dielectric strength, permittivity, and CTE and modulus. For the packaging design engineer, this type of package requires trade-offs in terms of electrical behaviour and thermo-mechanical behaviour. Underfills with high dielectric strength (e.g. can withstand high voltages) tend to have high CTE's above the glass transition temperature (T_g). Hence it is important to undertake both electrical and thermo-mechanical analysis.

3. Device Level Modelling

The version of TCAD software used in this study is 'Medici' [3]. Medici predicts the electrical characteristics of arbitrary two-dimensional structures under user specified operating conditions. The program solves Poisson equation to determine the potential distribution in a device. It is applicable to a broad variety of technologies, ranging from submicron devices to large power structures. From TCAD modelling the electric potential distribution (as in Fig 7) on the device was extracted and these electric potential were the boundary condition for package level modelling.

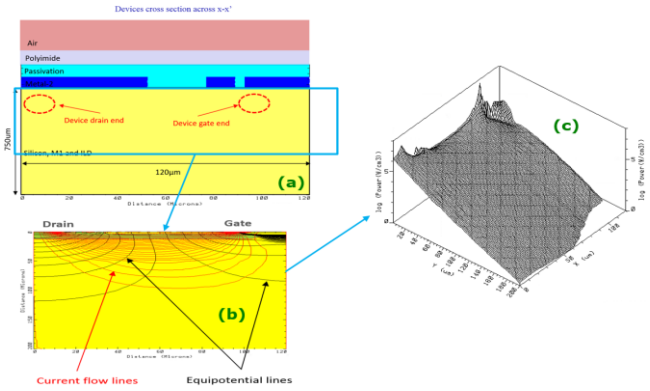

Fig 7. (a) Device cross section, (b) Equipotential lines on the device generated from TCAD software, and (c) 3D plot of the logarithmic power distribution on the device

4. Package Level Modelling

The challenging aspect of the LIGBT package in high voltage application is preventing underfill dielectric breakdown and solder fatigue failure. The underfill reduces the inelastic strain in the solder and improves the thermal fatigue life of the flip chip solder joint. Furthermore underfill (UF) materials reduce and redistribute the stresses and

strains in the structure by minimising the coefficient of thermal expansion (CTE) mismatch.

Underfill dielectric breakdown (also referred as breakdown voltage) is the maximum electric field which an underfill can withstand before complete breakdown. It has been reported that the dielectric strength of an underfill should be above 20 KV/mm [4].

In high voltage applications, the underfill needs to withstand the extreme electric fields, hence its dielectric strength should be higher than the extreme electric field. In contrast, choosing an underfill with high dielectric breakdown value could compromise the solder joint reliability. Hence the choice of underfill for flip chip assembly is important in the context of overall reliability.

4.1. Electromagnetic Modelling of Package Structure

A finite element model was built for the flip-chip package assembly (see fig 8a). The electromagnetic analysis was undertaken by solving the Poisson equation (equation (1))

$$\nabla \times E = 0 \quad \Rightarrow \quad \nabla(\nabla V) = -\frac{\rho}{\varepsilon} \qquad (1)$$

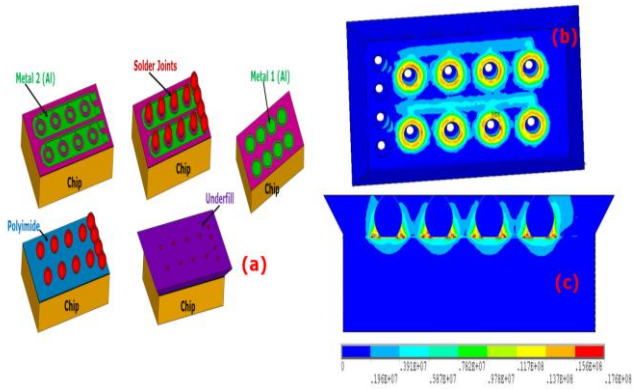

Fig 8: (a) Package model for the electro-static analysis (b) electric field vector sum distribution on the bottom of the underfill, and (c) electric field vector sum distribution on the cross section of the underfill

The material properties of device were sourced from public domain [5] for initial study. The permittivity values of underfill, solder (Sn3.5Ag), polyimide, SiO2, aluminium, Si die are respectively 3.47, 2, 3.2, 3.9, 1.6, and 11.8.

The TCAD simulation electric potential distribution was set as boundary condition on the package level simulation and electrostatic analysis was undertaken in order to predict the electric field in the underfill. Higher electric field distribution was concentrated in the region close to polyimide/solder/underfill interface as in Fig 8 (c)

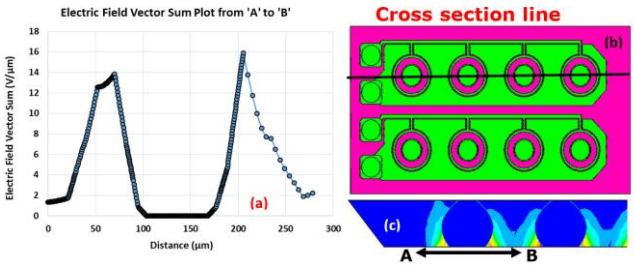

Fig 9: (a) Electric field versus distance from 'A' to 'B' across the solder bump, (b) Top view of the cross section line, (c) electric field vector sum distribution from the side view.

Figure 9 details the electric field around solder bumps and across the underfill. What is of interest here is the magnitude of the field in relation to the dielectric field strength.

At high electric field values, there can be a risk of dielectric breakdown. Increase in underfill relative permittivity value decreases the extreme electric field vector sum in the underfill. If the maximum electric field is less than dielectric breakdown strength of the underfill, then underfill can withstand the breakdown related failure. Among commercially available underfill, five underfill adhesives types from three leading manufacturers, Henkel Loctite Corporation [6], United Adhesives [7] and Materbond Inc. [8] were selected in this study for their high dielectric breakdown strength value. All these selected underfill have dielectric breakdown value in the range of 20 - 40 KV/mm and relative permittivity value in the range of 3 to 4.

4.2. Thermo-Mechanical Modelling of Package Structure

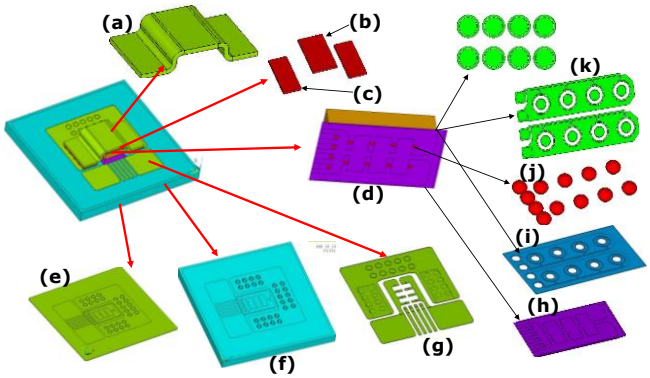

Fig.10: Components of package structure (a) Copper foil, (b) solder layer between copper foil and die, (c) solder layer between copper foil and PCB, (d) chip package, (e) copper layer on the bottom of the FR4 PCB, (f) FR4 PCB, (g) coper layer on top of the FR4, (h) underfill layer, (i) polyimide layer, (j) solder bump, and (k) aluminium metal layer (metal 1 and 2)

Thermo-mechanical finite element modelling of package structure of LIGBT device was undertaken in order to predict the strain and stresses in the solder layers. The package components consists of LIGBT device is as in Fig 10. Solder material has viscoplastic material properties. The Anand's viscoplastic model [9, 10] was used in this study to model the behaviour of the solder. FEA simulation was undertaken in ANSYS using the element SOLID185.

Table 1: Elastic and thermal material properties

Material	**Density (kg/m^3)**	**CTE ($10^{-6}/K$)**	**Young's Modulus (GPa)**	**Poisson Ratio**
FR4 PCB	1850	18.5	22	0.28
Polyimide	1420	13	14.5	0.34
Dielectric (SiO2)	2200	0.54	69	0.17
Aluminium (Al)	2700	23.1	124	0.35
Silicon (Si)	2329	2.8	131	0.3
Solder (Sn3.5Ag)	7360	21.85+0.0204*T(°C)	-0.075*T(°C)+52.582	0.4
Copper (Cu)	8900	16.9	180	0.31

Table 2: Structural and thermal material properties of Underfill materials used in this study

Underfill Name	**Density (kg/m^3)**	**CTE ($10^{-6}/K$)**	**Young's Modulus (GPa)**	**Poisson Ratio**
UF1230 (United Adhesives)	1670	75 (> T_g) 19 (< T_g)	7.6	0.32
UF1240 (United Adhesives)	1600	89 (> T_g) 22 (< T_g)	7	0.32
Loctite 3655 (Hysol)	1740	80 (> T_g) 25 (< T_g)	3.5	0.316
Loctite 3653 (Hysol)	1520	110(>T_g) 35 (< T_g)	2.8	0.274
EP3UF (Materbond)	1420	25	3.103	0.29

Relevant material properties are given in tables 1 and 2. The standard temperature cycling with ramp and dwell time of 3 and 15 minutes with range of (-25, 125) was imposed on the model. The plastic strain distribution of solder bump is shown in Fig 8. Accumulated plastic strain of solder bump, solder layer between copper foil and PCB, and the solder layer between copper foil and the silicon substrate were evaluated by volume weighted averaging of thin layer (10 µm) of the total volume. A Coffin Manson fatigue model [11] was utilised for lifetime of solder. The fatigue model parameters utilised in this study is as in equation (2)

$$\Delta\varepsilon_{Pl}^{acc}\left(N_f\right)^{0.6978} = 3.921 \qquad (2)$$

Where N_f is the cycles to failure, and $\Delta\varepsilon_{Pl}^{acc}$ is the accumulated plastic strain in one cycle.

5 . Results

It was noted that solder layer between copper foil and the silicon substrate has the worst lifetime in comparison with lifetime of the solder bumps enclosed in the underfill. This highlights the solder bump's stress reduction capabilities by the underfill. Figure 11 & 12 details the thermo-mechanical behaviour of the packaged assembly, and the predicted plastic work at each of the solder joints as well as the joints that connect the copper heat spreaders.

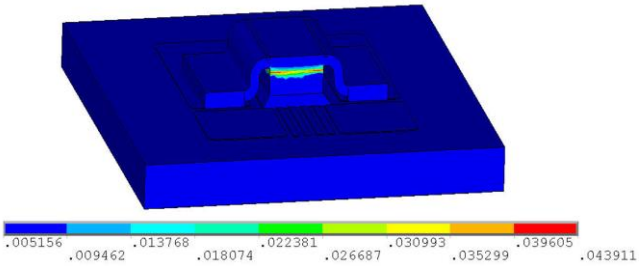

Fig 11: Accumulated plastic strain distribution in one cycle on the package

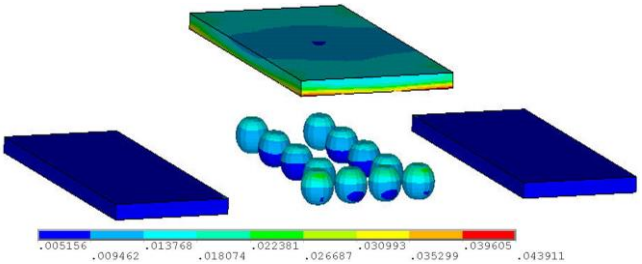

Fig 12: Accumulated plastic strain distribution in one cycle on the solder layers/bumps of the package

Table 4: Cycles to failure of solder layer and solder bump for various underfill materials

Underfill	Lifetime of solder layer (Cycles to Failure)	Lifetime of solder bump (Cycles to Failure)
UF1	1696	4403
UF2	1737	3041
UF3	1825	3644
UF4	1864	3496
UF5	1842	3622

Assuming that the damage model (equation 5) can be used for both types of joints, then clearly the solder layer may be the weak link in terms of thermo-mechanical life.

6 . Conclusion

The aim of the work reported in this paper is to develop a co-design/simulation methodology for the flip-chip assembly of lateral IGBT's. This requires electrical and thermo-mechanical modelling at both the device and package levels. Of importance is the properties of the underfill in minimising the risk of dielectric breakdown and solder joint fatigue. The paper provides details of this methodology, comparisons for different underfills in terms of their ability to withstand high voltages, and maximise the reliability of the solder joints.

Acknowledgement

This research has been funded by the Engineering and Physical Science Research Council (EPSRC) through the

Underpinning Power Electronics HUB (EP/K035304/1). It supports the cross theme project: Compact and Efficient off-line LED Drivers Using 800V Lateral IGBTs and Chip-On-Board Assembly

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