Improved Nanopipelined RTD Adders using Generalized Threshold Gates

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ABSTRACT[1]

Many logic circuit applications of Resonant Tunneling Diodes are based on the MOnostable-BIstable Logic Element (MOBILE). Threshold logic is a computational model widely used in the design of MOBILE circuits, i.e. these circuits are built from threshold gates (TGs). This paper describes the design of full adders (FAs) using TG based circuit topologies. Both the selection of different MOBILE TG networks and the use of gates that can be considered extensions of the MOBILE TG are addressed. The FAs are applied to the design of nanopipelined carry propagations adders which are evaluated and compared to a previously reported one, showing advantages in terms of speed, power and power delay product.

Keywords: Resonant Tunneling Diodes, MOBILE, Threshold gate, nanopipelining, adder

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I. INTRODUCTION

Resonant tunneling devices (RTDs) are nowadays considered the most mature type of quantum-effect devices. They are already operating at room temperature and they exhibit very attractive characteristics as high-speed operation and low power consumption. RTDs are very fast non linear circuit elements which have been integrated with transistors to create novel quantum devices and circuits. This incorporation of tunnel diodes into transistor technologies has shown an improved circuit performance: higher circuit speed, reduced component count, and/or lowered power consumption [1], [2], [19], [20]. Most of the reported working circuits have been fabricated in III/V materials while Si-based tunnelling diodes compatible to standard CMOS fabs are currently an area of active research [5].

RTDs exhibit a negative differential resistance (NDR) region in their current-voltage characteristics (Figure 1a) which can be exploited to significantly increase the functionality implemented by a single gate in comparison to conventional MOS and bipolar technologies, thus reducing circuit complexity. Figure 1a depicts the circuit symbol used for RTDs and their typical *I-V* curve showing key parameters for circuit design: peak current and voltage, I_p and V_p, and valley current and voltage, I_v and V_v. Many RTD based logic blocks rely on using the clocked series connection of a pair of RTDs or Monostable Bistable Logic Element (MOBILE) [6] which operates on the basis of the comparison of peak currents (Figure 1b). In general, MOBILE logic families combine the basic pair of series-connected RTDs with different three terminal devices to achieve input-output isolation and functionality (Figure 1c). Inherent self-latching property of MOBILE allows the implementation of pipeline at the gate level.

The operating principle of MOBILE is extremely well suited to implement the arithmetic operation on which Threshold Gates [7] (TGs) are based [8], [9]. TGs are a generalization of conventional Boolean gates, which are able to implement more complex functions, what is attractive from the point of logic design (less gates and interconnec-

tions). TG design style is a well recognized powerful alternative to the standard logic design because of the intrinsic complexity of the functions performed by TGs allowing realizations that require less threshold gates than standard threshold logic. MOBILE TGs have been experimentally demonstrated and it has been reported the logic architecture of a nanopipelined carry propagation adder using them [10].

Currently research on circuit topologies using RTDs and transistors is an active area. Different generalizations of threshold gates, also suitable to be realized with MOBILE RTD structures which further increase the functionality of conventional TGs, are being investigated [11], [12], [13], [14]. Comparatively, less effort is dedicated to the evaluation and comparison of these building blocks within networks implementing logic applications. As in conventional design, different gate networks realizing same functionality exhibit different power and delay performance, even using the same logic style for the gates. Fan-in and fan-out capabilities of the building blocks are critical and their electrical behaviour can make a logic solution better than others. However, little attention is given to this in the literature. This work explores threshold-gate based MOBILE logic styles with this focus and their usage in the design of nanopipelined adders that significantly improve speed and reduce power-delay product with respect to the previously reported one [10]. The rest of the paper is organized as follows. Section II introduces both the electrical and the logical background of this work. Section III describes the design and characterization of MOBILE TGs implementations as a motivation for the proposed full adders introduced in Section IV. Architectures of 8-bit adders using them are described, simulated and compared in Section V. Finally, Section VI gives some conclusions.

II. BACKGROUND

In this section the operation principle of clocked series-connected RTDs (MOBILE) is summarized. Then, the threshold gate is formally defined and its MOBILE implementation described. Finally, the previously reported RTD based adder which serves as a reference is introduced.

A. MOBILE operating principle

The MOBILE (Figure 1b) [6] is a rising edge triggered current controlled gate which consists of two RTDs connected in series and driven by a switching bias voltage (V_{bias}). When V_{bias} is low, both RTDs are in the on-state (or low resistance state) and the circuit is monostable. Increasing V_{bias} to an appropriate maximum value ensures that only the device with the lowest peak current switches (*quenches*) from the on-state to the off-state (or high resistance state). Output is high if the driver RTD is the one which switches and it is low if the load switches. Assuming equal current densities for both RTDs, peak currents are proportional to RTD areas, λ_A and λ_B, for load and driver respectively. Thus, for $\lambda_A < \lambda_B$ the load switches (the output V_{out} goes to low or "0") and if otherwise, $\lambda_B < \lambda_A$, the driver switches (the output V_{out} goes to high or "1").

Logic functionality can be achieved if the peak current of one of the RTDs is controlled by an input. In the configuration for an inverter MOBILE shown in Figure 1c, the peak current of the driver RTD can be modulated using the external input signal V_{in}. During a critical period when V_{bias} rises, the voltage at the output node V_{out} goes to one of the two stable states (low or high), corresponding to "0" and "1" in binary logic. RTD areas are selected in such a way that the value of the output depends on whether the external input signal V_{in} is "1" or "0". Constraints on relationships among RTD areas for inverter functionality are depicted also in

Figure 1c. These constraints assume that the transistor behaves like an ideal switch. That is, for V_{in} high, the transistor does not limit the RTD current and its peak current, which is proportional to λ_1, adds to the one of the driver in the non functional branch, λ_B. For V_{bias} high, the output node maintains its value even if the input changes. That is, this circuit structure is self-latching allowing to implement pipelining at the gate level without any area overhead associated to the addition of the latches which allows very high through-output. This circuit topology can be easily extended to systematically implement TGs which have been experimentally shown [8], [10].

A sufficiently slow V_{bias} rising is required for MOBILE operation. That is, there is a critical rise time for the switching bias below which the gate does not operate correctly and this determines its operating frequency. Under that critical time rise time, there is at least one input combination for which the gate does not produce the expected logic output. It is due to AC currents associated to parasitics (more important for faster bias changes) that somewhat "alter" the ideal MOBILE operating principle based on peak currents comparison. This critical value depends on both circuit (size of RTDs and transistors) and technological parameters [15], [16].

B. MOBILE TGs

Threshold logic has been pointed out as an efficient computational model for the design of RTD based circuits. That is, the basic building blocks for RTD logic circuits are threshold gates instead of the conventional Boolean gates (AND, OR,...).

A TG or linear separable function is defined as a logic gate with n binary input variables, $x_i, (i = 1, \ldots, n)$, one binary output y, and for which there is a set of $(n + 1)$ real numbers: threshold T and weights $w_1, w_2, \ldots, w_n$, such that its input-output relationship is defined as

$y = 1$ *iff* $\sum_{i=1}^{n} w_i x_i \geq T$, and $y = 0$ otherwise. Sum and product are the conventional, rather than the logical, operations. The set of weights and threshold can be denoted in a more compact vector notation way by $[w_1, w_2, \ldots, w_n; T]$.

Figure 1d shows the implementation of a generic TG defined as $y = 1$ *iff* $w_1x_1 + w_2x_2 - w_3x_3 - w_4x_4 \geq T$, and 0 otherwise. The RTD areas determine the weights w_i ($i = 1, \ldots, 4$) and the threshold *T.* Input stages controlled by external inputs are placed in parallel to RTD_1 or RTD_2 depending on whether the associated weight is positive or negative, allowing the control of the peak currents of both NDRs.

C Reference nanopipelined TG-based adder

Figure 2 shows the logic diagram of the nanopipelined carry propagation adder proposed in [10]. It consists of a chain of full adders (FAs) and memory elements (MOBILE buffers and inverters) to support pipeline. Only those associated with inputs are depicted. Each FA is realized with a network of MOBILE TGs as depicted in Figure 3.

The FA takes three binary inputs and generates the carry output, which is one if two or more inputs are logic ones (majority function), and the sum output, realized by an EXOR logic operation. In the proposed realization, the carry operation is implemented by a single gate due to the fact that the majority function is the threshold function [1, 1, 1; 2]. When the weighted sum of inputs is equal or greater than 2, the output is logic 1, since all weights are 1, two or three inputs at one produce a high output. However, the sum operation requires the implementation of a three-input EXOR. This is a non threshold function and thus requires a network of TGs. The four gate network used and showed in Figure 3a is based on a general technique to implement symmetric functions [7]. It is important to realize that it contains the three-input majority gate as is shown. Thus, the carry output can be extracted from the EXOR network directly.

Table in Figure 3b shows that the outputs of the first level TGs codify the number of ones in the inputs: n_1 is 1 if there is at least one input at one, n_2 is 1 if there are at least two ones and n_3 is one if all the three inputs are 1. Output of gate [1, -1, 1; 1] generates the 3-EXOR.

Circuit schematic is shown in Figure 3c. Bias signals to operate cascaded MOBILE-type circuits [10] are also shown (Figure 3d). A four phase (evaluation, hold, reset and wait) overlapping clocking scheme is used. Second stage evaluates (rising edge of V_{bias2}) while the first stage is in the hold phase (V_{bias1} high). For a number of logic levels greater than three, four bias signals are required. In one clock period all the gates are activated. Data can be processed at a frequency given by $f_{max} = 1/(4 \cdot t_{r(crit)})$ where $t_{r(crit)}$ is the minimum rise time that produces a correct behavior in all gates of a network. Otherwise, the latency time, t_{lat}, is given by the number of levels of the network: for a network of *k* levels $t_{lat} = k \cdot t_r$.

III. MOBILE THRESHOLD GATE IMPLEMENTATIONS

This Section describes some experiments of characterization of MOBILE TG implementations which provide support for both the design methodology followed in the implementation of the adders, and for the new concepts on which the proposed adders rely on, as it will be clarified later. As it was previously stated, the minimum value for the rise time of the bias signal for which a MOBILE gate operates correctly depends on both design parameters, like RTD areas and transistor dimensions, and technological parameters. We have carried out extensive simulation and analysis of MOBILE gates in order to derive design guidelines to optimize their performance and to determine which TGs exhibit better performance.

MOBILE TGs with different fan-in have been designed and evaluated using a non commercial university InP technology in which RTD and HFET transistors can be co-integrated. For this RTD, V_p is 0.21V, the peak current density 21KA/cm^2, the peak to valley current ratio is about 6.25

at room temperature and the capacitance is 4fF/μm^2. The transistor threshold voltage is –0.2V for the depletion HFET and 0.2 V for the enhancement one. Minimum gate-length is 0.6μ and *transconductance parameter 500μA/V^2 (depletion type) and 900μA/V^2 (enhancement type)*. Gate design implies sizing of RTDs and transistor. As in the simple inverter gate (Figure 1c), target logic functionality imposes a set of constraints on RTD area relationships which must be fulfilled and which can be used to select RTD sizes. However, the solution to this set of inequalities is not unique. Circuit performance in terms of operating frequency and power depends on the selected RTD areas as it is shown in the following. Transistor sizing also determines correct operation and circuit performance.

First, the simplest TGs, the inverter (Figure 1c) and the follower (input branch in parallel to load RTD), have been evaluated through HSPICE simulations using experimentally validated models for the RTDs and the transistors. Figure 4 depicts operating frequency and PDP (power/frequency) as a function of transistor width. Minimum gate-length transistors have been used. The sizes of the RTDs have been selected solving the design constraint using as cost function to minimize the sum of the RTD areas and technological constraints on minimum sizes. High and low voltage values for clocked V_{bias} and V_{in} are 0V and 0.7V respectively. Results for both depletion and enhancement transistors are shown. It can be clearly observed that the enhancement transistor is better for the inverter and the depletion one for the follower. In addition, an analysis of the operation frequency shows that a large enough transistor is required to supply the required current of the RTD associated with each specific input branch, but it exists an optimal transistor width over which operating frequency starts to decline. Although a larger transistor in the input branch leads an NDR characteristic closer to an ideal one, which explains the initial increment of the frequency, it involves higher parasitic capacities that are responsible for its reduction. Similar experiments carried out with more complex TGs also indicate that for branches in parallel to load (driver) RTD depletion (enhancement) HFETs are preferable for

operating frequency and power-delay product, as well as the existence of an optimal transistor width.

Figure 5 depicts operating frequency and power for different RTD sizings of an inverter. They have been obtained adding a term δ to the left hand side of the design inequalities in Figure 1c, and solving for different values of this parameter with the cost function previously described. While increasing δ, the operating frequency improves, although more significantly for lower δ values. However, solutions with larger δ imply larger RTD areas and the power consumption increases.

Second, experiments increasing the fan-in have been carried out. TGs with positive unitary weights and TGs with negative unitary weights with identical loads have been characterized. In each case, the threshold value resulting in the slowest implementation has been selected. Table I summarizes frequency results. It can be clearly observed that gates with negative weights operate at higher frequencies than their positive counterparts. This is due to the fact that positive weights are implemented by input branches in parallel to upper RTD, and so their transistors have a gate to source voltage which is reduced while evaluation takes places (unlike transistors in branches in parallel to bottom RTD). When bias signal starts to rise, MOBILE structures behave like a resistive voltage divisor and the output node voltage increases. This translates in that the transistors associated with upper branches are larger than those in bottom ones. In the case of the non-commercial InP technology that we have used, this is true even if depletion transistors are used for upper branches and enhancement devices for bottom ones to compensate (as we have done). Larger transistors mean higher intrinsic parasitic capacitances and loads for previous stages. The experiment suggests that negative weights are preferable. This information might be exploited at the logic level to derive logic networks with better performance. This has been done in the first proposed FA in next Section.

As expected, there is a frequency reduction associated with fan-in. Table I suggests that speed advantages of gate pipelining are not well exploited if high fan-in is used. A reduced number of input branches is preferable. This number could be kept low and still implement complex functions (in terms of number of input variables) if the switch transistor is substituted by a transistor network. This is the idea behind Generalized Threshold Gates (GTGs), on whose basis the third FA proposed in next section has been designed.

IV. PROPOSED FULL ADDERS

In this section, three alternative FAs we have developed are described. The first one is also based on TGs but a different logic network is used. The others use MOBILE structures which generalize the threshold gate. In next section, carry propagation adders built from these FAs will be evaluated and compared to the reference one.

Full Adders based on TGs

As stated in Section III, it would be desirable to obtain representations for the target functions which avoid, when possible, positive weights. Figure 6a shows an alternative TG network realization of the FA. Note that the complement of both the carry and the sum is produced. However, carry propagation adders can be also implemented chaining these modified FAs. The complement of the carry output is generated by gate [–1, –1, –1; –1]. This gate has been obtained from the one implementing the majority function, ([1, 1, ,1; 2]), changing the sign of each weight, and subtracting the sum of the weights from the original threshold (2) to determine new one (2 – (1 + 1+ 1) = –1). This transformation constitutes a basic property of threshold functions [7]. It states that given a threshold function $f(x_1, x_2, ..., x_n)$ defined by $[w_1, w_2, \ldots, w_n; T]$, $f(x'_1, x'_2, ..., x'_n)$ is also a threshold function defined by

$\left[-w_1, -w_2, \ldots, -w_n; T - \sum_{i=1}^{n} w_i\right]$. Since the three input majority is an auto dual function, the complement is obtained. The transformation has been applied to all the gates in the first level of the conventional FA realization (Figure 6a). The complement of the sum is obtained as it is shown in Table included in Figure 6b. Circuit diagram is depicted in Figure 6c.

Full Adders based on MTTG

Recently, we have proposed RTD structures implementing Multi-Threshold Threshold Gates (MTTGs) [17] which further increase the functionality of the original TGs while maintaining their MOBILE operating principle and associated advantages [14].

MTTGs are a generalization of the conventional TGs. Formally, a *k*-threshold MTTG is a logic element with n binary input variables, $x_i, (i = 1, \ldots, n)$, one binary output y, and for which there is a set of $(n + k)$ real numbers: thresholds $T_i, (i = 1, \ldots, k)$, and weights $w_1, w_2, \ldots, w_n$, such that its input-output relation is defined as: $y = 1$ *iff* $T_{2j-1} \leq \sum_{i=1}^{n} w_i x_i < T_{2j}$, with $T_{j+1} > T_j, (j = 1, \ldots, k/2)$; output y is equal to zero otherwise. As in the TGs, the set of weights and thresholds can be denoted in the vector notation way by $[w_1, w_2, \ldots, w_n; T_1, \ldots, T_k]$.

EXOR functions, which require TGs networks to be implemented, are MTTGs and as a result, it can be implemented by a single gate. In particular, the 2-EXOR is the MTTG [1, 1; 1, 2] and the 3-EXOR the [1, 1, 1; 1, 2, 3], which means that FAs can be designed using MTTGs. Figure 7a depicts the proposed logic diagram and the Figure 7b the schematic with three series connected RTDs in order to implement two-threshold functions. Note that again the complemented carry and sum outputs are generated. The carry is implemented as in previous proposed FA using a gate

with all negative weights. For the sum, a solution which uses two 2-EXOR MTTGs and an inverter TG, included to support pipeline, has been selected. An alternative FA realization in which a 3-EXNOR MTTG substitutes the two MTTGs and the inverter is also possible. This three-threshold function requires four series connected RTDs and exhibits significantly lower operation frequency than the former one. Because of this, it will not be considered for adder designs.

Full Adders based on GTGs

Input branches in all previous MOBILE structures in this paper consist of an RTD and a transistor controlled by an input variable. However, it is possible to increase the functionality that a single TG gate can implement while keeping the number of input branches low using transistor networks to control input branches. For example [11] reports a 2-EXOR with only two series connected RTDs instead of the three required by its MTTG realization and with an input branch in which two series transistors control current. We refer to this type of MOBILE structures as generalized TGs (GTGs). It can be shown that a function can be implemented by different GTGs with distinct number of input branches. The extreme case is a single one controlled by a transistor network that implements the target functionality or its complement. If the functionality is realized, the input branch is placed in parallel to the load RTD, and with the driver if the complement is implemented. Because of the performance advantages already mentioned in Section III, using few input branches, associated with negative weights (in parallel to driver RTD) is promising for high speed operation. Figure 8 depicts the circuit topology of this generic GTG. The option of a single input branch is considered in what follows. Any function can be implemented in such a way if dual rail inputs are available.

Figure 9 depicts the proposed GTG based FA. Logically it is equivalent to the MTTG based FA in Figure 7a. It can be clearly observed that the transistor network in the gate generating the

complement of the carry is on if at least two of the inputs are at logic one. Input branch for 2-EXOR gate is on for input combinations (0, 0) and (1,1). Note that negative literals are obtained by means of conventional** inverters. Pipelined operation of cascaded GTGs with the inverters, which do not exist in previously reported MOBILE topologies, has been validated through extensive simulations of several complex examples. A realization implementing the 3-EXOR o 3-EXNOR by a single gate using GTGs is also possible. As for the MTTGs, operating frequency is smaller and so the implementation of adders from such FAs will not be considered in next section.

V. CARRY PROPAGATION ADDERS

In order to evaluate the different logic networks and gate topologies applied in the FA designs, we have designed nanopipelined *n*-bit carry-propagation adders connecting them as in Figure 2 and have compared to the reference one described in Section II.C.

They have been denoted as: adder_1, which uses the proposed TG FA in Figure 6; Adder_2, based on the MTTG FA in Figure 7 and adder_3, built from the GTG FA in Figure 9. Note that these three FAs get the sum and the carry complemented, but are chained as conventional ones. This, together with the use of MOBILE inverters as memory elements to support pipeline, translate in that even stages (0, 2,..) generate the complement of their associated sum bit and odd stages (1, 3...) without being complemented. Odd stages receive complemented inputs and produce carry and sum outputs. Output latches (MOBILE elements) required to support pipeline and not shown on the figure, are in charge of generating right polarity for even sum bits. The three proposed adders, as well as the reference one, require a two-level network for the FA. This means the latency in terms of clock cycles is the same for the four adders.

**. Implemented using only two transistors. Conventional inverter is used to distinguish it from a MOBILE inverter.

In order to compare the circuit architectures, we have carried out simulations of 8-bit adders designed with the technology described in Section III. Required gates have been dimensioned using the design and simulation methodologies described in that Section.

Table I summarizes comparison among the four 8-bit adders in terms of frequency, power and power-delay product. Devices counts are reported too. All elements required to support pipeline, as well as inverters required by GTG gates, have been included in the simulations. It can be clearly observed the superiority of all proposed designs in comparison with the reference one, both in terms of frequency and power. Very significant reductions in PDP are observed for all new designs.

Among them, we can realize that the best speed result corresponds to the GTG adder (adder_3) which has almost twice the maximum frequency exhibited by adder_1. At the maximum operation frequency, adder_1 gets the best results in terms of power consumption. Nevertheless, the GTG one has the lowest PDP value due to its high operation frequency which compensates the higher power consumption obtained in comparison with the TG one.

It is important to realize that even if only TGs are used (adder_1) benefits with respect to the reference adder are obtained from the alternative logic diagram implementing the FA. It is achieved more then twice the operating frequency of the reference adder. The power for the proposed TG adder is almost 50% of the power for the reference one. This is due to the fact that the existence of input branches with depletion transistors largely contributes to the static power consumption. In order to optimize operation frequency, depletion transistors are used for all input branches, but those associated with driver RTD. Thus, in the reference design, we have 11 input branches with depletion transistor and 1 with enhancement, while in the proposed TG adder there are 10 with enhancement transistor and only two with depletion ones. At an operating frequency of 1.33 GHz, power consumption for GTG (adder_3) and proposed TG (adder_1) solutions are similar. The design based in MTTGs (adder_2) consumes more power.

In [21] we have reported that adding latches to MOBILE gates and alternating positive edge-triggered and negative edge-triggered stages, a network can be operated with a single bias phase. This greatly simplifies clock distribution issues. The four adders have been redesigned to implement the single phase architecture. Again, the three proposed ones exhibit advantages with respect to the single phase version of the reference one.

Finally, to complete the discussion of the obtained results, some comparison to transistor only implementations have been carried out. A Direct Coupled FET Logic (DCFL) implementation of a full adder in our technology exhibits a frequency of 2.2GHz and a power consumption of 1.2mW (simulation results). However, multi-bit carry propagation adders operate at a frequency which depends on the number of chained FAs (note in Table II we are reporting 8 bit adders). In fact, in order to implement multi-bit adders based on the DCFL FA at the reported FA frequency, it would be necessary to add memory elements to support pipeline, which would increase device count and power consumption. This means the power consumption of the DCFL FA suitable to be pipelined will be over 1.2mW (at 2.2Ghz). We have evaluated power for the MOBILE RTD FAs (which already operate in a pipelined fashion). Results show that they are well under 1mW for the four FAs. In particular, it is 0.56mW at 3.3GHz for the GTG FA. In addition, literature searching can also help us to place our work in reference. In [22], an four bit in a 0.5μm GaAs technology is reported with an operating frequency of 2 GHz and which compares very favorably to other logic styles (DCFL, BFL, CCDL,..). Thus, even using this advanced dynamic (there is also a clock) logic style, 8 bit adders would operate at a lower frequency than the one achieved with our RTD designs.

VI. Conclusions

In this paper different logic gate topologies based on threshold logic concepts have been explored using RTDs and HFET devices. Three FAs have been described which use TGs and a pair of extensions: the MTTG which allows more than one threshold value, and the GTG that can be interpreted as a MOBILE inverter in which the transistor in his input branch is extended to a transistor network implementing a given functionality. These FAs have been evaluated in

the design of 8-bit nanopipelined carry propagation adders and compared to a previously reported one, based on TGs. All of them have been implemented with the same technology and following an identical methodology. The three proposed adders exhibit better frequency and less PDP than the previously reported one. Even if only TGs are used benefits are obtained from the alternative logic diagram implementing the FA. The GTG adder has shown the best performance in terms of speed and power consumption in comparison with TG and MTTG ones. Nanopipelined architectures for multipliers and divisors recently reported [18] can take advantage of these advanced proposed adders.

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CAPTIONS TO THE FIGURES

Figure 1.- MOBILE circuits.

a) RTD *I-V* characteristic.

b) Basic MOBILE.

c) MOBILE inverter.

d) MOBILE TG.

Figure 2.- Logic diagram of pipelined *n*-bit carry propagation adder.

Figure 3.- Reference TG FA.

a) Logic diagram.

b) Logic behaviour.

c) Circuit structure.

d) Bias scheme for MOBILE circuits.

Figure 4.- Operating frequency and PDP as a function of transistor width.

a) MOBILE follower.

b) MOBILE inverter.

Figure 5.- Operating frequency and power consumption as a function of δ for a MOBILE inverter.

Figure 6.- Proposed TG FA .

(a) Logic diagram.

(b) Logic behaviour.

(c) Circuit structure.

Figure 7.- Proposed MTTG FA.

(a) Logic diagram.

(b) Circuit structure.

Figure 8.- Circuit structure for generic *n*-input GTG.

Figure 9.- Proposed GTG FA.

(a) Logic diagram.

(b) Circuit structure.

Table I .- Operating Frequency of TGs

Table II .- Comparison among 8-bit adders

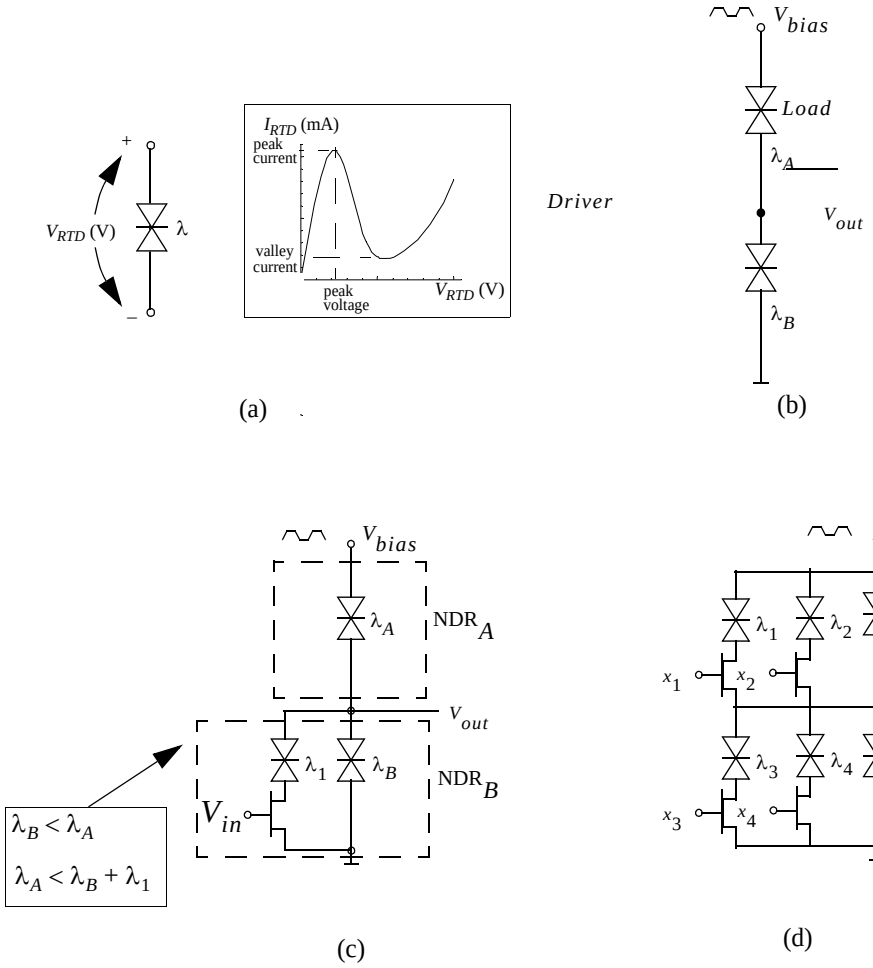

+
V_{RTD} (V)
λ
−
I_{RTD} (mA)
peak current
valley current
peak voltage
V_{RTD} (V)
Driver
V_{bias}
Load
λ_A
V_{out}
λ_B
(a)
(b)
V_{bias}
λ_A
NDR$_A$
V_{out}
λ_1
λ_B
NDR$_B$
V_{in}
$\lambda_B < \lambda_A$
$\lambda_A < \lambda_B + \lambda_1$
(c)
V_{bias}
λ_1
λ_2
λ_A
x_1
x_2
y
λ_3
λ_4
λ_B
x_3
x_4
(d)

Figure 1.

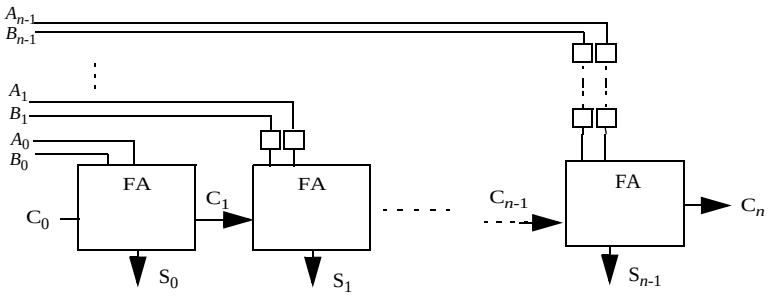
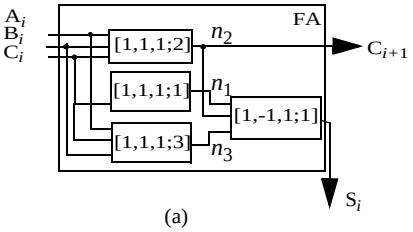


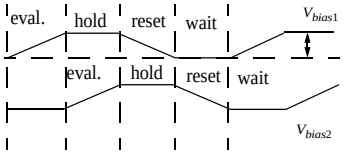
Figure 2.



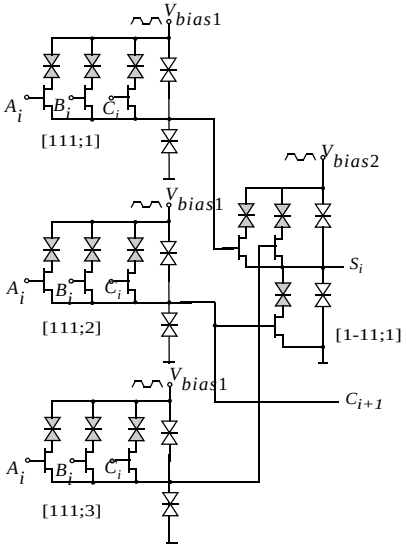
(a)

$(A_i + B_i + C_i)$	n_1	$\boldsymbol{n_2 = C_{i+1}}$	n_3	$n_1 - n_2 + n_3$	$\boldsymbol{S_i}$
0	0	**0**	0	0	**0**
1	1	**0**	0	1	**1**
2	1	**1**	0	0	**0**
3	1	**1**	1	1	**1**

(b)

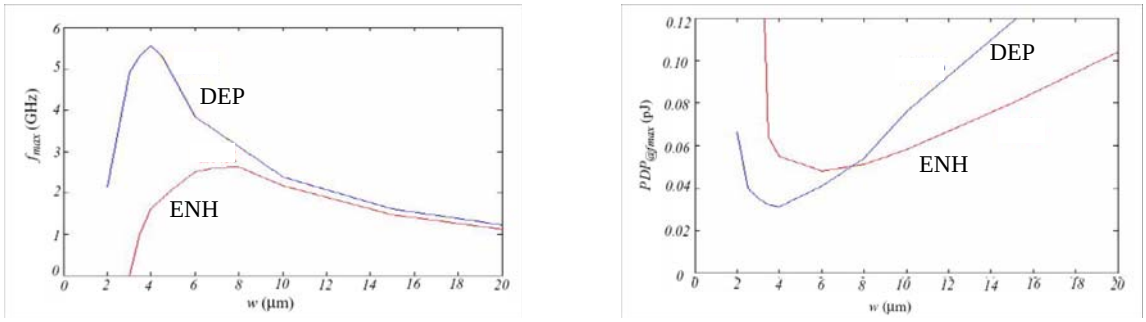


(d)

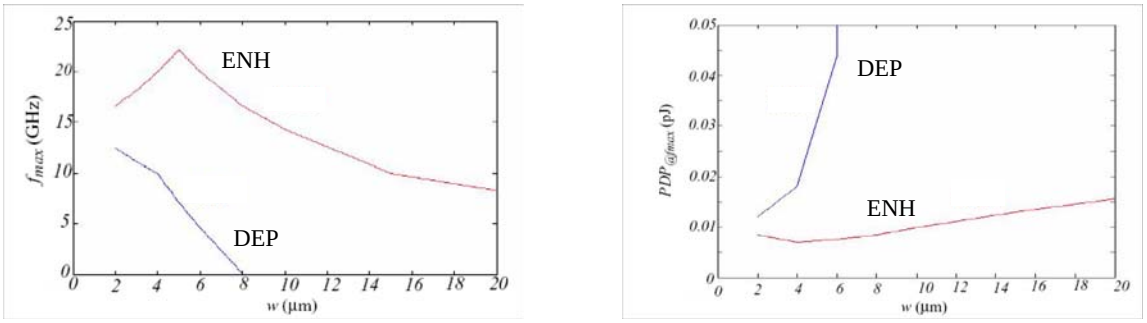


(c)

Figure 3.


DEP
ENH
f_{max} (GHz)
w (µm)
DEP
ENH
$PDP_{@fmax}$ (pJ)
w (µm)

(a)


ENH
DEP
f_{max} (GHz)
w (µm)
DEP
ENH
$PDP_{@fmax}$ (pJ)
w (µm)

(b)

Figure 4.

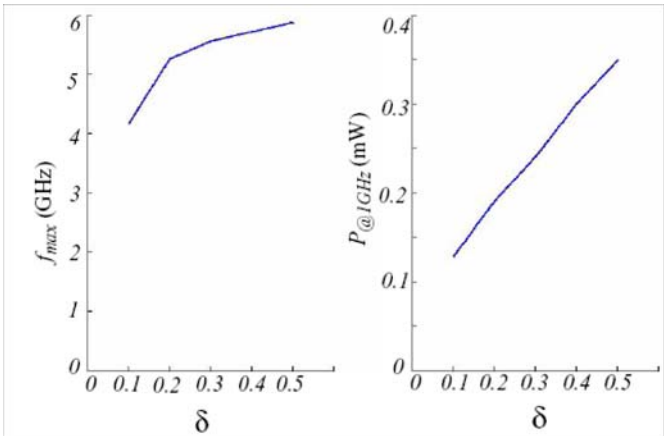
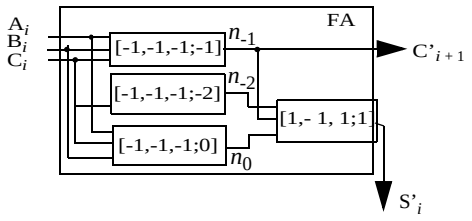

6
5
4
3
2
1
0
f_{max} (GHz)
0 0.1 0.2 0.3 0.4 0.5
δ
0.4
0.3
0.2
0.1
0
$P_{@1GHz}$ (mW)
0 0.1 0.2 0.3 0.4 0.5
δ

Figure 5.

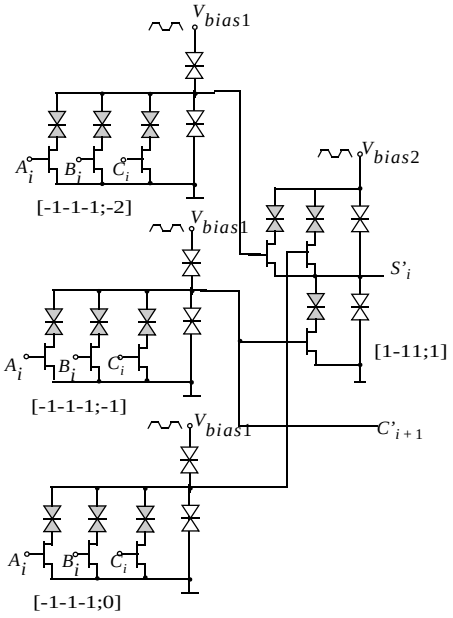


(a)

A_i

$(-A_i - B_i - C_i)$	n_{-2}	$\boldsymbol{n_{-1} = C'_{i+1}}$	n_0	$n_{-2} - \boldsymbol{n_{-1}} + n_0$	$\boldsymbol{S'_i}$
0	1	**1**	1	1	**1**
−1	1	**1**	0	0	**0**
−2	1	**0**	0	1	**1**
−3	0	**0**	0	0	**0**

(b)



(c)

Figure 6.

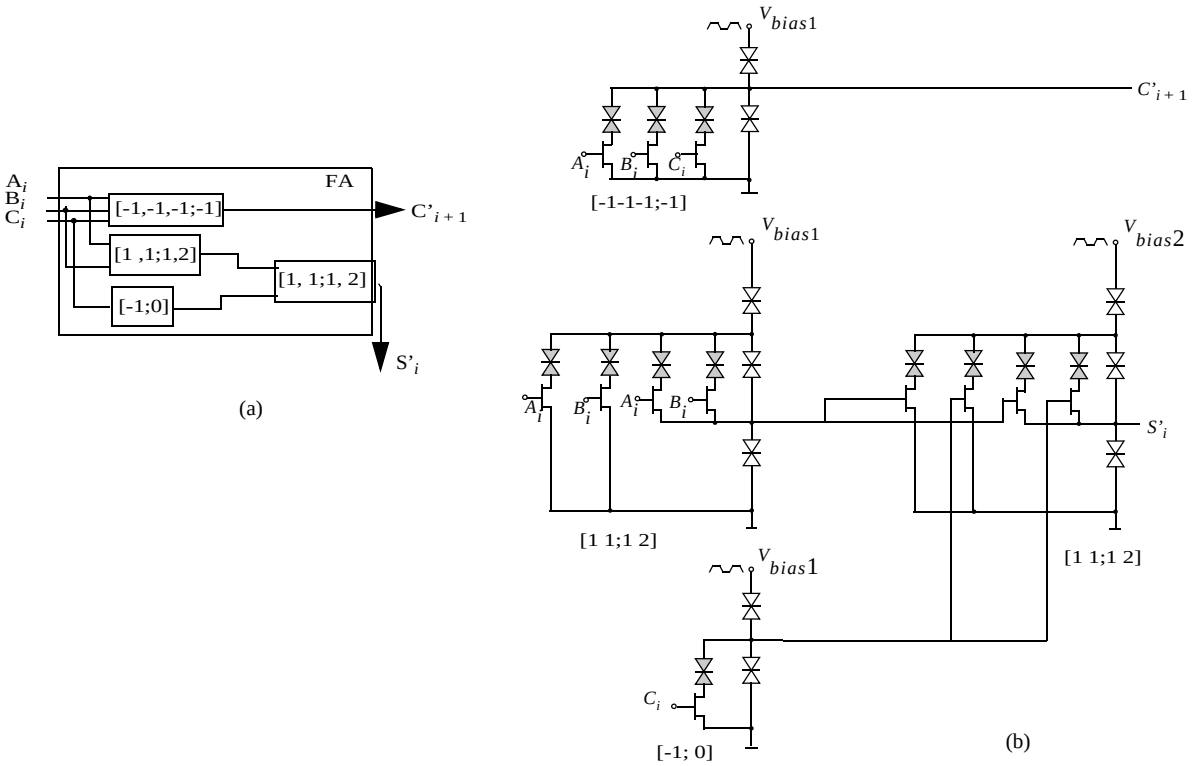

A_i
B_i
C_i
FA
[-1,-1,-1;-1]
[1 ,1;1,2]
[1, 1;1, 2]
[-1;0]
C'_{i+1}
S'_i
(a)
V_bias1
V_bias2
A_i
B_i
C_i
[-1-1-1;-1]
[1 1;1 2]
[-1; 0]
S'_i
(b)

Figure 7.

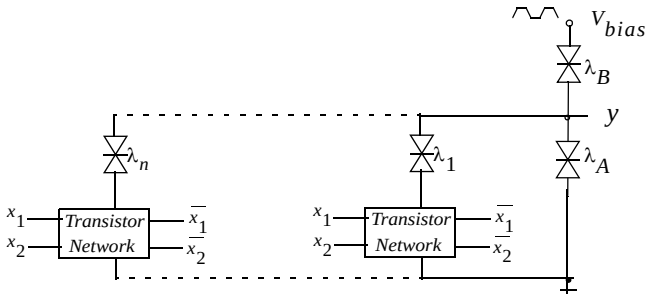

V_{bias}
λ_B
y
λ_n
λ_1
λ_A
x_1
x_2
Transistor Network
$\overline{x_1}$
$\overline{x_2}$
x_1
x_2
Transistor Network
$\overline{x_1}$
$\overline{x_2}$

Figure 8.

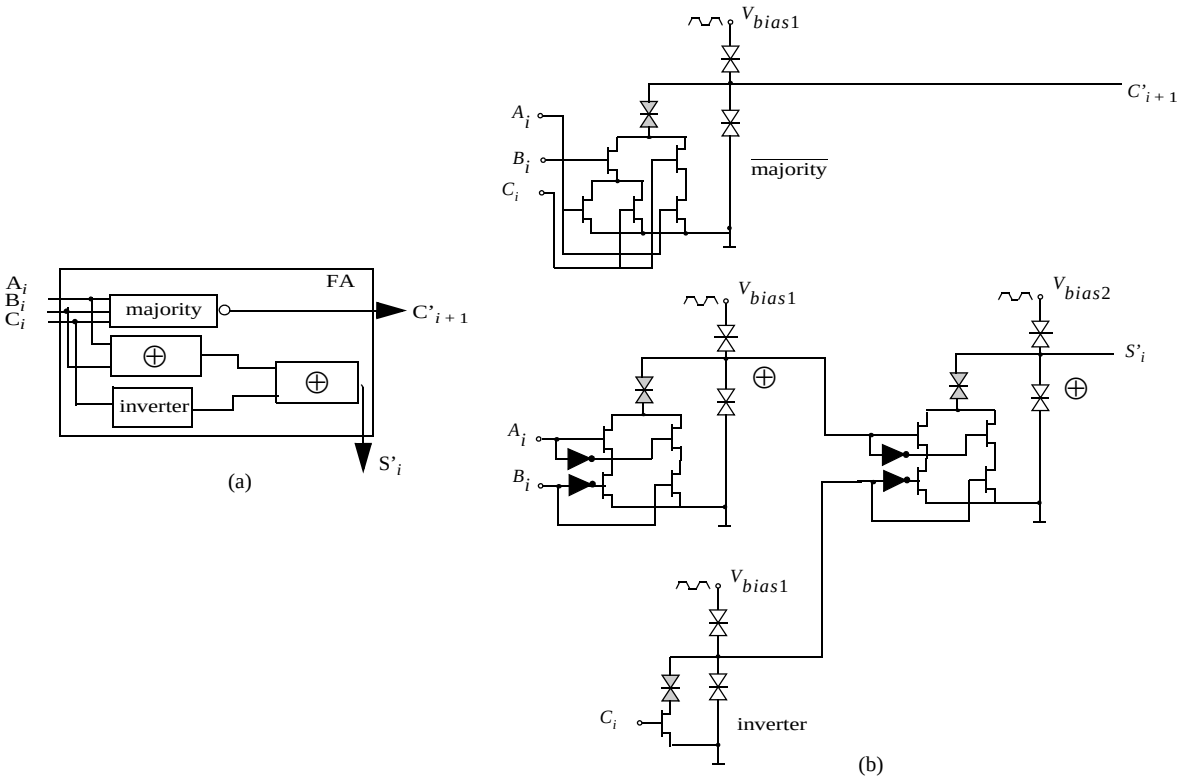

A_i
B_i
C_i
FA
majority
inverter
C'_{i+1}
S'_i
(a)
V_bias1
V_bias2
majority
S'_i
inverter
(b)

Figure 9.

Table I

Fan-in	**Positive weights** Function	Fmax(GHz)	**Negative weights** Function	Fmax(GHz)
2	[1 1; 2]	1.51	[-1 -1; -1]	7
4	[1 1 1 1; 4]	0.77	[-1 -1 -1 -1; -3]	4.16
6	[1 1 1 1 1 1; 6]	0.43	[-1 -1 -1 -1 -1 -1 ; -5]	2.86

Table II

	gates	Device count	F_{max}(GHz)	P@Fmax (mW)	PDP@Fmax (pJ)	P@1.33GHz (mW)
Reference	TG	584	0.77	19.22	24.99	--
Adder_1	TG	584	1.67	11.90	7.13	11.82
Adder_2	TG &MTTG	599	1.89	16.82	8.90	15.43
Adder_3	GTG	605	3.13	15.20	4.86	11.47