Domino inspired MOBILE networks

Juan Núñez, María J. Avedillo and José M. Quintana

MOBILE networks can be operated in a gate-level pipelined fashion allowing high throught-output. If MOBILE gates are directly chained, a four-phase clock scheme is requiered. A single phase scheme has been recently reported that alternates rising and falling edge triggered MOBILE gates. This paper proposes and validates a novel two-phase interconnection scheme resembling conventional domino pipelines. It exhibits advantages in terms of speed with respect to both four-phase and single-phase interconnections schemes. In adition, the new architecture improves logic flexibility regarding domino pipeline counterpart since inverting and non-inverting stages can be interspersed.

Introduction: Resonant tunnelling diodes (RTDs) are considered today as one of the most mature types of quantum-effect devices, already operating at room temperature, and being promising candidates for future nanoscale integration. RTDs exhibit a negative differential resistance (NDR) region in their current-voltage characteristics, which can be exploited to significantly increase the functionality implemented by a single gate in comparison to MOS and bipolar technologies [1]. Circuits taking advantage of the NDR region have been reported, which cover different applications (memories, logic, oscillators, A/D converters, ...) and with different goals (high speed, low power, ...).

Logic circuit applications of RTDs are mainly based on the MOnostable-BIstable Logic Element (MOBILE) [2] which exploits the negative differential resistance of their *I-V* characteristic (Fig. 1a). The MOBILE in Fig. 1b is an edge-triggered current controlled gate which consists of two RTDs connected in series and driven by a switching bias voltage, V_{CK}. When V_{CK} is low, both RTDs are in the on-state and the

circuit is monostable. Increasing to an appropriate maximum value ensures that only the device with the lowest peak current switches from the on-state to the off-state. Output is high if the driver RTD switches and it is low if the load does. Logic functionality can be achieved if the peak current of one of the RTDs is controlled by an input. In the configuration of the rising edge-triggered inverter MOBILE shown in Fig. 1c, the peak current of the driver RTD can be modulated using the external input signals. RTD peak currents are selected such that the value of the output depends on whether the network transistor evaluates to “1” or to “0”.

Rising (falling) edge-triggered MOBILE logic gates evaluate the inputs with the rising (falling) edge of the bias voltage and hold the logic level of the output while the bias voltage is high (low), even though the inputs change (self-latching operation). The output returns to zero (to one) with the falling (rising) edge of the clock until the next evaluation. The self-latching operation allows the implementation of gate-level pipelined architectures without extra memory elements [1]. Conventionally, a four phase clock scheme is applied to operate MOBILE networks. Four clock signals are enough, since the first phase can be used for the fifth level and so on. These signals, with restrictive constraints between rising and falling times and the delays between two consecutives signals, must be distributed for a correct operation of the MOBILE network.

In order to increase the robustness, it is desirable to replace the four-phase clock scheme by a simpler one. In this sense, recently a single clock phase scheme [3] has been proposed which alternates rising and falling edge-triggered stages. However, transistor network implementing functionality in falling edge triggered MOBILE gates is made of p-type transistors, unlike rising edge triggered MOBILE that uses n-type transistors. This translates in larger gate widths and so larger parasitic degrading circuit performance.

Domino pipeline networks. Many high performance digital systems are implemented with dynamic domino logic. Domino circuits are operated in a pipelined fashion with a multi-phase clock scheme. For very high performance applications targeting very high through-output rates, two complementary overlapped clock signals are used.

In spite of their speed advantages, it is well know that domino circuits exhibit a functional limitation such that only non inverting blocks can be chained (a static inverter is added between each two dynamic stages to guarantee that all inputs to the next logic block are set to 0 after the pre-charge period). However, there are many situations where inverting logic needs to be used in conjunction with non inverting logic. Different solutions have been proposed to overcome this limitation including: 1) dual-rail domino circuits which almost doubles the number of transistor compared to single-rail domino circuits, doubling power and in many cases decreasing circuit speed; 2) Logic redesign of the target gate network in order to push inverters towards the inputs of the domino logic section and which in same cases requires replicating parts of the circuit, increasing as well, complexity and power; 3) Modifying gate topology to separately control evaluation and precharge domino operation modes. In general this is accompanied by extra clock phases which make distribution harder.

Two-phase MOBILE Networks: Table 1 summarizes characteristics of the two MOBILE clock schemes previously described. An alternative solution consists of the design of networks of only positive edge triggered MOBILE gates operated with a two phase clock scheme like domino circuits. There are clear advantages of the proposed two-phase scheme over the one-phase solution since worse evaluation time is larger for the second one as it uses falling edge gates with PMOS functional networks. In addition to the advantages associated to a simpler clock distribution network, two-phase exhibits higher through-output than the four-phase one.

Moreover, the limitation of only non-inverting stages of domino is avoided due to the inherent self-latching property of MOBILE operating principle. Evaluation is carried out with the positive edge. Thus, for the high level of clock signal, previous output stage can be logic zero or logic one (unlike domino). In other words, either the MOBILE reset condition (logic zero) or its complement can drive next stage after it has evaluated without corrupting the result. In this way, inverting and non-inverting stages are allowed.

Simulation results. We have carried out the design of two gate-level pipeline networks in order to validate proposed interconnection scheme and to show that it overcomes functional limitations of domino dynamic logic. A library of rising-edge triggered MOBILE logic gates has been designed, from which proposed pipeline networks are built up. This library has been implemented with MOS-NDR devices (circuit made up of transistors that emulate the RTD *I-V* characteristic) and the MOBILE gate topology from [4] in a 1.2V 130nm CMOS commercial technology. In order to obtain more accurate results, parasitic extracted versions of the circuits have been considered and representative corners analyses (including variations of the transistors models, temperature and bias voltage) have been performed.

In a first experiment, the operation of a chain of ten MOBILE inverters has been evaluated. Inverting (direct connection to the next stage) and non-inverting (loaded with a static CMOS inverter) stages, with fan-out 5, have been interspersed. Fig. 2 shows corners analysis (@1GHz) waveforms corresponding to the clock signal from which both clock phases are obtained (with a two-phase clock generation circuit which has been also designed and included in simulations), the input and the output. Note that the output switches five clock cycles after each change of the input is captured.

The second experiment deals with the design of a logarithmic binary carry-merge adder. Unlike conventional CMOS domino topologies, in which a static inverter is

placed between dynamic stages, reported implementations of such adders [5] embed into the static gate part of the logic functionality of the next dynamic gate (compound domino). Fig. 3a depicts a pipeline realization of this architecture, in which each pipeline stage consists of a dynamic and a static gate (i.e. CM1 and CM2). Note that if a dynamic gate is clocked by $V_{CK,1}$, the next one uses $V_{CK,2}$ and so. Fig. 3b shows the proposed MOBILE counterpart of Fig. 3a. Every gate (dynamic or static) in Fig 3a is now a MOBILE gate and so a pipeline stage. That is, the greater logic flexibility (inverting and non-inverting gates can be interconnected) of this architecture translates in finer gate-level pipelined networks. The proposed interconnection scheme has been fully verified @1GHz (including corners analysis) through the design of an 8 bits Kogge-Stone adder.

Conclusions: A novel domino-inspired pipeline interconnection scheme based on MOBILE has been proposed. Unlike conventional CMOS domino architectures, it is not necessary to intersperse static gates between dynamic stages. This leads to advantages in terms of logic flexibility and a better gate-level pipeline performance. The correct operation of two key representative networks, implemented in the proposed design style, has been verified from corners simulations of their extracted circuits.

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References

1 MAZUMDER, P. et al., “Digital circuit applications of resonant tunneling devices”, *Proc. IEEE*, **86**, Apr. 1998, pp. 664-686.

2 AKEYOSHI, T., et al., “Weighted sum threshold logic operation of MOBILE’s (Monostable Bistable Logic Element) using resonant-tunnelling transistors”, *IEEE Electron Device Lett.*, **14**, pp. 475-477, Oct. 1993.

3 NÚÑEZ, J., et al., “Simplified single-phase clock scheme for MOBILE networks”, *IET Electronics Letters*, **47**, (11), pp. 648-650, 2011.

4 NÚÑEZ, J., et al., “Efficient Realisation of MOS-NDR Threshold Logic Gates”, *IET Electronics Letters*, **45**, (23), pp. 1158-1160, 2009.

5 MATHEW, S.K., et al., “Sub-500-ps 64-b ALUs in 0.18-µm SOI/Bulk CMOS: Design and Scaling Trends”. IEEE Journal of Solid State Circuits, **36**, (11), pp. 1636-1646, 2001.

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Table captions

Table 1 Summary of properties of different MOBILE clock schemes. $T_{EVAL,R}$ ($T_{EVAL,F}$) is the evaluation times of the rising (falling) slowest gate in network, respectively.

Figure captions

Fig. 1 (a) RTD current-voltage characteristic and symbol. (b) MOBILE. (c) Rising edge-triggered MOBILE gate.

Fig. 2 Interconnection of MOBILE inverters: corners analyses simulation results @1GHz.

Fig. 3 Kogge-Stone adder: block diagram of the generation of the carry-merge branch associated to bit *i*. (a) Domino CMOS implementation. (b) Proposed MOBILE pipeline architecture.

Table 1

	1 phase	**4 phases**	**2 phases (proposed)**
Building blocks	*Rising & Falling*	*Rising*	*Rising*
Clock cycle	$2 \cdot T_{EVAL,F}$	$4 \cdot T_{EVAL,R}$	$2 \cdot T_{EVAL,R}$
Latency (per network stage)	$T_{EVAL,F}$	$T_{EVAL,R}$	$T_{EVAL,R}$
Through-output	$1/(2 \cdot T_{EVAL,F})$	$1/(4 \cdot T_{EVAL,R})$	$1/(2 \cdot T_{EVAL,R})$

Figure 1

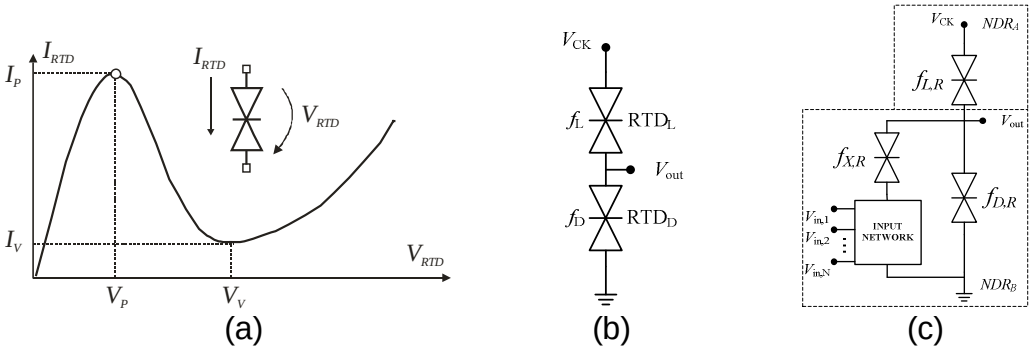

I_{RTD}
I_P
I_V
V_P
V_V
V_{RTD}
I_{RTD}
V_{RTD}
(a)
V_{CK}
f_L
RTD_L
V_{out}
f_D
RTD_D
(b)
V_{CK}
NDR_A
$f_{L,R}$
V_{out}
$f_{X,R}$
$f_{D,R}$
$V_{in,1}$
$V_{in,2}$
$V_{in,N}$
INPUT NETWORK
NDR_B
(c)

Figure 2

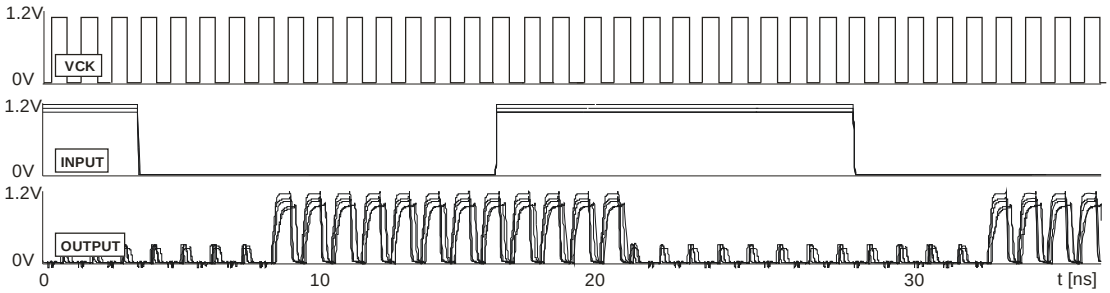
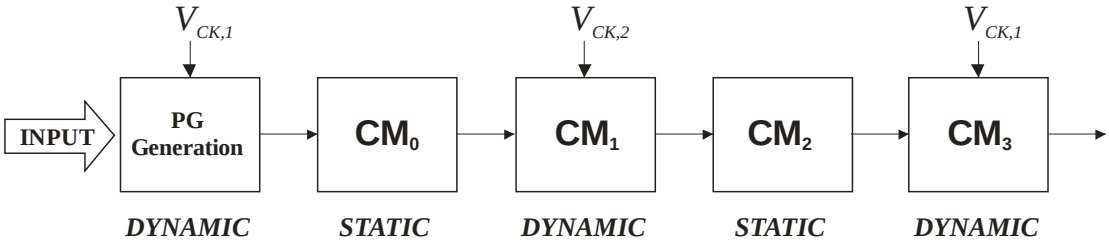
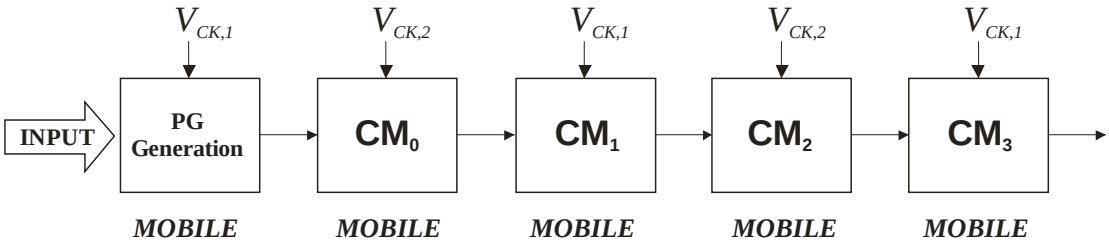


Figure 3


$V_{CK,1}$
$V_{CK,2}$
$V_{CK,1}$
INPUT
PG Generation
CM0
CM1
CM2
CM3
DYNAMIC
STATIC
DYNAMIC
STATIC
DYNAMIC

(a)


$V_{CK,1}$
$V_{CK,2}$
$V_{CK,1}$
$V_{CK,2}$
$V_{CK,1}$
INPUT
PG Generation
CM0
CM1
CM2
CM3
MOBILE
MOBILE
MOBILE
MOBILE
MOBILE

(b)