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Electrical Properties of Atomic Layer Deposition HfO_2 and HfO_xN_y on Si Substrates with Various Crystal Orientations

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The use of high-*k* gate oxide on Si substrates with alternative orientations is expected to contribute for the fabrication of high mobility devices. In this paper, the interfacial and electrical properties of the plasma enhanced atomic layer deposition (PE–ALD) HfO_2 and HfO_xN_y gate oxides on Si substrates with three different crystal orientations, (001), (011), and (111), were comparatively studied. While PE–ALD HfO_2 films were prepared using oxygen plasma as a reactant, PE-ALD HfO_xN_y films were prepared by in situ nitridation using oxygen/nitrogen mixture plasma. For all crystal orientations, in situ nitridation using oxygen/nitrogen mixture plasma improved electrical properties producing lower leakage currents and smaller equivalent oxide thickness values. Both HfO_2 and HfO_xN_y films have shown the lowest leakage current and interface state density on Si(001), whereas the poorest electrical properties were obtained on Si(111). The results are discussed based on the experimental results obtained from various analytical techniques, including *I-V*, *C-V*, conductance methods, and X-ray photoelectron spectroscopy.
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For the fabrication of high-speed devices, various mobility enhancement techniques are attracting great interests. One of the promising ways to achieve high mobility is the use of Si substrates with high index orientation, which results in increased carrier mobility compared to the Si(001) substrate. For example, hybrid orientation technology has been proposed to produce high-mobility complementary metal-oxide-semiconductor (CMOS) devices.[1] For the full implementation of this technology as well as the nonplanar devices such as surround gate transistors, the interface between gate oxide and substrates with various orientations should be well understood. Generally, it has been reported that the interface defect densities are higher for high index Si substrates, mainly due to the larger number of dangling bonds.[2] Also, the interface trap density of $Si–SiO_2$ is critically dependent on the surface orientations.[3,4] However, the interface properties of high-*k* oxides on Si substrates with various orientation have rarely been studied. Only recently, the mobility enhancement effects of *p*-FETs with HfO_2 gate oxides on high index orientation Si substrates were reported to be similar to those with thermal oxides.[5-7]

Meanwhile, as the physical thickness of high-*k* gate oxides reduces, a number of fundamental problems arise, such as the increase of leakage current, the degradation of dielectric reliability and channel mobility, and low thermal stability of high-*k* thin films.[8] The incorporation of nitrogen into high-*k* gate oxides has been considered as a promising way to alleviate these concerns. The incorporated nitrogen atoms reduce the leakage currents by passivating oxygen vacancy states and enhancing structural stability. Recently, we reported that in situ nitridation during plasma enhanced atomic layer deposition (PE–ALD) using nitrogen containing reactant (oxygen/nitrogen mixture plasma) produces HfO_xN_y films with significantly improved electrical properties.[9] In this paper, we have comparatively studied the interfacial and electrical properties of PE–ALD HfO_2 and HfO_xN_y thin films on Si substrates with three different orientations, Si(001), Si(011), and Si(111) substrates. Especially, we studied the effects of substrate orientation on the leakage current and reliability of high-*k* gate oxide, which has rarely been reported in spite of its importance for future microelectronic industry. The nitrogen incorporation and binding structure were studied using X-ray photoelectron spectroscopy (XPS). The interfacial and electrical properties of PE–ALD HfO_2 and HfO_xN_y were studied using various electrical measurement techniques including capacitance-voltage (*C-V*), current-voltage (*I-V*), and voltage stress test.

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Experimental

A homemade remote PE–ALD system was used in this study. Tetrakis(dimethylamino)hafnium (TDMAH) was used as a Hf precursor. The TDMAH was contained in a bubbler, and its temperature was kept at room temperature. The flows of reactant gases (oxygen and nitrogen) and purging gas (Ar) were controlled by mass flow controller (MFC). The oxygen and nitrogen gases were flown into an rf plasma source, which consists of a quartz tube wrapped with a multiple-turn coil set at 13.56 MHz providing a power level of up to 600 W. For the current experiments, the flow of the oxygen, controlled by MFC, was 20 sccm, and the plasma power was 300 W. The chamber was purged by 75 sccm Ar gas between precursor and reactant exposure step. Typical HfO_2 or HfO_xN_y ALD sequence was composed of TDMAH exposure time of 1.5 s, plasma reaction time of 3 s, and purging time of 5 s between those. For in situ nitridation, the N/O flow ratio was fixed at 2. The growth temperature was 250°C and the growth rates (1.3 Å/cycle) were determined by ellipsometry. The stoichiometry, impurity contents, and chemical binding structures were analyzed by XPS (Escalab 220IXL).

The films were grown on Si(001), Si(011), and Si(111) substrates at the same growth conditions. The total number of deposition cycles were 30, resulting in ~4 nm thick films. For electrical measurements, the films were deposited on p-type (boron doped, 5×10^{14} cm^{-3}) Si substrates, which were cleaned at 70°C for 10 min in RCA solution [1:1:5(v/v/v) $NH_4OH/H_2O_2/H_2O$] following dipping in buffered oxide enchant solution for 30 s to remove native oxide. Next, to reduce the trap charges, postdeposition annealing was carried out at 400°C for 10 min in an oxygen environment. For the fabrication of MOS capacitors, Pt was used as a gate electrode, which was deposited by dc magnetron sputtering in 5 mTorr Ar with 18 W dc power through patterned shadow mask. After Pt electrode deposition, forming gas annealing was carried out at 400°C for 30 min in H_2 5%–N_2 95%. Au film deposited by thermal evaporation was used as a back contact. *C-V* and *I-V* characteristics were determined by using a Keithley 4200 semiconductor parameter analyzer with an HP4284 LCR meter. The voltage applied to capacitors were swept from inversion (+2.5 V) to accumulation (−2.5 V) and back to check the amount of *C-V* hysteresis. The midgap interface state density (D_{it}) was determined by a conductance method carried out at various frequencies from 1 kHz to 1 MHz. To determine the dielectric reliability, the flatband voltage shifts were measured after constant voltage stress (−3 V) for 1, 3 5, and 10 min.

Results

Figure 1 shows N 1s and Si 2p XPS spectra of as-deposited PE–ALD HfO_2 using oxygen plasma and oxygen/nitrogen mixture

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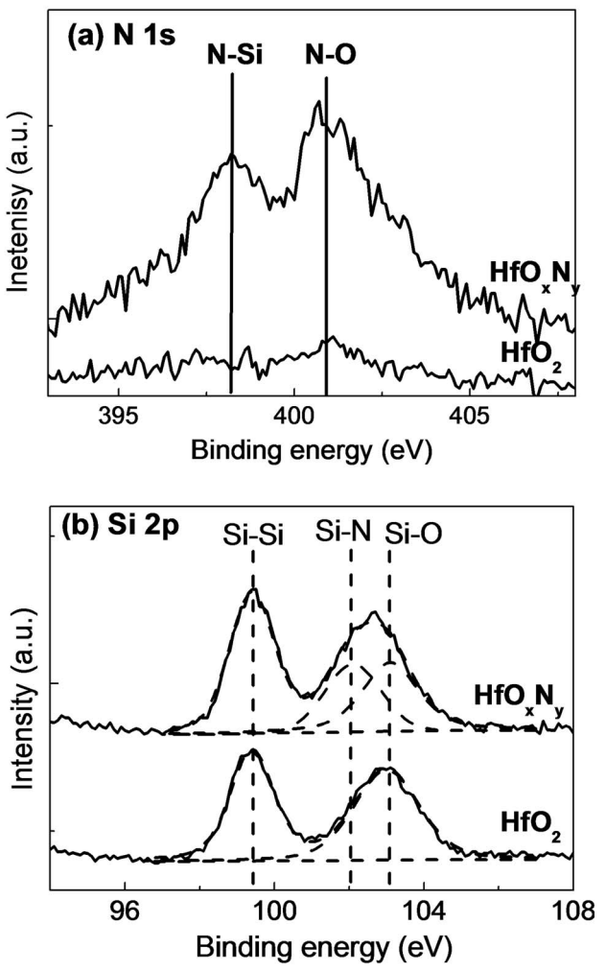

Figure 1. (a) N 1s and (b) Si 2p XPS spectra of as-deposited HfO_2 and HfO_xN_y.

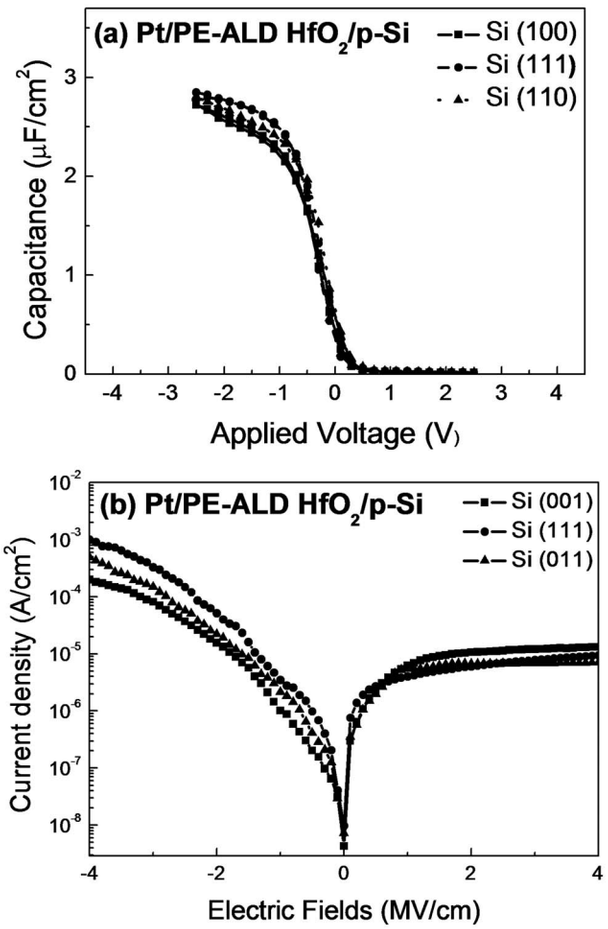

Figure 2. (a) Capacitance-voltage and (b) current-voltage curves of MOS capacitors with HfO_2 as a gate insulator.

plasma on Si(001) substrate. While the nitrogen peak is below the detection limit for PE–ALD HfO_2 with oxygen plasma, clear nitrogen peak related features (N–Si at 398.0 eV and N–O at 401.5 eV) are seen for the film deposited using nitrogen/oxygen plasma (Fig. 1a). The nitrogen content in the film deposited using nitrogen/oxygen plasma was determined to be 4.5 atom % based on the nitrogen/oxygen peak intensity ratio.[10]

Thus, nitrogen is easily incorporated during the PE–ALD HfO_2 by nitrogen addition to oxygen plasma, producing a PE–ALD HfO_xN_y film. The modulation of nitrogen concentrations was feasible by changing the N/O flow ratio. The Si 2p spectrum is composed of two peaks, one peak due to Si–Si bonding at 99.3 eV and the other peak at ~103.0 eV (Fig. 1b). While the peak at 103.3 eV for PE–ALD HfO_2 is due to Si–O bonds, a new peak due to the Si–N bonding is found by deconvolution at 102.4 eV for PE–ALD HfO_xN_y. The Si–O bonding for PE–ALD HfO_2 is attributed to the interlayer formed during initial deposition of HfO_2. Meanwhile, the existence of Si–N bonds coexisting with Si–O indicates that the interlayer of PE–ALD HfO_xN_y/Si is composed of oxynitride formed by oxygen and nitrogen mixture plasma. Even with these differences, the growth rates of PE–ALD HfO_2 and HfO_xN_y were almost the same as the 1.3 Å/cycle. Also, x-ray diffraction analysis has shown that all as-deposited PE–ALD HfO_2 and HfO_xN_y films are amorphous at low growth temperature used in this study (250°C) on Si(001), Si(011), and Si(111).

Figure 2a shows the *C-V* curves of MOS capacitors, Pt/PE–ALD HfO_2/Si, made on Si substrates with three different orientations. For all three samples, the V_{FB} values were almost the same (0.08 V), but the hysteresis values were slightly different. From the hysteresis, the trapped oxide charges N_{ot} can be calculated by[11]

$$\Delta V_{FB} = \frac{N_{ot} q A}{C_{acc}} \quad [1]$$

where ΔV_{FB} is the hysteresis width, C_{acc} is the accumulation capacitance, q is the electron charge (1.60218×10^{-19} C), and A is the electrode area. The measured trapped oxide charges were 1.12×10^{12} cm^{-2} for Si(001), 1.80×10^{12} cm^{-2} for Si(111), and 1.40×10^{12} cm^{-2} for Si(011). The equivalent oxide thickness (EOT) values were obtained from the capacitance values at an accumulation condition. To overcome the measurement problems associated with series resistance and leakage currents, the EOT values were extracted using a resistance correction procedure.[12] For this, the capacitances were measured at two different measurement frequencies (10 and 100 kHz) and the actual frequency-independent capacitances were obtained using

$$C = \frac{f_1^2 C_1 (1 + D_1^2) - f_2^2 C_2 (1 + D_2^2)}{f_1^2 - f_2^2} \quad [2]$$

where D_i is a dissipation defined by $G_i/\omega C_i$ measured at frequency f_i. G_i is a conductance at frequency f_i and ω is angular velocity ($=2\pi f_i$). To determine interface state density (D_{it}), the conductance

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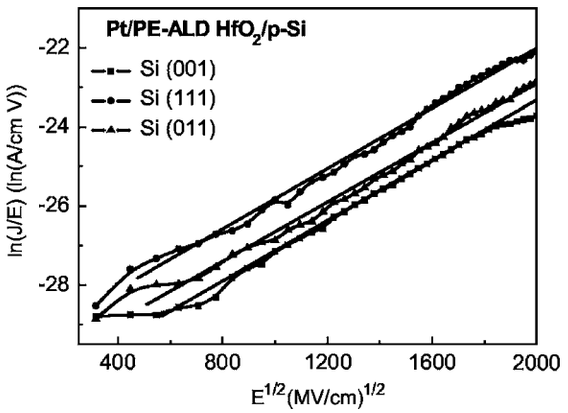

Figure 3. The $\ln(J/E)$ vs $E^{1/2}$ for the MOS capacitors shown. The straight line indicates conduction occurs through the PF mechanism.

was measured at various frequencies from 1 kHz to 1 MHz. From the measured conductance, the midgap interface state density was obtained from[13]

$$D_{it} = \left(\frac{G}{\omega}\right)_{max} [qf_D(\sigma_s)]^{-1} \approx \frac{2.5}{q}\left(\frac{G}{\omega}\right)_{max} \quad [3]$$

where $f_D(\sigma_s)$ is the universal function of standard deviation of band banding σ_s. The EOT values of these three samples were almost the same [Si(001):1.20 nm, Si(111):1.15 nm, Si(011):1.18 nm]. The relative independence of EOT values of HfO_2 on surface orientation agrees with a previous report on Si(001) and Si(111).[7] However, the interface state density (D_{it}) of HfO_2 on Si(111) (5×10^{11} cm^{-2} eV^{-1}) was ~3.5 times higher than that on Si(001) and 2 times higher than that on Si(011) substrates. This result is analogous to the results for thermal SiO_2 on Si substrates with different orientations.[3,4] In a previous study, it was shown that D_{it} is strongly correlated with excess Si ions at the interface, which is an inherent property of Si–SiO_2 interface depending on Si orientations, and not related to contaminants or oxide thickness.[14] The *I-V* curves in Fig. 2b show that the leakage currents of PE–ALD HfO_2 on Si(001) at −1 MV/cm is 1.0×10^{-6} A/cm^2, which is ~2 times lower than that on Si(011) and 3.5 times lower than that on Si(111).

The Poole–Frenkel (PF) hopping current is given by[15]

$$J_{PF} \approx AE \exp\left\{-\frac{q[\phi_t - \sqrt{qE/(\pi\varepsilon_i)}]}{k_B T}\right\} \quad [4]$$

where ϕ_t is the energy level of a trap with respect to the conduction band of the insulator, E is the effective electric field across the insulator, and ε_i is the high-frequency dielectric constant. Also, $A = q^3/(8\pi h m^*_{ox} \phi_B)$, where h is Planck's constant, ϕ_B is the barrier height at the interface of the injecting electrode and the oxide film, and m^*_{ox} is the ratio of the effective mass of the electron in the oxide to that in vacuum. Figure 3 shows that the $\ln(J/E)$ vs $E^{1/2}$ has a linear relation indicating that the leakage mechanism of the current MOS capacitors made with PE–ALD HfO_2 is dominated by PF hopping conduction for about ~0.5 V to −3.3 V of applied voltages.

Figure 4a shows *C-V* curves of Pt/PE–ALD HfO_xN_y/Si with different orientations. The addition of nitrogen significantly alters the characteristics. First, the EOT values of all three samples are reduced to ~0.95 to 1.00 nm. The reduction of EOT by nitrogen incorporation is a general observation, which agrees with a previous report showing that 5% N incorporation in HfO_2 films increases the dielectric constant by ~17%.[16] D_{it} of HfO_xN_y was the lowest on Si(001) (2.0×10^{11} cm^{-2} eV^{-1}), which is three times lower than that on Si(111). The hysteresis values of these films are significantly increased compared to those of HfO_2 by ~0.17 V. From the hysteresis, the trapped oxide charges were calculated using Eq. 1; 3.40×10^{12} cm^{-2} for Si(001), 4.25×10^{12} cm^{-2} for Si(111), and 3.90×10^{12} cm^{-2} for Si(011). The *I-V* characteristics are shown in Fig. 4b. The leakage current density at −1 MV/cm of PE–ALD HfO_xN_y on Si(001) is ten times lower than that of HfO_2 and six times lower than that of HfO_xN_y on Si(111). The key electrical properties described thus far are summarized in Table I.

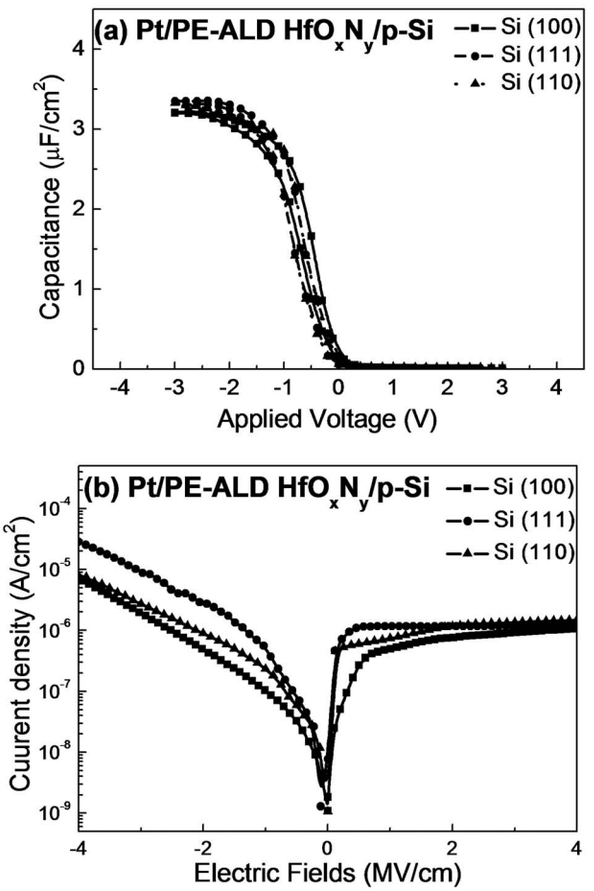

Figure 4. (a) Capacitance-voltage and (b) current-voltage curves of MOS capacitors with HfO_xN_y as a gate insulator.

To determine the dielectric reliability of PE–ALD HfO_2 and HfO_xN_y on various substrates, the constant voltage stress (CVS) measurements were carried out. Because charge trapping by electrical stress can induce oxide degradation,[17] *C-V* measurement after constant voltage stress is a useful tool to determine the reliability of gate oxide. The gate injection (negative bias applied in gate), which

Table I. Key electrical properties of Pt/ALD HfO_2 and HfO_xN_y/*p*-Si MOS capacitor.

		EOT (nm)	D_{it} (cm^{-2} eV^{-1})	Trapped oxide charges (cm^{-2})	Leakage currents (A/cm^2)
HfO_2	Si(001)	1.20	1.1×10^{11}	1.12×10^{12}	1.0×10^{-6}
	Si(111)	1.15	5.0×10^{11}	1.80×10^{12}	3.5×10^{-6}
	Si(011)	1.18	2.5×10^{11}	1.40×10^{12}	2.5×10^{-6}
HfO_xN_y	Si(001)	1.00	2.0×10^{11}	3.40×10^{12}	1.0×10^{-7}
	Si(111)	0.95	5.8×10^{11}	4.25×10^{12}	5.7×10^{-7}
	Si(011)	0.95	4.3×10^{11}	3.90×10^{12}	2.3×10^{-7}

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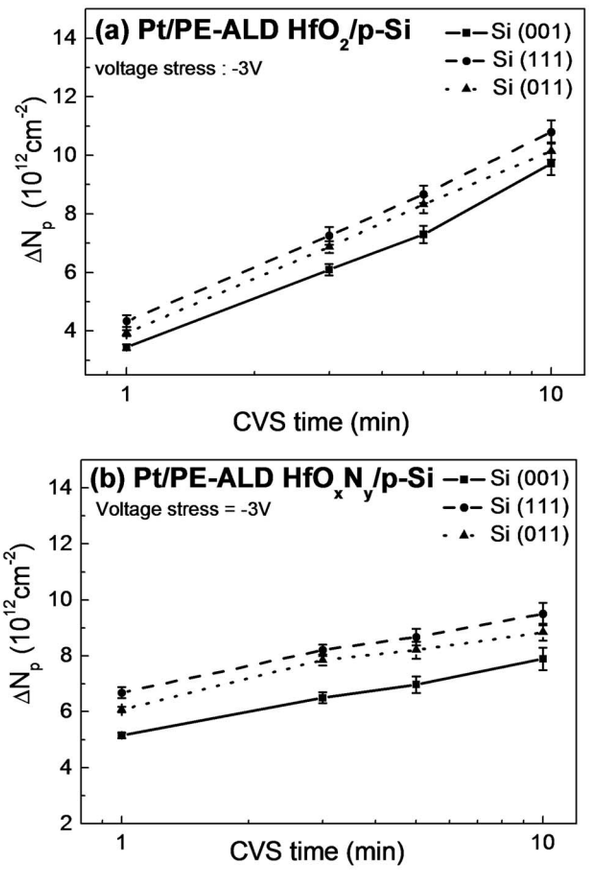

Figure 5. Trapped positive charge density (ΔN_p) data of (a) HfO_2 and (b) HfO_xN_y after current voltage stress (−3 V) at room temperature.

induces the positive charge and hole trapping near the interface, is especially important for determining the reliability of ultrathin films.[18] Thus, negative voltage (−3 V) was applied for our measurements. After negative voltage stress, the *C-V* curves were shifted to negative direction due to the generation of positive trap charges. The observed V_{FB} shift (ΔV_{FB}) can be converted to trapped positive charge density (ΔN_p) using the relation

$$\Delta N_p = \frac{-C_{ox}\Delta V_{FB}}{q} \quad [5]$$

Figures 5a and b show the ΔN_p as a function of stress time for PE–ALD HfO_2 and HfO_xN_y on Si substrates with various orientations, respectively. The results show that the ΔN_p values are Si(001) < Si(011) < Si(111) for both PE–ALD HfO_2 and HfO_xN_y. It should also be noted that the ΔN_p enhancement by a stress time of PE–ALD HfO_xN_y, represented by the slope of plots, is smaller than that of HfO_2, indicating the better reliability of HfO_xN_y than HfO_2, irrespective of Si substrate orientations. For example, ΔN_p of HfO_xN_y on Si(001) after 10 min stress is 0.8×10^{13} cm^{-2}, which is smaller than that of HfO_2 (1.0×10^{13} cm^{-2}). This means that incorporated N in dielectric layer can reduce charge trap generation leading to enhancement in the dielectric reliability. Both figures show ΔN_p vs CVS time curves are well fitted by a logarithmic relation. This implies that the V_{FB} shift (ΔV_{FB}) is well explained by charge trapping kinetics during electrical stresses.[19]

Discussions

The experimental results show that the in situ nitridation produces better performance in terms of EOT, leakage currents, and reliability, irrespective of substrate orientations. For both PE–ALD HfO_2 and HfO_xN_y, however, the high index substrates, Si(111) or Si(011), has larger interface density and higher leakage currents than Si(001). The larger interface state of high index plane is probably due to a large number of interface dangling bonds. Meanwhile, the origin of larger leakage for high index substrate is not obvious. Since our *C-V* measurements indicate that the capacitance values are almost the same for each substrate, there should be no big difference in total or interlayer thickness. In fact, the growth rates of HfO_2 or HfO_xN_y were independent of substrate orientations when we measured them by ellipsometry for relatively thick oxides. Also, it was reported that the interlayer thickness of ALD HfO_2 is independent of substrate orientations.[20] Thus, we can rule out the effects of thickness.

The next possibility is the differences in band offset between HfO_2 and Si substrates, depending on the substrate orientations. Although the band offset is not the same as barrier height, which directly determines the tunneling currents, it is strongly correlated with barrier heights. Therefore, low valence band offset corresponds to low barrier heights, and the possibility of different hole conduction caused by barrier height change with Si orientations can be considered. In previous studies on the interfaces between SiO_2 and Si, the valence band offset of Si(001) is 0.19 eV larger than Si(111) and 0.09 eV larger than Si(011).[21,22] But this small difference in valence band offset cannot be the main reason for the observed leakage current difference because the valence band offsets (3.40 eV) are generally higher than conduction band offset (2.40 eV) for HfO_2 on Si.[23] Because of the larger valence band offset than conduction band offset, the electron conduction from the gate was calculated to be about six orders of magnitude higher than the hole conduction from the substrate.

Thus, we propose that the large leakage currents for high index plane are due to the large trap densities, as observed for *C-V* measurements (Fig. 2 and 4). Previously, the leakage currents caused by interface states have rarely been studied. In a previous study, the interface state-assisted tunneling is proposed to be dominated only at a very low voltage region because the interface states are generally located two-dimensionally at oxide–Si interface.[24] Recently, the measurements using depth profiling charge pumping methods have shown that the "near interface traps" (border traps) exist throughout the interface layer.[25,26] The density of these near interface traps increases with the distance from the interface up to ~1 nm and decreases at larger distances. We propose that the flow of electrons becomes more feasible through trap-assisted tunneling by these near interface traps. Because the number of these traps is higher for high-index substrates, the leakage becomes larger than Si(001). Thus, the current results indicate that the role of interface state or near interface trap at the interfacial layer, which is dependent on the substrate orientations, is important for electrical properties such as leakage current and reliability.

Conclusion

In this study, we compared the electrical and interfacial properties of PE–ALD HfO_2 and HfO_xN_y on Si substrates with various orientations. The in situ nitridation improved the electrical properties, including leakage current and dielectric reliability for both HfO_2 and HfO_xN_y. And the defect density, including interface state and trapped oxide charges, are Si(001) < Si(011) < Si(111) in HfO_2 and HfO_xN_y. These defect densities affect the dielectric reliability and leakage currents. On the basis of these results, the large leakage currents for high-*k* gate oxide on high-index plane were attributed to the trap-assisted tunneling mechanism, which is determined by the number of near interface traps.

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Acknowledgments

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