Series Voltage Regulator for Radial DC-microgrid

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Abstract—The concept of a novel Series Voltage Regulator (SVR) for controlling dc bus voltage of a radial dc microgrid is presented in this paper. The proposed SVR uses a dual active bridge dc-dc converter followed by a full-bridge dc-dc converter. It injects dynamic voltage in series with the dc grid to compensate resistive drop over the network. As a result, the voltage level at the different points of the grid becomes independent of load variation and stays within the specified limit. Note that the required power rating of the SVR is very low (say 2.7%) compared to the load demand considering 5% voltage regulation. In this work, the voltage regulator is connected at the mid-point of the grid, but it may be connected in some other locations to get optimal rating of the same. The proposed configuration is simulated in MATLAB/SIMULINK at 380V level to check the dynamic performance under various operating conditions. A scaled down version (at 30V level) of the proposed system is developed in the laboratory to experimentally validate the concept. The results show the effectiveness of such voltage regulator for radial dc microgrid, especially under critical load condition.

Index Terms—DC microgrid, DAB, DC-DC bidirectional converter, Series Voltage Regulator.

NOMENCLATURE

L_d Total leakage inductance referred to primary side
L'_d Total leakage inductance referred to secondary side
V_{tp} Voltage across primary of transformer
V_{ts} Voltage across secondary of transformer
V_{Ld} Voltage across the inductor
I_{Qp} Primary winding reactive current
I_{Qs} Secondary winding reactive current
r_{ij} Transmission line resistance between bus i and bus j
R_{Li} Load resistance connected to bus i
I_{ij} Current from bus i to bus j
V_i Voltage at bus i
D_{Ti} Diode across the switch T_i
C_{Ti} Snubber capacitor across the switch T_i
V_c Control signal for Full bridge dc-dc converter
V_{trip} Peak value of triangular wave form
V_{grid} dc grid voltage at bus-0
M_{iv},M_{id} Scalar constants
Z_{in},Z_o Impedances seen at input and output sides of DAB
M_{in} Coefficient of small signal variation of input current (i.e. $\hat{i}_{in} = M_{in}\hat{i}_{dc1}$)

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I. INTRODUCTION

RECENT developments and trends in the electrical power consumption and generation system clearly indicate an increasing use of dc in end-user equipment. A dc distribution system allows simple integration of renewable energy sources and direct connection of battery banks and Super Capacitors (SC) [1] - [2]. It is well known that the rural electrification through distributed power generation units (e.g. small wind farm, solar park, etc.) is beneficial compared to centralized power generation unit (nuclear, large wind farms, etc.) [3]. So, the concept of dc distribution system consisting of distributed generation (DG) units has been evolving. Note that the DGs are connected to dc microgrid through power electronic converters to control the dc bus voltage. In [4], various control methods are discussed on the coordinated operation of the DGs for a single bus system, which have their own merits and limitations. The droop control is one of the popular methods to achieve constant voltage by means of coordination between parallel converters [5] - [6]. However, it has some limitations; the most important one is the voltage drop across transmission line resistance which causes deterioration of power sharing [7] among the sources. In [8], [9], modified droop control techniques are proposed which utilize dc bus signaling and adaptive adjustment of droop co-efficients. In [10], a three level hierarchical control is proposed where, droop control is present at the inner most layer. In [11], a model predictive control based droop control for current regulation is proposed for dc microgrid.

All aforementioned studies focused only on one bus system where sources and loads are connected at one point. However, a dc distribution system for remote community consists of more number of load buses with significant distance among them. A simple low power dc microgrid is implemented in Neelakantarayanagaddi village of India [12], where the source is connected in one bus and loads are connected at the remaining buses. The power flow is taking place from its source-bus to the end-bus in one direction. Therefore, the voltage levels at different points of the grid are dependent on load power due to voltage drop along the transmission line resistances. The situation gets worse (i.e. bus voltage falls below specified limit) when the load reaches to the critical value and bus under consideration is far away from the generation [13]- [14].

Therefore, voltage regulation in a radial dc grid is essential to meet system specifications. Note that the problem related to voltage regulation is also found in the ac grid. The Dynamic Voltage Restorer (DVR) is one of the products which can provide improved voltage quality in an ac grid [15]. The voltage drop problem in dc grid can be eliminated by placing

the DG in the bus, whose voltage reaches to its lower limit [16]. The DG is supplying part of the load power and hence reduces the voltage drop along the line which improves the bus voltage under consideration. The energy storage system may also be used to address this issue, as described in [17]. Rating of the energy storage under heavy load condition is an important issue which may increase cost of the system.

In this paper, Series Voltage Regulator (SVR) is proposed which dynamically injects voltage in series with the dc microgrid to compensate voltage drop across the line resistance. As a result, the load bus voltage stays within the specified limit and becomes independent of load variation. Note that the power rating of the SVR can be kept at very low value (e.g. 2.7% of the grid power) compared to other approaches.

The high gain dc-dc converter is the building block of SVR. The various high-gain dc-dc converters are reviewed in [18]. Among them, Dual Active Bridge (DAB) is chosen for this application due to isolation between input and output, high efficiency, and moderate power rating. The SVR is formed with a DAB followed by a dc-dc converter. DAB provides unipolar dc voltage with a step-down ratio decided by the transformer. The dc-dc converter (in the second stage) regulates output voltage as per requirement and is capable to change the polarity of the output voltage. Note that the proposed SVR can also support bi-directional power flow through it which is a prerequisite for some particular applications.

This paper is organized in eight sections. Section-I introduces radial type dc microgrid and associated problems with loading. The proposed configuration for voltage drop compensation and optimal placement of SVR are presented in Section-II. Section-III describes the overall control of proposed SVR. The design related issues and operation under steady-state are explained in Section-IV and V, respectively. Section-VI and VII gives the simulation and experimental results under various operating conditions. Finally, Section-VIII concludes the work.

II. PROPOSED CONFIGURATION

A. Connection Diagram

Fig.1 shows the configuration of a typical radial dc microgrid where various sources are connected at bus-0 and loads are connected at remaining buses. This system is widely used due to its simplicity and cost effectiveness [19]. Also, the expansion of load branches is easy for such configuration. The bus voltage variation with loading is the main limitation which is already explained in Section I. The voltage at the buses which are far away from generation (e.g. bus-3 and bus-4 here) may fall below the specified limits due to loading. The proposed SVR need to be connected at the right place such that all node voltages remain within $\pm 5\%$ deviation. The input side of the SVR is connected across the grid with terminals A and B. The output side is connected in series with the grid (in between the bus-2 and bus-3). According to the connection, the output of SVR experiences lower voltage (V_{svro}) associated to line-drop and up to rated line current (I_{svro}), whereas the input of SVR handles rated dc grid voltage (V_1) and lower current (I_{in}).
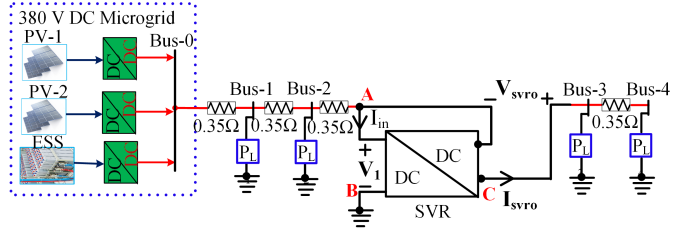

Fig. 1. The dc microgrid with SVR

B. Topology

The proposed topology of SVR is shown in Fig.2. The SVR comprises of a DAB followed by a full-bridge dc-dc converter. The two bridges (primary and secondary) in DAB are operated to generate high-frequency square-wave voltage at the transformer terminals. The phase shift between two square-waves can be adjusted to control power flow from V_1 to V_2 or vice versa. Power flow always happens from the bridge generating leading square-wave to the other bridge [20]. Note that the DAB is operated in power control mode. The output voltage of DAB (V_2) is always maintained to its reference value under the variation of output current (I_{inb}) and input voltage (V_1). The constant output voltage of DAB is connected to the input of the full bridge dc-dc converter. The full bridge is operated in voltage control mode with unipolar modulation [21] to generate an adjustable dc voltage (V_{svro}). So, under steady state, as well as transient conditions, the required amount of voltage with suitable polarity can be added in series with the dc grid. In this proposed configuration, the SVR regulates the voltage at bus-3 by adding controlled series voltage with appropriate polarity.

C. Optimal placement of SVR

In a radial dc microgrid, as shown in Fig.1, the load power is drawn from the source which is concentrated at one point. In this scenario, the voltage drop across the transmission line resistance increases, and hence, the voltage of the buses decreases. The SVR is placed before the bus whose voltage falls below a specified limit, i.e. 5% of Bus-0 voltage. The voltage drops and bus voltages are calculated using the backward/forward sweep method [22]. According to this method, at each iteration, two computational stages are performed, i.e. a backward sweep for current summation and then a forward voltage calculation. For this load flow study, 2.5 kW loads are considered which are connected at each buses (from bus-1 to bus-4 except bus-0) and transmission line resistance between buses are assumed as 0.35 Ω. The voltages of each buses and transmission line drops are calculated without SVR. The bus-voltage vs. bus-number is plotted in Fig.3. It clearly indicates that the bus-3 voltage is less than the 5% of bus-0 voltage. Therefore, the SVR is placed just before bus-3. The uncertainty issues, like load change and change of transmission line resistance may be considered for the optimal placement of SVR. The voltage regulation problem under the expansion of dc microgrid may be addressed by increasing the rating of the SVR or by adding multiple SVR at critical locations in the system.
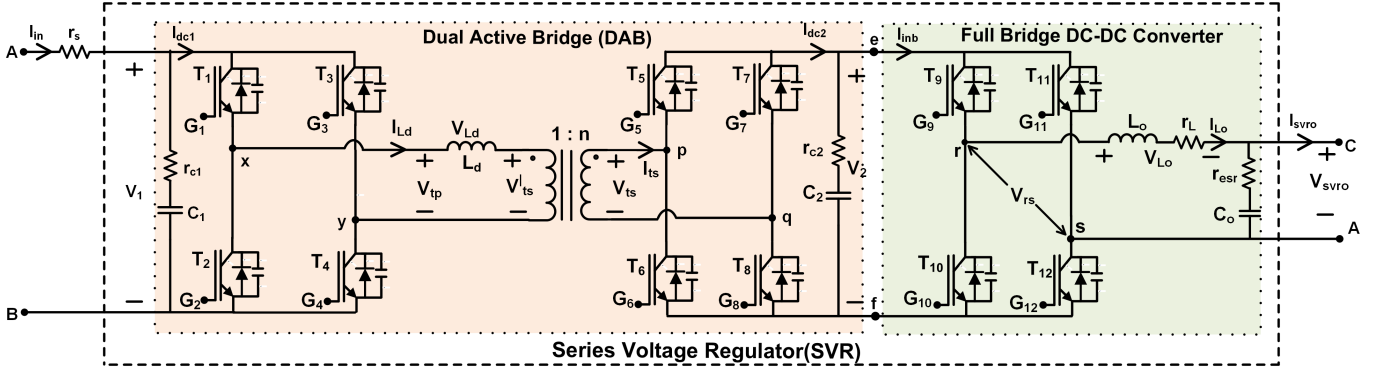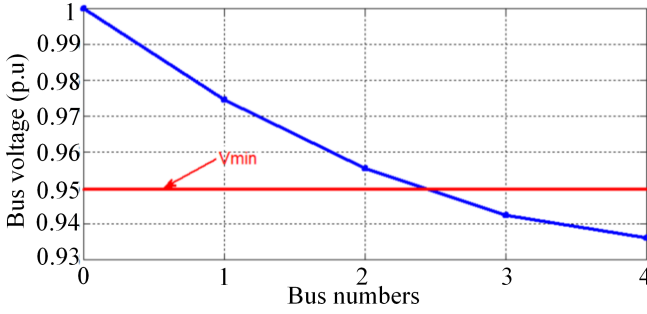
Fig. 2. The Schematic of the SVR

Fig. 3. Voltage at different buses

III. PROPOSED CONTROL SCHEME OF SVR

Fig.4 shows the overall control scheme for SVR. The proposed scheme consists of two control-blocks to ensure bus-3 voltage within a specified limit at different loading conditions. The Block-I performs power flow control and maintains a constant voltage at the output of DAB. The Block-II shows the control for full-bridge dc-dc converter, which is operated in voltage control mode.

A. Power Control

The 1st stage of the SVR, i.e. DAB is operated in power control mode. The control for DAB, as shown in Block-I of Fig.4, consists of two control loops which are outer voltage loop and inner current loop. The main purpose of this control is to maintain required power flow through the SVR keeping the output of DAB (i.e. V_2) constant. The difference between the reference and actual values of V_2 (where $e = V_2^* - V_2$) is fed to a Proportional-Integral (PI) type voltage controller which generates reference (i.e. I_{in}^*) for the inner current loop. The actual input current of the DAB is then compared with reference value and the error is passed to the current controller with transfer function G_{ciin}. Note that only the integral controller is enough for the inner current loop. The inner current loop generates desired phase shift in terms of D (phase-shift = πD. Here D is varying from 0 to 0.5. The control keeps the output voltage of DAB (i.e. V_2) constant irrespective of the variation of load, as well as the input voltage of DAB (i.e, V_1). The gains of the controllers are chosen in

such a way that the bandwidth of the outer voltage loop is 10 times lesser than the inner current loop. The design of various controllers are presented in Section-V.

B. Voltage Control

The control of full-bridge dc-dc converter to adjust output voltage of SVR (V_{svro}) is shown in Fig.4. The voltage drop across the line (up to bus-3) is given as the reference to the controller. The voltage reference is generated through the following equation.

$$V_{svro}^* = V_{grid}^* - V_1. \tag{1}$$

The error is formed in between the reference and actual output voltage (i.e. $e = V_{svro}^* - V_{svro}$) which is fed to a PI controller. The PI controller provides the control signal (i.e., V_c) to generate PWM signals for switches T_9 to T_{12}. The gains of the PI controller are chosen in such a way that the bandwidth of this voltage loop is 10 times lower than switching frequency.

IV. STEADY-STATE ANALYSIS

The operation of DAB and dc-dc converter are analyzed here under steady state condition.

A. Dual Active Bridge (DAB)

A DAB is an isolated bidirectional dc-dc converter, having two full-bridge dc/ac converters and a high frequency (HF) transformer. The HF transformer provides the voltage matching of two sides with different voltage levels and galvanic isolation. Details of the analysis of DAB are available in [23], [24] and [25]. Fig.5 shows the timing diagram explaining an operation of different bridges (such as B-I and B-II) and conduction sequence of IGBTs and diodes. The symbols used in the waveforms are clearly shown in Fig.2. It is important to mention that the energy stored in the decoupled inductor is sufficient to realize zero voltage switching (ZVS) of all the switches. In relation to Fig.2 (and Fig.5), following equations may be derived:

$$\frac{I_1 + I_2}{\frac{DT_s}{2}} = \frac{V_1 + V_2'}{L_d}, \quad for \ \ 0 < t < \frac{DT_s}{2} \tag{2}$$

$$\frac{I_2 - I_1}{\frac{T_s}{2} - \frac{DT_s}{2}} = \frac{V_1 - V_2'}{L_d}, \quad for \ \ \frac{DT_s}{2} < t < \frac{T_s}{2} \tag{3}$$
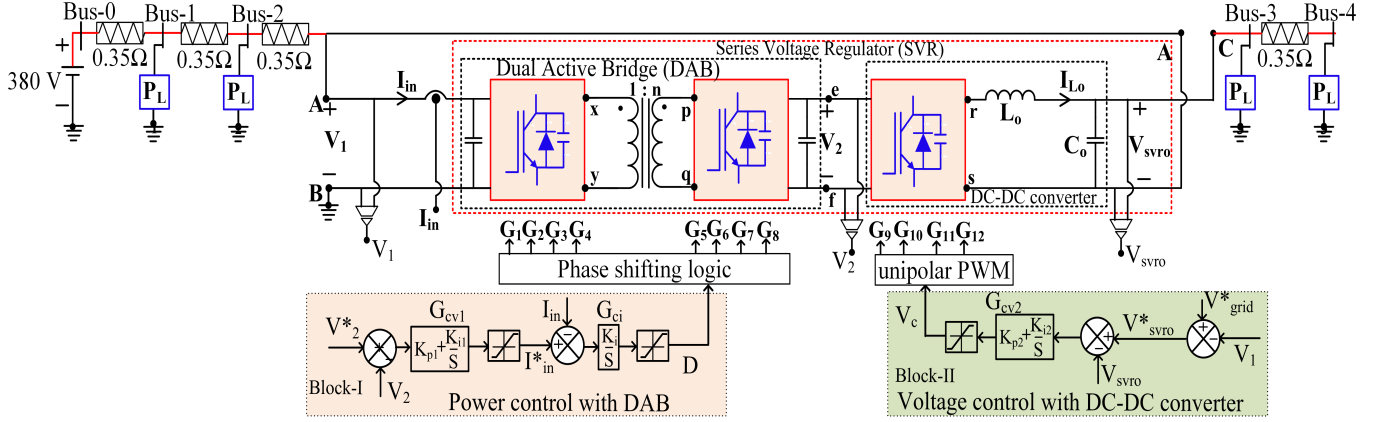
Fig. 4. The overall control block diagram

Considering the slope of AB and BC in Fig.5,

$$\frac{I_1}{\frac{DT_s}{2} - t_z} = \frac{I_2}{t_z} \quad (4)$$

where $V_2' = \frac{V_2}{n}$, $n = \frac{V_2}{V_1} = \frac{N_2}{N_1} = \frac{I_{in}}{I_0}$. Solving above equations, the expressions of I_1, I_2 and t_z are as follows.

$$I_1 = \frac{T_s[V_2 + nV_1(2D-1)]}{4nL_d} \quad (5)$$

$$I_2 = \frac{T_s[nV_1 + V_2(2D-1)]}{4nL_d} \quad (6)$$

$$t_z = \frac{T_s[nV_1 + V_2(2D-1)]}{4(nV_1 + V_2)} \quad (7)$$

Since the average of input side capacitor current is zero, the average input current (I_{in}) of DAB may be calculated as follows.

$$I_{in} = <I_{dc1}> = \frac{V_2 T_s(D - D^2)}{2nL_d} \quad (8)$$

The input power to the DAB is:

$$P_{in} = <I_{dc1}> V_1 = I_{in}V_1 = \frac{V_1 V_2 T_s(D - D^2)}{2nL_d} \quad (9)$$

Neglecting loss, the output current (I_{inb}) of DAB in Fig.2 (i.e. input current of full bridge dc-dc converter) can be written as follows.

$$I_{inb} = <I_{dc2}> = \frac{V_1 T_s(D - D^2)}{2nL_d} \quad (10)$$

The power transferred by the DAB is:

$$P_{o2} = <I_{dc2}> V_2 = I_{inb}V_2 = \frac{V_1 V_2 T_s(D - D^2)}{2nL_d} \quad (11)$$

The maximum power may be transferred from primary to secondary when $D = 0.5$. Additionally, the reactive component of the transformer current (i.e. I_Q) is higher for higher value of D [26]. In Fig.5, the source for this reactive current is the negative part of I_{Ld} when V_{tp} is positive (i.e. from 0 to t_z) and positive part of I_{Ld} when V_{ts} is negative (from t_z to $\frac{DT_s}{2}$). Note that the reactive component of the current

is circulated inside DAB. The total reactive current over one complete cycle is defined as:

$$I_Q = I_{Qp} + I_{Qs} \quad (12)$$

where I_{Qp} and I_{Qs} are the reactive current component at the primary side and secondary side respectively. These currents can be expressed as: $I_{Qp} = \frac{2I_2 t_z}{T_s}$, and $I_{Qs} = \frac{2I_1(\frac{DT_s}{2} - t_z)}{T_s}$. The total reactive power associated to the converter is written as:

$$Q = V_1 I_{Qp} + V_2' I_{Qs} \quad (13)$$

The ratio of reactive to active power (λ) is calculated using (14).

$$\lambda = \frac{Q}{P_{in}} \quad (14)$$

B. Full bridge dc-dc converter

The full bridge dc-dc converter is used to generate adjustable voltage for desired voltage regulation. The waveforms of under ideal operating condition are shown in Fig.6. The switching signals for T_9, T_{10}, T_{11} and T_{12} are generated through the comparison of triangular carrier signal (V_{tri}) and control signal (V_c). The polarity of the output voltage can be changed from $+V_2$ to $-V_2$ and vice versa by changing the sign of the control signal (i.e. from $+V_c$ to $-V_c$). Note that the switches T_9, T_{12} and T_{10}, T_{11} are operated as a pair. The gate pulses for T_9 and T_{12} are inverse of T_{10} and T_{11} with appropriate dead time [21]. An LC filter is used at the output of dc-dc converter for filtering out the ripples from the output voltage.

The magnitude of V_{rs} is changing from $+V_2$ to $-V_2$. The I_{Lo} is the current flowing through the filter inductor. The SVR output voltage (V_{svro}) and output current (I_{svro}) are the average values of V_{rs} and I_{Lo} respectively.

Applying Volt-Sec balance, relation between the output and input voltages may be given by (15).

$$V_{svro} = (2d_1 - 1)V_2 \quad (15)$$

Where $d_1 = \frac{t_{on}}{T_s} = 0.5(1 + \frac{V_c}{V_{trip}})$

The output capacitor voltage (V_{svro}) is always less than or equal to input voltage (V_2) and varies from $+V_2$ to $-V_2$. Thus it functions as a buck converter.
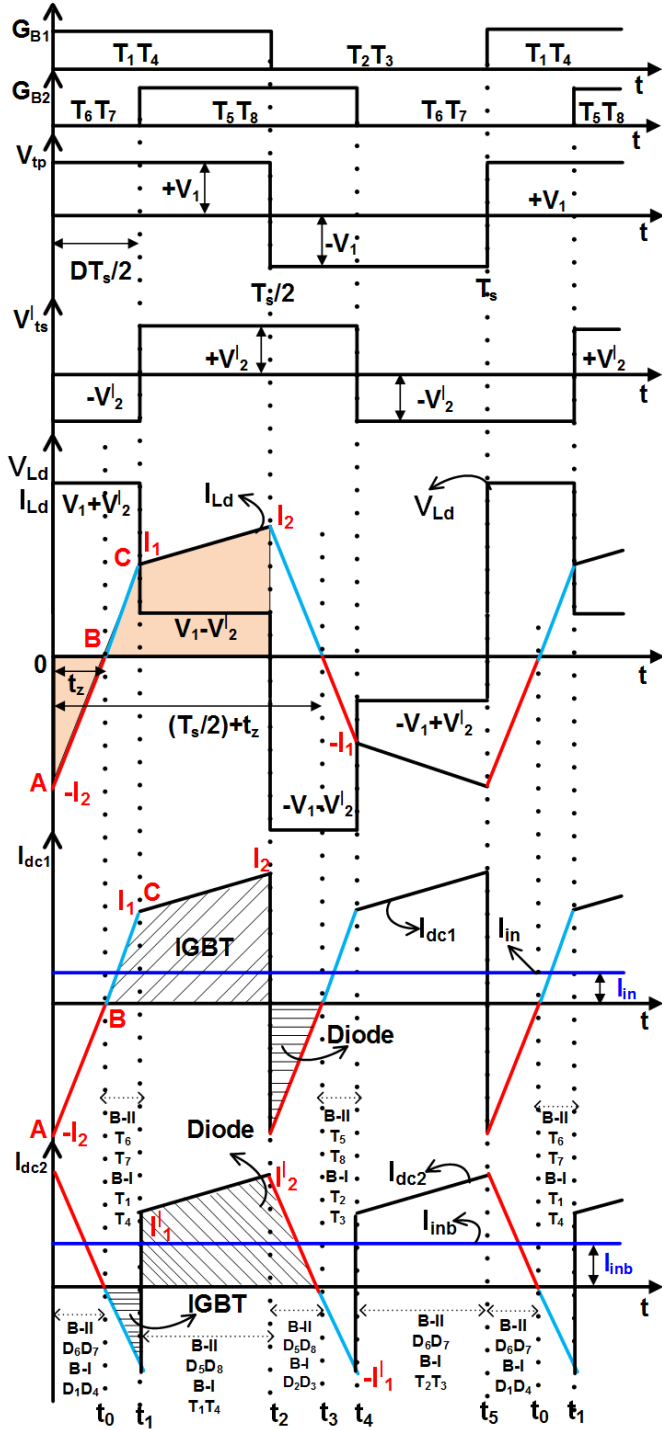
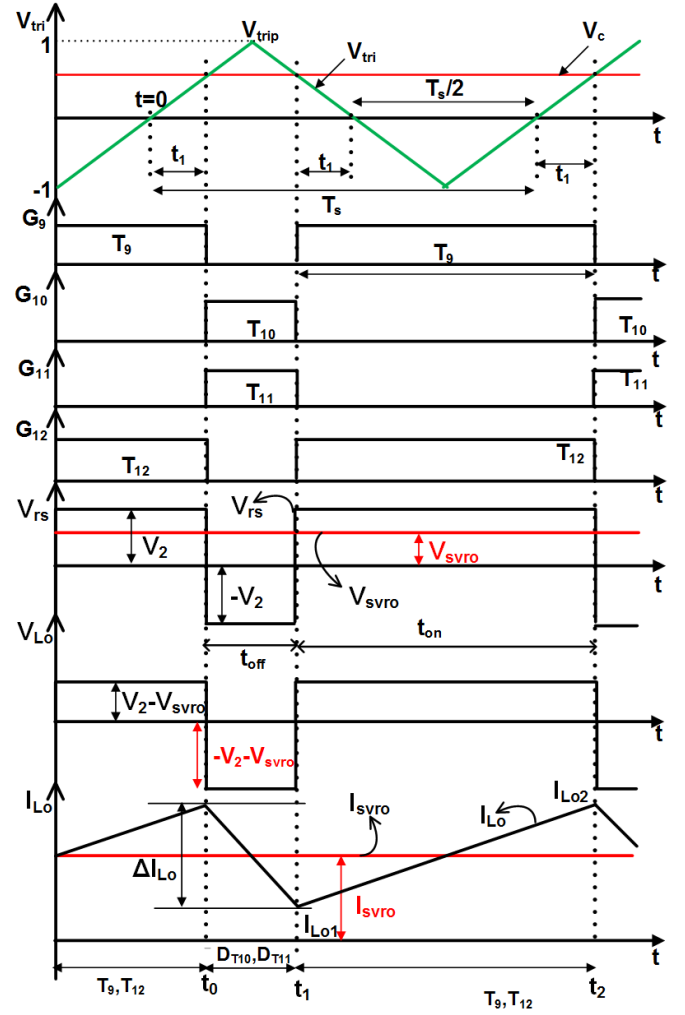Fig. 5. Waveforms of DAB under ideal operating conditions

Fig. 6. Waveforms of full bridge dc-dc converter under ideal operating conditions

$$G_{v2d} = \frac{\hat{v}_2}{\hat{d}} = \frac{M_{id}Z_o\left(\frac{1}{n} + Z_{in}M_{iv}\right)}{1 - Z_{in}Z_oM_{iv}^2} \quad (17)$$

where $M_{iv} = \frac{T_s}{2nL_d}(D - D^2)$, $M_{id} = \frac{V_2T_s}{2nL_d}(1 - 2D)$, $Z_{in} = \frac{r_s(1+Sr_{c1}C_1)}{1+SC_1(r_{c1}+r_s)}$, $Z_o = \frac{r_o(1+Sr_{c2}C_2)}{1+SC_2(r_{c2}+r_o)}$, $M_{in} = \frac{1+SC_1r_{c1}}{1+SC_1(r_{c1}+r_s)}$

Using equations (16) and (17), the DAB input-current to output-voltage transfer function (G_{v2iin}) may be written as follows.

$$G_{v2iin} = \frac{\hat{v}_2}{\hat{i}_{in}} = \frac{\hat{v}_2}{\hat{d}} \frac{\hat{d}}{\hat{i}_{in}} \quad (18)$$

With the help of above transfer functions, the control block diagram of DAB is shown in Fig.7.

The closed loop transfer function between I_{in}^* and I_{in} can be expressed as

$$G_i = \frac{I_{in}}{I_{in}^*} = \frac{T_i}{1 + T_i} \quad (19)$$

where $T_i = G_{ci}G_{iind}H_{i1}$.

The K_i of the current controller (G_{ci}) is designed to set the gain-cross-over frequency at $\frac{1}{10}$ times of the switching fre-

V. DESIGN AND PARAMETER SELECTION

A. Controller gains

The control signal (D) to input-current (I_{in}) transfer-function (G_{iind}) and control signal (D) to output-voltage (V_2) transfer-function (G_{v2d}) of DAB can be written as follows [27].

$$G_{iind} = \frac{\hat{i}_{in}}{\hat{d}} = \frac{M_{in}M_{id}\left(1 + \frac{Z_oM_{iv}}{n}\right)}{1 - Z_{in}Z_oM_{iv}^2} \quad (16)$$

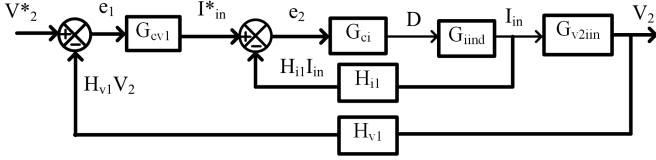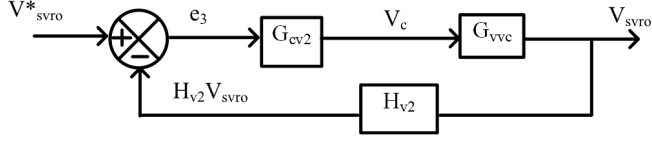Fig. 7. The control block diagram for DAB

Fig. 8. The control block diagram for full bridge dc-dc converter

quency. With the help of MATLAB toolbox, K_i is calculated as 100.

The transfer function between V_2 and V_2^* can be expressed as follows.

$$G_{v1} = \frac{V_2}{V_2^*} = \frac{T_{v1}}{1 + T_{v1}} \qquad (20)$$

where $T_{v1} = \frac{G_i}{H_{i1}} G_{cv1} G_{v2iin} H_{v1}$.

The gains of the voltage controller (i.e. K_{p1}, K_{i1} of G_{cv1}) are selected in such a way that the bandwidth of the outer voltage loop should be 10 times lower than the inner current loop. Considering this, K_{p1} and K_{i1} is calculated as 1.9 and 10.1, respectively.

The control block diagram for buck dc-dc converter is shown in Fig.8. The control signal (V_c) to output-voltage (V_{svro}) transfer-function (G_{vvc}) is written as follows [28].

$$G_{vvc} = \frac{\hat{V}_{svro}}{\hat{V}_c} = \frac{(XR_o)V_2}{(XR_o) + Y(X + R_o)} \qquad (21)$$

Where $X = r_{esr} + \frac{1}{SC_o}$, $Y = r_L + SL$, R_o is the load resistance.

The transfer function between V_{svro} and V_{svro}^* can be expressed as:

$$\frac{V_{svro}}{V_{svro}^*} = \frac{T_{v2}}{1 + T_{v2}} \qquad (22)$$

where $T_{v2} = G_{cv2} G_{vvc} H_{v2}$.

The gains of the voltage controller (i.e. K_{p2}, K_{i2} of G_{cv2}) in buck dc-dc converter are selected in such a way that the bandwidth of the voltage loop should be 10 times lower than the switching frequency. Considering this, K_{p2} and K_{i2} can be calculated as 3.973 and 0.02, respectively.

B. Power rating of SVR

In this paper, power rating of the SVR is selected as follows without considering losses. The resistance between buses (r_{ij}) is considered as 0.35Ω. The load connected at each bus is 2500 W which is realized through a resistance(R_{Li}) of 58Ω. The current (I_{Li}) drawn by each load at 380 V is 6.55 A. At full-load condition, the voltage drop up to Bus-3 (In Fig.1) is computed as 20.63 V ($0.35 \times (4I_L + 3I_L + 2I_L)$). This voltage drop is nearly 5% of grid voltage (i.e. 380 V). The

same voltage drop is compensated by SVR, such that the bus-3 voltage is equal to Bus-0 voltage. The SVR is connected in series with dc grid and is placed in-between Bus-2 and Bus-3. The maximum current flowing through bus-2 and bus-3 is 13.1A. Therefore, the rating of the SVR is 270.33W ($I_{23} \times V_{svro}$). This power is nearly 2.7% of total load (i.e. 10kW) connected to the dc microgrid.

VI. SIMULATION RESULTS

A dc microgrid at 380V level having four nodes (load connected at each node using a variable-resistance of 58Ω (that represents 2.5kW of power) with transmission line resistance of 0.35Ω is considered for simulation study. The 380V dc voltage source is assumed as dc grid and the parameters of SVR for simulation are: P_o =500W, V_1 =380V±5%, V_{svro} =0-24V (by providing constant output voltage of DAB that is V_2 =24V), F_{sw} =10 kHz, C_1 =500μF, C_2 =1200μF, L_d =3.034mH, C_o =20μF, L_o =2.2mH. The results are presented for the following cases.

A. Case-I: Sudden load increase in all buses

Suppose the microgrid is running at light load condition, say 30 % of the rated load. The voltage of all the buses stays close to bus-0 voltage, i.e. 380V. Now, suddenly, load of all the buses is changed from 30% to 100% at 1 sec (Fig.9 (f)). It is observed that the bus-3 voltage (Fig.9 (a)) suddenly falls below desired value. With SVR, bus-3 voltage (Fig.9 (b)) is restored to its previous value (i.e. 380 V) within 100ms. The response time of SVR during transient is decided by the voltage controller (i.e. second stage of the power circuit) and the capacitor which is connected across the output of SVR. Here, SVR adds the appropriate series voltage with proper polarity to compensate drop across line resistance. Fig.9 (c) and (d) indicate the output and input voltages of the SVR, respectively. It is also noticed that the DAB output voltage (Fig.9 (e)) is maintained at its reference (i.e. 24V) under the variation of input voltage and loading condition. Note that power flow within the SVR is from input side to output side for this operating condition.

B. Case-II: Sudden load decrease in all buses

In this case, the loading condition of all buses is changed from 100% to 30% at 2 sec (Fig.10 (f)). The bus-3 voltage with and without SVR are shown in Fig.10 (a) and (b) respectively. The voltage compensation required from the SVR is reduced due to light load condition. However, a voltage overshoot of 15% (Fig.10 (b)) is observed in bus-3 voltage during transient. This is due to the dynamics of output side capacitor voltage of the SVR. The output and input voltages of SVR are shown in Fig.10 (c) and Fig.10 (d) respectively. The output voltages of DAB for this operating condition is shown in Fig.10 (e), which is maintained to its reference value (i.e. 24 V).

VII. EXPERIMENTAL RESULTS

A. Prototype description

The hardware prototype is shown in Fig.11. For simplicity, two buses are only considered. To demonstrate a fall in voltage
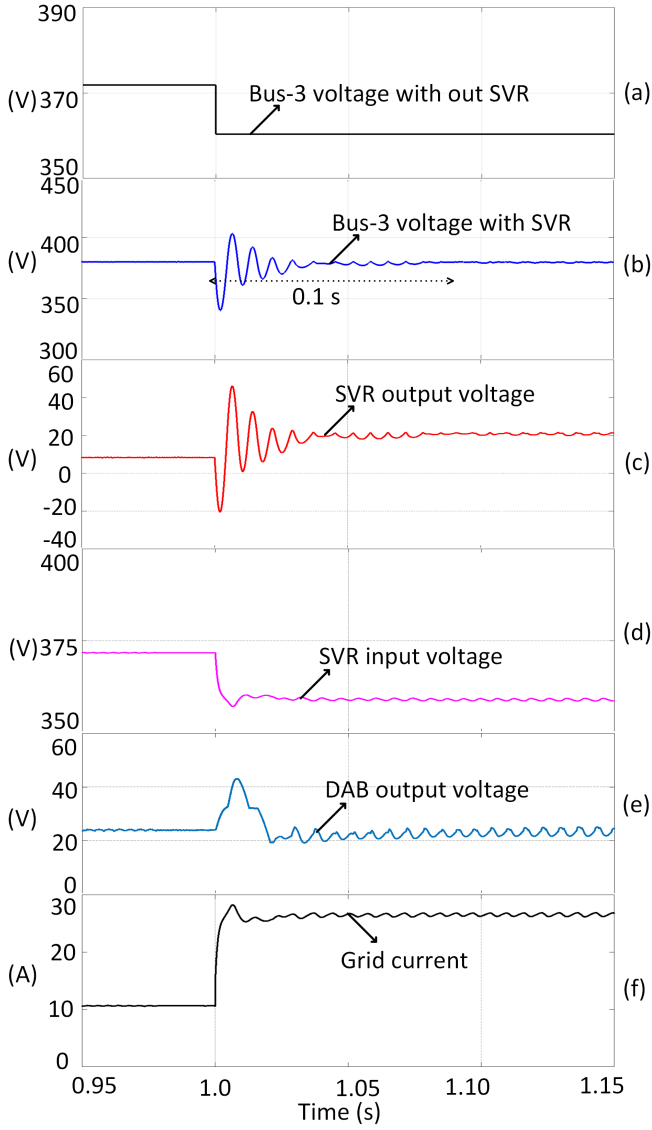
Fig. 9. Transient response of the system for load increase at all buses: (a) Voltage at bus-3 without SVR, (b) Voltage at bus-3 with SVR (V_3), (c) Output voltage of SVR (V_{svro}) (d) Input voltage of SVR (V_1), (e) DAB output voltage (V_2), (f) Grid current (I_{01})
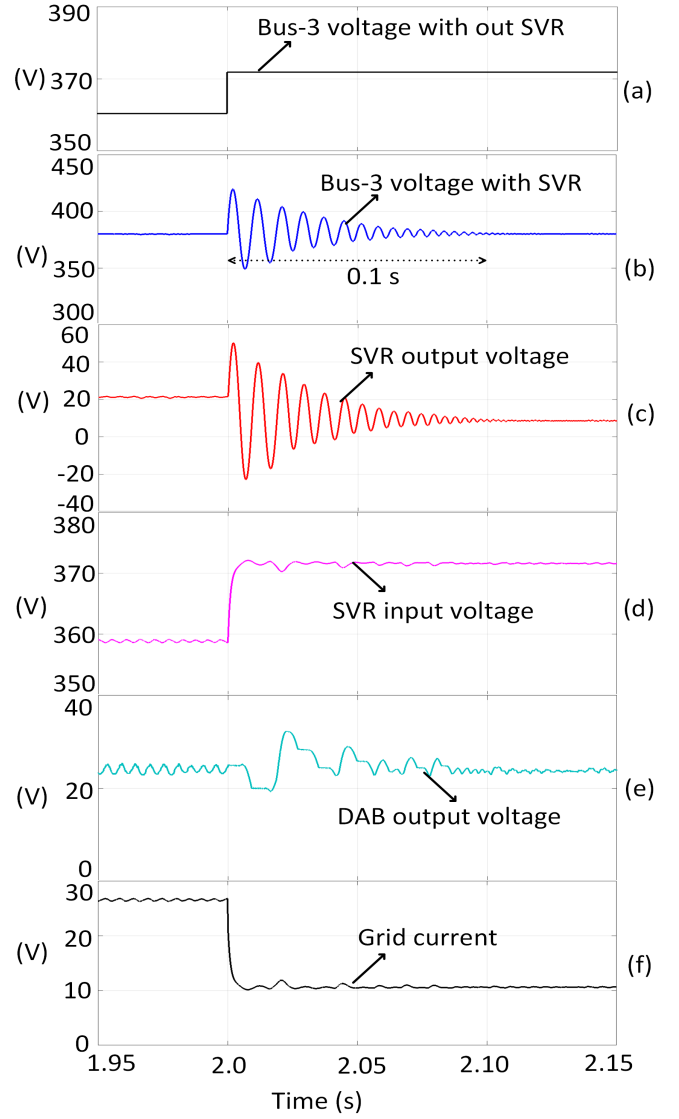

Fig. 10. Transient response of the system for load decrease at all buses: (a) Voltage at bus-3 without SVR, (b) Voltage at bus-3 with SVR (V_3), (c) Output voltage of SVR (V_{svro}) (d) Input voltage of SVR (V_1), (e) DAB output voltage (V_2), (f) Grid current (I_{01})

and corresponding compensation, two buses are sufficient. Source is connected at bus-0 and loads are connected at bus-3. An equivalent resistance of 0.3Ω (100W) is connected between source and load which represents resistance of the transmission line. Semikron make half-bridge IGBT module (SKM75GB12T4) available in the laboratory is used to form DAB and dc-dc converter of the power circuit. The transformer and decoupled inductor are made with Ferrite core (N-87) of size ETD-59. The primary and secondary windings have 12-turns and 6-turns, respectively. The input source voltage (V_s) is 30V, while V_3 bus-3 voltage is regulated to 30V using SVR. Remaining hardware parameters are C_1 =4700μF 450V, C_2 =4700μF 450V, C_o =32μF 100V, L_o =0.5mH 10A and the switching frequency is 10kHz. The entire control is implemented using a VIRTEX-5 FPGA based GENESYS evaluation board [29].

B. Load variation from 112W (0.62pu) - 180W (1pu) and vice versa

Fig.12 and Fig.13 show the waveforms when load is increased from 112W (0.62 pu) to 180W (1 pu). Note that the load variation is performed through a variable resistance whose value is decreased from 8Ω to 5Ω. The load voltage, i.e. bus-3 voltage (Fig.12 (ch3)) is maintained at 30V and the corresponding voltage provided by SVR is shown in Fig.(Fig.12 (ch2)). It is observed that SVR output voltage is increased from 2.9V to 4.09V to compensate for the voltage drop due to loading. The input of the SVR is plotted in Fig.12 (ch4). The DAB output under the variation of load is shown in Fig.13. Similarly, the results under load change from $180W(1pu) - 112W(0.62pu)$ are also verified. Due to space constraint results are not given for this case. It is observed that the reverse phenomena are happening in this case (i.e.
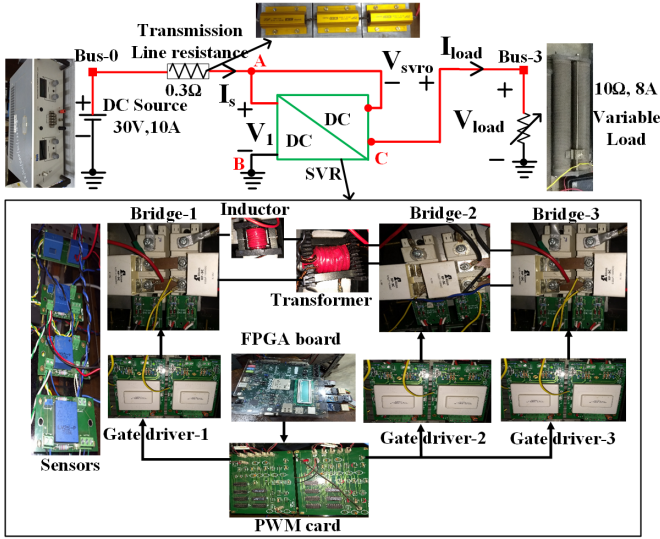
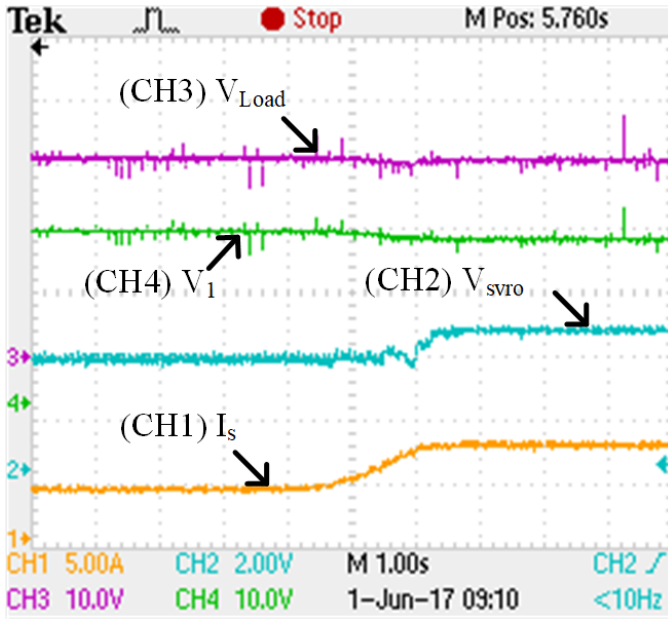Fig. 11. Photographic view of the hardware prototype

Fig. 13. DAB waveforms with increasing load: ch1: I_s grid current (2 A/div), ch3: V_2 DAB output voltage (10 V/div).

Fig. 12. Experimental waveforms with increasing load: ch1: I_s grid current (5 A/div), ch2: V_{svro} output voltage of series regulator (2 V/div), ch3: V_{load} load voltage at bus-3 (10 V/div), ch4: V_1 Input voltage of the series regulator (10 V/div).

Fig. 14. High frequency transformer waveforms at light load ($R_{load} = 8\Omega$): ch1: I_{Ld} Primary current (2 A/div), ch2: V_{ts} Secondary voltage (20 V/div), ch3: V_{Ld} Decoupled inductor voltage (50 V/div), ch4: V_{tp} Primary voltage (50 V/div).

load decrease) compared to its previous operating condition (i.e. load increase).

C. Performance of DAB under ZVS operation

The voltage across the transformer windings and decoupled inductor along with current waveform are presented in Fig.14 under light load condition (say 0.62pu). The same waveforms under full load condition are shown in Fig.15. It is observed that the phase-shift angle and current peak are increased with the increase of loading condition, that is expected. It is also noticed that the $\frac{Q}{P_{in}}$ ratio is more at high load condition compared to light load as the reactive and active powers are depending on the phase-shift Fig.16 shows the ZVS operation
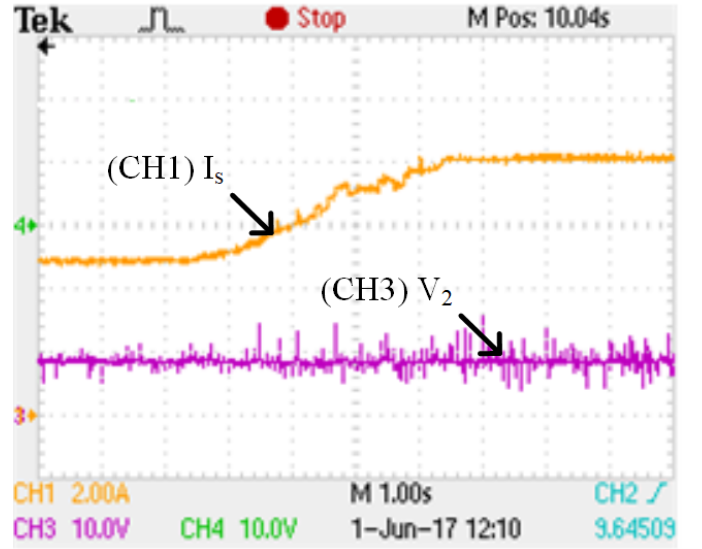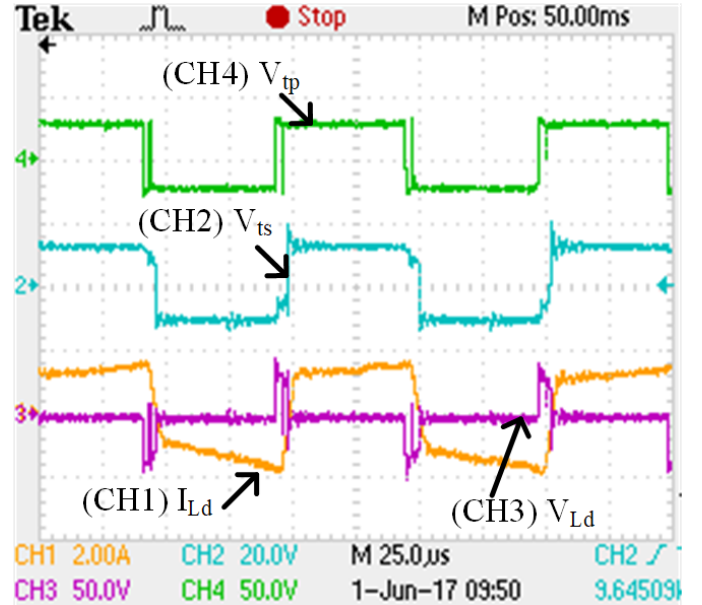
at turn-ON for both primary and secondary side bridges at full load condition which are identified with circles. Similarly, at light load condition, the ZVS operations at turn-ON are shown in Fig.17.

VIII. CONCLUSION

This paper presents the concept of a novel series voltage regulator for dc microgrid. Topologically, this is a cascading of Dual Active Bridge (DAB) and a full bridge dc/dc converter connected in input-parallel and output-series mode. The dc/dc converter can generate both positive and negative voltages and
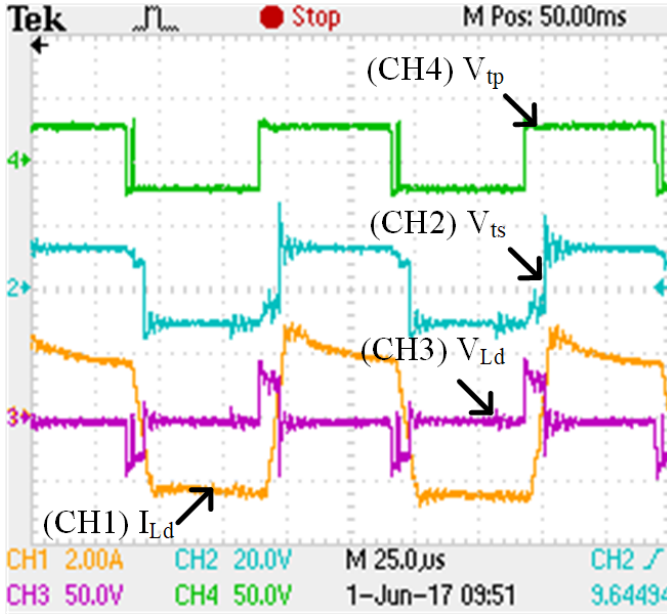
9

Fig. 15. High frequency transformer waveforms at high load ($R_{load} = 5\Omega$): ch1: I_{Ld} Primary current (2 A/div), ch2: V_{ts} Secondary voltage (20 V/div), ch3: V_{Ld} Decoupled inductor voltage (50 V/div) , ch4: V_{tp} Primary voltage (50 V/div).
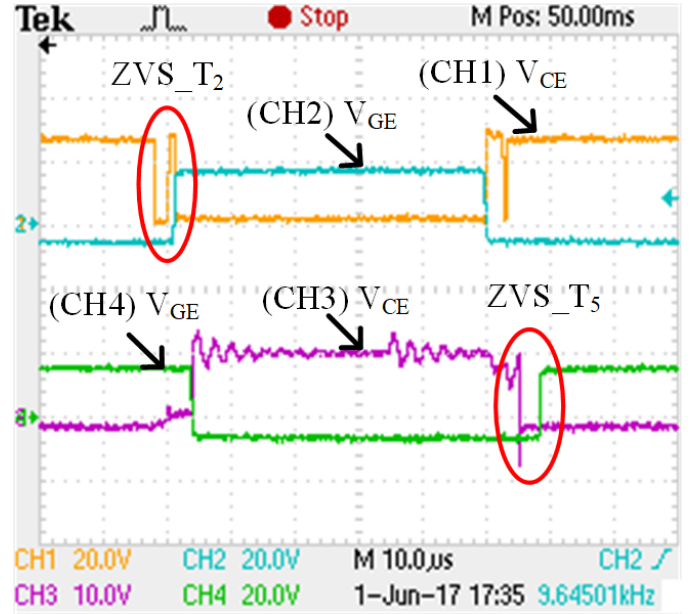

Fig. 17. ZVS waveforms for T_2 and T_5 at light load ($R_{load} = 8\Omega$): ch1: V_{CE} of T_2 (20 V/div), ch2: V_{GE} of T_2 (20 V/div), ch3: V_{CE} of T_5 (10 V/div) , ch4: V_{GE} of T_5 (20 V/div)..
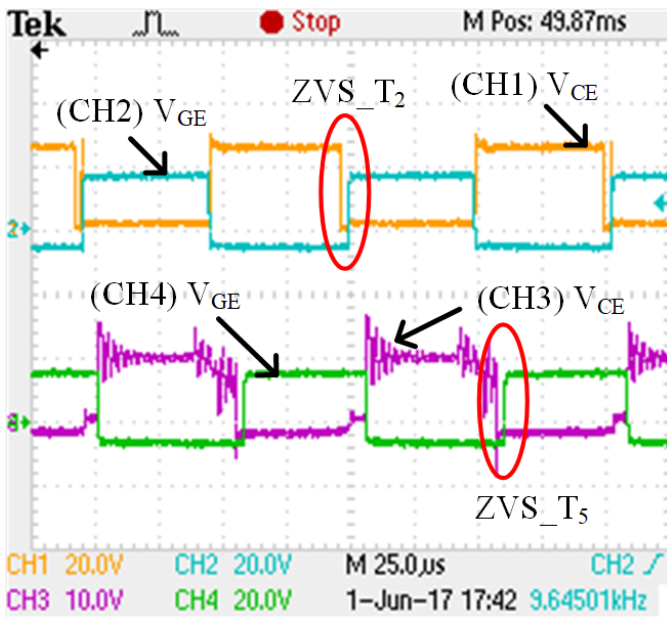

Fig. 16. ZVS waveforms for T_2 and T_5 at high load ($R_{load} = 5\Omega$): ch1: V_{CE} of T_2 (20 V/div), ch2: V_{GE} of T_2 (20 V/div), ch3: V_{CE} of T_5 (10 V/div) , ch4: V_{GE} of T_5 (20 V/div).

related problems of the dc distribution systems and expected to be very popular in future.

therefore is capable of handling forward and reverse power flow during voltage sag and swell respectively. The turn-on of switching devices in DAB occur at zero voltage which reduces switching losses of the converter. The SVR dynamically regulates bus voltages of the dc microgrid for various loading conditions. Optimal placement of the SVR keeps the dc distribution system regulated. The performance of SVR is extensively checked through simulation and experimental prototype. The proposed SVR removes the voltage fluctuation

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