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# Design of a Transimpedance Amplifier for an Optical Receiver

Dissertação para obtenção do Grau de Mestre em

**Engenharia Electrotécnica e de Computadores**

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UNIVERSIDADE NOVA DE LISBOA

**Setembro, 2017**

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*To my beloved family...*

# Acknowledgements

I would like to thank Professor Nuno Paulino for his support, commitment, advice and supervision, motivation and encouragement throughout the development of this thesis. Especially for all his help and patience when helping me sort out problems, even when sometimes things appeared to be stuck. I would also like to thank Professor Luís Oliveira for the assistance provided. I would also like to thank to all my close friends and colleagues for many interesting discussions, their support and friendship. In particular, André Cardoso, Dário Pedro, Diogo Correia, Diogo Ferreira, Diogo Mendes and so many others.

Last, but not least, I thank my mother, father and sister for all their care, support and stimulus to do more and well, not only during this thesis, but also throughout the entire academic course. And to Beatriz, who was always present for the good and bad moments, for all her love, support, and especially, for the encouragement and never having stopped believing that I could make it through to the end.

# Abstract

In today's world, technology is so developed that it is possible to transmit huge amounts of data in a short time.

In the experiments with high energy levels in laboratories carried out in CERN, it is essential to have a method capable of carrying all this information and at the same time of being tolerant to the radiation from these same experiments.

Optical fibres are currently the best method transmitting the data created by these experiments. In order to receive the information from the optical fibre a Photodiode (PD) is used to produce current from the light of the optical fibre. This current is however small. It is necessary to use an amplifier which, in addition to amplifying the current coming from the photodiode, also converts it into a voltage for the next phases of the optical receiver.

These amplifiers are known as transimpedance amplifiers and are the critical part of optical receivers since an high gain is required to amplify the current from the photodiode and at the same time a high bandwidth to receive the hight data rate signals.

This thesis presents a complete analysis of these amplifiers, showing various types of topologies and their pros and cons. In order to arrive at the amplifier with the desired characteristics, this thesis uses mathematical equations that allow us to describe the operation of the Transimpedance Amplifier (TIA) and to determine the optimal range between the gain, the bandwidth and the noise of the amplifier (input referred noise). All the theoretical expressions as well as the behaviour of the whole system was verified using electrical simulations.

**Keywords:** Fiber optics, Transimpedance amplifiers, Amplifier gain, Bandwidth, Input reffered noise, Complementary metal-oxide-semiconductor (CMOS).

# Resumo

No mundo atual a tecnologia está tão desenvolvida que é possível transmitir enormes quantidades de dados num curto espaço de tempo.

No *Conseil Européen pour la Recherche Nucléaire* (CERN) são realizadas experiências em laboratório, com altas quantidades de energia. Por isso, torna-se imprescindível recorrer a um método capaz de transportar toda esta informação, mas que se mostre tolerante à radiação destas mesmas experiências.

As fibras óticas são, atualmente, o melhor método para estas transmissões de informação. A produção de informação a partir da luz passa por um processo complexo.

Com a utilização de, pelo menos, um fotodíodo (PD), é possível produzir corrente a partir da luz fornecida pela fibra ótica. Esta corrente é, no entanto, pequena. Para a utilizar é necessário um amplificador que, para além de amplificar a corrente proveniente do fotodíodo, converta esta corrente em tensão, para a fornecer, de forma correta, às próximas fases de tratamento da informação.

Estes amplificadores são conhecidos como amplificadores de transimpedância e são a parte fulcral dos recetores óticos, porque é necessário ter um elevado ganho para amplificar a corrente proveniente do fotodíodo e, ao mesmo tempo, uma elevada largura de banda, para transmitir a altas frequências. Para uma melhor compreensão destes amplificadores eles foram cuidadosamente estudados na tecnologia CMOS de 65 nm.

Esta tese apresenta uma análise completa destes amplificadores, mostrando vários tipos de topologias, os seus prós e os seus contras. Para chegar ao amplificador com as características pretendidas, foram utilizadas equações matemáticas que permitem descrever o seu funcionamento e determinar a gama ótima entre o ganho, a largura de banda e o ruído referente à entrada do amplificador.

Todas as expressões teóricas, bem como o comportamento de todo o sistema, foram verificados e validados, através de simulações elétricas.

**Palavras-chave:** Fibra óptica, Amplificadores de transimpedância, ganho do amplificador, largura de banda, ruído referente à entrada, CMOS.

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# Acronyms

**Ad** Open loop gain.

**CERN** Conseil Européen pour la Recherche Nucléaire.

**CMOS** Complementary metal-oxide-semiconductor.

**DC-DC** Direct current to direct current.

**DRC** Design Rule Check.

**LA** Limiting Amplifier.

**LVS** Layout vs. Schematic.

**OC** Offset Cancellation.

**PD** Photodiode.

**PEX** Practices Extraction.

**PRBS** Pseudorandom Binary Sequence.

**SC** Switched Capacitor.

**SOC IC** System on a Chip Integrated Circuit.

**TIA** Transimpedance Amplifier.

# Nomenclature

Some of the most common and constant symbols used throughout the thesis are listed below.

**Electrical Symbols**

**I** Current

**V** Voltage

**Units**

**A** Ampere

**dBm** Decibel Miliwatt

**dB** Decibel

**Hz** Hertz

**m** Metro

**rad** Radian

**s** Second

**V** Volt

**Mathematical Symbols**

$\approx$ Approximately equal to

$\log_a(x)$ Base logarithm $a$ of $x$

**Other Symbols**

**f** Frequency

**t** Time

Chapter 1

# Introduction

## 1.1 Context and Motivation

This chapter's purpose is to contextualize the Transimpedance Amplifier sub-block and its function in an optical receiver to be implemented in a 65nm CMOS technology for a high-speed optical link (as well as other sub-blocks such as: a Power-on Reset and an Offset cancelling). It will be explained what motivated this project in the first place and the main goals to be achieved during this work. It will also discuss some of the state of the art topologies and techniques for building and solving some of the most relevant problems associated with this type of amplifiers. Finally, a work plan will be presented as well as the chosen circuit topology and the respective theoretical analysis.

The European Organization for Nuclear Research, known as CERN ("Conseil Européen pour la Recherche Nucléaire") performs high energy physics experiments at the LHC (Large Hadron Collider) so the need for a way to efficiently transfer the huge amount of data originating from these experiments to the counting room is very pressing. Due to the radioactive character of these experiments the most practical way to do it is using optical fibre since it has a high tolerance to radiation and is almost immune to magnetic fields and electromagnetic noise.

It is therefore necessary to have a high speed radiation-tolerant optical receiver and the most economical way to do this is to have all the blocks embedded in the same IC (Integrated Circuit).

As shown in Figure 1.1 and without going into too many details, the photodiode receives light from the optical fiber and transforms it into current. The TIA, one of the most critical building blocks in the optical receiver, converts this current into voltage and the LA receives this voltage and is able to convert to bits.

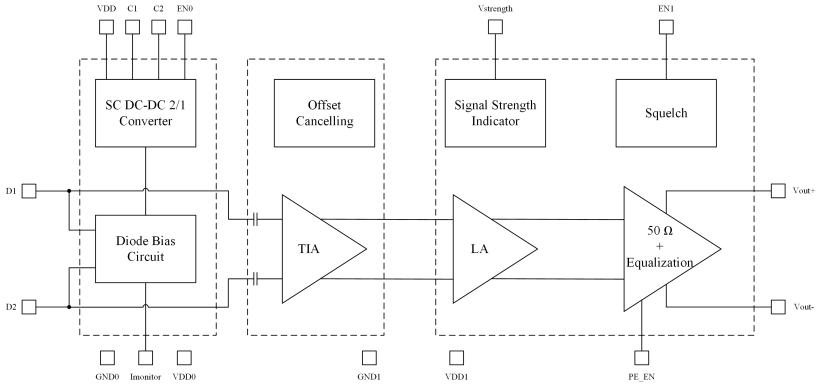



Figure 1.1: Optical Receiver Block Diagram.

## 1.2 Goal and Approach

In contrast to previous studies, the goal of this research is to go further and design a fully differential TIA compatible with a serial 5 Gb/s data rate. This requires enhanced bandwidth and optimized transimpedance gain, input referred noise and group delay variation from the TIA.

To achieve wide bandwidth and low group delay variation, a differential TIA is proposed. The Proposed design also combines regulated cascode and peaking inductors so as to have wide band response. Performance of the proposed TIA is compared with other existing TIAs, and the proposed TIA shows significant improvement in bandwidth and group delay variation compared to other existing TIA architectures.

## 1.3 Dissertation Structure

The following chapters of this document present the design of a trans-impedance amplifier for an optical receiver, starting from the state-of-the-art review through to the layout implementation and statement of the final conclusions. The chapters are structured as shown in the following summary:

- **Chapter 1: Introduction** presents the work and proposes the implementation approach. The motivations are outlined and the architecture is explained;
- **Chapter 2: State of the Art** shows the history behind the technology. Several interesting considerations are explored, in order to establish the background of existing TIA topologies. The search for new ideas and potential income;
- **Chapter 3: Power-on Reset and Brown-Out Reset Implementation** analyses and designs each sub-block making up the total block (POR-BOR);
- **Chapter 4: Proposed TIA circuit.** Mathematical equations are also analyzed for optimizing the static gain, bandwidth and input referred noise;

- **Chapter 5: Offset Cancellation Implementation** discusses the importance of cancelling the offset produced, for example, by device mismatch and drift due to thermal variations. Lastly, the proposed OC circuit is presented.
- **Chapter 6: Conclusion and Future Work** summarizes the study and its achievements. Further comments, criticisms and improvements are taken into consideration, so the project can evolve and progress.

CHAPTER 2

# STATE OF THE ART

## 2.1 Role and working principle of TIA

In an optical receiver, a transimpedance amplifier (TIA) is used to amplify a current signal, $I_{in}$, converted from the incoming optical signal by a photodiode (PD), to a voltage signal, $V_{out}$ [1]. The circuit is therefore characterized by several properties, including transimpedance gain, bandwidth and input referred noise current as shown in Figure 2.1:

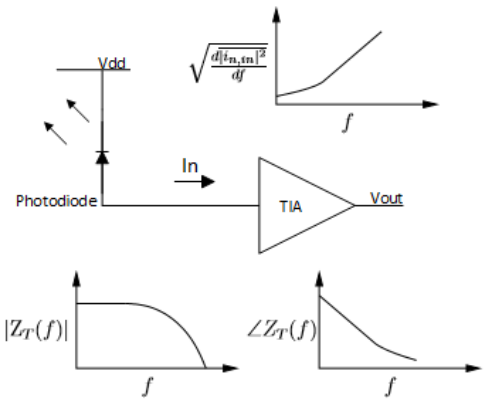



Figure 2.1: Transimpedance Amplifier, Behzad Razavi-"Design of Integrated Circuits for Optical Communications".

The transimpedance gain of the TIA is the ratio of the output voltage to the input current.

$$|Z_T(f)| = \left|\frac{V_{out}}{I_{in}}\right| \tag{2.1}$$

The noise contribution of the TIA is characterized by the input referred noise current. The input referred noise current is the noise current that could be applied to the equivalent noiseless TIA that would produce an output noise voltage equal to that in the original noisy circuit [1]. This is shown below in Figure 2.2.

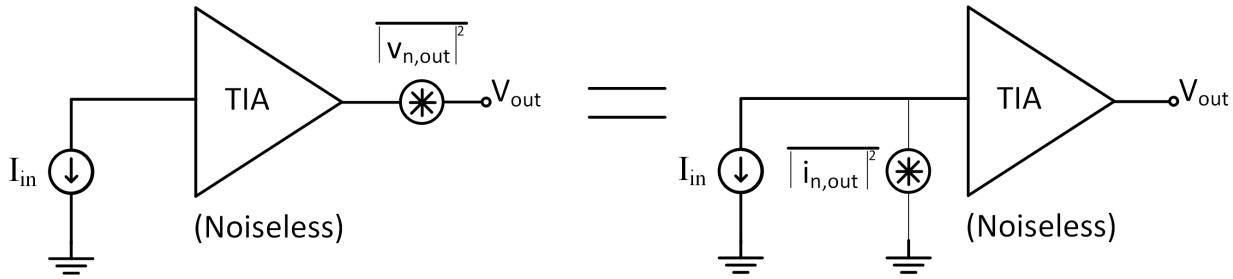



Figure 2.2: Input Referred Noise Current, Behzad Razavi-"Design of Integrated Circuits for Optical Communications".

The input referred noise current is related to the output noise voltage by the following equation.

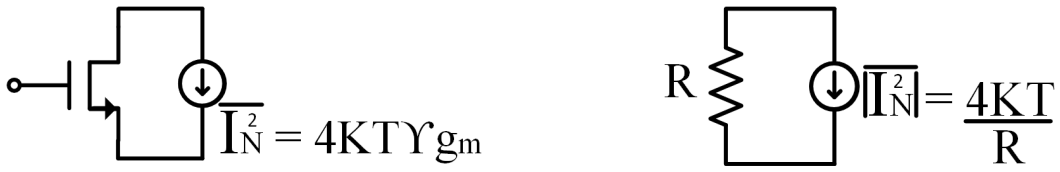
$$\overline{|I_{n,in}^2|} = \frac{\overline{|Vout_{n,out}^2|}}{|Z_T^2|} \tag{2.2}$$

The input referred noise current is used to provide a fair comparison between amplifiers since it does not depend on the transimpedance gain of the amplifier.

Equation 2.2 shows that it is necessary to calculate the noise at the output and then refer to the input, dividing the value calculated by the static gain.

To calculate the voltage noise in a transistor and resistance it is necessary to consider the resistance and transistor noises [1].

The thermal noise in a transistor can be represented by a current source connected between the drain and the source with a spectral power density given by, $\overline{|I_n^2|} \approx 4kTgm$, Figure 2.3a, where k is the Boltzmann constant and T is the temperature of the transistor. The thermal noise in a resistance can be represented by a current source in parallel with the resistor, where $\overline{|I_n^2|} = \frac{4kT}{R}$, Figure 2.3b.




a Thermal noise in a transistor MOSFET.

b Thermal noise in a resistance.

Figure 2.3: Thermal noise.

After calculating the transfer functions for both noise sources, it is possible to calculate the equivalent noise voltage referred to the input. Considering that the sources of noise

are independent, it is then possible to arrive at the sum of their contributions by adding up the power of each noise source (superposition theorem) as is shown in Figure 2.4.

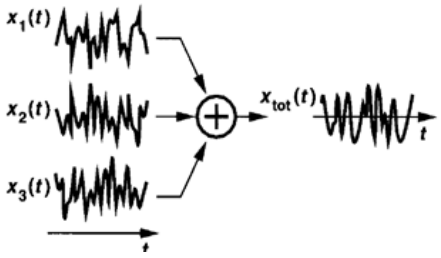



Figure 2.4: Independent noise sources,"Design of Analog Cmos Integrated Circuits" [2].

### 2.1.1 Basic Transimpedance Amplifier

Since photodiodes generate a small current and most of the subsequent processing occurs in the voltage domain, the current must be converted to voltage [1]. As depicted in Figure 2.5, a resistor, $R_L$, can perform this function, providing a transimpedance gain equal to $-R_L$ and leads to a severe trade-off between gain, noise and bandwidth.

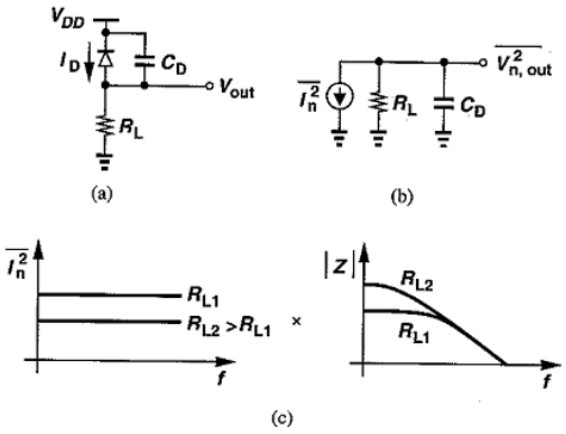



Figure 2.5: (a) Conversion of photodiode current to voltage by a resistor, (b) equivalent circuit for noise calculation, (c) effect of resistor value, Behzad Razavi-"Design of Integrated Circuits for Optical Communications". Used under fair use, 2013.

To calculate the noise voltage it is necessary to consider the noise from the resistance $R_L$ and from the transistor. Knowing that the noise from the resistance is given by $\overline{I_n^2} = \frac{4kT}{R_L}$ (noise current) and that the noise from the transistor is given by $\overline{I_n^2} = 4kTgm$, the noise voltage at the output can be obtained from,

$$\overline{Vout_{n,out}^2} = \int_0^\infty \overline{I_n^2} |R_{out}| \, df \tag{2.3}$$

Replacing $\overline{I_n^2} = \frac{4kT}{R_L}$ and $R_{out} = R_L \| \frac{1}{sC_D}$ in ( 2.3) results in the set of equations shown below.

$$\begin{aligned}\overline{Vout_{n,out}^2} &= \int_0^\infty \frac{4kT}{R_L} \left| R_L \| \frac{1}{C_D j 2\pi f} \right| df \\ &= \int_0^\infty \frac{4kT}{R_L} \frac{R_L^2}{R_L^2 C_D^2 4\pi^2 f^2 + 1} df \\ &= \frac{kT}{C_D}\end{aligned} \tag{2.4}$$

Equation ( 2.4) shows that the total integrated noise is independent of $R_L$. However, for a fair comparison it is more interesting to use the input referred noise, which can be obtained from the total integrated noise voltage ( 2.2):

$$\begin{aligned}\overline{\left|I_{n,in}^2\right|} &= \frac{\overline{\left|Vout_{n,out}^2\right|}}{\left|Z_T^2\right|} \\ &= \frac{kT}{R_L^2 C_D}\end{aligned} \tag{2.5}$$

Equation ( 2.5) indicates that, in order to reduce the input referred noise, the resistance value, $R_L$, must be maximized. However, the 3-dB bandwidth ($R_B$) of this particular circuit, is given by the pole $\frac{1}{2\pi R_L C_D}$. In short, the circuit's properties are:

$$|Z_T(f)| = R_L \tag{2.6}$$

$$\overline{\left|I_{n,in}^2\right|} = \frac{kT}{R_L^2 C_D} \tag{2.7}$$

$$R_B = \frac{1}{2\pi R_L C_D} \tag{2.8}$$

From equations ( 2.6) and ( 2.7) it is possible to conclude that in order to increase the gain and decrease the input noise, the $R_L$ resistance value should be increased. However, when the resistance value increases, the bandwidth, in turn, decreases as is shown in equation ( 2.8). It therefore implies a trade-off between the gain, input noise, and bandwidth that cannot be mitigated using a simple diode/resistor combination. Rather, it is important to create more complex structures that facilitate this trade-off and increase the flexibility of design.

## 2.2 Common TIA topologies

Generally there are two types of TIA topologies: open loop TIAs and feedback TIAs [1]. The goal of designing a TIA is to provide a circuit with a low input impedance respecting

the bandwidth requirements. It is also important to obtain high gain and low input noise, as low as possible. These two topics will be discussed later.

### 2.2.1 Open Loop TIAs

To obtain a low input impedance, open loop TIAs normally use a common base or a common gate topologies [1].

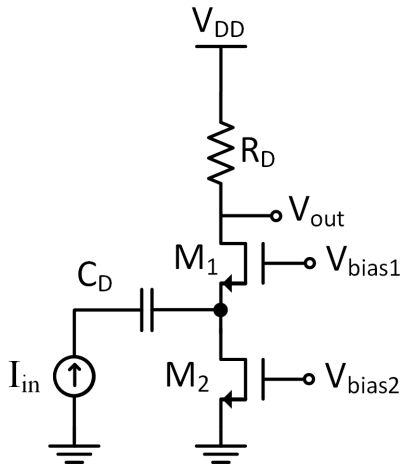



Figure 2.6: Common-gate.

Figure 2.6 shows a transistor M1 as a common-gate with a load resistor, $R_D$ (the gain of this design is approximately equal to $R_D$), and a transistor M2 operating as the bias current source. To simplify the equations, the transistor M2 will be considered as the ideal current source.

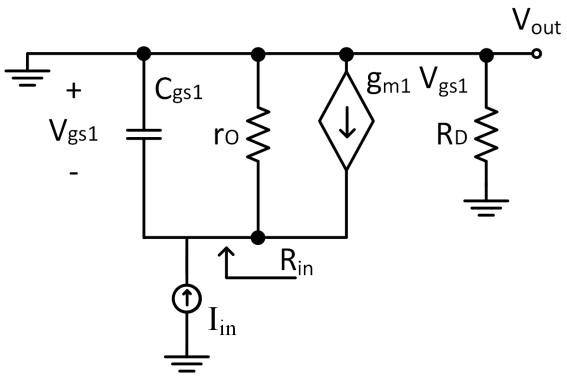



Figure 2.7: Small-signal model of common-gate.

From Figure 2.7 it is possible to calculate the input impedance expression $\left|\frac{V_{in}}{I_{in}}\right|$, $R_{in}$ [1], which results in:

$$R_{in} = \frac{r_O + R_D}{1 + (g_m + g_{mb})\, r_O} \tag{2.9}$$

If $(g_m + g_{mb})\, r_O >> 1$ and, for long channel devices operating in the saturation region, $r_O >> R_D$ is considered:

$$R_{in} \approx \frac{1}{g_m + g_{mb}} \tag{2.10}$$

Equation ( 2.10) indicates that in order to reduce the input impedance, the $g_m$ and $g_{mb}$ must be maximized.

However, the downside of this common-gate is the input noise that the load resistor makes, caused by this circuit [1].

$$\overline{I_{n,in}^2} = \overline{I_{n,M2}^2} + \overline{I_{n,RD}^2} \tag{2.11}$$

Since $\overline{I_{n,M2}^2} = 4kTgm_2$ and $gm_2 = \frac{2I_{D2}}{V_{GS2}-V_{TH2}}$, where $I_{D2}$ and $V_{GS2} - V_{TH2}$ are the drain current and gate-source overdrive voltage of $M_2$, comes:

$$\overline{I_{n,M2}^2} = 4kT\, \frac{2\, I_{D2}}{V_{GS2} - V_{TH2}} \tag{2.12}$$

In order to maintain the initial biasing conditions, operating saturation region in this case, $R_D\, I_{D2}$ must be less than $V_{DD}$ and $V_{DS2}$ must exceed $V_{GS2} - V_{TH2}$ [1]:

$$\frac{4kT}{\overline{I_{n,RD}^2}} + \frac{8kT}{\overline{I_{n,M2}^2}} < \frac{V_{DD}}{I_{D2}} \tag{2.13}$$

Equation ( 2.13) shows that if load resistor increases, the input noise contribution of $R_D$ decreases but, to maintain the initial biasing conditions, the bias current needs to increase and therefore increases the input noise contribution of $M_2$. However, instead of increasing the bias current, to maintain the transistor in saturation, the supply voltage may increase but the power consumption would also increase. In conclusion, this matter occurs because the input noise caused by the resistance load, $R_D$, is directly proportional to the bias current, $I_{D2}$ of the transistor $M_2$.

### 2.2.2 Feedback TIAs

One of the most popular feedback TIAs is a shunt-shunt feedback structure. This is composed by a resistor, $R_F$, which connects the output to the $V^-$ node, providing feedback around an ideal voltage amplifier.

From Figure ( 2.8) and $V_X = \frac{V_{out}}{-\ Openloopgain(Ad)}$ it follows that:

$$\frac{V_{out}}{I_{in}} = -\frac{Ad}{Ad+1}\, \frac{R_F}{1 + \frac{R_F C_D}{Ad+1}\, s} \tag{2.14}$$

If considered an ideal amplifier, this will result in:

$$\frac{V_{out}}{I_{in}} \approx -R_F \tag{2.15}$$

From equation ( 2.15) it is possible to conclude that increasing the resistance, $R_F$, increases the transimpedance gain.

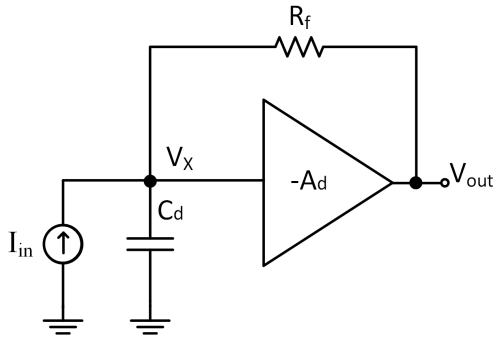



Figure 2.8: Feedback TIA.

Returning to equation ( 2.14) (closer to the real), the bandwidth of this circuit is given by the following expression [1]:

$$f_{3dB} \approx \frac{Ad+1}{2\pi R_F C_D} \tag{2.16}$$

From equation ( 2.16) it is possible to see the impact that $R_F$ has on $f_{3dB}$. If the resistance increases, the bandwidth will also decrease. Regarding to the input noise of this TIA, attention needs to be paid to the noise caused by the resistance, $R_F$, and the ampop [1].

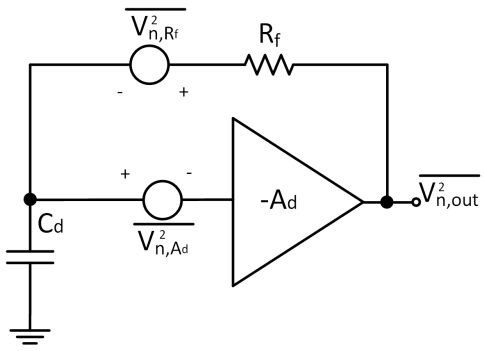



Figure 2.9: Noises sources in feedback TIA.

For the sake of simplicity the input noise of the resistance will be considered, which results in [1]:

$$\overline{I_{n,in}^2} \approx \frac{4kT}{R_F} \tag{2.17}$$

The noise from $R_F$ is therefore directly applied to the input. This is similar to the load resistor in the common-gate amplifier but the critical difference is that in the topology of Figure 2.6, the resistance, $R_F$, does not carry a bias current and therefore can be increased without increasing the supply voltage.

## 2.3 Literature Review

### 2.3.1 Transimpedance Amplifier Topologies

#### 2.3.1.1 Regulated Cascode TIA

As described in section 2.2.1, on the basic principles of a TIA open loop, a common-gate structure is usually used because it has a low input impedance. By having a low input impedance, the TIA will isolate the photodiode capacitance, preventing it from determining the bandwidth.

The ability of the common gate to isolate the large capacity of the photodiode is due to the $g_m$ of the input transistor. One of the solutions for decreasing the input impedance is to increase the bias current and for this, the sizes of the transistors are increased. However, the downside of increasing the size of the transistors is that it also increases the size of the parasitic capacities on the transistor input. To solve this problem, a Regulated Cascode (RGC) TIA [3–7] has been used.

The schematic of the Regulated Cascode is shown in the figure 2.10. The current produced by the photodiode is converted to voltage through transistor $M_1$ and resistance $R_1$, from the pre-amplifier RGC. The resistance $R_S$ is used to bias $M_1$. The transistor $M_B$ and the resistance $R_B$ operate as a local feedback to reduce the input impedance.

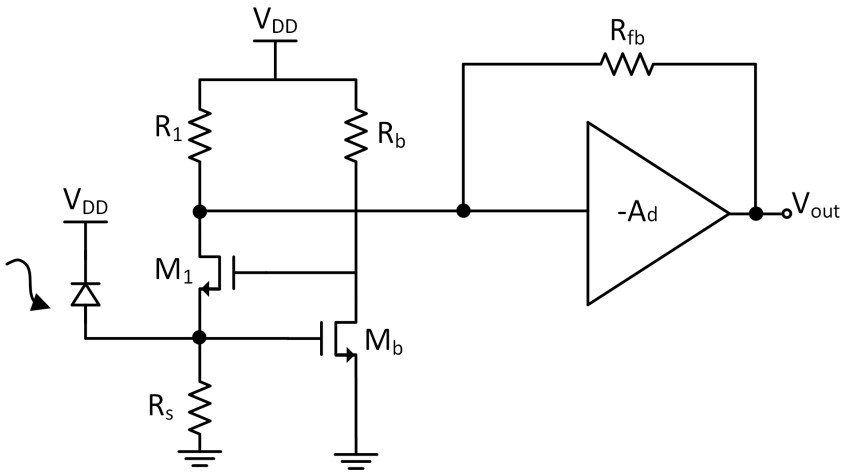



Figure 2.10: Regulated Cascode TIA.

With the body effect exclusion, caused by the transistor $M_1$, the input impedance of the RGC structure will be given by the following expression:

$$R_{in} \approx \frac{1}{g_{m1}\,(1 + g_{mb}\,R_B)} \tag{2.18}$$

From equation 2.18 and comparing it with the input impedance equation of the common gate (excluding the body effect), 2.10 from section 2.2.1, it can be concluded that the input impedance RGC structure is $\frac{1}{1+g_{mb}\,R_B}$ lower than the common gate structure.

Due to this difference, it is possible to conclude that the RGC decouples the photodiode capacitance better when determining the amplifier's bandwidth.

This topology, RGC, was used in [3] to create a 1.25 Gbps TIA. The RGC was used as a current buffer followed by a voltage gain. This TIA was able to reach 58 dBΩ with a bandwidth of 950 MHz and a photodiode capacitance of 500 fF.

This topology was also used in [4] to create a 2.5 Gbps transimpedance amplifier. With a bandwidth of 2.2 GHz and a photodiode capacitance of 500 fF, the TIA is able to achieve 55.3 dBΩ.

[5] is another application of a topology RGC to create a 5 Gbps TIA. With a gain of 52.8 dBΩ, this RGC managed to achieve a bandwidth of 4.2 GHz with a photodiode capacitance of 1 pF.

The RGC was also used in [6] to create a 3.125 Gps TIA, which is very important in the optical communication subject. This TIA was able to achieve a gain of 72 dBΩ with a bandwidth of 2.4 GHz and a photodiode capacitance of 0.5 pF.

Lastly, the RGC structure was used in [6] to create a 4 Gbps single-to-differential TIA, used as a current-amplifying. This TIA operates a bandwidth of 2.9 GHz, with a gain of 61.4 dBΩ and a photodiode capacitance of 1 pF.

#### 2.3.1.2 Feedback TIAs

This section describes a number of different feedback topologies. Figure 2.11 shows the most common feedback structures.

Figure 2.11 a) shows a shunt-shunt feedback with a common source gain stage [8]. In order to convert the input current into voltage in the common source, a resistance $R_D$ needs to be connected to the drain node. To isolate the load resistance, $R_D$, from the feedback resistance, $R_{FB}$, it is necessary to use a source follower.

Figure 2.11 b) describes the same topology but instead of using a common source gain stage, a cascode gain stage was used [9].

The common source gain stage is given by:

$$\frac{V_{out}}{Iin} = -g_m\,(R_L \| r_O) \tag{2.19}$$

The $g_m$ variable is the transconductance of the transistor, $R_L$ is the load resistance and $r_O$ is the drain to source resistance of the transistor in saturation. If $r_O >> R_L$ then:

$$\frac{V_{out}}{Iin} \approx -g_m R_L \tag{2.20}$$

The load resistance $R_L$ is equal to the load resistance $R_D$ (when transistor $M_2$ is excluded), which is represented in Figure 2.11 a). It is concluded that the gain is directly proportional to the load resistance $R_D$. However, using a cascode structure, $R_L$ is given by the common gate input impedance (excluding the transistor $M_b$ and the body effect). As shown in equation 2.10, in the previous section 2.2.1, the common gate's input impedance is given by the following formula:

$$R_{in} \approx \frac{1}{g_m} \tag{2.21}$$

From equation 2.21, since the Miller capacitance $C_{GD1}$ (gate to drain capacitance from transistor $M_1$) can be calculated as $C' = C(1 - A)$, where A is the voltage gain, it is possible to conclude that the Miller effect will decrease from:

$$C' \approx C(1 + g_{m1} R_D) \tag{2.22}$$

to:

$$C' \approx C\left(1 + \frac{g_{m1}}{g_{m2}}\right) \tag{2.23}$$

From equation 2.23, to simplify, it is considered $g_{m1} = g_{m2}$ which results in:

$$C' \approx 2C \tag{2.24}$$

Returning to Figure 2.11 b), by placing a common gate (transistor $M_2$) between the transistor $M_1$ (common source structure) and the load resistance $R_D$, it is possible to conclude from equation 2.24 that this will minimize the Miller effect.

Once the transistor $M_2$ is in series with transistor $M_1$ and $R_D$, the current remains the same, so the voltage gain is equal compared to the common source structure. The downside of the cascode structure is that it requires a higher supply voltage to maintain the same gain as the common source structure. The Miller Effect will be discussed in detail in section 2.3.4.

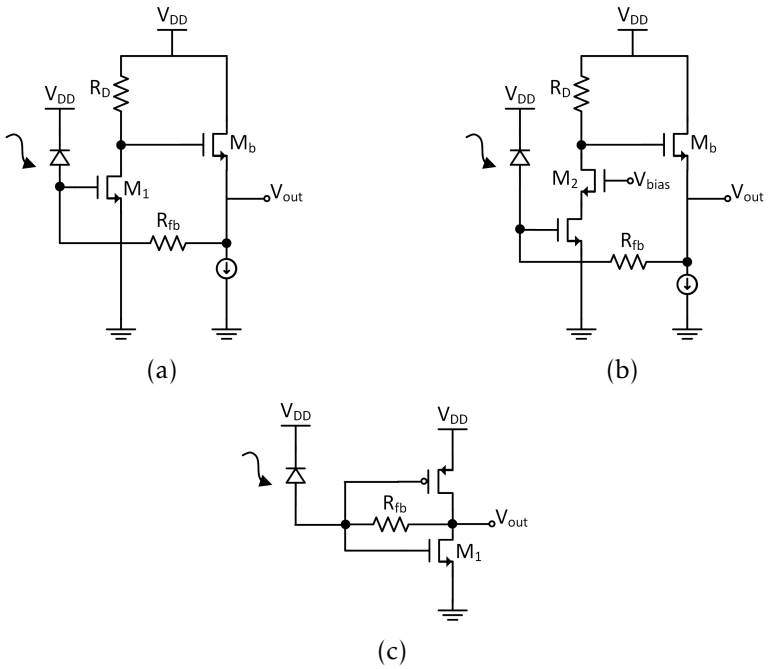



Figure 2.11: Feedback TIA Topologies a) Common Source b) Cascode c) CMOS Inverter.

Figure 2.11 c) shows a CMOS inverter [10]. Using a PMOS transistor in this structure, it is possible to achieve a higher gain. One of the downsides of this topology is that it will increase the parasitic capacitance due to the use of PMOS transistors.

The common source topology was used in [8] to create a 2.5 Gbps optical receiver. This optical receiver uses a TIA with a shunt-shunt feedback structure. The TIA achieves a gain of 59 dBΩ with a bandwidth of 5.9 GHz.

The cascode topology was used in [9] to create a 5 Gbps optical receiver front end TIA. To minimize the Miller effect, this optical receiver also uses a TIA with a shunt-shunt feedback and a cascode structure. As represented in Figure 2.11 b) [9], a source follower is used to isolate the load resistance $R_D$ and feedback resistance $R_{FB}$. This TIA was able to achieve a gain of 58.7 dBΩ with a bandwidth of 2.6 GHz and a photodiode capacitance of 200 fF.

The CMOS Inverter was used in [10] to create a 10 Gbps TIA using multiple inductive-series peaking. This technique will be discussed in detail in section 2.3.3.3.

### 2.3.2 Differential TIAs

Differential TIA, as shown in Figure 2.12, is usually employed to suppress supply voltage and substrate noise. It also increases the output swing of a single ended structure to twice.

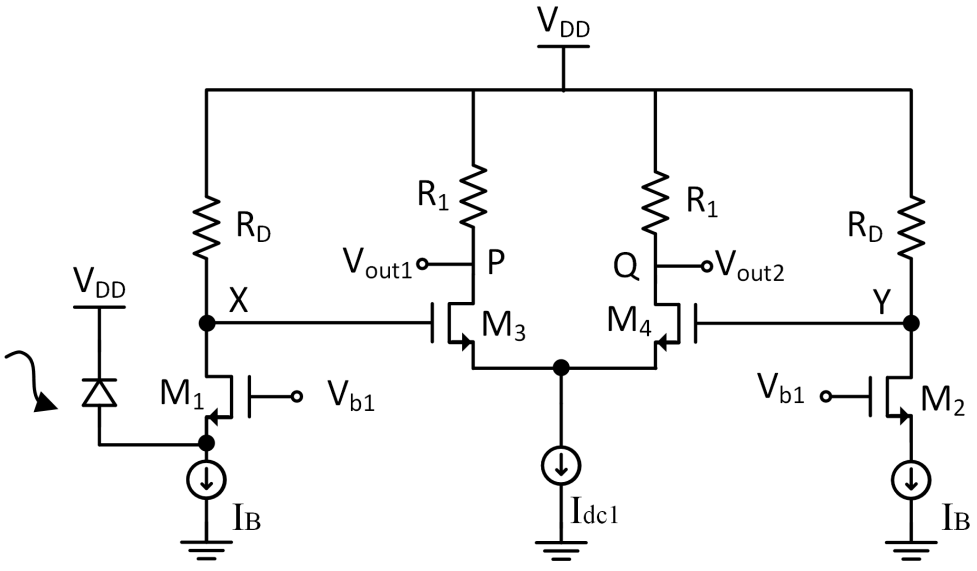



Figure 2.12: Pseudo-differential CG stage. [1]

There are three issues in this transimpedance almplifier that will be discussed [1].

Firstly, the $V_{out1}$ and $V_{out2}$ output waves are asymmetric. This occurs because node X will go through two different paths. On the one hand it operates as a common source stage (transistor $M_3$) in X-P path. On the other hand, it operates as a cascade of a source follower (transistor $M_4$) and a common gate (transistor $M_3$) in X-Q path.

Besides this, considering half of the circuit in Figure 2.12, the circuit's input referred noise is $\sqrt{2}$ times the input referred noise of a single ended transimpedance [1].

Finally, even if the TIA differential circuit is perfectly symmetric, the output swings are not fully differential. Figure 2.13 shows that when the diode, in Figure 2.12, is on, $V_{out1}$ and $V_{out2}$ follow symmetric directions. However, if the diode turns off, $V_{out1}$ and $V_{out2}$ become equal. This will make the threshold decision very difficult.

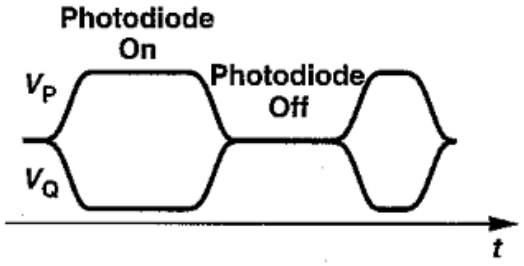



Figure 2.13: Output waveforms from a pseudo-differential CG stage. [1]

To avoid these issues, use of a fully differential TIA [11–14].

A fully differential topology was used in [11] to create a transimpedance amplifier for an optical receiver based on wide-swing cascode topology. With a gain of 66 dBΩ, this TIA managed to achieve a bandwidth of 2.4 GHz with a 19.5 mW power consumption and 1.8 V voltage supply.

This topology was also used in [12] to create a transimpedance amplifier for an optical receiver. This TIA architecture shows a tunable transimpedance gain from 40 dBΩ to 52 dBΩ, with a bandwidth of 5.6 GHz and 4.2 GHz, respectively.

In [13] a fully differential topology was also used. The TIA architecture, as shown in Figure 2.14, is loaded by linear PMOS transistors in order to acquire the largest possible bandwidth. Once the cascade of stages gain increases much faster than the bandwidth decreases, there were used four cascade stages were used to have a higher gain and higher speed operation.

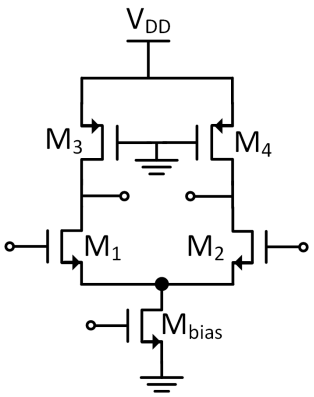



Figure 2.14: Implementation of a voltage amplifier stage [13].

Cascading differential stages is also beneficial for the common-mode rejection of the TIA [13]. This transimpedance amplifier managed to achieve a bandwidth of 2.9 GHz with a voltage gain of 73 dBΩ.

Last of all, a high-speed fully integrated optical receiver was used in [14]. The transimpedance amplifier structure achieved a voltage gain of 75.3 THzΩ with a bandwidth of 2.7 GHz and a photodiode capacitance of 1 pF. The current consumption of the full receiver was 187 mA for a supply voltage of 1.2 V [14].

### 2.3.3 Bandwidth Extension

The bandwidth of a gain stage is always limited by the capacitive load, usually at the output node that, along with $R_D$, can result in a large time constant. However, sometimes the bandwidth requirements are not attainable. For that reason, it is recommended that bandwidth extension techniques be used.

This section will present some bandwidth extension techniques.

#### 2.3.3.1 Capacitive Degeneration

Capacitive Degeneration is another bandwidth enhancement technique that consists in degenerating the transistors of a differential pair by placing a resistor and a capacitor in parallel connected between the sources of the transistors, as shown in Figure 2.15. This effective ly increases the transconductance of the circuit at higher frequencies, which compensates the voltage gain decrease due to the pole being at the output node.

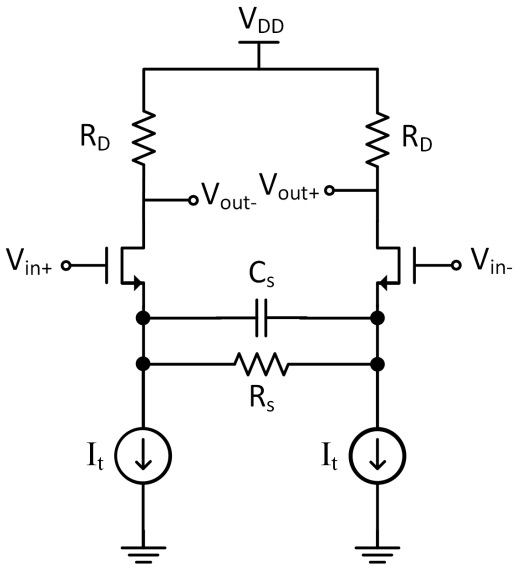



Figure 2.15: Differential pair with capacitive degeneration [1].

Applying a single-ended analysis in this circuit (considering the half circuit) it is possible to calculate the transfer function for the equivalent transconductance, $G_m$, and the corresponding poles and zeros as demonstrated in [1]:

$$G_m(s) = \frac{g_m (R_s C_s s + 1)}{R_s C_s s + 1 + g_m \frac{R_s}{2}} \tag{2.25}$$

From equation 2.25 it is possible to calculate the pole (equation 2.26) and zero (equation 2.27):

$$p = \frac{1 + g_m \frac{R_s}{2}}{R_s C_s} \tag{2.26}$$

$$z = \frac{1}{R_s C_s} \tag{2.27}$$

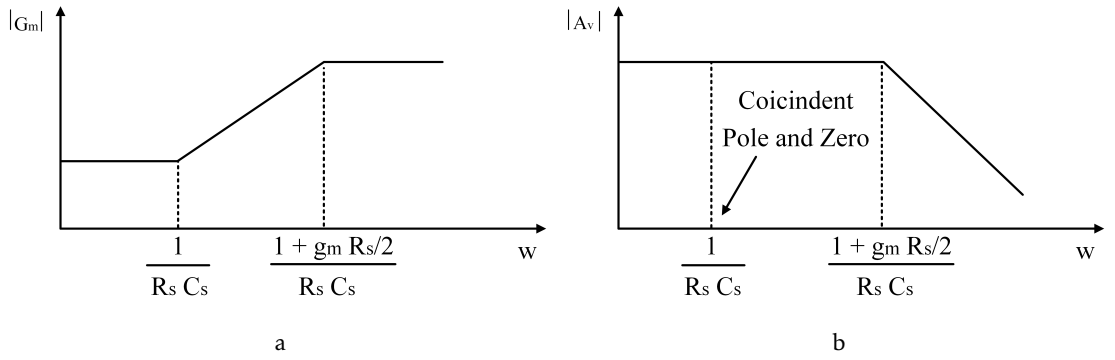



Figure 2.16: Variation of the effective transconductance, Gm, and voltage gain with frequency [1].

Figure 2.16 shows that the effective transconductance zero should be placed so as to cancel the output node pole, thereby, extending the circuit's bandwidth up to the transconductance pole. The disadvantage of this technique is that the voltage gain will decrease in order to keep the same GBW (relation between gain and bandwidth).

A capacitive source degeneration topology was used in [15] to create a 10 Gps transimpedance amplifier for an optical communication. With a gain of 51.7 dBΩ, this TIA was able to achieve a bandwidth of 8.5 GHz with an input referred noise of 4.9 pA/$\sqrt{Hz}$.

#### 2.3.3.2 Shunt Peaking

Shunt inductive peaking has been in use for a long time as a technique for extending circuit bandwidth. This method is called shunt inductive peaking because the resistor/inductor combination appears in parallel with the load capacitance. The key is to use an inductor in order to resonate the capacitance that limits the bandwidth.

Before looking at an example of a circuit that uses a Shunt inductive peaking technique, it is important first to analyze a simple common source stage without a shunt peaking, as illustrated in Figure 2.17 a).

From Figure 2.17 b) it is possible to calculate the common source gain and the pole by using equation 2.28 and equation 2.29, respectively:

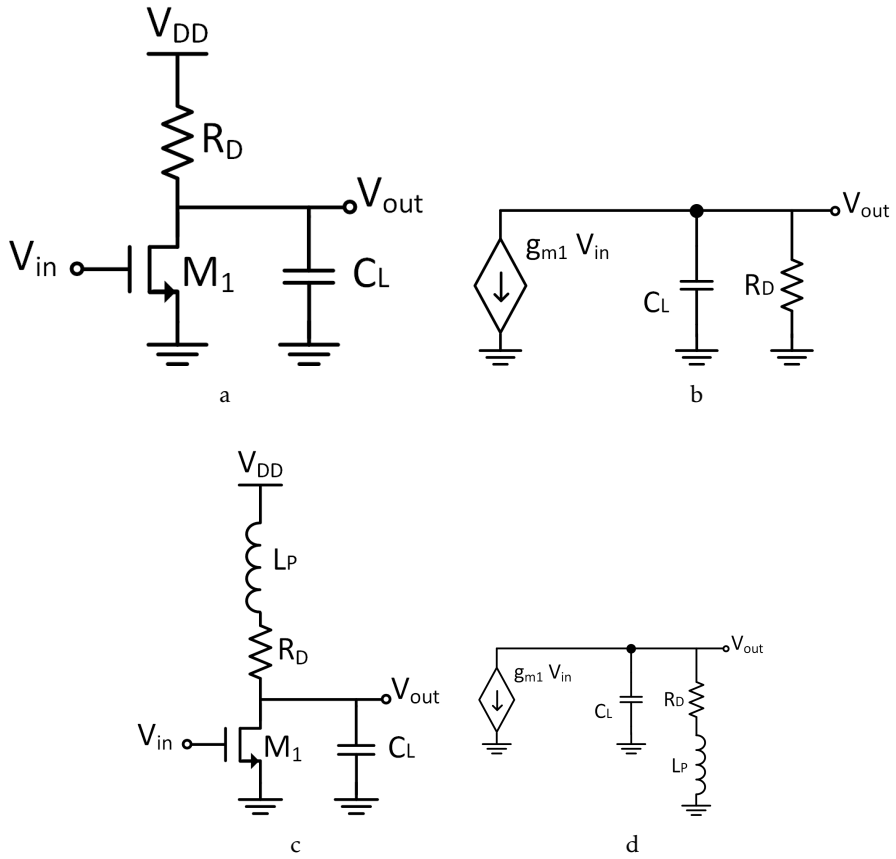



Figure 2.17: (a) Common source stage with load capacitance, (b) Small-signal equivalent of (a), (c) Common source stage with a Shunt Peaking, (d) Small-signal equivalent of (c) [1].

$$\frac{V_{out}}{V_{in}} = -\frac{g_m R_D}{1 + C_L R_D s} \tag{2.28}$$

$$p = \frac{1}{R_D C_L}\ rad/s \tag{2.29}$$

From equation 2.29, assuming that this is the dominant pole in the system, the bandwidth of the amplifier is determined by the $R_D C_L$ time constant.

To improve the bandwidth, an inductor $L_P$ was placed in series with the load resistance $R_D$, as shown in Figure 2.17 c).

Applying $\frac{V_{out}}{V_{in}}$ in Figure 2.17 d), results in:

$$\frac{V_{out}}{V_{in}} = -\frac{g_m (R_D + L_P s)}{1 + C_L R_D s + C_L L_P s^2} \tag{2.30}$$

From equation 2.28 and 2.30 it is now possible to make a bode diagram of the common source structure gain and make a comparison between the CS structure with and without shunt peaking.

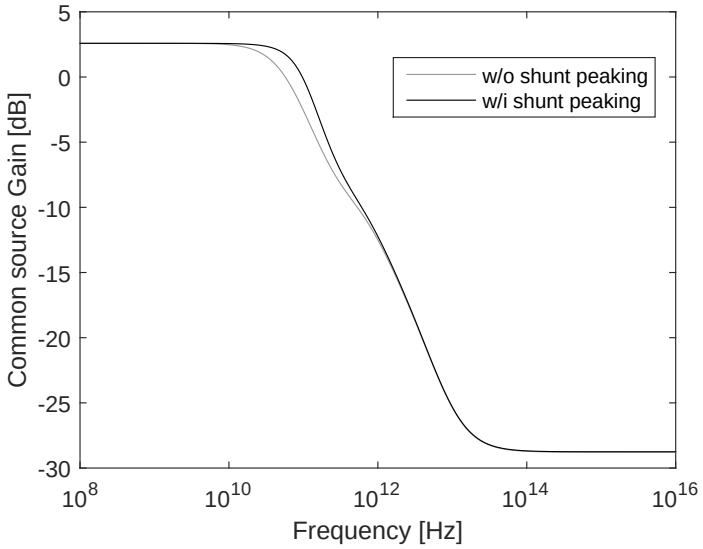



Figure 2.18: Bode Diagram of a CS amplifier with and without the shunt peaking technique.

From Figure 2.18, it was concluded that including a shunt inductive peaking to cancel the load capacitance extends the bandwidth. Intuitively, when the frequency increases, the impedance looking into the load resistor $R_D$ increases and for that reason it will let more current flow to charge the capacitance.

The downside of using this technique is that adding an inductor will also add parasitic capacitances so that it is important to minimize the inductor's size.

Many TIAs have been using this inductive peaking technique [16–18].

[16] describes a 10 Gps fully integrated optical receiver where shunt peaking is used. This circuit achieved 87 dBΩ with a bandwidth of 7.6 GHz. Operating under a 1.8 V supply, the power dissipation is 210 mW.

Shunt inductive peaking was also used in [17] to create a 2.5 Gps ultra-low-power TIA made in 90nm CMOS technology. This transimpedance amplifier operates a bandwidth of 2.68 GHz with a gain of 54 dBΩ and total power consumption of 781.37 $\mu$W.

Lastly, shunt inductive peaking technique was also used to create a transimpedance amplifier for 10 Gbps optical application [18]. The TIA consumed 18 mW to achieve a voltage gain of 59 dBΩ with a bandwidth of 8.6 GHz in the presence of a 0.15 pF photodiode capacitance from a 1.8 V supply.

#### 2.3.3.3 Series Inductive Peaking

Section 2.3.3.2 looked at the shunt peaking technique. However, it is also possible to use inductive peaking in series with load capacitance.

Another bandwidth extension technique is the Series Inductive Peaking. Unlike the Shunt peaking, this technique involves placing an inductor $L_P$ in series with the load capacitance $C_L$. A resonant circuit is created to pull more current into the load capacitance,

inscreasing the bandwith and, consequently, improving the speed.

The load capacitance receives more current because when the frequency increases near the resonance frequency, the impedance looking into the load capacitance will be reduced, as shown in equation 2.31.

$$\begin{aligned} Z_{equivalent} &= s\,L_P // (s\,C_L)^{-1} \\ &= \frac{s\,L_P}{s^2\,L_P\,C_L + 1} \end{aligned} \tag{2.31}$$

In order to maximize the flat frequency response or group delay, the inductor $L_P$ can be adjusted. A more detailed analysis to adjust the inductor in shunt peaking and series inductive peaking techniques will be discussed in section 2.3.3.4.

Series inductive peaking has been used, as mentioned in section 2.3.1.2, to create a 10 Gps transimpedance amplifier in 0.18 $\mu$m CMOS technology in [10]. As shown is Figure 2.19, a TIA is used as a multi-stage amplifier with a series inductive peaking technique in each stage, in order to increase the bandwidth and therefore the circuit speed.

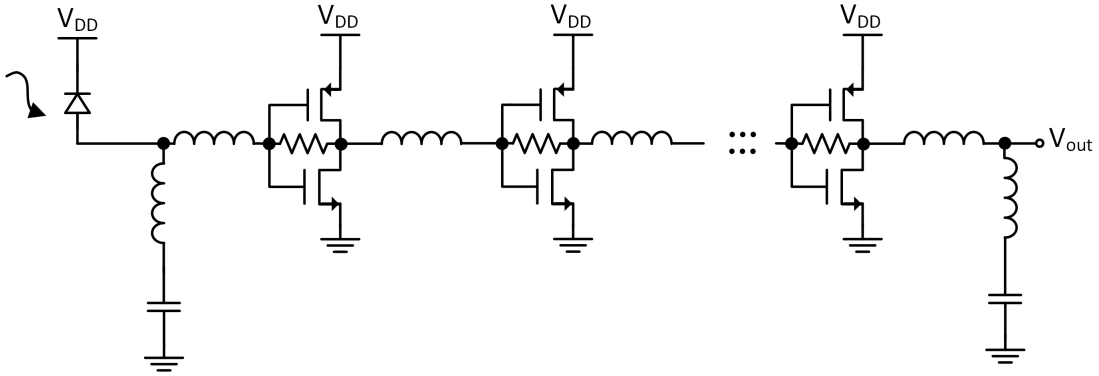



Figure 2.19: Transimpedance amplifier using series inductive peaking.

Usually, when a cascade topology with PMOS transistor is used, the bandwidth is frequently degraded because of the large parasitic capacitances added by PMOS transistor.

Another reason to reduce the bandwidth is because the series inductive peaking is not used in circuits. Thus, the usage of inductors, as shown in Figure 2.19, makes possible to absorb the parasitic capacitance's effect and therefore the bandwidth increase.

It was performed a simulation in [10] in order to conclude that the usage of a five stage amplifier makes possible to increase the bandwidth up to three times when using the series inductive peaking technique.

The transimpedance amplifier in [10] achieved a gain of 61 dBΩ with a bandwidth of 7.2 GHz.

#### 2.3.3.4 Shunt vs Series Peaking

After studying the two techniques used to increase the bandwidth, shunt inductive peaking and series inductive peaking in section 2.3.3.2 and 2.3.3.3 respectively, it is important

to make a comparison between these two implementations in three characteristics:

- Maximum Bandwidth;
- Maximally Flat Frequency Response;
- Maximally Flat Group Delay;

In order to compare the above characteristics, the three circuits, shown in Figure 2.20, will be analyzed.

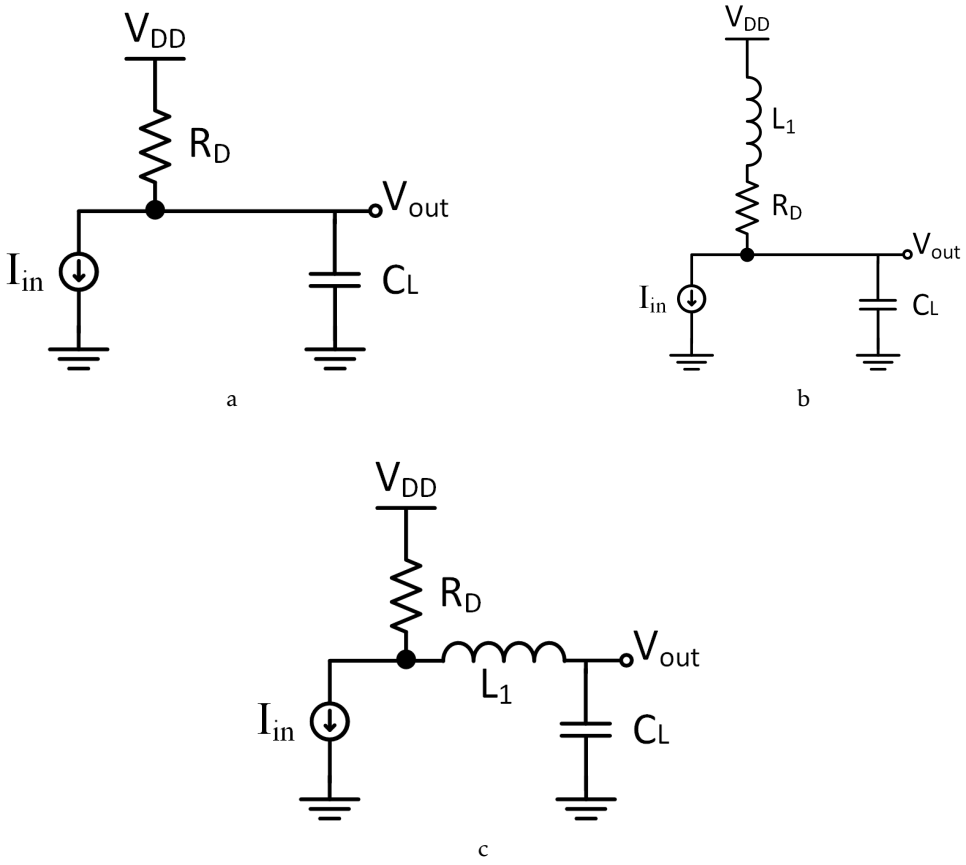



Figure 2.20: Various Methods of Inductive Peaking a) RC Circuit Without Inductive Peaking b) Shunt Inductive Peaking c) Series Inductive Peaking.

Figure 2.20 a) shows a circuit implemented by placing a load resistance $R_D$ in parallel with a load capacitance $C_L$. The load resistance $R_D$ is used to create a pole with the load capacity. Assuming that it is the dominant pole, the bandwidth is determined by the time constant $(R_D\, C_L)^{-1}$.

In order to increase the bandwidth it is possible to decrease the resistance $R_D$. However, this will increase the input noise, as already mentioned in section 2.1.1.

Due to this limitation the intention is to use inductive peaking techniques, as shown in Figure 2.20 b) and Figure 2.20 c).

The difference between the Figure 2.20 a) and Figure 2.20 b) is that the latter an inductor $L_1$ in series with the load resistance $R_D$. This technique, as mentioned earlier, is known as shunt peaking because the inductor is in parallel with the load capacitance.

Finally, the difference between the Figure 2.20 a) and Figure 2.20 c) is that the latter an inductor $L_1$ in series with the load capacitance $C_L$ to generate the resonant circuit. This technique, also mentioned earlier, is known as series inductive peaking.

Based on the techniques previously studied, it is possible to conclude that even if the size of the inductor is increased, the circuit's bandwidth will always reach a point where bandwidth growth is saturated and it will also cause an unwanted peak not only in frequency response but also in group delay.

Consequently, in [19], it is possible to calculate the value of the inductor $L_1$ in order to maximize the flat frequency response, maximize the flat group delay or maximize the bandwidth. The inductor $L_1$ is calculated as follows:

$$L_1 = m R_D^2 C_L \tag{2.32}$$

Where m is a numerical value that determines the type of response from the circuit and its value is given in Table 2.1 [19].

Table 2.1: Values of m for Shunt and Series Inductive Peaking

| Response | Shunt Inductive Peaking | Series Inductive Peaking |
|---|---|---|
| Maximally Flat Frequency Response | 0.4 | 0.5 |
| Maximally Flat Group Delay | 0.3 | 0.333 |
| Maximum Bandwidth | 0.76 | 0.53 |

In order to compare the bandwidth increase, using inductive shunt peaking and series inductive peaking, it is possible to observe the frequency response and step response presented in Figure 2.21 for each type of peaking.

Figures 2.21 a) and b) show the frequency response and step response that maximize the flat frequency response of each circuit. It is possible to conclude that the shunt inductive peaking technique increased 1.73 times more bandwidth than the unmodified RC circuit. It should also be noted that the series inductive peaking technique increased 1.42 more bandwidth than the unmodified RC circuit.

Figures 2.21 c) and d) show the frequency response and step response that maximize the flat group delay of each circuit. With the maximization of the flat group delay it is possible to conclude that the shunt inductive peaking technique had an enhancement of 1.58 compared to the unmodified RC circuit. On the other hand, the series inductive peaking technique increased 1.39 more bandwidth than the original circuit. It should also be noted that, in this circuit, both the techniques used to increase the bandwidth ran out of overshoot, i.e. managed to reach the desired value more quickly.

Finally, Figures 2.21 e) and f) show the frequency response and step response that maximize the bandwidth of each circuit. It is possible to conclude that the shunt inductive peaking technique increased 1.88 times more bandwidth than the original RC circuit.

However, the series inductive peaking technique has not improved much compared to the results obtained in the flat frequency response study. The downside of maximizing the bandwidth is that an unwanted peak appears near to the frequency response and therefore an overshoot in step response, when using these techniques (shunt and series inductive peaking).

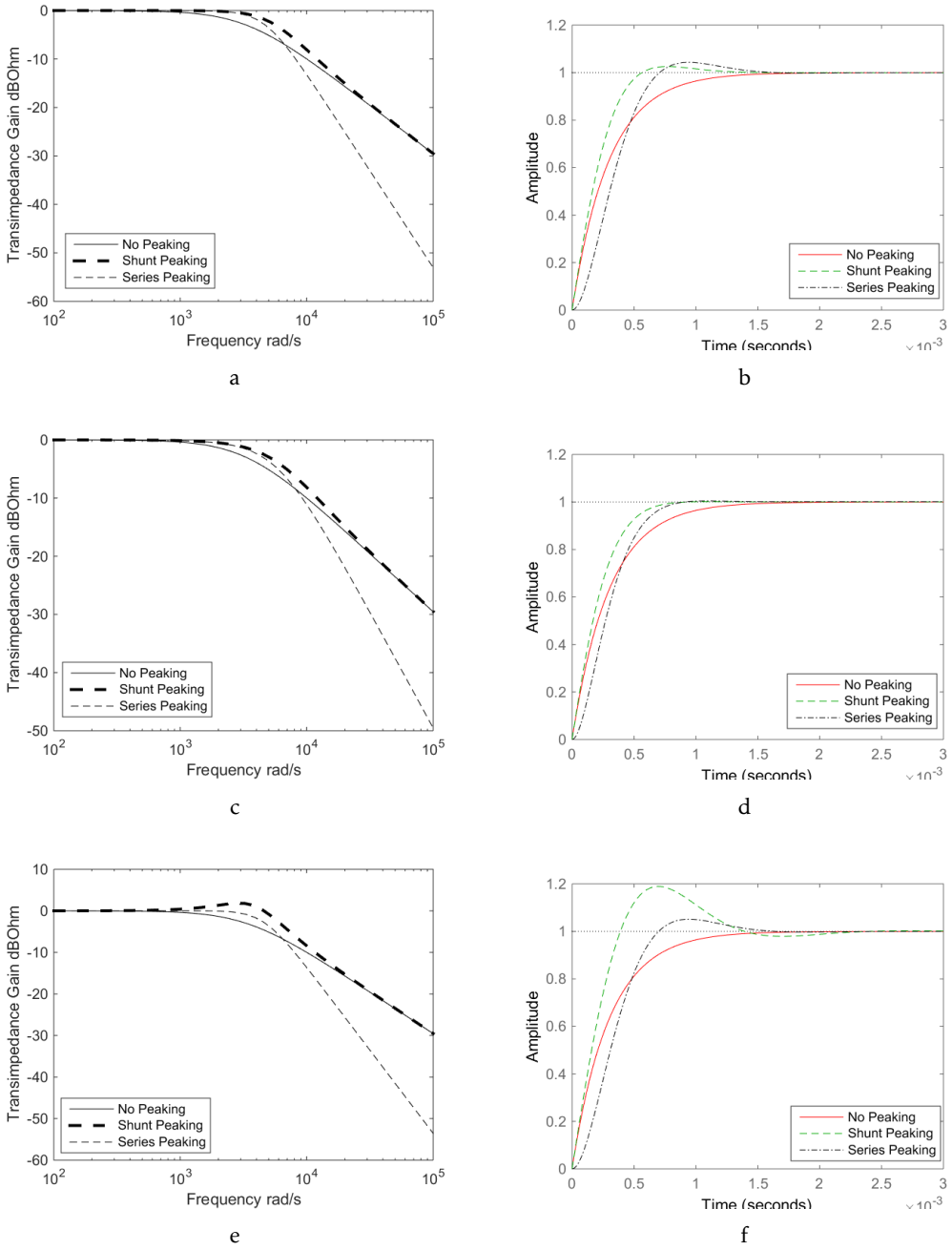



Figure 2.21: Bandwidth Improvement Using Shunt and Series Inductive Peaking a) and b) Maximally Flat Frequency Response c) and d) Maximally Flat Group Delay e) and f) Maximum Bandwidth.

### 2.3.4 Miller Effect

As mentioned in section 2.3.1.2, the Miller effect is a very important concept that needs to be understood, together with the solutions for decreasing it.

From Figure 2.22 it is possible to conclude that there is an overlap between the gate and the drain which creates parasitic capacitances between them. In short gate length devices, this overlap capacitance is significant compared to other parasitic capacitances and so it is fundamental to consider that.

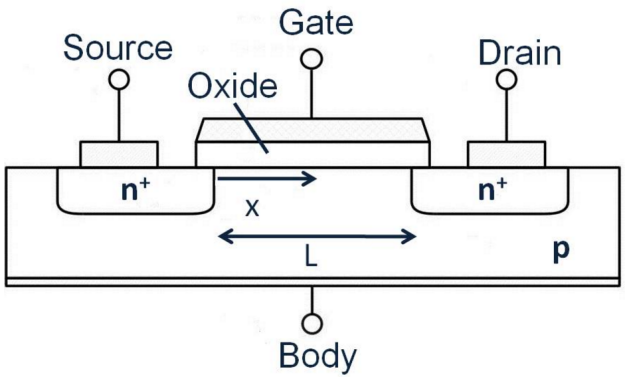



Figure 2.22: Transistor structure.

In a common source circuit, Miller's capacitance is the name given to the parasitic capacitance between the gate and the drain, $C_{GD}$,because it is the capacitance that connects the input to the output, as shown in Figure 2.23.

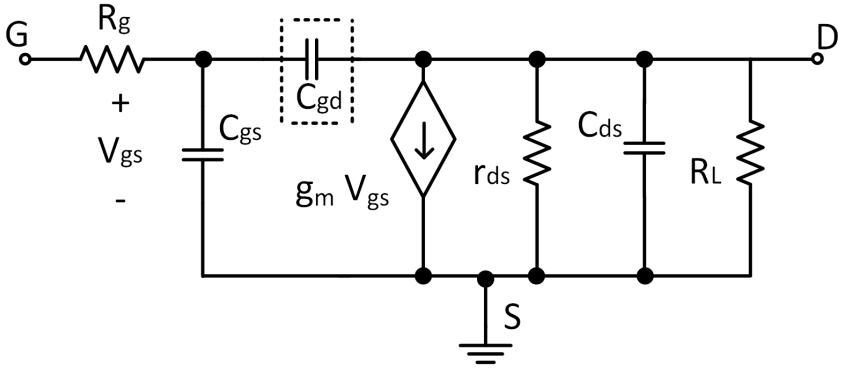



Figure 2.23: Transistor structure.

Miller's theorem, in [20], says that it is possible to replace the $C_{GD}$ by two shunt capacitances in the input and output, as shown in Figure 2.24.

Figure 2.24 shows that a series admittance is connected between two points with a known voltage gain of K.

In order to replace the admittance by two shunt admittances in input and output, it is necessary to consider two currents, $I_1$ and $I_2$, that remain the same throughout the whole process.

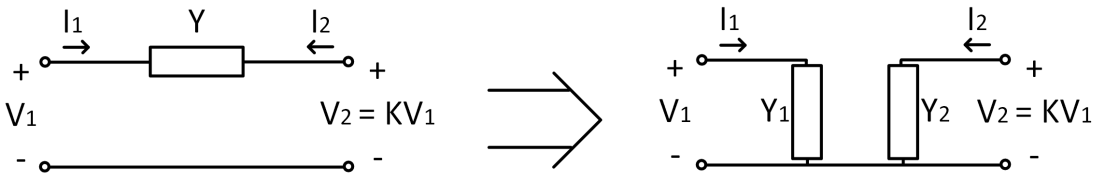



Figure 2.24: Miller Theorem.

First of all it is important to know the equations capable of determining the currents $I_1$ and $I_2$, as shown on the left side of the Figure 2.24:

$$I_1 = (V_1 - V_1 K)\, Y \tag{2.33}$$

$$I_2 = (V_1 K - V_1)\, Y \tag{2.34}$$

Emphasising V1, results in:

$$I_1 = V_1 (1 - K)\, Y \tag{2.35}$$

$$I_2 = V_1 (K - 1)\, Y \tag{2.36}$$

So it is possible to equate 2.35 and 2.36 to the currents, as shown at the right side of the Figure 2.24:

$$V_1 (1 - K)\, Y = V_1\, Y_1 \tag{2.37}$$

$$V_1 (K - 1)\, Y = K\, V_1\, Y_2 \tag{2.38}$$

The shunt admittances' values can be determined by the following expressions:

$$Y_1 = Y (1 - K) \tag{2.39}$$

$$Y_2 = Y (1 - \frac{1}{K}) \tag{2.40}$$

From Equations 2.39 and 2.40, it is concluded that, with an increase in the circuit's $K$ gain, the input impedance will also increase and, in turn, the frequency of the pole will decrease. The bandwidth will therefore decrease. However, as mentioned in section 2.3.1.2, there are techniques capable of decreasing the Miller effect.

### 2.3.5 Comparison of published TIAs

Table 2.2 shows an overview of all the TIAs studied in the course of this report. The black circles indicate the best performances for specific design parameters of the circuits.

Table 2.2: Comparison of existing TIAs

| Reference | Process | Bit Rate (Gb/s) | ZT (dBΩ) | BW (GHz) | Spot noise (pA/$\sqrt{Hz}$) |
|---|---|---|---|---|---|
| [4] | 0.6 $\mu$m | 2.5 | 55.3 | 2.2 | - |
| [6] | 0.18 $\mu$m | 3.125 | 72 | 2.4 | - |
| [7] | 0.18 $\mu$m | 4 | 61.4 | 2.9 | 26.8 |
| [9] | 0.18 $\mu$m | 5 | 58.7 | 2.6 | 13 |
| [10] | 0.18 $\mu$m | 10 | 61 | 7.2 | 8.2 |
| [11] | 0.18 $\mu$m | 2.4 | 82 | 2.4 | 36 |
| [13] | 0.13 $\mu$m | 4.5 | 73 | 2.9 | - |
| [15] | 0.18 $\mu$m | 10 | 51.7 | 8.5 | 10 |
| [16] | 0.18 $\mu$m | 10 | 87 | 7.6 | - |
| [17] | 90 nm | 2.5 | 54 | 2.68 | 4.9 |
| [18] | 0.18 $\mu$m | 10 | 59 | 8.6 | 25 |

### 2.3.6 Power-on Reset and Brown-Out Reset

Power-on-reset (POR) circuits are an essential component of the System on a Chip Integrated Circuit (SOC IC).

The primary function of a POR circuit is to control and initialize critical nodes in analogue and digital circuits. The circuit should issue a reset signal keeping the system in the reset state until the power supply reaches a steady-state level (or at least a level at which the circuits are able to operate).

This signal is then used to initialize various nodes in analog and digital circuitry surrounding the POR circuit.

The POR signal stays at logic 1 (Reset) as long as the power supply is below a certain voltage, also called Brown-Out (BO) voltage [21]. When BO reaches the supply voltage or a certain voltage that makes the circuit work properly, the POR output is changed to logical level 0.

During normal operation, sudden disturbances in the power supply line (heavy current drawn by the load) can also lead the circuit to malfunction (brown-out event). In order to ensure proper operation after the brown-out event, the reset signal should be generated to bring all circuits to a well defined state. The circuit responsible for monitoring power supply line and generating reset signal is known as Brown-Out Reset (BOR) circuit.

Figure 2.25 shows the time relation between the POR & BOR and the supply voltage, $V_{dd}$.

A POR topology has been used in [21] to work with a supply voltage between 1.8 V and 5.5 V. This architecture generates a Reset signal from a predetermined delay that occurs when the supply voltage crosses a predefined threshold voltage. This delay can be increased or decreased via programmable fuses.

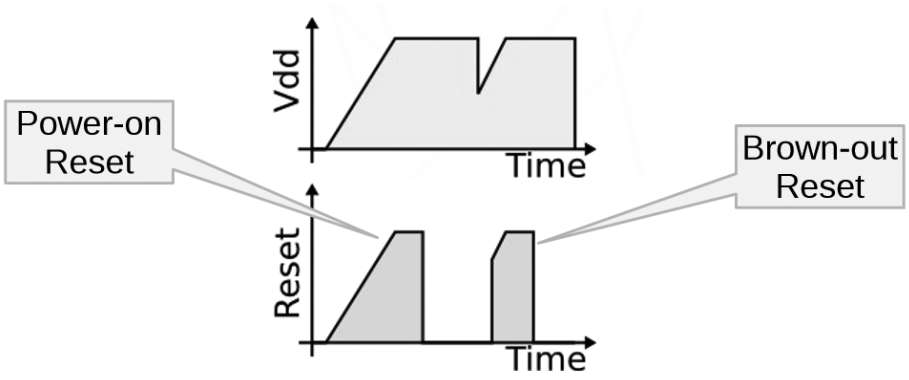



Figure 2.25: POR and BOR methodology.

## 2.4 Radiation Effects on CMOS Technology

In order to use microelectronics in high-energy physics experiments they need to be hardened against the radioactive environment in which they are placed. It is therefore of the greatest importance to study the radiation effects in modern CMOS process.

These effects are known as Total-Ionizing Dose (TID) Effects and are caused by continuous exposure to radiation and are characterized by permanent changes in electronic devices.

### 2.4.1 TID Effects on Modern CMOS Process

TID radiation effects on CMOS devices are mainly related to the charging in the oxides and the consequent effects of this charging. These phenomena have a large impact, especially, in the gate oxides (possibly causing deterioration of some of the transistor performance parameters), in the transistor edges (possibly causing leakage current between the adjacent transistors) and in the isolation oxides (possibly resulting in an inter-device isolation loss) [22].

#### 2.4.1.1 Gate Oxide Effects

The ionizing radiation effects rely on electron-hole pairs formed in the oxide. When a high-energy particle impacts a solid, it ionizes the lattice atoms forming these pairs at a constant rate, while the particle loses energy as it passes through it. Part of the pairs recombine themselves in the gate oxide while the remaining electrons and holes take opposite directions in the applied electric field [22].

Electrons move towards the gate. Due to their high mobility in the $SiO_2$ the gate contact is quickly outpaced and no electrons remain in the gate oxide. On the other hand, holes are trapped in the oxide gate (they have low effective mobility), creating a net positive charge and others will move to the Si/SiO2 where they create an interface trap, as shown in Figure 2.26 d). The hole transport process is highly dispersive in time, being able to occur over many years after a radiation pulse [22].

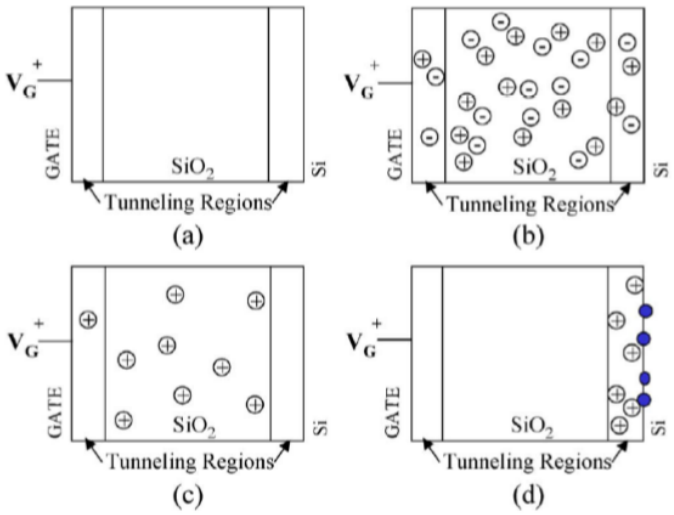



Figure 2.26: Charge distribution in a gate oxide at three times after exposure to a pulse of irradiation at t = 0 for a thick gate oxide. (a) t = $0^{-}$ , (b) t = $0^{+}$ , (c) t = $0^{++}$ , and (d) t>> $0^{++}$ [22].

While the oxide trapped charge is always positive, the interface trapped charge state depends on the bias conditions and the device type. The interface states act as negative charges in the gate-oxide of a NMOS transistor, or positive charges in the gate-oxide of a PMOS transistor [22].

The introduction of these new charge sources can affect the device's performance. The trapped charge in the gate oxide and/or at the $Si/SiO_2$ interface induces a shift in the CMOS transistor threshold voltage $\Delta V_T$.

#### 2.4.1.2 Radiation-Induced Leakage Current

Previously introduced in section 2.4.1.1, electron-hole pairs are created along the track of the impinging particle. The positive charge trapped in the field oxide due to ionizing radiation, in a NMOS device, can invert the underlying P-doped region and form a conducting channel between the source and drain terminals as depicted in Figure 2.27 a) [22].

This process results in two conductive paths as shown in Figure 2.27 b), resembling parasitic transistors in parallel with the main device. This also results in a shift in the effective threshold voltage, sometimes large enough to create a source-drain current in the transistor at off state ($V_{GS} = 0$) as shown is Figure 2.28.

Another contribution from radiation-induced leakage currents is the loss of inter-device isolation. This can result in signal corruption, reduced margins and additional supply current.

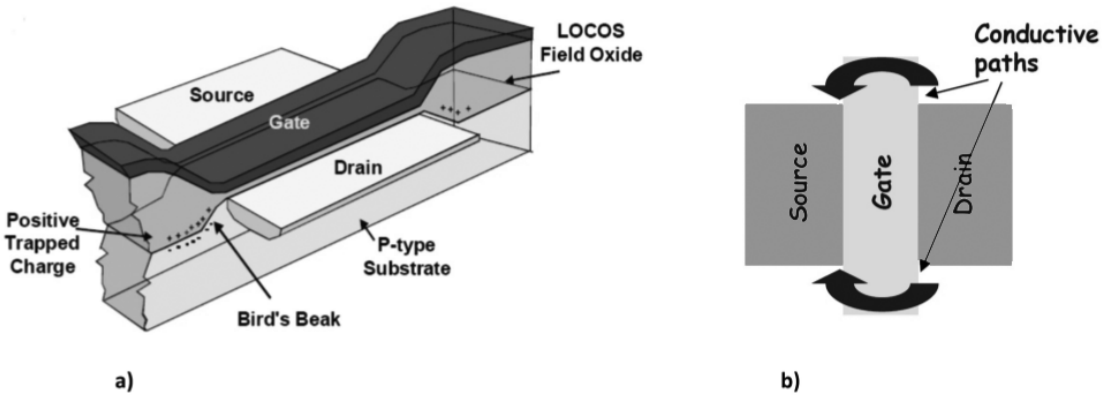



Figure 2.27: a) Radiation-induced hole trapping in thick isolation field oxides driving the parasitic field oxide transistor into inversion. b) Parasitic conductive paths [23].

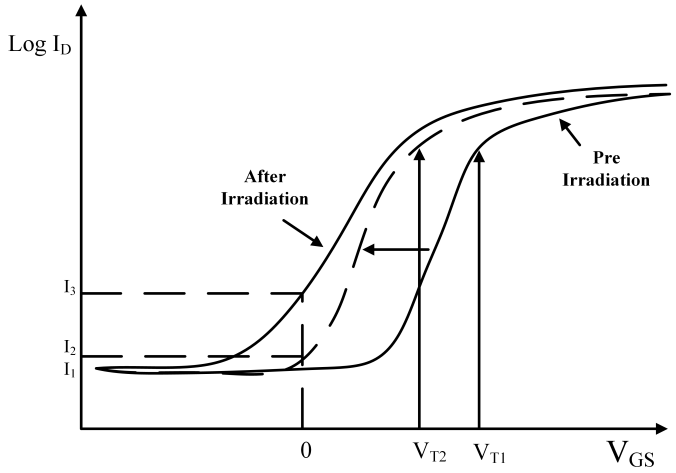



Figure 2.28: Increase of the sub-threshold current in an n-channel transistor given by a decrease in the threshold voltage [24].

#### 2.4.1.3 Hardness-by-Design Techniques

Hardness-by-design is a method for designing radiation-tolerant microelectronic components without the use of special manufacturing processing techniques (hardening-by-process). In this section, some design techniques used to mitigate TID effects will be addressed.

In order to eliminate radiation-induced edge leakage, introduced in section 2.4.1.2 and based on conductive parasitic paths between a device source/drain, an enclosed layout can be used, as shown in Figure 2.29, and hence, there will be no edge leakage. [22].

Other technique is the usage of a p+ diffusion ring preventing the inversion of the p-substrate at the interface between the field oxide, as shown in Figure 2.30.

This structure avoids the inversion of the p+ subtract because the electric field is

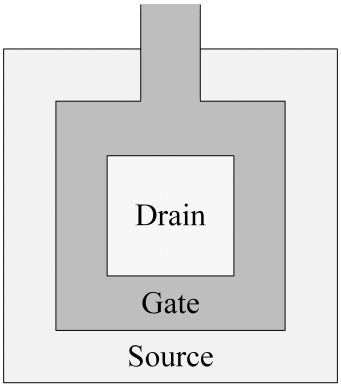



Figure 2.29: CMOS transistor with an enclosed layout [23].

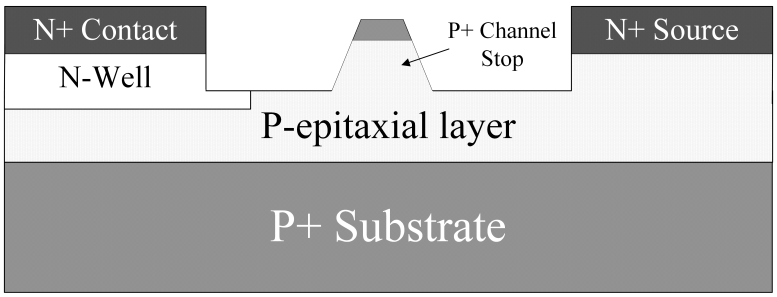



Figure 2.30: Cross-section of a CMOS process with a p+ channel stop designed into the FOX isolation [22].

bigger since the distance increases (the local threshold voltage is increased).

Chapter 3

# Proposed POR-BOR Circuit

As previously discussed in section 2.3.6 of chapter 2, one of the parts of this project is to design a circuit that produces a reset signal when the supply voltage falls below a reference voltage.

It starts with the description of the block and in general was conceived and designed to meet all of CERN's requirement, i.e. that it should:

- Work for wide temperature range (from -20 to 100 ºC) and all process corners;
- Be low power (< < 1mW after reset is released);
- Provide 3 active high reset signals for redundancy due to radiation effects (Triple modular Redundancy used in lpGBTX);
- Ensure a proper reset of the chip for supply voltage rise times from 1$\mu$s to 10ms;
- Have an external reset pin;
- Have a brownout detection circuit configured with different reference voltages, e.g. 0.7V to 1.05V;
- Be designed in TSMC 65nm 6M technology;

A detailed explanation is also provided of the function of each sub-block (originating the POR) and why they were used.

Finally, circuit simulations (POR-BOR) are provided in all corners, from -20 ºC to 100 ºC, along with comparisons of results obtained in the schematics and layout (of each sub-block through to the full block).

## 3.1 Proposed Circuit

As mentioned above, in line with CERN's requirements, a circuit that performs the intended function has been designed.

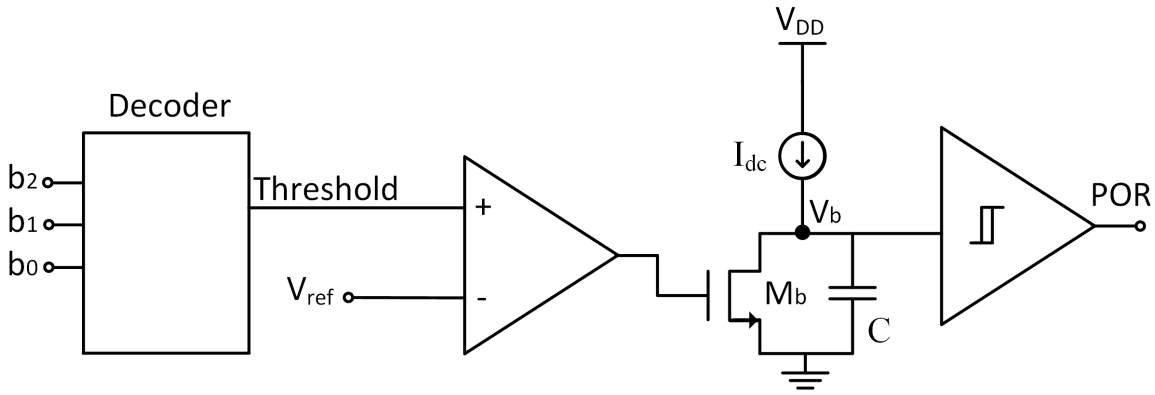



Figure 3.1: Top level schematic POR-BOR. The NMOS with undefined bulk have their bulk connected to ground.

Figure 3.1 shows the simplified schematic of the proposed Power-on Reset and Brown-Out Reset.

It is important to understand the general functioning of the circuit. When a power supply is switched on, the supply voltage gradually rises and the current generator remains off. So the capacitor voltage $V_b$ is low. During this period, the output of the Schmitt Trigger (POR) tracks the supply voltage $V_{dd}$. When the $V_{dd}$ exceeds the threshold voltage of the current generator, the current generator $I_{dc}$ starts to charge capacitance C. When $V_b$ exceeds the high switching point of the Schmitt Trigger, the POR signal goes lower and so the reset phase is over.

The duration of the reset signal is set by the current $I_{dc}$, the capacitance C and the the high switching point of the Schmitt Trigger.

If the supply voltage drops, the current generator $I_{dc}$ switches off and the $V_b$ is very slowly discharged (only by leakage currents). In order to speed up the circuit response to brown-out events, a brown-out detector is added. It compares the supply voltage with a voltage reference and if the supply voltage is too low, the transistor $M_b$ is opened, shorting the capacitor C.

Once the capacitance voltage $V_b$ drops below the low switching point of the Schmitt Trigger, the Schmitt Trigger turns one and generates the reset pulse. When the supply voltage is high enough, the transistor $M_b$ is opened, the process of charging the capacitance C starts and the circuit behaves as during the power-on process.

### 3.1.1 Current Source

Figure 3.2 shows the current source chosen to charge the capacitor.

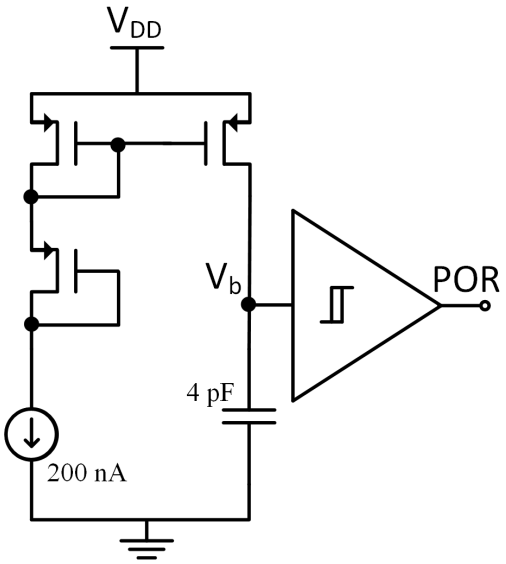



Figure 3.2: Current source with Schmitt Trigger. The PMOS with undefined bulk have their bulk connected to $V_{dd}$.

In order to obtain an acceptable capacitor charging time (between 10$\mu$s to 30$\mu$s with a capacitor value of 4pF) and to reduce the power of the circuit, a current source of 200nA has been used, because:

$$\begin{aligned} V_b &= \int_0^T \frac{ic(t)}{C}\,dt \ \ (V) \\ &= \frac{I}{C}\,t \ \ (V) \end{aligned} \tag{3.1}$$

Replacing $I = 200nA$, $C = 400pF$ in ( 3.1) and $V_b = 0.95$ results in:

$$\begin{aligned} 0.95 &= \frac{200\,10^{-9}}{4\,10^{-12}}\,t \ \ (V) \\ t &= 18 \ \ (\mu s) \end{aligned} \tag{3.2}$$

From equation ( 3.2) it was concluded that the 4pF capacitance needs only 18 $\mu$s to reach 0.95V.

Once this block (POR-BOR) works in a time interval between 1$\mu$s to 10ms, the 18$\mu$s becomes an acceptable result for the capacitor's charging time.

### 3.1.2 Decoder with 3 bits and Threshold Voltage

CERN has requested a block that would be able to generate multiple reference voltages from the power supply $V_{dd}$ with 3 input bits.

It is therefore imperative to create a decoder with 3 input bits, as shown in Figure 3.3.

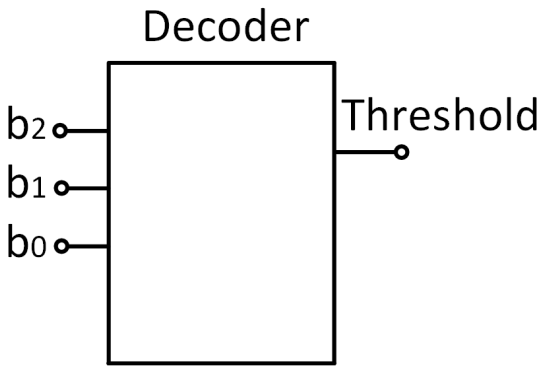



Figure 3.3: Top level decoder with 3 input bits.

Table 3.1: Decoder with 3 input bits Logic.

| | **S3** | **S2** | **S1** |
|---|---|---|---|
| **D1** | 0 | 0 | 0 |
| **D2** | 0 | 0 | 1 |
| **D3** | 0 | 1 | 0 |
| **D4** | 0 | 1 | 1 |
| **D5** | 1 | 0 | 0 |
| **D6** | 1 | 0 | 1 |
| **D7** | 1 | 1 | 0 |
| **D8** | 1 | 1 | 1 |

To design the decoder and following the logic as shown in table 3.1, some background knowledge of logic is required.

#### 3.1.2.1 Logic Gates

Logic gates or logical circuits are devices that operate one or more logical input signals to produce an output signal. In the output there are 2 possible outcomes:

- Signal presence or "1" (true);
- Absence of signal or "0" (false);

The decoder, is implemented by using combinations of NAND and NOT gates. Figures 3.4 show the simplified schematic of these gates. All the logic gates are designed with the minimum length (L) and width (W) allowed by the technology, in order to reduce the area and power dissipation.

Figures 3.4 a) and b) show the table of truth by using a NAND and a NOT gates, respectively.

With this information it is now possible to implement a decoder by using NAND and NOT gates as shown in Figure 3.5.

From Figure 3.5 it is possible to enable 8 different reference voltages due to the 8 outputs of the decoder.

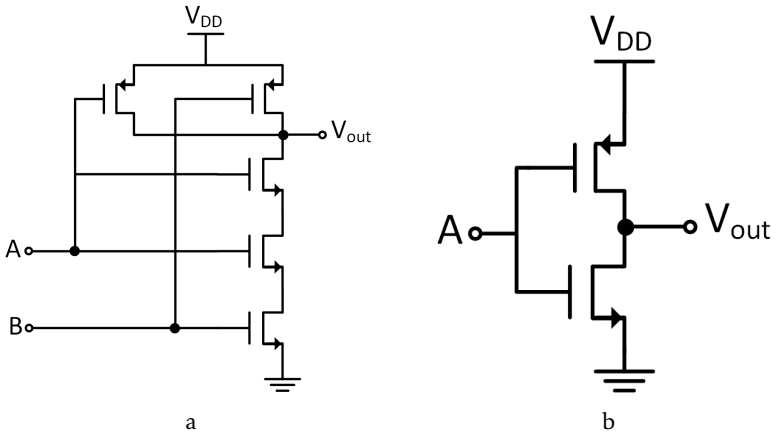



Figure 3.4: Simplified schematic of the logic gates used in the decoder circuit. The PMOS and NMOS with undefined bulk have their bulk connected to $V_{dd}$ and ground, respectively.

Table 3.2: Left - Table of Truth NAND gate. Right - Table of Truth NOT gate.

| b1 | b0 | Result |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

| b0 | Result |
|---|---|
| 0 | 1 |
| 1 | 0 |

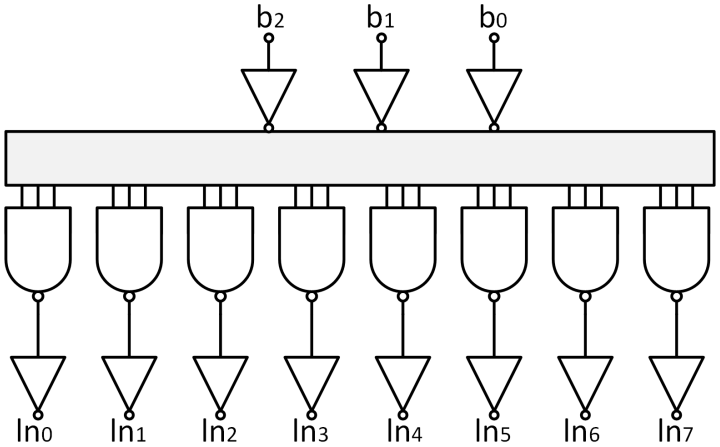



Figure 3.5: Decoder with 3 input bits.

Table 3.3: Depending on the input bits, the reference voltage changes.

| b2 | b1 | b0 | Reference Voltage to Reset (V) |
|---|---|---|---|
| 0 | 0 | 0 | 0.7 |
| 0 | 0 | 1 | 0.75 |
| 0 | 1 | 0 | 0.8 |
| 0 | 1 | 1 | 0.85 |
| 1 | 0 | 0 | 0.9 |
| 1 | 0 | 1 | 0.95 |
| 1 | 1 | 0 | 1.0 |
| 1 | 1 | 1 | 1.05 |

After the decoder is complete, it is important to understand which reference voltages are needed to perform the next circuit.

However, the bandgap (reference voltage), provided by CERN, has only a reference voltage of, approximately, 0.3V. Because of this, it is necessary to have a resistive ladder that can give a shift of supply voltage, in order to be correctly compared with the bandgap. Figure 3.6 shows the resistive ladder intended for this purpose.

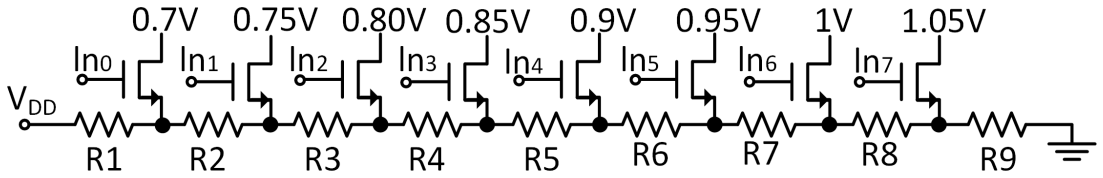



Figure 3.6: Resistive ladder. The NMOS with undefined bulk have their bulk grounded.

In Figure 3.6, the output of each transistors is the same, a little lower than bandgap voltage (0.3V) to make sure that the comparator switches when the supply voltage is below the minimum voltage required. However, Figure 3.6 shows that the output of each transistor goes from 0.75V to 1.15V, in order to know, depending on the input bits, which transistor will be triggered. So it is possible to know which voltage should be compared with the bandgap voltage.

The key part of Figure 3.6 is to know the reason why the supply voltages, chosen by CERN, increase from $V_{dd}$ to $V_{ss}$ and not the other way around.

The explanation is simple. Since the output voltage of each transistor must be approximately 0.3 V (bandgap reference voltage), the lower the supply voltage is, the greater must be the coefficient of the voltage divider, to compensate it.The opposite also applies. The higher the voltage, the lower will be the coefficient of the voltage divider.

To meet the requirements imposed by CERN, regarding the reference voltages, and knowing that the resistances are in series, using the voltage divider it is possible to obtain the values of the resistances:

$$
\begin{aligned}
0.27 &= \frac{R9}{R1+R2+R3+R4+R5+R6+R7+R8+R9}\,1.05 \\
0.27 &= \frac{R9+R8}{R1+R2+R3+R4+R5+R6+R7+R8+R9}\,1.0 \\
0.27 &= \frac{R9+R8+R7}{R1+R2+R3+R4+R5+R6+R7+R8+R9}\,0.95 \\
0.27 &= \frac{R9+R8+R7+R6}{R1+R2+R3+R4+R5+R6+R7+R8+R9}\,0.9 \\
0.27 &= \frac{R9+R8+R7+R6+R5}{R1+R2+R3+R4+R5+R6+R7+R8+R9}\,0.85 \\
0.27 &= \frac{R9+R8+R7+R6+R5+R4}{R1+R2+R3+R4+R5+R6+R7+R8+R9}\,0.8 \\
0.27 &= \frac{R9+R8+R7+R6+R5+R4+R3}{R1+R2+R3+R4+R5+R6+R7+R8+R9}\,0.75 \\
0.27 &= \frac{R9+R8+R7+R6+R5+R4+R3+R2}{R1+R2+R3+R4+R5+R6+R7+R8+R9}\,0.7
\end{aligned}
\tag{3.3}
$$

From a system of equations based on those represented in 3.3, some valid results could be reached:

$$
\begin{aligned}
R1 &= 59.75\,k\Omega \\
R2 &= 2.50\,k\Omega \\
R3 &= 2.19\,k\Omega \\
R4 &= 1.93\,k\Omega \\
R5 &= 1.72\,k\Omega \\
R6 &= 1.54\,k\Omega \\
R7 &= 1.38\,k\Omega \\
R8 &= 1.25\,k\Omega \\
R9 &= 25\,k\Omega
\end{aligned}
\tag{3.4}
$$

Again, in order to reduce the area and power dissipation, all the NMOS transistors are designed with the minimum length (L) and width (W) allowed by technology.

### 3.1.3 Comparator

After the circuit is complete, which caused the shift of the supply voltage, and having the bandgap reference voltage provided by CERN, it is necessary to draw a comparator to see when the supply voltage (indirectly) is lower than the bandgap voltage.

The behaviour of the comparator is described as follows: while the supply voltage is greater than the reference voltage, the output of the comparator is $V_{ss}$. However, when the supply voltage is less than the reference voltage, the output of the comparator will be $V_{dd}$. Figures 3.7 and 3.8 are show the behaviour of the comparator. Figure 3.8 is a zoom of figure 3.7, which shows the comparator's output transition from $V_{ss}$ (ground) to $V_{dd}$.

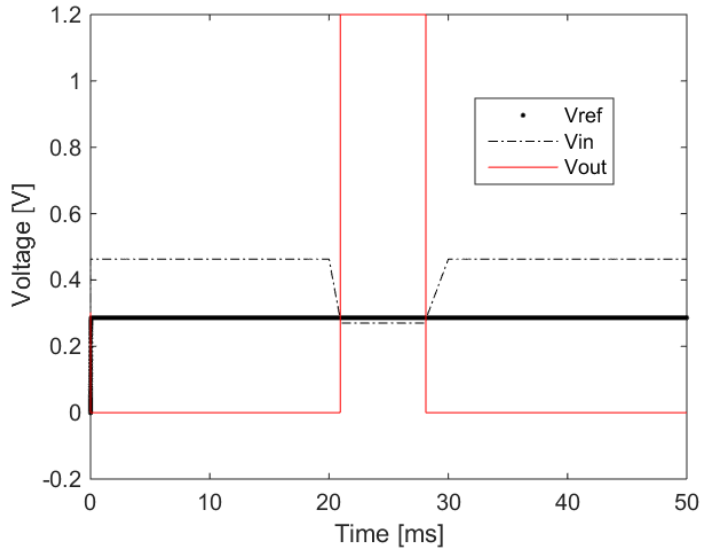



Figure 3.7: Comparator Output on the basis of $V_{in}$ and $V_{ref}$.

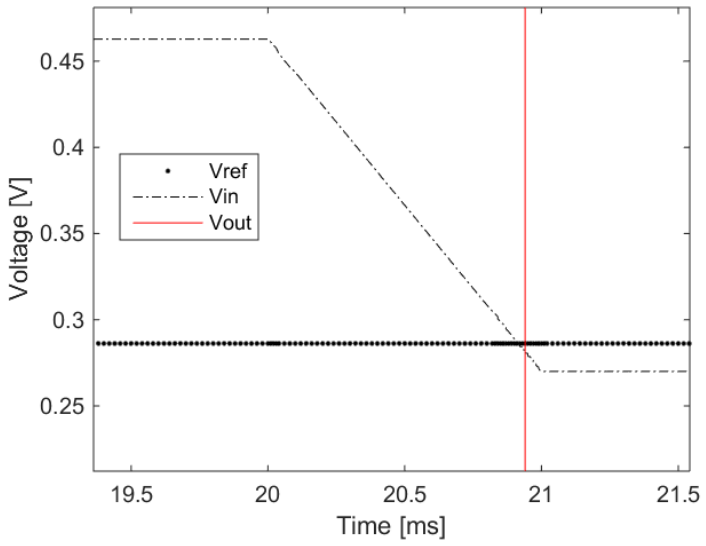



Figure 3.8: Zoom of the Comparator Output on the basis of $V_{in}$ and $V_{ref}$.

In order to work as intended (described above), the comparator was implemented as follows:

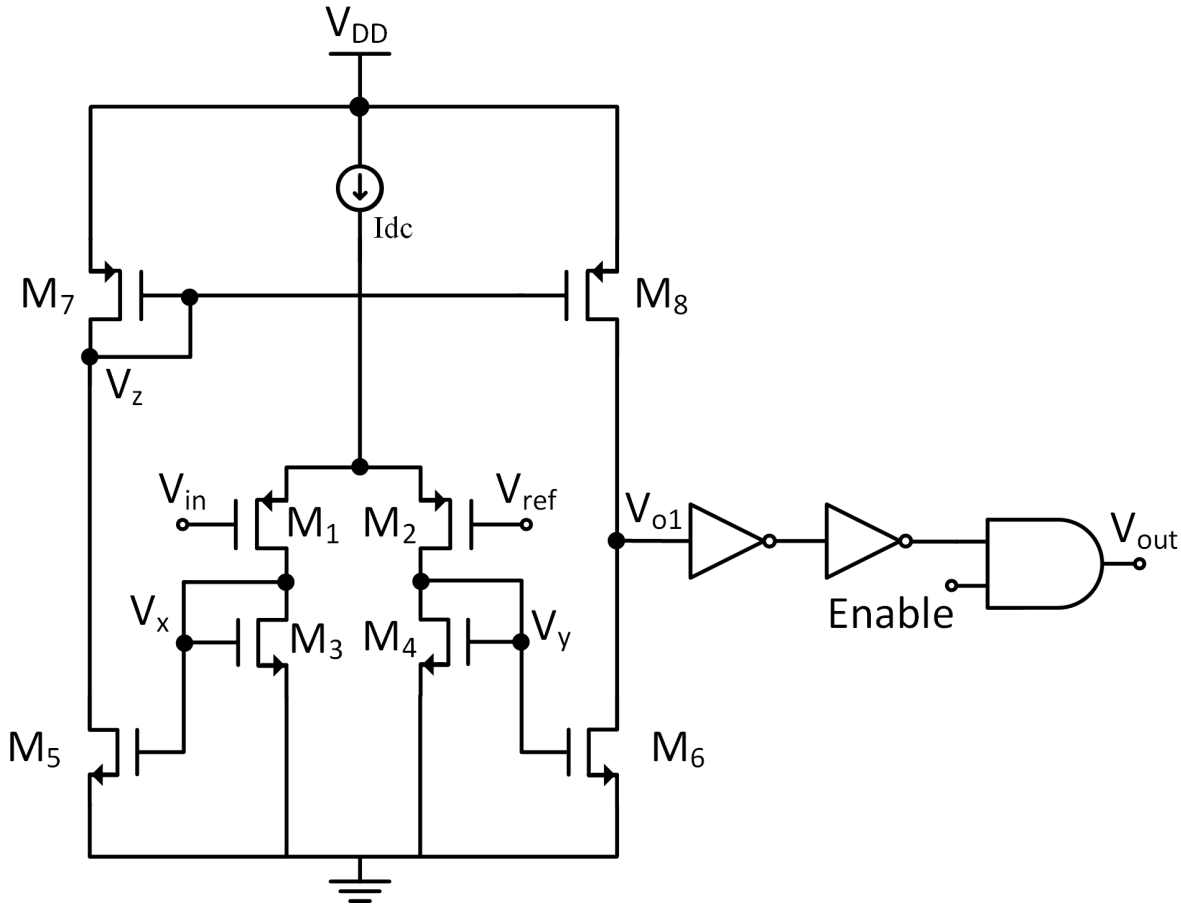



Figure 3.9: Simplified schematic of the comparator. PMOS and NMOS with undefined bulk have their bulk connected do $V_{dd}$ and ground, respectively.

Figure 3.9 shows the simplified schematic of the comparator used in Brown-Out Reset. The operation of this schematic is as follows:

- Assuming that $V_{in}$ is greater than $V_{ref}$, transistors $M_{2,4}$ will pull more current than transistors $M_{1,3}$. Consequently, the node $V_y$ will be the highest possible, approximately, $V_{dd} - V_{Idc}$. The transistor $M_6$ therefore has the maximum $V_{gs}$ and for that reason will pull more current than transistors $M_{5,7}$. Once the transistor $M_6$ pulls more current, the node $V_{01}$ will tend to $V_{ss}$;
- However, if $V_{ref}$ is greater than $V_{in}$, transistors $M_{1,3}$ will pull more current than transistors $M_{2,4}$. Following the same sort of idea as for the previous topic, $V_x$ will be, approximately, $V_{dd} - V_{Idc}$. Because of this, node $V_z$ will tend to $V_{ss}$ and, therefore, the transistor $M_8$ will have the highest $V_{gs}$, in module. So node $V_{01}$ will tend, approximately, to $V_{dd}$ ($V_{dd} - V_{ds_{M_8}}$).

It is necessary to have sufficient gain, so that the comparator is able to switch between $V_{dd}$ and $V_{ss}$ (level 1 and level 0, respectively). With a current source of 7.47 $\mu$A and the transistors sizes presented in table 3.4 the comparator has a gain of 30 dB.

Table 3.4: Transistor dimensions used in the comparator.

| Transistor | W ($\mu$m) | L ($\mu$m) | Number of Fingers | Multiplier |
|---|---|---|---|---|
| M1/M2 | 1.5 | 0.13 | 5 | 1 |
| M3/M4 | 0.5 | 0.16 | 2 | 1 |
| M5/M6 | 0.375 | 0.16 | 4 | 1 |
| M7/M8 | 0.5 | 1 | 2 | 1 |

However, to obtain from the output of the comparator two distinct logical levels ($V_{dd}$ and $V_{ss}$), inverters are required in the output of the differential pair because it will increase the gain and, consequently, the signal will saturate to $V_{dd}$ or $V_{ss}$, as shown in Figure 3.10.

In order to obtain the desired response from the comparator's output, 2 inverters in series are needed.

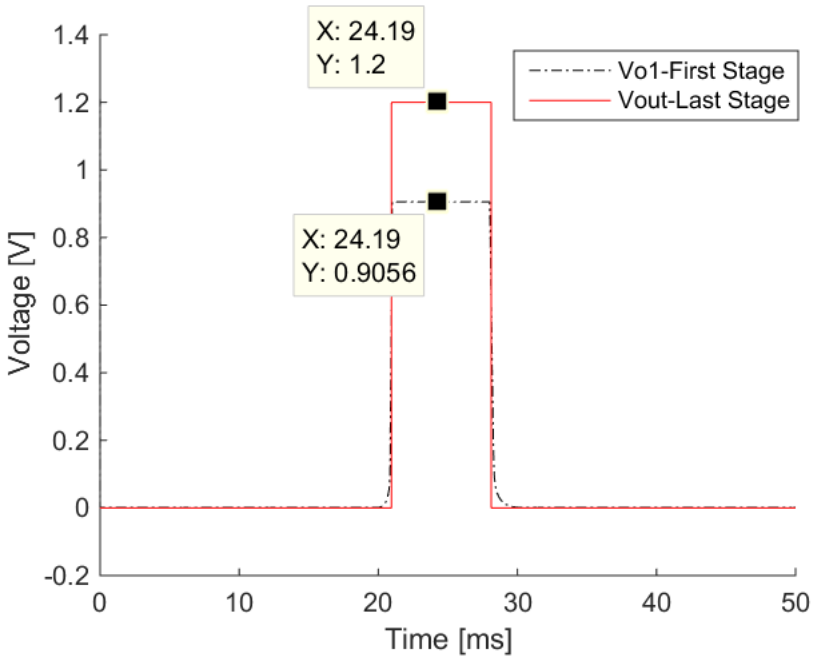



Figure 3.10: Comparator's first stage output (Vo1) and last stage (Vout).

#### 3.1.3.1 Monte Carlo Simulations

In order to verify the sensitivity of this comparator, Monte Carlo simulations were performed and the results are shown in Tables 3.5 and 3.6.

The Monte Carlo simulations made it possible to estimate the expected gain and offset of this comparator, when the temperature is contained between -20 ºC and 100 ºC range.

Table 3.5: Monte Carlo simulations- Calculation of the offset.

| Temperature | Min (mV) | Max (mV) | Mean (mV) |
|---|---|---|---|
| -20 ºC | 2.8 | 3.8 | 3.2 |
| 100 ºC | 1.1 | 3.5 | 2.9 |

Table 3.6: Monte Carlo simulations- Calculation of the gain.

| Temperature | Min (mV) | Max (mV) | Mean (mV) |
|---|---|---|---|
| -20 ºC | 30.3 | 31.3 | 30.8 |
| 100 ºC | 26.8 | 28.6 | 27.9 |

The offset was calculated using the absolute value between the intersection of $V_{dd\ shift}$ with $V_{ref}$ and the comparator's output when it reaches 0.6 V.

From Tables 3.5 and 3.6, it can be concluded that the comparator does not vary much with respect to temperature.

### 3.1.4 Schmitt Trigger

The final sub-block of Power-on Reset & Brown-out Reset to be described is the Schmitt Trigger. This sub-block is responsible for activating the external circuits, which depend on it, when the capacitor's voltage reaches a certain acceptable value.

In order to meet one more requirement set by CERN, the Schmitt Trigger output value should be $V_{dd}$ while it is on the Reset mode, in other words, while the capacitor does not reach a certain voltage. However, it has to be able to switch its output voltage from $V_{dd}$ to $V_{ss}$ when the capacitor reaches the desired voltage.

This sub-block was accordingly implemented in the circuit as shown in Figure 3.11.

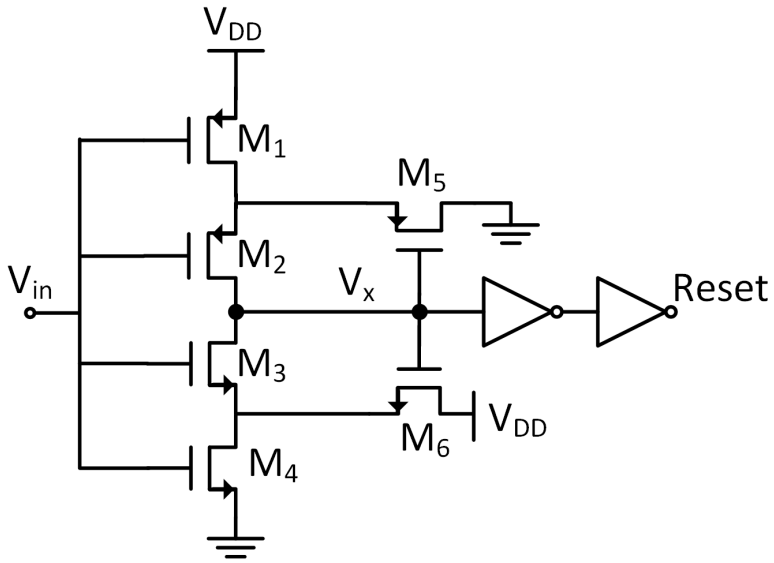



Figure 3.11: Simplified schematic of the Schmitt Trigger. PMOS and NMOS with undefined bulk have their bulk connected to $V_{dd}$ and ground, respectively.

From Figure 3.11 it is possible to understand the circuit's operation:

- When $V_{in}$ is 0 V initially (the capacitor is discharged), the transistors $M_1$ and $M_2$ are ON and the transistors $M_3$ and $M_4$ are OFF. Because of this, the current that passes on these 4 transistors is 0 A meaning that the $V_{ds}$ of transistors $M_1$ and $M_2$ are 0 V. The $V_x$ node is therefore charged with a certain $V_{dd}$ voltage, which turns the Schmitt Trigger's output into its Reset mode, preventing the external circuits from operating. While the capacitor does not reach a desired voltage, the output from this block will always be in Reset mode;

- When the voltage $V_{in}$ (capacitor) reaches a certain value (in this dissertation this is 0.8 V), the transistors $M_1$ and $M_2$ will tend to be OFF while the transistors $M_3$ and $M_4$ will switch from OFF to ON. In this transitional period, the $V_x$ node discharges and will tend to $V_{ss}$ because the $V_{ds}$ of each transistor NMOS ($M_3$ and $M_4$) is approximately 0 V (the same idea as in the previous topic: The $V_{ds}$ is approximately 0 V because the current is approximately 0 A). Once the node $V_x$ is 0 V, the Schmitt Trigger's output is 0 V too and, because of this, the external circuits' work will begin.

After this explanation about the behaviour of Schmitt Trigger's block, it is necessary to establish how the switch voltages (switching $V_{dd}$ to $V_{ss}$ and the other way around) of this sub-block works. The threshold voltage varies depending on the difference of the W/L ratio of the PMOS and NMOS transistors.

Figures 3.12, 3.13, 3.14 and 3.15 show the variation of the threshold's voltage when varying the W/L relationship between PMOS and NMOS in Figure 3.11.

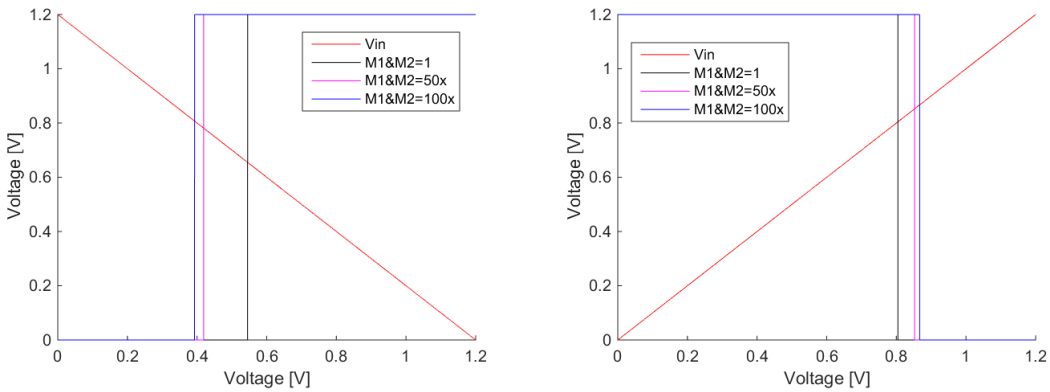
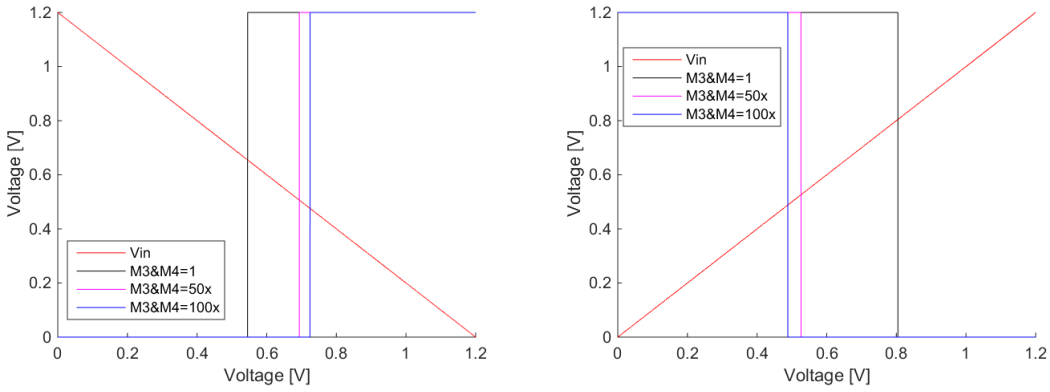


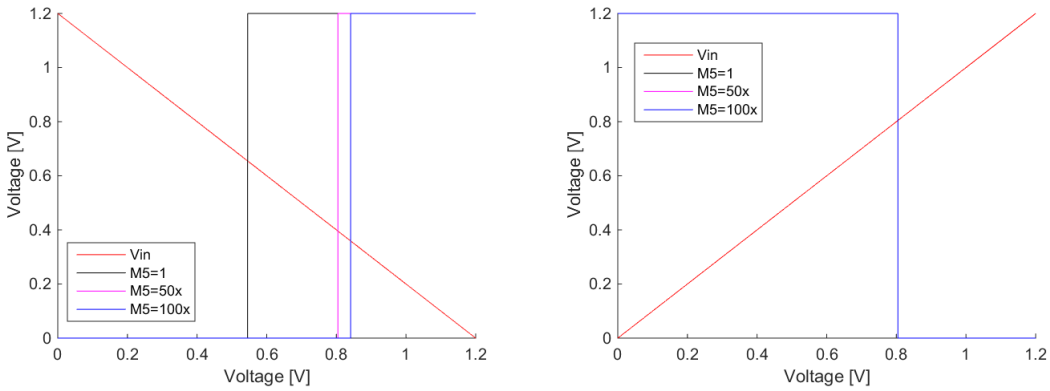

Figure 3.12: Variation in threshold output of the Schmitt Trigger with respect to the size of transistors $M_1$ and $M_2$.

Figures 3.12 a) and b) indicate that the larger the size of transistors $M_1$ and $M_2$, the greater the Reset time will be because the capacitor's threshold voltage increases when charging but decreases when discharging. This means that the capacitor's charging



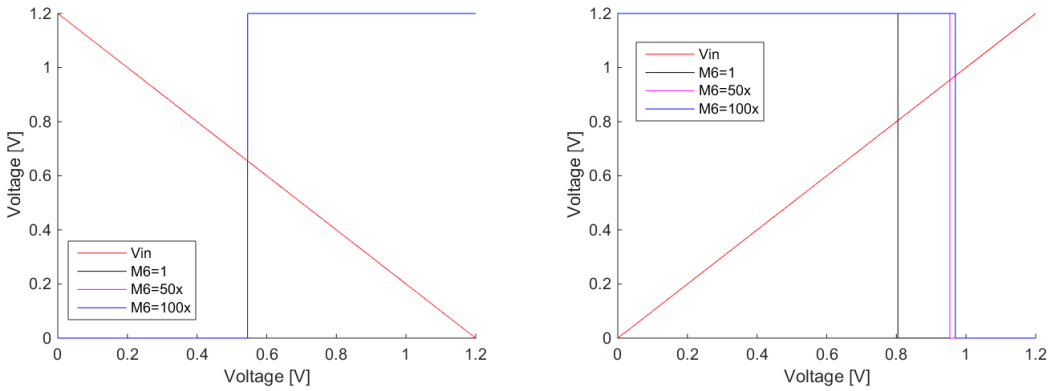

a b

Figure 3.13: Variation in threshold output of the Schmitt Trigger with respect to the size of transistors $M_3$ and $M_4$.




a b

Figure 3.14: Variation in threshold output of the Schmitt Trigger with respect to the size of transistor $M_5$.




a b

Figure 3.15: Variation in threshold output of the Schmitt Trigger with respect to the size of transistors $M_6$.

period to the Schmit-Trigger's output switch from $V_{dd}$ to $V_{ss}$ needs to be longer than the capacitor's discharging period to switch from $V_{ss}$ to $V_{dd}$.

Figures 3.13 a) and b) indicate that the larger the size of the transistors $M_3$ and $M_4$, the lower the Reset time will be, because the capacitor's threshold voltage decreases when charging but increases when discharging. This means that the capacitor's discharging period to the Schmitt-Trigger's output switch from $V_{ss}$ to $V_{dd}$ needs to be longer than the capacitor's charging period to switch from $V_{dd}$ to $V_{ss}$.

Unlike transistors $M_1$, $M_2$, $M_3$ and $M_4$, which influence the rise and fall of the Schmitt Trigger's output signal, transistors $M_5$ and $M_6$ only influence one of the arches as shown in Figures 3.14 and 3.15.

Figures 3.14 a) and b) show that the transistor $M_5$ only influences the transition from $V_{ss}$ to $V_{dd}$ (capacitor's discharge). It is therefore possible to conclude that the bigger the $M_5$ transistor's size, the greater the capacitor's discharge will be to activate the Reset.

On the other hand, Figures 3.15 a) and b) show that the transistor $M_6$ only influences the transition from $V_{dd}$ to $V_{ss}$ (capacitor's charge). From that it is possible to conclude that the bigger the $M_6$ transistor's size is, the greater the capacitor's discharge will be to deactivate the Reset.

Having observed the impact of the transistors' size on the Schmitt Trigger's output signal threshold in both arches, it is important to discover which are the threshold requirements to comply with CERN's requirements. With thresholds of 0.8 V for the capacitor charging and 0.6 V for the capacitor discharging, the transistors will have the following dimensions, as shown in Table 3.7.

Table 3.7: Transistor dimensions used in the Schmitt Trigger.

| **Transistor** | **W ($\mu$m)** | **L ($\mu$m)** | **Number of Fingers** | **Multiplier** |
|---|---|---|---|---|
| M1/M2 | 4 | 1 | 5 | 1 |
| M3/M4 | 1 | 1 | 1 | 1 |
| M5 | 1 | 1 | 1 | 1 |
| M6 | 1 | 1 | 1 | 1 |

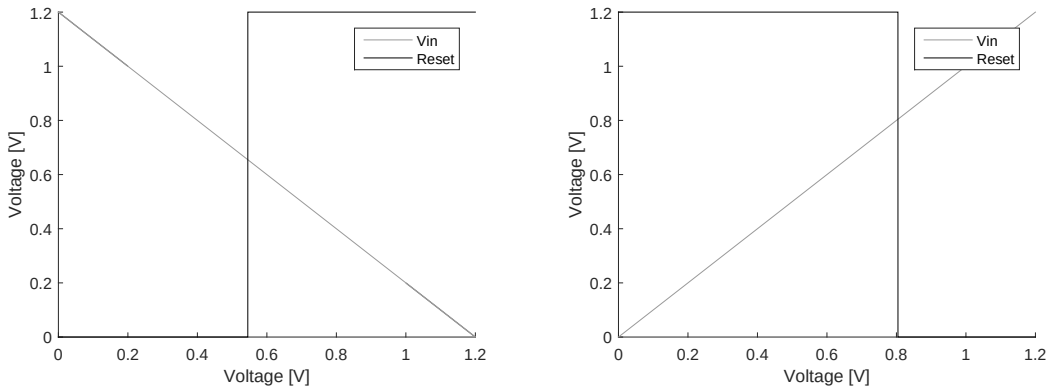
#### 3.1.4.1 Monte Carlo Simulations

In the same way as for the comparator, in sub-section 3.1.3.1, Monte Carlo simulations have also to be run on the Schmitt Trigger.

The main part of this simulation is measuring the maximum variation of both thresholds, positive and negative arch, of the Schmitt Trigger's output signal.

In Figures 3.16 a) and b) it is possible to observe the arcades' intersections with an input signal of $V_{in}$. The values of these intersections are stored to establish the minimum and maximum thresholds in both arches.

From Tables 3.8 and 3.9, it can be concluded that the threshold voltage in both arches does not vary much with respect to temperature (between -20 ºC to 100 ºC).




a b

Figure 3.16: Monte Carlo simulations.

Table 3.8: Monte Carlo simulations- Calculation of the threshold when the capacitor is charging.

| Temperature | Min (mV) | Max (mV) | Mean (mV) |
|---|---|---|---|
| -20 ºC | 786.1 | 809.9 | 798.8 |
| 100 ºC | 802.9 | 827.5 | 815.4 |

Table 3.9: Monte Carlo simulations- Calculation of the threshold when the capacitor is discharging.

| Temperature | Min (mV) | Max (mV) | Mean (mV) |
|---|---|---|---|
| -20 ºC | 609.1 | 646.5 | 626.8 |
| 100 ºC | 675.8 | 712.6 | 693.5 |

## 3.2 POR-BOR - The Overall System

Having arrived at an understanding of the Power-On Reset & Brown-Out Reset circuit functionalities, in section 3.1, and the sub-blocks implemented in this block, it is necessary to test the whole circuit in all its corners with a temperature between -20 ºC and 100 ºC:

- FF → Fast NMOS and Fast PMOS;
- TT → Typical NMOS and Typical PMOS;
- SS → Slow NMOS and Slow PMOS;
- SF → Slow NMOS and Fast PMOS;
- FS → Fast NMOS and Slow PMOS;

But first it is imperative to determine what needs to be tested.

Figure 3.17 a) shows the variation of the supply voltage ($V_{dd}$) over time. In this case, the input bits chosen for study were the largest, i.e. b0 = 1 V, b1 = 1 V and b2 = 1 V. As shown in table 3.3 in section 3.1.2.1, this value corresponds to a reference voltage of approximately 1.05 V.

So, as can be seen in Figure 3.18, only the POR is activated because the supply voltage has still not reached an allowed voltage for external circuits' operation (the enabled circuit disables operation of the comparator - BOR).

Returning to Figure 3.17, at a certain point, in this case 10 ms, the enable is activated, allowing BOR to function. So when the supply voltage falls below a certain reference's value (in this case 1.05 V because all the input bits, from the decoder, are ON), the comparator (BOR) is activated and, consequently, the Reset signal is also activated, preventing external circuits from working.

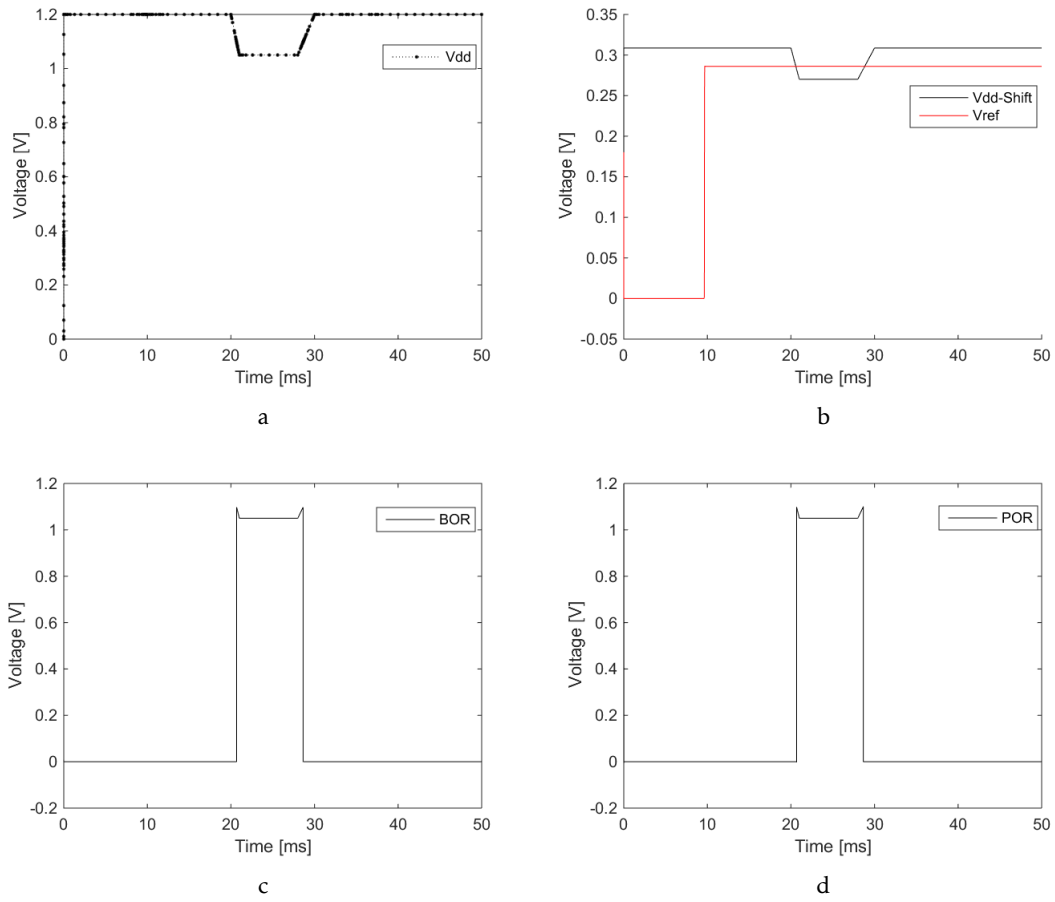



Figure 3.17: Power-On Reset & Brown-Out Reset simulations.

From these simulations, presented in Figure 3.17, it is necessary to determine some of the CERN's requirements:

- The exact values of the supply voltage, $V_{dd}$, bandgap and $V_{dd\,shift}$ of when the Reset is activated;

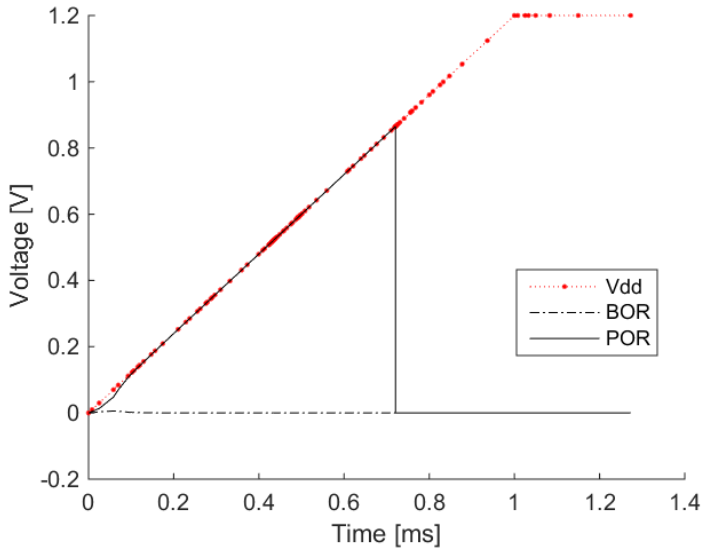



Figure 3.18: Power-On Reset & Brown-Out Reset simulations - zoom between 0 ms and 1.4 ms with a $V_{dd}$ rise time of 1 ms.

- The time that Reset takes to switch its value to $V_{dd}$ when the supply voltage reaches the threshold value of POR (initial time- between 0 ms and 2 ms);
- The main block (comparator) and the whole circuit Power consumption.

It is therefore necessary to measure the requirements imposed by the CERN in all the corners with a temperature between -20 ºC and 100 ºC.

### 3.2.1 Simulation Results

Once it is known what needs to be measured in the corners, the exact value of the supply voltage when the Reset is activated is presented in the first two Tables in A.1.

The bandgap, the $V_{dd\,shift}$, the power consumption values and the Reset time that is taken to switch the value to $V_{dd}$, when the supply voltage reaches the threshold value of POR, are presented in Tables A.1.

The first two tables in A.1 show that the values obtained in the corners are results very close to the desired reference voltage. However, it is necessary to determine why the voltage difference, at higher temperatures, is greater than at lower temperatures. So in the tables below, in A.1, the bandgap (BG) and $V_{dd\,shift}$ values are calculated for when the Reset was activated.

It should be noted that the relative error of the bandgap voltage and $V_{dd\,shift}$ values is less than 2% in all simulations. Since the difference in the reference voltage, shown on the first two tables in A.1, is not in the Power-On Reset & Brown-Out Reset (because the relative error is less than 2% in all the simulations, as explained earlier), it may be concluded that the problem lies in the bandgap provided by CERN.

In the tables below, in A.1, it can be observed that the bandgap's value varies depending on the temperature and process. This conclusion is very important because the greater the bandgap voltage value is, the faster the intersection between $V_{dd_{shift}}$ and the voltage value of the bandgap (BG) will be. In addition to this, the faster the activation of the Reset by BOR is, the greater the value will be of the voltage of the output POR-BOR will be.

According to the Total Power Consumption (TPC in A.1), a value of less than 40 $\mu$A was obtained and, as predicted, the sub-block that consumes most current is the comparator (POR-BOR's critical area), as shown in A.1.

Finally, regarding to the Reset time, it should be noted that the minimum time, in which the Reset remains active until the supply voltage ($V_{dd}$) reaches a desired threshold voltage, is 12 $\mu$s with a $V_{dd}$ rise time of 1 $\mu$s.

### 3.2.2 Schematics vs Layout

This block (POR-BOR) is the final step and after getting through all the corners, it is necessary to implement the layout.

Given that the simulations of each sub-block, Power-On Reset and Brown-Out Reset, were made at the start and since the value that each sub-block must have is known (from the schematic simulations), the remaining purpose of this section is to establish the layout for each of the sub-blocks and to compare the simulations of the results of both, layout vs. schematic.

In the end, the goal is to gather all the layouts made of each sub-block in order to occupy the minimum area possible and get results closer results to the schematic ones.

The following sub-sections will show each sub-block's layout and, simulation (layout vs schematic).

#### 3.2.2.1 Current Source - Layout vs Schematic

As this sub-block has only PMOS transistors and resistances, they share the same well, N-Well to be precise. It is therefore only necessary to deal with the transistors and resistors so that they occupy the minimum area possible and cover it with an N-well guard ring.

Figure 3.19 shows the layout of the current source. A space may be observed between the PMOS transistors and the guardring. This space is due to the fact that there is a rule, at least 1 $\mu$m, between the gates and the well, in this case the N-well.

After the layout was run in the DRC and LVS, the parasitic capacities (PEX) were extracted in order to make a simulation and compare it with the schematic.

Figure 3.20 shows that the results between the schematic and the layout are very close. In the schematic simulation, the current source is approximately 218 nA while in the layout it is approximately 217 nA, so it can be concluded that there is a minimum difference of 1 nA.

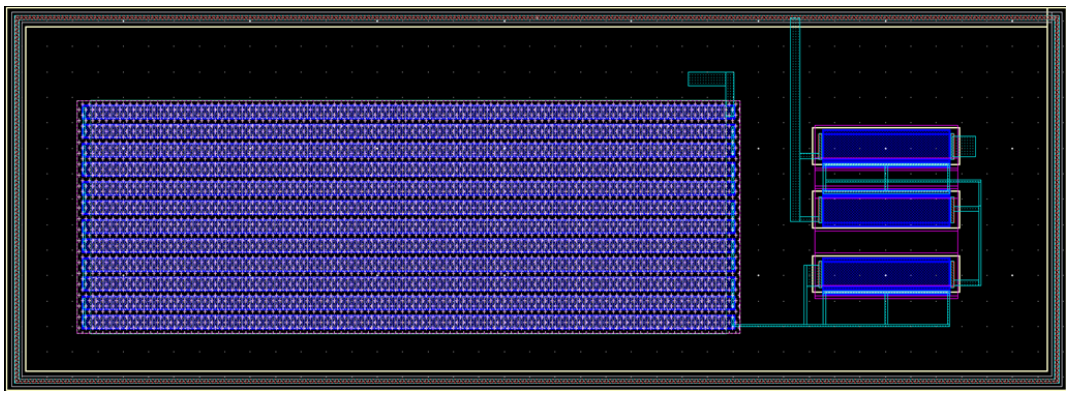


Figure 3.19: Layout implementation of the current source.

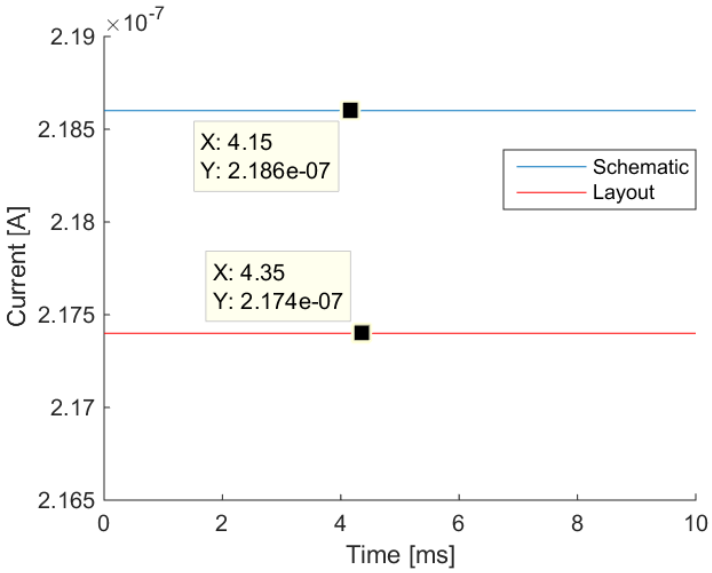



Figure 3.20: Current Source simulation results - schematic vs layout.

#### 3.2.2.2 Decoder and Threshold - Layout vs Schematic

This section will be divided into 2 parts:

- 3 bits Decoder;
- Threshold voltage;
- Simulation results - schematic vs layout.

Figure 3.21 shows the 3 bits decoder's layout. It should be noted that the logical ports, NAND and NOT gates, are both symmetrically placed when viewed from the right and left side and also in order to occupy the minimum area possible.

As shown in Figure 3.22, the left side represents the 3 bits decoder, on the right side it is possible to view the resistances used to achieve the desired voltage. Lastly, in the centre, there are the NMOS transistors, which can be used as switches. Since the NMOS

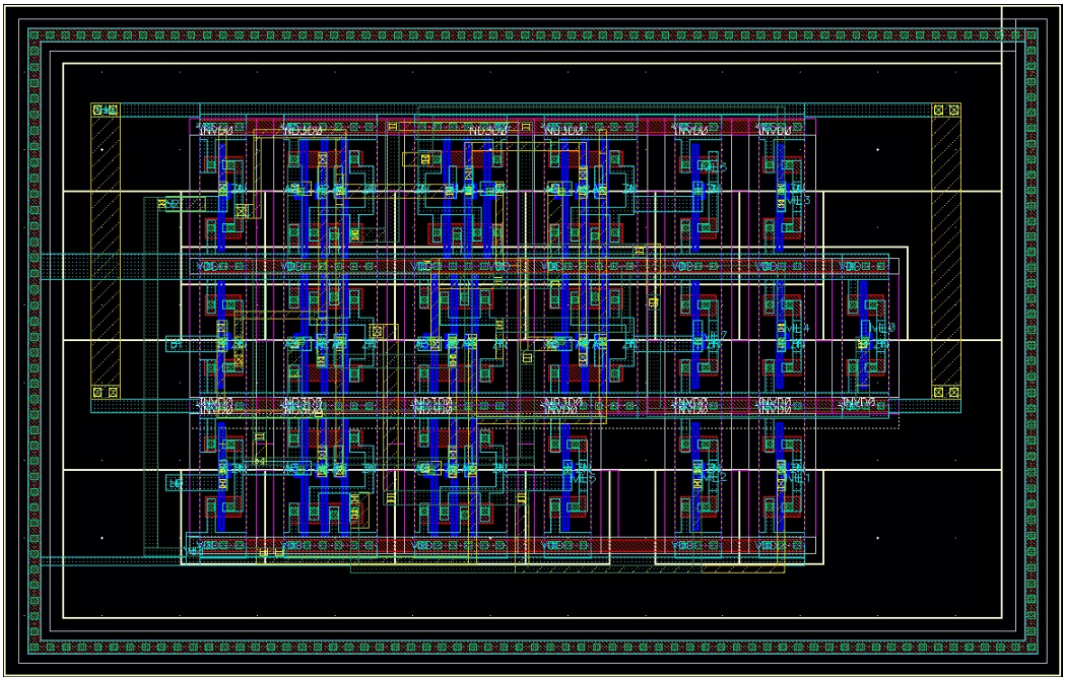


Figure 3.21: Layout implementation of the 3 bits decoder.

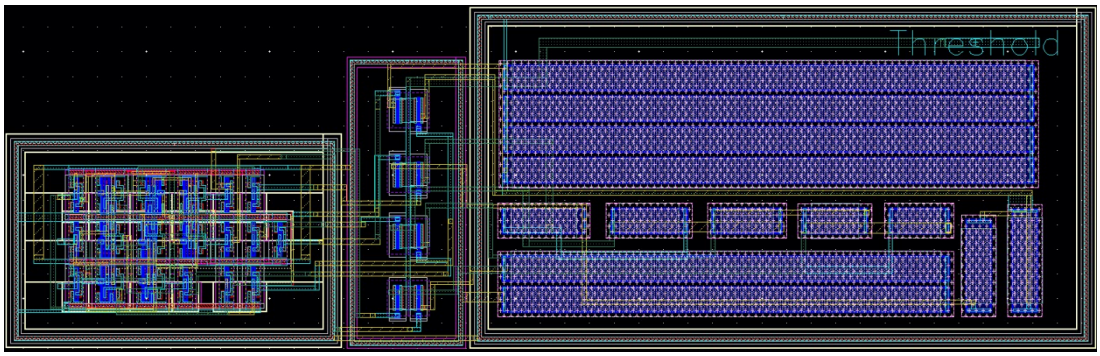



Figure 3.22: Layout implementation of the threshold.

transistors are soaked in a P-Well, the guardring of the NMOS transistors is different from the PMOS transistors.

Once again, the main intention was to save as much area as possible.

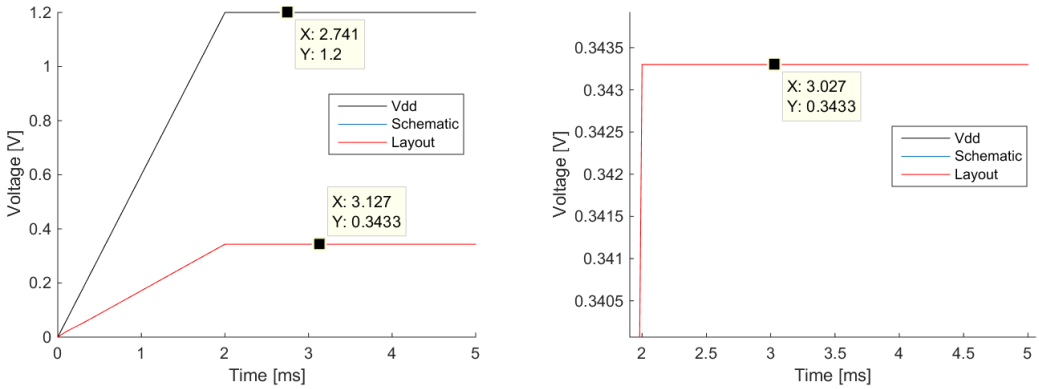
Figures 3.23 a) and b) show that the difference between the results of the schematic and layout is approximately 0 V. This simulation was made with input bits equal to 1 and a temperature equal to 27 ºC in TT (typical-typical).

#### 3.2.2.3 Comparator - Layout vs Schematic

This section will present the comparator's layout and the comparison between the layout and schematic simulations.

Figure 3.24 represents the implementation of the comparator's layout.

Because this is the most critical sub-block in the POR-BOR, the layout's symmetry




a b

Figure 3.23: Threshold simulation results - schematic vs layout. b) is a zoom of a).

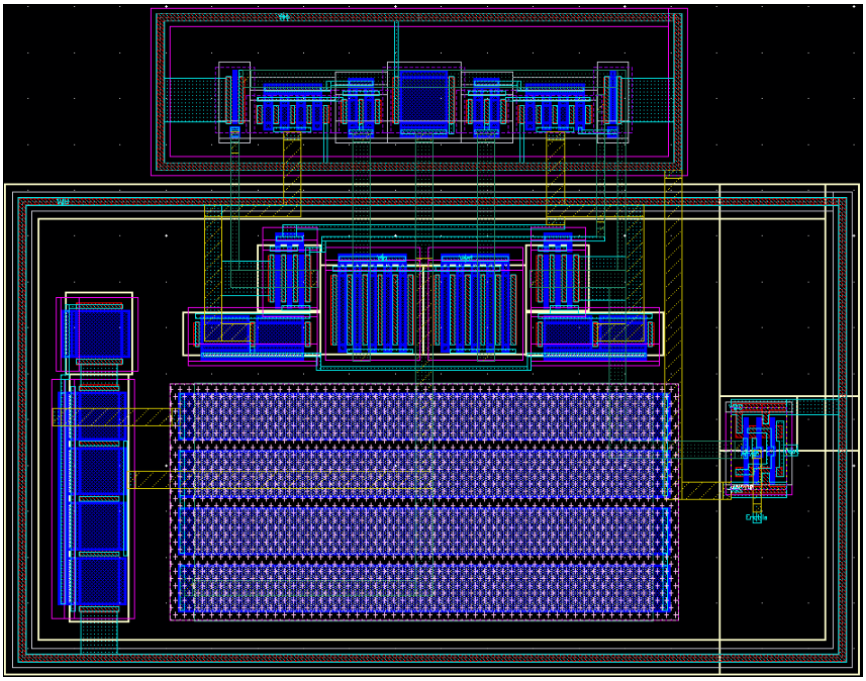
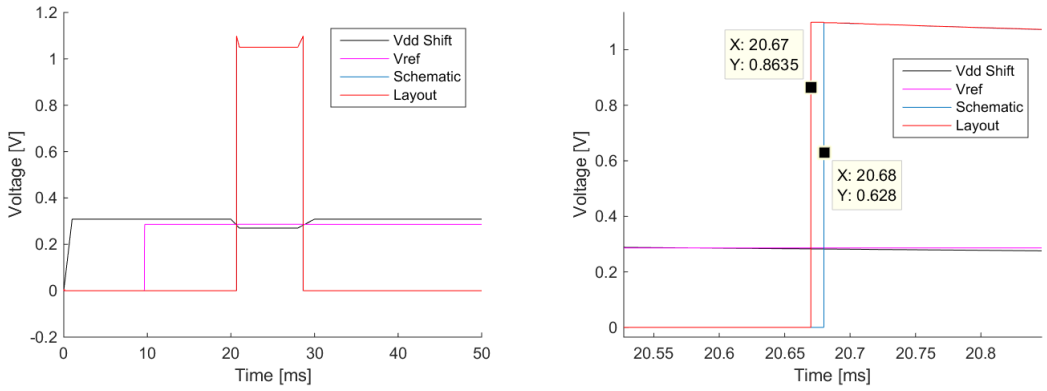


Figure 3.24: Layout implementation of the comparator.

is absolutely necessary. In the differential pairs' layout dummy transistors were used in order to look exactly the same on both sides (left and right).

It was also important to separate the NMOS transistors (located above) from the PMOS transistors (located at the bottom with the resistance in the centre), as can be seen in Figure 3.24,because these two types of transistors (PMOS and NMOS) are embedded in different wells (N-Well and P-Well, respectively).

Once again, the main intention was to save as much area as possible.




a b

Figure 3.25: Comparator's simulation results - schematic vs layout. b) is a zoom of a).

Figure 3.25 a) shows a simulation in which the comparator is active when the shifted supply voltage ($V_{dd\,shift}$) is less than the reference voltage. Regarding to the Figure 3.25 b), it is possible to notice that the results obtained in the schematic and layout are very close. When the comparator is activated and when it reaches the supply voltage (in this case 1.05 V because the input bits are equal to 1), transition time is saved from $V_{ss}$ to $V_{dd}$. This makes it possible to compare both sets of results (schematic and layout):

- Schematic → 20.68 ms;
- Layout → 20.67 ms;
- Difference between Schematic and Layout → 10 $\mu$s.

#### 3.2.2.4 Schmitt Trigger - Layout vs Schematic

This section follows the same reasoning as described in the previous section (Comparator: 3.2.2.3), because this circuit also features NMOS and PMOS transistors. So it is also necessary to separate these two types of transistors because, as stated before, they present different wells.

Figure 3.26 represents the implementation of the Schmitt Trigger's layout. Once again, since NMOS and PMOS transistors were used it is necessary to separate them because they present different well types.

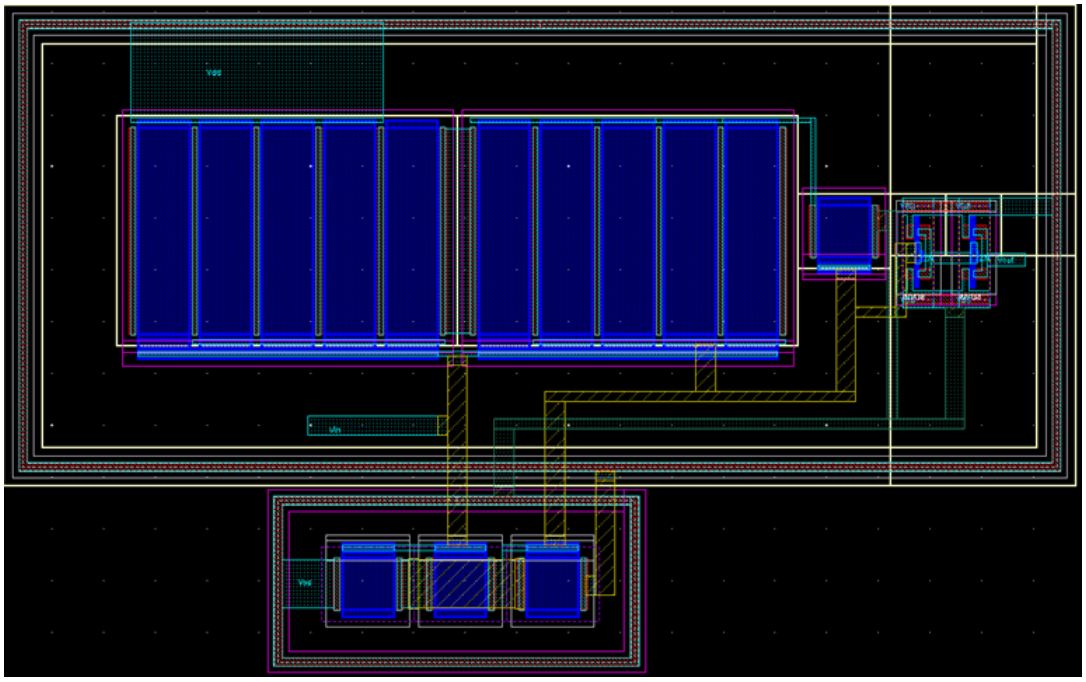
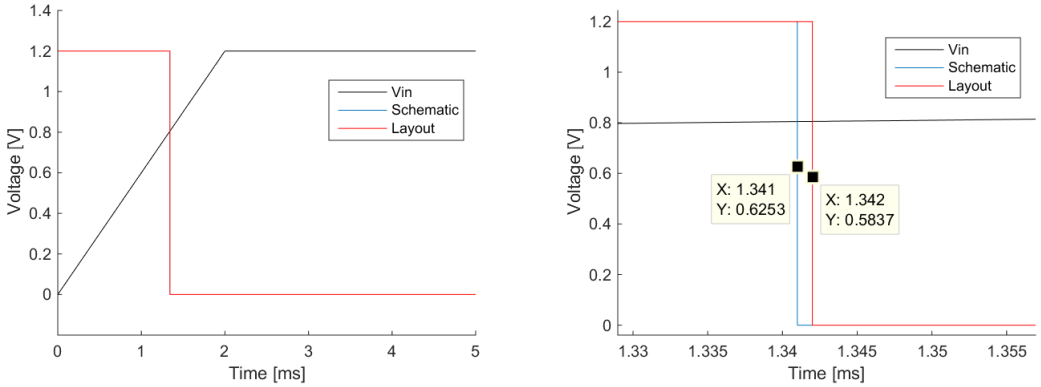


Figure 3.26: Layout implementation of the schmitt trigger.

It is also possible to observe in the Figure 3.26 that, once again, the space between the PMOS/NMOS transistors (gates) and the guardring (well), to comply with the rule, needs to be at least 1 $\mu$m.

After the layout was run in the DRC and LVS, the parasitic capacities (PEX) were extracted in order to make a simulation and compare it with the schematic.




a b

Figure 3.27: Comparator's simulation results - schematic vs layout. b) is a zoom of a).

Figure 3.27 b) shows that the results obtained in the schematic and layout, are very close. In the schematic simulation, the time that the Schmitt Trigger's output takes to change, in this case, from $V_{dd}$ to $V_{ss}$, is approximately 1.341 ms while in the layout it is approximately 1.342 ms, with a minimum difference of 1 $\mu$s.

#### 3.2.2.5 POR-BOR - Layout vs Schematic

This sub-section is where all the POR-BOR sub-blocks' features are common. It is essential to pay attention to where to put each sub-block in order to save the most area possible especially for the 4 pF capacitor because of the area it occupies, as shown at the left side of Figure 3.28.

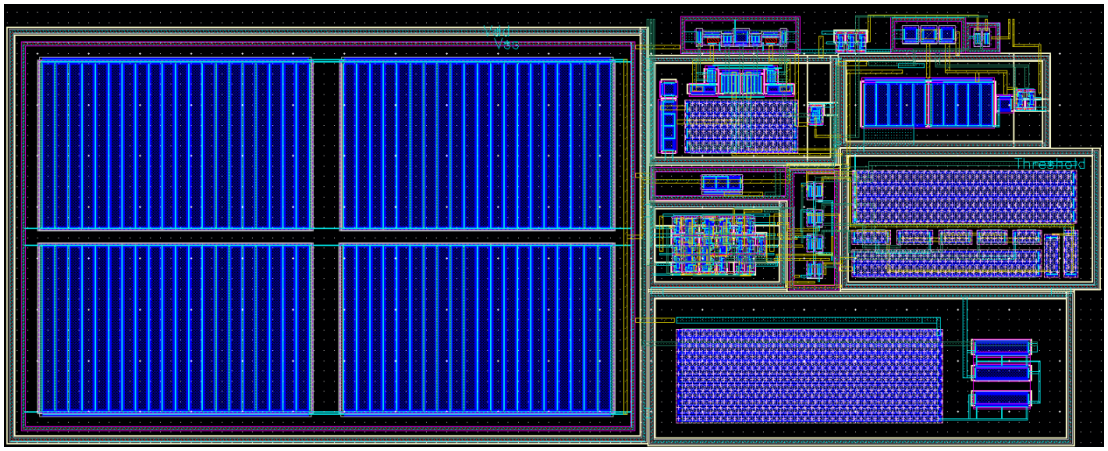



Figure 3.28: Layout implementation of the POR-BOR.

Figure 3.28 shows the top level of the Power-On Reset & Brown-Out Reset and also each sub-block's location:

- Current source → Bottom right;
- Threshold → Middle and right side;
- Comparator → Left of Schmitt Trigger;
- Schmitt Trigger → The Upper right;
- 4 pF Capacitor → Left side.

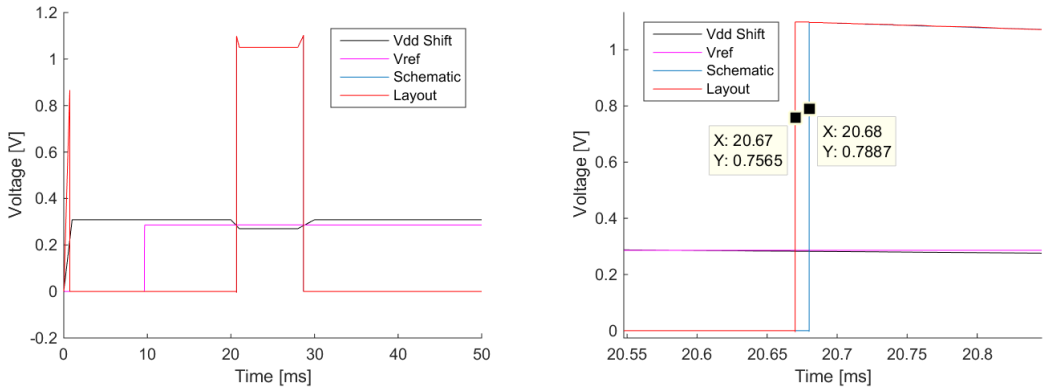
In order to meet the CERN requirements, only the first 3 metals ($M_1$, $M_2$ and $M_3$) were used to implement the layout.

It should be noticed that the main goal of the POR-BOR's layout implementation is to occupy the minimum area possible. Since the POR-BOR occupied area is 107 by 41 $\mu m^2$, and the chip provided by CERN is 1750 by 40 $\mu m^2$, the percentage of area that this block occupies is the following:

$$\begin{aligned} Percentage\ occupied\ in\ chip &= \frac{107 \times 41}{1750 \times 400} \times 100\ (\%) \\ Percentage\ occupied\ in\ chip &= 0.63\ (\%) \end{aligned} \tag{3.5}$$

From equation ( 3.5) it can be concluded that the Power-On Reset & Brown-Out Reset need only 0.63 % of the area, of the chip provided by CERN.

Finally, after the layoutwas run in the DRC and LVS, parasitic capacities (PEX) were extracted in order to simulate and compare results with those in the schematic simulation ones, as shown in Figure 3.29.




a b

Figure 3.29: POR-BOR's simulation results - schematic vs layout. b) is a zoom of a).

Figure 3.29 shows that the results obtained from the layout are close to those obtained from the schematic, with a difference of 10 $\mu$s. It is therefore also important to conclude that the final block (POR-BOR) meets all the requirements proposed by CERN between a temperature's range of -20 ºC and 100 ºC, in each process (FF, FS, TT, SS, SF).

Chapter 4

# Proposed 5 Gb/s TIA

Designing an high speed TIA is technically challenging and requires a novel design approach as well as trade-offs between some parameters such as gain, bandwidth, noise and linearity.

This section presents an architecture to achieve the requirements imposed by CERN, relating to:

- Gain;
- Bandwidth;
- Noise;
- Power Consumption.

In addition the sections below present the proposed architecture and the mathematical study made to achieve the best results in order to meet all the requirements.

Lastly, it is possible to get the results of each corner's simulation between -40 ºC and 100 ºC, in order to make a comparison between the schematic and the layout results.

## 4.1 Proposed design of TIA

As mentioned in section 2.3.2, in order to suppress the supply voltage's variation and the substract noise, it was necessary to use a differential amplifier, as shown in Figure 4.1.

Figure 4.1 shows the original proposed implementation of the TIA circuit. The main task of this circuit is to amplify and convert into a voltage signal the current signal, $I_{in}$, converted by the PD when there is an incoming optical signal, as mentioned in section 2.1. So it is important to establish the role of each component in Figure 4.1:

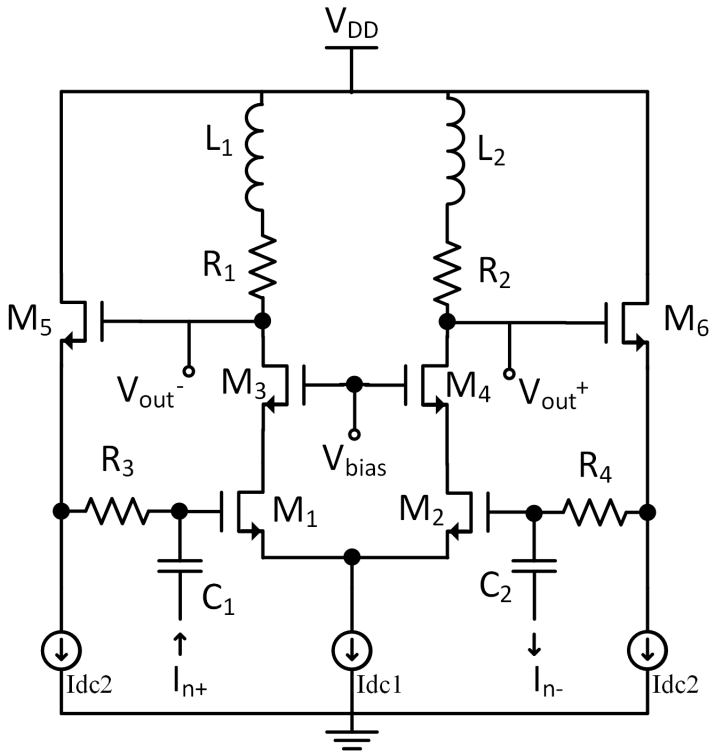



Figure 4.1: Circuit implementation of proposed TIA. NMOS with undefined bulk have their bulk connected to ground.

- Capacitors $C_1$ & $C_2$ → These capacitors decouple the transimpedance amplifier and isolate the photodiode bias current preventing it from determining the TIA's DC operating point. This is important because the photodiode, over time, will provide an increasing bias current (possible to reach 1 mA). $I_{dc2}$ is therefore used to bias the transistors $M_1$, $M_2$, $M_5$ and $M_6$;

- Transistors $M_1$ & $M_2$ and resistors $R_1$ & $R_2$ → The purpose of these resistors and transistors is to convert the photodiode's current into an output voltage with gain (in this case, open-loop gain).

  In order to increase the bandwidth, a low input resistance is necessary. However, for that, it is necessary to increase the amplifier's open-loop gain which is possible by increasing the transistors' width ($M_1 and M_2$) and the bias current, $I_{dc1}$. In high-frequency operations, it is difficult to increase the amplifier's open-loop gain to a value higher than 20 dB because of the relatively low transconductance gm of the 65 nm MOS transistors.

  Since the open-loop gain does not exceed a value of 20 dB, it is unnecessary to increase the current source by increasing the transistor's width because it will increase the input capacitance and in turn decrease the bandwidth;

- Resistors $R_3$ & $R_4$ → In order to increase the bandwidth and due to the limitation of

the relatively low transconductance $g_m$, feedback resistors $R_3$ and $R_4$ can be reduced to decrease the input resistance. However, the gain provided by feedback resistors, $R_3$ and $R_4$, will decrease and an additional thermal noise will be induced due to the lower value of the feedback resistance. TIA's output ($V_{out+}$ and $V_{out-}$) will therefore degrade. Because of this it is necessary to use techniques capable of increasing the bandwidth. The shunt peaking technique was chosen to do this.

- Inductors $L_1$ & $L_2$ → One of the techniques described in this dissertation was the shunt peaking technique, as described in section 2.3.3.2, and as mentioned in the previous topic, this technique was used in the TIA.

  In order to increase the bandwidth, inductors $L_1$ and $L_2$ are used to resonate the capacitance that limits the bandwidth. $L_1$ and $L_2$ values are set so as to work at an optimum group delay (avoiding the appearance of a unwanted peak near the frequency response).

- Transistors $M_5$ & $M_6$ → Ideally, it should directly connect the feedback resistors to the TIA's output ($V_{out+}$ and $V_{out-}$). However, the resistors $R_3$ and $R_4$ would consume unwanted current. Therefore, in order to achieve this ideal case, the transistors $M_5$ and $M_6$ are placed between the TIA's outputs and the feedback resistors, $R_3$ and $R_4$.

## 4.2 System analysis

To achieve an optimum gain performance, bandwidth and input-referred noise, it is important to get more insight into the design.

This section it will look at the TIA's small signal model to obtain mathematical expressions of this architecture. These mathematical expressions will provide information about the gain, bandwidth, input-referred noise, location of the poles and zeros.

### 4.2.1 Small signal model

This 65 nm technology presents a more complex model where the capacitors $C_{gs}$, $C_{gd}$, $C_{ds}$, $C_{sb}$ and $C_{db}$ are placed inside the transistor, as shown in Figure 4.2.

From Figures 4.1 and 4.2 and aplying a single-ended analysis in this circuit (considering half of the circuit), it is possible to design the small signal model as shown in Figure 4.3.

As presented in Figure 4.3, it is possible to conclude that the small signal model is extremely complex which makes the calculations very complicated. Therefore, for the sake of simplicity and in order to prove that a simpler model behaves similarly to the real answer, use of the simplest model is recommended for any type of calculation such as gain, bandwidth, and input referred noise.

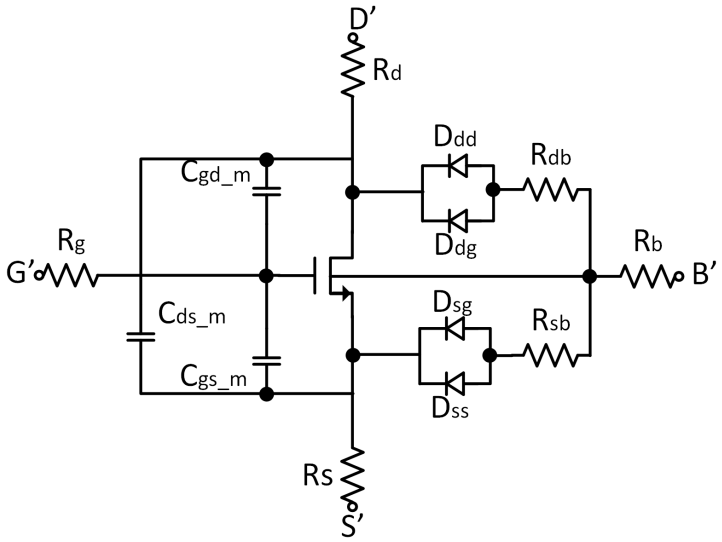



Figure 4.2: Equivalent circuit model for the 65 nm RF NMOS transistor.

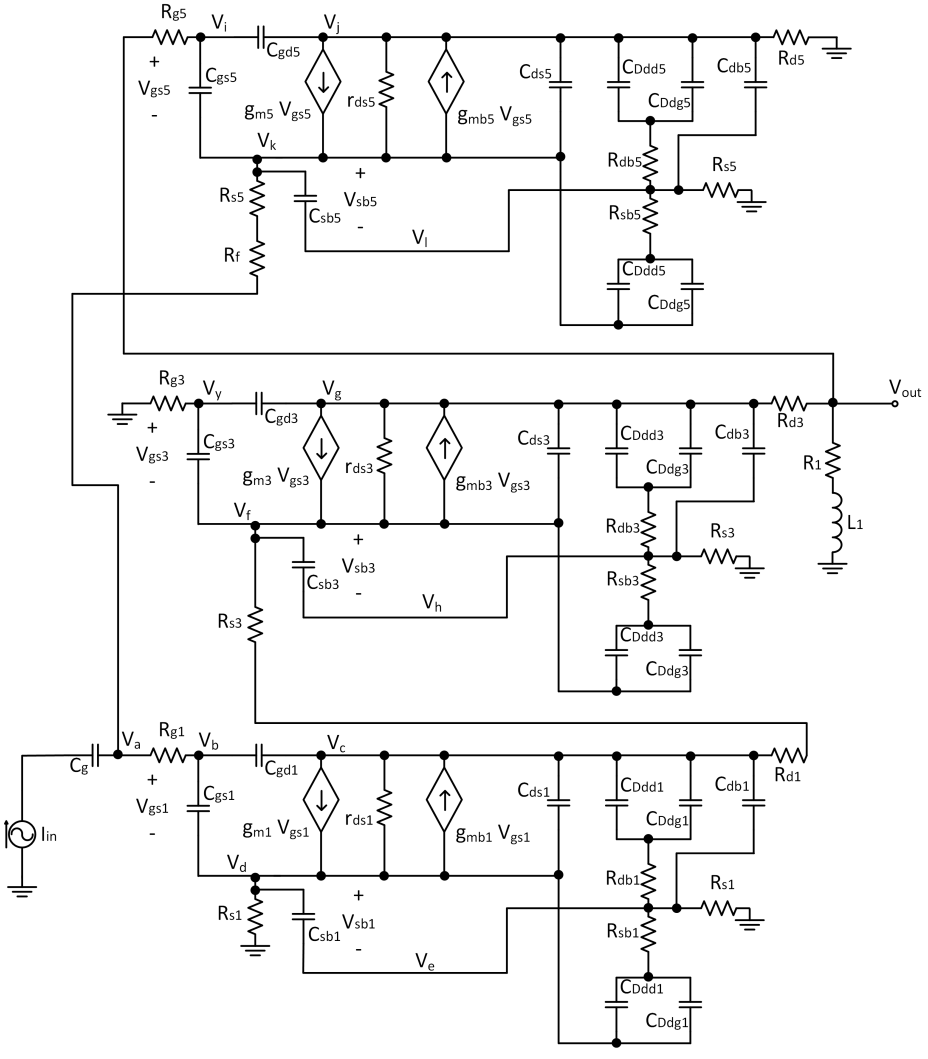



Figure 4.3: Small signal model of proposed circuit (complex model).

Subsequently, the simpler model will ignore the external transistor's resistances, except the resistor $R_g$ (ie. $R_d$, $R_s$, $R_b$, $R_{db}$ and $R_{sb}$) and also the external transistor's capacitors (ie. $C_{gd\_m}$, $C_{gs\_m}$, $C_{ds\_m}$, $C_{Ddds}C_{Ddgs}$, $C_{Dss}$ and $C_{Dsg}$), as shown in Figure 4.4.

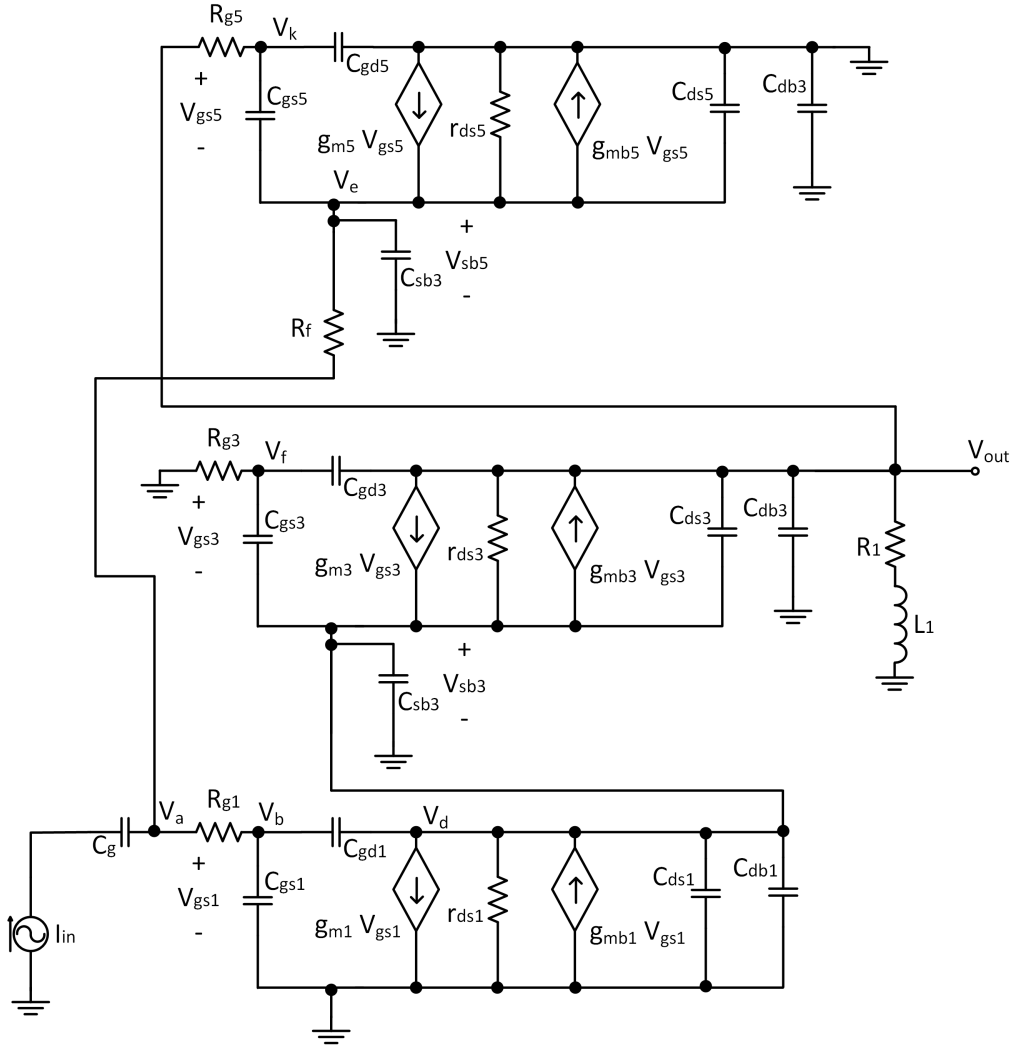



Figure 4.4: Small signal model of proposed circuit (simple model).

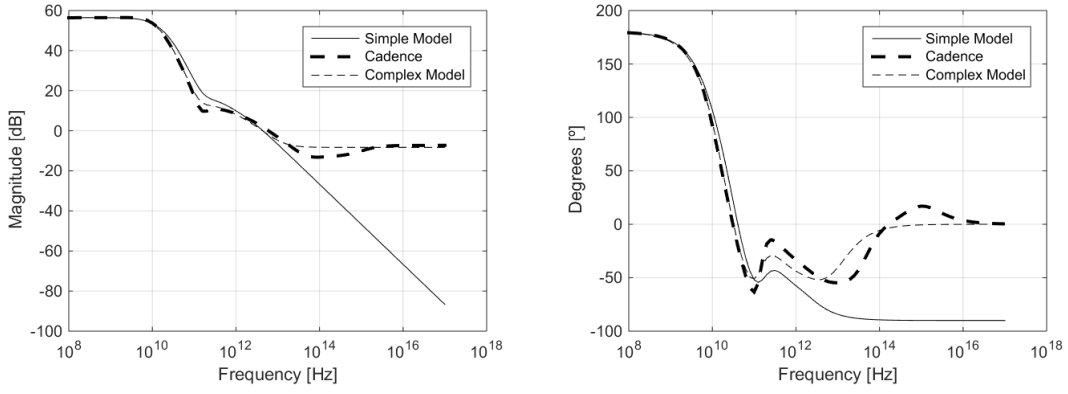
After designing the two small signal models (simple and complex) it is necessary to validate them by calculating their transfer functions ($\frac{V_{out}}{I_{in}}$), which are demonstrated in 4.2.1 (complex model) and 4.2.1 (simplest model).

$$\begin{cases} z_1 = \frac{1}{s\ C_{ddd1}} + R_{db3} \\ z_2 = \frac{1}{s\ C_{dss1}} + R_{sb1} \\ z_3 = \frac{1}{s\ C_{ddd3}} + R_{db3} \end{cases}$$

$$
\begin{cases}
z_4 = \frac{1}{s\ C_{dss3}} + R_{sb3} \\
z_5 = \frac{1}{s\ C_{ddd5}} + R_{db5} \\
z_6 = \frac{1}{s\ C_{dss5}} + R_{sb5} \\
\\
-I_{in} + \frac{V_a - V_k}{R_f + R_{s3}} + \frac{V_a - V_b}{R_{g1}} = 0 \\
\\
\frac{V_b - V_a}{R_{g1}} + (V_b - V_d)\ s\ C_{gs1} + (V_b - V_c)\ s\ C_{gd1} = 0 \\
\\
(V_d - V_b)\ s\ C_{gs1} - g_{m1}\ (V_b - V_d) + \frac{V_d}{R_{s1}} + (V_d - V_e)\ s\ C_{sb1} + \\
\frac{V_d - V_c}{r_{ds1}} + g_{mb1}\ (V_d - V_e) + (V_d - V_c)\ s\ C_{ds1} + \frac{V_d - V_e}{z_2} = 0 \\
\\
(V_c - V_b) s\ C_{gd1} + g_{m1}\ (V_b - V_d) + \frac{V_c - V_d}{r_{ds1}} - g_{mb1}\ (V_d - V_e) + \\
(V_c - V_d)\ s\ C_{ds1} + \frac{V_c - V_e}{z_1} + (V_c - V_e)\ s\ C_{db1} + \frac{V_c - V_f}{R_{d1} + R_{s3}} = 0 \\
\\
(V_e - V_d)\ s\ C_{sb1} + \frac{V_e - V_c}{z_1} + \frac{V_e - V_d}{z_2} + (V_e - V_c)\ s\ C_{db1} + \frac{V_e}{R_{b1}} = 0 \\
\\
(V_f - V_y)\ s\ C_{gs3} - g_{m3}\ (V_y - V_f) + g_{mb3}\ (V_f - V_h) + \frac{V_f - V_g}{r_{ds3}} + \\
(V_f - V_g)\ s\ C_{ds3} + (V_f - V_h)\ s\ C_{sb3} + \frac{V_f - V_h}{z_4} + \frac{V_f - V_c}{R_{s3} + R_{d1}} = 0 \\
\\
\frac{V_y}{R_{g3}} + (V_y - V_f)\ s\ C_{gs3} + (V_y - V_g)\ s\ C_{gd3} = 0 \\
\\
(V_g - V_y)\ s\ C_{gd3} + g_{m3}\ (V_y - V_f) - g_{mb3}\ (V_f - V_h) + \frac{V_g - V_f}{r_{ds3}} + \\
(V_g - V_f)\ s\ C_{ds3} + \frac{V_g - V_h}{z_3} + (V_g - V_h)\ s\ C_{db3} + \frac{V_g - V_{out}}{R_{d3}} = 0 \\
\\
(V_h - V_f)\ s\ C_{sb3} + \frac{V_h - V_g}{z_3} + \frac{V_h - V_f}{z_4} + (V_h - V_g)\ s\ C_{db3} + \frac{V_h}{R_{b3}} = 0 \\
\\
\frac{V_{out} - V_g}{R_{d3}} + \frac{V_{out}}{R_1 + s\ L_1} + \frac{V_{out} - V_i}{R_{g5}} = 0 \\
\\
\frac{V_i - V_{out}}{R_{g5}} + (V_i - V_k)\ s\ C_{gs5} + (V_i - V_j)\ s\ C_{gd5} = 0 \\
\\
\frac{V_j}{R_{d5}} + (V_j - V_l)\ s\ C_{db5} + \frac{V_j - V_l}{z_5} + (V_j - V_k)\ s\ C_{ds5} + (V_j - V_k)/r_{ds5} - \\
g_{mb5}\ (V_k - V_l) + g_{m5}\ (V_i - V_k) + (V_j - V_i)\ s\ C_{gd5} = 0 \\
\\
(V_l - V_j)\ s\ C_{db5} + \frac{V_l}{R_{b5}} + \frac{V_l - V_j}{z_5} + \frac{V_l - V_k}{z_6} + (V_l - V_k)\ s\ C_{sb5} = 0 \\
\\
\frac{V_k - V_l}{z_6} + (V_k - V_l)\ s\ C_{sb5} + (V_k - V_j)\ s\ C_{ds5} + \frac{V_k - V_j}{r_{ds5}} \\
+ g_{mb5}\ (V_k - V_l) - g_{m5}\ (V_i - V_k) + \frac{V_k - V_a}{R_{s5} + R_f} + (V_k - V_i)\ s\ C_{gs5} = 0
\end{cases}
\tag{4.1}
$$

$$
\begin{cases}
-I_{in} + \frac{V_a - V_e}{R_f} + \frac{V_a - V_b}{R_{g1}} = 0 \\
\frac{V_b - V_a}{R_{g1}} + V_b \ s \ C_{gs1} + (V_b - V_d) \ s \ C_{gd1} = 0 \\
(V_d - V_b) \ s \ C_{gd1} + g_{m1} \ V_b + \frac{V_d}{r_{ds1}} + V_d \ s \ C_{ds1} + V_d \ s \ C_{db1} + \\
(V_d - V_{out}) \ s \ C_{ds3} + \frac{V_d - V_{out}}{r_{ds3}} + g_{mb3} \ V_d + V_d \ s \ C_{sb3} - \\
g_{m3} \ (V_f - V_d) + (V_d - V_f) \ s \ C_{gs3} = 0 \\
\frac{V_f}{R_{g3}} + (V_f - V_d) \ s \ C_{gs3} + (V_{f-Vout}) \ s \ C_{gd3} = 0 \\
(V_{out} - V_f) \ s \ C_{gd3} + g_{m3} \ (V_f - V_d) - g_{mb3} \ V_d + \\
\frac{V_{out} - V_d}{r_{ds3}} + (V_{out} - V_d) \ s \ C_{ds3} + V_{out} \ s \ C_{db3} + \frac{V_{out}}{R_1} + \frac{V_{out} - V_k}{R_{g5}} = 0 \\
\frac{V_k - V_{out}}{R_{g5}} + V_k \ s \ C_{gd5} + (V_k - V_e) \ s \ C_{gs5} = 0 \\
(V_e - V_k) \ s \ C_{gs5} - g_{m5} \ (V_k - V_e) + g_{mb5} \ V_e + \\
\frac{V_e}{r_{ds5}} + V_e \ s \ C_{ds5} + V_e \ s \ C_{sb5} + \frac{V_e - V_a}{R_f} = 0
\end{cases}
\tag{4.2}
$$

After obtaining the simple and complex equations' systems, the next step lies in replacing the parameters by real values (in this case, obtained in cadence) and validating the simple model, as it can be observed in Figures 4.5 a) and b).




a b

Figure 4.5: Comparison of simulated frequency response, a), and phase, b), of simple model, complex model and real model (Cadence).

From Figures 4.5 a) and b), it can be concluded that the results obtained based on the simplest model return a good approximation of the real model because both of them have

roughly the same static gain of 56.45 dB and the same bandwidth of 10 GHz, as shown in Figure 4.6.

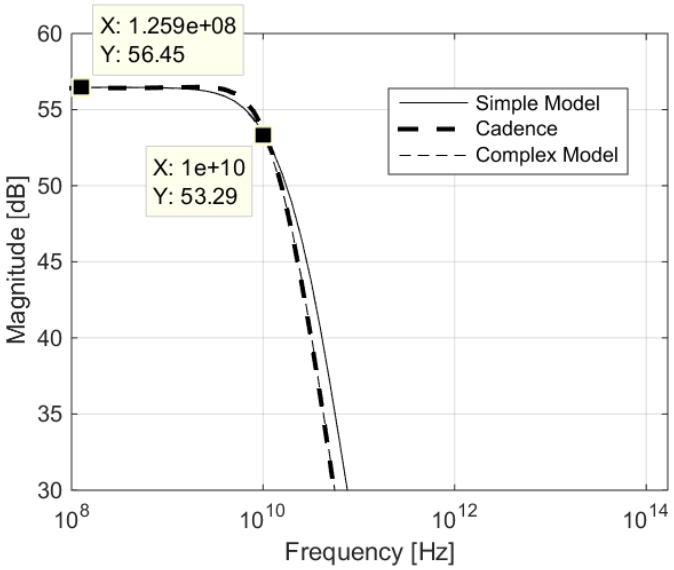



Figure 4.6: Comparison zoom of simulated frequency response of simple model, complex model and real model (Cadence).

It becomes advantageous to use the simplest model in order to obtain the static gain, bandwidth, and input referred noise due to the number of equations involved which in turn allows easier optimization of the circuit.

### 4.2.2 Transimpedance gain, location of poles and zeros

As shown in section 4.2.1, it is very difficult to represent, by mathematical formulas, the actual behaviour of the circuit. The closer a mathematical formula is from reality the more complex it will be. However, due to the increasing dependency between them the greater will be the difficulty in parametrizing the component values.

A simple solution was found with a similar response to the reality, as shown in 4.2.1. However, it is still complex to calculate the poles, zeros and the input referred noise.

In this section, in order to calculate the static gain, the simplest model will be used. However, for the calculation of the poles, zeros and input referred noise, even more simple equations will be used in order for it to be possible to obtain expressions which can be interpreted (the input referred noise will be calculated in section 4.3.2).

To calculate the static gain, open circuited capacitors are considered, at low frequency. Using the formulas presented in 4.2.1 with s = 0 it is possible to obtain the following expression for the static gain:

$$Z(0)_T = -\frac{g_{m1}\ R_1\ r_{ds1}\ (1+g_{m3}\ r_{ds3})\ (r_{ds5}+R_f+g_{m5}\ r_{ds5}\ R_f)}{(r_{ds1}+r_{ds3}+(g_{m3}+g_{mb3})\ r_{ds1}\ r_{ds3})\ (1+g_{m5}\ r_{ds5})+R_1\ \Big(1 + g_{mb3}\ r_{ds1}+g_{m5}\ (1+r_{ds1}\ (g_{m1}+g_{mb3}+g_{m1}\ g_{m3}\ r_{ds3}))\ r_{ds5}\Big)}\ \Omega \tag{4.3}$$

In order to increase the static gain it is necessary to maximize the $g_{m1}$ value. This, results in:

$$Z(0)_T = -\frac{r_{ds5}+R_f+g_{m5}\ r_{ds5}\ R_f}{g_{m5}\ r_{ds5}}\ \Omega \tag{4.4}$$

From equation 4.4, considering $g_{m5}\ r_{ds5}\ R_f$ greater than $r_{ds5}$ and $R_f$, the following expression is yielded:

$$\begin{aligned} Z(0)_T &= -\frac{g_{m5}\ r_{ds5}\ R_f}{g_{m5}\ r_{ds5}}\ \Omega \\ &= -\ R_f\ \Omega \end{aligned} \tag{4.5}$$

Equation 4.5 shows that the TIA's static gain is approximately equal to the value of the feedback resistance. However, it is not possible to only increase the feedback resistance while the TIA doesn't reach the desired static gain because the feedback resistance influences not only the bandwidth but also the input referred noise.

It is therefore necessary to determine the location of the circuit's poles and conclude how the feedback resistance influences the bandwidth.

As previously stated, the calculation of the poles and zeros are originated by equations simpler than those from the simpler model (the simple model is represented in Figure 4.4) in order to simplify the calculations.

Due to the amount of capacitors and other significant variables that influence the complexity of the equations, in order to simplify the calculations, only the capacitor $C_{gs}$ was considered because it is the one that most influences of all the capacities. So all the other internal capacitors were neglected (the common gate, $M_3$ and $M_4$, and the body effect are also neglected). The system of equations is therefore presented as follows:

$$\begin{cases} -I_{in}+V_a\ s\ C_{gs1}+\frac{V_a-V_k}{R_f}=0 \\ \\ \frac{V_{out}}{R_1+s\ L_1}+g_{m1}\ V_a+(V_{out}-V_k)\ s\ C_{gs5}=0 \\ \\ -g_{m5}\ (V_{out}-V_k)-(V_{out}-V_k)\ s\ C_{gs5}-\frac{V_a-V_k}{R_f}=0 \end{cases} \tag{4.6}$$

Solving the previous equations in order to $\frac{V_{out}}{I_{in}}$, the resulting equation can be seen in ( 4.7):

$$Z(s)_T = \frac{V_{out}}{I_{in}}\ (s) = -\frac{(R_1 + L_1\ s)\ (g_{m1} + g_{m1}g_{m5}\ R_f - C_{gs5}\ s + C_{gs5}\ g_{m1}\ R_f\ s)}{(C_{gs1} + C_{gs5})\ s + g_{m5}\ (1 + C_{gs1}\ R_f\ s + g_{m1}\ (R_1 + L_1\ s)) + C_{gs5}\ s\ \Big(g_{m1}\ (R_1 + L_1\ s) + C_{gs1}\ s\ (R_1 + R_f + L_1\ s)\Big)}\ \Omega \tag{4.7}$$

After obtaining equation 4.7, it is possible to compare it with the simpler model's results obtained in 4.2.1 and validate whether the two responses are similar, as shown in Figure 4.7.

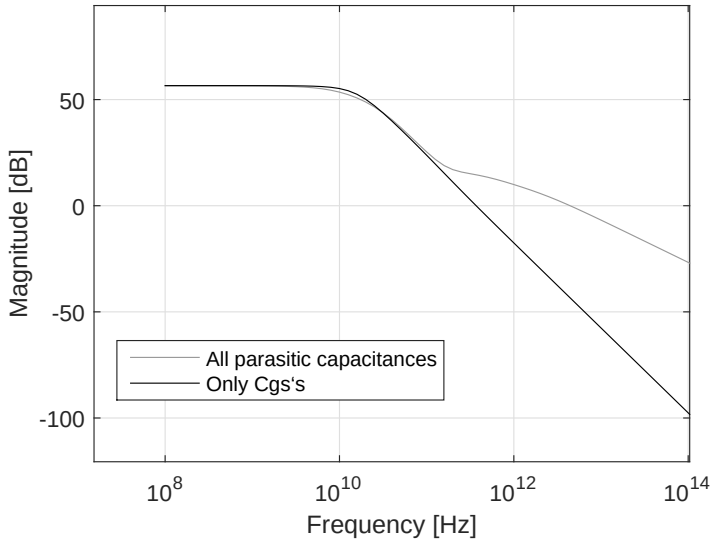



Figure 4.7: Comparison between the simulated frequency response of the simple model with all the parasitic capacitances and the simple model only with the $C_{gs}$ capacitors.

From Figure 4.7 it is possible to conclude that using the expression based on the values of $C_{gs}$ will provide results similar to the simpler model, presented in section 4.2.1. Since both outputs have a similar frequency response, within the desired bandwidth, it can be concluded that equation 4.7 results in a good approximation to reality (within the desired bandwidth).

So the next step will be to obtain the dominant zeros and poles of equation 4.7.

In order to obtain the zeros it is necessary to equalize the numerator to zero as follows:

$$(R_1 + L_1\ s)\ (g_{m1} + g_{m1}g_{m5}\ R_f - C_{gs5}\ s + C_{gs5}\ g_{m1}\ R_f\ s) = 0 \tag{4.8}$$

Putting s in evidence, results in:

$$s = -\frac{R_1}{L_1} \tag{4.9}$$

$$s = -\frac{g_{m1} + g_{m1}\ g_{m5}\ R_f}{C_{gs5}\ (-1 + g_{m1}\ R_f)} \tag{4.10}$$

For calculation of the poles it is necessary to equalize the denominator to zero, as shown in the following equation:

$$\begin{aligned}(C_{gs1}+C_{gs5})\ s+g_{m5}\ (1+C_{gs1}\ R_f\ s+g_{m1}\ (R_1+L_1\ s))+C_{gs5}\ s\ \Big(g_{m1}\\ (R_1+L_1\ s)+C_{gs1}\ s\ (R_1+R_f+L_1\ s)\Big)=0\end{aligned} \tag{4.11}$$

Since the denominator shows a cubic equation, as seen in ( 4.11), it is necessary to use the general solution of the cubic equation. So putting the equation 4.11 in the form of $s^3\ a+s^2\ b+s\ c+d=0$ results in:

$$\begin{aligned}s^3\ C_{gs5}\ C_{gs1}\ L_1+s^2\ (C_{gs5}\ g_{m1}\ L_1+C_{gs5}\ C_{gs1}\ R_1+C_{gs5}\ C_{gs1}\ R_f)+s\ \Big(C_{gs1}+C_{gs5}\\ +g_{m5}\ C_{gs1}\ R_f+g_{m5}\ g_{m1}\ L1+C_{gs5}\ g_{m1}\ R_1\Big)+g_{m5}+g_{m5}\ g_{m1}\ R_1=0\end{aligned} \tag{4.12}$$

[25] shows how to calculate a cubic equation:

$$\begin{cases}\Delta_0=b^2-3\ a\ c\\ \Delta_1=2\ b^3-9\ a\ b\ c+27\ a^2\ d\\ C=\sqrt[3]{\frac{\Delta_1\pm\sqrt{\Delta_1^2-4\Delta_0^3}}{2}}\\ \zeta=\frac{1}{2}+\frac{1}{2}\ \sqrt{3\imath}\\ s_k=-\frac{1}{3a}\ \left(b+\zeta^k\ C+\frac{\Delta_0}{\zeta^k\ C}\right),\ k\in\{0,1,2\}\end{cases} \tag{4.13}$$

Combining ( 4.12) and ( 4.13) results in:

$$s\cong-\frac{g_{m5}\ R_1+g_{m1}\ R_f}{C_{gs5}\ R_1-C_{gs5}} \tag{4.14}$$

$$s\cong-\frac{g_{m5}+g_{m1}\ g_{m5}\ \sqrt{R_f^2-R_1}}{C_{gs1}+g_{m1}\ g_{m5}\ L_1+C_{gs5}\ g_{m1}\ g_{m5}\ R_f+g_{m1}\ R_1} \tag{4.15}$$

$$s\cong-\frac{g_{m5}-g_{m1}\ g_{m5}\ \sqrt{R_f-R_1}}{C_{gs1}+g_{m1}\ g_{m5}\ L_1+C_{gs1}\ g_{m5}\ R_f+g_{m1}\ R_1} \tag{4.16}$$

From equations ( 4.14), ( 4.15) and ( 4.16) and making the study regarding to the feedback resistance, it is possible to conclude that the higher the feedback resistance value is, $R_f$, the smaller will be the pole in ( 4.16) and therefore the less bandwidth the circuit will have.

In order to prove the relation between the poles and the feedback resistance the bode diagram was calculated for various values of resistance, $R_f$, as seen in Figures 4.8 a) and b).

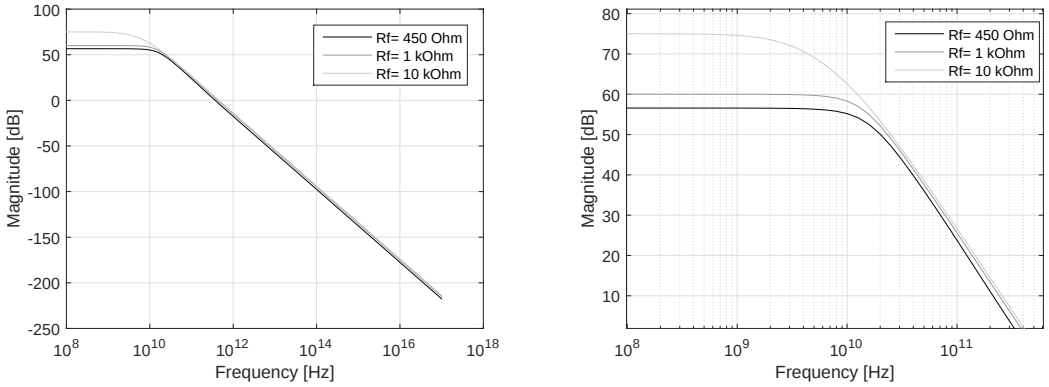



Figure 4.8: Comparison between simulated frequency responses of diferent feedback resistance values. b) is a zoom of a).

Table 4.1: Static gain and bandwidth depending on the feedback resistance $R_f$, from Figure 4.8.

| **Rf** | **450 Ω** | **1 kΩ** | **10 kΩ** |
|---|---|---|---|
| **Gain (dB)** | 56.58 | 60.02 | 74.97 |
| **Bandwith (GHz)** | 15 | 12.6 | 3.2 |

From Table 4.1 it can be concluded the same as with the poles - The higher the feedback resistance, the lower the bandwidth. Because of this trade off in the static gain and bandwidth, it is important to know what are the needs of each project, in order to obtain a correct optimization.

### 4.2.3 Noise analysis

This section will analyse the input referred noise of the circuit at low frequency.

As mentioned in section 4.2.2, the equation ( 4.7) is a good approximation to the real circuit (regarding to the desired bandwidth). So for the calculation of the output and input noise this same approach will be used, in order to simplify the calculations.

Figure 4.9 represents the small signals model of the equation ( 4.7) with the noise addition imposed by the resistors and the transistors. Using the superposition theorem it is possible to calculate the output noise that each component imposes on the circuit, as it can be seen in the following equations ( 4.17 to 4.20):

$$V_{n\,R_f} = \frac{(R_1 + L_d s)\,(g_{m1} + g_{m1} g_{m5} R_f - C_{gs5}\,s + C_{gs5} g_{m1} R_f s)\,I_{n\,R_f}}{g_{m5}\,(1 + C_{gs1} R_f\,s + g_{m1}\,(R_1 + L_d\,s)) + s\,(C_{gs5}\,(1 + g_{m1}\,(R_1 + L_d\,s)) + C_{gs1}\,\big(1 + C_{gs5}\,s\,(R_1 + R_f + L_d\,s)\big))} \tag{4.17}$$

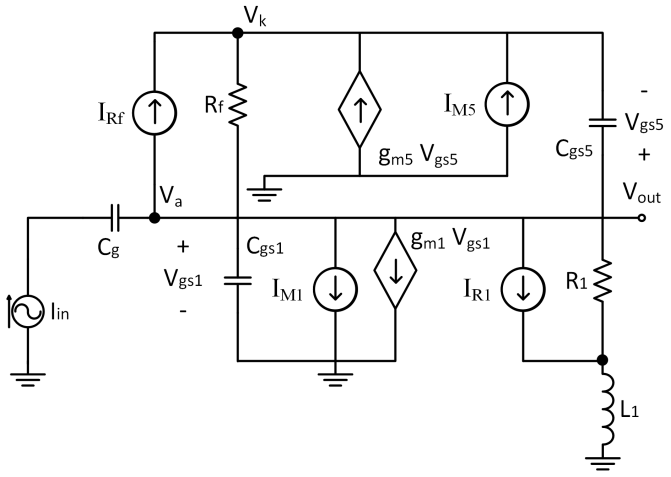



Figure 4.9: Small signal model of proposed circuit (simplified model).

$$V_{n\,M_1} = -\frac{(R_1 + L_d\,s)\,(g_{m5} + C_{gs1}g_{m5}R_f\,s + s\,(C_{gs1} + C_{gs5} + C_{gs1}C_{gs5}R_f\,s))\,I_{n\,M_1}}{g_{m5}\,(1 + C_{gs1}R_f\,s + g_{m1}\,(R_1 + L_d\,s)) + s\,(C_{gs5}\,(1 + g_{m1}\,(R_1 + L_d\,s)) + C_{gs1}\,\Big(1 + C_{gs5}\,s\,(R_1 + R_f + L_d\,s)\Big)\Big)} \tag{4.18}$$

$$V_{n\,R_1} = -\frac{(R_1 + L_d\,s)(g_{m5} + C_{gs1}g_{m5}R_f\,s + s\,(C_{gs1} + C_{gs5} + C_{gs1}C_{gs5}R_f\,s))\,I_{n\,R_1}}{g_{m5}\,(1 + C_{gs1}R_f\,s + g_{m1}\,(R_1 + L_d\,s)) + s\,(C_{gs5}\,(1 + g_{m1}\,(R_1 + L_d\,s)) + C_{gs1}\,\Big(1 + C_{gs5}\,s\,(R_1 + R_f + L_d\,s)\Big)\Big)} \tag{4.19}$$

$$V_{n\,M_5} = \frac{(R_1 + L_d\,s)\,(g_{m1} + g_{m1}g_{m5}R_f - C_{gs5}\,s + C_{gs5}g_{m1}R_f\,s)\,I_{n\,M_5}}{g_{m5}\,(1 + C_{gs1}R_f\,s + g_{m1}\,(R_1 + L_d\,s)) + s\,(C_{gs5}\,(1 + g_{m1}\,(R_1 + L_d\,s)) + C_{gs1}\,\Big(1 + C_{gs5}\,s\,(R_1 + R_f + L_d\,s)\Big)\Big)} \tag{4.20}$$

Combining $\overline{I_{n,Rf}} = \sqrt{\frac{4kT}{R_f}}$, $\overline{I_{n,R1}} = \sqrt{\frac{4kT}{R_1}}$, $\overline{I_{n,M1}} = \sqrt{4kTgm_1}$, $\overline{I_{n,M5}} = \sqrt{4kTgm_5}$ and increasing each of the equations to the square and adding them up it is possible to obtain the total output referred noise (to simplify the expression, the noise at low frequencies is considered):

$$\overline{\left|Vout^2_{n,out}\right|} \approx \frac{4KTR_1\,(g^2_{m5}R_f + g_{m1}g^2_{m5}R_1R_f + g^2_{m1}R_1\,(1 + 3g_{m5}R_f + g^2_{m5}R^2_f))}{(g_{m5} + g_{m1}g_{m5}R_1)^2R_f} \tag{4.21}$$

From equation ( 4.21) and dividing it by the circuit's gain, results in noise on the entry (again, the circuit at low frequencies is considered in order to simplify the expression):

$$\overline{\left|I_{n,in}^2\right|} \approx \frac{4KT\left(g_{m5}^2 R_f + g_{m1} g_{m5}^2 R_1 R_f + g_{m1}^2 R_1\left(1 + 3g_{m5} R_f + g_{m5}^2 R_f^2\right)\right)}{R_1 R_f\left(g_{m1} + g_{m1} g_{m5} R_f\right)^2} \tag{4.22}$$

Considering the approximation $g_{m5} \to 0$, we get:

$$\overline{\left|I_{n,in}^2\right|} \approx \frac{4KT}{R_f} \tag{4.23}$$

As previously stated in section 2.2.2 and as proved in the circuit under study, the input referred noise depends essentially on the feedback resistance. As can be seen in the equation ( 4.23), in order to reduce the input referred noise, the resistance value, $R_f$, must be maximized.

### 4.2.4 Input Impedance

This section will discuss the importance of the TIA's input impedance.

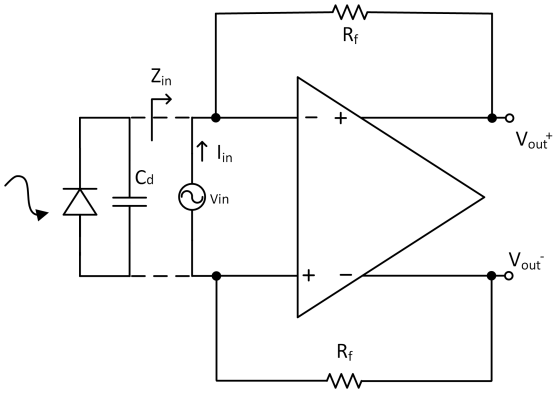



Figure 4.10: Input impedance calculation.

As shown in Figure 4.10, the photodiode presents capacity $C_d$. In order for the current transmitted, by the photodiode, to be fully received by the TIA low input impedance is necessary in this circuit. It is therefore important to calculate the input impedance of the circuit ($\frac{V_{in}}{I_{in}}$). Since the open loop gain (Ad) is not infinite:

$$V_{out} = A_d\left[V^+ - V^-\right] \tag{4.24}$$

Considering that $V^+ - V^- = -V_{in}$ , results in:

$$V_{out} = -A_d\, V_{in} \tag{4.25}$$

Given the path between $V_{out}^+$ and $V_{out}^-$ and by stressing $I_{in}$, we get:

$$\begin{aligned} &-V_{out}^- + I_{in}\, R_f - V_{in} + I_{in}\, R_f + V_{out}^+ = 0 \Leftrightarrow \\ &2\, I_{in}\, R_f + V_{out} - V_{in} = 0 \Leftrightarrow \end{aligned} \tag{4.26}$$

Combining ( 4.25) and ( 4.26) results in:

$$
\begin{aligned}
&2\, I_{in}\, R_f - V_{in}\, Ad - V_{in} = 0 \Leftrightarrow \\
&2\, I_{in}\, R_f - V_{in}\, [1 + Ad] = 0 \Leftrightarrow \\
&V_{in}\, [1 + Ad] = 2\, I_{in}\, R_f \Leftrightarrow \\
&Z_{in} = \frac{V_{in}}{I_{in}} = \frac{2\, R_f}{1 + Ad}
\end{aligned}
\tag{4.27}
$$

From the equation ( 4.27) it is possible to conclude that the higher the feedback resistance, $R_f$, the higher the input impedance, $Z_{in}$, will be. Therefore, in order to decrease the input impedance, it is necessary to increase the open loop gain, Ad.

## 4.3 Results - Corner Simulations

The proposed TIA is designed in 65 nm CMOS technology with a supply voltage of 1.2 V and with a photodiode capacitance of 300 fF. RF NMOS and PMOS transistors are used in high frequency operations. The whole system is characterized in a SPECTRE environment.

### 4.3.1 Transimpedance gain response

The SPECTRE simulation of transimpedance gain response is shown in Figure 4.11. Transimpedance gain response is studied in two different scenarios - when there is no broadband techniques (using only a resistive load) and when there is a compensation with shunt peaking. It shows that without any compensation the bandwidth is 7.8 GHz and also that incorporating the shunt peaking technique will increase the bandwidth up to 10.3 GHz, as shown in Figure 4.11.

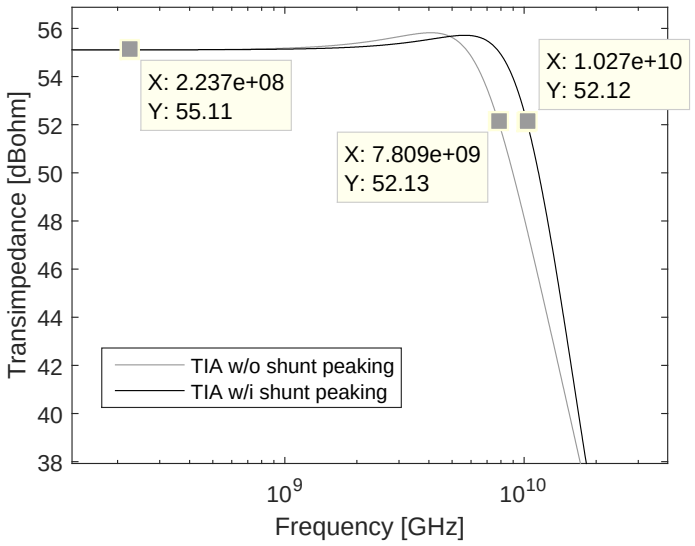



Figure 4.11: Transimpedance gain response of proposed TIA.

It is therefore possible to establish the bandwidth increase with the use of inductors:

$$\left(1 - \frac{10.27}{7.809}\right) \times 100 = 31.5\% \tag{4.28}$$

From the equation 4.28 it was concluded that the bandwidth is extended by 31.5% against the design only with a resistive load, $R_1$. So, the proposed architecture achieves 55.1 dBΩ of transimpedance gain and a 3-dB bandwidth of 10.3 GHz (Typical-Typical process).

### 4.3.2 Input referred noise

Figure 4.12 shows the simulated input referred noise of the circuit with and without shunt peaking. In the expression for the input referred noise, it should be noted that the thermal noise of resistors and transistors is only represented at low frequencies. However, at higher frequencies, the input referred noise starts to increase because of the frequency dependent factors in the noise expression.

As shown in Figure 4.12, at low frequencies, the input referred noise is similar between the TIA without shunt peaking and with shunt peaking, but at higher frequencies, especially around the 3-dB point, the input referred noise is improved by using shunt peaking. At the 3-dB point, the input referred noise in the TIA without shunt peaking is 12 $pA/\sqrt{Hz}$ and in the TIA with shunt peaking is 8.7 $pA/\sqrt{Hz}$.

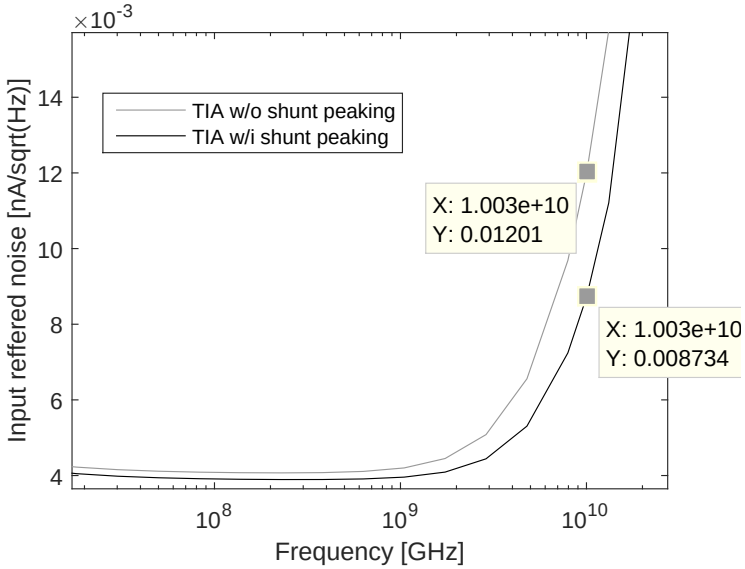



Figure 4.12: Simulated input referred noise.

### 4.3.3 TIA corners

Like the simulations carried out in several corners in section 3.2.1, in this topic it is also necessary to simulate the circuit in different conditions (in the process and temperature)

to confirm that it complies with the defined specifications. These specifications defined by Conseil Européen pour la Recherche Nucléaire (CERN) are the following:

- Operating temperature range → Between -40 ºC and 100 ºC;
- Supply voltage → Between 1.2 V and 1.32 V;
- Low cutoff frequency → Maximum of 100 kHz;
- High cutoff frequency → Minimum of 3.5 GHz;
- Minimum input current (start of life conditions) → 20 $\mu A_{pp}$;
- Total integrated input reffered noise → Maximum of 1.45 $\mu A$;

Once it is known what it takes to measure the specifications in the corners, the next tables show the process corners' results.

Table 4.2: TIA simulation results - Gain.

| Gain [dB] | FF | | | TT | | | FS | | | SS | | | SF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC |
| **Vdd 1.1** | 54.28 | 54.1 | 53.92 | 54.94 | 54.94 | 54.88 | 55.31 | 55.19 | 55.05 | 55.15 | 55.44 | 55.52 | 54.39 | 54.58 | 54.61 |
| **Vdd 1.2** | 54.38 | 54.18 | 53.99 | 55.18 | 55.11 | 55.02 | 55.45 | 55.29 | 55.14 | 55.64 | 55.77 | 55.78 | 54.8 | 54.86 | 54.83 |
| **Vdd 1.32** | 54.43 | 54.23 | 54.04 | 55.34 | 55.22 | 55.12 | 55.52 | 55.34 | 55.19 | 55.97 | 55.98 | 55.96 | 55.08 | 55.05 | 55 |

Table 4.3: TIA simulation results - Bandwidth.

| Bandwidth [GHz] | FF | | | TT | | | FS | | | SS | | | SF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC |
| **Vdd 1.1** | 11.98 | 11.77 | 11.32 | 8.481 | 8.979 | 9.14 | 9.894 | 10.02 | 9.844 | 5.578 | 6.535 | 6.993 | 6.934 | 7.916 | 8.318 |
| **Vdd 1.2** | 13.03 | 12.74 | 12.18 | 9.735 | 10.09 | 10.16 | 10.86 | 10.81 | 10.63 | 6.771 | 7.565 | 8.014 | 8.342 | 9.028 | 9.371 |
| **Vdd 1.32** | 13.86 | 13.47 | 13 | 10.84 | 10.97 | 10.97 | 11.76 | 11.59 | 11.36 | 7.985 | 8.579 | 8.9 | 9.705 | 10.23 | 10.44 |

Table 4.4: TIA simulation results - Input reffered noise.

| Input reffered noise [$\mu$A] | FF | | | TT | | | FS | | | SS | | | SF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC |
| **Vdd 1.1** | 0.22 | 0.252 | 0.285 | 0.213 | 0.247 | 0.281 | 0.228 | 0.253 | 0.283 | 0.224 | 0.26 | 0.296 | 0.23 | 0.26 | 0.296 |
| **Vdd 1.2** | 0.216 | 0.248 | 0.282 | 0.211 | 0.245 | 0.278 | 0.216 | 0.245 | 0.276 | 0.223 | 0.258 | 0.294 | 0.222 | 0.254 | 0.287 |
| **Vdd 1.32** | 0.213 | 0.246 | 0.279 | 0.21 | 0.244 | 0.277 | 0.21 | 0.24 | 0.27 | 0.222 | 0.257 | 0.292 | 0.218 | 0.25 | 0.282 |

As observed in table 4.2, it is expected that the static gain will not vary much due to the fact that this is approximately equal to the feedback resistance's value, $R_f$. It is also noted that the higher the temperature, the lower the static gain will be because the feedback resistance will decrease with the temperature increase.

Regarding the bandwidth table (table 4.3), greater oscillations are observed because it does not only depend on the feedback resistance, $R_f$, but is also influenced by other factors, as shown in section 4.2.2. As previously stated, as the static gain decreases with the temperature increase, the bandwidth will necessarily increase, as expected.

From Table 4.4 it is expected that the total integrated input referred noise does not over-oscillate because it depends essentially on the resistances $R_f$ and $R_d$. Considering that the resistances do not change much in the processes, the total integrated input

referred noise will also not vary much. It is also noted that the total integrated input referred noise is low because it is a differential TIA.

### 4.3.4 Eye diagram

The TIA's output eye diagram for an input Pseudorandom Binary Sequence (PRBS) current of 20 $\mu A_{pp}$ is shown in Figure 4.13, which illustrates the clear eye opening in the eye diagram with a peak to peak jitter of 31.34 ps. The high bandwidth achieved in the design prevents the vertical closure of the eye's data.

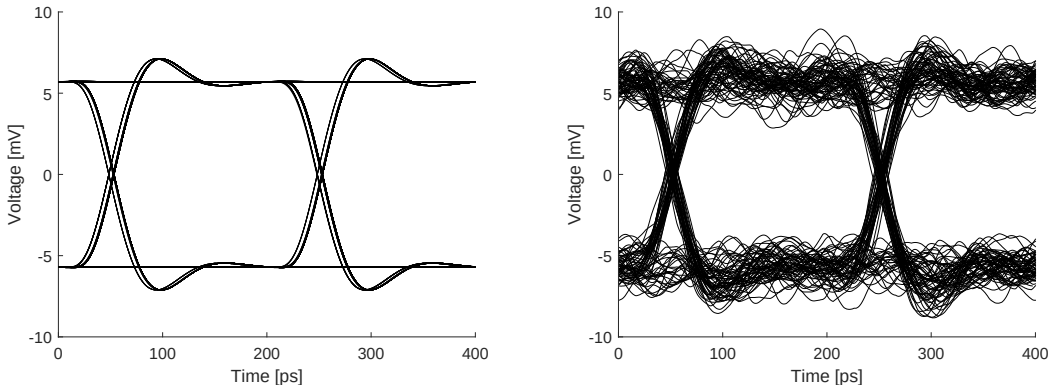



Figure 4.13: Output eye diagram - a) without noise; b) with noise.

### 4.3.5 Layout

Once the proposed TIA has been tested and validated in all the processed corners, it is necessary to implement the layout. In the end, the main goal remains to occupy the smallest possible area and get closer results to the schematic results. So after the layout implementation, the next step is to simulate all the processes using the TIA's layout.

Figure 4.14 shows the layout of the proposed design. In the middle of the figure the entire block of the TIA is represented except the inductors that are placed on the left and right.

Like in section 3.2.2.5, the main objectives are to:

- Implement the TIA's layout in order to make the circuit as symmetrical as possible in order to get an identical answer to the schematic;
- Occupy the minimum area possible.

Considering that the area occupied by this block is 575 by 258 $\mu m^2$, and the chip provided by CERN is 1750 by 40 $\mu m^2$, the percentage of this block's occupying area is as follows:

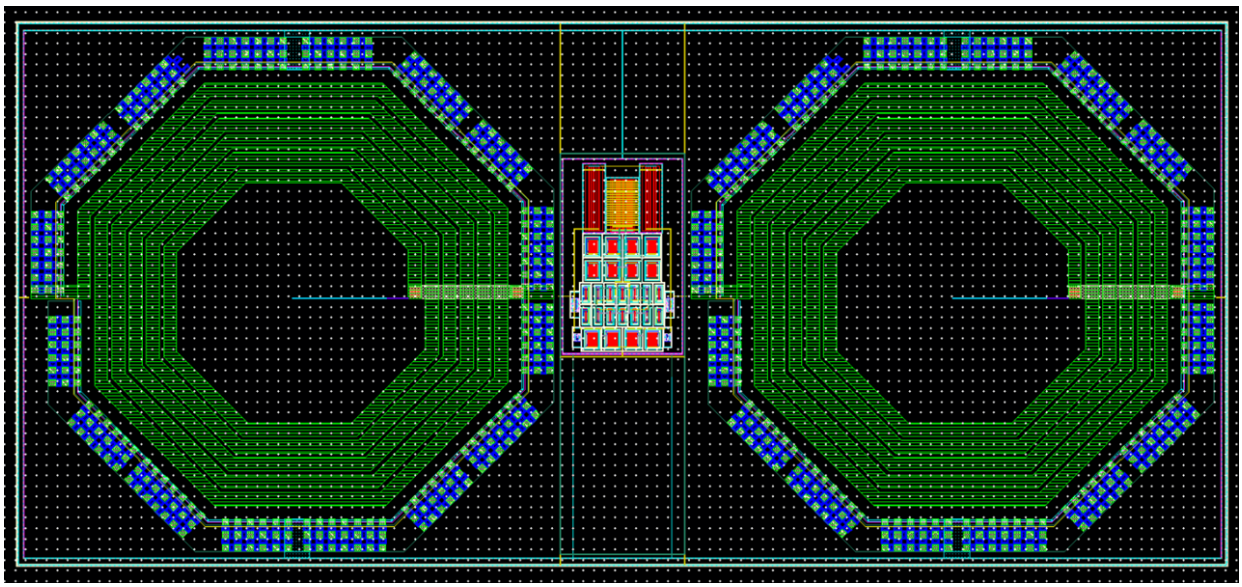


Figure 4.14: Layout implementation of the proposed TIA.

$$\begin{aligned} Percentage\ occupied\ in\ chip &= \frac{575 \times 258}{1750 \times 400} \times 100\ (\%) \\ Percentage\ occupied\ in\ chip &\approx 21.2\ (\%) \end{aligned} \tag{4.29}$$

It should be noted, from equation 4.29, that the TIA occupies approximately 21.2% of the area of the chip. However, the inductors occupy 8.7% each, which means that 17.4% of the total TIA's area is mainly occupied by these inductors.

Once the design is implemented, the next step is to simulate the layout in all the processes, as shown in tables 4.5, 4.6 and 4.7.

Table 4.5: TIA simulation results - Gain.

| Gain [dB] | FF | | | TT | | | FS | | | SS | | | SF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC |
| **Vdd 1.1** | 55.08 | 54.95 | 54.79 | 55.72 | 55.72 | 55.66 | 56.08 | 55.98 | 55.87 | 55.89 | 56.15 | 56.21 | 55.18 | 55.34 | 55.35 |
| **Vdd 1.2** | 55.23 | 55.06 | 54.87 | 56 | 55.93 | 55.83 | 56.25 | 56.12 | 55.98 | 56.45 | 56.53 | 56.5 | 55.64 | 55.66 | 55.61 |
| **Vdd 1.32** | 55.34 | 55.16 | 54.95 | 56.19 | 56.09 | 55.97 | 56.37 | 56.22 | 56.08 | 56.81 | 56.8 | 56.74 | 55.95 | 55.91 | 55.82 |

Table 4.6: TIA simulation results - Bandwidth.

| Bandwidth [GHz] | FF | | | TT | | | FS | | | SS | | | SF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC |
| **Vdd 1.1** | 6.95 | 6.88 | 6.58 | 5.46 | 5.73 | 5.81 | 6.12 | 6.22 | 6.15 | 4.04 | 4.54 | 4.79 | 4.69 | 5.16 | 5.36 |
| **Vdd 1.2** | 7.54 | 7.39 | 6.99 | 6.1 | 6.3 | 6.33 | 6.72 | 6.74 | 6.63 | 4.74 | 5.17 | 5.37 | 5.44 | 5.79 | 5.92 |
| **Vdd 1.32** | 8.17 | 7.93 | 7.45 | 6.76 | 6.88 | 6.87 | 7.29 | 7.24 | 7.1 | 5.42 | 5.77 | 5.92 | 6.13 | 6.43 | 6.53 |

Table 4.7: TIA simulation results - Input reffered noise.

| Input reffered noise [$\mu$A] | FF | | | TT | | | FS | | | SS | | | SF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC |
| **Vdd 1.1** | 0.242 | 0.279 | 0.316 | 0.24 | 0.274 | 0.309 | 0.231 | 0.266 | 0.301 | 0.258 | 0.282 | 0.313 | 0.257 | 0.287 | 0.321 |
| **Vdd 1.2** | 0.239 | 0.276 | 0.313 | 0.233 | 0.267 | 0.302 | 0.227 | 0.262 | 0.297 | 0.238 | 0.268 | 0.3 | 0.243 | 0.275 | 0.31 |
| **Vdd 1.32** | 0.237 | 0.274 | 0.31 | 0.229 | 0.263 | 0.297 | 0.225 | 0.259 | 0.293 | 0.228 | 0.258 | 0.291 | 0.235 | 0.268 | 0.302 |

From tables 4.5, 4.6 and 4.7, it can be concluded that the values obtained are very similar to the values obtained from the schematic (tables 4.2 and 4.4) except for the bandwidth values (table 4.3). This occurs because in the implementation of the layout, in addition to the intrinsic transistor's own parasitic capacity (equal to the schematic), there are also the parasitic capacities that appear between the transistors that are ignored in the schematic. So these extra capacities will influence the layout's bandwidth but not the schematic bandwidth.

### 4.3.6 Performance comparison between proposed TIA and others

In this section a comparison is made between this project and the state of the art (section 2.3.5) in table 4.8. It is not possible to make a fair comparison between different TIAs since they are developed in different CMOS technologies. The proposed architecture achieves the highest bandwidth and the input referent noise out of all the TIA architectures in CMOS technology.

Table 4.8: Comparison between the proposed TIA and the other existing TIA architectures.

| **Reference** | **Process** | **Bit Rate (Gb/s)** | **ZT (dBΩ)** | **BW (GHz)** | **Spot noise (pA/$\sqrt{Hz}$)** |
|---|---|---|---|---|---|
| [4] | 0.6 $\mu$m | 2.5 | 55.3 | 2.2 | - |
| [6] | 0.18 $\mu$m | 3.125 | 72 | 2.4 | - |
| [7] | 0.18 $\mu$m | 4 | 61.4 | 2.9 | 26.8 |
| [9] | 0.18 $\mu$m | 5 | 58.7 | 2.6 | 13 |
| [10] | 0.18 $\mu$m | 10 | 61 | 7.2 | 8.2 |
| [11] | 0.18 $\mu$m | 2.4 | 82 | 2.4 | 36 |
| [13] | 0.13 $\mu$m | 4.5 | 73 | 2.9 | - |
| [15] | 0.18 $\mu$m | 10 | 51.7 | 8.5 | 10 |
| [16] | 0.18 $\mu$m | 10 | 87 | 7.6 | - |
| [17] | 90 nm | 2.5 | 54 | 2.68 | 4.9 |
| [18] | 0.18 $\mu$m | 10 | 59 | 8.6 | 25 |
| Proposed Design | 65 nm | 5 | 55.11 | 10.27 | 3.98 |

CHAPTER 5

# Proposed Offset Cancellation Circuit

Frequently, especially in high gain amplifiers, it is necessary to include some DC-offset cancellation block in order to avoid the amplifier's output swing saturation by undesired low frequency components. The offset in differential stages may occur by a device mismatch, low-frequency noise contributions and thermal variations. In this analysis it is also necessary to consider the offset generated at the TIA input.

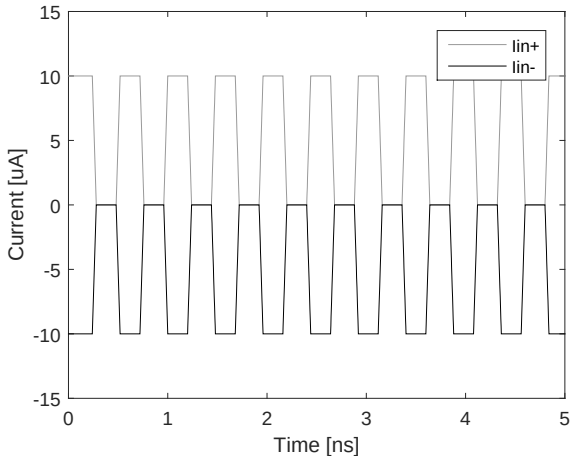



Figure 5.1: Current signal converted from the incoming optical signal by the PD.

As shown in Figure 5.1, when one of the TIA inputs receives, in this case, 10 $\mu$A of current generated by photodiode, the other input will receive -10 $\mu$A. The problem is when the photodiode does not generate current. Because of that, the photodiode provides 0 A to the two TIA inputs. So the TIA inputs will be centered at 5 $\mu$A and -5 $\mu$A and not at zero, which results in an offset. An external feedback loop can be the solution to these problems.

## 5.1 Block diagram and Circuit of proposed Offset Cancellation

In this chapter, the main goal is to decouple an AC. It is therefore necessary to use a low-pass circuit to filter out the undesirable AC component, which means that removing an AC signal's noise from a DC signal makes the DC signal cleaner. This circuit is presented in Figure 5.2.

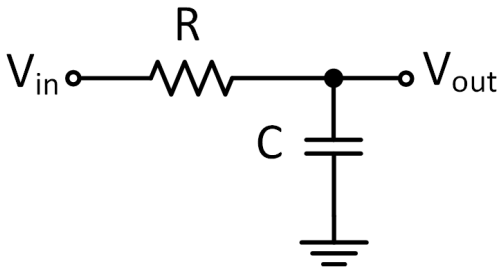



Figure 5.2: AC decoupling circuit.

As mentioned before, this circuit exhibits a low-pass behaviour and it can be demonstrated by its transfer function:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{1}{1 + s\,RC} \tag{5.1}$$

Equation ( 5.1) shows a low-pass function that filters the frequency components above the cut-off frequency $f_c = \frac{1}{2\pi RC}$. In order to have a low cut-off frequency it is necessary to have a large RC product which is the main disadvantage of this offset compensation technique because it will burn a lot of chip area.

In order to cancel the TIA's offset it is necessary to connect this low-pass filter to the Limiting Amplifier (LA)'s output with the TIA's input, as shown in Figure 5.3.

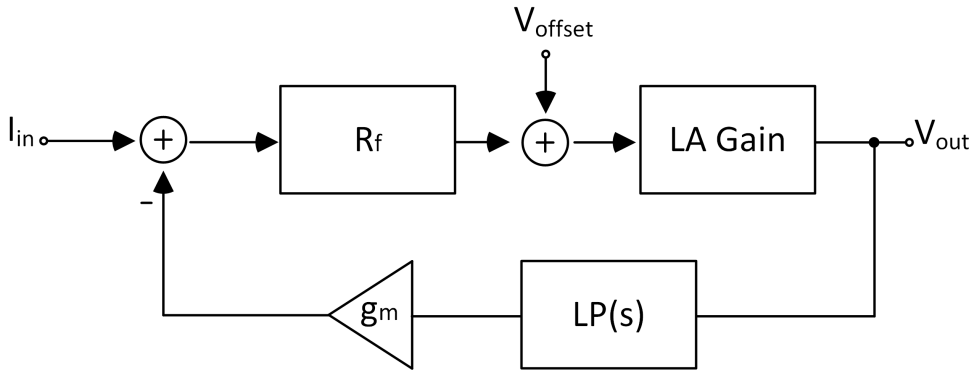



Figure 5.3: Block diagram of proposed circuit.

From Figure 5.3 and using the superposition theorem it is possible to calculate the transfer function.

Considering $I_{in}$, we get:

$$V'_{out} = \frac{I_{in} R_f \, LA_{gain}}{1 + R_f \; g_m \, LA_{gain} \, LP(s)} \tag{5.2}$$

Replacing $LP(f_{in}) \approx 0$, results in:

$$V'_{out} = I_{in} R_f \, LA_{gain} \tag{5.3}$$

Considering now $V_{offset}$, we get:

$$V''_{out} = \frac{V_{offset} \, LA_{gain}}{1 + R_f \; g_m \, LA_{gain} \, LP(s)} \tag{5.4}$$

Replacing $LP(f_0) \approx 1$, $V''_{out}$ can be determined by:

$$V''_{out} = \frac{V_{offset}}{R_f \, g_m} \tag{5.5}$$

Combining ( 5.3) and ( 5.5) results in:

$$\begin{aligned} V_{out} &= V'_{out} + V''_{out} \Leftrightarrow \\ V_{out} &= I_{in} R_f \, LA_{gain} + \frac{V_{offset}}{R_f \, g_m} \end{aligned} \tag{5.6}$$

The equation 5.6 indicates that in order to reduce the offset, the resistance $R_f$ or the $g_m$ values must be maximized. However, as $R_f$ or $g_m$ increase, the offset will reduce, from which problems can arise, for example, those relating to the bandwidth, as previously explained in chapter 4. To reduce this issue it is necessary to take into account a trade-off between the bandwidth and the offset.

A parametrization was therefore performed to choose the most acceptable values for the reduction of the offset cancellation and minimize the bandwidth as far as possible. Figure 5.4 and tables 5.1 and 5.2 show the proposed circuit and the transistor dimensions, respectively.

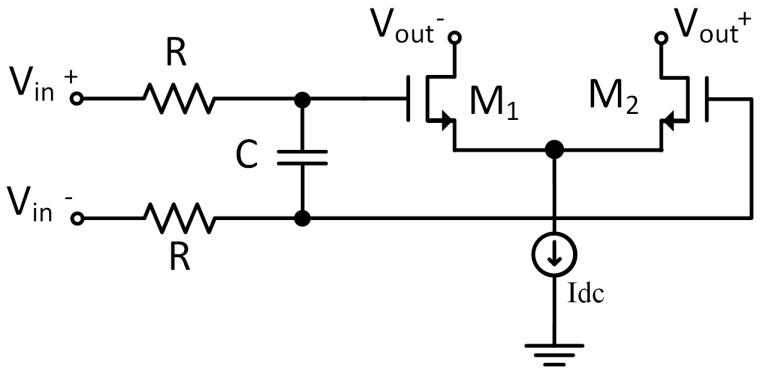



Figure 5.4: Circuit implementation of the proposed circuit. NMOS with undefined bulk have their bulk connected to the ground.

Table 5.1: Transistor dimensions used in the offset cancellation circuit.

| Transistor | W ($\mu$m) | L (nm) | Number of Fingers | Multiplier |
|---|---|---|---|---|
| M1/M2 | 1 | 60 | 5 | 1 |

Table 5.2: Resistances, capacitance and current values used in the offset cancellation circuit.

| Component | Value |
|---|---|
| R | 1.3 MΩ |
| C | 37.5 pF |
| $I_{dc}$ | 315 $\mu$A |

With the offset cancellation block completed it is possible to show the differences between a simulation made with and without the offset cancellation, as shown in Figures 5.5 a), b), c) and d).

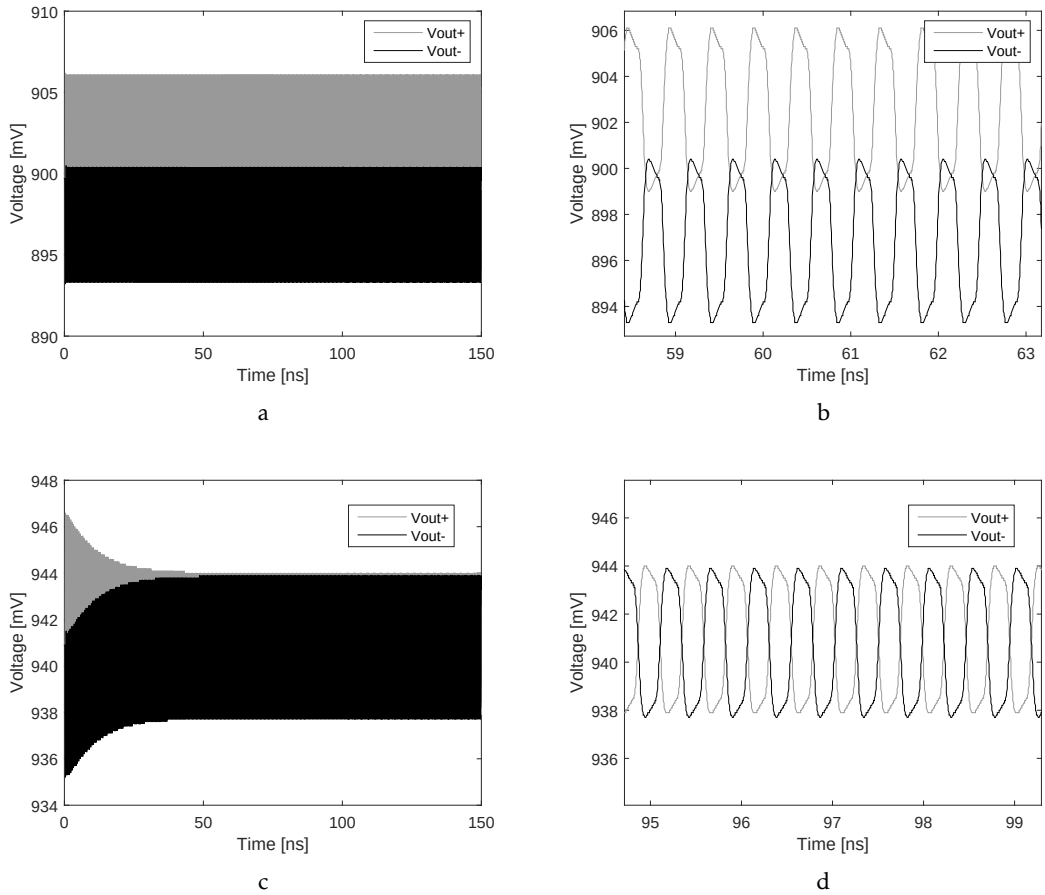



Figure 5.5: Simulations with and without offset cancellation block. b) is a zoom of a) and d) is a zoom of c).

As represented in Figures 5.5 c) and d), the offset originated by the input source current is cancelled and therefore the result of differential output is centred to zero.

## 5.2 Simulation Results

Once the transistor dimensions used in the offset cancellation circuit are known, the next step is to measure the offset in the corners.

The TIA offset values are presented in Tables 5.3 and 5.4.

Table 5.3: Simulation results without OC.

| TIA's offset [mV] | FF | | | TT | | | FS | | | SS | | | SF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC |
| **Vdd 1.1** | 5.17 | 5.07 | 4.97 | 5.58 | 5.59 | 5.54 | 5.83 | 5.75 | 5.66 | 5.71 | 5.91 | 5.97 | 5.23 | 5.36 | 5.37 |
| **Vdd 1.2** | 5.24 | 5.12 | 5.00 | 5.75 | 5.69 | 5.64 | 5.92 | 5.81 | 5.71 | 6.05 | 6.13 | 6.15 | 5.48 | 5.53 | 5.51 |
| **Vdd 1.32** | 5.27 | 5.14 | 5.04 | 5.85 | 5.77 | 5.69 | 5.96 | 5.85 | 5.75 | 6.27 | 6.20 | 6.27 | 5.68 | 5.66 | 5.62 |

Table 5.4: Simulation results with OC.

| TIA's offset [mV] | FF | | | TT | | | FS | | | SS | | | SF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC |
| **Vdd 1.1** | 0.09 | 0.11 | 0.13 | 0.18 | 0.16 | 0.15 | 0.16 | 0.15 | 0.15 | 0.31 | 0.26 | 0.22 | 0.22 | 0.18 | 0.16 |
| **Vdd 1.2** | 0.09 | 0.09 | 0.11 | 0.15 | 0.13 | 0.12 | 0.13 | 0.12 | 0.13 | 0.29 | 0.23 | 0.20 | 0.18 | 0.15 | 0.13 |
| **Vdd 1.32** | 0.09 | 0.08 | 0.10 | 0.09 | 0.09 | 0.10 | 0.09 | 0.09 | 0.11 | 0.24 | 0.19 | 0.17 | 0.11 | 0.10 | 0.09 |

Table 5.3 clearly shows the offset at the TIA output. This offset, as previously mentioned in section 5, is due to the existence of one only photodiode. So, with the blocking of the offset cancellation, it is possible to conclude that this offset, caused by the photodiode, is almost cancelled out, as shown in Table 5.4.

### 5.2.1 Layout

After validating all the corners, in order to conclude study of this block (Offset cancellation), it is necessary to implement the layout.

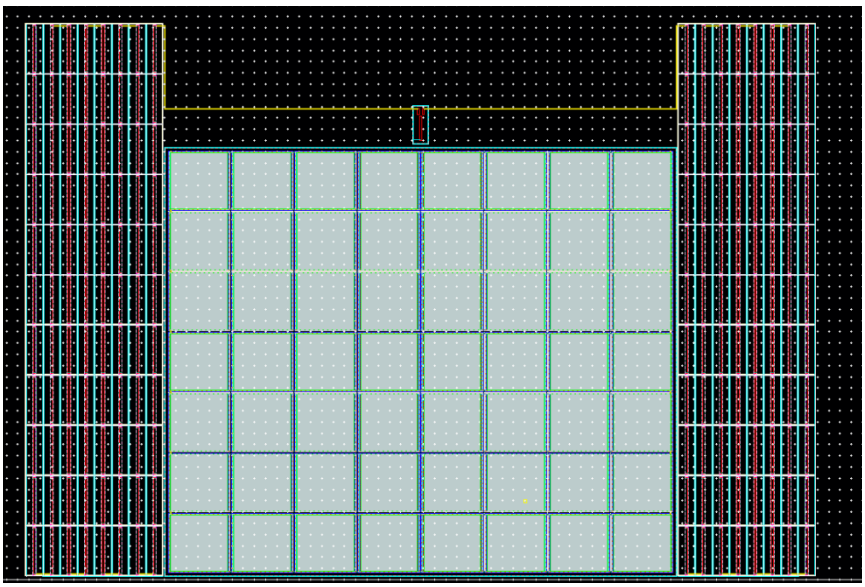


Figure 5.6: Layout implementation of the offset cancellation.

Figure 5.6 shows the layout of the offset cancellation. As presented in the figure, the circuit was carefully made as symmetrical as possible in order to get an identical answer to the schematic. In this implementation, only the first 3 metals were used ($M_1$, $M_2$ and $M_3$).

Like in sections 3.2.2.5 and 4.3.5, the main goal is to implement the Offset cancellation's layout in order to occupy the minimum area possible. Considering that the area occupied by this block is 350.5 by 245.5 $\mu m^2$, and that the chip provided by CERN is 1750 by 40 $\mu m^2$, it is possible to conclude that the percentage of this block's occupation area is the following:

$$\begin{aligned} Percentage\ occupied\ in\ chip &= \frac{350.5 \times 245.5}{1750 \times 400} \times 100\ (\%) \\ Percentage\ occupied\ in\ chip &\approx 12.3\ (\%) \end{aligned} \tag{5.7}$$

Once the layout is completed, in order to compare the schematic results with the layout results, it is necessary to simulate the layout with extraction, including the parasitic capacities. The next tables show the layout simulation in all the processes, just as in section 5.2, to calculate the offset of the TIA.

Table 5.5: Simulation results with OC.

| TIA's offset [mV] | FF | | | TT | | | FS | | | SS | | | SF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC | -40 ºC | 27 ºC | 100 ºC |
| **Vdd 1.1** | 0.37 | 0.36 | 0.36 | 0.74 | 0.35 | 0.13 | 0.44 | 0.40 | 0.38 | 0.46 | 0.41 | 0.35 | 0.47 | 0.43 | 0.30 |
| **Vdd 1.2** | 0.35 | 0.34 | 0.32 | 0.10 | 0.28 | 0.36 | 0.41 | 0.30 | 0.27 | 0.29 | 0.26 | 0.24 | 0.42 | 0.37 | 0.29 |
| **Vdd 1.32** | 0.33 | 0.31 | 0.30 | 0.09 | 0.25 | 0.30 | 0.38 | 0.29 | 0.25 | 0.27 | 0.24 | 0.20 | 0.39 | 0.30 | 0.25 |

Table 5.5 indicates that the results obtained from the layout are close to the results obtained from the schematic (Table 5.4) with a minimal difference. This slight increase in the offset may occur due to a device mismatch.

CHAPTER 6

# Conclusions and Future Work

## 6.1 Conclusions

The main goal of the work presented in this thesis was to develop a Power-on Reset & Brown-Out Reset, a Transimpedance amplifier and an Offset Cancellation in 65-nm technology. For this, it was necessary to conduct intense research into circuits already implemented and of interest to this work. Chapter 2 therefore provides an overview of the existing transimpedance amplifiers and POR-BOR in CMOS technology. Their design pros and cons were also discussed in detail.

As concerns the transimpedance amplifier, the main goal of this block is to extend the bandwidth of the TIA circuit so that it can be operated at a data rate of 5 Gb/s. However, trade-offs between the static gain, bandwidth, and the input referred noise are required to optimize the TIA in order to achieve all the proposed requirements. Bandwidth techniques have therefore been studied to improve the frequency response of the TIA, such as:

- Capacitive Degeneration;
- Shunt Peaking;
- Serie Inductive Peaking;
- Miller Effect.

Lastly, the proposed TIA is based on a differential architecture with a cascode structure and peaking inductors that enhance the bandwidth. The total system has been analyzed for transimpedance gain response, bandwidth and input reffered noise performance.

However, an issue is presented in Figure 6.1. PMOS and NMOS transistors, on the left side of the Figure 6.1, are operating as bias current source and need to give to PD a minimum voltage of 2 V. Since the power supply ( Switched Capacitor (SC) Direct current to direct current (DC-DC) 2/1 Converter) is approximately 2.4 V and must provide 2 V to the photodiode, there is only 0.4 V left over for the two other transistors. So it is very difficult to put the two transistors in saturation ($V_{DS} > V_{TH}$) in all processes (corners). It is not therefore possible to implement the total system (Biasing circuit + TIA + LA).

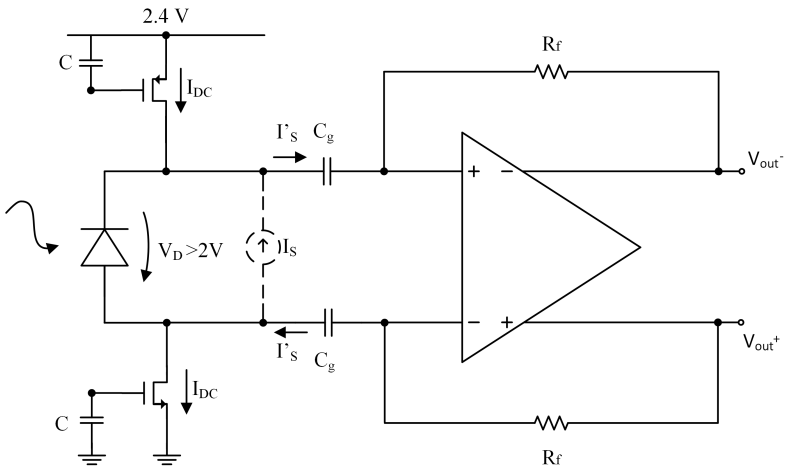



Figure 6.1: Biasing circuit.

As regards the Power-on Reset & Brown-Out Reset, to perform its task the POR-BOR needs auxiliary circuits, such as a current source, comparator, Schmitt trigger and a 3 bits decoder.

The innovation of this block is the use of a 3 bits decoder to change the threshold voltage at the reset activation point. The user should thus be able to choose up to 8 different reference voltages (between 0.7 V to 1.05 V).

The last block described in this thesis is the Offset Cancellation. This block must be able to cancel the offset originated by the device's mismatch, the low-frequency noise contributions and the thermal variations. In this work, Offset Cancellation was designed with the purpose of cancelling the offset created at the TIA input by using only one photodiode.

## 6.2 Future Work

Following on from the work done in this thesis, future improvements can be made. As previously explained in section 6.1, a differential TIA could not be implemented in this system. However, there are some solutions to this issue:

- Decreasing the voltage drop on the photodiode to put the two transistors in saturation ($V_{DS} > V_{TH}$) in all processes (corners);

- Using two photodiodes instead of one. Therefore, one of the TIA's inputs needs to be connected to a PMOS and the other to an NMOS;
- Using a pin with enough voltage to supply the photodiode and the biasing circuit, instead of using a DC-DC converter to generate approximately 2.4 V.
- Implementing a single TIA instead of a differential one. Only one transistor is therefore used as a biasing circuit (NMOS) instead of two (PMOS and NMOS as shown in Figure 6.1).

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Appendix A

# POR-BOR Simulation Results - Corners

Table A.1: Simulation Results - Corners.

| -20 ºC | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **b2** | **b1** | **b0** | **Ideal Vout (V)** | **FF (V)** | **TT (V)** | **FS (V)** | **SS (V)** | **SF (V)** |
| 0 | 0 | 0 | 0.70 | 0.707 | 0.720 | 0.705 | 0.721 | 0.727 |
| 0 | 0 | 1 | 0.75 | 0.755 | 0.770 | 0.755 | 0.784 | 0.784 |
| 0 | 1 | 0 | 0.80 | 0.803 | 0.820 | 0.803 | 0.838 | 0.836 |
| 0 | 1 | 1 | 0.85 | 0.852 | 0.870 | 0.852 | 0.890 | 0.888 |
| 1 | 0 | 0 | 0.90 | 0.900 | 0.920 | 0.901 | 0.942 | 0.939 |
| 1 | 0 | 1 | 0.95 | 0.949 | 0.970 | 0.950 | 0.994 | 0.990 |
| 1 | 1 | 0 | 1.00 | 0.997 | 1.020 | 0.999 | 1.045 | 1.041 |
| 1 | 1 | 1 | 1.05 | 1.046 | 1.070 | 1.048 | 1.096 | 1.091 |
| **100 ºC** | | | | | | | | |
| **b2** | **b1** | **b0** | **Ideal Vout (V)** | **FF (V)** | **TT (V)** | **FS (V)** | **SS (V)** | **SF (V)** |
| 0 | 0 | 0 | 0.70 | 0.732 | 0.745 | 0.732 | 0.762 | 0.758 |
| 0 | 0 | 1 | 0.75 | 0.782 | 0.797 | 0.784 | 0.815 | 0.810 |
| 0 | 1 | 0 | 0.80 | 0.833 | 0.849 | 0.835 | 0.869 | 0.863 |
| 0 | 1 | 1 | 0.85 | 0.883 | 0.901 | 0.886 | 0.923 | 0.916 |
| 1 | 0 | 0 | 0.90 | 0.934 | 0.954 | 0.938 | 0.977 | 0.968 |
| 1 | 0 | 1 | 0.95 | 0.984 | 1.006 | 0.990 | 1.032 | 1.021 |
| 1 | 1 | 0 | 1.00 | 1.034 | 1.058 | 1.041 | 1.086 | 1.074 |
| 1 | 1 | 1 | 1.05 | 1.085 | 1.110 | 1.093 | 1.141 | 1.126 |

| -20 ºC - FF | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **b2** | **b1** | **b0** | **BG (V)** | **Vdd Shift (V)** | **Relative Error** | **Schmitt Trigger's PC (A)** | **Comparatos's PC (A)** | **TPC (A)** | **Reset Time (s)** |
| 0 | 0 | 0 | 0.274 | 0.273 | 0.36% | 1.54E-09 | 9.73E-06 | 2.41E-05 | 1.36E-05 |
| 0 | 0 | 1 | 0.273 | 0.272 | 0.37% | 1.56E-09 | 9.94E-06 | 2.44E-05 | 1.36E-05 |
| 0 | 1 | 0 | 0.273 | 0.271 | 0.73% | 1.57E-09 | 1.03E-05 | 2.48E-05 | 1.36E-05 |
| 0 | 1 | 1 | 0.272 | 0.271 | 0.37% | 1.57E-09 | 1.09E-05 | 2.54E-05 | 1.36E-05 |
| 1 | 0 | 0 | 0.272 | 0.270 | 0.74% | 1.62E-09 | 1.17E-05 | 2.62E-05 | 1.36E-05 |
| 1 | 0 | 1 | 0.272 | 0.270 | 0.74% | 1.71E-09 | 1.27E-05 | 2.71E-05 | 1.36E-05 |
| 1 | 1 | 0 | 0.272 | 0.269 | 1.10% | 1.83E-09 | 1.38E-05 | 2.82E-05 | 1.36E-05 |
| 1 | 1 | 1 | 0.272 | 0.269 | 1.10% | 1.97E-09 | 1.50E-05 | 2.94E-05 | 1.36E-05 |

| 100 ºC - FF | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **b2** | **b1** | **b0** | **BG (V)** | **Vdd Shift (V)** | **Relative Error** | **Schmitt Trigger's PC (A)** | **Comparatos's PC (A)** | **TPC (A)** | **Reset Time (s)** |
| 0 | 0 | 0 | 0.286 | 0.282 | 1.40% | 1.84E-08 | 1.40E-05 | 3.02E-05 | 1.24E-05 |
| 0 | 0 | 1 | 0.286 | 0.282 | 1.40% | 1.85E-08 | 1.46E-05 | 3.07E-05 | 1.24E-05 |
| 0 | 1 | 0 | 0.285 | 0.281 | 1.40% | 1.85E-08 | 1.53E-05 | 3.15E-05 | 1.24E-05 |
| 0 | 1 | 1 | 0.285 | 0.281 | 1.40% | 1.86E-08 | 1.63E-05 | 3.25E-05 | 1.24E-05 |
| 1 | 0 | 0 | 0.285 | 0.280 | 1.75% | 1.87E-08 | 1.74E-05 | 3.36E-05 | 1.24E-05 |
| 1 | 0 | 1 | 0.285 | 0.280 | 1.75% | 1.89E-08 | 1.86E-05 | 3.48E-05 | 1.24E-05 |
| 1 | 1 | 0 | 0.285 | 0.279 | 2.11% | 1.90E-08 | 1.99E-05 | 3.61E-05 | 1.24E-05 |
| 1 | 1 | 1 | 0.285 | 0.279 | 2.11% | 1.92E-08 | 2.13E-05 | 3.75E-05 | 1.24E-05 |

| -20 ºC - TT | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **b2** | **b1** | **b0** | **BG (V)** | **Vdd Shift (V)** | **Relative Error** | **Schmitt Trigger's PC (A)** | **Comparatos's PC (A)** | **TPC (A)** | **Reset Time (s)** |
| 0 | 0 | 0 | 0.279 | 0.278 | 0.36% | 1.88E-09 | 6.58E-06 | 1.82E-05 | 1.83E-05 |
| 0 | 0 | 1 | 0.279 | 0.277 | 0.72% | 1.87E-09 | 6.74E-06 | 1.84E-05 | 1.83E-05 |
| 0 | 1 | 0 | 0.279 | 0.277 | 0.72% | 1.83E-09 | 7.02E-06 | 1.87E-05 | 1.83E-05 |
| 0 | 1 | 1 | 0.278 | 0.276 | 0.72% | 1.84E-09 | 7.44E-06 | 1.91E-05 | 1.82E-05 |
| 1 | 0 | 0 | 0.278 | 0.276 | 0.72% | 1.83E-09 | 8.03E-06 | 1.97E-05 | 1.83E-05 |
| 1 | 0 | 1 | 0.278 | 0.276 | 0.72% | 1.88E-09 | 8.75E-06 | 2.04E-05 | 1.82E-05 |
| 1 | 1 | 0 | 0.278 | 0.276 | 0.72% | 1.96E-09 | 9.57E-06 | 2.12E-05 | 1.83E-05 |
| 1 | 1 | 1 | 0.278 | 0.275 | 1.08% | 2.08E-09 | 1.04E-05 | 2.21E-05 | 1.83E-05 |
| **100 ºC - TT** | | | | | | | | | |
| **b2** | **b1** | **b0** | **BG (V)** | **Vdd Shift (V)** | **Relative Error** | **Schmitt Trigger's PC (A)** | **Comparatos's PC (A)** | **TPC (A)** | **Reset Time (s)** |
| 0 | 0 | 0 | 0.291 | 0.288 | 1.03% | 3.05E-09 | 1.02E-05 | 2.28E-05 | 1.52E-05 |
| 0 | 0 | 1 | 0.290 | 0.287 | 1.03% | 3.11E-09 | 1.05E-05 | 2.32E-05 | 1.52E-05 |
| 0 | 1 | 0 | 0.290 | 0.287 | 1.03% | 3.17E-09 | 1.09E-05 | 2.36E-05 | 1.52E-05 |
| 0 | 1 | 1 | 0.290 | 0.286 | 1.38% | 3.26E-09 | 1.15E-05 | 2.41E-05 | 1.52E-05 |
| 1 | 0 | 0 | 0.289 | 0.286 | 1.04% | 3.36E-09 | 1.22E-05 | 2.48E-05 | 1.52E-05 |
| 1 | 0 | 1 | 0.289 | 0.286 | 1.04% | 3.49E-09 | 1.29E-05 | 2.56E-05 | 1.52E-05 |
| 1 | 1 | 0 | 0.289 | 0.286 | 1.04% | 3.63E-09 | 1.38E-05 | 2.65E-05 | 1.52E-05 |
| 1 | 1 | 1 | 0.289 | 0.286 | 1.04% | 3.78E-09 | 1.47E-05 | 2.74E-05 | 1.52E-05 |

| -20 ºC - FS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **b2** | **b1** | **b0** | **BG (V)** | **Vdd Shift (V)** | **Relative Error** | **Schmitt Trigger's PC (A)** | **Comparatos's PC (A)** | **TPC (A)** | **Reset Time (s)** |
| 0 | 0 | 0 | 0.273 | 0.272 | 0.37% | 4.00E-09 | 6.41E-06 | 1.81E-05 | 2.33E-05 |
| 0 | 0 | 1 | 0.273 | 0.272 | 0.37% | 3.98E-09 | 6.52E-06 | 1.82E-05 | 2.33E-05 |
| 0 | 1 | 0 | 0.272 | 0.271 | 0.37% | 3.93E-09 | 6.74E-06 | 1.84E-05 | 2.33E-05 |
| 0 | 1 | 1 | 0.272 | 0.271 | 0.37% | 3.80E-09 | 7.08E-06 | 1.87E-05 | 2.33E-05 |
| 1 | 0 | 0 | 0.272 | 0.270 | 0.74% | 3.74E-09 | 7.57E-06 | 1.92E-05 | 2.33E-05 |
| 1 | 0 | 1 | 0.271 | 0.270 | 0.37% | 3.68E-09 | 8.19E-06 | 1.99E-05 | 2.33E-05 |
| 1 | 1 | 0 | 0.271 | 0.270 | 0.37% | 3.67E-09 | 8.93E-06 | 2.06E-05 | 2.33E-05 |
| 1 | 1 | 1 | 0.271 | 0.269 | 0.74% | 3.70E-09 | 9.73E-06 | 2.14E-05 | 2.33E-05 |
| **100 ºC - FS** | | | | | | | | | |
| **b2** | **b1** | **b0** | **BG (V)** | **Vdd Shift (V)** | **Relative Error** | **Schmitt Trigger's PC (A)** | **Comparatos's PC (A)** | **TPC (A)** | **Reset Time (s)** |
| 0 | 0 | 0 | 0.284 | 0.282 | 0.70% | 6.08E-09 | 9.86E-06 | 2.25E-05 | 1.79E-05 |
| 0 | 0 | 1 | 0.284 | 0.282 | 0.70% | 6.11E-09 | 1.01E-05 | 2.28E-05 | 1.79E-05 |
| 0 | 1 | 0 | 0.284 | 0.282 | 0.70% | 6.16E-09 | 1.04E-05 | 2.31E-05 | 1.79E-05 |
| 0 | 1 | 1 | 0.284 | 0.282 | 0.70% | 6.23E-09 | 1.08E-05 | 2.35E-05 | 1.79E-05 |
| 1 | 0 | 0 | 0.283 | 0.281 | 0.71% | 6.32E-09 | 1.13E-05 | 2.40E-05 | 1.79E-05 |
| 1 | 0 | 1 | 0.283 | 0.281 | 0.71% | 6.43E-09 | 1.20E-05 | 2.46E-05 | 1.79E-05 |
| 1 | 1 | 0 | 0.283 | 0.281 | 0.71% | 6.56E-09 | 1.27E-05 | 2.53E-05 | 1.79E-05 |
| 1 | 1 | 1 | 0.283 | 0.281 | 0.71% | 6.72E-09 | 1.35E-05 | 2.61E-05 | 1.79E-05 |
| **-20 ºC - SS** | | | | | | | | | |
| **b2** | **b1** | **b0** | **BG (V)** | **Vdd Shift (V)** | **Relative Error** | **Schmitt Trigger's PC (A)** | **Comparatos's PC (A)** | **TPC (A)** | **Reset Time (s)** |
| 0 | 0 | 0 | 0.280 | 0.278 | 0.71% | 2.42E-09 | 4.31E-06 | 1.43E-05 | 2.58E-05 |
| 0 | 0 | 1 | 0.284 | 0.282 | 0.70% | 2.41E-09 | 4.42E-06 | 1.44E-05 | 2.58E-05 |
| 0 | 1 | 0 | 0.285 | 0.283 | 0.70% | 2.37E-09 | 4.62E-06 | 1.46E-05 | 2.58E-05 |
| 0 | 1 | 1 | 0.285 | 0.283 | 0.70% | 2.38E-09 | 4.92E-06 | 1.49E-05 | 2.58E-05 |
| 1 | 0 | 0 | 0.284 | 0.283 | 0.35% | 2.32E-09 | 5.34E-06 | 1.53E-05 | 2.58E-05 |
| 1 | 0 | 1 | 0.284 | 0.282 | 0.70% | 2.33E-09 | 5.86E-06 | 1.59E-05 | 2.58E-05 |
| 1 | 1 | 0 | 0.284 | 0.282 | 0.70% | 2.33E-09 | 6.45E-06 | 1.64E-05 | 2.58E-05 |
| 1 | 1 | 1 | 0.284 | 0.282 | 0.70% | 2.41E-09 | 7.06E-06 | 1.70E-05 | 2.58E-05 |

| 100 ºC - SS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **b2** | **b1** | **b0** | **BG (V)** | **Vdd Shift (V)** | **Relative Error** | **Schmitt Trigger's PC (A)** | **Comparatos's PC (A)** | **TPC (A)** | **Reset Time (s)** |
| 0 | 0 | 0 | 0.296 | 0.294 | 0.68% | 1.84E-09 | 7.38E-06 | 1.80E-05 | 1.90E-05 |
| 0 | 0 | 1 | 0.296 | 0.293 | 1.01% | 1.88E-09 | 7.53E-06 | 1.82E-05 | 1.90E-05 |
| 0 | 1 | 0 | 0.295 | 0.293 | 0.68% | 1.93E-09 | 7.75E-06 | 1.84E-05 | 1.90E-05 |
| 0 | 1 | 1 | 0.295 | 0.293 | 0.68% | 2.00E-09 | 8.04E-06 | 1.87E-05 | 1.90E-05 |
| 1 | 0 | 0 | 0.295 | 0.293 | 0.68% | 2.10E-09 | 8.40E-06 | 1.90E-05 | 1.90E-05 |
| 1 | 0 | 1 | 0.295 | 0.293 | 0.68% | 2.21E-09 | 8.83E-06 | 1.95E-05 | 1.90E-05 |
| 1 | 1 | 0 | 0.295 | 0.293 | 0.68% | 2.34E-09 | 9.31E-06 | 1.99E-05 | 1.90E-05 |
| 1 | 1 | 1 | 0.295 | 0.293 | 0.68% | 2.50E-09 | 1.01E-05 | 2.07E-05 | 1.90E-05 |

| -20 ºC - SF | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **b2** | **b1** | **b0** | **BG (V)** | **Vdd Shift (V)** | **Relative Error** | **Schmitt Trigger's PC (A)** | **Comparatos's PC (A)** | **TPC (A)** | **Reset Time (s)** |
| 0 | 0 | 0 | 0.283 | 0.281 | 0.71% | 8.53E-10 | 6.77E-06 | 1.84E-05 | 1.48E-05 |
| 0 | 0 | 1 | 0.285 | 0.282 | 1.05% | 8.63E-10 | 7.00E-06 | 1.86E-05 | 1.48E-05 |
| 0 | 1 | 0 | 0.285 | 0.282 | 1.05% | 8.77E-10 | 7.39E-06 | 1.90E-05 | 1.48E-05 |
| 0 | 1 | 1 | 0.284 | 0.282 | 0.70% | 9.07E-10 | 7.96E-06 | 1.96E-05 | 1.48E-05 |
| 1 | 0 | 0 | 0.284 | 0.282 | 0.70% | 9.66E-10 | 8.68E-06 | 2.03E-05 | 1.48E-05 |
| 1 | 0 | 1 | 0.284 | 0.281 | 1.06% | 1.02E-09 | 9.54E-06 | 2.12E-05 | 1.48E-05 |
| 1 | 1 | 0 | 0.284 | 0.281 | 1.06% | 1.15E-09 | 1.05E-05 | 2.21E-05 | 1.48E-05 |
| 1 | 1 | 1 | 0.284 | 0.281 | 1.06% | 1.26E-09 | 1.14E-05 | 2.30E-05 | 1.48E-05 |

| 100 ºC - SF | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **b2** | **b1** | **b0** | **BG (V)** | **Vdd Shift (V)** | **Relative Error** | **Schmitt Trigger's PC (A)** | **Comparatos's PC (A)** | **TPC (A)** | **Reset Time (s)** |
| 0 | 0 | 0 | 0.297 | 0.292 | 1.68% | 3.92E-09 | 1.06E-05 | 2.32E-05 | 1.30E-05 |
| 0 | 0 | 1 | 0.296 | 0.292 | 1.35% | 3.97E-09 | 1.10E-05 | 2.37E-05 | 1.30E-05 |
| 0 | 1 | 0 | 0.296 | 0.291 | 1.69% | 4.04E-09 | 1.16E-05 | 2.43E-05 | 1.30E-05 |
| 0 | 1 | 1 | 0.296 | 0.291 | 1.69% | 4.12E-09 | 1.23E-05 | 2.50E-05 | 1.30E-05 |
| 1 | 0 | 0 | 0.296 | 0.291 | 1.69% | 4.22E-09 | 1.32E-05 | 2.58E-05 | 1.30E-05 |
| 1 | 0 | 1 | 0.296 | 0.290 | 2.03% | 4.33E-09 | 1.41E-05 | 2.68E-05 | 1.30E-05 |
| 1 | 1 | 0 | 0.296 | 0.290 | 2.03% | 4.47E-09 | 1.50E-05 | 2.77E-05 | 1.30E-05 |
| 1 | 1 | 1 | 0.295 | 0.290 | 1.69% | 4.62E-09 | 1.67E-05 | 2.94E-05 | 1.30E-05 |

Appendix B

# Layout Tutorial and DRC/LVS/PEX

This tutorial describes how to generate a layout view in the Cadence Virtuoso Layout Editor, how to perform layout verification in Calibre, and how to re-simulate the design with the extracted parasitics in Spectre. It will also be described in this tutorial how to make an inverter.

## B.1 Schematic and Layout

Figure B.1 shows the inverter schematic.

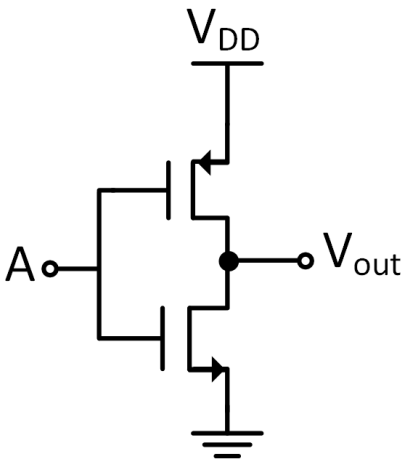


Figure B.1: Inverter schematic. PMOS and NMOS with undefined bulk have their bulk connected to $V_{dd}$ and ground, respectively.

Once the schematic is created, it is necessary to click in the upper left corner in Launch > Layout GXL, as shown in Figure B.2. It should be noted that 4 pins have been created in this circuit: $V_{in}$, $V_{out}$, $V_{dd}$ and $V_{ss}$, as shown in Figure B.2.

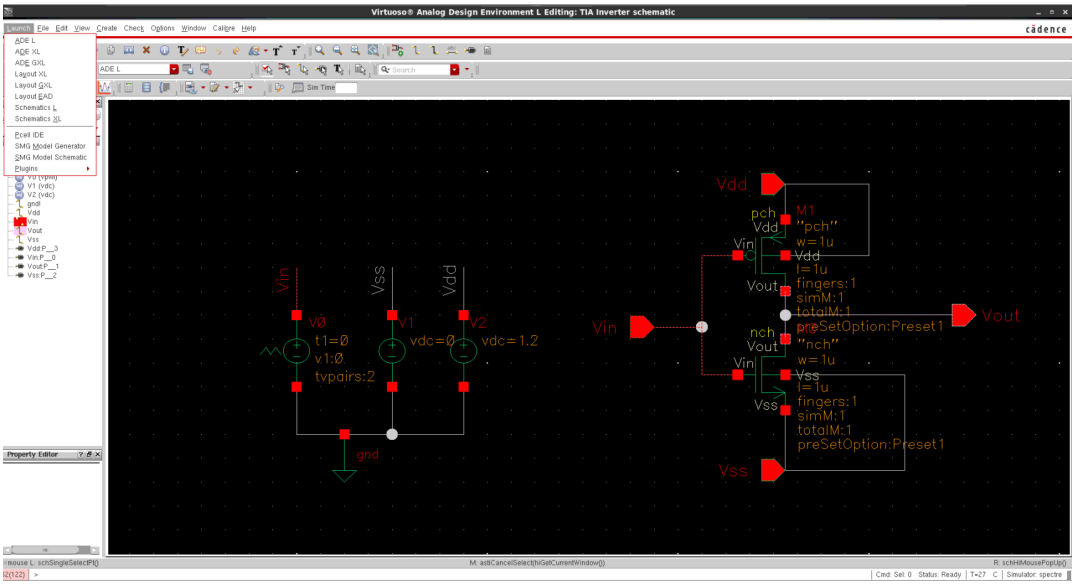


Figure B.2: Running a Layout File.

After clicking on the Layout GXL tool, a window will appear to create a new layout file or open an existing one. The next step is to select the option "Create new". An environment similar to that shown in Figure B.3.

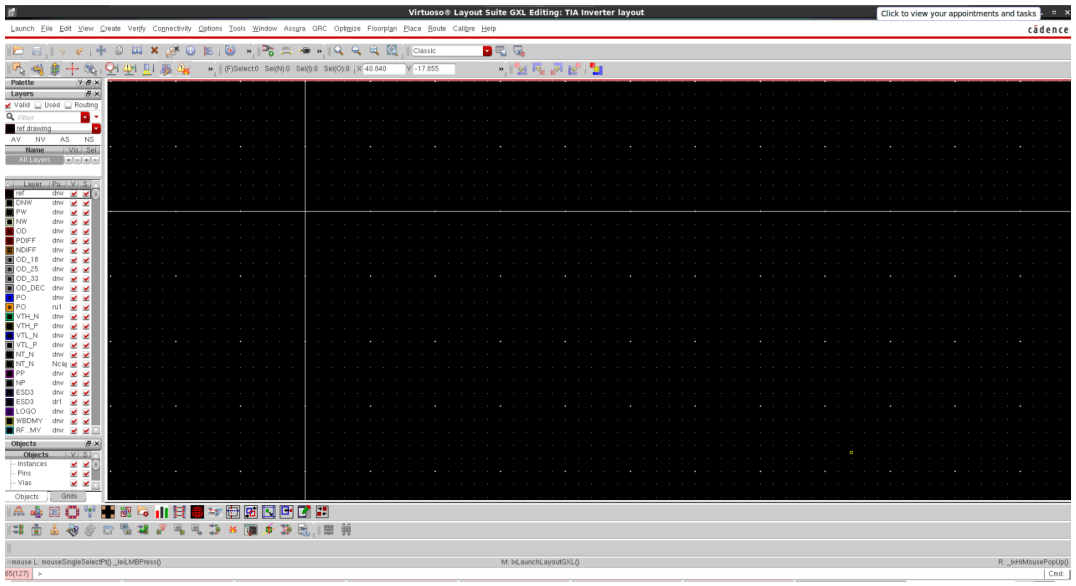


Figure B.3: Layout File - GXL Editing.

Since the 65 nm technology already provides the layout of the transistors, it is only necessary to draw the rest of the circuit which will be done in the environment created in Figure B.3 by choosing:

- Connectivity > Generate > All From Source.

This will import all the schematic components into the layout (pins and transistors), as shown in Figure B.4.

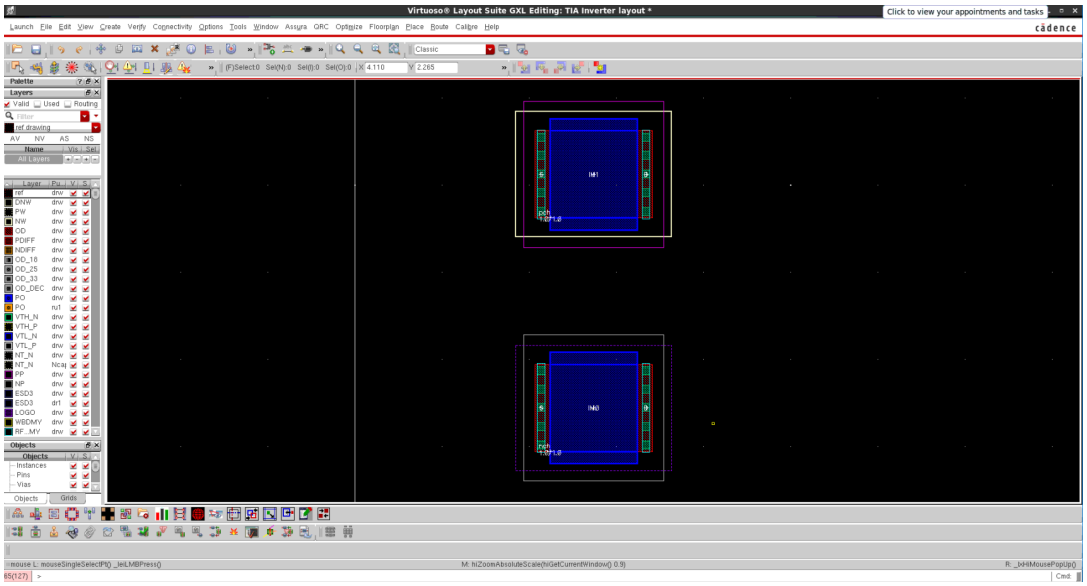

Figure B.4: Transistors of the inverter's layout.

Figure B.4 shows the PMOS (top) and NMOS (bottom) transistors. As observed on the left side of Figure B.4, all the components required to build the circuit can be found in the group "Layers". At this stage it is necessary to know how to make the links between the transistors which requires some knowledge and notions about metals and vias:

- Metals → Component that is used to make the connections of the circuit. There are several types of metals, depending on the technology. In 65 nm technology they exist up to the metal 9. However, vias are required to make the connection between different metals;
- Vias → Component used to connect different types of metal. For example, to connect the metal 1 with metal 2 a Via M1-M2 is necessary.

The next step is to connect the 2 transistors (in this tutorial the area is not a concern. The important thing is to show the basics of the layout). To connect the 2 transistors metal 1 will be used. So on the left side of Figure B.4, it is necessary to write "m1" (metal 1) and choose the "drw" (draw) option, as seen in Figure B.5.

After this, it is necessary to make the connections between the transistors. To do this, after clicking on "M1 drw", click on bind "r" and make the connection, as observed in Figure B.6.

In order to connect the gates it is necessary to connect with polly. It is also necessary to connect the polly to a metal (in this case it will also be metal 1). For this a Via will be needed to connect Metal 1 with Polly, as shown in Figure B.7 (to use Vias the bind "o" option should be used).

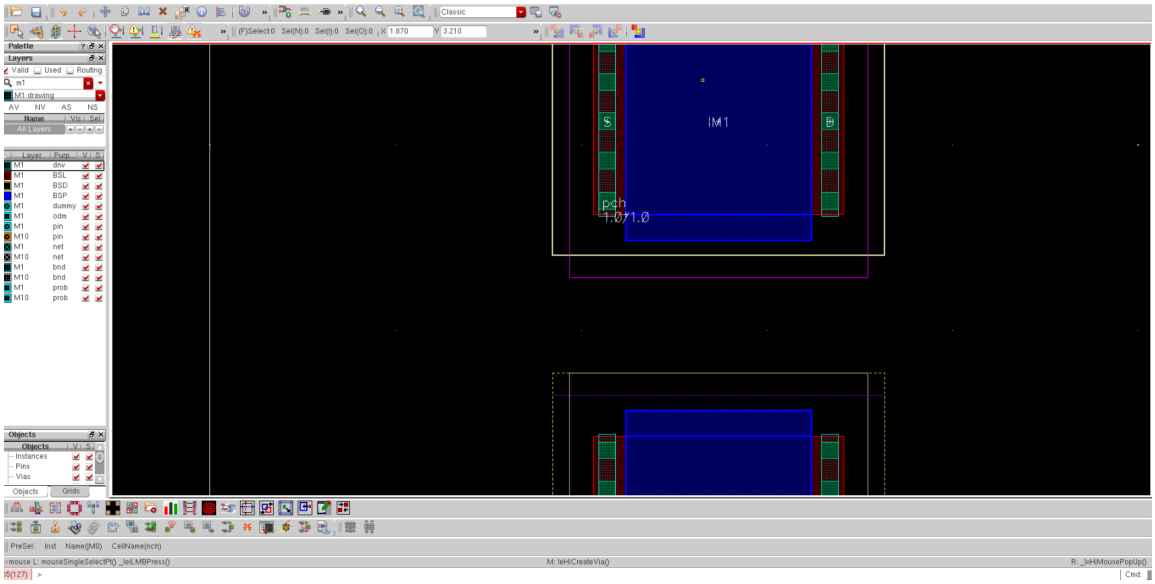


Figure B.5: Choosing metal.

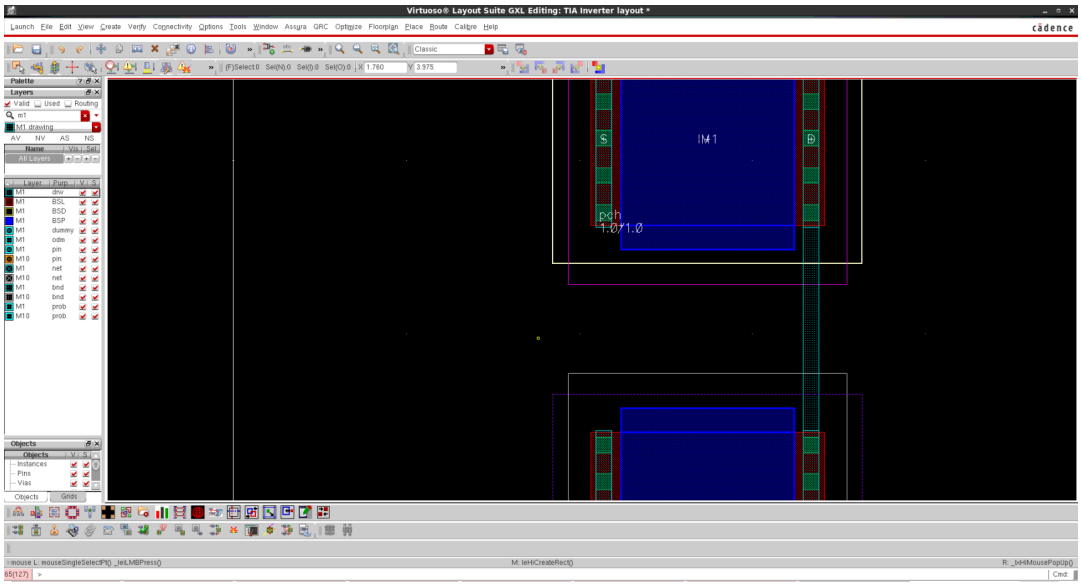


Figure B.6: Drain connection with metal 1.

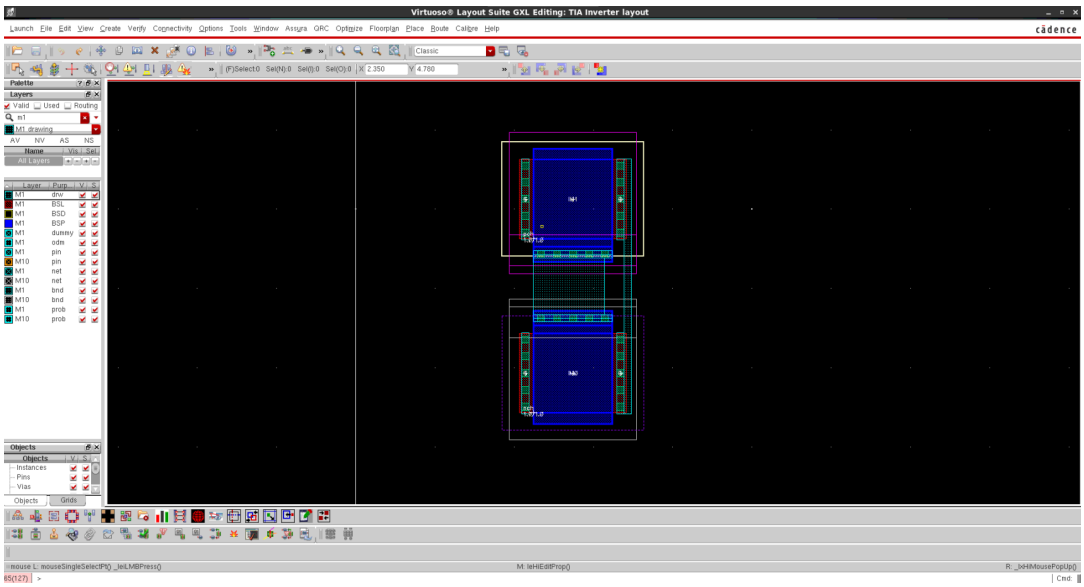


Figure B.7: Gate connection with metal 1 and polly.

The next step is to polarize the bulk of each transistor ($V_{dd}$ to PMOS and $V_{ss}$ to NMOS). So it is necessary to click on "o" again to use a via in order to connect the metal with the well. Since the PMOS transistor has a N-Well, the via used is the M1-NW. However, the NMOS transistor has a P-Well, so the via used, in this case, is M1-PW. Figure B.8 shows the bulks of both transistors connected to metal 1 by vias (M1-NW on top and M1-PW on bottom).

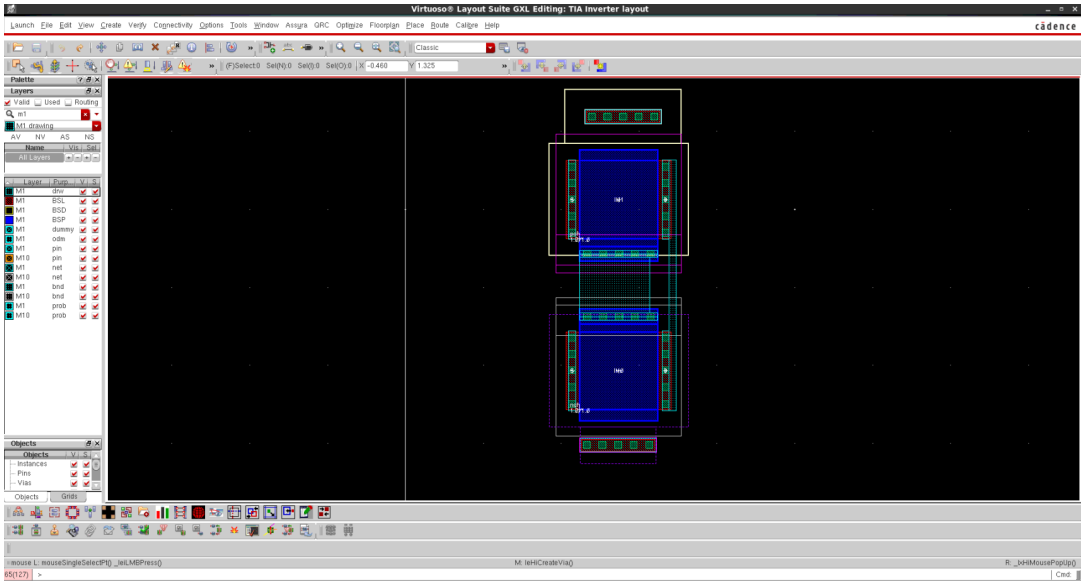


Figure B.8: Bulks connected.

When making connections, the last stage requires to connect the source and the PMOS transistor's bulk to $V_{dd}$ and also the source and the NMOS transistor's bulk to $V_{ss}$, as shown in Figure B.9.

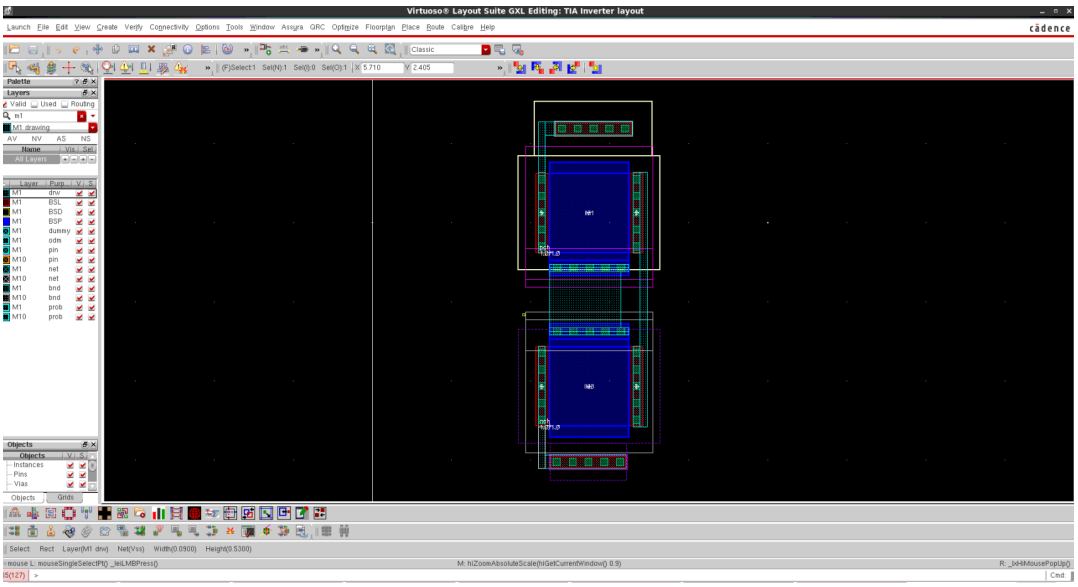


Figure B.9: Bulks and sources connected.

After all the connections have been made, the outputs and inputs must be connected to their respective pins (the names given to layout's pins must be the same as the schematic ones). So with Metal 1 selected, click on:

- Create > Pin

A window similar to that in Figure B.10 will appear.

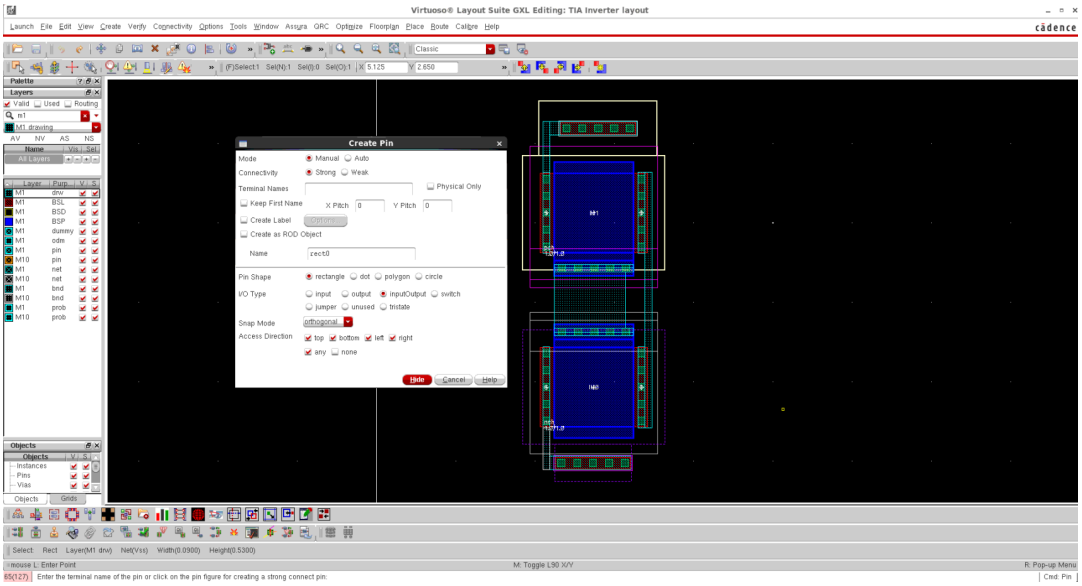


Figure B.10: Create a Pin.

It is then necessary to configure the pin ($V_{dd}$ for example):

- Therminal Names → $V_{dd}$;

- Pin Shape → polygon;
- I/O Type → input;
- Press Hide.

Now it is possible to draw the pin. Then, on the left side, it is necessary to find "M1 Pin" and therefore press "l". A window will appear as shown in Figure B.11.

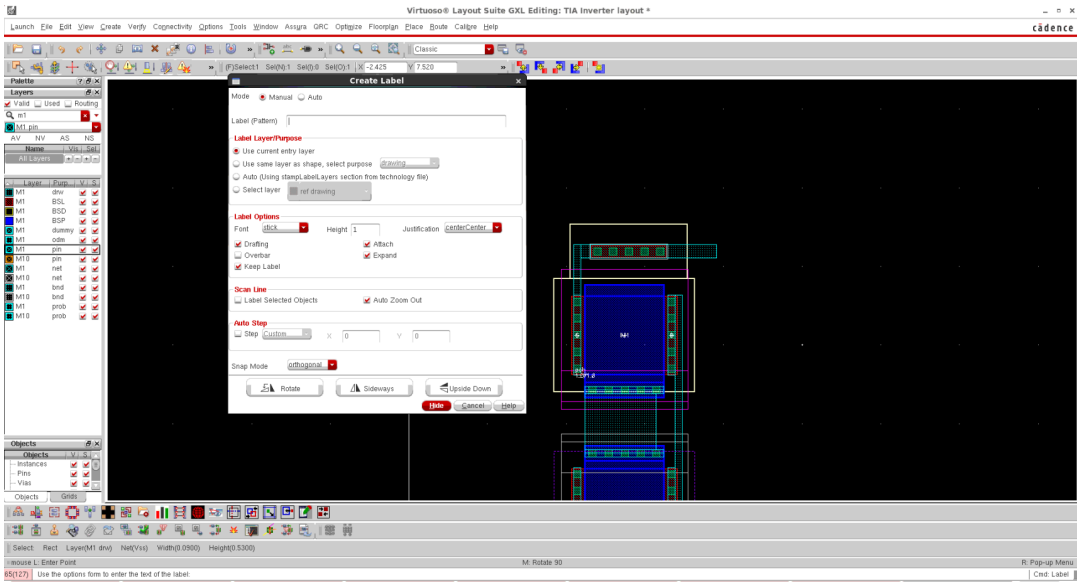


Figure B.11: Create a Pin.

In "Label (Pattern)", for the $V_{dd}$ pin, it is necessary to write $V_{dd}$ and place the label on the drawn metal in Figure B.11 (top right corner). Figure B.12 shows the layout after the $V_{dd}$ label has been placed.

Lastly, it is needed to do exactly the same for the other pins. At the end, the result is similar to Figure B.13.

## B.2 Design Rule Check (DRC)

Once the layout is complete, it is important to check if the layout breaches any of the design rules. Click on the Calibre menu item:

- Calibre > Run nmDRC;
- In the first pop up window click OK;
- When it asks to runset the file, just click to cancel. The file will be configured later.

The DRC Rules File has a ".drc" extension. The technology typically provides the rules file.

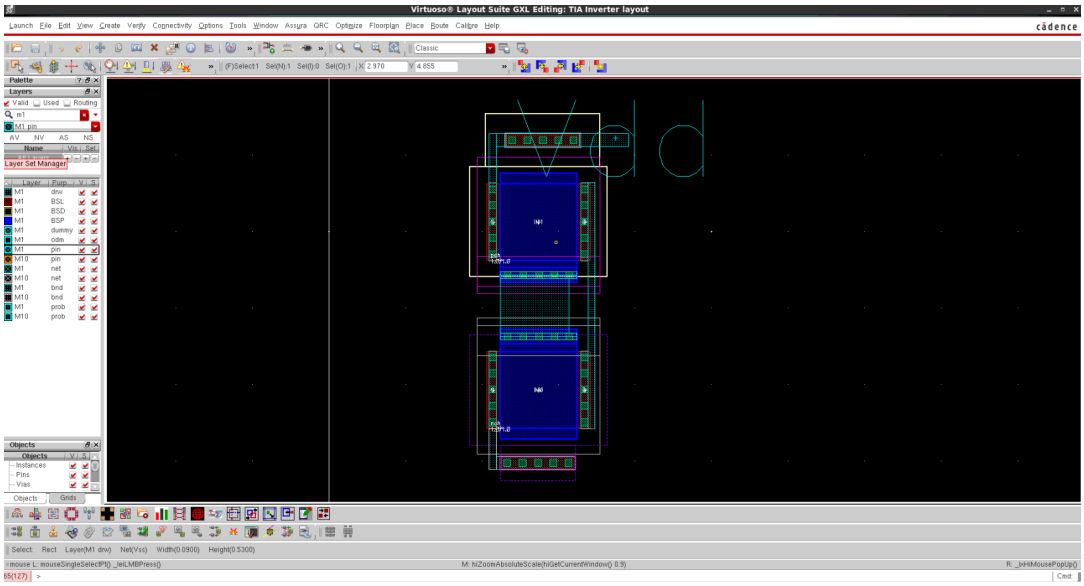


Figure B.12: Create a Label.

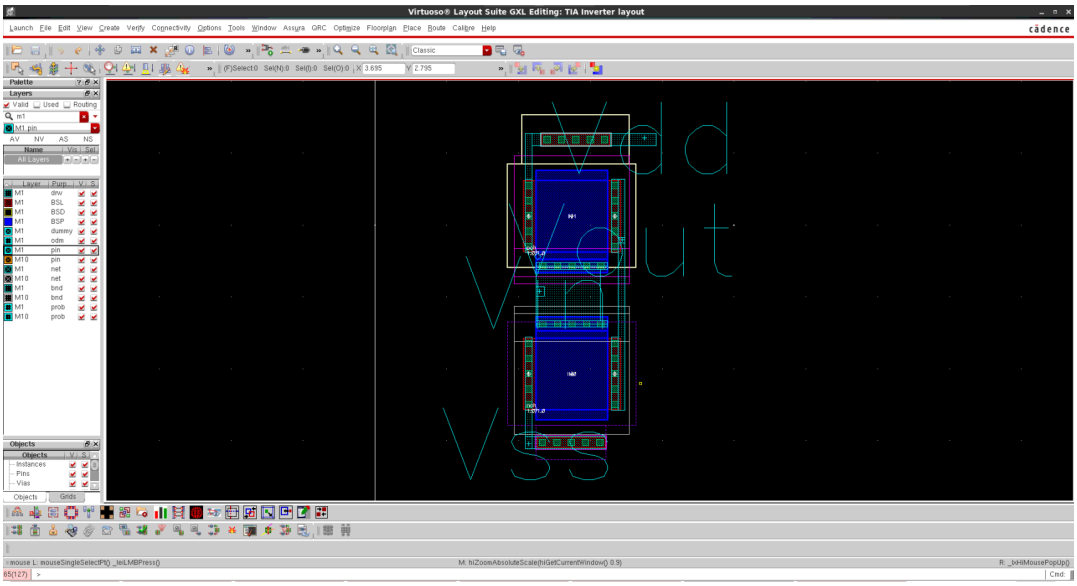


Figure B.13: Final layout circuit.

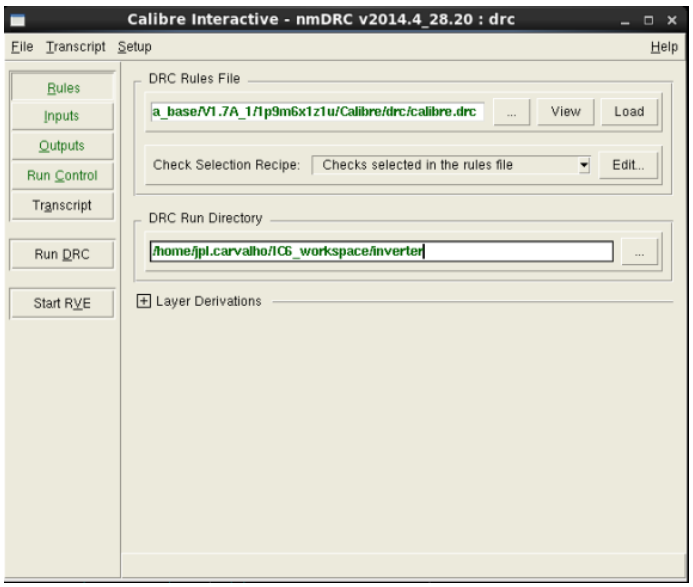


Figure B.14: Calibre DRC Config.

It is possible to set the DRC Run Directory to anything. You are recommend to create a new folder so that all the DRC files are stored there, as seen in Figure B.14.

After configuring the DRC file, press "Run DRC" and it takes a while to check all the Design Rule Check (DRC) rules defined in the technology files. A new window labeled as DRC RVE will pop-up with a list of violations. The list will contain different rules (i.e. RULE_XX) and by clicking on each rule it is possible to see a list of coordinates of where the rule was violated, as shown in Figure B.15. After fixing the errors, rerun DRC to confirm the errors were solved. Once all the violations are corrected, it is time to run Layout vs. Schematic (LVS).

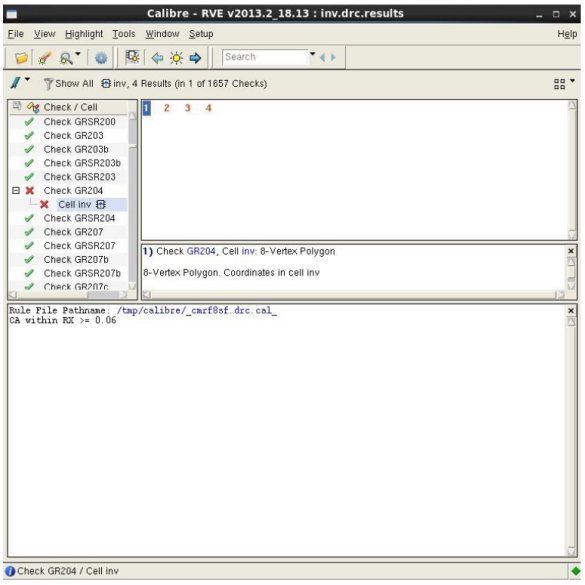


Figure B.15: Example Calibre DRC.

## B.3 Layout vs. Schematic (LVS)

Layout vs. Schematic will compare the layout view with the schematic view.

To start LVS press:

- Run > nmLVS;

Like when opening DRC, a configuration window will open. For the first time when it asks for runset file just click cancel.

LVS Rules File is a ".lvs" extension. Again, you are recommended to create a new folder so that all the LVS files are kept there, as seen in Figure B.16.

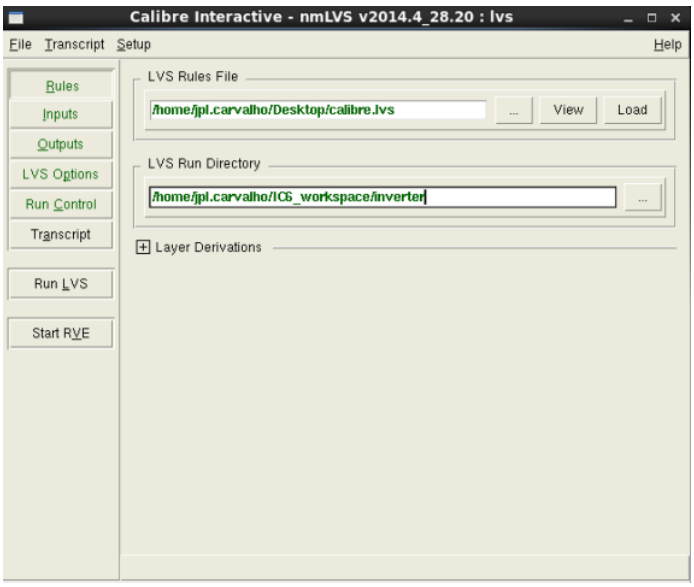


Figure B.16: Calibre LVS Config.

After the LVS file configuration, press "Run LVS". LVS will check if all the devices are connected in the same way and if they have the same width and length parameters. Top-level pins or terminals are checked as well. A successful LVS output is shown in Figure B.16. If any problems are encountered in LVS, it is possible to see a LVS output, depicted in Figure B.18.

## B.4 Practices Extraction (PEX)

Now it is time to extract the parasitic wire capacitances and resistances from the layout.

To perform a Practices Extraction (PEX), select:

- Calibre > Run PEX

In the same way as for DRC and LVS, a configuration window will open. For the first time when it asks for runset file just click cancel. PEX Rules File is a ".rcx" extension.

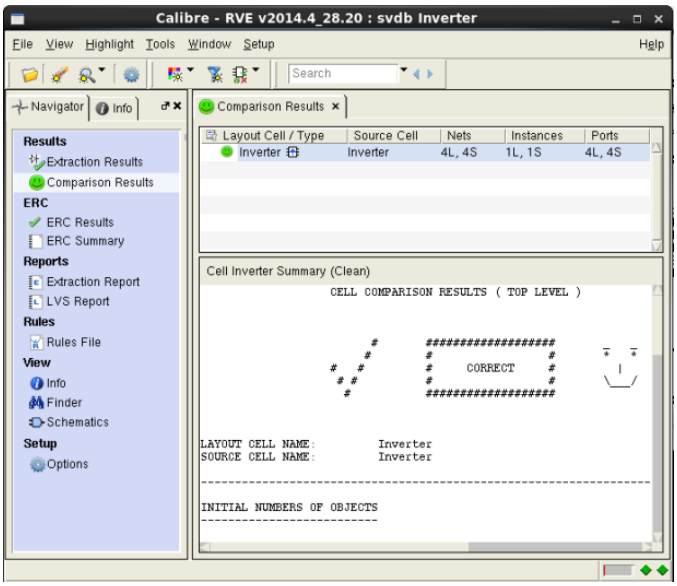


Figure B.17: Example Calibre Correct LVS.

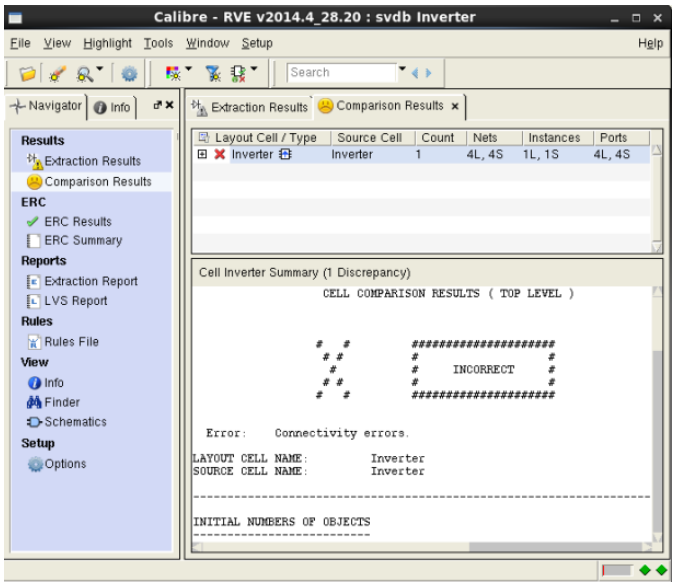


Figure B.18: Example Calibre Incorrect LVS.

Again, it is recommended to create a new folder so that all the LVS files are kept there, as shown in Figure B.19.

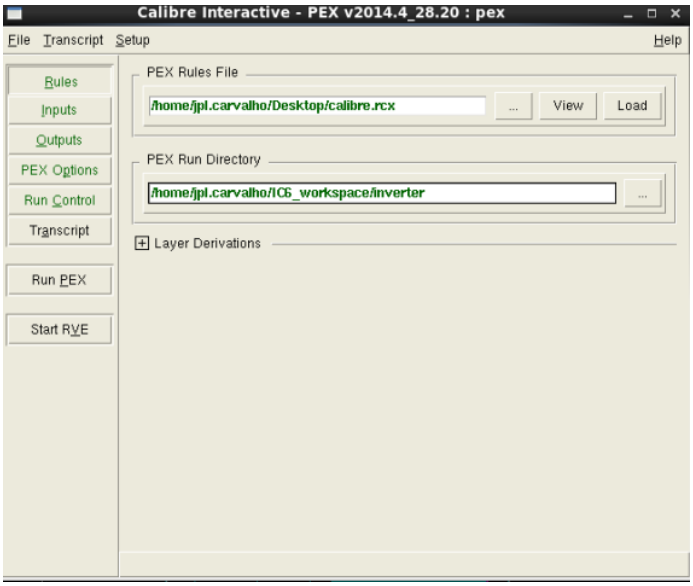


Figure B.19: Calibre PEX Config.

Check the Input tab on the left, and in the Layout tab click "Export from layout viewer" and in Netlist tab click "Export from schematic viewer". In addition, in the Outputs tab on the left, make sure that "Format" is set to CALIBREVIEW and "Extraction Type" is set to $R+C+CC$ in order to extract all the layout's parasitics.

To begin the extraction process, press "Run PEX" and a Calibre view setup window will appear, as shown in Figure B.20.

From Figure B.20:

- Cell Map → change to ".cellmap" extension file;
- Calibre View Type → change to "schematic";
- Create Terminals → change to "Create all terminals";
- Device Placement → change to "Arrayed";
- Open Calibre Cell View → change to "Read-More";
- Press "Ok".

After "Ok" has been pressed, a window will appear, as shown in Figure B.21.

From Figure B.21, the original circuit components and pins will be at the top of the schematic and the parasitic components will be near the bottom.


Figure B.20: Calibre View Setup options.

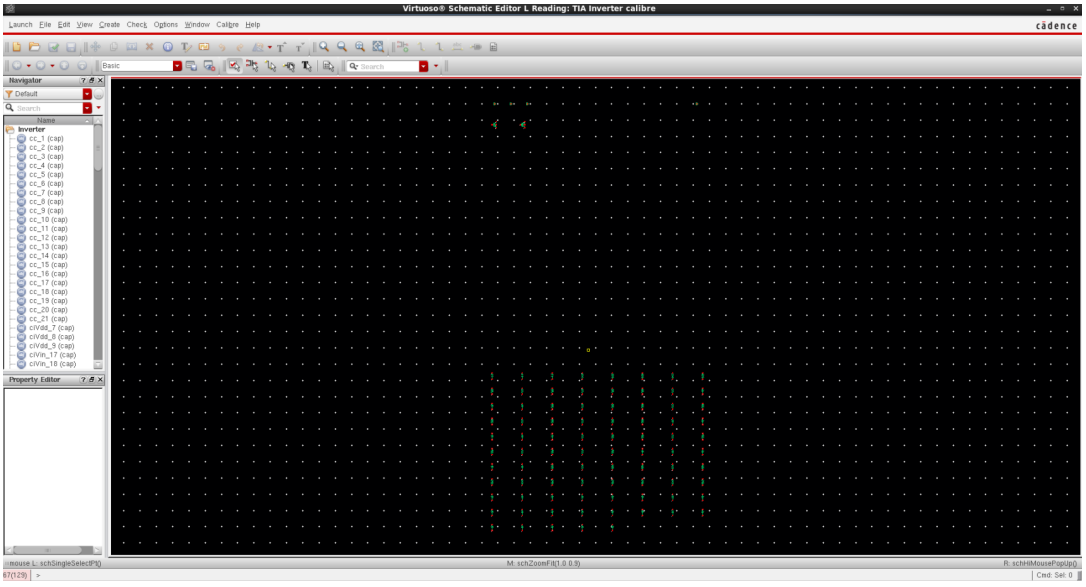


Figure B.21: Example generated calibre view extracted schematic.

## B.5 Simulating the extracted netlist

After extracting all the layout's parasitics, it is time to simulate. To compare the schematic and layout simulation, the schematic will be simulated in the first time. It is therefore necessary to set 10 ms in the transient simulation, as shown in Figure B.22.

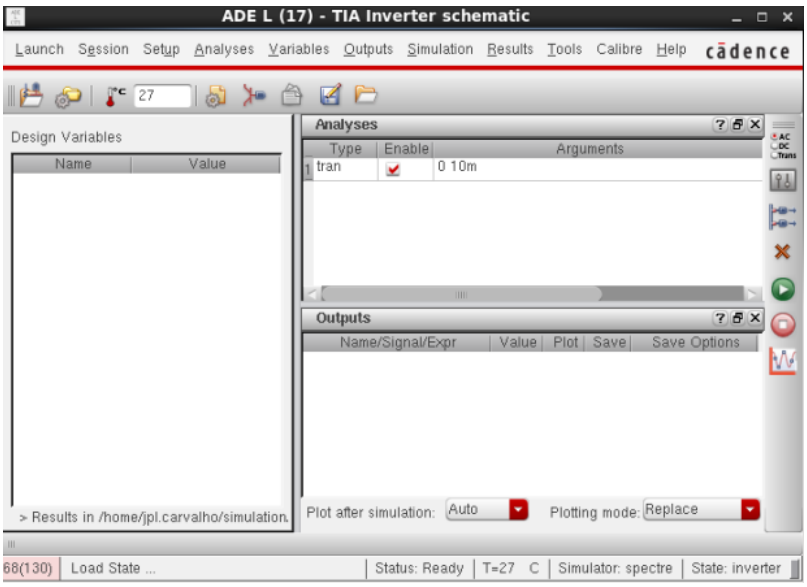


Figure B.22: Schematic Simulation.

It is necessary to click on "Append" to show the two outputs (schematic and layout). After this, press Results > Direct Plot > Transient Signal and click on $V_{out}$ pin. An inverter's output window will appear, as shown in Figure B.23.

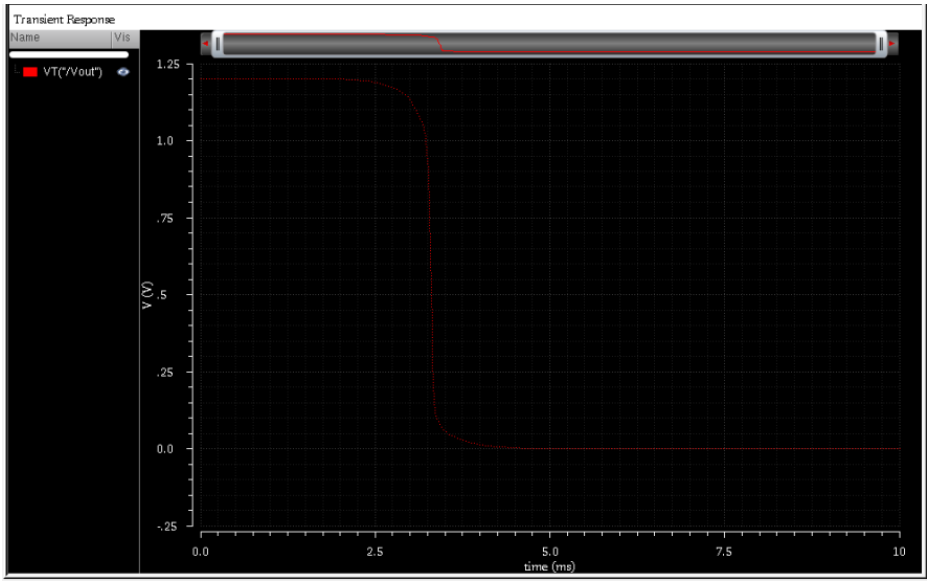


Figure B.23: Schematic Output.

Finally, at ADEL, select Setup > Environment and a window will appear, as shown in

Figure B.24.

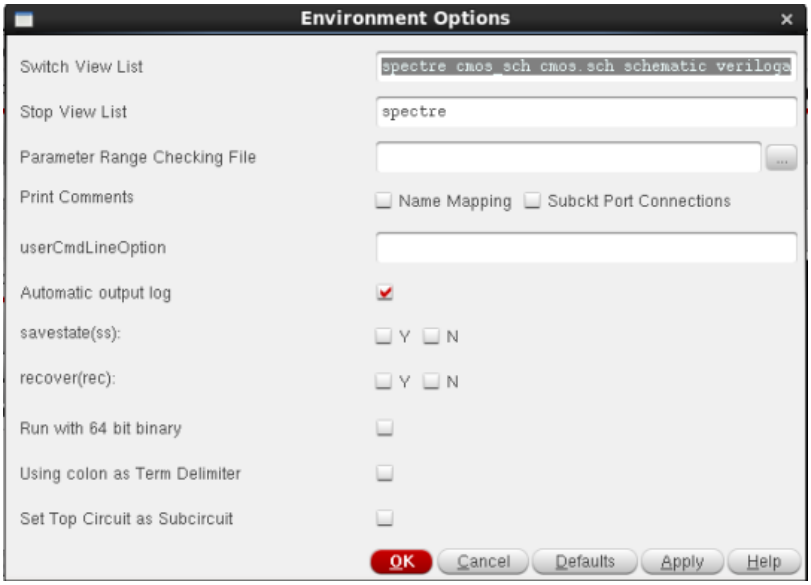


Figure B.24: Environment Options.

At "Switch View List" it is necessary to add "calibre" (without the quotes) as the first item in the list. Click "Ok" and Run ADEL. Lastly, press again Results > Direct Plot > Transient Signal and click on $V_{out}$ pin. An inverter's layout output window will appear, as shown in Figure B.25.

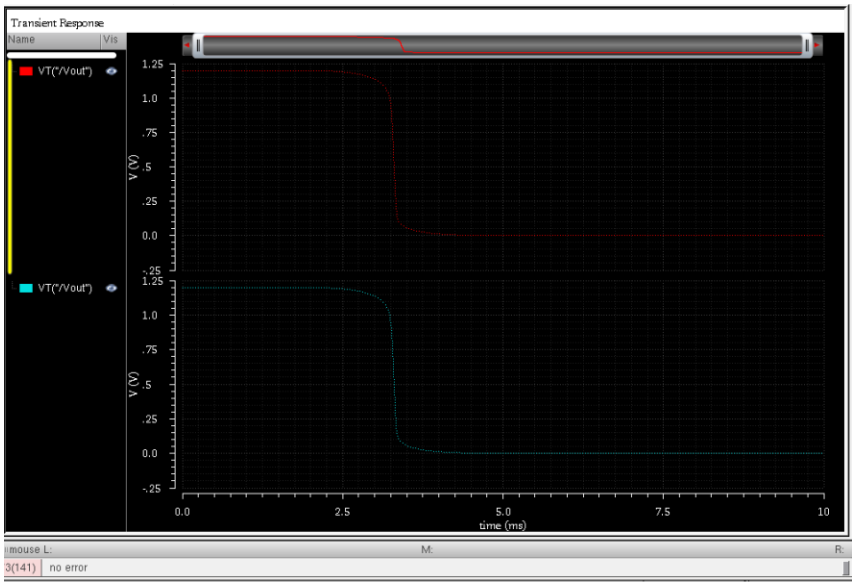


Figure B.25: Simulation - Schematic (red color) and Layout (blue color).