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Static and dynamic modelling for IGZO-TFT devices with high-κ multilayer dielectric.

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Abstract

Indium-Gallium-Zinc-Oxide thin-film transistors (IGZO-TFT) are a strong alternative technology for the current trend of Si based field-effect transistor (FET) for flat-panel display backplane and internet of things internet of things (IoT). In these applications, comprehensive understanding and accurate modelling of thin-film transistor (TFT) is compulsory for systematic circuit design.

In this study, IGZO-TFTs with high-κ multilayer dielectric, which were previously fabricated at CENIMAT/I3N Portugal are characterized in the University of Cambridge at the department of electrical engineering. Alongside this characterization, it is developed a compact static model that is capable of describing above-threshold linear behaviour. This model is based on physical parameters and also accounts the effects of contact resistance in source and drain terminals. Furthermore, it is developed a dynamic small signals model, based on conventional FET models and its validity is studied with the help of S-Parameters and capacitance-voltage characteristics (C-V) characteristics.

The great advantage of the developed models, in both static and dynamic aspects, is the low number of parameters required to be extracted physically with good fitting results. This can empower new users that are not so familiar with the modelling aspect to design simple electrical circuits with IGZO-TFTs.

Keywords: IGZO, TFT, Static models, Dynamic models, Compact models, small signal.

Resumo

Os transistores de filme fino baseados em óxidos de Índio Gálio e Zinco (IGZO-TFTs) são uma tecnologia alternativa muito interessante para a atual tendência de transistores de efeito de campo, que é baseada no Silício, para o painel traseiro de mostradores planos e aplicações em internet das coisas (IoT). Nestas, a compreensão exaustiva e uma boa modelagem do comportamento de TFTs são requisitos obrigatórias para a projeção sistemática de circuitos.

Neste estudo, os TFTs IGZO com dielétrico multicamadas de alta permissividade, que foram fabricados à posteriori nos laboratórios CENIMAT / I3N Portugal, são caracterizados no departamento de engenharia eletrotecnia da Universidade de Cambridge. Juntamente com essa caracterização, desenvolve-se um modelo estático compacto que é capaz de descrever o comportamento linear acima da tensão limiar de condução. Este modelo é baseado em parâmetros físicos e também contabiliza os efeitos da resistência de contato nos terminais de fonte e dreno. Além disso, é desenvolvido um modelo dinâmico de pequenos sinais, baseado em modelos de transistores de efeito de campo convencionais e a sua validade é estudada com a ajuda das características dos Parametros-S e curvas de capacidade tensão.

A grande vantagem dos modelos desenvolvidos, tanto no modelo estático assim como no dinâmico, é o baixo número de parâmetros necessários para serem extraídos fisicamente. Isso pode capacitar novos usuários que não estão tão familiarizados com o aspecto de modelagem para conseguirem projetar circuitos elétricos simples com esta tecnologia.

Palavras-chave: IGZO, TFT, modelagem, modelos estáticos, modelos dinâmicos, modelos compactos, pequenos sinais

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List of Symbols

N_{A} acceptor concentration.

V_{ch} channel potential.

q charge of an electron.

R_{DS} combined contact resistance from drain and source sides.

I_{DS} current flow between drain and source.

n_{tr} density of occupied traps.

κ dielectric constant.

ΔL Difference between mask channel length and effective channel length.

N_{D} donor concentration.

V_{D} drain voltage.

L_{eff} effective channel length.

ε electric permittivity of the material.

ψ electric potential.

R_{n} electron recombination rate.

G_{n} electron generation rate.

J_{n} electron current density.

R_{p} hole recombination rate.

G_p hole generation rate.

J_p hole current density.

α power parameter.

V_S source voltage.

V_T threshold voltage.

K transconductance parameter.

Acronyms

CAD	computer aided design.
C-V	capacitance-voltage characteristics.
CVU	capacitance-voltage unit.
DOS	density of states.
ENA	Keysight E5061B network analyser.
FET	field-effect transistor.
I-V	current-voltage characteristics.
IGZO	Indium-Gallium-Zinc-Oxide.
IGZO-TFT	Indium-Gallium-Zinc-Oxide thin-film transistors.
IoT	internet of things.
RPI	Rensselaer Polytechnic Institute.
SPICE	Simulation Program with Integrated Circuit Emphasis.
TFT	thin-film transistor.

Objectives

Device modelling can be very tedious, with large amount of parameters to be extracted as well different types os measurements that they might require. Furthermore, the rapid evolving device structure and materials in the TFT family demand for simple compact models that can serve as a platform for simple circuit design. This thesis work, which is part of the project BET-EU (Materials Synergy Integration for a Better Europe) under the Grant agreement No. 692373, is concerned with the viability of developing compact models for IGZO-TFTs with high-κ multilayer dielectric based on other existing models for rapid and simple modelling. Moreover the project is aimed to develop an above-threshold and small-signal model that require minimal number of direct measurements which may serve as a platform for simple circuit design applications.

Work Stucture

This work is organized as follows: The motivation introduces the relevance of IGZO-TFT technology and the importance of developing compact models to open doors for this technology to flourish in new applications; It is followed by the introduction where it is explained how device modelling came to be, what are compact models and how they are subdivided, small signal in three terminal devices and lastly the state of the art in TFT modelling. Chapter 2 explains the overall work-flow and methodology used in this project. Chapters 3 and 4 describe each of the studies. Chapter 3 includes the procedure for parameter extraction followed by the model representation. Chapter 4 includes all the work done on the development of the small signal model. Finally, Chapter 5 summarizes all the work done on TFT compact modelling, moreover some future ideas are presented.

Introduction

1

1.1 Motivation

FETs are developed using a wide range of semiconductor materials, with the most predominantly employed being the Silicon. FETs applications end up in many technological products and lead to performance increase and reduction in size and weight, with increasing miniaturization [1]. Ever since the Si FET technology started to mature a continuous progress has been made year after year in both large-scale integrated circuits and flat-panel displays.

Given this circumstances Indium-Gallium-Zinc-Oxide (IGZO) emerged as one of the most competitive alternative for such applications. The combination of low processing temperature, transparent nature, good uniformity even in large areas and excellent electrical properties (typically having the channel mobility higher in one order of magnitude when compared to α-Si) have proven to be a great asset for this technology.

In fact, it took only nine years after the first working prototype of IGZO-TFT, published by Hideo Hosono's group, to come up with a commercially available product by *Sharp*. The IGZO-TFTs were employed in the display of their flagship smart-phone [2].

Despite the rapid growth for IGZO in flat-panel displays, the same is not observed in other potential applications, such as IoT, augmented displays and wearables. Great part of it could be explained due to circuit design complexity. In one hand, the circuit design in flat-panel displays is limited to a few repetitive circuits, in that sense designing and optimizing is simple here. On the other hand, TFTs have a wider range of materials, device structure and processing methods when compared to conventional Si technology. For this reason the creation of a universal behavioural device model for TFTs is a big challenge [3].

The combination of these factors motivate the development of simple and accurate device behavioural models for a more specific group TFTs, that can have potential application in computer aided design (CAD) tools for new circuit designs.

1.2 The beginnings of device modelling

In the early days, when transistors were not microscopic, the circuit design was heavily empirical. With discrete elements such as capacitors, inductors, resistors and transistors at the disposal of the designer, he would build and test his circuit onto a circuit board. The design procedure would start with some simple electrical concepts and the "tweaking"(sizing in integrated circuits) would be made by simply replacing elements in value or type till the specifications were met. With the emergence of integrated circuits this simple procedure was no longer possible, this may be attributed to some key reasons.

Firstly, the integrated elements are now embedded in a common substrate, which makes the replacement difficult to practically impossible. Alongside this the common substrate to all elements will naturally form parasitic components that are not so easy to account for, empirically.

The second major reason comes along with “the size of both worlds”. In discrete elements, the different encapsulated components are linked to each other through bread-board tracks which separate them in tens of millimetres. While in the integrated case, these connections are in the micron level. This shorter distance, makes self-inductances of the interconnection lines, on integrated circuits, non-neglectable. Besides that to produce an inductive element with small tolerance is not so easy, many times it has to be implemented with an external element.

In the present days, designers resort to many CAD tools such as Simulation Program with Integrated Circuit Emphasis (SPICE), Spectre etc., for their circuit analysis. These softwares contain mathematical models that are capable of describing quantitatively the terminals behaviour of an element. With this the designer can forecast the behaviour of a desired circuit without the need of its fabrication, reducing time and cost. How well the forecast is done, is entirely up to the models behind the program. For this reason it is very important to understand how these models behave.

1.3 Compact models

Compact models are generally aimed at providing accurate device behaviour, which covers all working regions, for circuit simulation. The accuracy of a compact model does not only depend on the set of mathematical equations, but also on the accuracy of the numerical constants in these equations. In device modelling these constants are called parameters, which can be extracted through physical measurements, or in the impossibility of this, with numerical simulations. So, the model developer must not only account for the model equations but also for the parameter values.

While the main goal is accuracy, it is also necessary to account for speed of simulation. Some circuits may contain millions or more transistors, in such cases it is imperative that the mathematical model of each element is as simple as possible, otherwise the CPU time and/or memory storage will be prohibitive [4].

The compact models can be subdivided in two major groups, physical and empirical models which will be discussed in the next sections.

1.3.1 Physical based compact models

Physical based compact models are defined when the equations that describe the model are derived from device physics. These equations are based on analytical functions, where explicit results are desirable. The analyticity is very important because it grantees that the function is infinitely differentiable, otherwise the computer program could lead to

numerical instabilities. Especially in time based analysis, the calculation of harmonic-distortion often require the existence of derivatives.

Since the parameters have physical meaning and in general case have multiple extraction methods, they can help to check the correctness of the parameter extraction procedure.

The major drawback of these expressions is that they generally only apply for a specific range of voltage bias condition, outside of those ranges other expressions need to be used. In order to have good convergence and smooth transition between the various regions, a mathematical smoothing procedure is used, typically in the form of harmonic averaging. Other than that, these models take long time to be developed even with experienced researchers (several months to years) [5].

1.3.1.1 Foundation for physically based compact models

Having established the general characteristics of physically based compact models, we now analyse the building blocks that constitute the foundation of most of these models.

A semiconductor can be described by a set of coupled non-linear partial differential equations, more specifically Poisson's equation for drift diffusion

$$\nabla^2 \psi = \frac{-q}{\varepsilon}\left(p - n + N_{\mathrm{D}} - N_{\mathrm{A}} + n_{\mathrm{tr}}\right) \tag{1.1}$$

and the current continuity equation for carrier distribution

$$\begin{cases} \frac{\partial n}{\partial t} = \nabla \cdot J_{\mathrm{n}} + G_{\mathrm{n}} - R_{\mathrm{n}} \\ \frac{\partial p}{\partial t} = -\nabla \cdot J_{\mathrm{p}} + G_{\mathrm{p}} - R_{\mathrm{p}} \end{cases} \tag{1.2}$$

where

$$\begin{cases} J_{\mathrm{n}} = q\mu_{\mathrm{n}} n E + q D_{\mathrm{n}} \nabla n \\ J_{\mathrm{p}} = q\mu_{\mathrm{p}} p E - q D_{\mathrm{p}} \nabla p \end{cases} \tag{1.3}$$

In Eq. (1.1), ψ is the electric potential, q is the charge of an electron, μ_{n} and μ_{p} are the mobility of the electrons and holes, ε is the electric permittivity of the material, n and p represent the concentration of electrons and holes, respectively, N_{A} and N_{D} are the acceptor and donors concentration, respectively, and n_{tr} is the density of occupied traps. In Eq. (1.2), J_{n} and J_{p} are electron and hole current densities, G_{n} and G_{p} represent the generation rates, R_{n} and R_{p} are the recombination rates. Lastly, (1.3) the first part of the sum is related to the drift (proportional to electrostatic field), and the second part to diffusion (proportional to gradient of the carrier density) [6].

Dealing with these set of equations is somewhat cumbersome, and for the general case of device structures they will not lead to closed-form solutions. The best results are achieved with numerical methods which, as seen previously, come at the cost of using many computational resources.

In 1952 Shockley introduced an important simplification to this problem [7], by realizing that the rate of change of the electrical field is much greater in one dimension (gate

to active layer) than the other (source to drain). By decoupling x and y dimensions, the problem simplifies into two 1-D problems. One first equation describes the number of carriers in the channel, while the second equation describes the carrier flow from source to drain. Later, in 1966 H.C.Pao and C.T. Sah [8], based on this concept, proposed a MOSFET model that has been a benchmark ever since to many compact models, since it has only a few assumptions that are transversal to many other FET technologies [9].

By assuming, that the hole current and the recombination/generation can be neglected, the expression that gives the current I_{DS} that flows from drain and source is

$$I_{DS} = \mu \frac{W}{L} \int_{V_S}^{V_D} Q \quad dV_{ch} \tag{1.4}$$

In Eq. (1.4), W is the width of the transistor, L is the length, V_S and V_D are source and drain voltages, Q is the integrated mobile charge, and V_{ch} the channel potential.

From here, two main classes of models, that are capable of describing I_{DS} have emerged. The first kind, known as charge based models, define I_{DS} with an induced charge term. While the second type, surface-potential based models, assume a density of states (DOS) profile to solve the Poisson's equation, and I_{DS} is expressed in terms of surface potential at source and drain [10].

1.3.2 Empirical based compact models

In the other spectrum we have empirical based compact models, here the expressions are based on mathematical curve-fitting or polynomial approximations to describe the behaviour of any kind of transistor. Since the model does not require deep understanding of the device physics, the development time is greatly shorten. However, without proper understanding of the underlying device physics, the resulting parameters could be large and unmeasurable trough extraction procedure. In practice purely empirical models do not exist, the models used in simulation are often a combination of terms and coefficient that are physical and empirical.

1.4 Small-signal modelling

While the general case in the development of transistor models is the in-depth understanding of the device physics, there is another important element for circuit analysis (which electrical engineers very much like to use), the small-signal model. In small-signal analysis non-linear devices, such as the transistor, are described with linear equation under certain constrains of biasing. If the AC signal is small enough relatively to the bias voltage, then the whole signal can be represented as a DC signal with small perturbations. This small non-linear effect can then be approximated by the Taylor expansion series near the biasing point by its first order partial derivative. Finally, the partial derivative translates into variations of impedance throughout the signal, and can be used to represent a

linear equivalent circuit giving the response of the real device under a small AC signal [11].

1.4.1 Midband small-signal model

For a general three terminal device with G,S and D as the arbitrary terminals, the current-voltage characteristics (I-V) equation can be defined as follows :

$$\begin{cases} I_{\mathrm{D}} = f_1(V_{\mathrm{GS}}, V_{\mathrm{DS}}) \\ I_{\mathrm{G}} = f_2(V_{\mathrm{GS}}, V_{\mathrm{DS}}) \end{cases} \tag{1.5}$$

For small changes of V_{GS} and V_{DS}, the current differences would approximately follow the first order partial derivatives of both current functions respectively

$$\begin{cases} \mathrm{d}I_{\mathrm{D}} = \frac{\partial f_1}{\partial V_{\mathrm{GS}}}\mathrm{d}V_{\mathrm{GS}} + \mathrm{d}I_{\mathrm{D}} = \frac{\partial f_1}{\partial V_{\mathrm{DS}}}\mathrm{d}V_{\mathrm{DS}} \\ \mathrm{d}I_{\mathrm{D}} = \frac{\partial f_2}{\partial V_{\mathrm{GS}}}\mathrm{d}V_{\mathrm{GS}} + \mathrm{d}I_{\mathrm{D}} = \frac{\partial f_2}{\partial V_{\mathrm{DS}}}\mathrm{d}V_{\mathrm{DS}} \end{cases} \tag{1.6}$$

Now by assuming good linearities at the bias point, the partial derivatives are simplified to mere constants as follows

$$\begin{cases} i_{\mathrm{d}} = g_{\mathrm{m1}}v_{\mathrm{gs}} + \frac{v_{\mathrm{ds}}}{r_{o1}} \\ i_{\mathrm{d}} = \frac{v_{\mathrm{gs}}}{r_{o2}} + g_{\mathrm{m2}}v_{\mathrm{ds}} \end{cases} \tag{1.7}$$

The coefficient v_{ds} for i_{d} and v_{gs} for i_{g} can be represented as passive components, in this case r_{o1} and r_{o2} respectively. While v_{gs} for i_{d} and v_{gs} for i_{d} is only representable with active component, a voltage controlled current source (transconductance in the form of g_{m1} and g_{m2} are used). The small signal representation of these equations for mid-band range can be seen in Fig. 1.1.

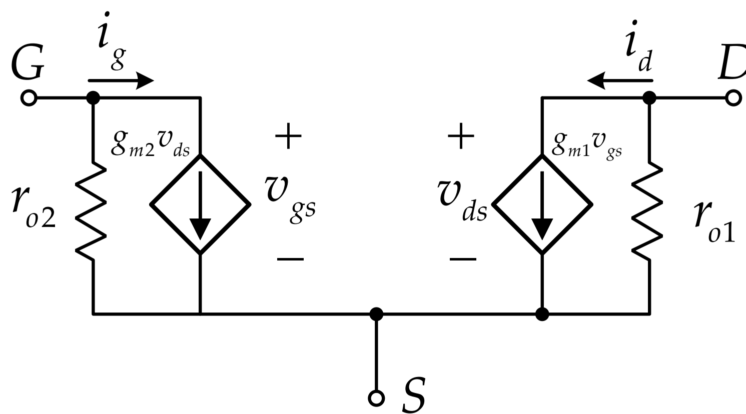


Figure 1.1: Small-signal model for a general 3 terminal device in mid-band frequency, also known as hybrid-pi model [12].

For simplification purposes in many FET devices it is considered that V_{DS} does not affect I_{G} and the r_{o2} is high enough that gate leakage current can be neglected, therefore the gate and source terminals are presented as open-circuit.

1.5 State of the art in TFT modelling

In recent years, many efforts have been made towards the physical approach in the hopes of developing simple and accurate models. From all the different families of TFTs, α-Si is the most well-studied. Numerous models have been published based on the study of DOS, which are capable of describing both static and dynamic behaviours in various working regions [13–15]. The effects of traps on V_{T} shift [16] and current leakage [17] have also been implemented in model design. In fact a commercial standard is available which captures most of device properties, called Rensselaer Polytechnic Institute (RPI) model. Also it has been implemented the EKV model, designed initially for the MOSFET, for this family of transistors [18].

For organic TFTs, many developments have been made based on the conduction mechanism in these devices [19, 20]. However, due to the high variety of materials and structures, the physical mechanism also differs. In that manner the effort has gone towards a more unified but less physical model [21].

As for metal-oxide TFTs modelling attempts are still in their primordial. Despite that, there has been reported good results with the use of RPI models, with minor adjustments, in IGZO devices [22]. In 2016 a model based on effective DOS extraction has been proposed for Verilog-AMS and SPICE aplications, called CAMCAS model that focuses in oxide-TFTs with potential extendibility to other families [3].

In the other spectrum, there has been developed empirical models based on neural networks that are design to make the model development as fast as possible [23, 24].

Methodology

2

In this chapter, it will be addressed the overall work-flow of the project. In the first instance the device fabrication and structure, prior to this project, are evoked. Following that, some guidelines about the development of both dynamic and static models are discussed.

2.1 IGZO-TFTs fabrication and structure overview

Prior to this project, IGZO-TFT with high-κ multilayer dielectric were fabricated, at CENIMAT/I3N Portugal. The TFTs were produced according to a staggered bottom gate, top-contact structure on Corning glass substrates (Fig. 2.1). RF magnetron sputtering was used to deposit thin films of Molybdenum as electrodes, IGZO (1:2:2 In:Ga:Zn atomic ratio) as active layer and Ta_2O_5/SiO_2 for the multilayer dielectric. The patterning is achieved through lift-off process, and to finish off a post-deposition annealing is done in air atmosphere at no more than 200 °C. The characteristic that stands out is the multi-layer dielectric, which is conceived to have high-κ and high bandgap energy to minimise problems of instability, gate-leakage and hysteresis. For a more detail explanation on the fabrication and characterization of similar devices [22] is an excellent read.

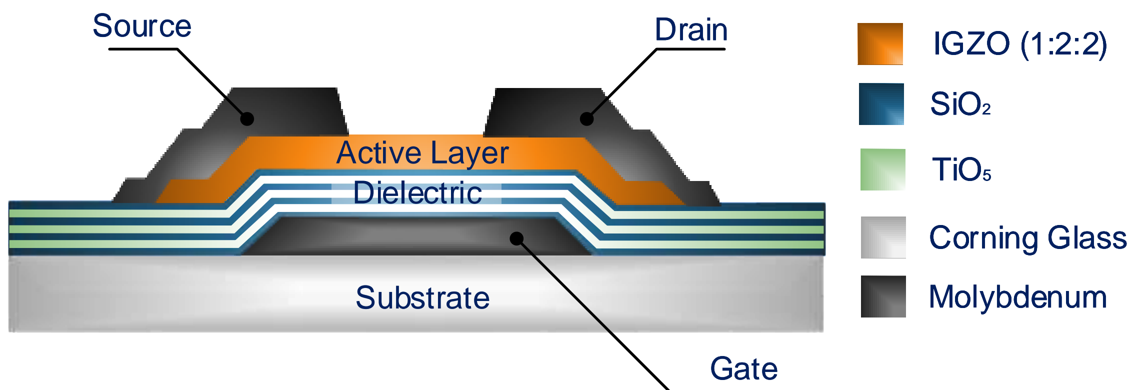


Figure 2.1: TFT device structure used in this work: staggered bottom gate, top-contact

The core work of this thesis is done at the Hetero-Genesys Laboratory of the University of Cambridge. They have a multi-disciplinary research environment including the development of compact models for TFTs. In that sense, all the characterization and development of models for the devices in study is done at this location.

2.2 Static model

As seen in chapter 1.3.1, the development of a new physical based compact model can take many months or even years. In that sense, the strategy here was to find a good compact model that was already developed starting with similar assumptions of our working devices. The first good candidate is the MOSFET level 1 model that has the following equations, for Triode region ($V_{GS} > V_T$ and $0 < V_{DS} < [V_{GS} - V_T]$)

$$I_{DS} = K\frac{W}{L}\left[(V_{GS} - V_T)\, V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{2.1}$$

and for Saturation ($V_{DS} > V_{GS} - V_T$ and $V_{GS} > V_T$)

$$I_{DS} = \frac{K}{2}\frac{W}{L}\,(V_{GS} - V_T)^2 \tag{2.2}$$

In Eq. 2.1 and Eq. 2.2 the K is the transconductance parameter, W and L are the width and length of the channel.

Having seen the MOSFET equations for I_{DS}, and after some quick $I_{DS}(V_{GS})$ measurements in the saturation region we observed that the TFT devices did not perfectly obey to this proportionality: $I_{DS} \propto (V_{GS} - V_T)^2$. This is mainly due to velocity saturation effects [25], so a more general power parameter (α) is used instead of 2. Besides this, the other major concern in TFTs comes from big contact resistance (R_{DS}). There is also another consideration done, that comes along with the channel length. When fabricating a TFT device the L value is typically attributed to the design mask value. However due to the fabrication process itself the channel length may not correspond exactly to this value. This variation (ΔL) can be quantified empirically and it is added to the mask L value. This result into the effective channel length, L_{eff}.

The static model for TFT can be defined as the structure shown in Fig. 2.2 where the I-V characteristics are modelled for the internal transistor and the R_{DS} in both contacts are accounted separately.

Based on [26] model which accounts for these effects, the primed voltages V'_{DS} and V'_{GS} can be defined as follow:

$$\begin{gathered} V'_{DS} = V_{DS} - I_{DS}\,(R_S + R_D) \\ V'_{GS} = V_{GS} - I_{DS} R_S \end{gathered} \tag{2.3}$$

The drain-source current for linear regime ($I_{DS,lin}$) can be written as a function of V'_{GS} as

$$I_{DS,lin} = K\frac{W}{L_{eff}}\left[\left(V'_{GS} - V_T\right)^{\alpha-1} V'_{DS} - \left(1 - \frac{1}{\alpha}\right)(V'_{DS})^{\alpha}\right] \tag{2.4}$$

With $\alpha = 2$ this equation simplifies into Eq. (2.1). If we now consider that $R_S = R_D = \frac{R_{DS}}{2}$, the final equation for $I_{DS,lin}$ can be obtained by substituting (2.3) into (2.4)

$$I_{DS,lin} = K\frac{W}{L_{eff}}\left[\left(V_{GS} - V_T - \frac{I_{DS}R_{DS}}{2}\right)^{\alpha-1}(V_{DS} - I_{DS}R_{DS}) - \left(1 - \frac{1}{\alpha}\right)(V_{DS} - I_{DS}R_{DS})^{\alpha}\right] \tag{2.5}$$

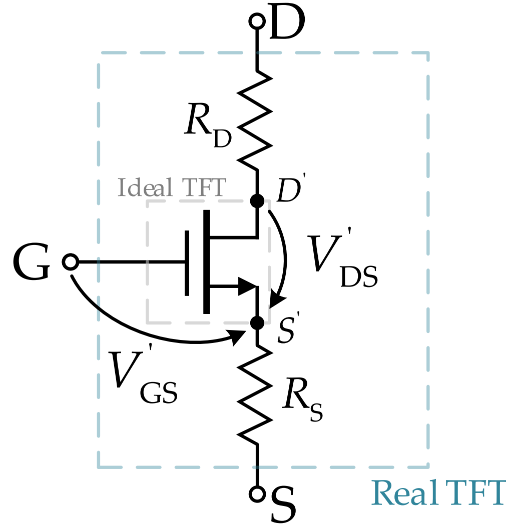


Figure 2.2: Equivalent circuit of static TFT model.

However for parameter extraction purposes, a simplification is necessary. Considering $\frac{I_{DS}R_{DS}}{2} \approx 0.5V_{DS}$ and by forcing V_{DS} to be very small, in comparison to V_{GS} and V_T, the Eq. (2.5) can be simplified into:

$$I_{DS,lin} = K\frac{W}{L_{eff}}(V_{GS} - V_T - 0.5V_{DS})^{a-1}(V_{DS} - R_{DS}I_{DS}) \tag{2.6}$$

For device modelling, the linear region is the most important for parameter extraction, furthermore the saturation regime can be deduced from this equation, by substituting $V_{DS} = \alpha_{sat}(V_{GS} - V_T)$. The term α_{sat} is applied as a correction parameter, since in real devices the transition between linear to saturation is not always at $V_{DS} = (V_{GS} - V_T)$. Another strategy, is to consider a smooth transition from V_{DS} to $V_{GS} - V_T$, this can be achieved with harmonic averaging methods. In fact this second method is chosen for this project, due to its simplicity.

With a satisfactory model, the different parameters were extracted, this will be presented in later chapter 3.

2.3 Dynamic model

For this part of the project, a small signal model based on MOSFET devices was modelled, the main challenge here was to find a common ground that could validate or discard the use of MOSFET small-signal model for the devices in study, this gains higher importance at high frequencies where parasitic capacitances are no longer neglected. The common ground was found with the calculation of unit-gain frequency which is equivalent to h_{21} parameter, this last one can be indirectly measured through S-parameters. For a simpler understanding of this part, the full procedure and discussion is presented in a single chapter (Chapter. 4).

3 Above-Threshold parameter extraction and Linear Model

In this section, it is extracted the parameters required to describe the TFT in the linear region for static modelling (Eq. (2.6)). These parameters are K, L_{eff}, V_{T}, α and R_{DS}. For the measurement set-up it is used a Keithley 4200 semiconductor characterization system to measure I-V characteristics. It is considered TFTs with $W \sim 20\mu$m and different channel lengths, $L \sim 20; 40; 80; 160$ μm, the reasoning for this design of experiment is mainly due to R_{DS} extraction. To minimise measurement errors, each sized TFT has 3 replicas making a total of 12 transistor for measurement. The DC bias conditions are chosen to be $V_{\text{DS}} = 5$ mV and a voltage sweep is performed between the gate and source from -5 to 15 V with an incremental step of 0.1 V, this ensures the TFT to work in linear region. For the output characteristics it is performed a voltage sweep from $V_{\text{DS}} = 0$ V to 15 V with 0.1 V increments, for each value of V_{GS}. For multiple voltages V_{GS} has steps of 1 V from 5 V to 15 V.

3.1 Threshold Voltage, V_{T}

The threshold voltage V_{T} value is the most important electrical parameter in most of transistor modelling (including the TFTs). Besides this the correct extraction of V_{T} gains extra relevance due to the fact that many other parameters depend on the value of V_{T} for their own extraction.

After reviewing several methods [27] it is selected the second derivative method [28], which offers an extraction of V_{T} with relatively easy procedure and ensures an independence from series resistances. This last point is very important, especially in TFTs that can have contact resistances in the $M\Omega$ level.

The idea behind this method comes from the concept of an ideal MOSFET in linear region, where the current $I_{\text{D}} = 0$ for $V_{\text{GS}} < V_{\text{T}}$ and for $V_{\text{GS}} > V_{\text{T}}$ the current I_{D} is directly proportional to V_{GS}. The first derivative $\left(\frac{dI_{\text{D}}}{dV_{\text{GS}}}\right)$ results into a step function that remains zero for $V_{\text{GS}} < V_{\text{T}}$, and produces a positive constant value for $V_{\text{GS}} > V_{\text{T}}$. Thus, the second derivative $\left(\frac{d^2I_{\text{D}}}{dV_{\text{GS}}^2}\right)$ results into a Dirac delta function which in this case, is zero for all values except for $V_{\text{GS}} = V_{\text{T}}$, here function tends to ∞. For a real device such simplification is not totally correct, instead of the function becoming ∞ at $V_{\text{GS}} = V_{\text{T}}$, it exhibits a maximum at this value.

In Fig. 3.1 it is illustrated this mathematical behaviour in both real and ideal FET.

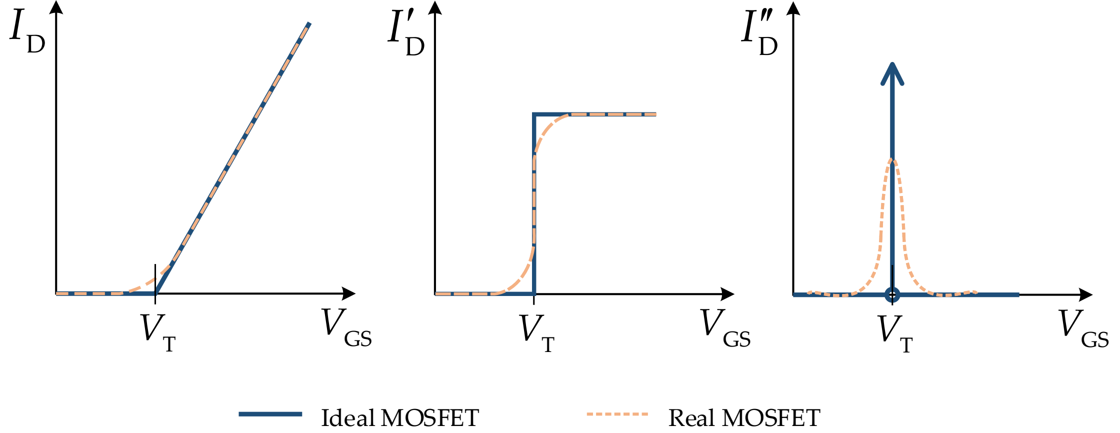


Figure 3.1: Second derivative method for V_T extraction in real and Ideal FET.

3.1.1 Results

After using the 2nd derivative method for the devices in study and smoothing out the data with OriginLAB (the Savitzky-Golay smoothing method is chosen to preserve the spike nature at V_T), it was obtained the following Fig.3.2. The extracted values of V_T can be found in Tab. 3.1.

Table 3.1: Extracted V_T values for different channel lengths

L (μm)	V_T (V)
20	0.68
40	0.81
80	0.30
160	0.23

The second derivative method can be quite noisy, this is mainly due to how the software does the derivative. Here the derivative is done by differentiating point by point, thus it is highly sensitive to small measurement changes. Regardless of that, the spike at V_T is very clear. In terms of the actual value of V_T, we observe a relatively large discrepancy for the different Ls (worst case has 0.58 V difference), this may present as a problem for the model. As a circuit designer perceptive you seek for a model that has standard parameters which can be trustworthy for any given transistor dimensions in that particular technology, otherwise the forecast ability of that model in circuit design is jeopardised.

3.2 Contact resistance, $R_{DS}W$ and ΔL

TFT devices are structured with several different materials, in this regard the interface between them produces a high resistance (when compared with MOSFET). The contact resistance R_{DS} happens at the interface between the active layer (IGZO) and source/drain

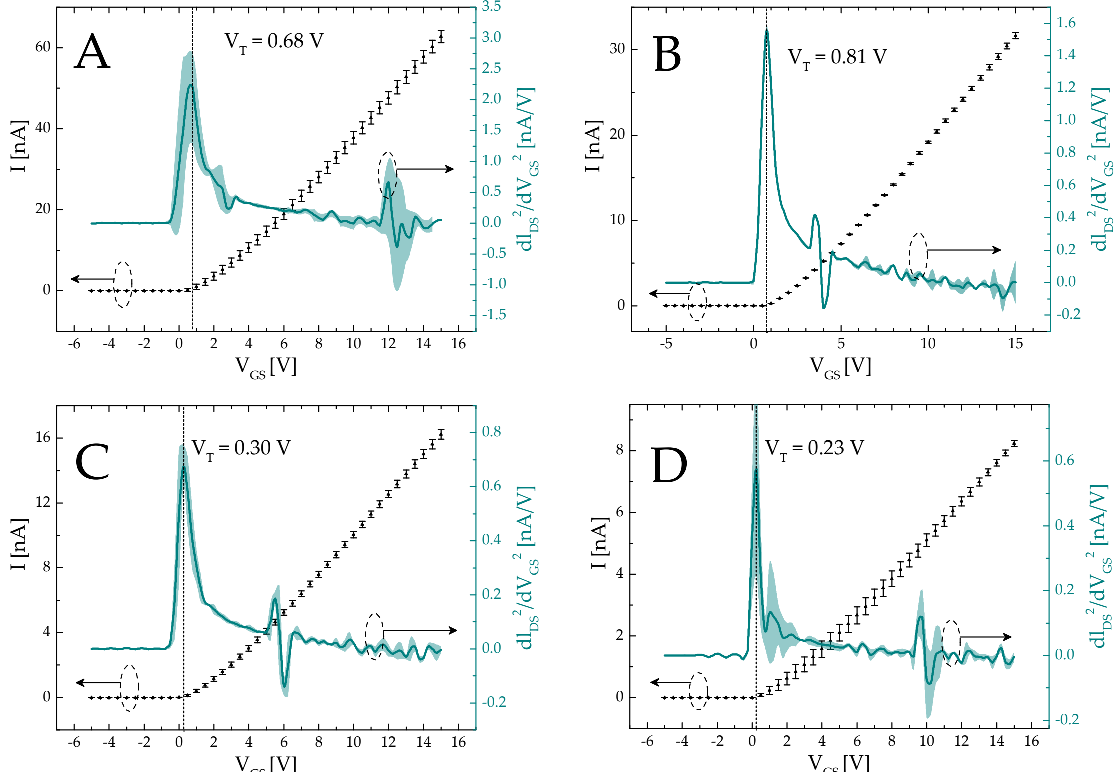


Figure 3.2: Extracted values of V_T for TFT devices with $W \sim 20\mu$m. The black plot is for $I_{\text{DS}}(V_{\text{GS}})$ characteristics, while the blue plot is the second derivative of the black plot. The error bar comes from the three replicas measured. A) $L \sim 20\mu$m; B) $L \sim 40\mu$m; C) $L \sim 80\mu$m; D) $L \sim 160\mu$m.

sides respectively. In order to find R_{DS}, the Eq. (2.6) is solved in order of total measured resistance, R_T

$$R_T = \frac{V_{\text{DS}}}{I_{\text{DS}}} = R_{\text{DS}}W + \frac{L + \Delta L}{K\left(V_{\text{GS}} - V_{\text{T}}\right)^{a-1}} \tag{3.1}$$

where L+ΔL is L_{eff} (effective channel length may differ from the masked due to fabrication process). According to (3.1), if one plots R_T versus L for various $V_{\text{GS}} - V_{\text{T}}$*, the intercept point should give ΔL and R_{DS} [29]. However in practice the intercept never happens in a single point, so a more accurate method is to use the slope (eg. A) and the y-intercept (eg. B) to create a new plot B versus A [30]. In this new plot the slope will give ΔL and the y-intercept the R_{DS}. The rewritten equation for 3.1, in respect to A and B is as follow:

$$\begin{cases} B = R_{\text{DS}} + A\Delta L \\ A = \frac{1}{KW(V_{\text{GS}} - V_T)^{\alpha-1}} \end{cases} \tag{3.2}$$

An illustrative procedure of these stages can be found in Appendix A

*The normalization of voltages is very important for good parameter extraction, especially after the discrepancy observed in Tab. 3.1.

3.2.1 Results

The intermediate plots of R_T vs $V_{GS} - V_T$ and R_T vs L can be found in Appendix B. The plot of B vs A is presented in Fig. 3.3 and the extracted values can be seen in Tab. 3.2.

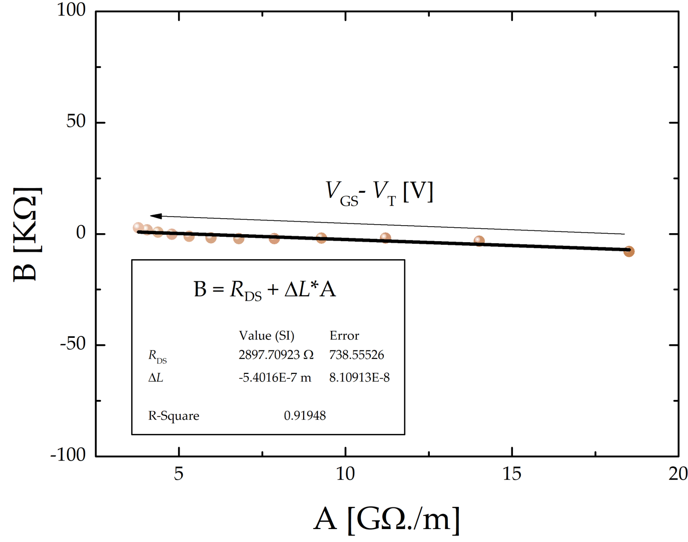


Figure 3.3: B vs A plot for R_{DS} and ΔL extraction

Table 3.2: Extracted values for $R_{DS}W$ and ΔL

$R_{DS}W$ (Ωcm)	ΔL (μm)
5.794 ± 1.4770	-0.54 ± 0.08

For general purposes value of R_{DS} is multiplied with W. By comparing this value with other TFT devices with similar structure [26, 31] (values for $R_{DS}W$ from few hundred Ωcm to several kΩcm), we can say that the contact resistance is quite low, this fact will come in handy for later parameter extraction.

3.3 Power parameter, α

The power parameter α can be extracted by dividing $I_{DS,lin}$ (2.6) with its first derivative ($g_{m,lin}$) as follow:

$$\frac{I_{DS,lin}}{g_{m,lin}} = \frac{V_{GS} - V_T - 0.5V_{DS}}{\alpha - 1} \frac{V_{DS}}{V_{DS} - R_{DS}I_{DS,lin}} \tag{3.3}$$

From Fig. 3.2 the current in linear region is at nA level and R_{DS} (@ $W \sim 20$ μm) is a few kΩ, therefore the voltage produced by $R_{DS}I_{DS,lin}$ is around the μV level. Thus the $R_{DS}I_{DS,lin}$ is much smaller than V_{DS} (5 mV). Apart from that, by comparing V_{DS} with the

other two voltages of Eq. 3.3 we can neglect V_{DS}. The final simplification is as follow:

$$\frac{I_{\text{DS,lin}}}{g_{\text{m,lin}}} = \frac{V_{\text{GS}} - V_{\text{T}}}{\alpha - 1} \tag{3.4}$$

The slope of $\frac{I_{\text{DS,lin}}}{g_{\text{m,lin}}}$ vs $(V_{\text{GS}} - V_{\text{T}})$ can be used to extract α. The result of the plot of Eq. 3.4 is presented in Fig. 3.4

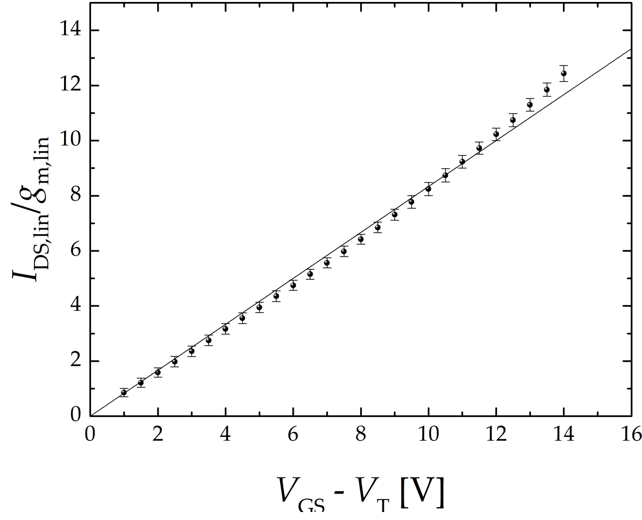


Figure 3.4: $\frac{I_{\text{DS,lin}}}{g_{\text{m,lin}}}$ vs $(V_{\text{GS}} - V_{\text{T}})$ for alpha extraction ($R^2 = 0.998$).

The linear fitting is done in such way that forces the intersect at (0,0), even with this the $R^2 = 0.998$ so a good extraction of α is achieved ($\alpha = 2.2$).

3.4 transconductance parameter, K

Since we have all other parameters for the model, K should be straight forward to obtain. A plot of $A^{-1/(a-1)}$ vs $V_{\text{GS}} - V_{\text{T}}$ may be used to extract K. This method is analogous to $\sqrt{I_{DS}/W}$ vs V_{GS} for mobility extraction in MOSFETs.

$$S^{a-1} = KW \tag{3.5}$$

Where S is slope of the best linear fit. The plotted $A^{-1/(a-1)}$ vs $V_{\text{GS}} - V_{\text{T}}$ graph may be found in Fig.3.5 The extracted value for K is 5.2×10^{-7}.

3.5 Model representation

After all the exhausting work of parameter extraction, we final arrive to the exciting part of model representation. Recalling the Eq. (2.5)

$$I_{\text{DS,lin}} = K\frac{W}{L_{\text{eff}}}\left[\left(V_{\text{GS}} - V_{\text{T}} - \frac{I_{\text{DS}}R_{\text{DS}}}{2}\right)^{\alpha-1}(V^*_{\text{DS}} - I_{\text{DS}}R_{\text{DS}}) - \left(1 - \frac{1}{\alpha}\right)(V^*_{\text{DS}} - I_{\text{DS}}R_{\text{DS}})^{\alpha}\right]$$

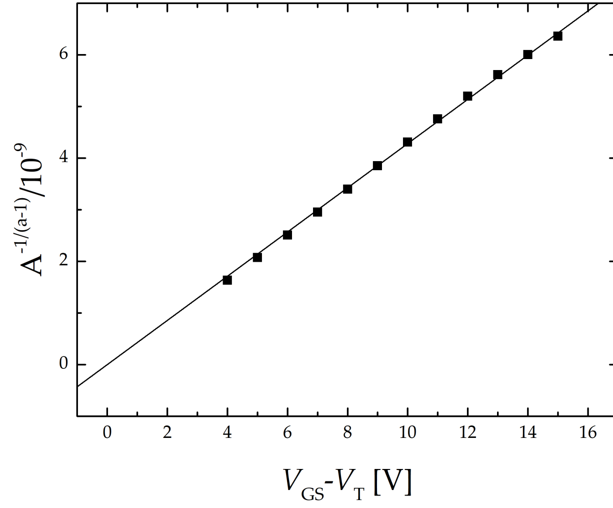


Figure 3.5: $A^{-1/(a-1)}$ vs $V_{GS} - V_T$ plot for K parameter extraction

and with the parameters extracted throughout this work (summarized in Tab. 3.3). The above threshold linear model is obtained with the resource of MATLAB as in Fig. 3.6.

Table 3.3: Summary of all parameters extracted for above-threshold linear model

L (μm)	$V_T(V)$	$R_{DS}W$ (Ωcm)	ΔL (μm)	α	K
20	0.68	5.794	-0.54	2.2	5.2×10^{-7}
40	0.81				
80	0.3				
160	0.3				

In order to be able to represent the output characteristics, some sort of saturation model is required, in this case the following is considered:

$$V_{DS}^{*} = \left[V_{DS}^{-m} + (V_{GS} - V_T)^{-m}\right]^{-\frac{1}{m}} \tag{3.6}$$

If we now let m be positive, then for $V_{DS} \gg V_{GS} - V_T$ the Eq. 3.6 will be dominated by the $V_{GS} - V_T$, in the other hand when $V_{DS} \ll V_{GS} - V_T$ the same equation will tend to V_{DS}. This constant m is defined empirically, with $m = 6$ the following output characteristics is obtained for different size transistors Fig. 3.7 and Fig. 3.8.

3.5.1 Discussion of Results

Analysing the results of the modelled I-V, and comparing it to the measured devices, one could say that the overall model is good to predict the behaviour of the TFT devices in study ($r^2 = 0.97$ for linear region). However this is done at the cost of having measured the V_T of every different size of transistor. Alongside that no apparent pattern is observed to enable the forecast ability of V_T without changing the fundamental model. Moreover

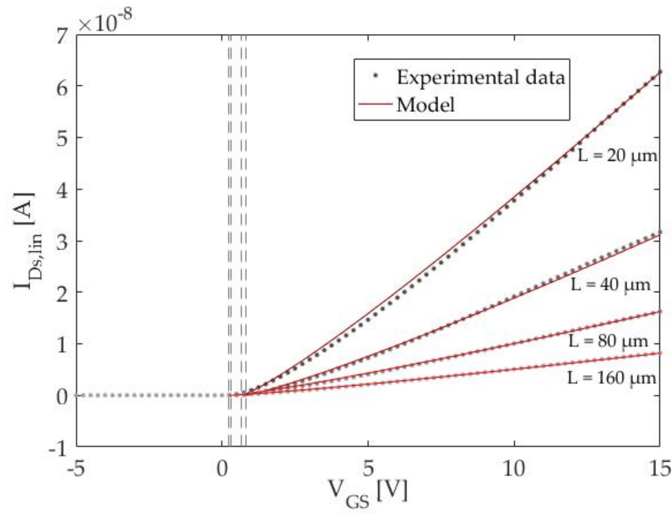


Figure 3.6: Comparison between the I_{DS} vs V_{GS} characteristics for the measured devices and developed model based on Eq. (2.5). The V_{DS} is maintained at 5 mV, to ensure the linear region

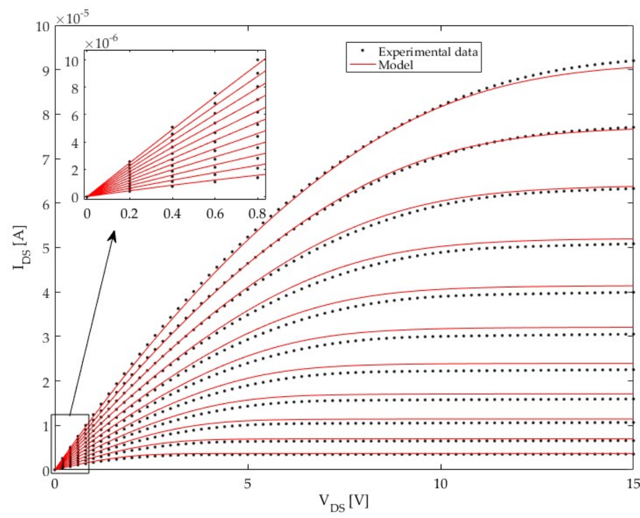


Figure 3.7: Output characteristics for $L \sim 20$ μm and $W \sim 20$ μm.

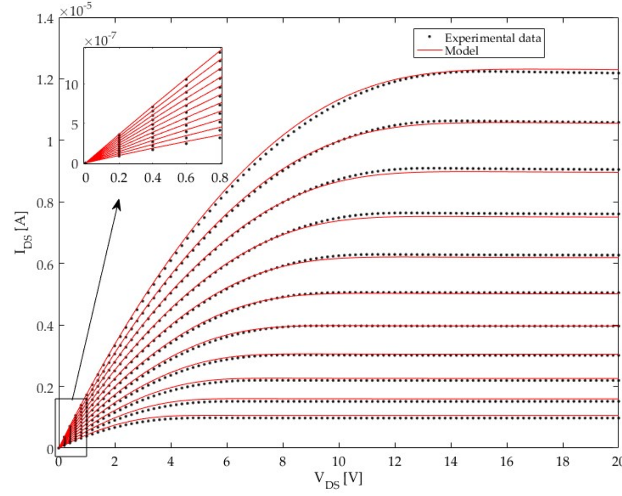


Figure 3.8: Output characteristics for $L \sim 160\ \mu$m and $W \sim 20\ \mu$m.

the equation of the model has only numerical solution, if no simplifications are assumed. Therefore solving these equations can take long time for each transistor. Restricting the use of this model for only simple circuit simulations. Regardless of that, this is already a good milestone.

Focusing on the output curves, the harmonic averaging method is quite good to make a smooth transition between the conventional linear and saturation regions. This avoids any convergence problems between these regimes. Nonetheless for this method to work the m value has to be attained empirically.

In many cases circuit designer like to do a simple and quick analysis (eg. DC operating point) in such scenarios it is interesting to have a simple separate saturation equation. A good option would be would be to consider the following equation:

$$I_{\mathrm{DS,sat}} = c\frac{K}{\alpha}\frac{W}{L}\left(V'_{\mathrm{GS}} - V_{\mathrm{T}}\right)^{\alpha} \tag{3.7}$$

where c had to be attained from fitting. The same harmonic averaging could be used for the transition between regions. However even with this we might not safeguard a smooth behaviour.

4 Small-signal model

From earlier chapter 1.4.1 we have seen that a generic three terminal device transistor can be represented with the hybrid-pi model. Moreover, the small signal model of the MOSFET that is adapted for TFT at low frequency is shown in Fig. 4.1. Here it is assumed based on the previous study, that the contact resistance is low enough hence it may be neglected.

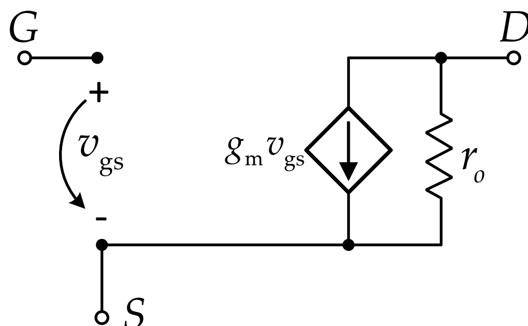


Figure 4.1: Low frequency small signal MOSFET model adapted for TFT

4.1 High Frequency TFT model

With the rise of the frequency of a given small AC signal, the whole TFT device physics has to be reconsidered especially with parasitic capacitances, that now start to shine.

The Bottom-Gate TFT structure is usually designed to ensure some overlap in the source electrode and Drain electrode as a misalignment margin for the lack of precision during lithography processes. Without this margin any unwanted offset may result in orders of magnitude reduction in I_{DS}. The downside of this overlap is the parasitic capacitance that forms in both source (C_{S}) and drain (C_{D}) electrodes.

Besides these parasitic capacitances there is the channel capacitance C_{ch} that forms between the gate and active layer. With these parasitic components in mind the model for small signal at high frequencies becomes the one shown in Fig. 4.2.

With this structure in mind and in order to evaluate the capability of this model to represent the devices in study, the relationship between input and output current is studied. This allows the calculation of current gain at short circuit (A_{i}).

$$A_{\mathrm{i}} = \frac{i_{\mathrm{out}}}{i_{\mathrm{in}}} \tag{4.1}$$

Where i_{out} and i_{in} are defined as

$$\begin{cases} i_{\mathrm{in}} = v_{\mathrm{in}} s C_{\mathrm{D}} + (v_{\mathrm{in}} - v_{\mathrm{out}}) s C_{\mathrm{S+ch}} \\ i_{\mathrm{out}} = v_{\mathrm{out}} g_{\mathrm{o}} + v_{\mathrm{in}} g_{\mathrm{m}} + (v_{\mathrm{out}} - v_{\mathrm{in}}) s C_{\mathrm{S+ch}} \end{cases} \tag{4.2}$$

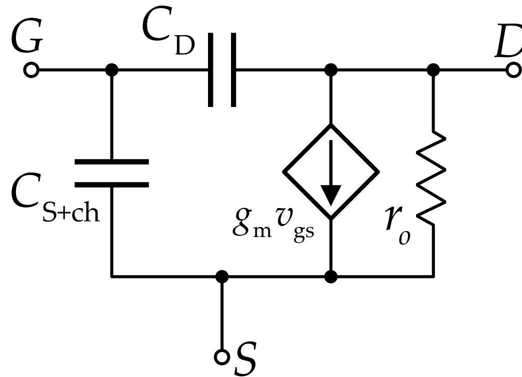


Figure 4.2: High frequency small signal MOSFET model adapted for TFT.

Substituiting Eq. (4.2) in Eq. (4.1) and considering $v_{out} = 0$ we get the current gain for the MOSFET model adapted to TFT as follow:

$$A_i = \frac{g_m - sC_D}{s(C_D + C_{S+ch})} \tag{4.3}$$

From equation Eq. (4.3) it is possible to extract that the model has one pole (at 0 Hz) and one zero (at $\frac{g_m}{C_D}$ Hz). If one considers that the zero is far from the cut-off frequency then the unit-gain frequency is given by:

$$f_T = \frac{g_m}{2\pi(C_D + C_{S+ch})} \tag{4.4}$$

4.1.1 Measurement setup

From the previous section, in order to build an AC model it is necessary to measure the current gain of the real device and compare the unit-gain frequency to evaluate the goodness of the model. One of the most common way to quantify this frequency is through a network analyser which can measure *s*-parameters, furthermore these parameters are useful for the calculation of *h*-parameters. More specifically the h_{21} value gives the short-circuit current gain (A_i).

For the purpose of these measurements, a Keysight E5061B network analyser (ENA) is used which is calibrated with CS-11 calibration substrate provided by GGB Industries, Inc. The standard measurement set-up is shown in Fig. 4.3. The bias-T separates the small signal input and output form the DC biasing circuitry.

This analyser is chosen due to its low frequency measurement capability (down to 5 Hz). In contrast, conventional network analysers work in the 100 kHz range, which may already be in the cut-off frequency level of the TFTs.

The ENA in use is capable of providing both DC and bias-T at port 1. However for port 2 an external bias-T is required. Since it is necessary to measure low frequencies (in comparison to MOSFET), the Picosecond 5546 bias-T is used which offers 3.5 kHz as per the low 3 dB frequency (lowest found on the market).

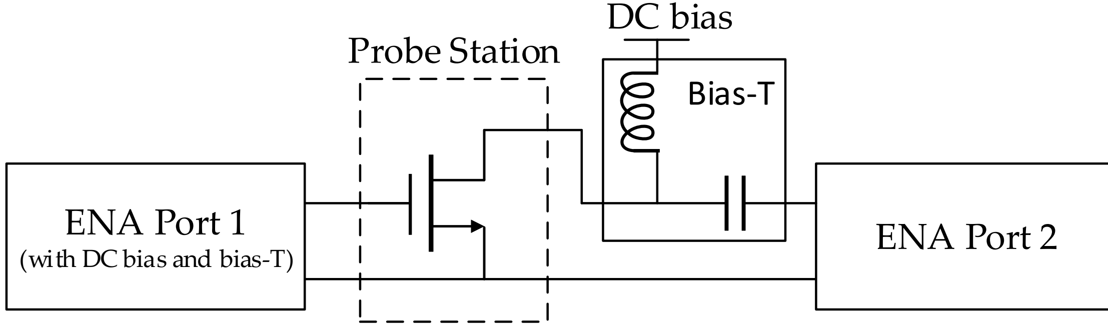


Figure 4.3: Measurement set-up for s-parameters and f_T.

The bias conditions are chosen to be V_{GS} = 8V and V_{DS} = 15V to ensure saturation regime. The devices used have W/L ratio of 160 μm/20 μm and 320 μm/20 μm, it is chosen large channel width mainly for an accurate capacitance extraction. In the same way that there is a variation of the channel length there is also a variation of channel width, at larger values of W this contribution is neglectable. The smaller channel length is chosen for a faster measurement, and it was the only fixed L value with different Ws available in the sample.

A calibration process is conducted by the aforementioned substrate and the Picoprobe Model 10 by GGB Industries, Inc. This calibration is essential to cancel out any parasitic effect from the setup (wires, probes etc.) for S-Parameter measurements.

4.1.2 Dominant *s*-parameters for measurement and analysis

Before starting any measurements of *s*-parameters it is important to analyse the expression of h_{21} in function to the *s*-parameters for a network of two-ports [32].

$$h_{21} = -\frac{2S_{21}\sqrt{R_{01}R_{02}}}{(1-S_{11})(Z_{02}^{*}+S_{22}Z_{02})+(S_{12}S_{21}Z_{02})} \tag{4.5}$$

Where, Z_{01} and Z_{02} are the normalizing impedance of source and load respectively, in which *s*-parameters are calculated or measured; * representes the complex conjugate of Z; finaly R_{01} and R_{02} represent the real part of Z_{01} and Z_{02} respectively.

Since in both source and load sides the normalized impedance that is used is 50 Ω (pure real impedance), the Eq. (4.5) simplifies into:

$$h_{21} = -\frac{2S_{21}}{(1-S_{11})(1+S_{22})+(S_{12}S_{21})} \tag{4.6}$$

To further simplify Eq. (4.6) it is necessary to understand how each *s*-parameter will contribute in the equation. In Fig. 4.4 it is shown the equivalent circuit to measure S_{11} and S_{21}; for S_{22} and S_{12} it is just necessary to change the position of Z_0 from one port to another.

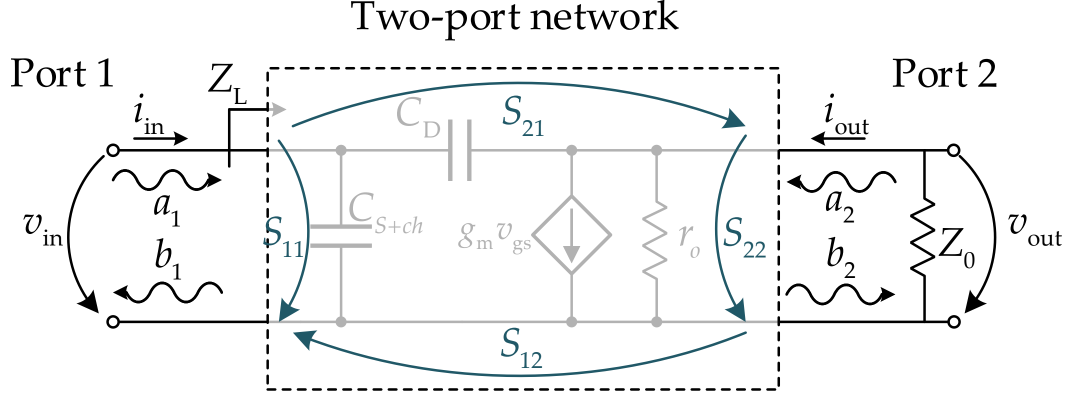


Figure 4.4: Equivalent circuit for S_{11} and S_{21} measurements.

The a_1 and a_2 represent the normalized incedent voltages, and b_1 and b_2 the normalized reflected voltages, these are defined as

$$\begin{bmatrix} a_1 & a_2 \\ b_1 & b_2 \end{bmatrix} = \begin{bmatrix} \frac{V_{in}+Z_0 I_{in}}{2\sqrt{Z_0}} & \frac{V_{out}+Z_0(-I_{out})}{2\sqrt{Z_0}} \\ \frac{V_{in}-Z_0 I_{in}}{2\sqrt{Z_0}} & \frac{V_{out}-Z_0(-I_{out})}{2\sqrt{Z_0}} \end{bmatrix} \tag{4.7}$$

The s-parameters matrix in respect to the normalized voltages is given by

$$\boldsymbol{S} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{b_1}{a_1}\Big|_{a_2=0} & \frac{b_1}{a_2}\Big|_{a_1=0} \\ \frac{b_2}{a_1}\Big|_{a_2=0} & \frac{b_2}{a_2}\Big|_{a_1=0} \end{bmatrix} \tag{4.8}$$

Using Eq. (4.7) in Eq. (4.8) it is possible to solve S_{11} and S_{22} with only terms of impedance, where Z_L is the correspondent impedance for $S_{xx}(S_{11};S_{22})$.

$$S_{xx} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4.9}$$

From the earlier DC model, if we analyse Fig. 3.7 and Fig. 3.8 it is possible to say that the TFTs on study are very resistive devices when compared to MOSFET, and this is also true for the general case of TFTs. As TFTs are normally biased from a few volts to 20 V this will generate currents of a few μA (at saturation), which corresponds to 100 kΩ or even MΩ level resistances. This fact results in S_{11} and S_{22} values to be near 1, as Z_L is much larger then Z_0.

One could argue that at higher frequencies the impedance of the capacitive elements will drop drastically, however for the frequency range of concern, that is before the cut-off frequency, this effect is not so drastic and so the assumption ($Z_L \gg Z_0$) remains correct for the working frequency range.

As illustrated in Fig. 4.4, the S_{11} and S_{22} represent the ratios between the reflected and incident electromagnetic power wave, for their respective ports. Since these reflection coefficients are near to 1, most of the energy from the wave is reflected back rather then transmitted from one port to another. Thus, the transmission coefficients given by S_{21} and S_{12} must be close to 0.

With the s-parameters briefly analysed we can now go back to Eq. (4.6) and try to see how the weight of each parameter will influence. The major complexity comes from the denominator since both terms $(1-S_{11})(1+S_{22})$ and $S_{12}S_{21}$ are close to 0. To try to find out which one is more relevant it is done the following:

$$\begin{cases} T_1 = (1-(1-\Delta_{11}))\cdot(1+(1-\Delta_{22})) \\ T_2 = \Delta_{12}\Delta_{21} \end{cases}$$

Where Δ represent a quantity that is close to 0. If now one assumes that the different Δs are all the same then the terms simplify into:

$$\begin{cases} T_1 = 2\Delta - \Delta^2 \\ T_2 = \Delta^2 \end{cases} \tag{4.10}$$

From here it is possible to conclude that the first term of the denominator will dominate over the second ($2\Delta \gg \Delta^2$). Hence, another observation that can be done is $(1+S_{22}) \approx 2$ and so the final simplification for Eq. (4.6) is

$$|h_{21}| \approx \left|\frac{S_{21}}{(1-S_{11})}\right| \tag{4.11}$$

This demonstrates that most relevant s-parameters for TFT modelling are S_{21} and S_{11}.

4.2 *S*-Parameters

In this section it is analysed S_{11} and S_{21}.

4.2.1 S_{11} theoretical analysis

First, it is necessary to calculate the theoretical expression that gives S_{11} for the CMOS model adapted to TFT. This is easily achieved through Eq. (4.9), where the most complicated part is finding Z_L. For this it is considered the following circuit present in Fig. 4.5

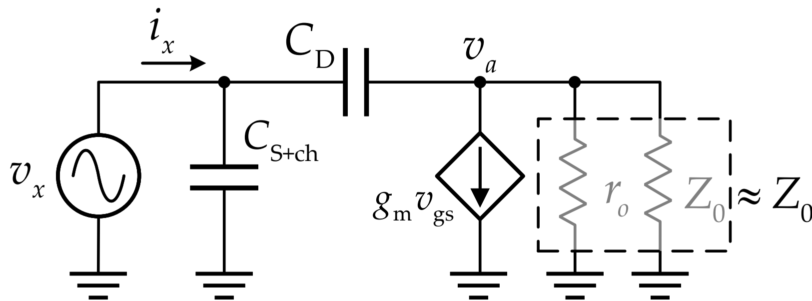


Figure 4.5: Equivalent circuit to obtain Z_L for S_{11} expression.

By applying Kirchhoff's current law (KCL) to the nodes x and a, we get the following equations

$$\begin{cases} i_x = v_x\,(sC_{\text{S+ch}}) + (v_x - v_a)sC_{\text{D}} \\ (v_x - v_a)\,sC_{\text{D}} = g_{\text{m}}v_x + g_0 v_a \end{cases} \tag{4.12}$$

Here the equations are written in terms of conductance to visually look simpler, furthermore it is done an approximation for $r_{\text{o}}//Z_0$ to Z_0. This is particularly possible in the TFT case, where the device is naturally very resistive. For example, the drain output resistance $(r_{\text{o}})^*$ is ideally ∞ and for the real device is on the MΩ level. In the other spectrum Z_0 is just 50 Ω, and therefore the conductance g_0 dominates over $1/r_{\text{o}}$.

Now, by solving Eq. (4.12) in respect to $\frac{v_x}{i_x} = Z_L$ we get

$$Z_{\text{L}} = \left[sC_{\text{S+ch}} + sC_{\text{D}} + \frac{sC_{\text{D}}\,(g_{\text{m}} - sC_{\text{D}})}{g_0 + sC_{\text{D}}} \right]^{-1} \tag{4.13}$$

Finally, by substituting Eq. (4.13) in Eq. (4.9) we get the expression of S_{11} for the CMOS model adapted to TFT.

$$S_{11} = -\frac{-{g_{\text{o}}}^2 + C_{\text{S+ch}}\,g_{\text{o}}\,s + C_{\text{S+ch}}\,C_{\text{D}}\,s^2 + C_{\text{D}}\,g_{\text{m}}\,s}{{g_{\text{o}}}^2 + C_{\text{S+ch}}\,g_{\text{o}}\,s + C_{\text{D}}\,g_{\text{m}}\,s + 2\,C_{\text{D}}\,g_{\text{o}}\,s + C_{\text{S+ch}}\,C_{\text{D}}\,s^2} \tag{4.14}$$

4.2.2 S_{21} theoretical analysis

In order to figure out the equation that describes the S_{21} for the MOSFET model adapted to TFT, it is considered the Eq. (4.7) and Eq. (4.8). From here we get the following

$$S_{21} = \frac{b_2}{a_1} = \frac{V_{\text{out}} - (-I_{\text{out}}Z_0)}{V_{\text{in}} + I_{\text{in}}Z_0} = \frac{2V_{\text{out}}}{I_{\text{in}}\,(Z_{\text{L}} + Z_0)} \tag{4.15}$$

By looking at this result, one can notice that the difficult part is to express the quotient of $V_{\text{out}}/I_{\text{in}}$, since Z_{L} is already determined in Eq. (4.13). Observing the Eq. system (4.12), the second equation can be solved in order to v_a which is the same as V_{out} and $v_x = V_{\text{in}}$.

$$V_{\text{out}} = V_{\text{in}} \cdot \frac{sC_{\text{D}} - g_{\text{m}}}{g_0 + sC_{\text{D}}} \tag{4.16}$$

Now, by dividing both terms with I_{in} we get the following

$$\frac{V_{\text{out}}}{I_{\text{in}}} = Z_{\text{L}} \cdot \frac{sC_{\text{D}} - g_{\text{m}}}{g_0 + sC_{\text{D}}} \tag{4.17}$$

Finally, by substituting Eq. (4.17) in Eq. (4.15) with the result for Z_{L} from Eq. (4.13), we have

$$S_{21} = -\frac{2\,g_{\text{o}}\,(g_{\text{m}} - C_{\text{D}}\,s)}{{g_{\text{o}}}^2 + C_{\text{S+ch}}\,g_{\text{o}}\,s + C_{\text{D}}\,g_{\text{m}}\,s + 2\,C_{\text{D}}\,g_{\text{o}}\,s + C_{\text{S+ch}}\,C_{\text{D}}\,s^2} \tag{4.18}$$

*this is given by the operation of the transistor in the saturation region and it should not to be confused with the channel resistance, which is a different thing [33]

4.3 Model validation

4.3.1 Pre requirements

In order to attain the theoretical values of the s-parameters it is necessary to measure some variables. Analysing (4.14) and (4.18), we find that C_{S+ch}, C_D and g_m are still unknown.

For the first two, C-V measurement are done in Keithley 4200. It is considered the same transistors with W/L ratios of 160 μm/20 μm and 320 μm/20 μm, for later comparison purpose. A capacitance-voltage unit (CVU) voltage sweep is performed from -1 V to 10 V with 0.1 V increments, the frequency used is 10 kHz and a small AC signal is applied of 30 mV. The C-V characteristics for one of the devices can be found in Fig. 4.6.

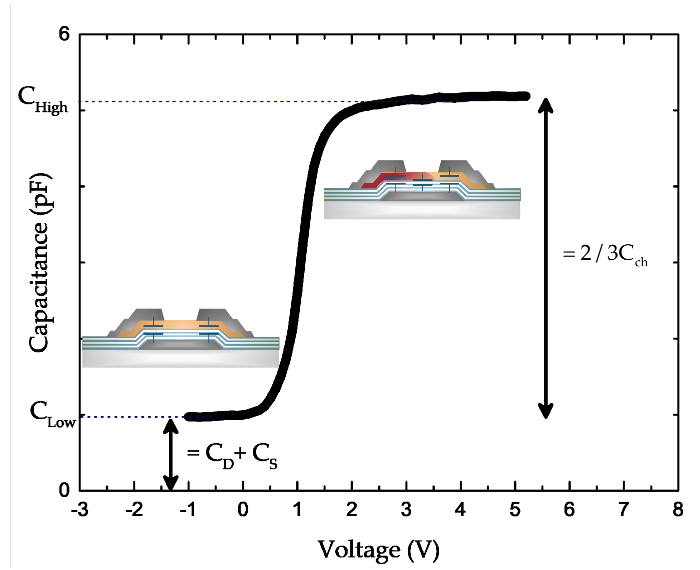


Figure 4.6: C-V characteristics for 320 μm/20 μm TFT

If we now Consider a symmetrical device both overlap capacitance will equal so:

$$C_S = C_D = \frac{C_{low}}{2} \tag{4.19}$$

After the pitch-off condition (at saturation) the channel capacitance is given by:

$$\frac{2}{3}C_{ch} = \left(C_{high} - C_{low}\right) \tag{4.20}$$

With the capacitance determined it was time to find the value for g_m. This value can be found from the first derivative of $\left(\frac{dI_D}{dV_{GS}}\right)$ at saturation condition. Another alternative much efficient and used in this project, is to considering equation 4.18. At very low frequency it will simplify into:

$$\lim_{s \to 0} S_{21} = -\frac{2g_m}{g_0} \tag{4.21}$$

The values obtained for the devices in study for this section is summarized in Tab. 4.1.

Table 4.1: Extracted values for s-parameters representation

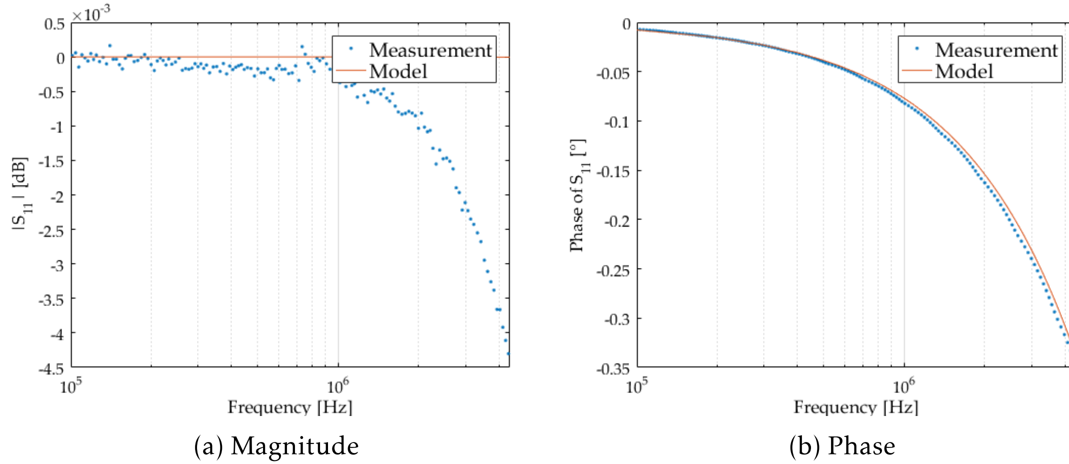
Transistor (W/L)	C_S (F)	C_{ch} (F)	g_m Ω^{-1}
320/20	4.91×10^{-13}	2.92×10^{-12}	8.91×10^{-5}
160/20	3.82×10^{-13}	1.14×10^{-12}	4.55×10^{-5}

From the observation of this table, the overlap capacitance (C_S) between the smaller and the larger device is not proportional to 0.5. If we discard the channel width variations, one possible explanation could be attributed to the ratio of overlap between drain/gate or source/gate which must be higher at the smaller device leading to a higher overlap capacitance.

4.3.2 Model representation

Having all relevant s-parameters measured and obtained the values for their representation. It was finally possible to compare both.

Starting with S_{11}, the following Fig.4.7 is obtained for the transistor with W/L = 160/20. Due to similar behaviour the other device is presented on Appendix C.



(a) Magnitude

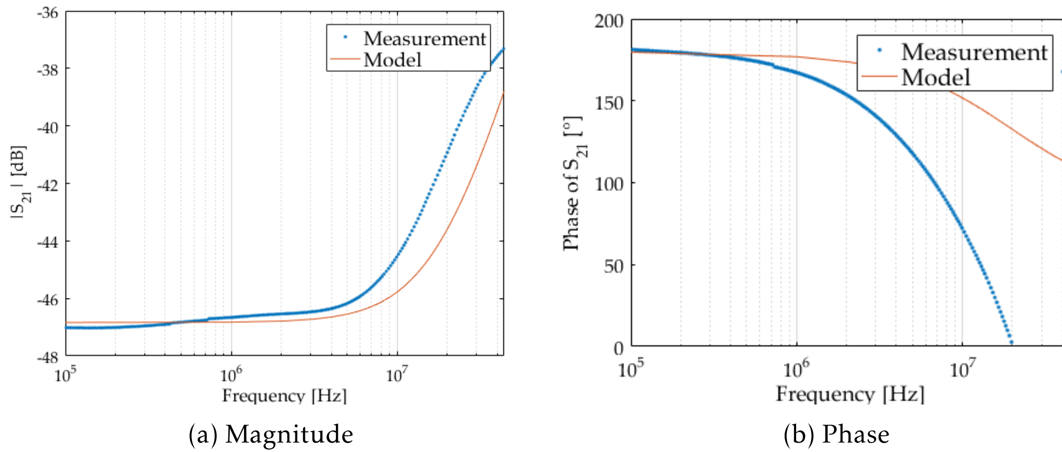
(b) Phase

Figure 4.7: Magnitude and phase measurement and simulation for S_{11} for TFT with W/L= 160/20.

From 4.14, it is suggested that the model has 2 zeros and 2 poles. From the calculation of both it was obtained 2 zeros at -6.2×10^{10} Hz and -6.2×10^{10} Hz; 2 poles at -6.6×10^{10} Hz and -9.1×10^{10} Hz. As zeros and poles are very far from the range of frequency of concern, the modelled value for S_{11} make sense in remaining at 0 dB. Since the measured S_{11} drops much earlier it suggests either the poles and zeros happen earlier or there has to be an extra pole and zero at earlier frequencies.

The next parameter for comparison is S_{21} (Fig. 4.8).

From the analytical expression for S_{21} Eq. (4.18), the model suggest to have 2 poles and 1 zero. The calculations point that the poles are located at -6.6×10^{10} Hz and -9.0×10^{9}



(a) Magnitude (b) Phase

Figure 4.8: Magnitude and phase measurement and simulation for S_{21} for TFT with W/L= 160/20.

Hz and the zero at 1.2×10^8 Hz. This time the measurement suggest the existence of a dominant zero earlier.

The last plot that is done is the $|h_{21}|$ based on Eq. (4.11). As discussed earlier this parameter directly reflects the short-circuit current gain. In practice, with the measured S_{11} and S_{21} the current gain is calculated and the f_T is the frequency at 0 dB. The measurement results of f_T and the simulation ones are shown in Fig. 4.9.

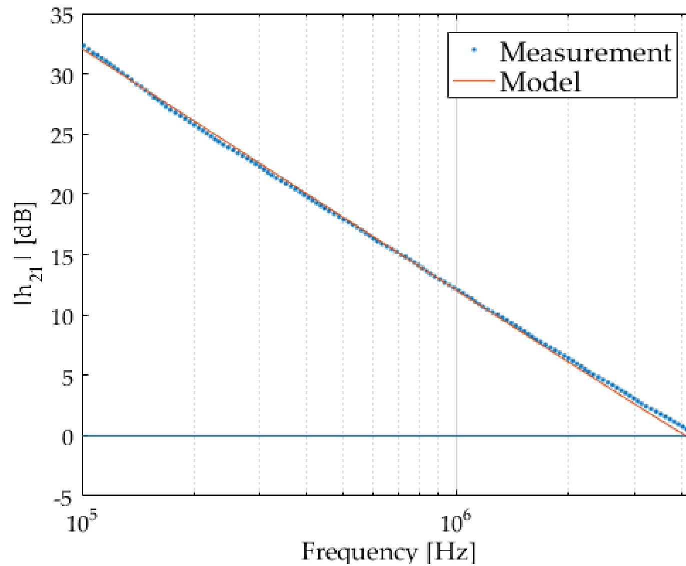


Figure 4.9: h_{21} simulation and measurement results for f_T determination.

Despite the earlier discrepancy observed the h_{21} results are quite satisfactory, in fact the f_T predicted by the model is 4.11 MHz and the measured is 4.41 MHz. The relative error is of 6.8%. One could hypothesis that for this to happen, in the earlier s-parameter measurement both S_{21} and S_{11} could have an extra pole and zero that now cancels out

since one term is divided by the other. From [24], a more complete model for TFT small signal is presented, which accounts for the V_{T} shift and R_{DS}. The major difference is that the contact resistance at the source side comes in-between the parallel of C_{ch} and C_{S}. This could be one possible reason for the discrepancy observed in the s-parameters. However the accuracy offered from this model comes at the cost of a much more complex s-parameters analysis.

This results are in agreement with the ones found in [34] where a different method is used to extract f_{T} on similar devices and the reported value is around 5 MHz.

In short the MOSFET model for small signals is capable of predicting f_T under 10% error with relatively simple equations, for the devices in study.

5 Conclusions and future prospectives

This thesis summarizes the work towards the development of compact models for IGZO-TFT with multilayer dielectric. The main goal of this project was to develop models for these devices and others with similar structure so it could empower new users to the circuit design world. For this different tasks were set:

- **Static modelling** Development of a static model, based on existent compact models for accurate and simple representation of linear characteristics as saturation.
- **Dynamic modelling** Study of the viability of MOSFET model for small-signals for the devices in study, based on A_i and f_T measurement and simulated values.

On the first task, twelve devices were studied from a single substrate of corning glass with IGZO-TFTs. Minimal amount of I-V characteristics are performed to extract most of the parameters with good accuracy (most of parameters are extracted from a single I-V measurement at linear region). Furthermore the developed model for linear region only requires 5 physical parameters (K, L_{eff}, V_{T}, α and R_{DS}) for an accurate representation ($r^2 = 0.97$). However the complete model only have numerical solutions and the discrepancy observed on the values of V_{T} might present as problems for the general application of the model. This discrepancies are most possibly due to variation in the fabrication process itself since it is not observed any clear tendency with W/L and typically short channel effects, that one could suspect to influence V_{T}, only appear at much smaller L. The output characteristics which includes the conduction in the saturation region was possible to model trough a technique of harmonic averaging between the V_{DS} and $V_{\mathrm{GS}} - V_{\mathrm{T}}$ values. Nonetheless the constant m required for this method is attained empirically which may not be generalizable for any device in that technology.

To complement the static model, a small signal model was studied. From the static model study the contact resistance was considered low ($R_{\mathrm{DS}}W = 5.794 \pm 1.477$ Ωcm), while other similar devices are in the orders of kΩ). In that manner a simple MOSFET based model was studied. The main focus was to figure out a method that could validate or negate the usage of a MOSFET based small-signal model for the devices in study. The common field was found though the measurement and modelling of h_{21} parameter. During the study it was theorised that the relevant s-parameters for analysis where just two of them S_{11} and S_{21} due to the resistive nature of TFTs, in comparison to MOSFET. From this study it was concluded that the small signal model used is capable of finding the unit gain cut-off frequency (f_{T}) under the 10% error margin.

Although both models, static and dynamic have promising accuracy and low number of parameters to be extracted, only with a working circuit achieved through these models can confirm the applicability of the same. One important aspect that is not accounted

when developing a model for a single device is the effect that neighbour elements have (eg. parasitic elements that form with the electrical connection of different transistors). The next step would be to try to implement these models in Verilog-A or SPICE and simulate a circuit that works in above-threshold regime. Later the same circuit would have to be fabricated for comparison.

The results presented in this thesis can be seen as an initial step for compact modelling for IGZO-TFTs with multilayer high-κ dielectric which may also have potential application in other similar structured devices.

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Appendix

A

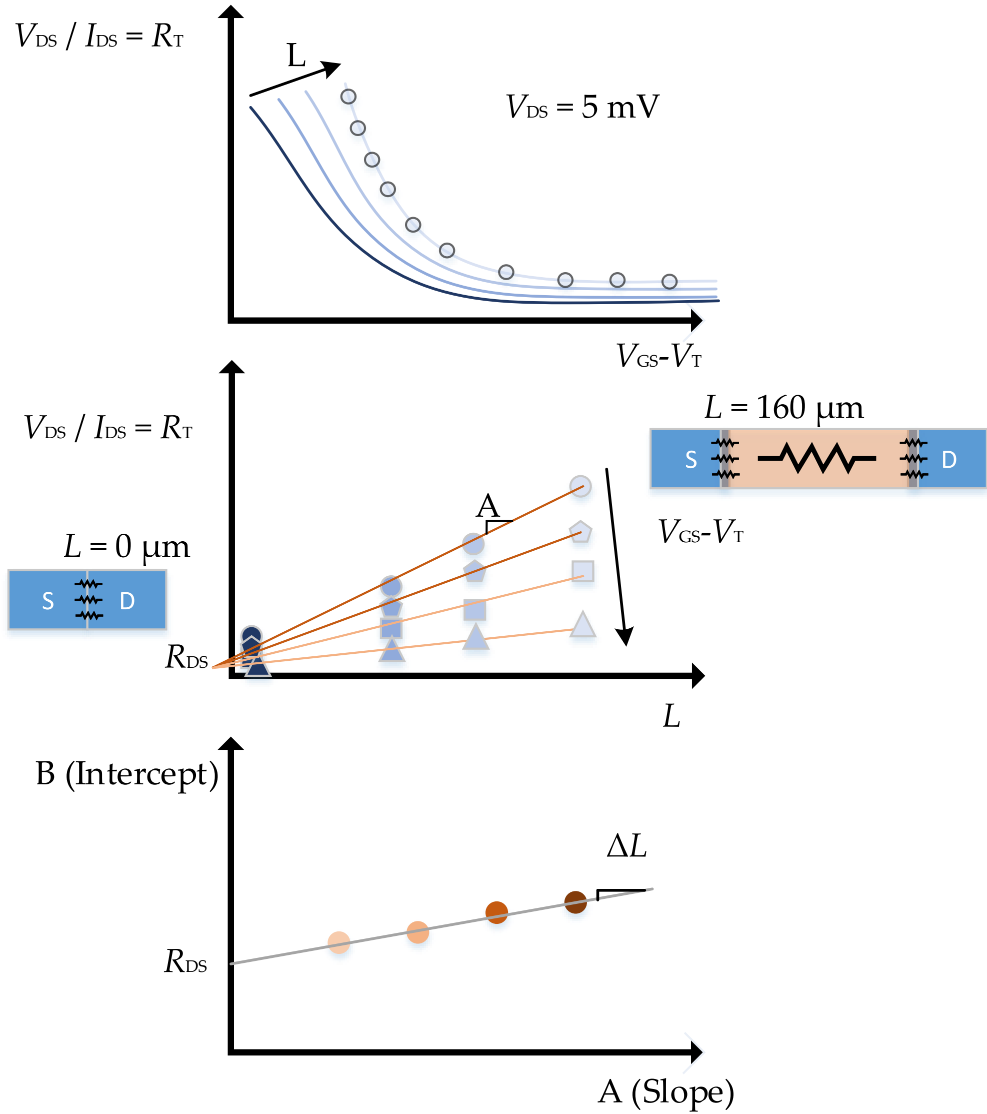


Figure A.1: Illustrative procedure for R_{DS} extraction used in this work.

Appendix B

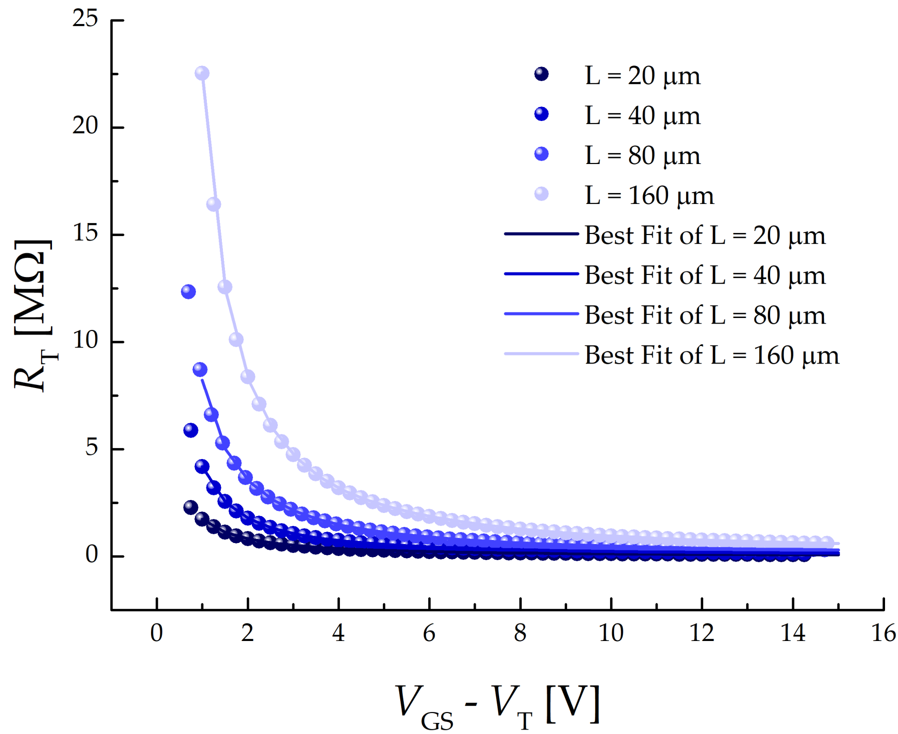


Figure B.1: R_T vs $V_{GS} - V_T$, for different *Ls*.In order to produce an arbitrary value of $V_{GS} - V_T$ for later plots. The best fit option is used to create a mathematical function that can return any value of R_T given a $V_{GS} - V_T$. The function generated is based on exponential decay of 3rd order.

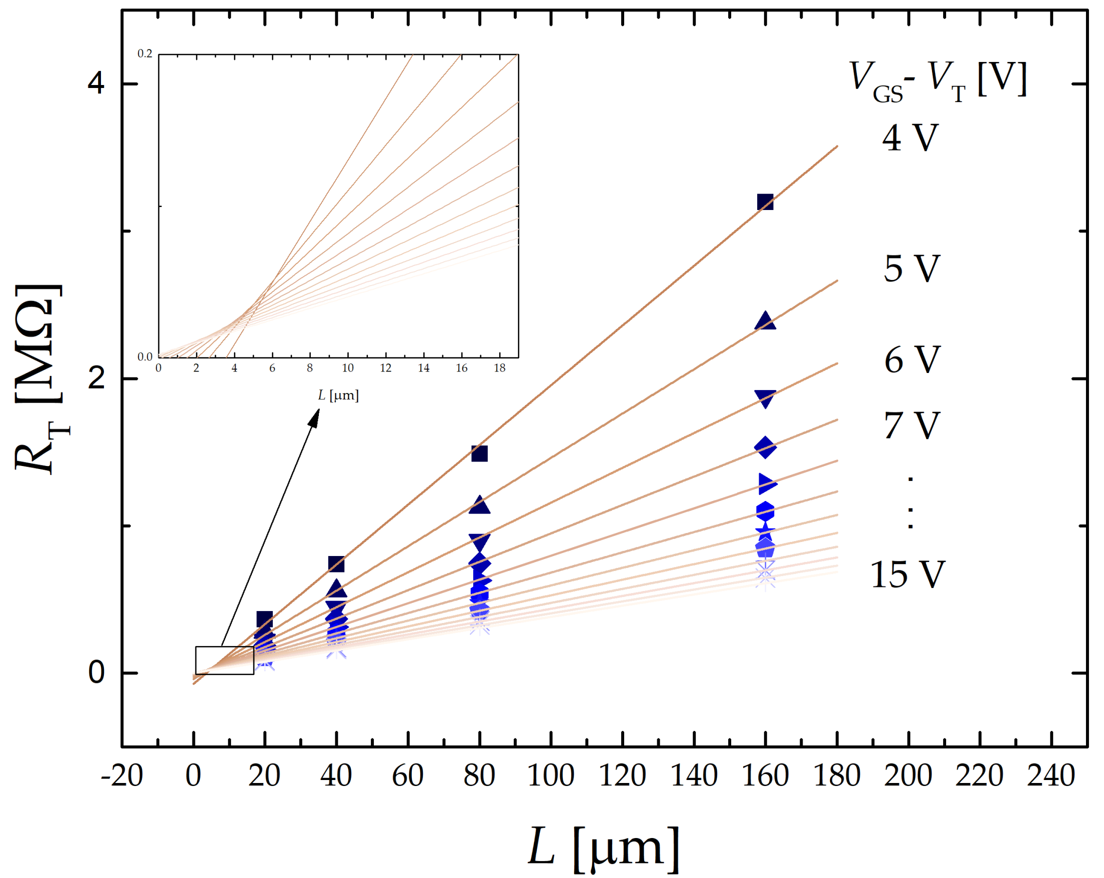
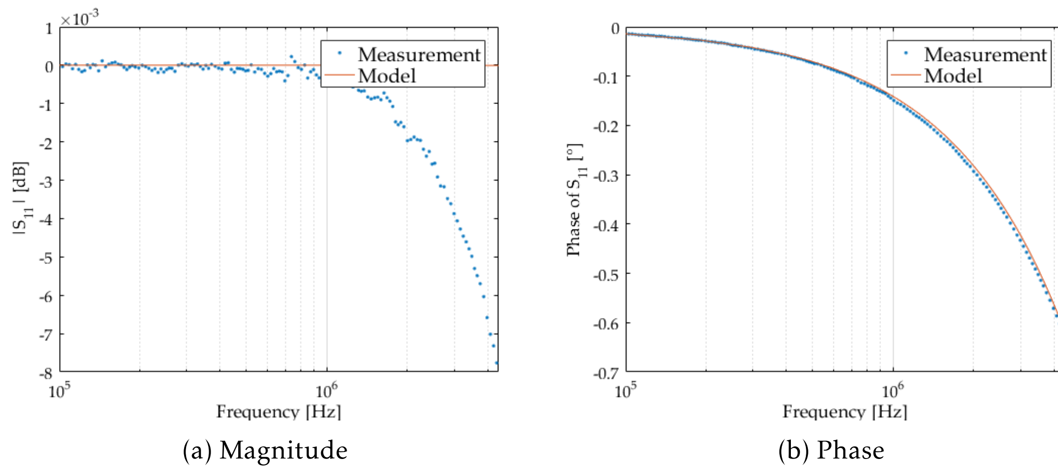


Figure B.2: R_T vs L for different $V_{GS} - V_T$. As we can see the from the amplification near the intersect, makes hard to extract L_{eff} and R_{DS}.

Appendix

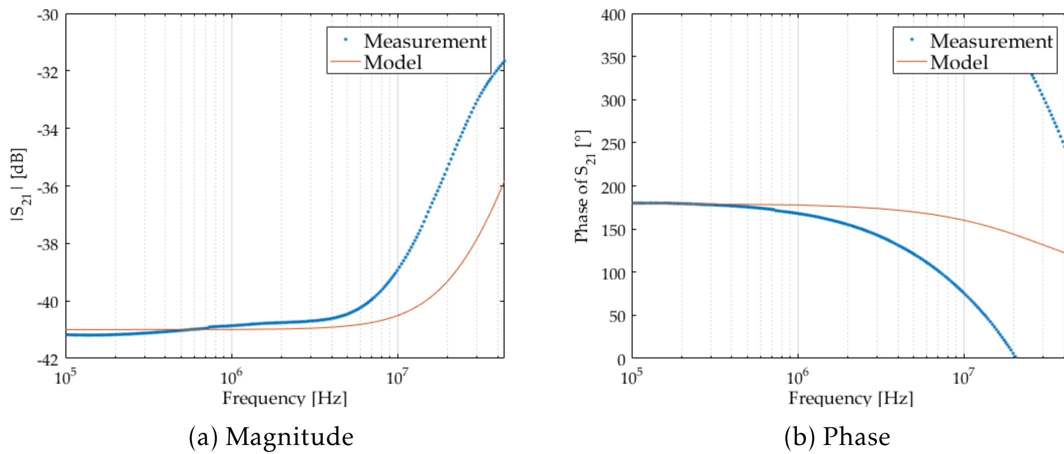
C

S-parameters measurement for $W/L = 320/20$ device.



(a) Magnitude (b) Phase

Figure C.1: Magnitude and phase measurement and simulation for S_{11} for TFT with W/L= 320/20.



(a) Magnitude (b) Phase

Figure C.2: Magnitude and phase measurement and simulation for S_{21} for TFT with W/L= 320/20.

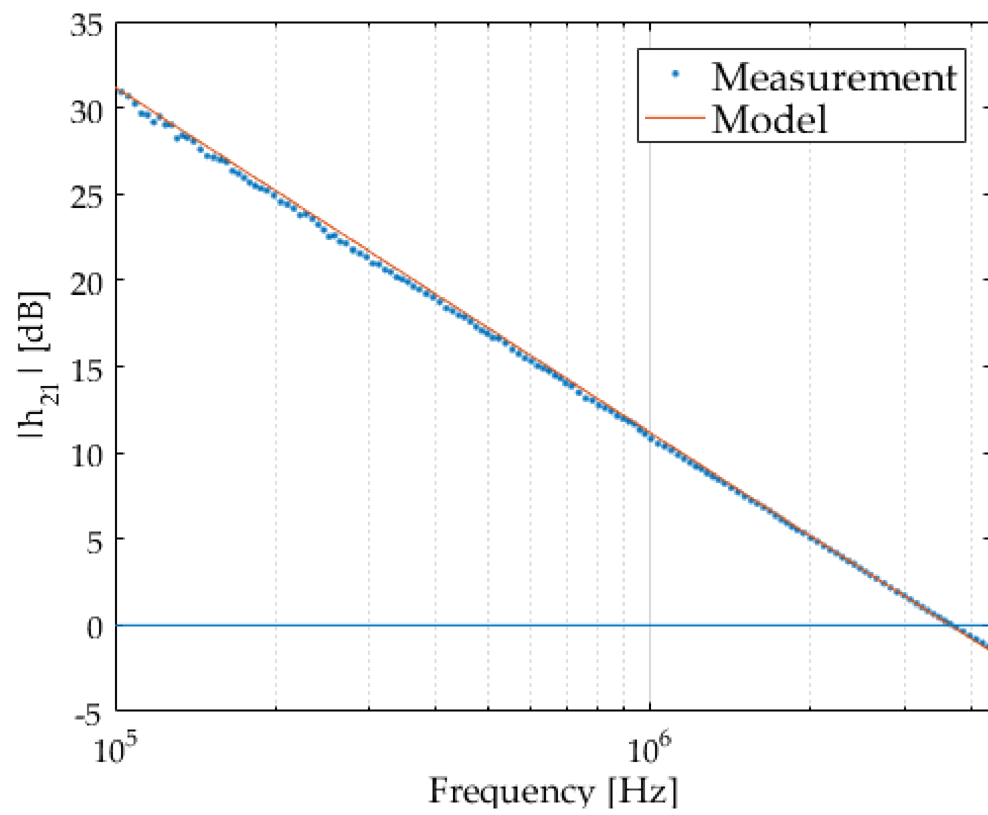


Figure C.3: h_{21} simulation and measurement results for f_T determination, for TFT with W/L= 320/20.