Ricardo Jorge Barros Fitas

Licenciado em Ciências da
Engenharia Eletrotécnica e de Computadores

Study of a Time Assisted SAR ADC

Dissertação para obtenção do Grau de Mestre em

Engenharia Electrotécnica e de Computadores

Orientador: Nuno Filipe Silva Veríssimo Paulino, Prof. Doutor,
Universidade Nova de Lisboa

Júri

Presidente: Prof. Doutor Paulo da Costa Luís da Fonseca Pinto, FCT-UNL
Arguente: Prof. Doutor João Carlos da Palma Goes, FCT-UNL
Vogal: Prof. Doutor Nuno Filipe Silva Veríssimo Paulino, FCT-UNL

FACULDADE DE
CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

Abril, 2017

Study of a Time Assisted SAR ADC

Acknowledgements

First of all, I would like to start thanking Prof. Nuno Paulino for his support, commitment, patience and motivation to find new approaches to problems which kept emerging. I would also like to show my gratitude to all the other Professors at DEE FCT-UNL who, despite not having the resources most of them would like and deserve to have, do their best on a daily basis to pass their knowledge and experience.

My friends and colleagues cannot be forgotten. Many interesting discussions and moments of fun and laughter were certainly some of the best I had so far.

Last, but not least, I thank my parents, brother, sister and grandparents, for all the caring, support and encouragement to do more and well through the entire length of my academic path. And to Andreia, who has been with me for the past three years, present for the good and the bad, for all her love and support and for keeping me going when I thought I couldn't do more.

Abstract

The demand for low power systems has been increasing in recent years and Analog-to-Digital Converters (ADCs) are key blocks of many of these systems as they convert a physical quantity into the digital domain so that this information can be further processed or stored using digital techniques.

Data Converters based on Charge Redistribution using of Successive Approximation Registers (SAR) are becoming one of the most popular ADC architectures for moderate speed, medium resolution and low power applications. Due to their low analog complexity SAR ADCs benefit from technology scaling. However, this scaling often comes with a supply voltage reduction and the noise levels do not decrease at the same rate, which translates into a performance decrease. Therefore, new opportunities emerge to explore other physical quantities such as time, frequency, phase or charge in the circuit.

This thesis focuses on studying how the time domain information can be used to increase the performance of SAR ADCs. To do so, a new SAR ADC architecture is proposed in which a Time-to-Digital Converter (TDC) is used to convert the time domain information, provided by the comparator, into the digital domain. This new architecture was modelled in MATLAB as a 12 bit TDC assisted SAR ADC, using information from electrical simulations of the comparator and the TDC, designed in Cadence in 65 nm ST Microelectronics CMOS technology.

Simulation results demonstrated that, to achieve a better performance when compared to more traditional SAR structures, the TDC energy and latency should be minimized. Another limiting factor was the large voltage range in which only 1 bit could be extracted from the time-to-voltage conversion by the TDC due to the comparator's fast response in this range. The proposed architecture was also extended to incorporate a *Bypass Window* in the time domain, which allowed to substantially decrease the number of clock cycles necessary to solve the 12 bits of the ADC.

Keywords: Analog-to-Digital Converter, Successive Approximation Register, Time-to-Digital Converter, Low power, Time, Bypass Window.

Resumo

A procura por sistemas de baixa potência tem vindo a aumentar e os Conversores Analógico-Digitais (ADCs) são blocos-chave de muitos desses sistemas, dado que convertem uma quantidade física para o domínio digital, para que essa informação possa ser processada digitalmente.

Os conversores baseados em Redistribuição de Carga, utilizando Registos de Aproximações Sucessivas (SAR), estão a aumentar a sua popularidade, sendo uma das arquiteturas mais populares atualmente. Devido à sua baixa complexidade analógica, os conversores SAR beneficiam do escalamento da tecnologia que vem muitas vezes associado a uma redução da tensão de alimentação, e tendo em conta que os níveis de ruído não diminuem na mesma medida, isto traduz-se numa diminuição do desempenho. Deste modo, surgem novas oportunidades para explorar outras quantidades físicas, como tempo, frequência, fase ou carga nos circuitos.

Esta tese tem como objetivo o estudo de como a informação no domínio do tempo pode ser utilizada para aumentar o desempenho dos conversores SAR. Para isso, é proposta uma nova arquitetura de um ADC, na qual um Conversor Tempo-para-Digital (TDC) é usado para converter a informação do domínio do tempo, fornecida pelo comparador, para o domínio digital. Esta nova arquitetura foi modelada em MATLAB como um SAR ADC de 12 bits assistido por um TDC, utilizando resultados de simulação de circuitos projetados na tecnologia CMOS 65 nm da ST Microelectronics.

Os resultados da simulação demonstraram que, para se obter um melhor desempenho quando comparado com estruturas SAR mais tradicionais, a energia e a latência do TDC devem ser minimizadas. Outro fator limitador é a grande gama de tensão na qual somente 1 bit pode ser extraído da conversão de tempo para tensão pelo TDC devido à rápida resposta do comparador nesta gama. A arquitetura proposta foi, ainda, modificada de modo a incorporar uma janela de *Bypass* o que permitiu diminuir substancialmente o número de ciclos de relógio necessários para resolver os 12 bits do ADC.

Palavras-chave: Conversor Analógico-Digital, Registo de Aproximações Sucessivas, Conversor Tempo-para-Digital, Baixa potência, Tempo, Janela de *Bypass*.

Contents

List of Figures

List of Tables

Acronyms

ADC Analog-to-Digital Converter.

CR Charge Redistribution.

CS Charge Sharing.

DAC Digital-to-Analog Converter.

DNL Differential Non-Linearity.

ELD Early-Late Detector.

INL Integral Non-Linearity.

LSB Least Significant Bit.

MCS Merged Capacitor Switching.

MSB Most Significant Bit.

SAR Successive Approximation Register.

SNR Signal-to-Noise Ratio.

TDC Time-to-Digital Converter.

Chapter 1

Introduction

1.1 Motivation and Background

The need for low power devices has been increasing in recent years. This trend is still continuing as the need for portability is increasing, as well as the need for newer implantable medical devices [1], hence long battery life is becoming a requirement for today's electronic systems. Analog-to-Digital Converters (ADC) are key blocks of these systems as they sample a physical quantity and convert into the digital domain so that this information can be further processed or stored using digital techniques.

Successive Approximation Register (SAR) ADCs, based on Charge Redistribution (CR) on weighted capacitors [2] techniques, have arisen among other ADC architectures for moderate speed, medium-resolution [3] and very low-power applications, while keeping analog simplicity [1]. The traditional SAR structure, shown in Figure 1.1, consists of a sample-and-hold circuit embedded in the DAC, a comparator, a digital-to-analog converter (DAC) and a control logic block which implements the binary search algorithm. This binary search algorithm requires N clock cycles for a N-bit SAR ADC. This translates into N comparator decisions which are a major source of power consumption in SAR ADCs and the bottleneck for SAR's throughput. Additionally, power in the capacitive arrays, in the case of a capacitive DAC, is wasted if the signal does not fall within the desired range. This is because the switching energy of the DACs is proportional to CV^2, hence keeping the unit capacitors small is important to keep the power consumption low. However, using very small unit capacitors degrades the matching between capacitors which will degrade the non-linearity parameters of ADCs, namely Integral Non-Linearity (INL) and Differential Non-Linearity (DNL). This means that the size of the unit capacitor must be chosen by making a trade-off between the $\frac{kT}{C}$ noise requirements, capacitor matching and power consumption [4]. Due to the low complexity of its analog blocks and being

mainly constituted by digital circuits, SAR ADCs benefit from technology scaling, hence a better performance is expected in terms both speed of operation and power consumption because the parasitics are decreased [1]. Moreover, since no complex analog circuitry such as operational amplifiers are used in SAR ADCs and no large voltage swings are required, unlike in other ADC architectures, SAR ADCs are more suitable to operate at low supply voltages, which also contributes to its low-power operation [5].

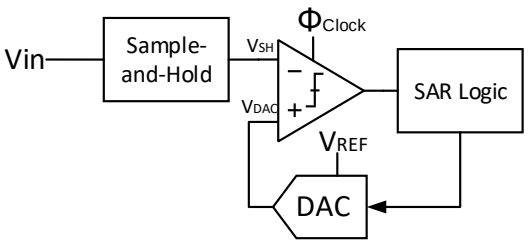


Figure 1.1: Conventional SAR ADC Architecture.

However, with the technology scaling and the supply voltage reduction, the design of analog circuits in CMOS technologies is becoming more challenging, as keeping the transistors working in saturation and still maintaining a sufficient signal swing becomes critical, while the noise levels do not go down with decreasing supply voltage. This translates into a direct decrease of the Signal-to-Noise Ratio (SNR) which will severely reduce the performance of the ADCs. That being said, new opportunities arise for using new physical quantities such as time, charge, phase or frequency instead of traditional quantities such as voltage and current in the circuits. In this sense, and bearing in mind that digital circuits benefit from technology scaling [6], it is interesting to study how these domains can be used to increase the performance of ADCs.

1.2 Original Contributions

The main purpose of this thesis is to study how the time domain information can be used to assist the commonly used successive approximation algorithm in SAR ADCs in order to achieve a better performance.

Considering the SAR ADC architecture, the time a comparator takes to perform a decision is directly related with its input signals. This means that extra information can be extracted if this time is measured using, for example, a Time-to-Digital Converter (TDC) [7]. By measuring the time at which the comparator output changes and using this information to select the DAC code in the SAR structure closer to the final ADC output code, several bits can be decided at once, hence power is saved both in the number of comparator decisions needed and in the DAC switching because no wrong steps are made in the bits decided by the TDC. Moreover, since several bits are decided at once, it is also possible to increase SAR's throughput [8]. By using such architecture, it is expected

that the performance of the system increases with technology scaling since most of the complexity is transferred to the digital domain. For this reason, the proposed circuits will be developed in a 65nm ST Microelectronics CMOS Technology and their characteristics included in the MATLAB high-level models of the proposed converter.

Since very low-power ADCs are crucial for implantable medical devices, this structure intends to be an alternative to the ADCs used nowadays for this applications.

1.3 Thesis Organization

This thesis is organized in 6 chapters, starting with this introductory one. Chapter 2 explores the fundamentals of Analog-to-Digital conversion, both in time and frequency domains. These concepts are critical when designing data converters since they limit the $\frac{F_{in}}{F_s}$ ratio, therefore frequency spacing between spectral components, and the in-band quantization noise.

The third chapter presents the principles behind SAR ADCs. The successive approximation algorithm is explained and the function of each circuit block is discussed. For each block, non-idealities are presented and circuit techniques to overcome such problems are proposed. The power consumption of these constituting blocks is studied in detail in order to improve the performance of these converters. Two different DAC switching schemes, which implement the successive approximation algorithm, are analysed in detail. Also, a comparison among these and other switching methods is made. Finally, recent SAR ADCs operating outside their traditional application spaces or with different architectures are briefly presented.

Time-to-Digital Converters are key components to convert the time domain information into the digital domain. In this sense, Chapter 4 focuses on the fundamentals of these converters, architectures and how to obtain sub-gate resolution in TDC circuits.

In Chapter 5, the proposed architecture, in which a TDC is introduced into the traditional SAR ADC architecture, is presented and explained. High-level MATLAB models of the proposed converter and the circuits implemented in 65 nm CMOS ST Microelectronics, along with electrical and system level simulations, can also be found in this chapter.

Finally, the last chapter presents the conclusions and proposes work to be further developed.

CHAPTER 2

Analog-to-Digital Conversion Fundamentals

The signal conversion (in ADCs) corresponds to the transformation of a analog input signal into a digital output signal. However, an analog signal has an infinite number of values in a finite time interval. As result, it is necessary to periodically sample the input signal. After the signal is sampled, it is then quantized so that a finite (digital) value can be assigned to the sampled signal and the analog to digital conversion is finished. The conversion procedure is then repeated until enough data is collected to perform the action demanded by the target application. It is also important to refer that the conversion algorithm depends on the converter's architecture, which is not the subject of this chapter. Instead, this chapter focuses in understanding the conversion process at a system level, as shown in Figure 2.1. Therefore, a brief mathematical approach to the sampling and quantization theories will be presented. Finally, some useful metrics to characterize converters will be presented.

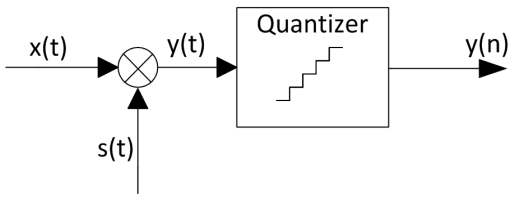


Figure 2.1: Ideal mathematical model of the Analog-to-Digital conversion process.

2.1 Sampling

Sampling is the procedure of transforming a time-continuous signal, $x(t)$[1], into a time-discrete signal. The sampling function, $s(t)$, is a sequence of *dirac* pulses equally separated by a time period T_s, defined as $T_s = \frac{1}{F_s}$, where F_s is the sampling frequency, therefore $s(t)$ can be written as Eq. 2.1. In this sense, the sampled signal, $y(t)$, can be defined as Eq. 2.2, [3]. Figure 2.2 is representative of the sampling process in the time domain.

$$s(t) = \sum_{n=-\infty}^{+\infty} \delta(t - nT_s) \tag{2.1}$$

$$y(t) = x(t) \cdot s(t) = \sum_{n=-\infty}^{+\infty} x(t - nT_s) \tag{2.2}$$

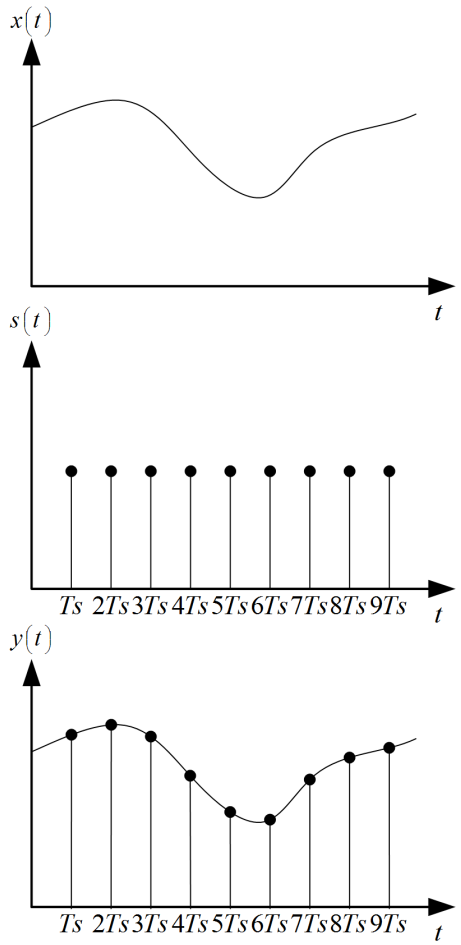


Figure 2.2: Sampling process in the time domain.

In order to analyse the impact of this operation in the frequency domain, Eq. 2.1 can be transformed into Eq. 2.3 by taking its Fourier Transform. Since Eq. 2.1 represents

[1] x(t) is assumed to be a band limited signal with a bandwidth from f = 0 Hz to f = BW Hz.

a periodic pulsed signal in the time domain, its Fourier Transform is simply a periodic pulsed signal in the frequency.

$$S(j\omega) = \frac{2\pi}{T_s} \sum_{k=-\infty}^{+\infty} \delta\left(j\omega - jk\frac{2\pi}{T_s}\right) \tag{2.3}$$

In the frequency domain, Eq. 2.2 can be rewritten as Eq. 2.4 since a multiplication in the time domain is evaluated as a convolution in the frequency domain [9]. The sampling mechanism in the frequency domain is illustrated in Figure 2.3.

$$Y(j\omega) = \frac{1}{2\pi} X(j\omega) \otimes S(j\omega) = \frac{1}{Ts} \sum_{k=-\infty}^{+\infty} X\left(j\omega - jk\frac{2\pi}{T_s}\right) \tag{2.4}$$

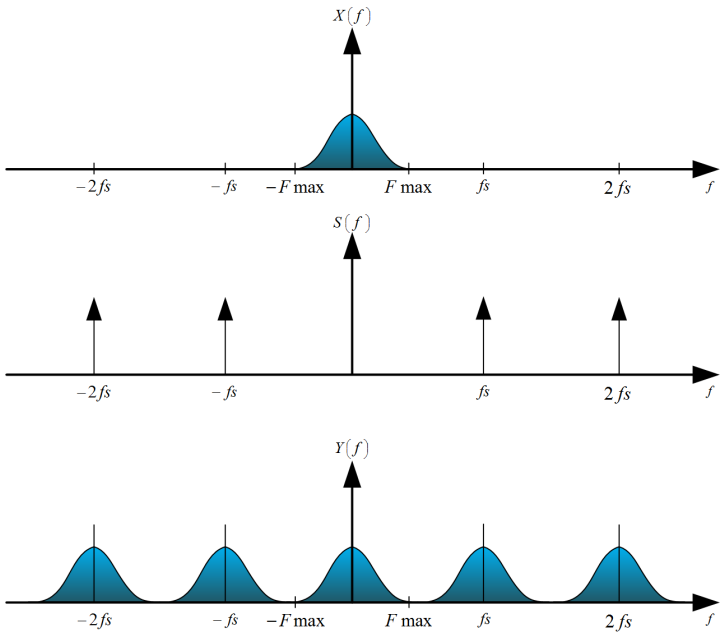


Figure 2.3: Sampling process in the frequency domain.

By observing the frequency spectrum of $Y(j\omega)$ in Figure 2.3, it is evident what Eq. 2.2 and Eq. 2.4 state: by sampling a signal with a train of *dirac* pulses equally separated by a time period T_s, an infinite number of replicas of the original signal spectrum ($X(j\omega)$) is created in the frequency spectrum, these *images* of the sampled signal centred at multiples of F_s [3, 9], as shown in the frequency spectrum of $Y(j\omega)$ in Figure 2.3.

As a consequence of this phenomenon, if the time difference between two adjacent samples, i.e. T_s, is too high, the spectral components of the sampled signal $Y(j\omega)$ will overlap. This phenomenon is known as *aliasing* and it is shown in Figure 2.4. The *aliasing* effect produces a mixing of sampled data in the frequency domain and the original signal can no longer be recovered. Hence, in order to avoid it, the *Nyquist-Shannon Criterion* must be respected [3].

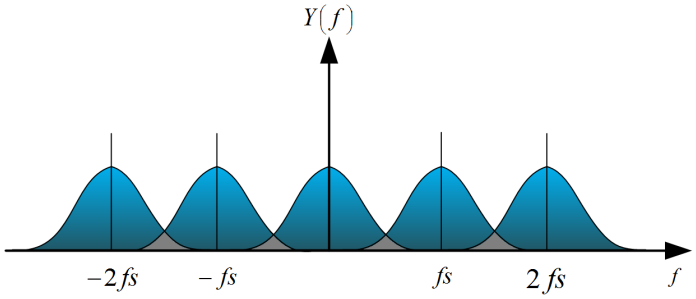


Figure 2.4: Aliasing effect.

2.1.1 Nyquist-Shannon Criterion

The *Nyquist-Shannon Criterion* was formulated in 1923 by Harry Nyquist [10] and extended in 1948-49 by Claude Shannon [11, 12] and states: a sampled signal can be recovered with no loss of information if the sampling frequency F_s is, at least, two times higher than the maximum signal frequency BW [3, 9]. The sampling frequency which satisfies this condition is known as the Nyquist Frequency, f_N, and is defined as Eq. 2.5.

$$F_s = f_N = 2 \cdot BW \tag{2.5}$$

In order to clean the frequency spectrum so that only the baseband component is present, a low pass filter is used. According to what was previously demonstrated, the larger the sampling frequency the more separated are the spectral components, thus the more relaxed are the low pass filter requirements [3].

It is also worth mentioning that ADCs which work close to the Nyquist Frequency are known as the *Nyquist Converters*. Another family of ADCs, which work at much higher frequencies than f_N are called *Oversampling Converters* but these are out of the purpose of this thesis.

2.2 Quantization

After the analog signal has been sampled, next step in the analog to digital conversion process is the quantization of the signal's physical quantity so that a digital value can be assigned to that sample. The digital representation of the signal depends on the number of bits N at the output, as well as on the full scale range FS of the quantizer. Knowing these two parameters, it is possible to define the value of the *Least Significant Bit* (LSB), Δ, as Eq. 2.6.

$$\Delta = \frac{FS}{2^N} \tag{2.6}$$

In Figure 2.5 the characteristic of an ideal quantizer is presented for an ideal 3 bit quantizer, corresponding each step size to one Δ. According to this characteristic, all input values will be encoded to the corresponding output code.

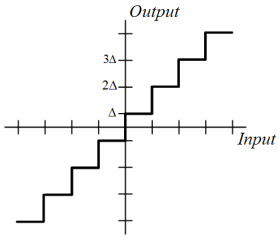


Figure 2.5: Ideal Quantizer characteristic.

However, since Δ is not infinitely small (since the number of bits N is not infinite), there will always be some error introduced by the quantization process, the *Quantization Error*, *qe*. From Figure 2.5, it is possible to observe that the quantization error depends on the input signal and has a maximum error of $\left|\frac{\Delta}{2}\right|$. Nevertheless, if it is assumed that the input signal is rapidly changing such that q_e is considered a random variable uniformly distributed between $\pm\frac{\Delta}{2}$, the probability density function of the quantization error in this range is also assumed to be constant and uniformly distributed. Under these conditions, the quantization error can be treated as white noise [3, 9]. Thus, the *Quantization Noise* power can be calculated from Eq. 2.8 P_{q_e} in the *Nyquist Bandwidth*.

$$P_{q_e} = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} q_e^2 \, dq_e = \frac{\Delta^2}{12} \tag{2.7}$$

If F_s is higher than that in the conditions of Eq. 2.5, Eq. 2.7 can be extended to Eq. 2.8.

$$P_{q_e} = \frac{\Delta^2}{12} \cdot \frac{2BW}{F_s} \tag{2.8}$$

According to Eq. 2.8, the quantization noise power can be reduced, in the signal bandwidth, both by increasing the quantizer's resolution and increasing the sampling frequency [3]. While increasing the quantizer's resolution decreases the quantization error, hence it's power, increasing F_s will result in the quantization noise power being spread through a wider frequency range, therefore its effect becomes smaller inside the band of interest, as shown in Figure 2.6.

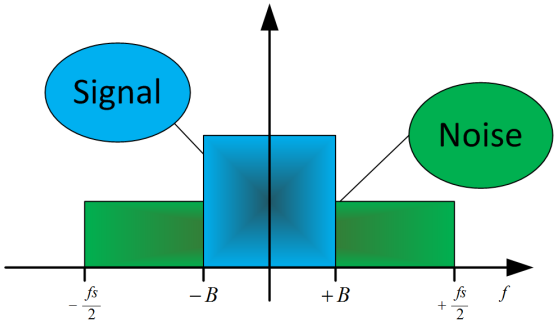


Figure 2.6: Frequency Spectrum

2.3 Performance Metrics

The performance of every data converter is generally categorized according to several metrics, both dynamic and static. This section intends to summarize these metrics.

The *Signal-to-Noise Ratio* (SNR) stands for the ratio of the input signal power to the quantization noise power. The SNR can be further extended to incorporate the power of all the unwanted frequency components. In this case, it should be named *Signal-to-Noise-and-Distortion Ratio* (SNDR).

Having a large SNDR usually translates into large a *Effective Number of Bits* (ENOB) and large *Total Harmonic Distortion* (THD). The THD is defined as the ratio of the sum of the power of all the signal harmonics higher than the first to the power of the first harmonic. These harmonics usually limit the *Spurious Free Dynamic Range* (SFDR), since it is a metric of the distance between the signal and the largest unwanted frequency component. Another important parameter when categorizing data converters is the *Dynamic Range* (DR), which defines the range of signal amplitudes in which the converter is able to operate. It is limited by the thermal noise, at low signal amplitudes, and by distortion and jitter, at higher signal amplitudes. These are dynamic performance metrics as they relate to the frequency behaviour of the converter.

The *Differential Non-Linearity* (DNL) and *Integral Non-Linearity* (INL) are linearity measures which specify the converter's step difference from an ideal LSB size and its input-output deviation from an ideal conversion curve, respectively. These are static metrics since they are obtained by slowly sweeping the converter's input over its full-scale range.

The *Walden Figure of Merit* (FoM) is a performance metric useful when comparing different data converters and it is formulated in Eq. 2.9. It takes into account the amount of power the converter needs to achieve a certain performance, expressed by the *Effective Number of Bits*, over a certain input signal frequency bandwidth, *BW*. The Figure of Merit is expressed in units of *joules per conversion step*, hence the lower FoM obtained, the better the converter's performance.

$$FoM = \frac{Power}{2^{ENOB} \times 2BW} \tag{2.9}$$

CHAPTER 3

ANALYSIS OF SAR ADCs

The popularity of SAR ADCs has been increasing throughout the last years for moderate-speed, medium-resolution [3] mainly due to their exceptional energy-efficiency [13]. This is accomplished because their analog complexity is kept low, hence SAR ADCs benefit from technology scaling [1, 14]. In this sense, the present chapter aims to study the principle of operation of this ADCs and to explore different SAR architectures reported in the literature.

3.1 SAR ADC Block Diagram

The conventional SAR ADC architecture is depicted in Figure 3.1. It comprises a sample-and-hold circuit, a comparator, a DAC and control logic block [2] that implements the successive approximation algorithm.

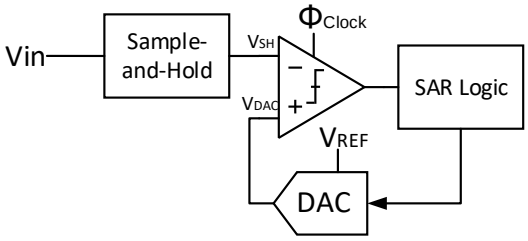


Figure 3.1: Conventional SAR Architecture with Sample-and-Hold Circuit - single ended.

The first step towards a full conversion in this kind of ADCs is sampling the input signal using the sample-and-hold circuit, V_{SH}. Afterwards, the control logic block tries to approximate the voltage produced by the feedback DAC, V_{DAC}, to V_{SH} by controlling

the DAC data input bits, one at a time, starting from the Most Significant Bit (MSB) and moving towards the LSB. Once all the bits are decided, the conversion is finished. The approximation method implemented by the control logic block is based on a binary search algorithm, known as the *Successive Approximation Algorithm* [3].

3.1.1 Successive Approximation Algorithm

The Successive Approximation Algorithm implemented by the control logic block is represented in the flow diagram of Figure 3.2 for an N-bit SAR ADC. In the beginning, all the feedback DAC data input bits (b_{N-1} *to* b_0) are set to ZERO. Then, the control logic block sets the MSB (b_{N-1}) of the DAC to ONE and the digital word is converted into V_{DAC}. Afterwards, the comparator present in the SAR ADC architecture evaluates if V_{DAC} is greater than V_{SH}. If that is the case, b_{N-1} is set back to ZERO, otherwise it is kept at ONE. This process is repeated until all bits are determined. According to this, a N-bit SAR ADC requires $N+1$ clock cycles to perform a full conversion [3].

3.1.2 SAR ADC Sub-Blocks

Each block in the SAR structure has a very specific function and its implementation strongly affects the performance of the converter. Therefore, this section intends to provide an overview of their implementation and present some design tradeoffs.

3.1.2.1 Sample-And-Hold

Ideally, this block should be able to acquire a sample of the signal without any interference. However, since this circuits generally consist of a switch and a capacitor to hold the sampled value, both components can affect the sampled signal.

The sampling capacitor, C_{hold}, for example, will also sample some noise along with the signal. For this reason, the sampling capacitor size should be chosen so that it respects the noise requirements, $\frac{kT}{C_{hold}}$. However, a big capacitor translates into large time constants [3].

The switch implementation should also be as linear as possible, which is not achievable by using only one transistor. Such a simple implementation presents a R_{ON} which varies with the input signal value, thus introducing distortion [3]. *Transmission gates* are often used to decrease the effective R_{ON} by using $NMOS$ and $PMOS$ devices in parallel and the signal related distortion effect can be overtaken by using techniques such as *bootstrapping* [15].

Moreover, *Charge Injection* effects occur due to the ON/OFF operation of the switching procedure. Half of the charge in the channel of the MOS switches during the OFF transition will be absorbed by C_{hold}. Likewise, MOS transistors absorb charge to be turned on. Again, the charge stored in C_{hold} will be modified and the sampled signal value altered. In order to compensate this, *dummy switches* can be used [3].

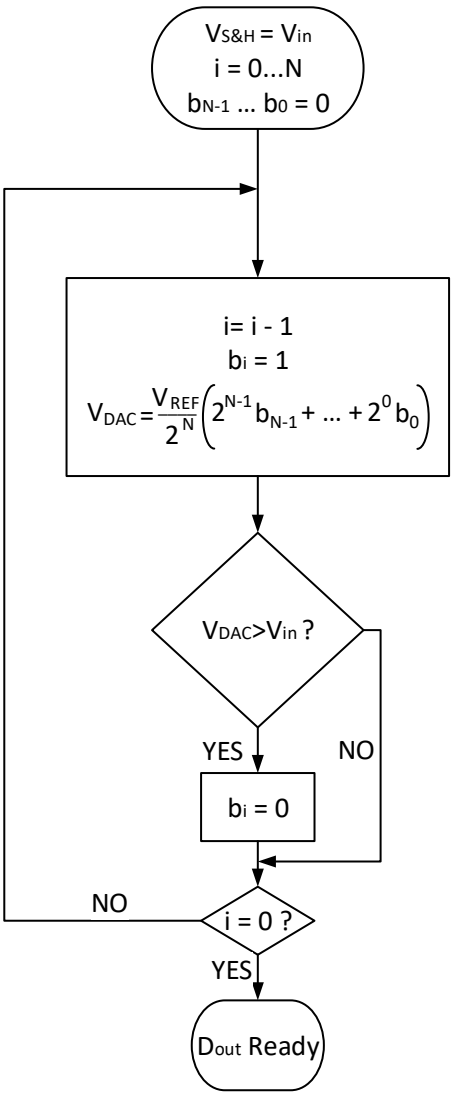


Figure 3.2: Flow Diagram of the Successive Approximation Algorithm.

The resulting circuit is no longer a simple circuit constituted by a switch and a capacitor. Also, using all these circuit techniques can translate into a large power consumption [3]. However, in Charge Redistribution SAR ADCs, the Sample-and-Hold function can be embedded in the (capacitive) DAC, therefore resulting in a much more energy-efficient solution [2, 14, 16].

3.1.2.2 Comparator

The comparator is the only active block in a SAR ADC. It compares the sampled signal V_{SH} with the DAC voltage V_{DAC} and its decision is used by the SAR Control Logic to perform the successive approximation algorithm [3].

Accuracy and *speed* are important parameters for the comparator as it should be able to

resolve very small voltage differences, at least $V_{LSB}/2$, within a reasonable amount of time. Since the comparator's decision time is directly related to the signals under comparison, this time domain information can be used to extract information from the amplitude domain [7], as will be done in this work.

Besides accuracy and speed, *kickback noise* and *offset* should also be taken into account. While *offset* is only translated in a deviation in the ADC's conversion curve, hence does not degrade the linearity metrics of the ADC (DNL and INL), *kickback noise* may cause a wrong decision by the comparator if its amplitude is too high. Therefore, comparator architectures in which the output stage is separated from the input stage are preferred since it helps both in decreasing the kickback and the input referred offset [3, 17].

3.1.2.3 SAR Control Logic

This block is responsible for implementing the binary search algorithm described in 3.1.1. More advanced switching algorithms allow to save power related to DAC switching and this is a subject under study in this work. This block, besides demanding some power to operate at reasonable speeds, benefits from technology scaling since it is mainly constituted by digital circuits.

3.1.2.4 Digital-to-Analog Converter

In SAR ADCs, the feedback DAC is used to produce a voltage as close as possible to the input voltage and it can be considered the most important block in a SAR ADCs since, together with the Sample-and-Hold circuit, the feedback DAC determines the overall linearity of the converter [3]. Moreover, the DAC *settling time* plays an important role in determining the maximum conversion speed. Nevertheless, enough time should be given so that V_{DAC} settles within half LSB [16]. If the comparator starts making a decision before the DAC is fully settled, a wrong decision may occur, hence the final output code will be incorrect if no correction methods are used [1].

Several types of DACs can be used in SAR ADCs, however charge domain DACs are the most suitable for low-power SAR ADCs due to their zero static power consumption [3, 4]. Moreover, capacitive DACs based on charge redistribution can provide inherent Sample-and-Hold function, as previously mentioned. Charge Sharing (CS) DACs are an alternative to Charge Redistribution architectures. Depending on its structure, CS DACs can be more energy-efficient than CR based DACs, however they need an auxiliary sampling capacitor and the performance reported in recent works does not match that possible with CR DACs [18]. For this reasons, emphasis will be given to DACs operating in the charge domain using charge redistribution schemes .

Considering a capacitive DAC, the power consumption depends on the switching method employed and the total capacitance of the capacitive array, hence keeping the unit capacitors small is important to keep the power consumption low. However, decreasing the value of the unit size capacitor degrades the matching between capacitors, which will

have a direct impact in the converter's linearity. Also, the $\frac{kT}{C}$ noise requirements should be respected. This means that the unit size capacitor must be chosen by making a tradeoff between power consumption, capacitor matching and noise requirements [3, 4].

3.2 SAR ADCs Power

Charge Redistribution SAR ADCs are capable of achieving very high energy-efficiency [13, 16], being most of the energy consumed by the comparator, the DAC switching and the digital circuits in the Control Logic block [14].

The comparator power depends on the number of comparisons performed, which increases with the resolution of the ADC, thus the comparator power can not be reduced without reducing the number of comparisons necessary.

As mentioned before, digital circuits benefit from technology scaling [6] so, in order to increase SAR ADCs energy-efficiency even more, more advanced DAC structures, namely *Capacitive Array with Attenuation Capacitor* [19] and *Split Capacitor Array* [20], and switching algorithms such as the *Energy Saving* [21], *Monotonic* [22, 14], *Merged Capacitor Switching (MCS)* [23] or *Vcm-based* [16], or *Tri-Level* [24] must be used. Table 3.1 summarizes the DAC switching schemes, according to [18].

Table 3.1: Comparison of DAC switching schemes for 10 bit SAR ADCs considering the Conventional switching method as the reference.

	Energy	Common Mode Voltage	Sensitivity to comparator offset	DAC capacitance
Conventional	1	Constant	Low	1
Monotonic	0.1874	Varying	High	0.5
Vcm-based (MCS)	0.1248	Constant	Low	0.5
Tri-Level	0.0311	Varying	High	0.25

3.3 SAR ADCs Switching Schemes

Several Switching schemes were developed throughout the last years in order to minimize the energy required by the DAC transitions. In this thesis, only the fully differential implementation of the Conventional and the MCS schemes will be explored in detail, since the other switching methods lead to a variation of the common-mode voltage, hence can not be used in the architecture proposed in Chapter 5.

It should be mentioned that fully differential implementations provide common mode rejection and present a better noise performance.

3.3.1 Conventional Switching Scheme

The Conventional Switching scheme, proposed in [2], is based on the trial and error algorithm presented in 3.1.1. Figure 3.3 depicts a conventional 3 bit fully differential SAR ADC structure. Since this ADC is fully differential, only the positive side of the ADC operation will be described, as the operation on the other side is complementary.

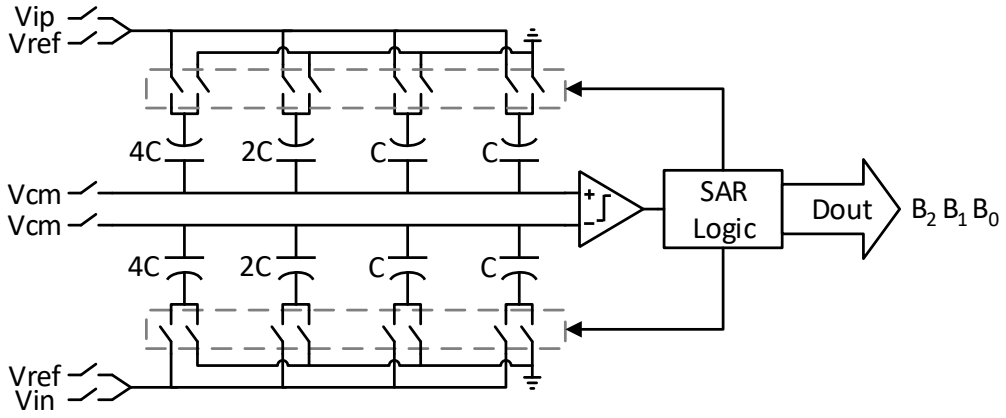


Figure 3.3: Conventional 3 bit SAR ADC architecture - differential circuit schematic.

The conversion starts with the sampling phase, ϕ_S. At the sampling phase, the bottom plates of the capacitor network are connected to V_{ip} and the top plates are connected to the common mode voltage, V_{cm}. Next, the bottom plate of the MSB capacitor is switched to the reference voltage, V_{ref}, and the bottom plates of the other capacitors on the positive DAC array switched to ground, gnd. On the negative array, the complementary operation is done. At the same time, the top plates of the capacitive network are disconnected from V_{cm}. After the DACs output voltages are settled, the comparator performs the first decision. In case $V_{ip} > V_{in}$, the MSB, B_2, is 1 and the MSB capacitor is left unchanged. Otherwise, B_2 is 0 and the MSB capacitor is switched to gnd. After the MSB is decided, the MSB-1 capacitor is connected to V_{ref} and the cycle goes on until the LSB, B_0 is determined, hence the conversion finished [2, 14]. Figure 3.4 shows all possible conversion steps for this ADC, including the switching energy per each step. The letters on top of every conversion step will be used in the next section to ease the reader's job following the determination of the switching energy for each conversion step.

Switching Energy

The energy drawn from the reference voltage, V_{ref}, to charge the top plate of a capacitor C from its initial state, at $t = 0$, to V_{ref}, at $t = T_f$, can be written according to Eq. 3.1, assuming the bottom plate voltage is left unchanged during this process.

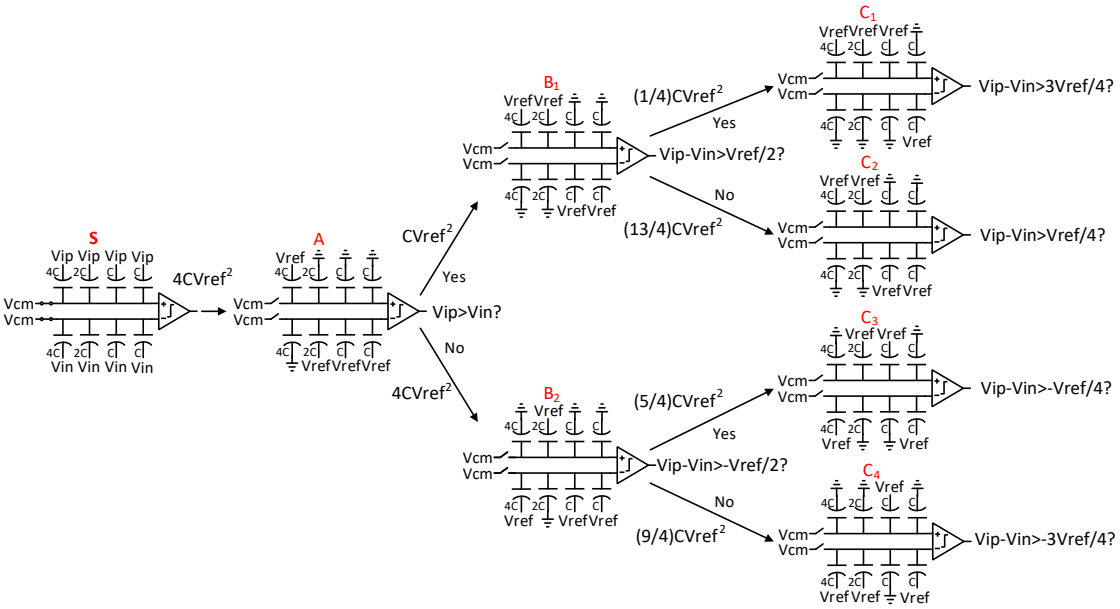


Figure 3.4: Conventional 3 bit SAR ADC switching procedure.

$$E = \int_0^{T_f} V_{ref} i_{ref}(t) dt \tag{3.1}$$

Considering that $i_{ref}(t) = -\dfrac{dQ}{dt}$ and $Q = CV$, Eq. 3.1 can be rewritten as Eq. 3.2, assuming that no more the current is drawn from V_{ref} after $t = 1$.

$$E = -V_{ref} \Delta Q = -V_{ref} (C \Delta V) \tag{3.2}$$

In order to derive the switching energy values exhibited in Figure 3.4, according to Eq. 3.2, the voltage difference between adjacent conversion steps must be calculated. To do so, charge conservation equations will be used.

Sampling Phase, ϕ_S The sampling phase is the first step of a full conversion as shown in Figure 3.4. In this case, the top plates are connected to the common-mode voltage and bottom plate sampling is used. Eq. 3.3 and Eq. 3.4 represent the charge at the top plates of both capacitor arrays during this phase.

$$Q_S^+ = 4C\left(V_{cm} - V_{ip}\right) + 2C\left(V_{cm} - V_{ip}\right) + C\left(V_{cm} - V_{ip}\right) + C\left(V_{cm} - V_{ip}\right) \tag{3.3}$$

$$Q_S^- = 4C\left(V_{cm} - V_{in}\right) + 2C\left(V_{cm} - V_{in}\right) + C\left(V_{cm} - V_{in}\right) + C\left(V_{cm} - V_{in}\right) \tag{3.4}$$

Phase A, ϕ_A After the signal has been sampled in ϕ_S, the bottom plate of the MSB capacitor is switched to V_{ref} in the positive DAC and the other capacitors in this DAC array connected to gnd. The complementary action is performed in the negative DAC. At

the same time, the top plates are disconnected from V_{cm}. This operation will force the DAC voltages to change since the charge is conserved. Eq. 3.5 and Eq. 3.6 represent the charge at the top plates of both capacitor arrays during this phase.

$$Q_A^+ = 4C\left(V_{DAC_A}^+ - V_{ref}\right) + 2C\left(V_{DAC_A}^+ - 0\right) + C\left(V_{DAC_A}^+ - 0\right) + C\left(V_{DAC_A}^+ - 0\right) \tag{3.5}$$

$$Q_A^- = 4C\left(V_{DAC_A}^- - 0\right) + 2C\left(V_{DAC_A}^- - V_{ref}\right) + C\left(V_{DAC_A}^- - V_{ref}\right) + C\left(V_{DAC_A}^- - V_{ref}\right) \tag{3.6}$$

Since the charge is conserved, by equating Q_S to Q_A, the output voltages of the DACs, V_{DAC}, are calculated in Eq. 3.7 and Eq. 3.8.

$$Q_S^+ = Q_A^+ \Leftrightarrow V_{DAC_A}^+ = V_{cm} - V_{ip} + \frac{V_{ref}}{2} \tag{3.7}$$

$$Q_S^- = Q_A^- \Leftrightarrow V_{DAC_A}^- = V_{cm} - V_{in} + \frac{V_{ref}}{2} \tag{3.8}$$

The resulting voltages are evaluated by the comparator, according to Eq. 3.9.

$$\Delta V_{DAC} > 0 \Leftrightarrow V_{DAC_A}^+ - V_{DAC_A}^- > 0 \tag{3.9}$$

The energy drawn from V_{ref}, in the transition from ϕ_S to ϕ_A, can be calculated according to Eq. 3.2. Expanding Eq. 3.2 to the present case results in Eq. 3.10 and Eq. 3.11.

$$E_A^+ = -V_{ref}\left(4C\left[\left(V_{DAC_A}^+ - V_{ref}\right) - \left(V_{cm} - V_{ip}\right)\right]\right) = 2CV_{ref}^2 \tag{3.10}$$

$$\begin{aligned} E_A^- = -V_{ref}\Bigg(2C\left[\left(V_{DAC_A}^- - V_{ref}\right) - (V_{cm} - V_{in})\right] + C\left[\left(V_{DAC_A}^- - V_{ref}\right) - (V_{cm} - V_{in})\right] \\ + C\left[\left(V_{DAC_A}^- - V_{ref}\right) - (V_{cm} - V_{in})\right]\Bigg) = 2CV_{ref}^2 \end{aligned} \tag{3.11}$$

Therefore, the total DAC energy from the sampling phase to the present phase is given by Eq. 3.12.

$$E_A = E_A^+ + E_A^- = 4CV_{ref}^2 \tag{3.12}$$

Phase B, ϕ_B Depending on the comparator's decision from Eq. 3.9, the MSB capacitor on the positive side of the DAC remains connected to V_{ref}, leading to phase B1, ϕ_{B_1}, or is switched to gnd, generating phase B2, ϕ_{B_2}. In any of the cases, the MSB-1 capacitor is connected to V_{ref}. The complementary operation is performed on the negative side of the DAC.

Phase B1, ϕ_{B_1} Due to the switching action in the bottom plates of the DAC, the top plate voltages are changed, in order to keep the total charge constant. Eq. 3.13 and Eq. 3.14 represent the charge at the top plates of both capacitor arrays during ϕ_{B_1}.

$$Q_{B_1}^{+} = 4C\left(V_{DAC_{B_1}}^{+} - V_{ref}\right) + 2C\left(V_{DAC_{B_1}}^{+} - V_{ref}\right) + C\left(V_{DAC_{B_1}}^{+} - 0\right) + C\left(V_{DAC_{B_1}}^{+} - 0\right) \quad (3.13)$$

$$Q_{B_1}^{-} = 4C\left(V_{DAC_{B_1}}^{-} - 0\right) + 2C\left(V_{DAC_{B_1}}^{-} - 0\right) + C\left(V_{DAC_{B_1}}^{-} - V_{ref}\right) + C\left(V_{DAC_{B_1}}^{-} - V_{ref}\right) \quad (3.14)$$

Due to the charge conservation, the resulting top plate voltages are expressed in Eq. 3.15 and Eq. 3.16. These voltages are evaluated by the comparator similarly to Eq. 3.9, however considering the voltages now present in the DACs.

$$Q_S^{+} = Q_{B_1}^{+} \Leftrightarrow V_{DAC_{B_1}}^{+} = V_{cm} - V_{ip} + \frac{3}{4}V_{ref} \quad (3.15)$$

$$Q_S^{-} = Q_{B_1}^{-} \Leftrightarrow V_{DAC_{B_1}}^{-} = V_{cm} - V_{in} + \frac{V_{ref}}{4} \quad (3.16)$$

The energy drawn from V_{ref}, in the transition from ϕ_A to ϕ_{B_1}, can be calculated according to Eq. 3.2. Expanding Eq. 3.2 to the present case results in Eq. 3.17 and Eq. 3.18.

$$\begin{aligned} E_{B_1}^{+} = -V_{ref}\Bigg(&4C\left[\left(V_{DAC_{B_1}}^{+} - V_{ref}\right) - \left(V_{DAC_A}^{+} - V_{ref}\right)\right] \\ &+ 2C\left[\left(V_{DAC_{B_1}}^{+} - V_{ref}\right) - \left(V_{DAC_A}^{+} - 0\right)\right]\Bigg) = \frac{1}{2}CV_{ref}^2 \end{aligned} \quad (3.17)$$

$$\begin{aligned} E_{B_1}^{-} = -V_{ref}\Bigg(&C\left[\left(V_{DAC_{B_1}}^{-} - V_{ref}\right) - \left(V_{DAC_A}^{-} - V_{ref}\right)\right] \\ &+ C\left[\left(V_{DAC_{B_1}}^{-} - V_{ref}\right) - \left(V_{DAC_A}^{-} - V_{ref}\right)\right]\Bigg) = \frac{1}{2}CV_{ref}^2 \end{aligned} \quad (3.18)$$

Therefore, the total DAC energy from the previous phase to the present phase is given by Eq. 3.19.

$$E_{B_1} = E_{B_1}^{+} + E_{B_1}^{-} = CV_{ref}^2 \quad (3.19)$$

Phase B2, ϕ_{B_2} The methodology to determine the DAC switching energy to phase B2 is similar to that used to calculate the switching energy to phase B1. Thus, Eq. 3.20 and Eq. 3.21 represent the charge at the top plates of both capacitor arrays during this phase.

$$Q_{B_2}^{+} = 4C\left(V_{DAC_{B_2}}^{+} - 0\right) + 2C\left(V_{DAC_{B_2}}^{+} - V_{ref}\right) + C\left(V_{DAC_{B_2}}^{+} - 0\right) + C\left(V_{DAC_{B_2}}^{+} - 0\right) \quad (3.20)$$

$$Q_{B_2}^- = 4C\left(V_{DAC_{B_2}}^- - V_{ref}\right) + 2C\left(V_{DAC_{B_2}}^- - 0\right) + C\left(V_{DAC_{B_2}}^- - V_{ref}\right) + C\left(V_{DAC_{B_2}}^- - V_{ref}\right) \quad (3.21)$$

Once the DACs are settled, the voltages at the top plates are derived using charge conservation equations Eq. 3.22 and Eq. 3.23.

$$Q_S^+ = Q_{B_2}^+ \Leftrightarrow V_{DAC_{B_2}}^+ = V_{cm} - V_{ip} + \frac{1}{4}V_{ref} \quad (3.22)$$

$$Q_S^- = Q_{B_2}^- \Leftrightarrow V_{DAC_{B_2}}^- = V_{cm} - V_{in} + \frac{3}{4}V_{ref} \quad (3.23)$$

The energy required to produce this voltage changes is calculated in Eq. 3.24 and Eq. 3.25. Eq. 3.26 determines the total energy required by the DAC.

$$E_{B_2}^+ = -V_{ref}\left(2C\left[\left(V_{DAC_{B_2}}^+ - V_{ref}\right) - \left(V_{DAC_A}^+ - 0\right)\right]\right) = \frac{5}{2}CV_{ref}^2 \quad (3.24)$$

$$\begin{aligned} E_{B_2}^- = -V_{ref}\Bigg(4C\left[\left(V_{DAC_{B_2}}^- - V_{ref}\right) - \left(V_{DAC_A}^- - 0\right)\right] + C\left[\left(V_{DAC_{B_2}}^- - V_{ref}\right) - \left(V_{DAC_A}^- - V_{ref}\right)\right] \\ + C\left[\left(V_{DAC_{B_2}}^- - V_{ref}\right) - \left(V_{DAC_A}^- - V_{ref}\right)\right]\Bigg) = \frac{5}{2}CV_{ref}^2 \end{aligned} \quad (3.25)$$

$$E_{B_2} = E_{B_2}^+ + E_{B_2}^- = 5CV_{ref}^2 \quad (3.26)$$

Phase C, ϕ_C The LSB is determined in the last phase of the conversion, which corresponds to phase *C* in the 3 bit conventional SAR ADC depicted in Figure 3.4. Again, the conversion path depends on the previous decision of the comparator, i.e. the comparator's decision from phase B.

Phase C1, ϕ_{C_1} This phase is reached if the successive approximation algorithm has not taken wrong steps through the full conversion. As previously explained, the charge at the top plates during this phase can be expressed by Eq. 3.27 and Eq. 3.28.

$$Q_{C_1}^+ = 4C\left(V_{DAC_{C_1}}^+ - V_{ref}\right) + 2C\left(V_{DAC_{C_1}}^+ - V_{ref}\right) + C\left(V_{DAC_{C_1}}^+ - V_{ref}\right) + C\left(V_{DAC_{C_1}}^+ - 0\right) \quad (3.27)$$

$$Q_{C_1}^- = 4C\left(V_{DAC_{C_1}}^- - 0\right) + 2C\left(V_{DAC_{C_1}}^- - 0\right) + C\left(V_{DAC_{C_1}}^- - 0\right) + C\left(V_{DAC_{C_1}}^- - V_{ref}\right) \quad (3.28)$$

The charge conservation principle allow us to calculate the DACs top voltages according to Eq. 3.29 and Eq. 3.30.

$$Q_S^+ = Q_{C_1}^+ \Leftrightarrow V_{DAC_{C_1}}^+ = V_{cm} - V_{ip} + \frac{7}{8}V_{ref} \quad (3.29)$$

$$Q_S^- = Q_{C_1}^- \Leftrightarrow V_{DAC_{C_1}}^- = V_{cm} - V_{in} + \frac{1}{8}V_{ref} \tag{3.30}$$

The energy consumed in the switching action of each DAC is determined in Eq. 3.31 and Eq. 3.32. The energy consumed by both arrays is given in Eq. 3.33.

$$\begin{aligned} E_{C_1}^+ = -V_{ref}\Bigg(&4C\left[\left(V_{DAC_{C_1}}^+ - V_{ref}\right) - \left(V_{DAC_{B_1}}^+ - V_{ref}\right)\right] + \\ &2C\left[\left(V_{DAC_{C_1}}^+ - V_{ref}\right) - \left(V_{DAC_{DAC_{B_1}}}^+ - V_{ref}\right)\right] + \\ &C\left[\left(V_{DAC_{C_1}}^+ - V_{ref}\right) - \left(V_{DAC_{DAC_{B_1}}}^+ - 0\right)\right]\Bigg) = \frac{1}{8}CV_{ref}^2 \end{aligned} \tag{3.31}$$

$$E_{C_1}^- = -V_{ref}\left(C\left[\left(V_{DAC_{C_1}}^- - V_{ref}\right) - \left(V_{DAC_{B_1}}^- - V_{ref}\right)\right]\right) = \frac{1}{8}CV_{ref}^2 \tag{3.32}$$

$$E_{C_1} = E_{C_1}^+ + E_{C_1}^- = \frac{1}{4}CV_{ref}^2 \tag{3.33}$$

Phase C2, ϕ_{C_2} If the comparator's decision in phase ϕ_{B_1} is contrary, the next step in successive approximation algorithm is ϕ_{C_2}. Eq. 3.34 and Eq. 3.35 express the top plate charge for each DAC array.

$$Q_{C_2}^+ = 4C\left(V_{DAC_{C_2}}^+ - V_{ref}\right) + 2C\left(V_{DAC_{C_2}}^+ - 0\right) + C\left(V_{DAC_{C_2}}^+ - V_{ref}\right) + C\left(V_{DAC_{C_2}}^+ - 0\right) \tag{3.34}$$

$$Q_{C_2}^- = 4C\left(V_{DAC_{C_2}}^- - 0\right) + 2C\left(V_{DAC_{C_2}}^- - V_{ref}\right) + C\left(V_{DAC_{C_2}}^- - 0\right) + C\left(V_{DAC_{C_2}}^- - V_{ref}\right) \tag{3.35}$$

The DACs top voltages can be determined according to Eq. 3.36 and Eq. 3.37.

$$Q_S^+ = Q_{C_2}^+ \Leftrightarrow V_{DAC_{C_2}}^+ = V_{cm} - V_{ip} + \frac{5}{8}V_{ref} \tag{3.36}$$

$$Q_S^- = Q_{C_2}^- \Leftrightarrow V_{DAC_{C_2}}^- = V_{cm} - V_{in} + \frac{3}{8}V_{ref} \tag{3.37}$$

The energy drawn from V_{ref}, in the transition from ϕ_{B_1} to ϕ_{C_2}, is computed in Eq. 3.38 and Eq. 3.39.

$$\begin{aligned} E_{C_2}^+ = -V_{ref}\Bigg(&4C\left[\left(V_{DAC_{C_2}}^+ - V_{ref}\right) - \left(V_{DAC_{B_1}}^+ - V_{ref}\right)\right] + \\ &2C\left[\left(V_{DAC_{C_2}}^+ - 0\right) - \left(V_{DAC_{B_1}}^+ - V_{ref}\right)\right] + C\left[\left(V_{DAC_{C_2}}^+ - V_{ref}\right) - \left(V_{DAC_{B_1}}^+ - 0\right)\right]\Bigg) = \frac{13}{8}CV_{ref}^2 \end{aligned} \tag{3.38}$$

$$E_{C_2}^- = -V_{ref}\left(2C\left[\left(V_{DAC_{C_2}}^- - V_{ref}\right) - \left(V_{DAC_{B_1}}^- - 0\right)\right] + C\left[\left(V_{DAC_{C_2}}^- - V_{ref}\right) - \left(V_{DAC_{B_1}}^- - V_{ref}\right)\right]\right) = \frac{13}{8}CV_{ref}^2 \tag{3.39}$$

Therefore, the total DAC energy from ϕ_{B_1} to ϕ_{C_2} is given by Eq. 3.40.

$$E_{C_2} = E_{C_2}^+ + E_{C_2}^- = \frac{13}{4}CV_{ref}^2 \tag{3.40}$$

Phase C3, ϕ_{C_3} From ϕ_{B_2} to ϕ_{C_3}, the bottom plate voltage of the 2 MSB capacitors is modified. Therefore, the top plate voltage of the capacitor arrays changes in order to keep the total charge constant. Eq. 3.41 and Eq. 3.42 represent the charge at the top plates of both capacitive DACs during this phase.

$$Q_{C_3}^+ = 4C\left(V_{DAC_{C3}}^+ - 0\right) + 2C\left(V_{DAC_{C_3}}^+ - V_{ref}\right) + C\left(V_{DAC_{C_3}}^+ - V_{ref}\right) + C\left(V_{DAC_{C_3}}^+ - 0\right) \tag{3.41}$$

$$Q_{C_3}^- = 4C\left(V_{DAC_{C3}}^- - V_{ref}\right) + 2C\left(V_{DAC_{C_3}}^- - 0\right) + C\left(V_{DAC_{C_3}}^- - 0\right) + C\left(V_{DAC_{C_3}}^- - V_{ref}\right) \tag{3.42}$$

The resulting top plate voltages, due to the charge conservation, are expressed in Eq. 3.43 and Eq. 3.44.

$$Q_S^+ = Q_{C_3}^+ \Leftrightarrow V_{DAC_{C_3}}^+ = V_{cm} - V_{ip} + \frac{3}{8}V_{ref} \tag{3.43}$$

$$Q_S^- = Q_{C_3}^- \Leftrightarrow V_{DAC_{C_1}}^- = V_{cm} - V_{in} + \frac{5}{8}V_{ref} \tag{3.44}$$

The energy required to produce this voltages is expressed in Eq. 3.45 and Eq. 3.46. Eq. 3.47 determines the total energy required by the DAC.

$$E_{C_3}^+ = -V_{ref}\left(2C\left[\left(V_{DAC_{C_3}}^+ - V_{ref}\right) - \left(V_{DAC_{B_2}}^+ - 0\right)\right] + C\left[\left(V_{DAC_{C_3}}^+ - V_{ref}\right) - \left(V_{DAC_{B_2}}^+ - 0\right)\right]\right) = \frac{5}{8}CV_{ref}^2 \tag{3.45}$$

$$E_{C_3}^- = -V_{ref}\left(4C\left[\left(V_{DAC_{C_3}}^- - V_{ref}\right) - \left(V_{DAC_{B_2}}^- - V_{ref}\right)\right] + C\left[\left(V_{DAC_{C_3}}^- - V_{ref}\right) - \left(V_{DAC_{B_2}}^- - V_{ref}\right)\right]\right) = \frac{5}{8}CV_{ref}^2 \tag{3.46}$$

$$E_{C_3} = E_{C_3}^+ + E_{C_3}^- = \frac{5}{4}CV_{ref}^2 \tag{3.47}$$

Phase C4, ϕ_{C_4} The last phase depicted in Figure 3.4 is ϕ_{C_4}, which corresponds to all conversion steps taken in the wrong direction. Similarly to what was done before, the top plate charge for each array is expressed by Eq. 3.48 and Eq. 3.49.

$$Q^+_{C_4} = 4C\left(V^+_{DAC_{C4}} - 0\right) + 2C\left(V^+_{DAC_{C_4}} - 0\right) + C\left(V^+_{DAC_{C_4}} - V_{ref}\right) + C\left(V^+_{DAC_{C_4}} - 0\right) \tag{3.48}$$

$$Q^-_{C_4} = 4C\left(V^-_{DAC_{C4}} - V_{ref}\right) + 2C\left(V^-_{DAC_{C_4}} - V_{ref}\right) + C\left(V^-_{DAC_{C_4}} - 0\right) + C\left(V^-_{DAC_{C_4}} - V_{ref}\right) \tag{3.49}$$

The voltages at the DACs top plates are derived using the charge conservation principle in Eq. 3.50 and Eq. 3.51.

$$Q^+_S = Q^+_{C_4} \Leftrightarrow V^+_{DAC_{C_4}} = V_{cm} - V_{ip} + \frac{1}{8}V_{ref} \tag{3.50}$$

$$Q^-_S = Q^-_{C_4} \Leftrightarrow V^-_{DAC_{C_4}} = V_{cm} - V_{in} + \frac{7}{8}V_{ref} \tag{3.51}$$

The energy drawn from V_{ref}, in the transition from ϕ_{B_2} to ϕ_{C_4}, is determined in Eq. 3.52 and Eq. 3.53.

$$E^+_{C_4} = -V_{ref}\left(C\left[\left(V^+_{DAC_{C_4}} - V_{ref}\right) - \left(V^+_{DAC_{B_2}} - 0\right)\right]\right) = \frac{9}{8}CV^2_{ref} \tag{3.52}$$

$$\begin{aligned} E^-_{C_4} = -V_{ref}\Bigg(&4C\left[\left(V^-_{DAC_{C_4}} - V_{ref}\right) - \left(V^-_{DAC_{B_2}} - V_{ref}\right)\right] + \\ &2C\left[\left(V^-_{DAC_{C_4}} - V_{ref}\right) - \left(V^-_{DAC_{B_2}} - 0\right)\right] + C\left[\left(V^-_{DAC_{C_4}} - V_{ref}\right) - \left(V^-_{DAC_{B_2}} - V_{ref}\right)\right]\Bigg) = \frac{9}{8}CV^2_{ref} \end{aligned} \tag{3.53}$$

Hence, the total energy due to switching is obtained in Eq 3.54.

$$E_{C_4} = E^+_{C_4} + E^-_{C_4} = \frac{9}{4}CV^2_{ref} \tag{3.54}$$

Final Remarks The conventional switching scheme is not very energy efficient, especially because the switching action is performed before the comparator's decision. This means that, in the case of an approximation in the wrong direction, the energy previously stored in a capacitor is wasted and more energy is required to charge the complementary capacitor. Therefore, the DAC switching energy is higher in the case where the input signal is low, as shown in Figure 3.5. Figure 3.5 shows the DAC switching energy as a function of the output code for a 10 bit SAR ADC using the conventional switching scheme.

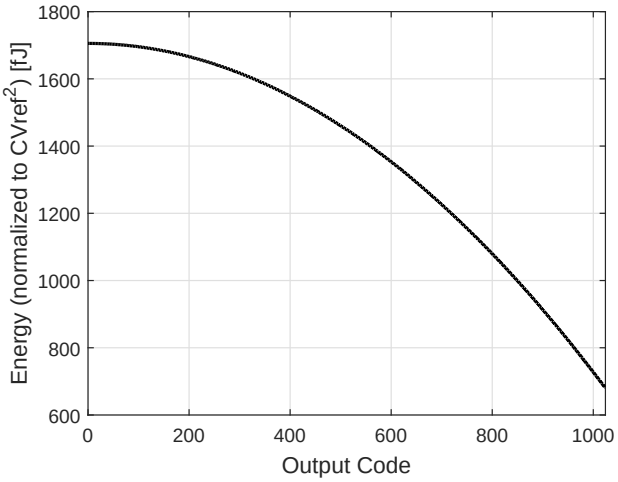


Figure 3.5: 10 bit SAR ADC switching energy as a function of the output code - conventional switching scheme.

3.3.2 Merged Capacitor Switching (MCS) or Vcm-based Switching Scheme

The Vcm-based switching scheme [16] does not follow the conventional successive approximation algorithm. Instead, as the signal is sampled on the top plates, the switching action can be performed after the comparator's decision, hence no wrong steps in the conversion are taken. Furthermore, since no switching is required in the first comparison, the MSB capacitor can be removed from the DAC arrays which halves the total capacitance of the DACs, Figure 3.6.

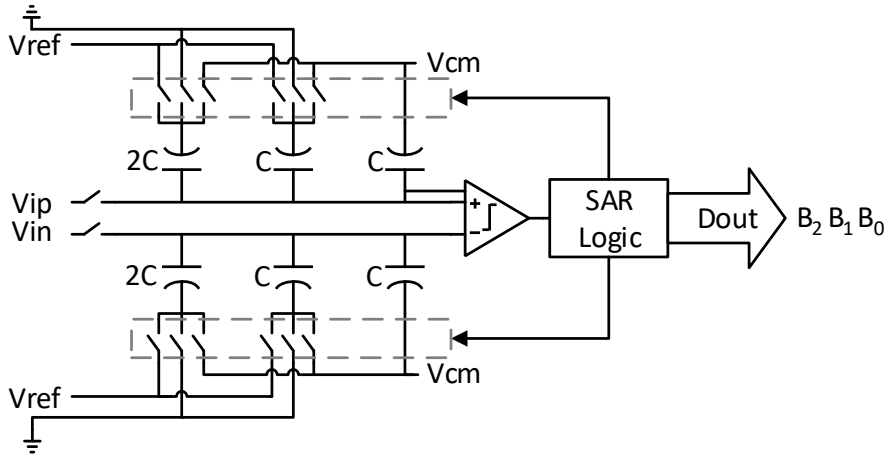


Figure 3.6: 3 bit SAR ADC Vcm-based architecture - differential circuit schematic.

The conversion starts with the sampling phase, ϕ_S. As mentioned before, the input signal is now sampled on the top plates of the DAC arrays, while the bottom plates are connected to the common mode voltage, V_{cm}. In the next phase,ϕ_A, the top plates are disconnected from the inputs and the bottom plates remain connected to V_{cm}. Notice that as the voltage across both capacitor networks remains constant, due to charge conservation,

no energy is required in this transition. At this moment, the comparator takes its first decision. In case $V_{ip} > V_{in}$, the bottom plate of the MSB-1 capacitor in the positive DAC is switched to gnd, whereas the MSB-1 capacitor in the other capacitive array is connected to V_{ref}. If the comparison's result is contrary, the complementary operation is performed. Notice that all the other bottom plates remain connected to V_{cm} and, regardless of the comparator's output, the capacitance switched is the same. After the DACs are settled, the comparator decides the MSB-1 bit, ϕ_B, and the process is repeated for the remaining bits, as depicted in Figure 3.7.

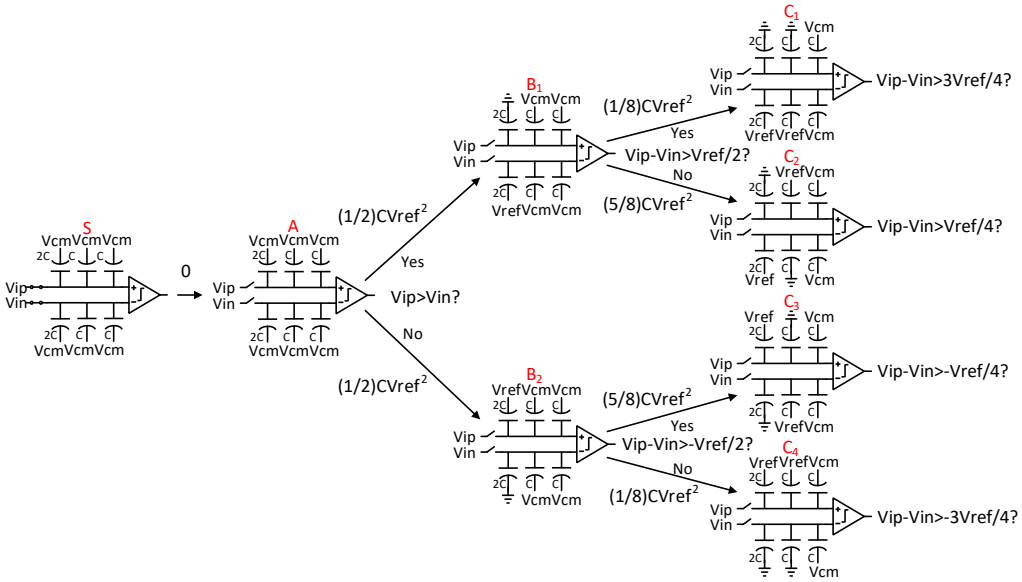


Figure 3.7: 3 bit SAR ADC Vcm-based switching procedure.

Besides showing all the possible conversion steps, Figure 3.7 also displays the DAC switching energy. The determination of these values is performed in a similar way to what was done to the conventional switching scheme, therefore it will not be repeated in this section. In Figure 3.8, the DAC switching energy is exhibited as a function of the output code for a SAR ADC using this switching scheme. Notice that the energy is completely symmetric as expected. Figure 3.8 also confirms that the Vcm-based switching method is much more energy efficient when compared to the conventional switching scheme.

3.4 Other SAR Architectures

Despite being used for moderate-speed, medium-resolution applications, SAR ADCs have found their way into other application spaces and are being used in several ways [25, 26].

High-speed SAR ADCs are being reported in recent scientific publications and conferences, making use of *Time-Interleaving* techniques [5, 26] and *Multiple-bits per Cycle* architectures [8, 26]. In [27], a combination of these two techniques is used.

SAR ADCs have also been used as sub-ADCs for Pipeline ADCs [28] and ΣΔ Modulators [29] and in [30] a SAR ADC with *Noise-Shaping* capability is presented.

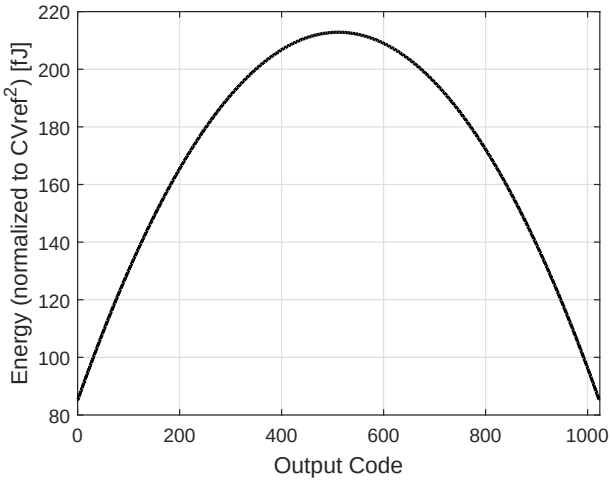


Figure 3.8: 10 bit SAR ADC switching energy as a function of the output code - Vcm-based switching scheme.

In [1], a SAR ADC specially developed for biomedical application makes use of several comparators to create a bypass-window which allows to skip some conversion steps, hence its power consumption is decreased.

A SAR ADC coarse-fine converter in which the residual voltage after the successive approximation coarse conversion is converted to time domain and a TDC is used to solve the LSBs is presented in [31].

SAR ADCs relying on Charge Sharing techniques, rather than Charge Redistribution, achieving very high energy-efficiency have recently been reported. However, these architectures are only suitable for very low speed, small resolution applications [18].

Chapter 4

Time-to-Digital Converters

Technology scaling and voltage supply reduction degrade the performance of pure analog systems, as previously explained in Chapter 1. On the other hand, digital circuits benefit from technology scaling in terms of area, speed and power consumption [6, 32]. Therefore, the trend is to minimize the analog complexity of today's circuits and move into the digital domain. Nevertheless, digital circuits can not extract valid information in the amplitude domain. On the contrary, their time domain resolution is very high [32]. In this sense, digital circuits can be used to increase the performance of analog circuits, including Analog-to-Digital Converters, if time domain related information can be resolved. In order to do so, *Time-to-Digital Digital Converters* can be used [7, 31].

Time-to-Digital Digital Converters are often described as highly precise stopwatches which convert time domain information into a digital representation [32]. TDCs can measure time intervals in the picoseconds range and their applications vary from time-of-flight measurements in high energy physics experiments to critical blocks in all-digital phase-locked loops [33].

The purpose of this chapter is to provide an introduction to the main concepts behind the time-to-digital conversion and presenting an overview to the most commonly used architectures to achieve high resolution in the time domain.

4.1 Counter Based TDC

The simplest form of a TDC is a digital counter, counting the cycles of a reference signal between a *START* and a *STOP* event [34], ΔT, as depicted in Figure 4.1.

This approach is not very efficient if a high time resolution is required, as it can only be increased by increasing the reference signal frequency, which always comes at the cost of increased power consumption [32].

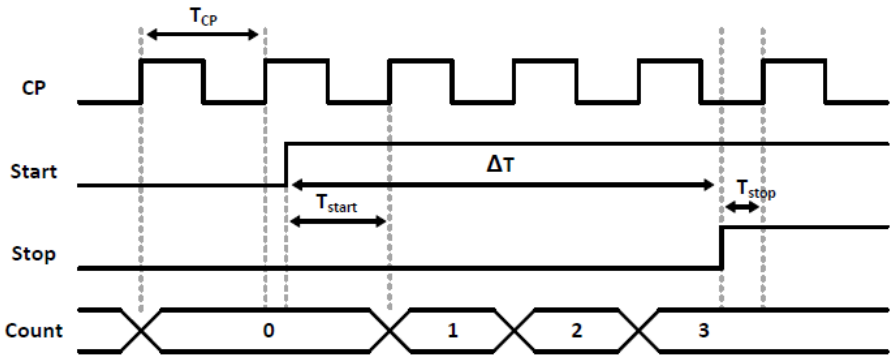


Figure 4.1: Counter Based TDC principle of operation.

4.2 Delay-Line Based TDC

In order to increase the resolution in a more efficient way, the time difference between the *START* and the *STOP* signals can be divided asynchronously, hence no longer requiring a reference signal. This can be accomplished by injecting the *START* signal into a *delay line* and sampling the delay elements in parallel when the *STOP* signal arrives at the *early-late detectors* (ELD). Each delay element consists of a buffer and the buffer's propagation delay, ΔT_1, corresponds to the TDC's resolution, T_{LSB}, in this architecture. The early-late detectors can be implemented by means of Flip-Flops, Latches or Arbiters [32], for example. This structure is known as the *Delay-Line* based TDC [35, 32] and its exhibited in Figure 4.2.

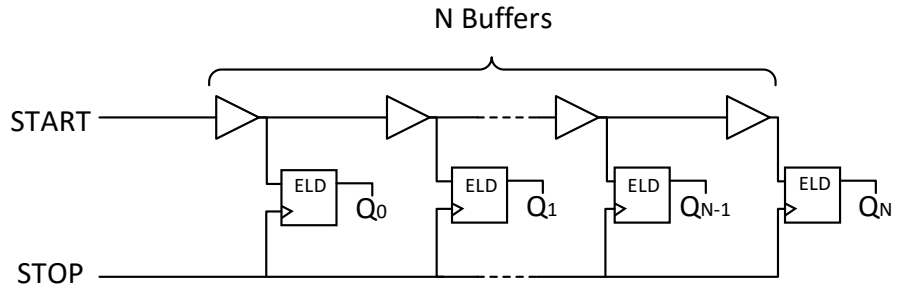


Figure 4.2: Delay-Line Based TDC Architecture.

In the *Delay-Line* based TDC, the sampling process triggers the ELDs and the *delay line* state is stored at the ELDs' output. The resulting output comes in a thermometer code, in which a HIGH value corresponds to a delay element for which the *START* signal has propagated through before the *STOP* event has occurred. By knowing the number of HIGH outputs, which is the same as the number of delay stages for which the *START* signal has passed before the *STOP* event has occurred, N, and the buffer propagation

delay, ΔT_1, it is possible to approximate ΔT by Eq. 4.1.

$$\Delta T = N \cdot \Delta T_1 \tag{4.1}$$

Although the resolution of this TDC is no longer linked to a reference signal, its time resolution is not very high as it is the same as the buffer delay ($T_{LSB} = \Delta T_1$). By replacing the buffers in the delay chain of Figure 4.2 for inverters, the resolution of the TDC is doubled simply because the delay of the inverter is half of the buffer's propagation delay $\left(T_{LSB} = \frac{\Delta T_1}{2}\right)$. However, this also translates into a modification of the output code, which is now a pseudo-thermometer code. In order to compute ΔT, one has now to observe a modification in the LOW-HIGH pattern at the output [32]. The stage at which this modification occurs has the same meaning of N, which has been explained before. Hence, ΔT can still be calculated according to Eq. 4.1, however considering ΔT_1 as the inverter propagation delay.

In any of the previous cases, the maximum time period measurable depends on the number of delay stages and their intrinsic delay. If large time periods are to be measured, several delay elements are required. This translates into large area occupied by the required circuit [32] and more susceptibility to process variations during the manufacturing process [6]. This problem can be overtaken by using a loop/ring configuration. In this case, the *START* signal is fed into the delay line and a loop counter is used to compute the number of times the *START* signal propagates through the loop, $Loop_{Count}$. By doing so, the *Dynamic Range* of the TDC is extended and the maximum time interval the TDC is capable of measuring is now limited by the number of bits of the counter [36]. With this architecture, ΔT is calculated as Eq. 4.2, where M denotes the number of delay elements.

$$\Delta T = \Delta T_1 \left(Loop_{Count} \cdot M + N\right) \tag{4.2}$$

4.3 Sub-Gate Delay Resolution TDCs

The TDC architectures introduced so far only allow to quantize time differences bigger than that of the inverter propagation delay, which depends on the technology. If finer resolution is needed, *Sub-Gate Delay* Resolution architectures should be employed [32].

4.3.1 Vernier Delay-Line TDC

The *Vernier Delay-Line* TDC [37, 38] can be analysed as an extension of the *Delay-Line* based TDC. In the *Vernier Delay-Line* TDC, two distinct delay lines are used, as depicted in Figure 4.3. The delay elements of each delay chain are designed such that they present different propagation delays, ΔT_1 and ΔT_2, being ΔT_2 slightly shorter than ΔT_1, hence one of the delay lines is faster than the other. The time *skew* between the two events is diminished throughout the delay chains according to Eq. 4.3, which defines the resolution for this structure [32].

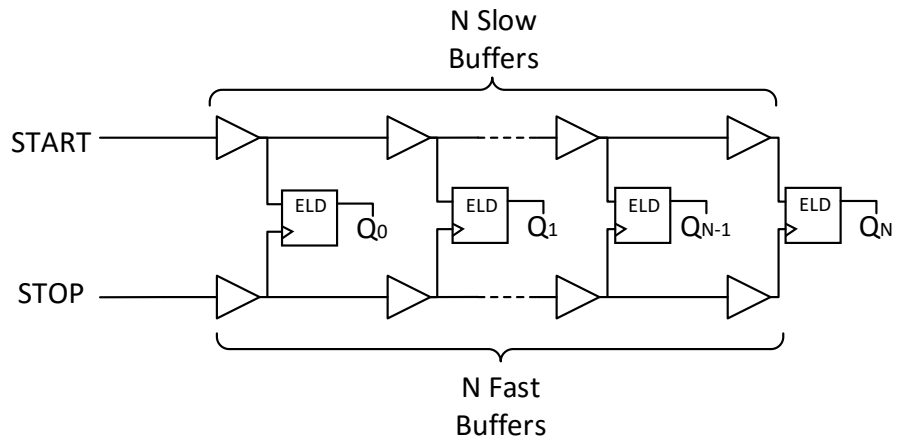


Figure 4.3: Vernier Delay-Line TDC Architecture.

$$T_{LSB} = \Delta T_1 - \Delta T_2 \tag{4.3}$$

This will allow the *STOP* signal, which is propagated in the *FAST* line, to catch up with the *START* signal after a certain period of time, as shown in Figure 4.4 [32].

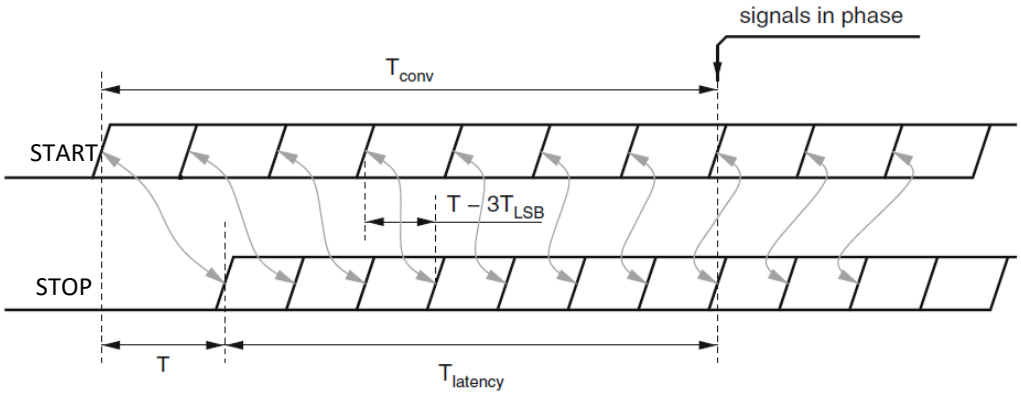


Figure 4.4: Operating principle of Vernier Delay-Line TDC.

Similarly to the *Delay-Line* based TDC, the *Vernier Delay-Line* TDC early-late detectors produce a HIGH output value if the delayed version of the *START* event propagates through a delay stage before the *STOP* signal triggers the stage's ELD. However, the *Vernier Delay-Line* TDC presents *latency* since the *STOP* signal also has to be propagated across a delay chain. This translates into a long conversion time and the output code, N, not being fully available at the moment the *STOP* event occurs, but only as the *STOP* signal propagates across the entire delay chain, which limits the measurement rate [37].

Only after it is fully propagated, is possible to approximate the time difference between the two events as Eq. 4.4.

$$\Delta T = N\,(\Delta T_1 - \Delta T_2) \tag{4.4}$$

Latency increases with the number of bits of the *Vernier Delay-Line* TDC and with the intrinsic propagation delay of the elements present in the *FAST* delay chain. However, modifying these parameters also changes the maximum measurable time difference (*Dynamic Range*) and the TDC's resolution. A loop implementation of this architecture is also possible being its benefits similar to those of the *Delay-Line* [32, 36].

Due to the *Vernier's Delay-Line* TDC capability to obtain sub-gate resolution and its modular structure (if no loop is used), which eases its implementation, this architecture arises as a strong candidate to be used in this work.

4.3.2 Other Sub-Gate Resolution TDCs

Several other *Sub-Gate Resolution* architectures such as the *Local-Passive Interpolator* [39], *Pulse-Shrinking* [40] and *Time Amplifier* [41] exist.

Interpolation techniques are behind the principle of operation of the *Local-Passive Interpolator* structure. The *Pulse-Shrinking* TDC consists on creating a pulse signal defined by the *START* and the *STOP* signals, being the width of this pulse reduced in each stage of the delay line. *Time Amplifier* architectures are usually employed to achieve very high resolution since they first stretch the time difference between the *START* and the *STOP* events and then quantize the amplified time difference.

CHAPTER 5

PROPOSED ARCHITECTURE

As previously mentioned in Chapter 1, this work intends to study how the time domain information can be used to increase SAR ADCs performance. In this sense, this chapter introduces the proposed architecture from a system prespective down to a high-level model. In between, CMOS implemented circuits will be presented.

5.1 System Level Description

The proposed converter's architecture is depicted in Figure 5.1. This structure is very similar to that of the conventional SAR ADC, with an additional block. This additional block, a Time-to-Digital Converter, will be used to measure the time required by the comparator to produce an output signal. Since this time is directly related to the signal under comparison, additional information about the signal's amplitude can be extracted [7]. A similar SAR architecture, which also makes use of the time domain information, is proposed in [31]. In this case, the authors implemented a Voltage-to-Time Converter (VTC) to convert the residual voltage after the coarse conversion into the time domain and a TDC is used to solve the LSBs.

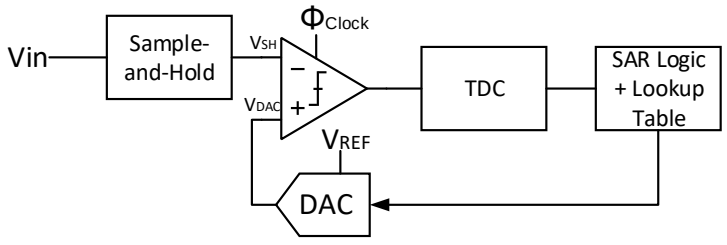


Figure 5.1: Proposed Architecture - Single Ended.

The proposed architecture differs from that in [31] by eliminating the need of the VTC and also by using the time domain information to obtain the MSBs. The use of the VTC is avoided since the comparator can be used to perform the voltage to time conversion and the use of the time domain information to solve the MSBs presents several advantages in terms of:

- **Speed**, since several conversion steps can be skipped as the MSBs are solved by the TDC. Also, the bigger the ΔV_{in}, the faster the comparator's response. Thus, a smaller TDC (with the same time resolution) can be used due to the time to be measured being smaller. Besides, using a smaller TDC translates into having its output code faster, therefore the capacitive DACs have more time to *settle*;
- **Power Consumption**, not only by the fewer conversions made by the power hungry comparator but also because a smaller TDC can be used. Moreover, no energy is wasted in the conventional binary search algorithm as the MSBs' capacitors in feedback DACs are put directly in the position they will have at the end of the conversion;
- **Possibility of Creation of a Time Window** which will allow to skip the MSBs if the current sample is close to the previous sample, which again leads to an increase in the converter's speed and a decrease in the power consumption.

Summarizing, this system can be classified as a hybrid converter in which a *coarse* conversion is first performed in the time domain by the TDC. Afterwards, a *fine* conversion is performed by the conventional SAR algorithm.

5.2 High-Level Model - Single Ended

Before implementing the proposed architecture in CMOS circuits, a high-level model of the system must be developed in order to validate it, since such structure has never been reported in scientific publications.

The first step towards the mathematical description of the system is the characterization of the comparator's output delay *versus* comparator's input voltage (ΔT_{out} *vs* ΔV_{in}). Since this characteristic is the main concept behind this work, it should be as accurate as possible. Therefore, a comparator circuit was designed in 65nm CMOS and its ΔT_{out} *vs* ΔV_{in} characteristic extracted through electrical simulations. The comparator used [42] is based on the traditional *Double-Tail Comparator* [17] and its operation will be explained in the next section. The obtained characteristic is presented in Figure 5.2 for a load of 20 fF at each output.

TDC Model

After the comparator's time response has been characterized, modelling the TDC is necessary in order to be able to extract information from the time domain. Eq. 5.1 computes

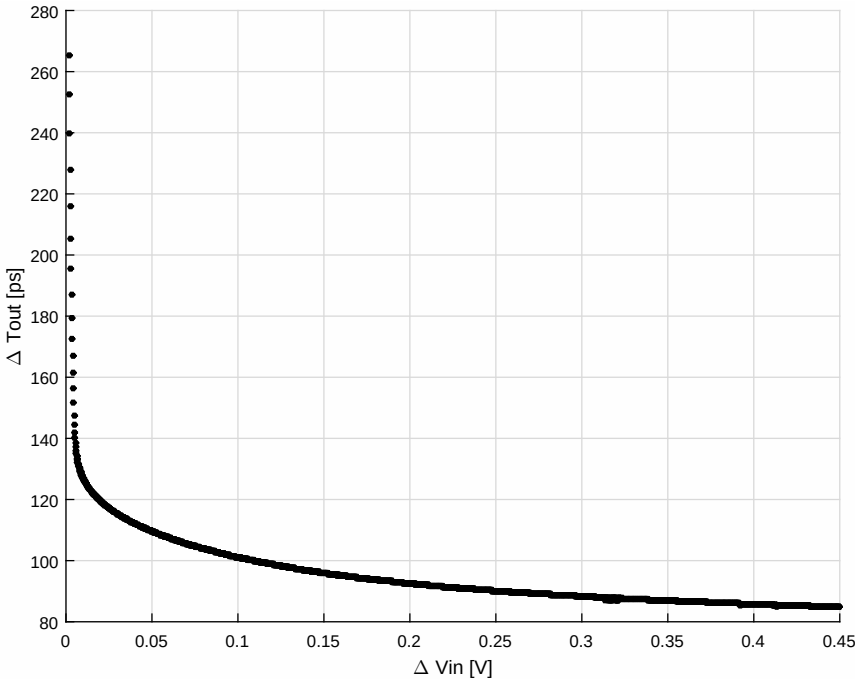


Figure 5.2: Simulation results of the comparator - Comparator's decision time *vs* ΔV_{in}.

the TDC output, according to the time the comparator takes to produce a valid output. In Eq. 5.1, $Comparator_{delay}$ corresponds to the time taken by the comparator to measure a certain ΔV_{in}, Max_{delay} and Min_{delay} to the maximum and minimum of the comparator's time characteristic of Figure 5.2 and N is the number of bits of the TDC.

$$TDC_{out} = floor\left(\frac{Comparator_{delay} - Min_{delay}}{Max_{delay} - Min_{delay}} \cdot (2^N - 1)\right) \tag{5.1}$$

Considering a 5 bit TDC and combining the time domain information from the comparator with the TDC's response (Eq. 5.1), it is possible to obtain Figure 5.3.

From Figure 5.3, it can be concluded that the TDC model is performing as expected, dividing the comparator's time response in equally spaced digital codes and the bigger the ΔV_{in}, the smaller the ΔT_{out}, thus the smaller the TDC's output code.

Coarse Converter

As previously explained, the TDC output code will be used to decide the MSBs in the proposed ADC architecture. However, the comparator's time response is not linear, hence the TDC characteristic is not linear (in the voltage domain) either, therefore it can not be used to solve N bits throughout the full input voltage range. To overcome this issue, a *Lookup Table* was implemented under the following methodology, considering that the TDC can decide up to a maximum of 5 bits:

1. Obtain the input voltage which led all the TDC output codes to change, V_{TDC};

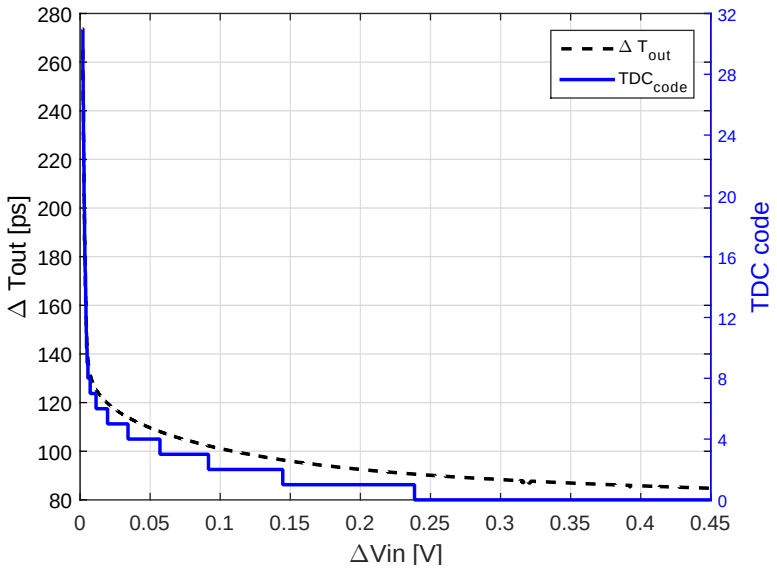


Figure 5.3: Comparator's decision time and TDC output code *vs* ΔV_{in}.

2. For each TDC_{code}, convert the corresponding V_{TDC} to a binary code;

3. Evaluate the number of equal bits between adjacent binary codes, N;

4. For each TDC_{code}, concatenate the binary value obtained, keeping only the number of bits determined in the previous step.

The the N *vs* ΔV_{in} characteristic is plotted in Figure 5.4 and the resulting *Lookup Table* for a 5 bit TDC is presented in Table 5.1. Notice that this *Lookup Table* can only be used for input values greater than $V_{REF}/2$. If this is not the case, another *Lookup Table*, complementary to Table 5.1, is used.

From Table 5.1 it can be concluded that limiting the maximum number of bits to be decided by the TDC to 5 bits does not allow to take the maximum advantage of the TDC since the code to be programmed in the DAC is unchanged after code 6. Therefore, the TDC usage is extended beyond this point in the fully-differential implementation.

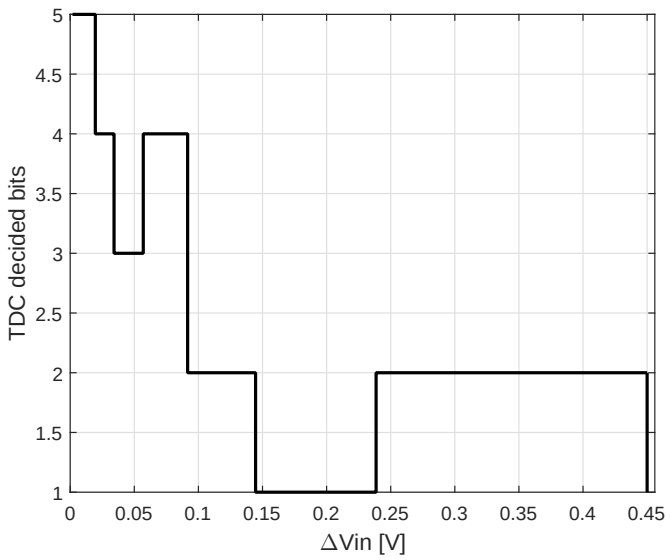


Figure 5.4: Number of bits decided by the TDC *vs* ΔV_{in}.

Table 5.1: *Lookup Table* to be used by the *Coarse* Converter.

TDC_{code}	DAC_{code}	N
31	16	5
28	16	5
26	16	5
24	16	5
22	16	5
20	16	5
19	16	5
17	16	5
16	16	5
15	16	5
14	16	5
13	16	5
12	16	5
11	16	5
10	16	5
9	16	5
8	16	5
7	16	5
6	16	5
5	8	4
4	4	3
3	9	4
2	2	2
1	1	1
0	3	2

System Behavioural Model

Considering the models for the comparator and TDC described above and using the traditional binary search algorithm for the SAR *Fine* Converter, the whole system's operation can be described according to the proposed algorithm:

1. Apply a signal to be tested;
2. Check comparator's output and TDC_{code};
3. Apply the corresponding code to the capacitive DAC, according to the *Lookup Table* present in Table 5.1 - ***Coarse* Conversion**;
4. Apply the SAR conventional algorithm in the remaining bits - ***Fine* Conversion**.

The proposed system was implemented in MATLAB as a 12 bit ADC making use of a 5 bit TDC. Non-idealities such as capacitor mismatch and comparator offset were included and 0.9 V used as V_{REF}.

The converter's response to a full range DC sweep can be observed in Figure 5.5. Figure 5.6 exhibits the converter's DNL and INL and in Figure 5.7 the number of comparisons necessary for each input voltage value is revealed. In Figure 5.8, the percentage of comparisons used in the full conversion is shown.

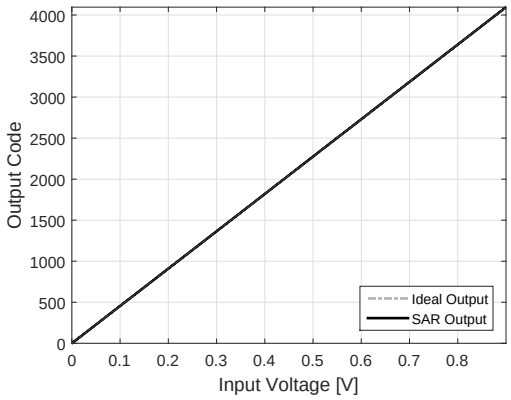


Figure 5.5: System's digital output code *vs* V_{in} - the two lines are overlap.

These results were obtained after digital correction of the Coarse Converter and considering a capacitor mismatch of $\sigma = 1.5\%$. The digital correction was implemented by deciding one bit less than what the TDC could provide. This ensures that even in the case of an offset on the TDC or mismatch between delays, the DAC is always programmed in a way that it is capable of keeping track of the signal. Moreover, robustness against PVT variations is increased.

The results obtained allow to validate the architecture and to verify that the TDC can be used to solve the MSBs. Although the percentage of 12 comparisons is still significant, performance improvements relatively to conventional SAR architectures can be expected, as long as the of the TDC and subsequent digital mapping logic energy are kept low.

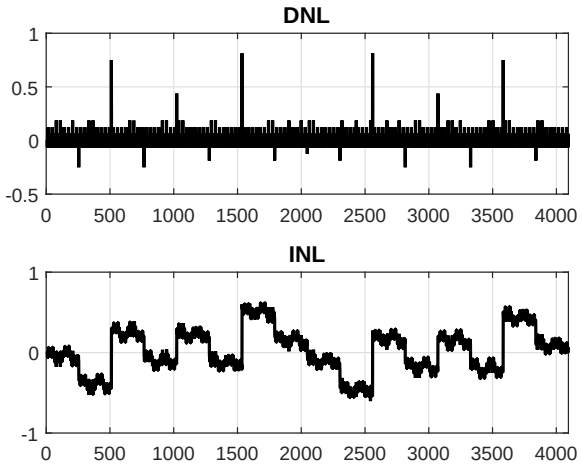


Figure 5.6: System's DNL and INL.

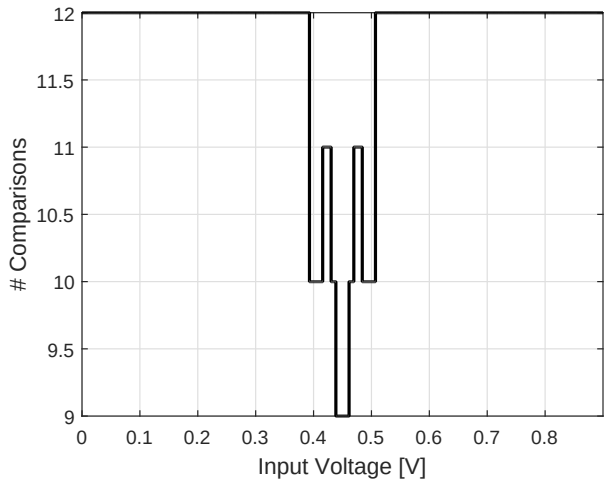


Figure 5.7: Number of comparisons *vs* V_{in}.

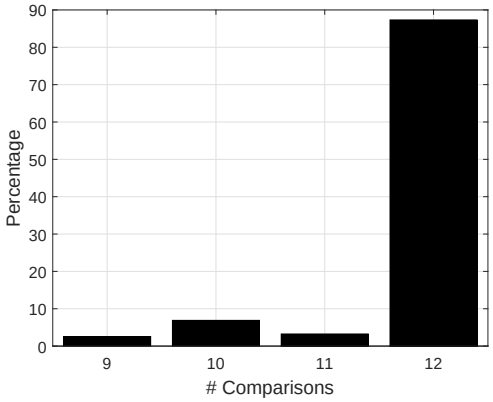


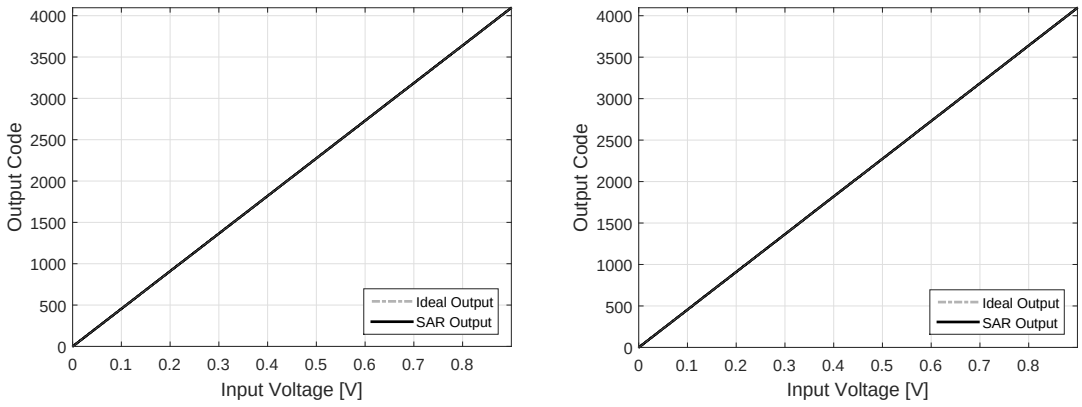
Figure 5.8: Percentage of comparisons.

Extended Model - Time domain *Bypass Window*

The previous architecture can be further extended to incorporate a *Bypass Window* [1, 43], which will be used in every new conversion to verify if the sample under evaluation is close to the previous one. In this case, only the LSBs need to be solved by the SAR algorithm and power is saved since no energy is wasted in the MSBs of the DAC. Otherwise, the previous algorithm is used for the full conversion.

The *Time Window* can be controlled digitally depending on the TDC's output. Moreover, the number of MSBs programmed in the DAC can also be modified. Doing so will influence the number of bits to be skipped, hence the number of LSBs to be solved by the SAR algorithm. These parameters can be optimized, taking into account the input signal, so that the power consumption of the whole converter is minimized.

The simulation results for the extended model, considering two different *Bypass Time Windows*, are organized as follows: The system's response to a full range DC sweep can be observed in Figure 5.9. Figure 5.10 exhibits the converter's DNL and INL and in Figure 5.11 the number of comparisons necessary for each input voltage value is revealed. In Figure 5.12, the percentage of comparisons used in the full conversion is shown. It should be mentioned that in both cases, the number of bits pre-programmed by the DAC was fixed to five.

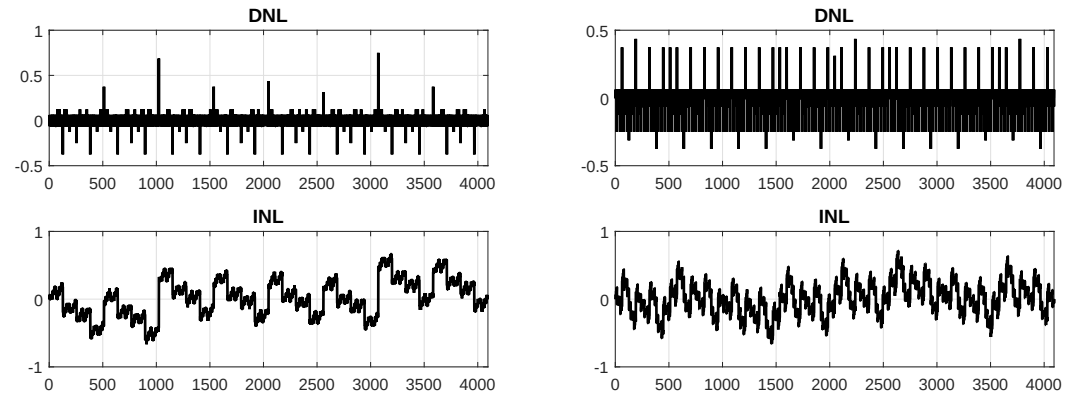


a Large Time Window - $\Delta V_{Window} \approx 2.4mV$.

b Small Time Window - $\Delta V_{Window} \approx 19.6mV$.

Figure 5.9: System's digital output code *vs* V_{in}. - the two lines are overlap.

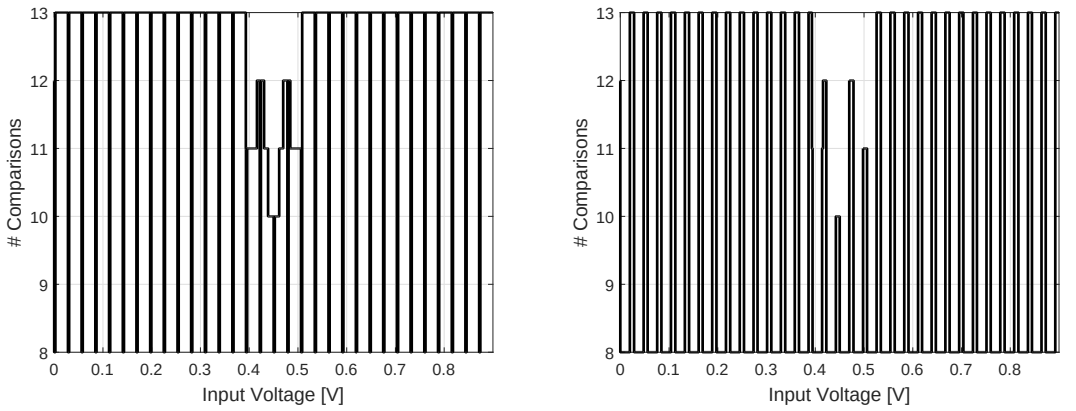
The results obtained for the extended model demonstrate that the implementation of the time window allow to reduce the effective number of comparisons needed if the signal is within predefined window. Of course, when the signal is out of range, one more iteration may be necessary and, if in case the TDC response in the input signal level only allows to decide 1 bit, 13 comparisons may have to be performed. However, it is expected that the converter benefits from the window implementation since, approximately 70 % of the time, its behaviour is similar to a 8 bit converter. Besides, if the signal is *quasi-static*, such as biomedical signals, this number is expected to increase, as long as the signal



a Large Time Window - $\Delta V_{Window} \approx 2.4mV$.

b Small Time Window - $\Delta V_{Window} \approx 19.6mV$.

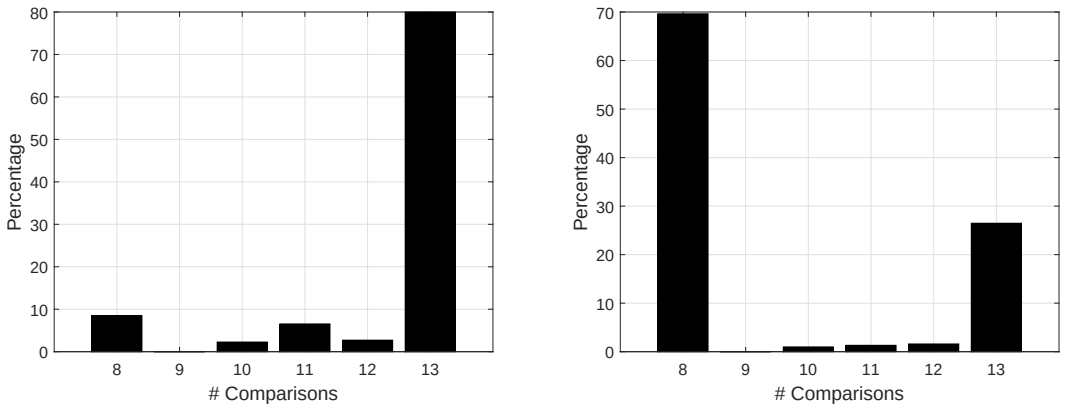
Figure 5.10: System's DNL and INL.



a Large Time Window - $\Delta V_{Window} \approx 2.4mV$.

b Small Time Window - $\Delta V_{Window} \approx 19.6mV$.

Figure 5.11: Number of comparisons *vs* V_{in}.



a Large Time Window - $\Delta V_{Window} \approx 2.4mV$.

b Small Time Window - $\Delta V_{Window} \approx 19.6mV$.

Figure 5.12: Percentage of comparisons.

remains inside the predefined window and the converter only needs more comparisons when the signal presents some spikes.

These results also prove that the system can be effectively tuned to achieve better performance, depending on the input signal. In the signal under test, the use of a smaller time window (greater voltage window) allowed to significantly decrease the number of comparisons needed. For these reasons, it is expected that the power consumption of this architecture is lower than in the previous structure, in which the TDC was only used to implement a *Coarse Converter*.

5.3 CMOS Circuits Implementation

In order to obtain a more realistic model of the system, real circuit's characteristic curves should be obtained. In this sense, this section introduces the circuits already implemented in 65nm CMOS, namely the comparator and the TDC.

5.3.1 Comparator

The comparator will be used in two distinct ways. On one hand, it will be used to perform the voltage to time conversion. On the other hand, it will do its conventional job in SAR ADCs.

The comparator implemented [42], based on the *Double-Tail* Comparator [17], is depicted in Figure 5.13. This comparator is suitable to operate at low supply voltages since it has only a few transistors stacked and, at the same time, is faster and less power hungry than the *Double-Tail* Comparator or the *StrongArm* Comparator [42]. By having the output stage separated from the inputs, it also allows to reduce the kickback and input referred offset [3].

The operation of this comparator is as follows. During the reset phase ($\Phi_{Clock} = 0$), Mtail1 and Mtail2 are off, avoiding static power consumption, M3 and M4 pull both *fn* and *fp* nodes to VDD, hence transistors MC1 and MC2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During the decision-making phase ($\Phi_{Clock} = 1$), Mtail1 and Mtail2 are ON, M3 and M4 turn OFF. At the beginning of this phase, the control transistors, MC1 and MC2, are still OFF, since *fn* and *fp* are close VDD. Therefore, *fn* and *fp* start to drop with different rates depending on the input voltages. The fastest node to drop will trigger the latch operation which will increase its dropping rate even more. Also, transistors Msw1 and Msw2, which act like switches controlled by the nodes *fn* and *fp*, respectively, allow both to increase the comparator's speed and to save power since one of the nodes is not fully discharged, hence doesn't need to be completely charged back to *VDD* in the next clock cycle [42]. Figure 5.14 depicts a single comparison in which the comparator's operation can be verified.

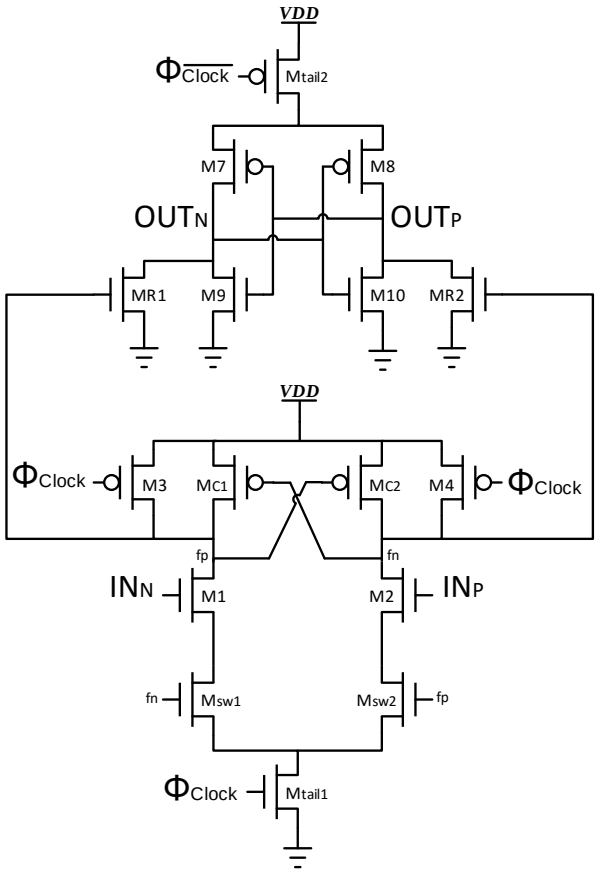


Figure 5.13: Comparator Circuit, as proposed in [42].

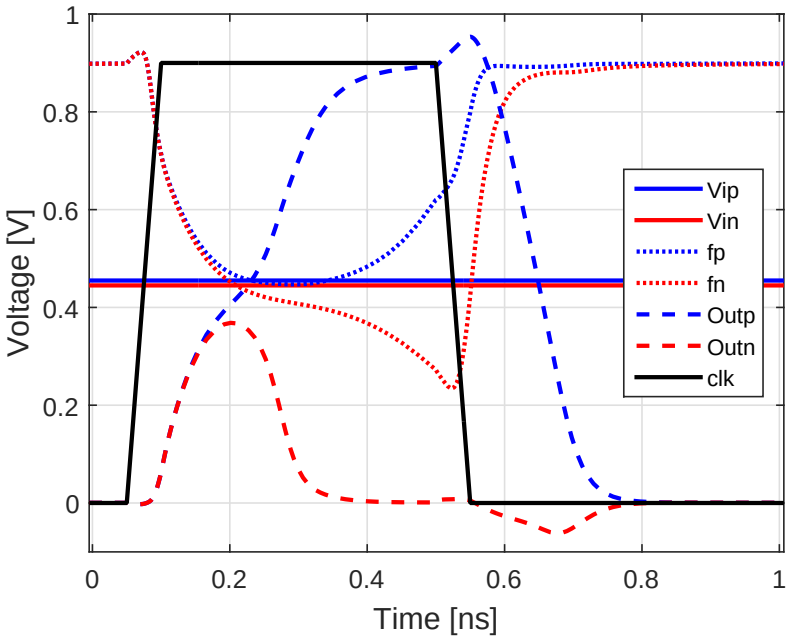


Figure 5.14: Single Comparison - $\Delta Vin = 10mV, Vcm = 450mV, Load = 20fF$.

In the CMOS implementation, large transistors were used to improve matching [44] . Transistor sizes are presented in Table 5.2.

Table 5.2: Comparator transistor sizes.

Transistor	**Width** (μm)	**Length** (μm)
$M_{1,2}$	17.50	0.15
$M_{3,4}$	3.00	0.09
$M_{7,8}$	20.00	0.15
$M_{9,10}$	7.50	0.15
$M_{R_{1,2}}$	3.00	0.15
$M_{C_{1,2}}$	2.00	0.09
$M_{sw_{1,2}}$	7.50	0.15
M_{tail_1}	15.00	0.12
M_{tail_2}	15.00	0.15

5.3.2 Time-to-Digital Converter

The TDC is a fundamental block in the proposed architecture, since it will be responsible for quantizing the time taken by the comparator to produce a valid output. Therefore, its design should be careful in order to avoid non-linearities which may introduce distortion in the full converter. The *Vernier Delay-Line* TDC [38] was the chosen architecture for its intrinsic monotonicity, ability to obtain sub-gate resolution and modularity which eases its implementation [32].

This architecture, as previously discussed in Chapter 4, is based on two *delay lines*, one faster than the other, and *early-late detectors* [32, 38].

The implemented *Vernier Delay-Line* TDC circuit is presented in Figure 5.15. Note that a delay was added to the beginning of the *START* line so that a offset is created. This offset is necessary, otherwise digital codes would be wasted since the comparator's time response is never smaller than approximately 70 ps.

Note that inputs $STOP_P$ and $STOP_N$ will be connected to the comparator outputs so that both outputs are sensed. The *START* input is to be used by the clock signal.

Each delay element consists of a CMOS buffer, which is constituted by two CMOS inverters. In Table 5.3, transistor's sizes for the *Offset*, *Fast* and *Slow* CMOS inverters are presented. It should be mentioned that the *Fast* inverter is used to implement the *Fast* Delay Line and the *Slow* inverter the *Slow* Delay Line.

The *early-late detectors* were implemented as *SR Latches* using *NAND* gates, as depicted in Figure 5.16. Several other types of *early-late detectors*, such as *Transmission-Gate* Edge Triggered Register, C^2MOS Register and *True Single-Phase Clocked* Register based approaches [6] were tested. However, their performance, in terms of speed, degraded the TDC response, hence these ELDs discarded. Table 5.4 exposes transistor sizes used

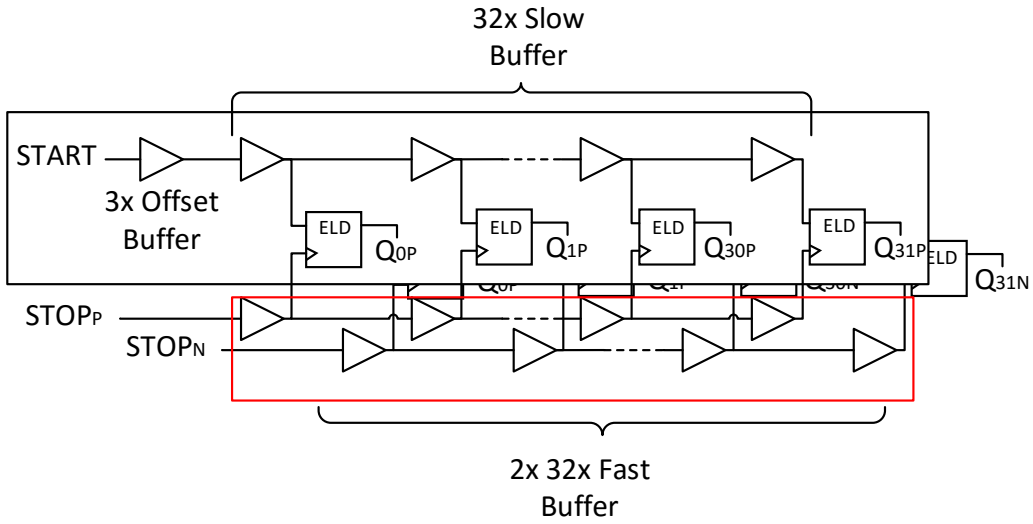


Figure 5.15: Differential Time to Digital Converter Circuit.

Table 5.3: Transistor sizes of the inverters used to implement the delay lines.

	PMOS		**NMOS**	
	Width (nm)	*Length (nm)*	*Width (nm)*	*Length (nm)*
Offset	360	60	135	60
Fast	1025	60	390	60
Slow	1000	60	350	60

in the *NAND* gates and in the CMOS inverter. This sizes were chosen according to the methodology described in [6].

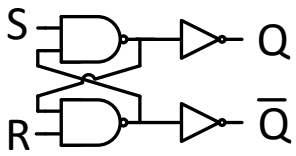


Figure 5.16: SR Latch to be used as *early-late detector*.

In Figure 5.17, the transient response for a 10 ps interval between the *START* and *STOP* signals is shown. The *START* signal is propagated in the *Slow* delay line whereas the *STOP* event goes through the *Fast* delay line. As the signals propagate through the TDC stages, we can verify that the time difference between the two events is reduced. While the signal in the *Slow* line arrives at a certain stage before the *STOP* signal, the TDC produces a logic value 1. Otherwise, the TDC responds with a 0. For the present simulation, the TDC produces an output code of 111100...000 (thermometer code). The measured TDC

Table 5.4: SR Latch transistor sizes.

	PMOS		NMOS	
	Width (nm)	*Length (nm)*	*Width (nm)*	*Length (nm)*
NAND	350	60	270	60
Inverter	350	60	135	60

resolution, via *SKILL* scripts, was approximately 2.14 ps, hence this output code is as expected.

Another noticeable fact is the delay between the moment the *START* signal arrives at a certain stage and its output being ready. This latency will be a bottleneck for proposed system since it will be limiting the sampling rate. It should also be mentioned that this latency is signal dependent.

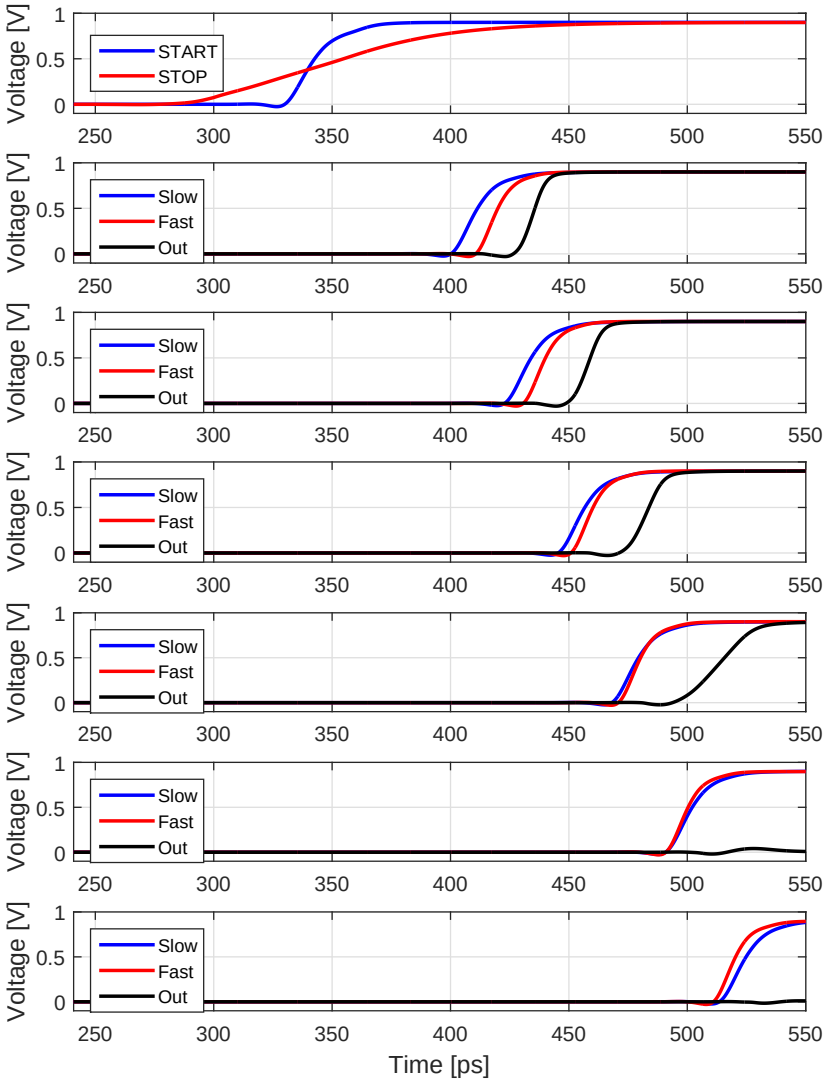


Figure 5.17: TDC response for a 10 ps interval between the *START* and *STOP* signals.

5.3.3 Comparator and TDC

Instead of relying in the characteristic curves of each block simulated separately, in order to capture non-linearities such as the loading effect, it makes sense to capture the behaviour of the comparator and the TDC together as a system. In this way, more reliable characteristics can be obtained to incorporate in the high level model of the proposed converter.

In Figure 5.18, the comparator's time response characteristic and the TDC output code are plotted *versus* the input voltage. From Figure 5.18, we can conclude that the loading effect of the TDC on the comparator was overestimated, since the comparator's response is faster than that obtained in Figure 5.2. The TDC characteristic is also different from that depicted in Figure 5.3. The minimum TDC output code is 3 due to the offset in the beginning of the TDC's *START* line.

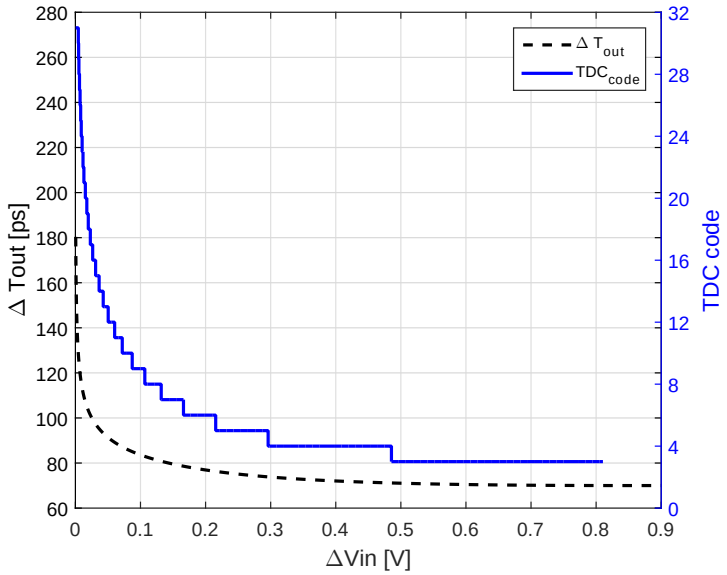


Figure 5.18: Comparator's decision time and TDC output code *vs* ΔV_{in}.

Another important parameter is the time between the comparator's output and the TDC output. As previously mentioned, latency is signal dependent and will be limiting the converter's sampling rate. In Figure 5.19, latency is shown as a function of the input signal.

Figure 5.20 depicts the energy consumption of the comparator and the TDC as a function of the input voltage. The comparator energy is signal dependent, whereas the TDC's is signal independent. Therefore, we can predict that it if the TDC can solve more than 4 bits in the voltage domain, it is worth using an architecture such as the proposed since the energy consumption of the TDC is smaller than 4 usages of the comparator.

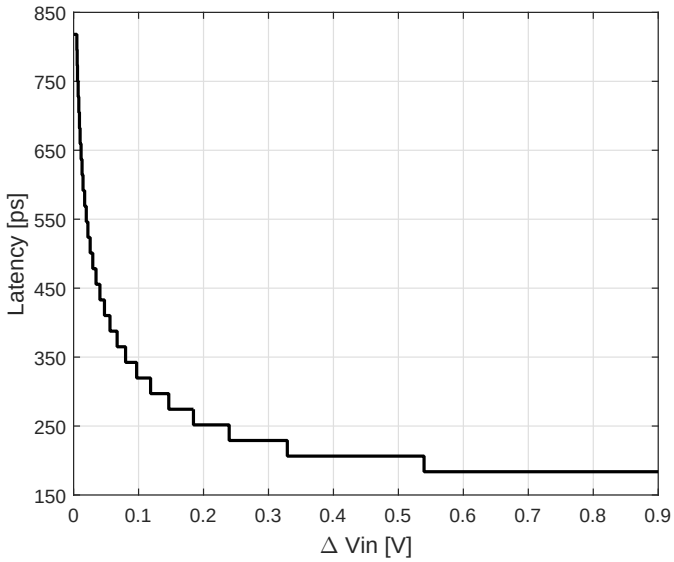


Figure 5.19: Latency *vs* ΔV_{in}.

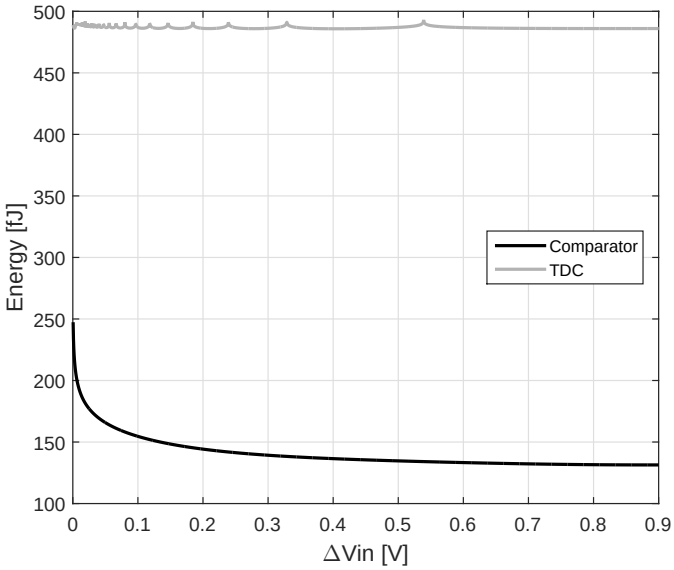


Figure 5.20: Energy *vs* ΔV_{in}.

5.4 High-Level Model - Fully Differential

In Section 5.2 it was demonstrated that the proposed architecture can effectively decrease the number of comparisons needed to solve 12 bits. In this section, the fully-differential architecture of the proposed converter is presented, Figure 5.21. The high-level models of the fully-differential architecture, developed in this section, take into account the circuit's responses from the CMOS implementation and the DAC energy, modulated following the methodology described in Chapter 3.

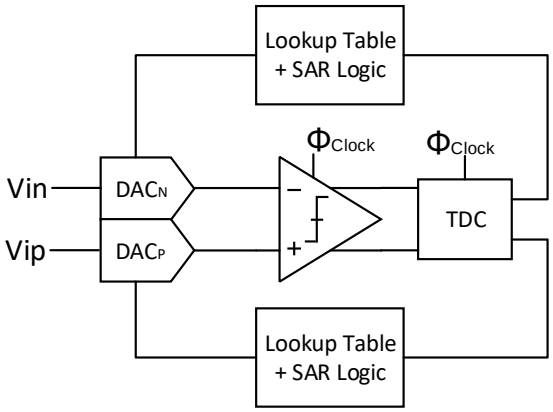


Figure 5.21: Proposed Architecture - Fully Differential.

In order to develop the differential model, a new *Lookup Table*, Table 5.5, was created, following the same method as in Section 5.2. Instead of limiting the maximum number of bits to 5, the TDC is now allowed to solve up to 9 MSBs in the voltage domain. Although more bits could be solved, any deviations from the characteristics exhibited in Figure 5.18 would decrease the converter's performance. Notice that Table 5.5 shows values for differential signals above and below zero.

Data from Table 5.5 can be used to represent the number of bits to be programmed, $TDCbits$, as a function of the input signal, Figure 5.22. The number of bits the TDC is able to solve is directly related to the comparator's time response. Since the comparator's time response does not vary significantly for large differential input signal values, according to Figure 5.18, the TDC can not solve many bits in this range, as exhibited in Figure 5.22. In practice, for digital correction purposes, one less bit than what is represented in Figure 5.22, will be programmed in the DAC. This will limit the voltage range in which the TDC is worth using, however it is necessary to increase the system's robustness.

Increasing the number of bits decided by the TDC in the voltage domain in the presence of a large differential input signal would be possible by increasing its resolution. That, however, would increase the power consumption and decrease the dynamic range. Another approach could be a *Coarse-Fine* TDC, using an architecture such as the *Time Amplifier* together with the *Vernier Delay-Line*.

Table 5.5: Differential Model - *Lookup Table*

$\Delta V < 0$			$\Delta V > 0$		
TDC code	*DAC code*	*TDC bits*	*TDC code*	*DAC code*	*TDC bits*
3	0	2	3	3	2
4	0	1	4	1	1
5	5	4	5	10	4
6	1	2	6	2	2
7	6	4	7	9	4
8	13	5	8	18	5
9	3	3	9	4	3
10	14	5	10	17	5
11	29	6	11	34	6
12	7	4	12	8	4
13	60	7	13	67	7
14	30	6	14	33	6
15	61	7	15	66	7
16	123	8	16	132	8
17	15	5	17	16	5
18	124	8	18	131	8
19	62	7	19	65	7
20	125	8	20	130	8
21	251	9	21	260	9
22	31	6	22	32	6
23	252	9	23	259	9
24	126	8	24	129	8
25	253	9	25	258	9
26	253	9	26	258	9
27	63	7	27	64	7
28	254	9	28	257	9
29	254	9	29	257	9
30	254	9	30	257	9
31	127	8	31	128	8

In order to validate the proposed architecture, MATLAB simulations were performed, considering a 12 bit DAC, with capacitor mismatch of $\sigma = 1.5\%$, and the real response from the comparator and the TDC. It should be mentioned that digital correction was employed in the same conditions as before.

The converter's response to a full range DC sweep can be observed in Figure 5.23. Figure 5.24 exhibits the linearity parameters DNL and INL and, in Figure 5.25, the number of comparisons necessary for each input value is revealed. In Figure 5.26, the percentage of comparisons used in the full range conversion is shown. Conversion time is presented as a function of the input signal in Figure 5.27.

Figure 5.23 and Figure 5.24 demonstrate that the proposed converter is linear. The DAC's binary architecture can be observed by analysing the INL pattern in Figure 5.24.

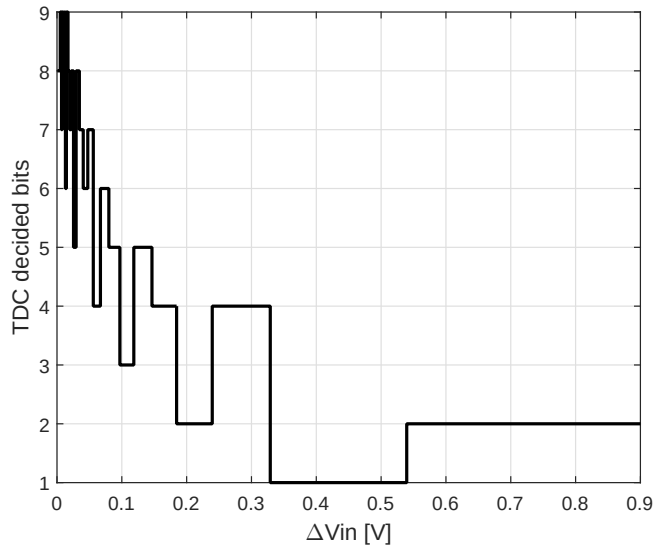


Figure 5.22: Number of bits decided by the TDC *vs* ΔV_{in}.

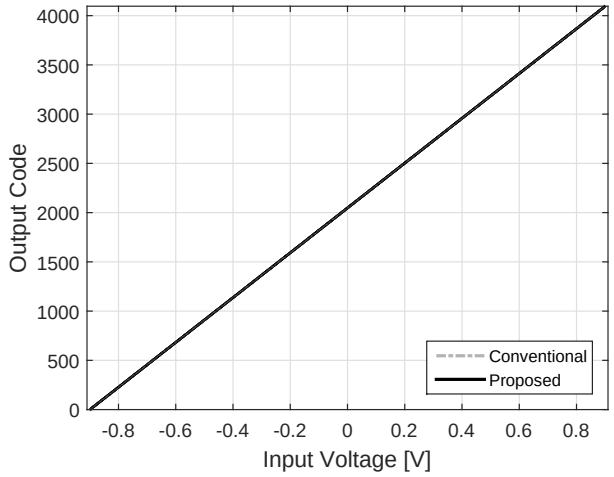


Figure 5.23: System's digital output code *vs* V_{in}. - the two lines are overlap.

The effects of capacitor mismatch in the DAC can also be observed in the INL shape, particularly the mismatch effect of the two most significant capacitors on the system's linearity.

The number of comparisons performed for each input signal mirrors the *Lookup Table*, 5.5, bearing in mind that digital correction was used. The large range of input values, in Figure 5.25, for which the converter needs 12 comparisons is as expected due to the low variability of the comparator's time response. On the other hand, when the comparator's time response changes significantly, less comparisons are needed since the TDC can provide more voltage resolution. Figure 5.26 shows that the proposed architecture decreases the number of 12 comparisons needed by 30%, when compared to the traditional successive approximation algorithm.

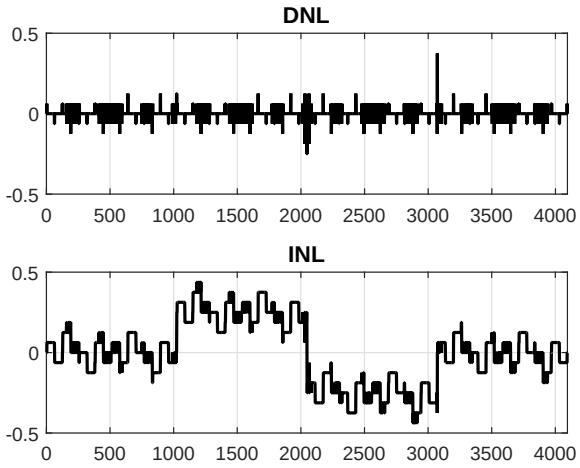


Figure 5.24: System's DNL and INL.

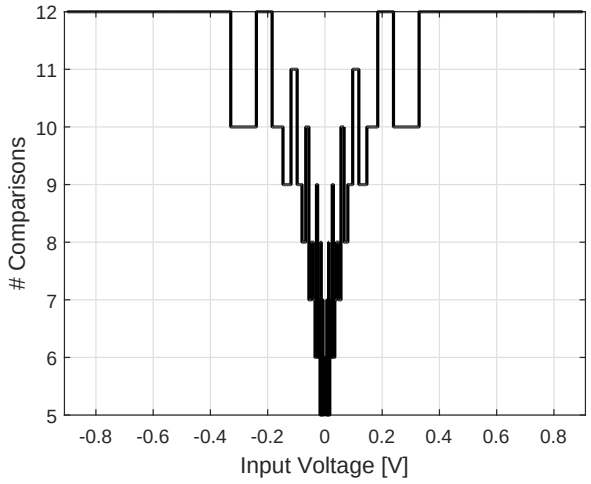


Figure 5.25: Number of comparisons *vs* V_{in}.

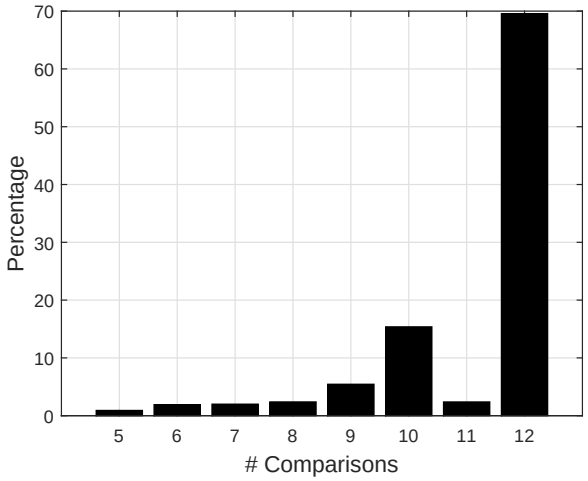


Figure 5.26: Percentage of comparisons.

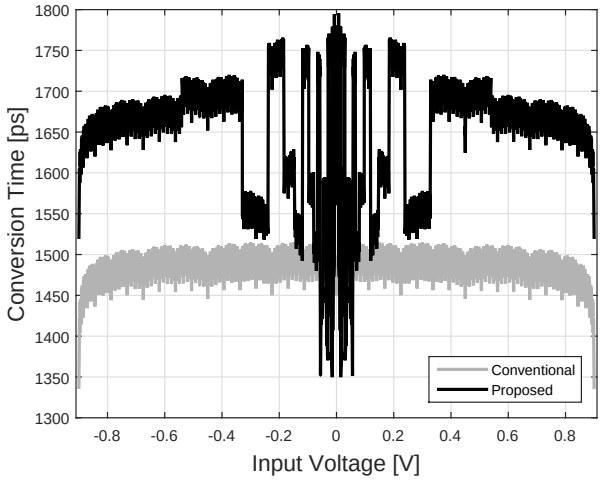


Figure 5.27: Conversion time *vs* V_{in}.

From the comparison between the traditional successive approximation converter and the proposed system in terms of conversion time performed in Figure 5.27, it can be concluded that the proposed architecture requires more time to complete a full conversion unless the differential signal is very small (approximately 10 mV). This can be explained by the latency of the TDC, which is significant, as depicted in Figure 5.19. The small voltage window for which the proposed converter is faster corresponds to the voltage range in which the TDC provides more voltage resolution and less comparisons are needed. In this case, the TDC latency is smaller than the time required to perform more comparisons, thus the reduced conversion time. Since this simulation did not take into account the DAC settling time, it can be assumed that the proposed converter requires, at maximum, 2 ns to perform a full conversion, which translates into a maximum sampling frequency of 500 MHz.

5.4.1 Energy

In this subsection, the energy consumption of the Conventional Switching, Figure 5.28, Vcm-based (MCS), Figure 5.29, and Charge Sharing, Figure 5.30, switching schemes are compared with the proposed system using the same switching schemes for the successive approximation algorithm. Although Charge Sharing architectures have not been deeply emphasized in this work, modelling their energy consumption is straightforward as they simply need energy to pre-charge the capacitor array, therefore the energy required by these architectures is signal independent and proportional to CV^2.

It should be mentioned that the these results were obtained considering a 12 bit ADC with C_{unit} of $1fF$, $0.9V$ as the reference voltage and a capacitor mismatch with $\sigma = 1.5\%$. For all the switching schemes, the *Total Energy* includes the DAC and the comparator energy. The *Total Energy* in the proposed architecture takes into account the DAC energy, considering that several bits are programmed at once, the comparator energy, for the

comparisons performed, and the TDC energy.

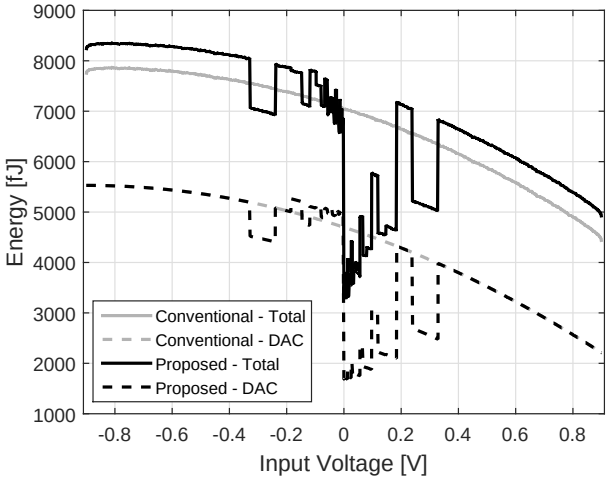


Figure 5.28: Conventional Architecture and Proposed Architecture using the Conventional Switching scheme *vs* V_{in}.

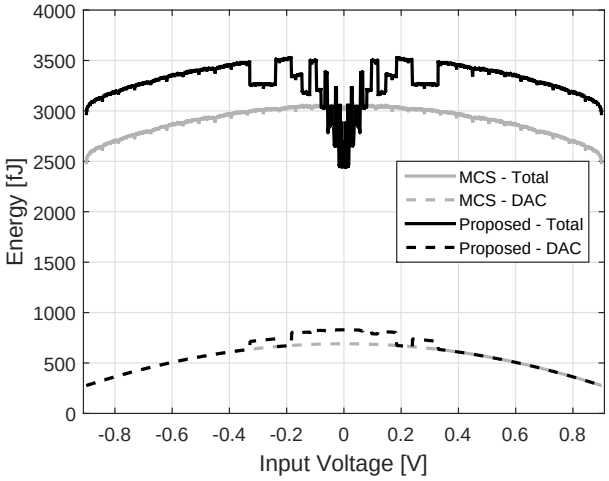


Figure 5.29: Vcm-based Architecture and Proposed Architecture using the Vcm-based Switching scheme *vs* V_{in}.

By analysing the *DAC Energy* curves from Figure 5.28, the input signal range in which only 1 bit is being programmed in the DAC is easily identified since the two lines are overlap. When the TDC provides more than 1 bit, two different situations occur. If the differential input signal is negative (and close to zero), the energy required by the proposed architecture DAC to program several bits at the same time is greater than when the Conventional switching algorithm is used. The reason for this is that no charge recycling takes place. Notice that, at approximately $-0.3V$, the DAC energy consumption of the proposed architecture is lower than the conventional due to the MSB-1 capacitor not being switched. In case the differential input signal is positive, the proposed architecture strongly benefits from using the TDC since several bits are programmed at once but no

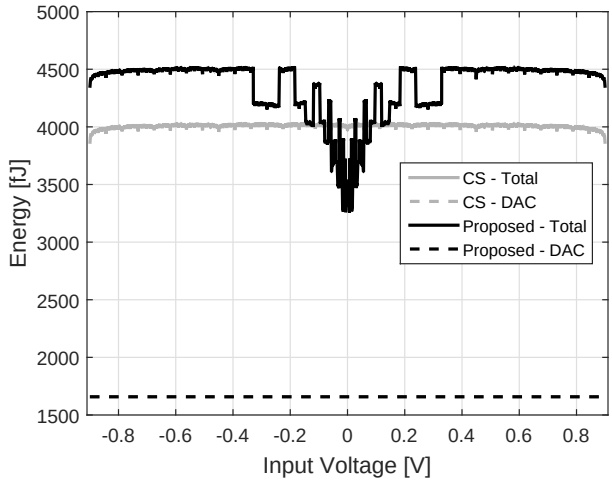


Figure 5.30: Charge Sharing Architecture and Proposed Architecture using the Charge Sharing Switching scheme *vs* V_{in}.

switching occurs in the most significant capacitors due to the DAC architecture. Evaluating, now, the *Total Energy* lines, the proposed converter requires less energy than the conventional architecture when the input signal is positive and close to zero. In these conditions, the proposed converter benefits from the DAC architecture and the TDC providing several bits, consequently fewer comparisons are performed. When the input signal is negative but close to zero, although the proposed converter may benefit from the TDC usage, since the DAC consumes more energy, the benefits are not so pronounced or even none. In case input signal is large and the TDC only *"decides"* 1 bit, the proposed architecture consumes more energy since, although the energy required by the DAC and the comparator are the same as in the Conventional architecture, the TDC energy has be to taken into account.

From Figure 5.29, it can be observed that the energy consumption is signal dependent, as in the case of the Conventional architecture. However, as explained in Chapter 3, the energy is symmetric. The signal range in which only 1 bit is being *decided* in the time domain is, as in the previous case, identified by analysing the DACs energy consumption. In the proposed architecture making use of the Vcm-based switching, the energy required by the DAC is never inferior to the Vcm-based architecture since there's always some switching action required. The *Total Energy* required by the proposed architecture is greater than the simple Vcm-based architecture, except for the small signal range in which the TDC provides several bits and considerably less comparisons are used. Notice that the offset present between the two *Total Energy* curves when only 1 bit is resolved by the TDC corresponds to the TDC energy consumption, as depicted in Figure 5.20.

The energy consumed by the DACs when Charge Sharing is used is the same, Figure 5.30, since the energy is used to pre-charge the DAC arrays and is signal independent. When Charge Sharing schemes are used, the DAC energy can be decreased by utilizing more complex pre-charging algorithms but this often requires more clock cycles. The

conclusions about *Total Energy* of the proposed system using Charge Sharing are similar to those relative to the Vcm-based architecture.

Notice that the DAC energy could be decreased, in the Conventional and Vcm-based proposed architectures, by programming only 1 bit at once. This would force the maximum DAC energy to be equal to the traditional implementations but extra clock cycles would be needed, hence more energy required in the clock circuit. Additionally, the conversion time would increase, which would decrease the maximum sampling frequency.

These results demonstrate that the Vcm-based approach is the most appropriate for the proposed system, since its energy consumption is the smallest among the three tested architectures. From the *Total Energy* curves, it can be concluded that the proposed system is suitable for *quasi-static* signals, such as biomedical signals. In this case, the proposed system could benefit from the implementation of the *Bypass Window*, as demonstrated in 5.2. However, special care has to be taken to make sure the energy consumption is not excessive in case the input signal goes out of the predefined window since the TDC would have to be used twice. Moreover, the DAC architecture would need to be slightly modified in order to store the energy relative to the MSBs of the previous conversion to be further subtracted to the next signal.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

Successive Approximation data converters based on Charge-Redistribution have been increasing their popularity due to their suitability for moderate speed, medium resolution and very low-power applications. This is achieved because their analog complexity is kept low. Since most of the circuits are digital, SAR ADCs benefit from technology scaling and can be used at very low supply voltages, which contributes to their low-power operation. However, with technology scaling and voltage supply reduction, the design of analog circuits becomes more challenging as the noise levels do not decrease proportionally and keeping the transistors working in saturation and still maintaining enough voltage headroom is difficult. Therefore, the objective behind this thesis was to study how the time domain information could be used to increase the performance of Successive Approximation Analog-to-Digital Converters.

To do so, a new architecture was proposed in this thesis, in which a TDC is introduced into the traditional SAR ADC architecture to measure the comparator's time response. Since the comparator's time response is signal dependent, a TDC can be used to quantize the delay between the clock signal and the comparator's output. This time domain information was then used to create *Lookup Tables* which are used by the proposed system to approximate up to 9 MSBs with a single comparison, depending on the input signal range. Moreover, since the MSBs are solved in the time domain, the successive approximation algorithm does not take wrong decisions with these bits, thus energy is not wasted.

A single-ended high-level model of the proposed converter with 12 bit resolution was implemented in MATLAB which allowed to verify that the time domain information can be used decrease the number of comparisons (and clock cycles) necessary. This model was further extended to incorporate a time domain *Bypass Window*. The *Bypass Window*

extends the use of the TDC by using it to verify if the sample under conversion is close to the previous one. If that is the case, the SAR algorithm is only used to solve the LSBs and power is saved since no switching is made on the DAC's MSBs. If the signal goes out of the pre-defined window, the conversion starts using the previous algorithm in which the TDC is only used to solve the MSBs. Since the *Bypass Window* can be controlled digitally, the system can be tuned taking into account the input signal's characteristic. It was demonstrated that proper tuning of the time window allows to significantly reduce the number of comparisons needed, hence benefits on the power consumption of the converter are expected, as long as the TDC and subsequent digital mapping logic are kept low in a CMOS implementation. The controllability of the *Bypass Window* makes this architecture suitable to operate with *quasi-static* signals, such as biomedical signals. If the signal is slowly varying over time, it is expected that the sample under evaluation is close to the previous conversion, hence the number of comparisons needed to solve 12 bits is reduced.

In order to develop a more realistic model of the system, the comparator and the TDC were designed in 65nm ST Microelectronics CMOS Technology, in Cadence's design environment, and their characteristics (timing information, energy requirements, etc.) were included in the MATLAB high-level models. The comparator was based on the *Double-Tail* Comparator since it presents several advantages when compared to other architectures. The *Vernier Delay-Line* was the architecture chosen for the TDC implementation as its design is not very complex, due to being a modular structure, and achieves sub-gate resolution. Electrical simulations from these blocks showed that the comparator's time characteristic limits the voltage range in which the TDC can convert several bits in the voltage domain. The resolution of the TDC could be further increased in order to obtain a greater voltage resolution. This, however, would lead to an increase in the power consumption of this block. Another important aspect was the latency exhibited by the TDC, which has influence in the maximum sampling frequency of the system. By analysing the energy consumption of both circuits, it could be concluded that, although the TDC consumes more energy than the comparator, as long as it is able to solve more than 4 bits in the voltage domain, its usage benefits the proposed system in terms of energy-efficiency. Moreover, due to being constituted only by digital gates, it benefits from technology scaling therefore its performance, in terms of energy, is expected to increase, if more advanced technology nodes are used.

Finally, fully-differential models of the system were implemented, using the *Conventional* and the *Vcm-based* switching methods, and incorporating real circuit's characteristics. The DAC energy was also modulated according to the methodology described in Chapter 3. Although more benefits, when compared to the traditional implementations, were obtained using the *Conventional* switching method, its total energy consumption was greater than that obtained when using the *Vcm-based* switching technique, as expected, according to Chapter 3. The total energy of the proposed system was higher than the traditional approaches due to the TDC energy and the voltage domain in which it can

only solve 1 bit being too large. When the TDC was able to solve several bits and fewer comparisons needed, the total energy obtained using the proposed converter was lower than that using traditional techniques. This proves that the system could benefit from the implementation of the *Bypass Window*, as long as the TDC energy and consequent mapping logic are kept low, as mentioned before. This functionality was not implemented in the fully-differential model because the DAC architecture would need to be modified in order to store the energy of the MSBs from the previous conversion and modulating a new DAC architecture would be very time consuming. In terms of conversion time, the proposed system's performance is also poorer than when traditional architectures are used. The reason for this is, again, the large voltage range in which the TDC is only able to solve 1 bit in the voltage domain.

Summarizing, the proposed architecture does not achieve better performances, nor in terms of energy, nor in terms of conversion time, when compared to more traditional implementations, especially due to the TDC energy and latency and the large voltage range where it is only capable of solving 1 bit in the voltage domain.

6.2 Future Work

The TDC's characteristics, namely its energy consumption and latency, are a major bottleneck on the performance of the proposed architecture. The energy consumption can be minimized by freezing the delay lines when the output code is found, which prevents subsequent stages to change their output, whereas pipelining decreases latency.

The number of stages of the TDC could also be optimized, taking into account the time response of the comparator and the benefits obtained by having more or less delay stages.

Since the comparator's time response is very fast when the differential input signal is large, more effort should be put in the first stages of the TDC in order to increase its time resolution so that its voltage resolution increases as well. This could be done by designing a non-linear TDC, with greater resolution in the first stages or using a *Coarse-Fine* TDC.

Finally, it would be interesting to implement the *Bypass Window* in the fully-differential architecture and verify if the benefits predicted from the single-ended implementation still hold.

Bibliography

[1] G. Y. Huang, S. J. Chang, C. C. Liu, and Y. Z. Lin. "A 1-μW 10-bit 200-kS/s SAR ADC with a bypass window for biomedical applications". In: *IEEE Journal of Solid-State Circuits* 47.11 (2012), pp. 2783–2795. ISSN: 00189200. DOI: 10.1109/JSSC.2012.2217635.

[2] J. L. McCreary and P. R. Gray. "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques—Part I". In: *IEEE Journal of Solid-State Circuits* 10 (1975), pp. 371–379. ISSN: 0018-9200. DOI: 10.1109/JSSC.1975.1050629.

[3] M. J. Pelgrom. *Analog-to-Digital Conversion*. New York, NY: Springer New York, 2013, pp. 197–201. ISBN: 978-1-4614-1370-7. DOI: 10.1007/978-1-4614-1371-4. arXiv: arXiv:1011.1669v3. URL: http://link.springer.com/10.1007/978-1-4614-1371-4.

[4] M. Saberi, R. Lotfi, K. Mafinezhad, and W. A. Serdijn. "Analysis of power consumption and linearity in capacitive digital-to-analog converters used in successive approximation ADCs". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 58.8 (2011), pp. 1736–1748. ISSN: 15498328. DOI: 10.1109/TCSI.2011.2107214.

[5] R. Kapusta, J. Shen, S. Decker, H. Li, E. Ibaragi, and H. Zhu. "A 14b 80 MS / s SAR ADC With 73 . 6 dB SNDR in 65 nm CMOS". In: *Ieee Journal of Solid-State Circuits* 48.12 (2013), pp. 3059–3066. ISSN: 0018-9200. DOI: 10.1109/JSSC.2013.2274113.

[6] M. R. Jan, C. Anantha, and N Borivoje. *Digital Integrated Circuits–A Design Perspective*. Prentice-Hall, 2002.

[7] Y. Xu and A. Shabra. "A Flash-TDC Hybrid ADC Architecture". In: *Proceedings - IEEE International Symposium on Circuits and Systems* 2015-July.1 (2015), pp. 1270–1273. ISSN: 02714310. DOI: 10.1109/ISCAS.2015.7168872.

[8] H. Wei, C. H. Chan, U. F. Chio, S. W. Sin, U. Seng-Pan, R. P. Martins, and F. Maloberti. "An 8-b 400-ms/s 2-b-per-cycle sar adc with resistive dac". In: *IEEE Journal of Solid-State Circuits* 47.11 (2012), pp. 2763–2772. ISSN: 00189200. DOI: 10.1109/JSSC.2012.2214181.

[9] D. A. Johns and K. Martin. *Analog Integrated Circuit Design*. John Wiley & Sons, 2008.

[10] H. Nyquist. "Certain topics in telegraph transmission theory". In: *Proceedings of the IEEE* 90.2 (2002), pp. 280–305. ISSN: 00189219. DOI: 10.1109/5.989875. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=989875.

[11] C. E. Shannon. "A Mathematical Theory of Communication". In: *Bell System Technical Journal* 27.3 (1948), pp. 379–423. ISSN: 1538-7305. DOI: 10.1002/j.1538-7305.1948.tb01338.x. URL: http://dx.doi.org/10.1002/j.1538-7305.1948.tb01338.x.

[12] C. E. Shannon. "Communication in the presence of noise". In: *Proceedings of the IRE* 37.1 (1949), pp. 10–21.

[13] M. Yip and A. P. Chandrakasan. "A resolution-reconfigurable 5-to-10-bit 0.4-to-1 v power scalable SAR ADC for sensor applications". In: *IEEE Journal of Solid-State Circuits* 48.6 (2013), pp. 1453–1464. ISSN: 00189200. DOI: 10.1109/JSSC.2013.2254551.

[14] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin. "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure". In: *IEEE Journal of Solid-State Circuits* 45.4 (2010), pp. 731–740. ISSN: 00189200. DOI: 10.1109/JSSC.2010.2042254.

[15] A. M. Abo and P. R. Gray. "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter". In: *IEEE Journal of Solid-State Circuits* 34.5 (1999), pp. 599–606. ISSN: 00189200. DOI: 10.1109/4.760369.

[16] Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, R. P. Martins, and F. Maloberti. "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS". In: *IEEE Journal of Solid-State Circuits* 45.6 (2010), pp. 1111–1121. ISSN: 00189200. DOI: 10.1109/JSSC.2010.2048498.

[17] M. Van Elzakker, E. Van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta. "A 10-bit charge-redistribution ADC consuming 1.9 μw at 1 MS/s". In: *IEEE Journal of Solid-State Circuits* 45.5 (2010), pp. 1007–1015. ISSN: 00189200. DOI: 10.1109/JSSC.2010.2043893.

[18] T. Rabuske and J. Fernandes. *Charge-Sharing SAR ADCs for Low-Voltage Low-Power Applications*. Analog Circuits and Signal Processing. Cham: Springer International Publishing, 2017. ISBN: 978-3-319-39623-1. DOI: 10.1007/978-3-319-39624-8.

[19] Y. Yee, L. Terman, and L. Heller. "A two-stage weighted capacitor network for D/A-A/D conversion". In: *IEEE Journal of Solid-State Circuits* 14.4 (1979), pp. 778–781. ISSN: 0018-9200. DOI: 10.1109/JSSC.1979.1051264. URL: http://ieeexplore.ieee.org/xpls/abs{_}all.jsp?arnumber=1051264.

[20] B. P. Ginsburg and A. P. Chandrakasan. "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC". In: *IEEE Journal of Solid-State Circuits* 42.4 (2007), pp. 739–747. ISSN: 00189200. DOI: 10.1109/JSSC.2007.892169.

[21] Y. K. Chang, C. S. Wang, and C. K. Wang. "A 8-bit 500-KS/s low power SAR ADC for bio-medical applications". In: *2007 IEEE Asian Solid-State Circuits Conference, A-SSCC* 2 (2007), pp. 228–231. DOI: 10.1109/ASSCC.2007.4425772.

[22] C. Liu, S. Chang, G.-Y. Huang, and Y.-Z. Lin. *A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 µm CMOS process*. 2009. URL: http://ieeexplore.ieee.org/xpls/abs{_}all.jsp?arnumber=5205343.

[23] V. Hariprasath, J. Guerber, S.-H. Lee, and U.-K. Moon. "Merged capacitor switching based SAR ADC with highest switching energy-efficiency". In: *Electronics Letters* 46.9 (2010), p. 620. ISSN: 00135194. DOI: 10.1049/el.2010.0706.

[24] C. Yuan and Y. Lam. "Low-energy and area-efficient tri-level switching scheme for SAR ADC". In: *Electronics Letters* 48.9 (2012), p. 482. ISSN: 00135194. DOI: 10.1049/el.2011.4001.

[25] J. Fredenburg and M. P. Flynn. "ADC trends and impact on SAR ADC architecture and analysis". In: *Proceedings of the Custom Integrated Circuits Conference* 2015-Novem (2015), pp. 1–8. ISSN: 08865930. DOI: 10.1109/CICC.2015.7338380.

[26] B. Murmann. *ADC Performance Survey 1997-2016*. 2016. URL: http://web.stanford.edu/{~}murmann/adcsurvey.html.

[27] C. H. Chan, Y. Zhu, S. W. Sin, U. Seng-Pan, and R. P. Martins. "A 5.5mW 6b 5GS/S 4×-lnterleaved 3b/cycle SAR ADC in 65nm CMOS". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference* (2015), pp. 466–468. ISSN: 01936530. DOI: 10.1109/ISSCC.2015.7063128.

[28] C. C. Lee and M. P. Flynn. "A SAR-assisted two-stage pipeline ADC". In: *IEEE Journal of Solid-State Circuits* 46.4 (2011), pp. 859–869. ISSN: 00189200. DOI: 10.1109/JSSC.2011.2108133.

[29] M. Ranjbar, A. Mehrabi, O. Oliaei, and F. Carrez. "A 3.1 mW continuous-time ΔΣ modulator with 5-bit successive approximation quantizer for WCDMA". In: *IEEE Journal of Solid-State Circuits* 45.8 (2010), pp. 1479–1491. ISSN: 00189200. DOI: 10.1109/JSSC.2010.2047423.

[30] J. A. Fredenburg and M. P. Flynn. "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC". In: *IEEE Journal of Solid-State Circuits* 47.12 (2012), pp. 2898–2904. ISSN: 00189200. DOI: 10.1109/JSSC.2012.2217874.

[31] Y. J. Chen, K. H. Chang, and C. C. Hsieh. "A 2.02-5.16 fJ/Conversion Step 10 Bit Hybrid Coarse-Fine SAR ADC With Time-Domain Quantizer in 90 nm CMOS". In: *IEEE Journal of Solid-State Circuits* 51.2 (2016), pp. 357–364. ISSN: 00189200. DOI: 10.1109/JSSC.2015.2492781.

[32] S. Henzler. *Time-to-Digital Converters*. Vol. 29. Springer Series in Advanced Microelectronics. Dordrecht: Springer Netherlands, 2010. ISBN: 978-90-481-8627-3. DOI: 10.1007/978-90-481-8628-0. arXiv: arXiv:1011.1669v3. URL: http://link.springer.com/10.1007/978-90-481-8628-0.

[33] R. B. Staszewski, J. L. Wallberg, S. Rezeq, C. M. Hung, O. E. Eliezer, S. K. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M. C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold. "All-digital PLL and transmitter for mobile phones". In: *IEEE Journal of Solid-State Circuits* 40.12 (2005), pp. 2469–2480. ISSN: 00189200. DOI: 10.1109/JSSC.2005.857417.

[34] D. I. Porat. "Review of sub-nanosecond time interval measurements". In: *IEEE Transactions on Nuclear Science* NS-20 (1973), pp. 36–51. ISSN: 0018-9499. DOI: 10.1109/TNS.1973.4327349.

[35] R. Nutt. "Digital time intervalometer". In: *Review of Scientific Instruments* 39.9 (1968), pp. 1342–1345. ISSN: 00346748. DOI: 10.1063/1.1683667.

[36] J. Yu, F. F. Dai, and R. C. Jaeger. "A 12-bit Vernier Ring Time-to-Digital Converter in 0.13 μm CMOS Technology". In: *IEEE Journal of Solid-State Circuits* 45.4 (2010), pp. 830–842.

[37] T. E. Rahkonen and J. T. Kostamovaara. "The Use of Stabilized CMOS Delay Lines for the Digitization of Short Time Intervals". In: *IEEE Journal of Solid-State Circuits* 28.8 (1993), pp. 887–894. ISSN: 1558173X. DOI: 10.1109/4.231325.

[38] P. Dudek, S. Szczepański, and J. V. Hatfield. "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line". In: *IEEE Journal of Solid-State Circuits* 35.2 (2000), pp. 240–247. ISSN: 00189200. DOI: 10.1109/4.823449.

[39] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel. "A local passive time interpolation concept for variation-tolerant high-resolution time-to-digital conversion". In: 43.7 (2008), pp. 1666–1676.

[40] P. Chen, S. I. Liu, and J. Wu. "A CMOS pulse-shrinking delay element for time interval measurement". In: *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 47.9 (2000), pp. 954–958.

[41] M. Lee and A. a. Abidi. "A 9b, 1.25ps Resolution Coarse-Fine Time-to-Digital Converter in 90nm CMOS that Amplifies a Time Residue". In: *IEEE Symposium on VLSI Circuits, Digest of Technical Papers* (2007), pp. 68–69.

[42] S. Babayan-Mashhadi and R. Lotfi. "Analysis and design of a low-voltage low-power double-tail comparator". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 22.2 (2014), pp. 343–352. ISSN: 10638210. DOI: 10.1109/TVLSI.2013.2241799.

[43] S. Jeong, W. Jung, D. Jeon, O. Berenfeld, H. Oral, G. Kruger, D. Blaauw, and D. Sylvester. "A 120nW 8b sub-ranging SAR ADC with signal-dependent charge recycling for biomedical applications". In: *IEEE Symposium on VLSI Circuits, Digest of Technical Papers* 2015-Augus (2015), pp. C60–C61. DOI: 10.1109/VLSIC.2015.7231327.

[44] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers. "Matching Properties of MOS Transistors". In: *IEEE Journal of Solid-State Circuits* 24.5 (1989), pp. 1433–1439. ISSN: 1558173X. DOI: 10.1109/JSSC.1989.572629.