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Mestre

Low Phase-Noise CMOS RC Oscillator for RF Applications

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"We live on an island surrounded by a sea of ignorance. As our island of knowledge grows, so does the shore of our ignorance."

- John Archibald Wheeler

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Abstract

This thesis presents and discusses an approach to improve the performance of the RC oscillator, for operation in high frequency. This is achieved with the implementation of a fully integrated injection-locked oscillator (ILO), which consists in the direct injection of a reference signal into the oscillator circuit. This strategy allows to improve the phase noise of the RC oscillator, with a compromise between cost, area and energy consumption, better than the one that is obtained when considering the typical approach of using a phase-locked loop (PLL) structure. One of the inherent challenges in this approach comes from the reference generator, especially if full integration and high frequency operation is desired. The Spin torque oscillator (STO) structure was considered for being the generator reference. However, as these structures produce weak outputs, often below -40 dBm, the bandwidth where the oscillator is able to track the reference is narrow. This conditioned the circuit design, which had to be addressed by means of a two step design methodology in order to properly improve the phase-noise at all frequency offsets. The improvement of the close-in phase-noise of the oscillator, dominated by flicker noise, was done by resorting to harmonic synchronization and the remote offsets, which are dominated by white noise, were corrected with design optimizations of the oscillator, which includes circuit modifications and design guidelines. Two prototypes were fabricated to validate each of the steps. Measurement results of a prototype of an ILO demonstrated that the use of harmonic synchronization allowed the correction of the phase-noise up to a 10 MHz offset with a reference power of -50 dBm; the measurement results of a modified relaxation oscillator showed a phase-noise of -124 dBc/Hz at a 10 MHz offset, while achieving a closer-to-optimal figure-of-merit (FoM) of -162 dBc/Hz.The gained insight was used to drive the design of a high frequency and high performance ILO. Simulation results, for a frequency of 2.4 GHz, showed that by using a second order harmonic synchronization on a modified relaxation oscillator, and considering that the reference phase-noise is comparable to the typical values for an LC oscillator, it was possible to obtain an RC oscillator that presents FoM values more consistent with the theoretical optimum.

It was observed the reduction of the existent performance gap of the RC oscillator to the LC oscillator to roughly 10 dB, which is a relevant result taking into account the frequency of operation.

Keywords

RC Oscillators, phase-noise, injection-locking, harmonic synchronization, figure-of-merit, Radio-frequency, GHz range.

Resumo

Esta tese apresenta e valida uma abordagem por forma a melhorar a performance dos osciladores RC, para operação a alta frequência, por via da implementação de um oscilador sincronizado por injeção totalmente integrado, o qual consiste na injeção direta de um sinal de referência no circuito do oscilador. Esta estratégia permite melhorar o ruído de fase do oscilador RC, com um melhor compromisso entre custo, área e consumo de energia, quando comparando com a abordagem típica em que se usa uma PLL. Um dos desafios inerentes a esta abordagem relaciona-se com o gerador do sinal de referência, especialmente se integração completa e operação a alta frequência são desejáveis. Um oscilador de transferência de spin foi considerado para referência, contudo, porque estas estruturas produzem sinais de baixa potência, usualmente abaixo de -40 dBm, a banda de captura do oscilador é estreita. Isto condicionou o projeto do circuito o qual teve de ser abordado em duas etapas, por forma a garantir a correção do ruído de fase em todos os offsets. A correcção do ruído em offsets próximos da frequência de oscilação, que são dominados por ruído de "flicker", foi efetuada recorrendo a sincronização harmónica e os "offsets" mais distantes , que são dominados por ruído branco, são corrigidos com optimizações ao nível de projecto do oscilador, as quais incluíram modificações do circuito e orientações de projecto. Por forma a validar cada um dos passos, dois protótipos foram fabricados. Os resultados obtidos para um oscilador sincronizado por injecção demonstraram que o uso de injecção harmónica permitiu a correção do ruído de fase até um offset de 10 MHz com uma potência de injeção de -50 dBm; os resultados obtidos para um oscilador de relaxação modificado indicaram um ruído de fase de -124 dBc/Hz num offset a 10 MHz ao mesmo tempo que uma figura de mérito de -162 dBc/Hz próxima do ótimo teórico foi garantida. Os resultados serviram como base para orientação de um projecto de um oscilador sincronizado por injeção de alta performance capaz de operar a alta frequência. Resultados de simulação, para uma frequência de 2.4 GHz, mostram que usando injeção harmonica de segunda ordem num oscilador de relaxação modificado, e considerando que o ruído de fase da referência é comparável aos valoes típicos para um oscilador LC, é possível obter um oscilador RC capaz de apresentar valores de figura de mérito mais consistentes com os óptimos teóricos.

É observada a redução da diferença de performance do oscilador RC para o oscilador LC para cerca de 10 dB, o que é relevante tendo em conta a frequência de operação.

Palavras Chave

Osciladores RC, ruído de fase, sincronismo por injecção, sincronização harmónica, factor de mérito.

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List of Acronyms

ADC analogue-to-digital converter. 11

CMOS complementary metal-oxide-semiconductor. 10, 25, 67, 68, 71, 126

FoM figure-of-merit. v, 28, 88, 102, 106, 114, 115, 119, 120, 127

GMR giant magnetoresistance. 67

IF intermediate-frequency. 11, 12, 14
IIP2 input referred second-order intercept point. 12
ILO injection-locked oscillator. v, xiv, 3–6, 46, 47, 50, 51, 55–57, 61, 62, 68, 69, 72, 76, 86, 87, 120, 126–128
IoT internet-of-things. 15, 126
IRF image reject filter. 11
ISF input sensitivity function. 19–21, 53–56
ISM industrial, scientific and medical. 5, 15, 71

LF loop filter. 44, 45
LO local oscillator. 10, 11, 14

MOS metal-oxide-semiconductor. 17
MTJ STO magnetic tunnel junction spin torque oscillator. 67

NFC near field communication. 15
NL non-linear. 21, 26, 29, 37, 57, 76, 82, 126

PD phase detector. 44, 45
PDR phase-domain response. 55, 56
PLL phase-locked loop. v, 2–4, 44–46, 50, 53
PSD power spectral density. 17, 18
PSS periodic steady-state. xiv, 76, 77, 79

QAM quadrature amplitude modulation. 15
QL quasi-linear. 21, 26, 35–37, 57, 76, 87, 90, 126
QPSK quadrature phase-shift keying. 15

RF radio-frequency. 10, 25

SSB single side-band. 17
STO Spin torque oscillator. v, 3–5, 62, 65, 67–69, 71, 90, 93, 98, 120, 126, 127
STT Spin transfer torque. 65, 67
SV STO Spin valve spin torque oscillator. 67

TMR tunneling magnetoresistance. 67

VCO voltage-controlled oscillator. 44, 45

WSN wireless sensor network. 15

1

Introduction

Preamble

This chapter reveals the motivation and main objective of this thesis. It includes an overview of the design approach and summarizes the thesis outline and the original contributions.

Contents

1.1 Motivation

RC oscillators are widely used in applications where cost and area are major constraints, for instance, in disposable sensors for biomedical applications or wireless sensor networks (integrated inductors alone occupy comparable area to the one of an entire RC oscillator) [1, 2]. However, the extent of their applicability is constrained by their high phase-noise.

The operation principle of RC oscillators relies on the charge/discharge of an RC circuit. The implications of having a resistor relates mostly to noise, the noise induces phase-modulation that leads to the appearance of side-bands around the fundamental frequency (phase-noise) in the output spectrum of the oscillator [3]. LC oscillators, by its side, not only have a lower noise contribution on the account of their reduced resistive elements, typically parasitics, but they also present narrower side-bands, on the account of their operation principle being based on a resonant mechanism. Since they have lower phase-noise they tend to be the common adopted topology in modern transceivers [4].

The performance gap between both topologies becomes even more pronounced as the frequency of operation is increased. The performance of the RC oscillator tends to degrade, whereas the one of LC oscillators actually improves (at least while the frequency of operation is below the self-resonating frequency of the inductor) [5, 6].

Since the widespread use of portable devices and wireless communications, has led to an increase in the occupation of the spectrum, there is a constant necessity to use higher data rates and frequencies, which unfortunately limits the adoption of RC oscillators. Nevertheless, due to their many useful characteristics a continuous effort has been devoted to the development of mechanisms suitable to improve the performance of the RC oscillators. The implementation of frequency synthesizers allows the extension of their applicability to a wider range of standards (in terms of frequency of operation and phase-noise).

The applicability of the RC oscillators can be extended by implementing a PLL, which is a feedback circuit that allows precise frequency generation (as shown in Fig. 1.1(a)). However, the implementation of this structure comprehends an overhead in the circuit area, and power consumption of the transceiver [5, 7]. In addition, because it is a feedback structure it raises two issues concerning the synchronization time and stability issues, which often requires a complex and careful design.

Frequency synthesizers based on Injection-locking are a viable alternative to improve the performance of the RC oscillator (Fig. 1.1(b)) [8, 9]. The direct injection of a signal in a given node of the oscillator can be used for synchronization, and a performance comparable to the one of a PLL, can be obtained, without its drawbacks [10]. The main advantage of this approach relates the fact that these frequency synthesiz-

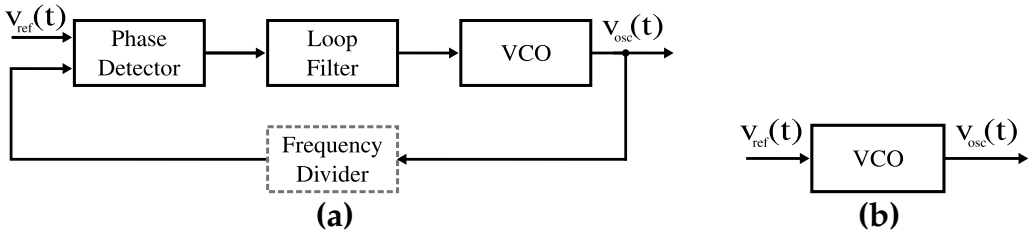

Figure 1.1: Frequency synthesizers: (a) Phase-locked loop. (b) Injection-locking.

ers can be implemented with lesser effort as they exempt the use of additional blocks, besides the oscillator itself. This approach also allows to disregard the associated concern with the used of a feedback structure; the loop instability.

This approach, unlike what is seen for the PLL, requires a reference capable of operating in the same range of frequencies of the oscillator, which poses a problem if radio-frequency operation is the target. Two options can be discussed to be used as reference generator, a crystal and a Spin torque oscillator [11–15]. If operation in the GHz range is intended, the crystal is not a viable solution on the account of its reduced frequency of operation (a couple hundred MHz). In addition, the use of the crystal does not impairs flexibility to the synthesizers, since the crystal produces a fixed frequency. In terms of tunability, an injection-locked oscillator (ILO) with a crystal as frequency generator would not offer great advantage to the PLL, since the PLL can be programmed to perform frequency hopping by adjustment of the frequency divider in the feedback loop (see Fig. 1.1(a)).

The other alternative is to use a STO, this is a relatively new structure and still under on-going research. This structure is able of sustaining oscillations in the GHz range with large tunability and its fabrication is compatible with standard silicon process. The use of this reference should allow to implement a fully integrated wide-range and high performance ILO suitable for multi-standard applications.

1.2 Research question

Is it possible to improve the performance of CMOS RC oscillators, at high frequency of operation, by implementing a frequency synthesizer without a strong penalty on the overall cost, area, energy consumption and design complexity?

1.3 Design of an ILO with a weak reference

This work presents a study on the implementation and design of a ILO based on a RC oscillator. The phase-noise of an injection-locked oscillator has a shape identical to the one that is seen when using a PLL structure (see Fig. 1.2), inside the locking

range (gives respect to the maximum offset frequency where the oscillator is able to track the reference) of the PLL/ILO the phase-noise is dominated by the reference. However, whereas the locking range of the PLL it is constrained by the loop filter, in the case of the injection-locked oscillator it is constrained by the amplitude of the reference signal [5, 7–9, 16].

One typical approach used when implementing an ILO is to design the free-running oscillator with the minimum power consumption possible [17]. Usually there is a trade-off between power consumption and noise, which implies that a design strategy of reducing the power consumption will most likely cause the degradation of the phase-noise. Afterwards the noise improvement is obtained with synchronization by injection. However, this sort of approach is not compatible with the use of the STO. One of the drawbacks of the STO structure is their weak outputs, which limit the locking range hence the noise improvement throughout the full extent of the oscillator sideband (as shown in Fig. 1.2).

In the event of weak injection, the frequency band where noise is improved is reduced, which means a complementary step should be considered to improve the remaining offsets. Therefore, it is recommended for the ILO to be designed following a two-step methodology in order to correct the phase-noise at all offsets as following (see Fig. 1.2):

1. Use weak injection to correct close-in phase-noise.

2. Determine and implement design optimizations to minimize the phase-noise of the RC oscillator at the further offsets.

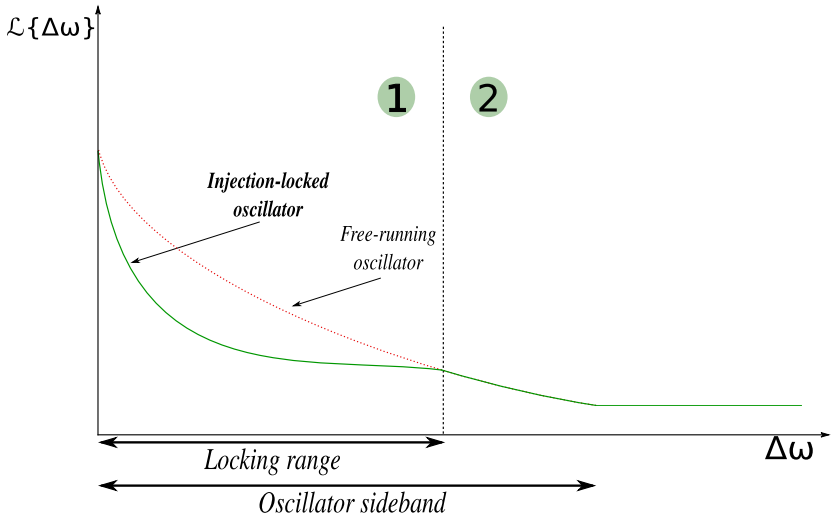

Figure 1.2: Sideband phase-noise of the injection-locked oscillator.

The relaxation oscillator is going to be considered as the base circuit in view of its higher theoretical performance and its number of injection points [18, 19]. The higher theoretical performance is relevant in order to obtain correction of the phase-noise at the limits of the sideband with good compromise between frequency of operation, energy consumption and noise. The existence of multiple injection points allows to test and validate different injection schemes with the purpose of improving the impact of the reference signal over the oscillator. The design will be validated for a frequency of 2.4 GHz, which is an high frequency channel of the industrial, scientific and medical (ISM) bands, where RC oscillators are of great interest on the account of their low cost and area, but it should also be demonstrated the validity for other standards frequencies.

One important remark concerns the difficulty in obtaining project equations. The description of the synchronization mechanism is of complex nature, specially if the oscillator to be synchronized relies on non-linearities to operate as in the case of the RC oscillator. Therefore, the implementation should based on simplified design guidelines.

Finally, the design validation should have a high level of independence to the integration of the reference. STO are still under research and the fabrication process is still being improved.

1.4 Thesis organization

The thesis is organized in 7 chapters as follows:

Chapter 2 - Background on CMOS RC Oscillators: In this chapter the desirable characteristics of the oscillator in order to cope with the requirements of the modern receiver topologies are discussed. The two existent mechanisms used to implement electric oscillators are introduced as well as some general ideas on the typical high frequency CMOS RC oscillator topologies. Their performance in terms of the trade-off between energy consumption and phase-noise is also addressed.

Chapter 3 - Injection-locking of CMOS Oscillators: In this chapter the phenomena of injection-locking is described and the synchronization models are presented.

Chapter 4 - Design of an ILO Based on an RC Oscillator: In this chapter the challenges involved in the implementation of an ILO are discussed. It concludes on the most suitable design approach taking into account the available references and the oscillator circuit.

Chapter 5 - Weak Injection in an RC Oscillator: In this chapter a qualitative study of synchronization by injection in an RC oscillator is presented. Design guidelines are considered to maximize the impact of the injected signal, and the minimum amplitude required for synchronization is determined.

Chapter 6 - High Performance RC Oscillator: In this chapter a modified relaxation oscillator circuit with high FoM at high frequency is presented. The performed modifications and design guidelines are discussed and validated.

Chapter 7 - Conclusions and Future Work: In this chapter the conclusions are presented as well as a brief discussion of future research directions..

1.5 Original contributions

Two new modified RC oscillator circuits capable of operating at a high frequency while exhibiting reduced phase-noise:

- Chapter 5: A methodology of simulation of ILO's to retrieve the locking range, and the dependency on the reference phase-noise are presented. An experimental evaluation of harmonic synchronization in RC oscillators using weak injection is also presented [20].
- Chapter 6: It is presented the study and design of a modified relaxation oscillator that has reduced phase-noise at higher offsets while operating at high frequency. The modifications also allowed the reduction of the relaxation oscillator performance gap to the theoretical optimum [21, 22].

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2

Background on CMOS RC Oscillators

Preamble

In this chapter the desirable characteristics of the oscillator in order to cope with the requirements of the modern receiver topologies are discussed. The two existent mechanisms used to implement electric oscillators are introduced as well as some general ideas on the typical high frequency CMOS RC oscillator topologies. Their performance in terms of the trade-off between energy consumption and phase-noise is also addressed.

Contents

Nowadays more and more devices are resorting to wireless communication for a number of purposes, from medical to recreation. However, extending this capability to a wide variety of devices is a challenge. Specially, taking into account that limitations exist in terms of battery life and available area. This means that constrains like integrability, low cost and low energy consumption are driving the work of the analogue designers. These impositions have been orienting the designers to develop fully on-chip receivers with multi-band selectivity and implemented in complementary metal-oxide-semiconductor (CMOS) technology [2, 6]. This set of characteristics open the way to the use of RC oscillators within the transceiver architecture on the account of their low cost, fairly easy implementation in CMOS technology and wide tuning range.

This chapter will try to offer a broad field of the context within which the work of this thesis was developed, by providing an insightful overview of CMOS RC oscillators. It will be detailed in what measure is the RC oscillator able to cope with nowadays design restrictions, when implementing receivers, and it will define the extent of their applicability. For that matter the RC oscillator will be presented as well as all the key related topics.

2.1 Wireless reception

radio-frequency (RF) transceivers should be able to be fully integrated, occupy the least possible area and be wideband. These restrictions however, take a bigger toll on the receiver design than on the transmitter due to a couple of issues that are a consequence of using open space as a propagation channel. The transmitted signal while traveling suffers from strong attenuation and reaches the receiver as a low power signal. Besides that the receiver antenna captures much more than the signal of interest, which means there is the problem of existing interfering signals during the process of demodulation. This poses a problem specially to the design of the receiver local oscillator (LO) since it is required to have a narrow spectral component in order for the receiver to have good interference rejection and good channel selectivity.

In the following sections a few commonly used receiver topologies are presented and discussed.

2.1.1 Heterodyne receiver

The Heterodyne or intermediate-frequency (IF) receiver is shown in Fig. 2.1 [5]. For the purpose of down-conversion it performs several frequency translations and can use one or more IF frequencies. The down-conversion for a low frequency alleviates the specifications on some of the blocks: e.g. low-pass filter and the analogue-to-digital converter (ADC). Typically, the demodulation is done in the analog domain, however, if the last frequency translation is done to a sufficient low frequency the demodulation process is possible to be performed in the digital domain.

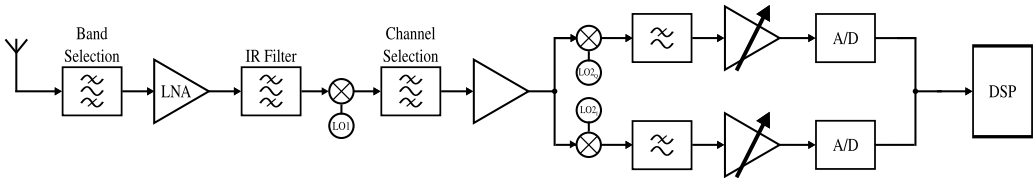

Figure 2.1: Heterodyne Receiver

It requires a few channel selection filters to deal with adjacent channels and interference. One of the most important is the image reject filter (IRF) that deals with the image signal. The image signal is a signal that is as far apart from LO signal as the signal of interest. The existence of the image signal poses a problem since it causes spectral overlapping over the signal of interest, as shown in Fig. 2.2. If we consider mixing effect over the image signal:

$$v_{IM,IF}(t) = \frac{V_{IM}V_{LO}}{2}\cos((\omega_{IM} - \omega_{LO})t) + \frac{V_{IM}V_{LO}}{2}\cos((\omega_{IM} + \omega_{LO})t) \tag{2.1}$$

Since $\omega_{IM} = 2\omega_{LO} - \omega_{RF}$:

$$v_{IM,IF}(t) = \frac{V_{IM}V_{LO}}{2}\cos((\omega_{LO} - \omega_{RF})t) + \frac{V_{IM}V_{LO}}{2}\cos((3\omega_{LO} - \omega_{RF})t) \tag{2.2}$$

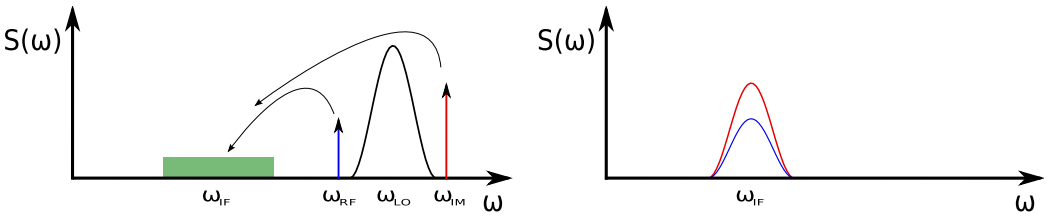

Figure 2.2: Image problem in the heterodyne receiver.

The desired channel and the image have a frequency difference of $2\omega_{IF}$, the choice of this ω_{IF} frequency is usually subject to great analysis since it will impose the required quality factor for the IR and the channel selection filter. There is a inherent trade-off between image rejection and channel selectivity and usually at least one of the filters must be implemented off-chip because high-performance filters are difficult to obtain in integrated technology. This consequently increases the implementation cost of the receiver.

2.1.2 Homodyne receiver

The Homodyne or Zero-IF receiver is shown in Fig. 2.3 [5]. This type of receiver directly translates the input signal to the baseband. This particularity results in a simpler architecture and allows the possibility of a complete integration since it does not require off-chip filters.

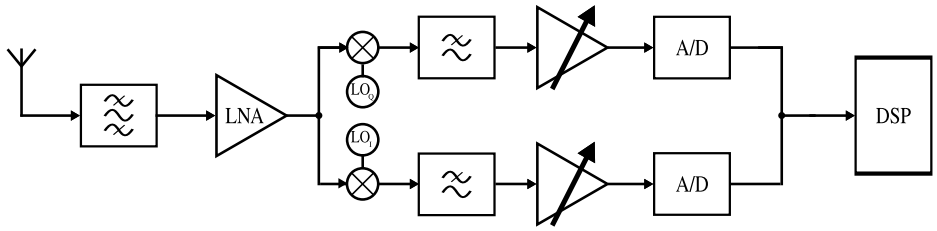

Figure 2.3: Quadrature Homodyne Receiver

However, because it directly shifts the signal of interest to baseband it has some drawbacks:

- It is affected by flicker noise, DC offset and 2^{nd} order distortion;
- Leakage occurs between blocks that can cause LO signal radiation to the antenna or LO self-mixing;
- Quadrature mismatch affects the constellation diagram.

2.1.3 Low-IF receiver

The Low-IF is a modern receiver that combines the architectures of the typical homodyne and the heterodyne receiver [1]. It is mainly based on the heterodyne receiver where the signal is shifted to a low IF. Since it does not down-convert the signal of interest to baseband, flicker noise is no longer a critical issue and the distortion requirements can be relaxed, making the Input referred second-order intercept point (IIP2) parameter less critical.

The limitation of this approach is that the image problem still persists like in the heterodyne receiver (see Fig. 2.2). Since full integration of the receiver is desirable, the image problem must not be addressed resorting to the use of rejection filters. Instead, cancellation techniques can be used like the Hartley (see Fig. 2.4) and the Weaver (see Fig. 2.5) architectures. Lets first introduce the Hartley configuration of the Low-IF receiver in Fig. 2.4:

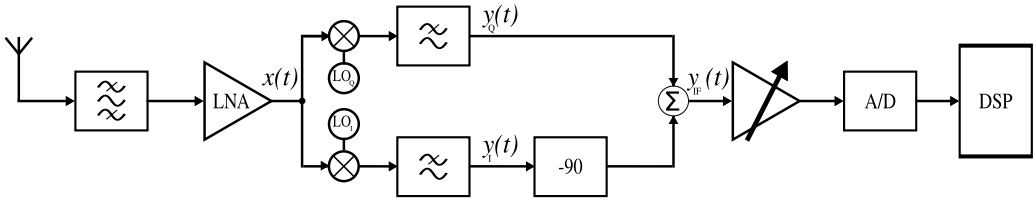

Figure 2.4: Low-IF receiver with Hartley image rejection configuration.

If one considers the input to be of the form:

$$x(t) = V_{RF}\cos(\omega_{RF}t) + V_{Im}\cos(\omega_{Im}t) \tag{2.3}$$

After the low pass filter the in-phase signal, $y_I(t)$, and quadrature signal, $y_Q(t)$:

$$y_I(t) = \frac{V_{RF}V_{LO}}{2}\cos[(\omega_{LO} - \omega_{RF})t] + \frac{V_{Im}V_{LO}}{2}\cos[(\omega_{Im} - \omega_{LO})t] \tag{2.4}$$

$$y_Q(t) = \frac{V_{RF}V_{LO}}{2}\sin[(\omega_{LO} - \omega_{RF})t] + \frac{V_{Im}V_{LO}}{2}\sin[(\omega_{Im} - \omega_{LO})t] \tag{2.5}$$

Since a phase shift of -90 is applied to the signal $y_I(t)$

$$y_I(t) = \frac{V_{IF}}{2}\cos(\omega_{IF}t) - \frac{V_{Im}V_{LO}}{2}\cos((\omega_{LO} - \omega_{Im})t) \tag{2.6}$$

If $y_I(t)$ and $y_Q(t)$, are summed, the image is suppressed:

$$y_{IF}(t) = V_{IF}\cos(\omega_{IF}t) \tag{2.7}$$

The same operation can be done with the Weaver architecture (see Fig. 2.5). It is similar but it uses a second mixer stage at the frequency ω_{IF}.

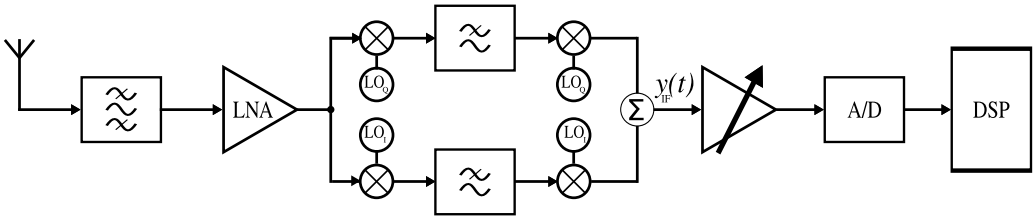

Figure 2.5: Low-IF receiver with Weaver image rejection topology.

It is possible to understand that suppressing the image trough its negative replica is dependent on accurate quadrature LO signals.The asymmetry in the down-converted signals can be expressed in gain and phase errors. Usually the gain error is introduced by the mixer stage that can present conversion loss which results in down-converted signals with unequal amplitudes. On the other hand the phase fluctuations are mainly caused by mismatches in the LO design. Usually they are of two types; mismatches due to the fabrication process and layout mismatches that causes uneven signal paths.

Let us consider that a given oscillator produces two quadrature signals with a phase error ϕ:

$$y_I(t) = V_{LO}\cos(\omega_{LO}t) \tag{2.8}$$

$$y_Q(t) = V_{LO}\sin\left(\omega_{LO}t + \phi\right) \tag{2.9}$$

Let us also consider that the mixer RF input signal is the following:

$$x_{RF}(t) = V_{RF}\cos(\omega_{RF}t) + V_{RF}\sin(\omega_{RF}t) \tag{2.10}$$

After down-conversion to IF, the low frequency components at the output of the mixer are:

$$z_I(t) = \frac{V_{IF}}{2}\left[\cos(\omega_{IF}t) + \sin(\omega_{IF}t)\right] \tag{2.11}$$

$$z_Q(t) = \frac{V_{IF}}{2}\left[\cos\phi\left[\cos(\omega_{IF}t) + \sin(\omega_{IF}t)\right] + \sin\phi\left[\cos(\omega_{IF}t) - \sin(\omega_{IF}t)\right]\right] \tag{2.12}$$

In eq. 2.12 its possible to observe the degeneration effect caused by the phase error. Feedback can minimize this problem by adjusting the phase difference between the two signal paths. This can be done, for instance, by coupling two oscillators. The use of quadrature signals allows to discard image-rejection filters that imply large die area or even external components to be implemented which increases the cost of implementation of the receiver [4, 23]. Quadrature coupled RC oscillators are known to have reduced quadrature errors even if mismatches occur in fabrication [24].

The ISM bands (see Fig. 2.6) are allocations of the frequency spectrum mostly dedicated to unlicensed RF applications. In these bands modern standards like Wi-fi, Bluetooth or even ZigBee are used, which make use of modulation schemes like quadrature amplitude modulation (QAM) or quadrature phase-shift keying (QPSK). These modulation schemes require oscillators capable of generating precise quadrature outputs. In recent years several applications were developed to operate in these bands like wireless sensor network (WSN), near field communication (NFC), medical disposable sensors or even internet-of-things (IoT) devices, which are characterized for being based on low cost receivers [2]. These applications have reinforced the interest in RC oscillators as they are capable of low quadrature errors, wide tuning range and reduced fabrication costs, when compared with LC oscillators.

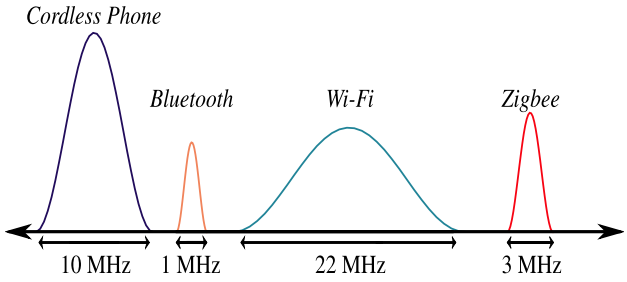

Figure 2.6: Wireless systems using ISM Bands.

2.1.4 Phase-noise

The oscillator output can suffer from deviations. Specially important are the noise induced phase-deviations which are accumulated since the oscillator by itself does not possess a phase regeneration mechanism (amplitude deviations can be neglected since the oscillator has an amplitude restoring mechanism [25]). As a result, the output of the oscillator becomes a phase-modulated signal,

$$v_{LO}(t) = V_{LO}.\cos\left(\omega_{LO}t + \phi(t)\right) \tag{2.13}$$

where V_{LO} is the amplitude, ω_{LO} is the oscillation frequency and $\phi(t)$ is the modulating signal of stochastic nature. This effect causes the power of the carrier to be spread throughout nearby frequencies. The main consequence of this is that if the oscillator has significant side-bands it will overlap the signal of interest with the content from the adjacent channels (see Fig. 2.7).

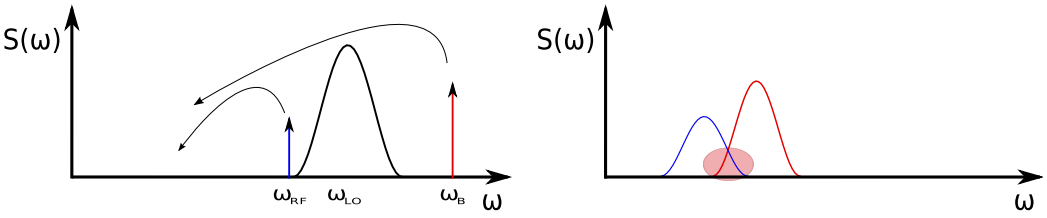

Figure 2.7: Spectral overlap due to a noisy oscillator.

This allows to conclude that the side-bands limit the applicability of the oscillator. Therefore, it is important the characterization and quantification of the side-bands, which can be done by relating their power to the power of the fundamental (considering a bandwidth of 1 Hz):

$$\mathcal{L}\{\Delta\omega)\} = 10\log\left(\frac{S(\omega_{LO}+\Delta\omega)}{S(\omega_{LO})}\right) \text{ (dBc/Hz)} \tag{2.14}$$

where $\Delta\omega$ is a frequency offset from the fundamental. Since the noise manifests itself as phase deviations of the oscillatory signal, this parameter is referred as phase-noise. It is a very important parameter of oscillators and, since it allows defining the oscillator aptitude to reject nearby channels, its accurate estimation is vital. However, the process of determining the relative side-band power of a phase-modulated signal, when the modulating signal is of a stochastic nature, is complex [26, 27]. Some methods of the characterization of phase-noise will be briefly reviewed in the following sections.

2.1.4.A Leeson-Cutler model

One of the most widespread models used for the estimation of phase-noise of electrical oscillators is the Leeson-Cutler model [28]. This allows a simple characterization of single side-band (SSB) phase noise spectral density (SSB Phase Noise) of resonators. The model distinguishes two regions (see Fig. 2.8):

- **Region $\frac{1}{f^3}$:** The content results from the multiplication of flicker noise power spectral density (PSD) with the transfer function of an integrator.

- **Region $\frac{1}{f^2}$:** The content results from the multiplication of white noise PSD with the transfer function of an integrator.

The $\frac{1}{f^3}$ region main contributor is the flicker noise. This appears mainly in metal-oxide-semiconductor (MOS) transistors and is caused by impurities in the interface defined by the gate oxide and the silicon substrate. It is found at low frequencies and since its power spectrum is inversely proportional to the frequency it is often named as $1/f$ noise or pink noise. For a single transistor it is analytically stated as following:

$$\overline{v_{nf}^2} = \frac{k_f}{c_{ox} W L f^{\alpha_f}} \tag{2.15}$$

where k_f is a process dependent constant which is bias independent, c_{ox} is the gate oxide capacitance per area, W is the width of the transistor, L is the length of the transistor and α_f is Hooge 1/f noise parameter. Because flicker noise PSD has a slope of -10 dB/dec and the integrator a slope of -20 dB/dec this region has a slope of -30 dB/dec.

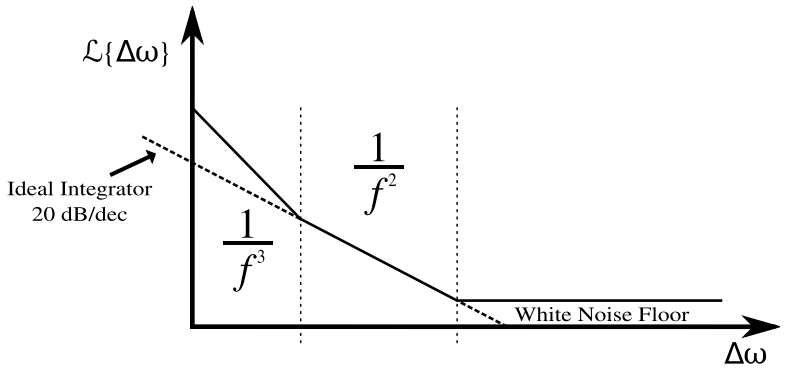

Figure 2.8: Leeson-Cutler phase noise model.

The $\frac{1}{f^2}$ region main contributor is integrated white noise:

$$\mathcal{L}\{\Delta\omega\}_{\frac{1}{f^2}} = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}|H(\Delta\omega)|^2}{S(\omega_{LO})}\right) \text{ (dBc/Hz)} \tag{2.16}$$

where $|H(\Delta\omega)|^2$ is the closed loop transfer function of the oscillator and $\frac{\overline{i_n^2}}{\Delta f}$ is the white noise PSD defined as following:

$$\frac{\overline{i_n^2}}{\Delta f} = 4FkTG_L \tag{2.17}$$

where F is the excess noise number (a posteriori fitting parameter), k is Boltzmann's constant, T is de absolute temperature, G_L is the parallel equivalent conductance of the load. This region has a slope of -20 dB/dec in view of the integrator frequency response.

2.1.4.B Impulse sensitivity function

Even though the Leeson-Cutler phase noise model offers a simple and intuitive description of the side-bands, it is not absolute accurate (hence the existence of a fitting parameter). Electrical oscillators are time-variant circuits as consequence of their natural large signal operation and their implementation making use of active devices. This implies the circuits present a time-dependent behavior, which means the typical analysis methodologies are not suitable (for instance, the use of incremental models). One of the known methodologies to study time-variant systems is to characterize their impulse responses [29]. In [30] a simulator assisted approach is proposed to analyze the oscillator based on impulse responses. In this approach the oscillator is modeled as a time-variant filter like the one shown in Fig. 2.9

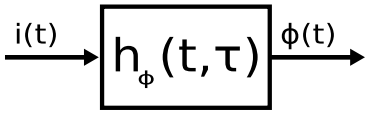

Figure 2.9: Oscillator node modeled as a time-variant filter.

The method consists in accounting how much phase-shift, $\phi(t)$, is observed at the output of the oscillator when a current impulse, $i(t)$, is injected into a given node. Because every node on circuit has a connected capacitance (either due to a real capacitor or a parasitic effect) they are able to condition the output phase and for that reason all of them must be characterized. The impulse response, $h_\phi(t,\tau)$, for a given

circuit node is determined as follows:

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_{osc}\tau)}{q_{max}} u(t-\tau) \tag{2.18}$$

where q_{max} is the maximum charge displacement across the equivalent capacitor on the node, $u(t)$ is the Heaviside function (the impulse response of an integrator is a step function) and $\Gamma(\omega_{osc}\tau)$ the input sensitivity function (ISF). The ISF is a periodic signal, obtained resorting to Spice simulations, which is a function of the circuit time-variance and describes how much phase shift results on the oscillator output from applying a unit impulse on a given node at instant τ.

The phase deviation induced by a given charge stimulus is called excess phase and is described as follows:

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau) i(\tau) d\tau \tag{2.19}$$

The induced charge variation is:

$$\Delta q = i(\tau) d\tau \tag{2.20}$$

The superimposition integral which accounts for all the nodes contributions for the oscillator output phase shift is:

$$\phi(t) = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_{osc}\tau) i(\tau) d\tau \tag{2.21}$$

This phase macro-model, amongst other things, is useful to determine the effect of noise on the oscillator phase by assuming that $i(t)$ is a noise current. The noise influence over the phase can be interpreted as the result of folding as shown in Fig. 2.10.

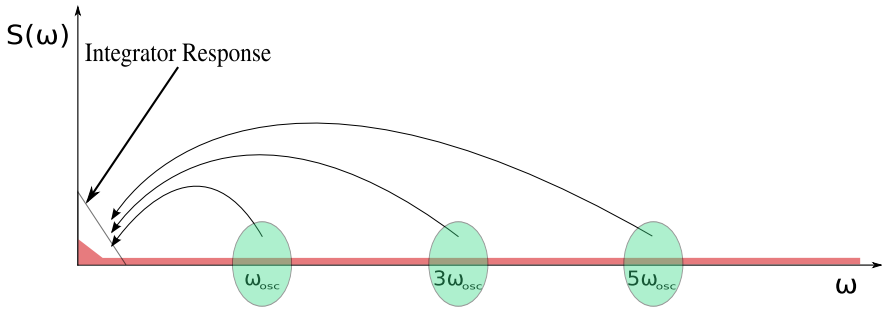

Figure 2.10: Noise folding describing how high frequency noise contributes to the phase-shift of the oscillator output.

Two typical ISF waveforms described in eq. 2.22 and 2.23 are shown in Fig. 2.11. They give respect to two common oscillator operation mechanisms, non-linear (based on hysteresis) and linear (based on resonance) that will be described in higher detail in the next section.

$$\Gamma_{NL}(t) = \sum_{n=0}^{\infty} \Gamma_n \sin(n\omega_{osc}t) \tag{2.22}$$

$$\Gamma_L(t) = \Gamma_1 \sin(\omega_{osc}t) \tag{2.23}$$

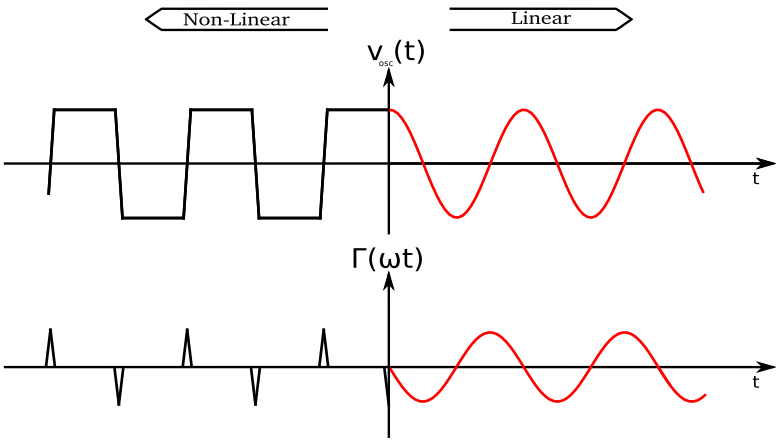

Figure 2.11: Typical ISF waveforms.

Once the total induced phase deviation is accounted (see eq. 2.21) the side-band power can be easily by calculating the power of a phase-modulated signal as follows [3]. Knowing that the output of the oscillator is given by:

$$v_{osc}(t) = V_{osc}.\cos\left(\omega_{osc}t + \phi(t)\right) \tag{2.24}$$

That can be rewritten as follows:

$$v_{osc}(t) = V_{osc}\left[\cos(\beta\sin(\omega_m t))\cos(\omega_{osc}t) - \sin(\beta\sin(\omega_m t))\sin(\omega_{osc}t)\right] \tag{2.25}$$

where β is the modulation index (the amplitude of eq. 2.21) and ω_m is an offset frequency. It can be expanded in Fourier series:

$$v_{osc}(t) = V_{osc}\sum_{-\infty}^{\infty} J_n(\beta)\cos(\omega_{osc}t + n\omega_m t) \tag{2.26}$$

where the coefficients $J_n(\beta)$ are Bessel functions and dependent of the modulation

index, β. This is expression is an analytical representation of the carrier, $J_0(\beta)$, and its infinite side-bands at frequencies $f_c \pm nf_m$. The relative power can be computed as follows:

$$P_{SDC} = 10\log\left(\frac{J_n(\beta)}{J_0(\beta)}\right)^2 \tag{2.27}$$

Finally, for a small modulation index ($\beta \ll 1$) it can be shown that the relative side-band power can be simply determined as follows:

$$P_{SDC} \approx 10\log\left(\frac{\beta}{2}\right)^2 \tag{2.28}$$

Despite the added complexity this method allows more accurate estimations of the spectral density as well as the location of the corner frequencies. It also gives some valuable information on the oscillator sensitivity to a given stimulus, with respect to its time-variance pattern:

- In a linear regime of operation the oscillator is only affected by stimulus close to the frequency of oscillation.

- The larger number of spectral components of the ISF in a non-linear regime of operation (see Fig. 2.10) means that the oscillator is sensitive to stimulus occurring not only in the vicinity of the oscillation frequency but also at its multiples.

The knowledge of the relation between the oscillator time patterns and the noise performance is advantageous when designing a given oscillator, and is specially important when designing RC oscillators since they that can demonstrate both time-patterns, linear and non-linear. This insight is also relevant for synchronization purposes, since it gives us an indication of the ranges of frequencies where the oscillator is sensitive to perturbations.

2.2 CMOS oscillators

The electrical oscillators used in the design of transceivers can be of two types, according the underlying mechanism that is used to generate the periodic signal. They can be quasi-linear (QL) if based in a resonant mechanism or non-linear (NL) if based in a hysteresis mechanism. The resonant mechanism is based in the mutual energy transfer between two reactive elements, and inductor and a capacitor (LC oscillator) while the hysteresis mechanism in based on an integrator and a memory element to provide amplitude limitation (RC oscillator) [31]. Before the introduction

of the corresponding circuit implementations, of both mechanisms, it is important to first define the concept of linearity for oscillators and what are the involved consequences.

2.2.1 Linear oscillators

The general definition for linear systems does not apply directly to an oscillator since it is an autonomous system and it does not have any input. In a general interpretation an oscillator is said to be linear if it can be described with a second-order linear differential equation. Lets consider the following time domain function:

$$h(t) = \sin(\omega_{osc} t + \varphi_0), \ \forall \ t \geq 0 \tag{2.29}$$

$$h(t) = \sin(\omega_{osc} t + \varphi_0)\, u(t) \tag{2.30}$$

where $u(t)$ is the Heaviside unit step function. Applying the Euler identity:

$$h(t) = \frac{e^{j\omega_{osc}t} e^{j\varphi} - e^{-j\omega_{osc}t} e^{-j\varphi}}{2j} u(t) \tag{2.31}$$

By operating the Laplace Transform (considering $\Re(s) \geq 0$):

$$H(s) = \frac{1}{2j}\left[\frac{e^{j\varphi_0}}{s - j\omega_{osc}} - \frac{e^{-j\varphi_0}}{s + j\omega_{osc}}\right] \tag{2.32}$$

Can be rewritten as:

$$H(s) = \frac{s\sin(\varphi) + \omega_{osc}\cos(\varphi)}{s^2 + \omega_{osc}^2} \tag{2.33}$$

Considering that this Laplace transform corresponds to the transfer function of a filter, it is possible to obtain an equivalent differential equation whose impulsive response is the one shown in eq. 2.29:

$$H(s) = \frac{Y(s)}{X(s)} \tag{2.34}$$

Eq. 2.33 can be rewritten as:

$$s^2 Y(s) + \omega_{osc}^2 Y(s) = s\sin(\varphi)X(s) + \omega_{osc}\cos(\varphi)X(s) \tag{2.35}$$

By operating the inverse Laplace Transform :

$$\frac{d^2 y}{dt^2} + \omega_{osc}^2 y(t) = \sin(\varphi)\frac{dx(t)}{dt} + \omega_{osc}\cos\varphi x(t) \tag{2.36}$$

Despite not having an input and a transfer function, it is assumed that a linear oscillator can be interpreted and studied as a second order system that has the impulse

response shown in eq. 2.29. These assumptions allow to model the linear oscillator as a second order feedback with a pole pattern of a pair of conjugated poles over the imaginary axis. This allows to simplify the analysis of the oscillator.

2.2.1.A Barkhausen criterion

If an oscillator presents a linear behaviour it can be modelled as the feedback system shown in Fig. 2.12 that has the equivalent transfer function shown in eq. 2.37. The system consists of an amplifying element A and a feedback network β.

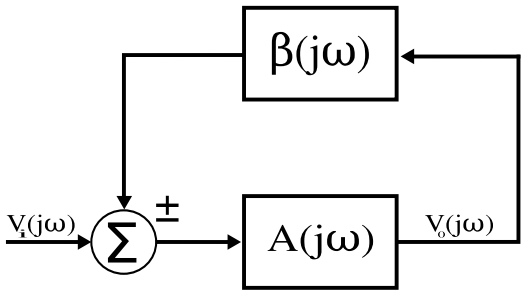

Figure 2.12: Feedback system.

$$\frac{v_o(j\omega)}{v_i(j\omega)} = \frac{A(j\omega)}{1 \mp A(j\omega)\beta(j\omega)} \tag{2.37}$$

From eq. 2.33 we know that oscillation occur when there exists a pair of complex conjugate poles over the imaginary axis. Therefore, the conditions that ensure oscillation can be found by analyzing the poles. That can be done by equating the denominator of the transfer function to zero:

$$|A(j\omega)\beta(j\omega)| = 1 \tag{2.38}$$

This result is named Barkhausen amplitude condition. However, depending on the phase introduced by the feedback network this value may be either -1 or 1, which allows deriving the Barkhausen phase condition:

$$\begin{aligned} &\angle A(j\omega)\beta(j\omega) = 0 + 2k\pi,\ k \in N \text{ (If referring to positive feedback)} \\ &\angle A(j\omega)\beta(j\omega) = \pi + 2k\pi,\ k \in N \text{ (If referring to negative feedback)} \end{aligned} \tag{2.39}$$

These are boundary conditions and they state that the total loop phase should be zero and that the amount of energy introduced, by the amplifying stage, should be equal to the amount of dissipated energy, by the feedback network. The loss of energy is related to resistive elements and the stored energy with the reactive elements.

2.2.1.B Quality factor

As previously discussed the losses must be compensated in order to obtain sustainable oscillations, which implies energy consumption. This suggests that the efficiency of oscillators can be benchmarked according the level of losses. Typically, this is done resorting to a metric called quality factor which is an indirect measure of the oscillator energy dissipation [5, 32]. The use of this parameter allows to avoid a complex and extensive enumeration and description of all the oscillator losses. It can be expressed according three different definitions:

1. The first definition is obtained from the shape of the oscillator signal spectral representation:

$$Q = \frac{\omega_{osc}}{B} \tag{2.40}$$

where ω_{osc} is the oscillation frequency and B is the -3 dB bandwidth. As the losses increase the bandwidth also increases which reduces the quality factor (see Fig. 2.13).

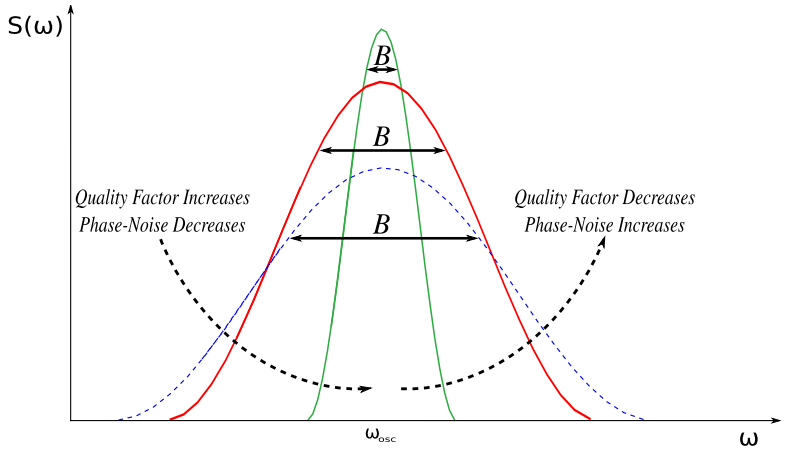

Figure 2.13: Quality factor vs phase-noise.

2. Another definition is to express the quality factor as a ratio between stored and dissipated energy [8].

$$Q = 2\prod \frac{\text{Maximum energy stored in a period}}{\text{Energy dissipated in a period}} \tag{2.41}$$

3. The last definition is obtained from the oscillator open-loop transfer function, $H(j\omega)$ [8].

$$Q = \frac{\omega_{osc}}{2} \sqrt{\frac{dA^2}{d\omega} + \frac{d\Theta^2}{d\omega}} \tag{2.42}$$

where A is the amplitude and Θ is the phase of $H(j\omega)$. The quality factor ends up suggesting the power distribution around the central frequency and that is why it also gives an indication on the phase-noise performance. As the losses increases the quality factor is reduced and the phase-noise increased (see Fig. 2.13).

2.2.1.C LC oscillator

The LC oscillator, shown in fig. 2.14, is a case of a linear oscillator and has been extensively used in generating and receiving RF signals due to its phase-noise performance. It is composed of an amplifying stage and a band-pass filter. The band-pass filter is composed of an inductor and a capacitor than exchange energy (inductor stores the energy as a magnetic field and the capacitor stores energy as an electric field). A periodic behavior can be achieved when the amount of energy being processed and exchanged amongst the reactive elements is unchanged. This is referred as resonant state and is obtained when the reactances of both reactive elements are equal (see eq. 2.43) [33]. The implementation in CMOS technology is shown in fig. 2.14. It is composed of an LC network, a cross-coupled differential pair and a current source.

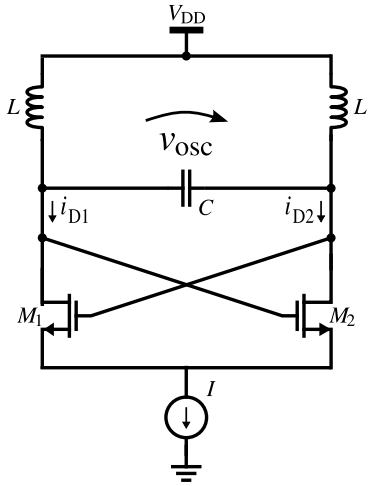

Figure 2.14: Differential CMOS LC oscillator.

The circuit implementation of a resonant mechanism is done resorting to active devices that originates the appearance of harmonics at the output, instead of just one pure tone. It is important to underline that the classification of an oscillator as NL reflects the type of mechanism that is implemented to achieve periodicity and is not the consequence of nonidealities of a particular element, like the transducers. The additional harmonic content is of very low power, when compared with the fundamental, the circuit is said to work in a QL mode of operation but the assumption of linearity is still valid. The resonant condition is as follows:

$$X_L = X_C \Leftrightarrow 2\pi f_{osc} L = \frac{1}{2\pi f_{osc} C} \tag{2.43}$$

and the frequency of oscillation is:

$$\omega_{osc} = \frac{1}{\sqrt{LC}} \tag{2.44}$$

Once the Barkhausen conditions are met the oscillator produces steady-state oscillations (Fig. 2.15).

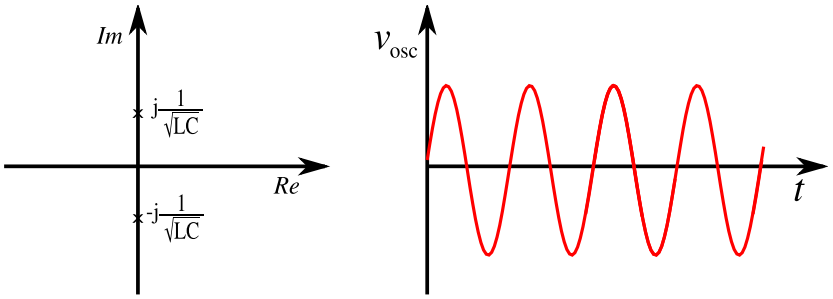

Figure 2.15: LC oscillator output in steady-state.

In order for the oscillations to occur it is required to compensate the losses since the inductor has a parasitic resistance (which is typically high in integrated oscillators since integrated inductors have a reduced Q, around 10). This is accomplished with the cross coupled differential pair that, if it is working in the linear region, (Fig. 2.16) implements a negative resistance (Fig. 2.17) [34–36].

The small signal equivalent of the cross-coupled pair is a resistance as follows:

$$r_x = \frac{v_x}{i_x} = -\frac{1}{g_m} \tag{2.45}$$

This means that the LC oscillator has the equivalent high model that is shown in Fig. 2.18 and that the inductor parasitic losses can be compensated by guaranteeing that:

$$g_m \approx \frac{1}{R_p} \tag{2.46}$$

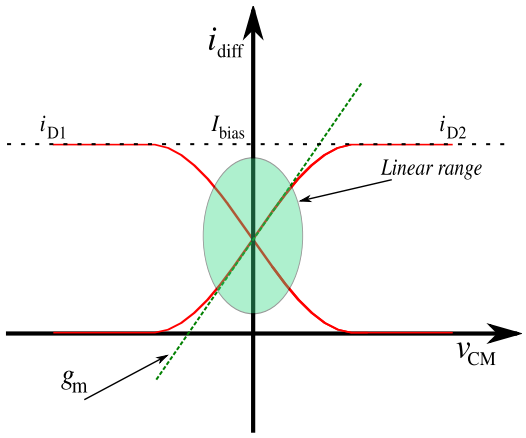

Figure 2.16: Curves of the transistors of the cross-coupled differential pair.

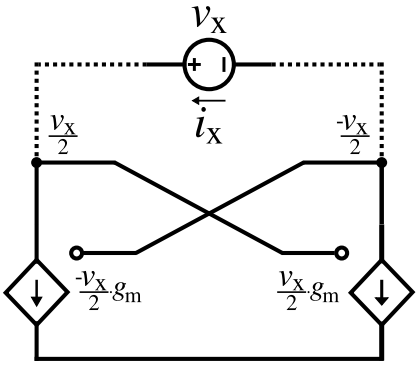

Figure 2.17: Small signal model of the cross-coupled differential pair.

where R_p is the inductor parasitic losses.

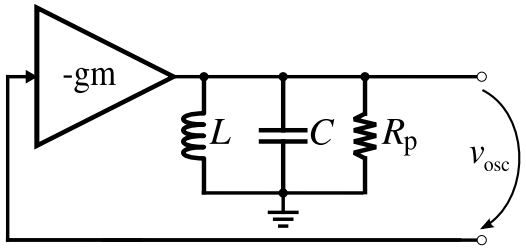

Figure 2.18: LC oscillator high level model.

The condition stated in eq. 2.45 is a condition of equilibrium (obtained in the stationary regime) which will not be obtained unless the circuit is made unstable during start-up (see Fig. 2.19). This is done in order to ensure the circuit unbalance and is guaranteed if:

$$g_m > \frac{1}{R_p} \tag{2.47}$$

By guaranteeing this condition, the generated noise, within the circuit, becomes enough to unbalance it and give initialization to oscillations (see Fig. 2.19). Since the circuit has losses, the poles will move towards the imaginary axis (this statement targets a simplistic explanation of the implied dynamics since the notion of poles does not makes sense during the transient state). Once the losses are compensated (see eq. 2.46), the amplitude will cease the exponential growth and will stabilize.

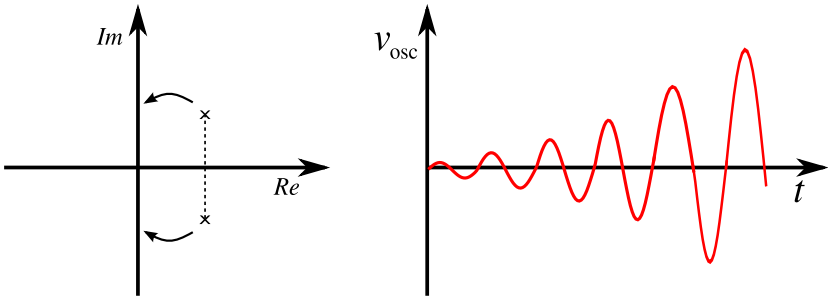

Figure 2.19: LC oscillator during start-up.

Because the circuit performance correlates with the losses, which are typically small, this oscillator is capable of low phase-noise. The performance of the oscillator can be put in perspective by means of a FoM. The performance parameters included in the typical FoM used to benchmark oscillators are noise, power, and oscillation frequency:

$$\text{FoM} = \mathcal{L}(\Delta\omega) + 10\log\left(\left(\frac{P}{10^{-3}}\right)\left(\frac{\Delta\omega}{\omega_{osc}}\right)^2\right) \tag{2.48}$$

where ω_{osc} is the fundamental frequency, $\Delta\omega$ is a frequency offset from ω_{osc}, $\mathcal{L}(\Delta\omega)$ is the phase-noise measured at $\omega_{osc} + \Delta\omega$ and P is the power consumption. The typical performance of LC oscillators can be seen in Tab. 2.1 [37].

Table 2.1: State-of-the art LC oscillators performance.

Ref.	Tech. (nm)	Year	f_{osc} (GHz)	P_{DC} (mW)	PN (dBc/Hz)	FoM (dBc/Hz)
[38]	65	2007	1.6	1.3	-111@0.1MHz	-189
[39]	180	1999	1.8	2	-112@1MHz	-183
[40]	130	2014	2.4	1.9	-133.6@5MHz	-190
[41]	250	2003	4.88	22	-186.7@1MHz	-185
[42]	130	2010	5.1	4.1	-126.1@1MHz	-194
[43]	180	2006	5.3	20.7	-134.4@1MHz	-196

2.2.2 Non-linear oscillators

Non-linear oscillators are a class of circuits that are able to produce a periodic signal without having a resonant mechanism (hence inductorless circuits). They are amplitude stabilized by means of hysteresis, which is implemented by a NL element. These oscillators are defined by non-linear differential equations, unlike the one shown in eq. 2.36, which means these oscillators are typically non-linearizable (which means the Barkhausen criterion is not applicable) and present a rich harmonic content [31]. The high-level representation of a NL oscillator is shown in Fig. 2.20.

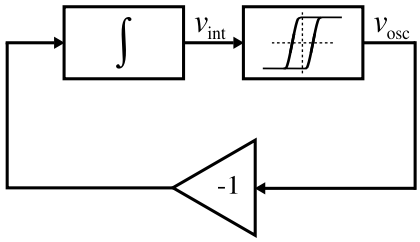

Figure 2.20: High-level model of a non-linear oscillator.

The oscillator is composed of a integrator (an RC impedance), a Schmitt-trigger (a comparator with hysteresis which limits the amplitude) and an inverter. The non-linear element and the negative feedback guarantees that the current that goes into the integrator, i_{osc}, alternates polarity periodically, which allows to sustain oscillations [5]. Typically, it produces a non-sinusoidal periodic output like a square-wave, a trapezoidal-wave or even a triangular-wave [4, 44]. However, in certain particular conditions it can operate close to a linear behavior when the amplitude is soft-limited instead of hard-limited, which results in an output roughly resembling a sine-wave. RC oscillators can be fully integrated (which is difficult with LC oscillators on the account of the low Q of integrated inductors), have low-cost, fit into a small footprint area (comparable to that of a single integrated inductor), have a wide tuning range (by changing the integrator time constant), and are able to provide quadrature (I/Q) signals with low quadrature error [1, 2, 4–6]. In the following sections a few topologies of RC oscillators will be revised.

2.2.2.A Ring oscillator

A ring oscillator is an RC oscillator that consists in a series of inverters in a feedback loop as shown in Fig. 2.21 [18, 45, 46]. It should exist an odd number of inverters to ensure that the loop phase is -180° in order to guarantee polarity alternation (although there are implementations where an even number of inverters can be used [47]).

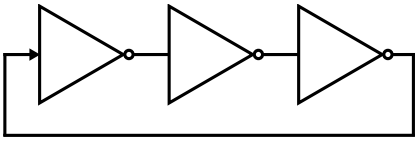

Figure 2.21: Ring oscillator.

Each inverter can be modeled as a gain stage, an integrator and a limiter as shown in Fig. 2.22. The CMOS implementation is shown in Fig. 2.23, where each inverter is implement with a PMOS/NMOS pair with a parasitic output capacitance. Each capacitance is charged/discharged with a current dependent on the resistance of the transistors, once one of the transistors on the inverter stops conduction the capacitance is either charged to the supply rail voltage or completely discharged to the reference node voltage. The output then consists of a square wave upper limited to the supply rail voltage, as shown in Fig. 2.24.

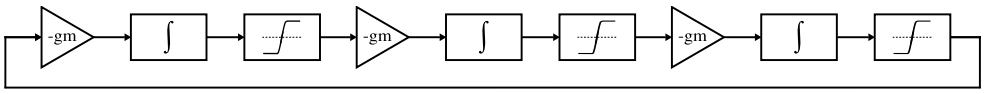

Figure 2.22: 3-stage ring oscillator high-level model.

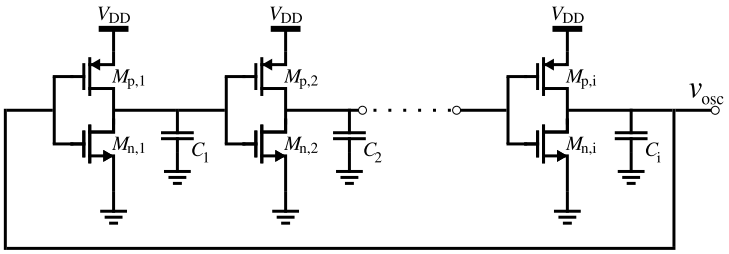

Figure 2.23: N-stage CMOS ring oscillator.

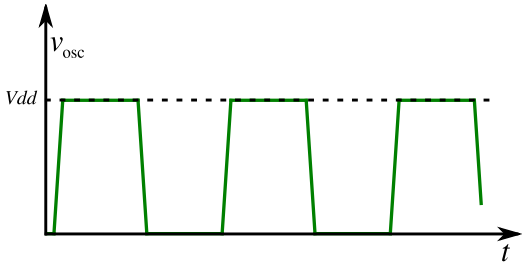

Figure 2.24: CMOS ring oscillator output.

This means that the frequency of oscillation is both dependent on the charge/discharge time of the inverter output capacitor (determined by the size of the transistors) and the number of inverters:

$$f_{osc} = \frac{1}{n2t_d} \tag{2.49}$$

where n is the number of inverters in the loop and t_d is the time delay of each inverter. If the transistors are made small this oscillator is capable of achieving high frequency with reduced energy consumption. Typically this oscillator is the one amongst the common RC topologies with higher practical performance [48, 49].

2.2.2.B Relaxation oscillator

A conventional relaxation oscillator uses two cross-coupled inverters with resistive loads, two current sources, and a capacitor as shown in Fig. 2.25 [4]. The working principle of the oscillator is shown in Fig. 2.26). As current is integrated, the voltage across the capacitor C_{osc} rises. When the voltage reaches the latch threshold, the cross-coupled inverters latch due to positive feedback.

After latching, the capacitor will start to discharge, which eventually causes the reversion of the latch state (the Schmitt-trigger shown in Fig. 2.20). The result is a repetitive charge/discharge of the capacitor.

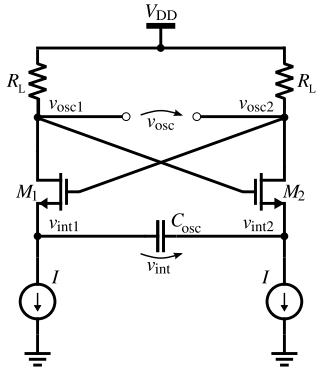

Figure 2.25: CMOS Relaxation oscillator high frequency implementation.

If the latch is designed with small transistors (M_1 and M_2), and by consequence small output load parasitic capacitances, the oscillator operates in relaxation mode. This means the output is a square-wave and the voltage waveform across the capacitor has a triangular configuration as shown in Fig. 2.27.

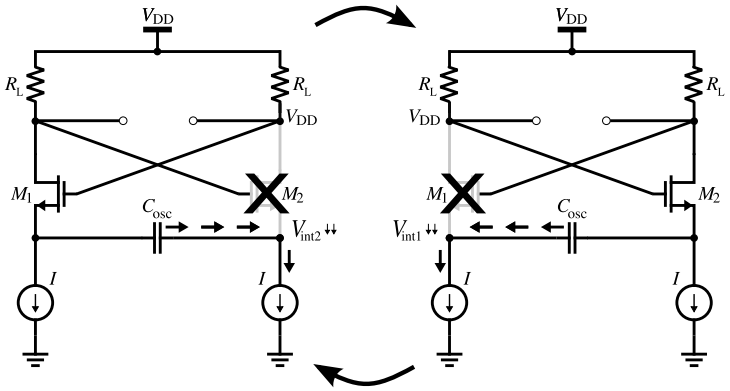

Figure 2.26: CMOS Relaxation oscillator operation.

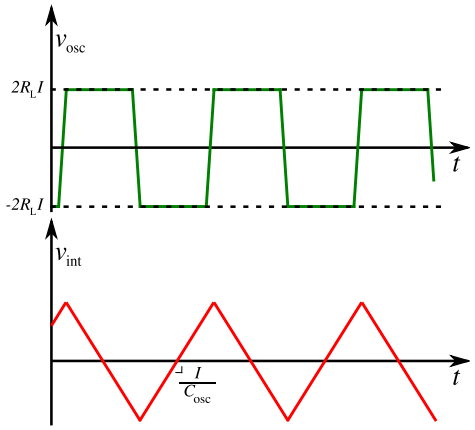

Figure 2.27: Relaxation oscillator waveforms under relaxation behavior.

Since the Schmitt-trigger, operating as a hard-limiter does not allow linearization of the circuit, the analysis usually relies on a first order approximation by studying the integration time [44]. It is assumed the frequency of operation can be well defined by determining the amount of charge that is accumulated in the capacitor during half the period of oscillation:

$$q = C_{osc}V_{osc} \tag{2.50}$$

It is assumed that the voltage drop across the transistors are negligible and that the capacitor charges between $-2RI$ and $2RI$. Knowing that the stored charge is a function of the current,

$$\int_{t_1}^{t_2} Idt = 4C_{osc}R_LI \tag{2.51}$$

and that $t_2 - t_1 = \frac{T_{osc}}{2}$.

$$\frac{1}{2}\int_0^{T_{osc}} dt = 4C_{osc}R_L \tag{2.52}$$

The frequency of oscillation is found to be approximately equal to:

$$f_{osc} \approx \frac{1}{8C_{osc}R_L} \tag{2.53}$$

This approximation tends to fail as the frequency of operation is increased. In that scenario the Schmitt-trigger stops operating as a hard-limiter and the oscillator no longer works in relaxation mode. This means the voltage across the capacitor is not a triangular wave and eq. 2.53 does not estimate accurately the frequency of oscillation.

Theoretical analysis of this oscillator suggest that this oscillator should be the one with higher achievable performance however, practical implementations indicate otherwise since they are always worse than the one of ring oscillator, specially as the frequency of operation is increased as demonstrated in Tab. 2.2 [8, 18, 19].

Table 2.2: State-of-the art RC oscillators performance

Ref.	Type	Tech. (nm)	Year	f_{osc} (MHz)	P_{DC} (mW)	PN (dBc/Hz)	FoM (dBc/Hz)
[19]	Relax.	65	2008	12	0.09	-109@0.1MHz	-162
[50]	Relax.	130	2011	214	1	-132.6@10MHz	-159.1
[18]	Ring	200	2005	232	1.5	-118.5@1MHz	-164
[51]	Ring.	65	2013	645	10	-111@1MHz	-157
[49]	Ring.	600	1999	900	30	-117@0.6MHz	-166
[48]	Ring	180	2004	913	18.95	-116.5@0.6MHz	-167
[8]	Relax.	500	1996	920	10	-102@1MHz	-151.3
[52]	Ring.	180	2011	1800	13	-102@1MHz	-156
[53]	Relax.	350	2007	2400	48	-105@1MHz	-155
[54]	Ring	130	2009	2500	2.86	-95.4@1MHz	-159
[55]	Ring	180	2003	3520	16.2	-106.4@4MHz	-153

2.2.2.C Two-integrator oscillator

The two-integrator oscillator, shown in Fig. 2.28 is another type of RC oscillator. It is characterized, by having inherent quadrature outputs obtained by cross-coupling two identical stages [4].

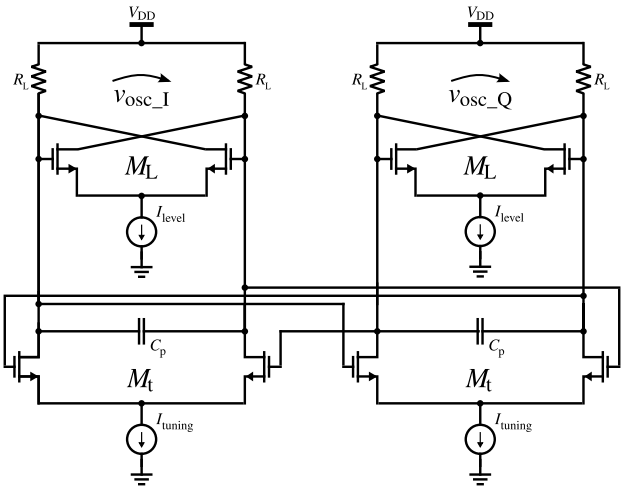

Figure 2.28: CMOS two-integrator oscillator high frequency implementation.

The main particularity of this oscillator is that despite having the same blocks as the relaxation oscillator they are not connected the same way. The stabilization mechanism and the integrator are not stacked (see Fig. 2.29) and so it is required another stage to form a loop (the circuit will not oscillate with only one stage). The coupling is cross-coupled to provide quadrature outputs. Since individual current sources exist it is possible to independently change the output amplitude and the operating frequency. The consequence though, is a penalty on the energy consumption.

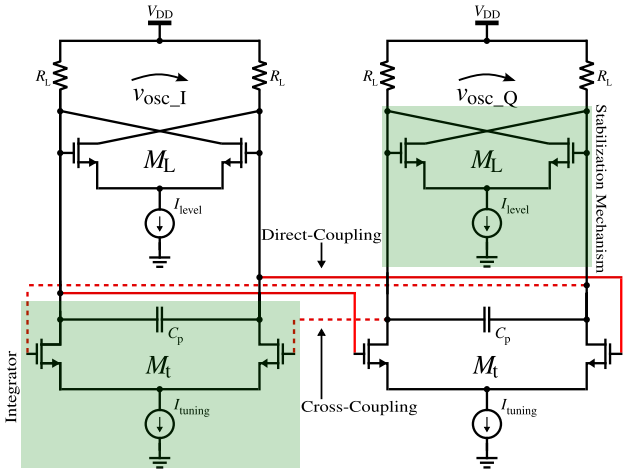

Figure 2.29: Two-integrator blocks description.

One other consequence of this configuration is that, due to the increase of the number of transistors connected to the output nodes, the level of parasitic capacitances is increased. This leads to the same scenario as the one aforementioned when the relaxation oscillator goes into high frequency of operation; the Schmitt-trigger is no longer a hard-limiter (due to the increased output capacitances this mode of operation is reached at a much lower frequency on the two-integrator).

If the Schmitt-trigger operates as a hard-limiter the oscillator output is roughly a square wave which is translated into a rich spectral content (see Fig. 2.30). If the Schmitt-trigger operates as a soft-limiter the output is roughly a sine-wave and its output spectrum content has fewer components (see Fig. 2.31). In this scenario the oscillator is said to be operating in QL regime [56].

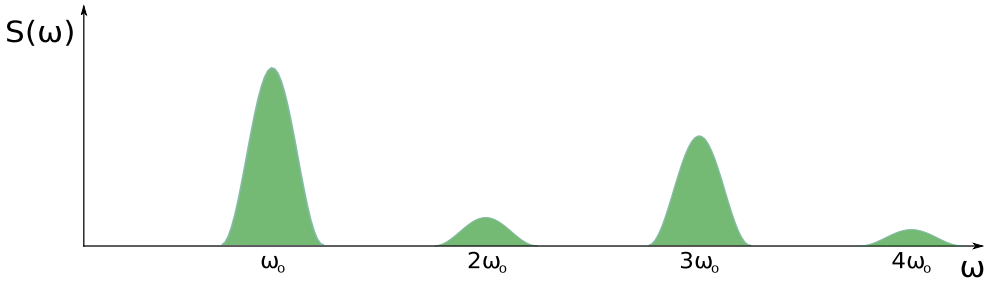

Figure 2.30: Spectral content when schmitt-trigger is a hard-limiter.

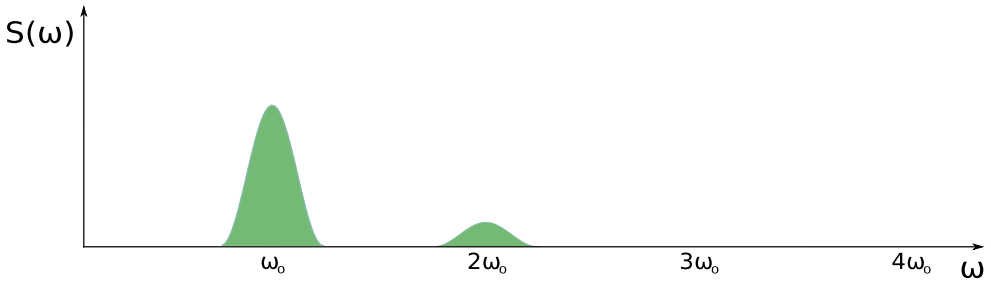

Figure 2.31: Spectral content when schmitt-trigger is a soft-limiter.

The QL assumption implies that the oscillator can be modeled and studied using the same methodology as if it was a linear oscillator. This means that it can be modeled as a linear feedback system and that the Barkhausen criterion can be applied. The equivalent linear model is shown in Fig. 2.32 [4].

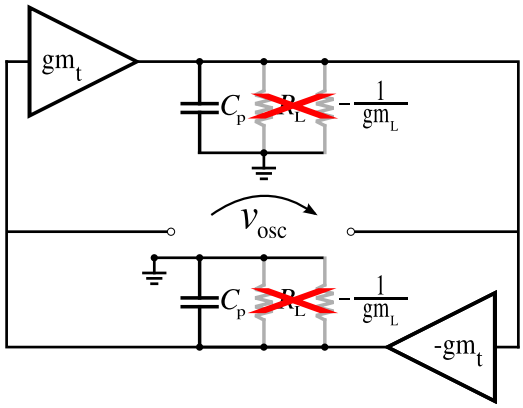

Figure 2.32: Two-integrator oscillator working in QL mode of operation.

The loop gain of the oscillator is:

$$\left|H(j\omega)\right| = \frac{g_{mt}}{(\omega_{osc}C_p)^2} \tag{2.54}$$

The operating frequency can be obtained by equating the loop gain to 1:

$$\omega_{osc} = \frac{g_{mt}}{C_p} \tag{2.55}$$

The operation in QL mode suggests that the transistors are always conducting and never switch off which means that if the oscillator moves towards this mode of operation a penalty over the energy consumption is to be expected.

2.3 Discussion

In this chapter the relevance of the RC oscillators in modern communication standards was detailed. However, it was underlined that they present a major flaw which is their phase-noise performance which is poor on the account of the presence of the resistor. Even at farther offsets, the difference in phase-noise performance to the LC oscillators is of the order of -20/-30 dBc as shown in Fig. 2.33.

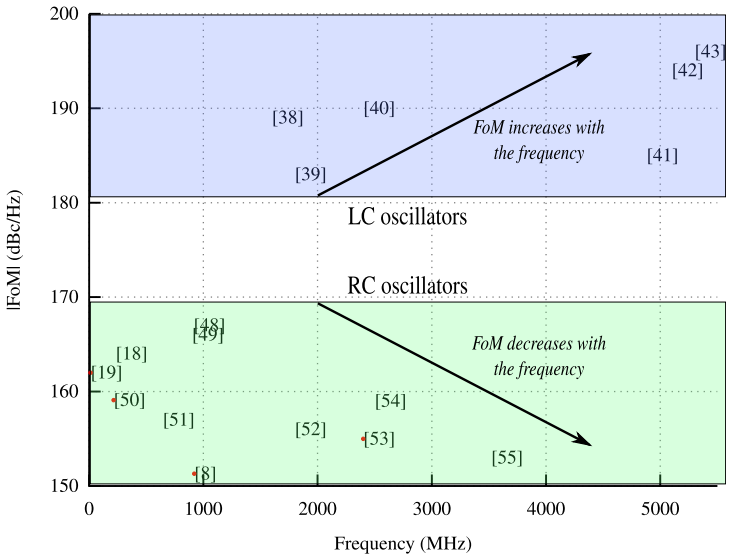

Figure 2.33: CMOS oscillators FoM comparison.

Because the RC oscillators are capable of working in two modes, NL and QL [56] and their performance differs from one mode to the other (the trade-offs will be discussed with higher detail throughout this thesis) it is not an easy task task to minimize the phase-noise while guaranteeing low power consumption, specially as the frequency of operation increases as shown in Fig. 2.33. A NL behavior guarantees low power consumption (transistors are only active during a short time frame) but higher phase-noise (more noise is folded back as shown in Fig. 2.10). The other way around occurs in a QL behavior.

This means that a compromise is expected to be found by guaranteeing that the oscillator operates in a regime between the NL and the QL modes of operations. This however, has two problems:

1. Design equations are very difficult to obtain.
2. On the account of parasitics, as the frequency of operation is increased the oscillator will inevitably move towards the QL mode.

Because the RC oscillators have useful properties it is then relevant to study how the phase-noise can be corrected at high frequency of operation with minor impact on the power consumption.

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3

Injection-locking of CMOS Oscillators

Preamble

In this chapter the phenomena of injection-locking is described and the synchronization models are presented.

Contents

3.1 Phase-noise correction

Attempts to reduce the phase-noise may include adoption of different technologies, scale the devices and/or improve the power management circuits that supplies the oscillators. However, design techniques can only improve the phase-noise of the oscillators up to a certain point. One method that can further improve the oscillator phase-noise performance past the limits of the previous approaches is to use frequency synthesizers.

A classical structure of a commonly used frequency synthesizer, the PLL, is represented in Fig. 3.1. It is composed of a reference signal, a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO) [5, 7, 16].

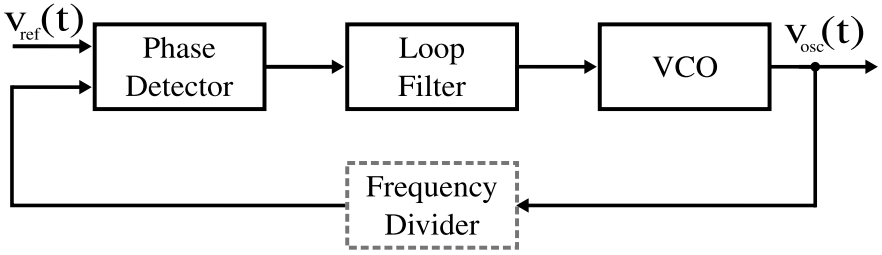

Figure 3.1: Phase-locked loop structure.

The PD outputs a voltage that is proportional to the phase difference between two input signals. The LF is typically an RC network and it averages the output of the PD generating a DC voltage to control de VCO frequency. The input of the VCO is a voltage that is proportional to the phase difference between the output signal of the PLL and the reference signal.

The loop will force the phase error to zero and once it happens the PD output no longer disturbs the VCO. When the frequencies are equal the loop is said to be locked and:

$$\phi_{osc}(t) - \phi_{ref}(t) \approx \text{Const.} \tag{3.1}$$

The LF sets the loop's gain margin and phase margin and as consequence it defines the compromise between the bandwidth of the PLL (also known as locking range) vs stability. The LF is also responsible to prevent the existence of ripple at the VCO input, that is problem since it causes unwanted frequency modulation. However, reducing the pole frequency to account for that situation increases the settling time. It is a defying task to design a PLL, specially the LF since it implies a number of trade-offs. Because some communication standards operate in the GHz range and the crystals that are used as references only go as high as a few MHz it is often required to use a digital frequency divider so that the PD compares frequencies of the same order. This block also allows the PLL to hop amongst a wide range frequencies. Despite the

complexity in the design and the overhead in both cost and power, the use of PLLs imparts flexibility to a given transceiver, turning it capable of complying to several standards.

Nevertheless there is also a known mechanism that can be used to either enhance the PLL by reducing its power penalty (by means of low power frequency dividers [9]) or to implement a competitive frequency synthesizer. The exploitation of the injection-locking phenomena has been known to allow the implementation of simpler frequency synthesizers with comparable performance to the one of a PLL, but with reduced area and power consumption [57, 58]. This phenomena turns possible the use of the VCO internal structures to mimic the operations of the PD and the LF seen on the PLL and obtain a frequency synthesizer with the simple direct injecting of a reference signal into the VCO, as shown in Fig. 3.2

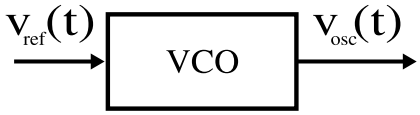

Figure 3.2: Direct injection of reference signal into the oscillator.

3.2 Injection-locking phenomena

Electrical oscillators are sensitive to charge variations. If a given stimulus is able to condition the oscillator internal charge/discharge operations it can affect the oscillator output phase, as shown in Fig. 3.3.

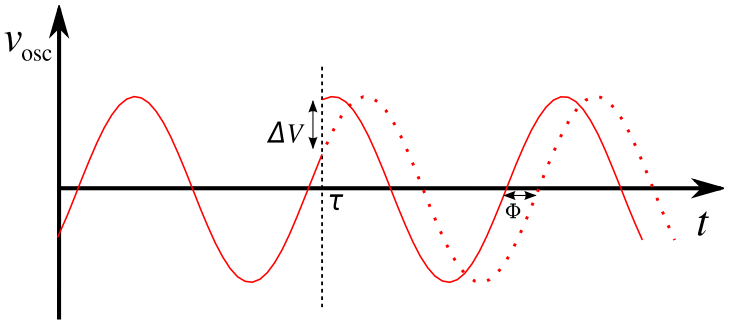

Figure 3.3: Phase-shift on the oscillator output due to a charge variation at instant τ.

One type of perturbation that is known to condition the oscillator response is noise, which induces stochastic phase-shifts and by consequence phase-modulation of the

output signal (hence phase-noise). However, not all stimulus have a negative impact. In fact this particularity of the oscillators is often explored, for instance, to achieve clock-deskew in ring oscillators by inducing a short duration charge variation [59]. Furthermore, if the induced stimulus is of periodic nature it can affect the oscillator time-variance and under certain conditions of magnitude and frequency, it can trigger a frequency shift of the oscillator time response enforcing synchronization as shown in Fig. 3.4 [10, 57, 60].

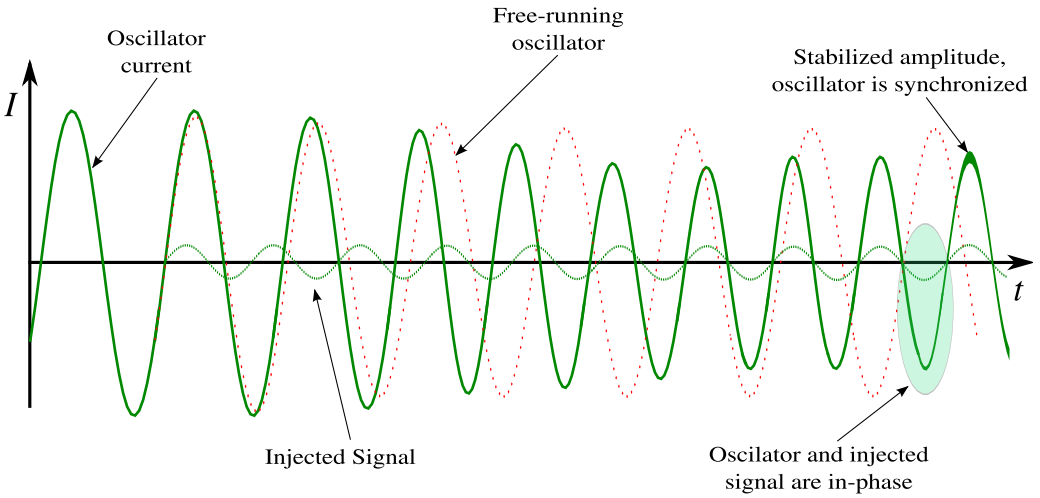

Figure 3.4: Synchronization of the oscillator using a periodic stimulus.

In the scenario where synchronization is obtained, the oscillator is then referred as an ILO, there will be a correlation between the phase-noise of the reference signal and the one of the synchronized oscillator similar to what is seen in a PLL structure [10, 61]. If the reference signal has better frequency stability than the free-running oscillator, the injection-locked oscillator will show better phase-noise performance than in the absence of perturbation.

Even though this mechanism has been used to achieve frequency division, clock-deskew or even quadrature generation [62] it is in frequency synthesis that is found its highest potential. The injection-locking phenomena has been exploited to accomplish high performance, high frequency, low-cost and low-power frequency synthesizers and are regarded as an alternative to the use of PLLs (since ILOs are in fact just oscillators, they imply less power and area than a PLL). However, ILOs are not a widespread option because the extent of their applicability and performance is still limited by their inherent narrow locking-range (maximum offset frequency that can still trigger synchronization).

3.3 Synchronization models

One typical implementation, due to its simplicity, of an ILO is shown in Fig. 3.5 where the reference signal is injected as a current between both branches of a differential LC oscillator [9, 63]. However, despite having a fairly straight forward implementation, the ILO modeling and analysis is not simple since the synchronization process is highly non-linear. There are two approaches to study the circuit; a frequency based analysis and a phase based analysis. Both will be briefly discussed.

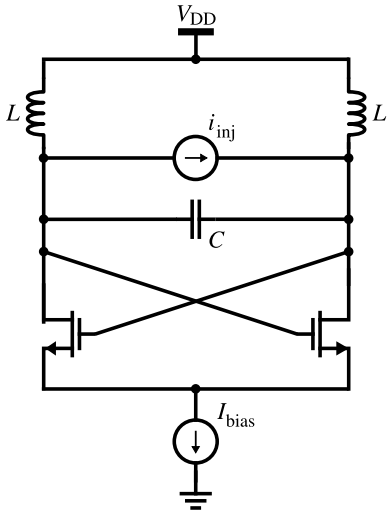

Figure 3.5: Injection-locked LC oscillator [9, 63].

3.3.1 Frequency-domain models

Some information on the synchronization phenomena can be extracted by analyzing the synchronized oscillator once in steady-state (see eq. 3.1). By doing that it is possible to construct a frequency model of the synchronization mechanism and derive simple relations between significant parameters like offset frequency and injection level.

3.3.1.A Adler's model

Lets us consider the simplified model for the synchronized LC oscillator shown in Fig. 3.6 [10]. It is composed of a nonlinear gain block and a linear filter that suppresses frequencies far from the frequency of oscillation.

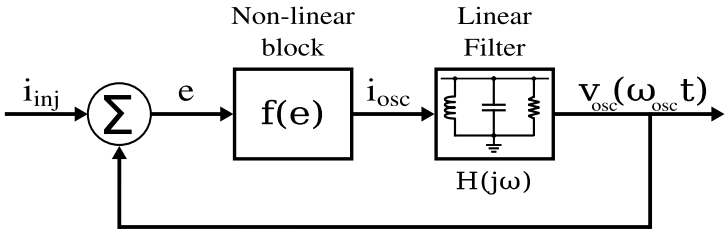

Figure 3.6: Injection-locked LC oscillator high-level model.

The model states that the current flowing through the tank, i_{osc}, is a non-linear function of the injected current, i_{inj}, (see non-linear block in Fig. 3.6). It is difficult to describe the non-linearities and the tank current magnitude across time however, it is still possible to achieve some insight on the process of synchronization by considering the following:

- As aforementioned the assumption of linearity is valid for the LC oscillator. This means that is possible to neglect the harmonic content that is generated by the non-linear block and analyze only what occurs at the frequency of oscillation ω_0.
- Phasors can used to understand the synchronization process since they simplify the characterization of the signal that results from the sum of two other signals with different amplitudes, frequencies and phases which is very difficult to accomplish using analytical methods.

The process of synchronization can be illustrated and analyzed as shown in Fig. 3.7.

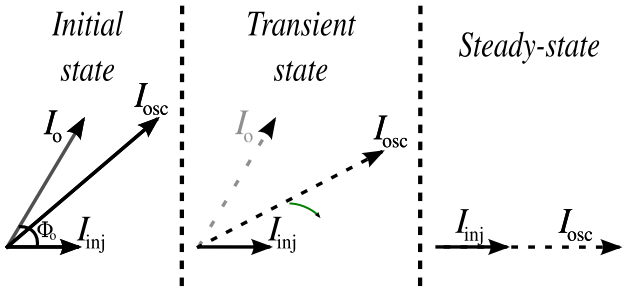

Figure 3.7: Depiction of the currents evolution until synchronization.

where I_{inj} is the instantaneous amplitude of the injection current, I_{osc} is the instantaneous amplitude of the current going through the tank and I_0 is the initial value for that current (in the absence of injection).

The oscillator once under injection suffers a phase shift since the current flowing through the tank changed (which means the resonant condition, a zero phase shift, no longer occurs at the free-running frequency). The oscillator will compensate the induced phase shift by shifting the oscillation frequency (check the transient state in Fig. 3.7). From the free-running frequency, ω_0, the oscillator will converge to a new frequency where the phase-shift is suppressed (check the steady-state in Fig. 3.7). The frequency translation occurs until the resonant frequency coincides with the frequency of the injected signal, $\omega_{osc} = \omega_{inj}$.

With this in mind it is possible to derive the following phase variation [10]:

$$\frac{d\phi(t)}{dt} = \Delta\omega - \frac{\omega_0}{2Q}\frac{I_{inj}}{I_0}\sin\left(\phi_0\right) \tag{3.2}$$

where ϕ_0 is the initial phase-difference and Q is the quality factor for a resonant network. When in steady state $\omega_{osc} = \omega_{inj}$ and:

$$\frac{d\phi(t)}{dt} = 0 \tag{3.3}$$

For an orthogonal relation ($\phi_0 = 90°$) between the oscillator and the injected current (where synchronization does not occur), the relation in eq. 3.2 can be simplified to determine the locking range:

$$\omega_L = \frac{\omega_0}{2Q}\frac{I_{inj}}{I_0} \tag{3.4}$$

Some remarks follow:

- Information of the locking range is obtained even though the evolution of the current i_{osc} amplitude across time is not known.
- This approximation is only valid for weak injection, where $I_{osc} \gg I_{inj}$.
- The model assumes sinusoidal synchronization signal.
- The locking range increases with the power of the injected signal.
- The injection level automatically sets the maximum frequency that the synchronization signal might present.
- The quality factor of the oscillator can be adjusted in order to surpass any limitations on the amplitude and frequency tunability of the injected signal generator as shown in Fig. 3.8.

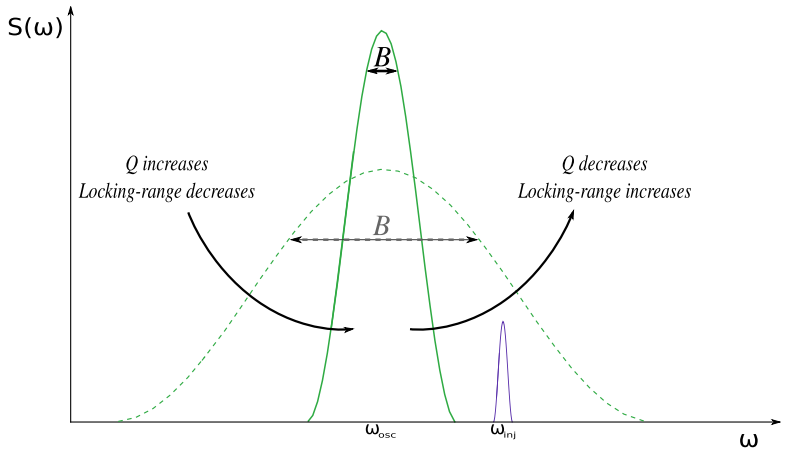

Figure 3.8: Quality factor vs locking-range.

By the end of the synchronization process, the injected and the oscillator signals show the same frequency (with a residual phase difference similar to what is found in the PLL). This means that the spectrum of the ILO will have a correlation with the one of the injected signal. Knowing also that the locking range establishes the maximum frequency where, for a given magnitude, the injected signal is still capable of conditioning the phase of the oscillator, a few considerations are possible regarding the phase-noise of the ILO (see Fig. 3.9).

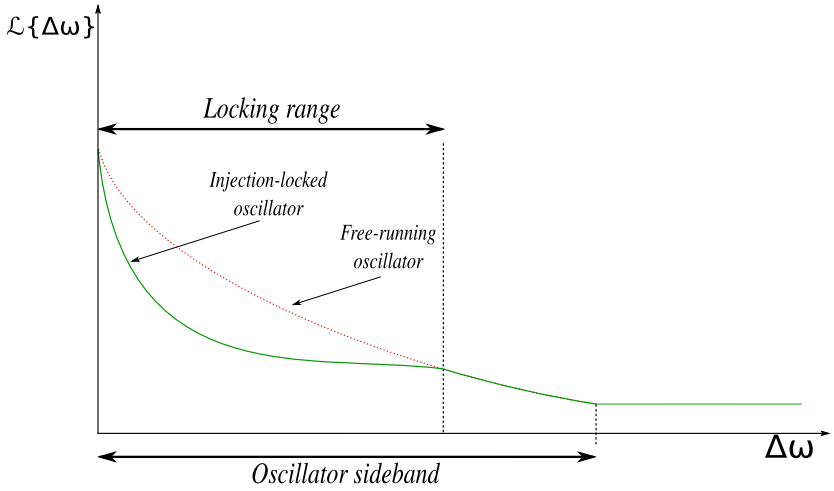

Figure 3.9: Phase-noise improvement within the locking-range.

It is within the locking-range the oscillator tracks the phase of the reference. Within this range the ILO acts as low-pass filter to the phase-noise of the synchronization signal as represented in eq. 3.5 [8, 9].

$$\mathcal{L}_{sync}(\Delta\omega) = \mathcal{L}_{free}(\Delta\omega)\frac{\Delta\omega^2}{\Delta\omega^2 + \omega_L^2} + \mathcal{L}_{inj}(\Delta\omega)\frac{{\Delta\omega_L}^2}{\Delta\omega^2 + \omega_L^2} \tag{3.5}$$

By observing eq. 3.5 it is possible to conclude that it is desirable to have the locking range increased as much as possible to also improve the phase-noise at the farthest offsets.

The Adler's model is based on the observation of the synchronized oscillator and it offers an intuitive and simplified description of the synchronization process. However, since it is a frequency model it does not discloses any information on transient regime and the settling time, which by consequence means it does not allow extraction of information regarding for instance the locking time (which can be of interest to analyze if frequency hoping is intended). Besides that, this model only suits resonators and is not directly applicable to other oscillators like the ones based on hysteresis. The generalization of this model typically comes with an overhead in the complexity with a penalty on the design process [64].

3.3.1.B Miller's model

There is a variation of the Adler's model that is the base for modeling synchronization with different frequency ratios [58]. The generalized Miller model is shown in Fig. 3.10 [9, 65, 66].

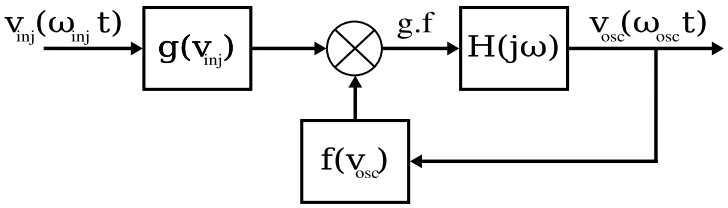

Figure 3.10: Miller injection model.

The functions $f(v_{osc})$ and $g(v_{inj})$ are two memoryless nonlinear functions that can be represented as follows:

$$g(v_{inj}) = \sum_{n=0}^{\infty} g_n . {v_{inj}}^n \tag{3.6}$$

$$f(v_{osc}) = \sum_{m=0}^{\infty} f_m . {v_{osc}}^m \tag{3.7}$$

This model states that the current feeding the tank is the result of a mixing operation. Therefore, if any of the resulting products from the mixing operation, $g.f$ shown in eq. 3.8, fall within the filter passing band, the synchronization is triggered [17, 57, 67].

$$g(v_{inj}).f(v_{osc}) = \sum_{n=0}^{\infty} G_n.\sin(n\omega_{inj}t).\sum_{m=0}^{\infty} F_m.\sin(m\omega_{osc}t) \tag{3.8}$$

This model predicts the existence of three different possibilities for synchronization according the ratio of frequencies:

- Fundamental synchronization: $\omega_{inj} = \omega_{osc}$
- Sub-harmonic synchronization: $n\omega_{inj} = \omega_{osc}$
- Super-harmonic synchronization: $\omega_{inj} = m\omega_{osc}$

Synchronization occurs when the free-running oscillator frequency ω_0 and the frequency of injected signal ω_{inj} are such that $m\omega_0 \approx n\omega_{inj}$. A synchronization of order n:m takes place if the frequency of the oscillator shifts until it reaches [57]:

$$\omega_{osc} = \frac{n}{m}\omega_{inj} \tag{3.9}$$

Harmonic synchronization is the base for the implementation of frequency dividers like the one shown in Fig. 3.11 [9, 68].

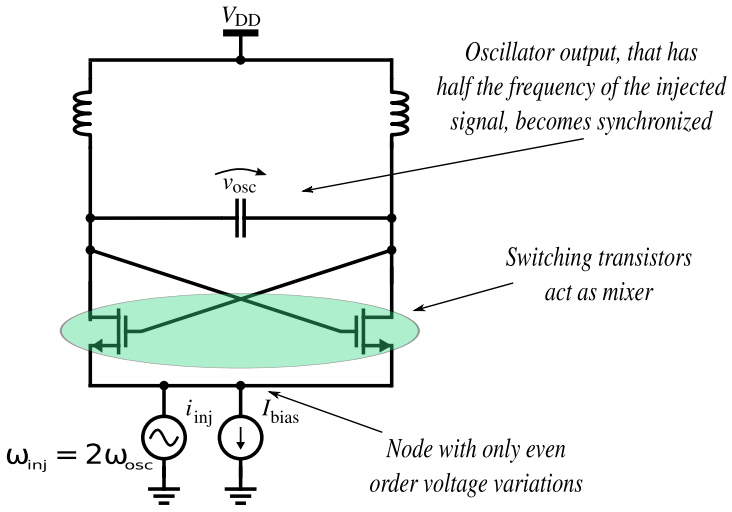

Figure 3.11: Injection-locked divider.

The amplitude of the injected current is determined by the mixer conversion gain [63, 69]:

$$\omega_L = \frac{\omega_0}{2Q} \cdot \frac{4}{\pi} \cdot \frac{I_{inj}}{I_0} \tag{3.10}$$

3.3.2 Phase-domain models

As an alternative to the frequency model there is the possibility to exploit the computational tools at hand to produce high-level phase macro-models of the oscillator. The phase macro models have been of great utility for instance in the design of PLLs by simplifying the analysis and simulation stages (it allows to focus into system-level challenges like loop stability). Phase-modeling allows to characterize the way the oscillator process certain stimulus into a phase-shift while making transparent any involved non-linearities and time-dependencies (allowing the oscillator to be simply described, for instance, in Verilog). Because the used methodologies are simulation-assisted they offer higher accuracy and can be applied to any combinations of topology/injection type. In the following sections a couple of methods will be discussed.

3.3.2.A The ISF-based model

One possibility to the study the induced phase-shifts on the oscillator during the synchronization process is to use an ISF-based approach (see section 2.1.4.B in Chapter 2). However, this method is not directly applicable because the ISF is computed based on the oscillator response after the settling time has passed and it will never present a frequency different from the one of the unperturbed oscillator (in other words $\phi(t)$ does not variate linearly with time and so it cannot describe frequency shifts). In [70] a methodology is proposed that turns possible to use the concept of the ISF in order to capture the synchronization phenomenon that results from injection. This is done by discretization of the injection signal approximating it as sequence of pulses and consequent computation of the superposition of the responses to each pulse as depicted in Fig. 3.12.

An ISF function is computed for each impulse and has a dependency on the response to the previous impulse. The total accumulated phase-shift can then be determined as following:

$$\phi(t) = \int_{-\infty}^{t} \Gamma(\tau + \phi(\tau)) i(\tau) d\tau \tag{3.11}$$

where

$$i_{inj}(t) = A\cos\left(\omega_{inj}t + \theta\right) \tag{3.12}$$

By using this approach the phase deviation of the oscillator, $\phi(t)$, will now variate with time ($\phi(t) \propto t$) and by consequence describe frequency shifts on the oscillator output.

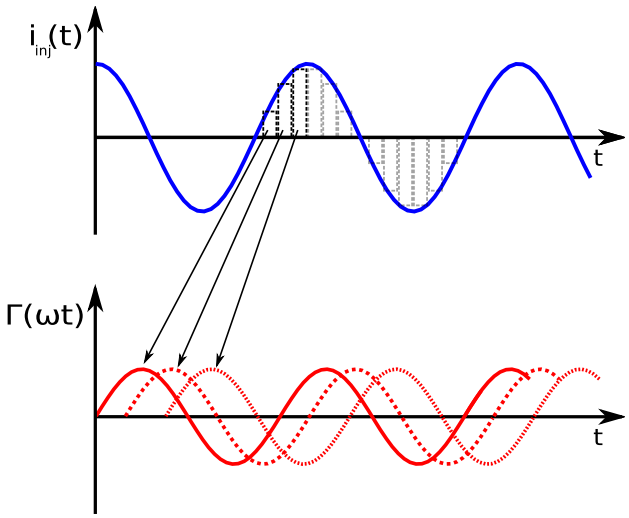

Figure 3.12: Time-shifting of the ISF.

Remembering eq. 3.9 it is possible to conclude on the phase shift that corresponds to a synchronization of order 1:m [57, 70]:

$$\phi(t) \approx \frac{\omega_{inj} - m\omega_{osc}}{m\omega_{osc}}t \tag{3.13}$$

By replacing 3.12 in 3.11 and equating to 3.13 it is possible to define the 1:m synchronization region:

$$\frac{\Gamma_m A}{2} \geqslant \left|\frac{\omega_{inj} - m\omega_{osc}}{m\omega_{osc}}\right| \tag{3.14}$$

where Γ_m is the magnitude of the nth Fourier component of ISF.

The ISF-based phase macro-model allows to predict the resulting phase-shift from the injection of weak and short-duration impulses. It avoids complex mathematical analysis by handing the complexity to computational tools. This is done resorting to spice tools and numerical methods which means this method allows to acquire the injection-locking region regardless the oscillator topology. However, even though this method has a general application, the ISF is design-specific and bias dependent which means it is not suitable to be applied on oscillators that change their time-pattern across their tuning range, like it often happens with RC oscillators (as the

frequency is increased their output tends to go from a trapezoidal-wave to a sine-wave).

3.3.2.B The phase-transfer model

Following also a simulation-assisted approach is the phase-transfer model where its parameters are extracted resorting to transient simulations [71]. This approach allows to acquire information regarding the oscillator time response such as lock time, locking range or tracking bandwidth.

The process starts by defining a phase-domain response (PDR), $P(\phi)$, for the oscillator that is function of the relative phase difference between the free-running oscillation and the reference signal. The phase difference is defined as following:

$$\phi(t) = \theta_{inj}(t) - \theta_{osc}(t) \tag{3.15}$$

The PDR function is extracted from a set of transient analysis, by observing the obtained phase-shift on the ILO output as result from the injection of a single period of the reference signal at different initial phase-differences (see Fig. 3.13). This procedure is similar to the ISF in the sense that is dependent on the injection signal, the design of the oscillator and the bias conditions (if the injection signal changes the PDR function must be redone).

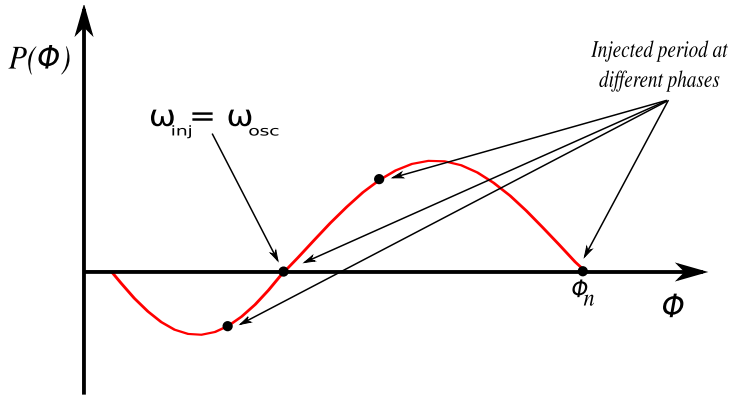

Figure 3.13: PDR function characterization.

Once the PDR is determined a behavioral model can be obtained, which is constructed on discrete events that account for injections of one period of the injection signal as shown in Fig. 3.14. It is also assumed that under the absence of injection the oscillator phase resumes the free-running scenario hence the inclusion of the phase term $\frac{2\pi N\Delta\omega}{\omega_{osc}}$.

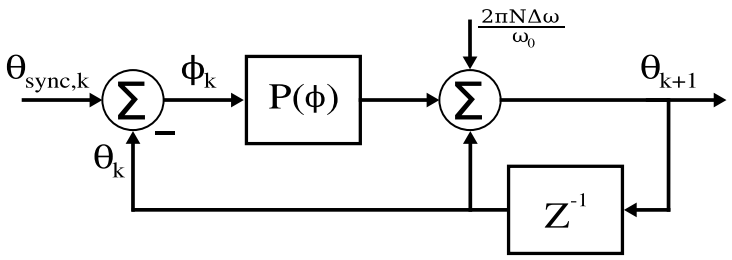

Figure 3.14: Non-linear behavioral model of the ILO.

The output phase-shift is given by:

$$\theta_{k+1} = \theta_k + P(\phi_k) + \frac{2\pi N \Delta\omega}{\omega_{osc}} \tag{3.16}$$

where N is the number of cycles and $\Delta\omega$ is the frequency offset.

Once the ILO is locked it is possible to define a Steady-State Phase Shift that compensates the phase difference between the oscillation and the injected signal as follows:

$$P(\phi_{ss}) = -\frac{2\pi N \Delta\omega}{\omega_{osc}} \tag{3.17}$$

Since the ILO can only track a synchronization signal that produces a phase shift large enough to compensate the difference in their frequencies, the locking-range can be expressed as follows:

$$\Delta\omega = \frac{P_{max} - P_{min}}{2\pi N} \tag{3.18}$$

This approach, unlike the ISF-based one, allows to predict the behavior of ILO under any type of injection scheme. However, since it is obtained relying in transient simulations it is time-consuming and it is most likely to get worse with the increase of the oscillator topology complexity. It is also expected the accuracy to be highly dependent on the number of performed observations in order to characterize the PDR function.

3.4 Discussion

Although the implementation of an ILO is possible with reduced circuit complexity, the phenomenon of synchronization is highly non-linear and time-dependent, thus far from being simply modeled. There has been a few attempts to develop comprehensive and intuitive models capable of offering a better understanding of the phenomenon, allowing to explain, quantify and predict the performance with

significant accuracy and level of applicability (considering several levels of injection, offset frequency, harmonic synchronization, etc).

It must be taken into account that what is desirable is that the modeling and analysis of the ILO to be done with reasonable compromise between accuracy and the complexity and having in mind that the case study is an RC oscillator.

Taking that into account, lets first observe the possible modeling options:

- Frequency Modeling:
  - Simple.
  - Does not provide insight over the settling time.
  - Not general, must be adjusted according the topology.

- Phase Modeling:
  - Complex and time-consuming.
  - Allows to extract more information than the frequency model.
  - Suitable for any topology.

RC oscillators are known to synchronize in a few periods (and in certain conditions in just one period) implying that the determination of time-quantities like the settling time or locking time is not a real concern, allowing to overlook the relevance of using phase-models [72]. Because the target should be to evaluate changes in the locking range (see Fig. 1.2) the use of the frequency model is the best option to support the analysis of the ILO on the account of its simplicity.

One other thing to bear in mind is that since the RC oscillators are capable of a wide range of time patterns in virtue of its regime of operation (from NL to QL as depicted in Figs. 2.30 and 2.31), phase-modeling would imply wrong estimations of the phase-shifts across the tuning range (each extracted model is only suitable to a specific set of operation conditions). This means that the use of phase-modeling would require extra effort without any practical advantage.

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4

Design of an ILO Based on an RC Oscillator

Preamble

In this chapter the challenges involved in the implementation of an ILO are discussed. It concludes on the most suitable design approach taking into account the available references and the oscillator circuit.

Contents

The implementation and performance of an ILO is constrained by the characteristics of the synchronization signal and by the response of the oscillator to a given stimulus. Thus, two points are important to discuss when planning the design of the ILO in order to optimize its performance:

- What kind of references are available?
- How can the impact of the reference signal be improved?

4.1 Reference signal generation

For the implementation of an ILO two possibilities can be considered to be used as a reference generator, the crystal and the STO, that will be discussed in the following sections. It is also discussed how the characteristics of these references impact the properties of the ILO.

4.1.1 Crystal oscillator

The use of crystals to implement a timing reference relies on a piezoelectric principle [11, 12]. This phenomena refers to the mechanical distortion that occurs when a voltage is applied to an electrode near or on the crystal (see Fig. 4.1). Because the crystal has elastic properties it is able to return to its initial state (generating an opposing voltage), this means that when submitted to an electric field the crystal vibrates.

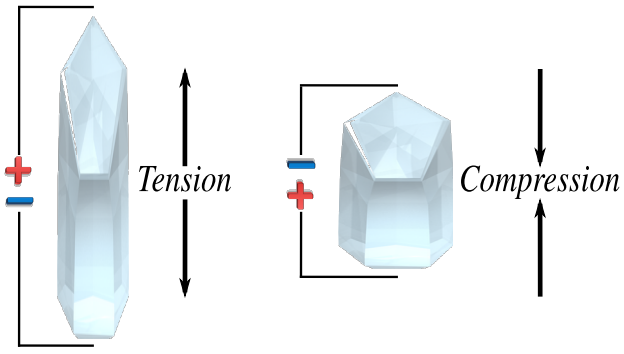

Figure 4.1: Piezoelectric phenomena on the crystal.

The crystals, are typically, cuts of quartz and ceramic with electrodes connected on each side. They are relevant in modern frequency synthesis due to its precise resonant frequency that is guaranteed by the low dependence of the crystal elastic constants and size with the temperature variation.

The crystal electrical symbol is shown in Fig. 4.2.

Figure 4.2: Crystal electrical symbol.

As it returns to its previous shape the crystal generates an opposing voltage, which means that the mechanical properties of the crystal can be translated into a simple RLC circuit as shown in Fig. 4.3.

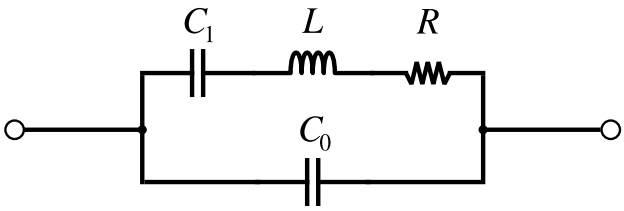

Figure 4.3: Crystal electrical model.

The Laplace transform of the equivalent impedance is:

$$Z_{xo}(s) = \left(\frac{1}{sC_1} + sL + R\right) \Big\| \left(\frac{1}{sC_0}\right) \tag{4.1}$$

This allows to identify in the crystal two resonant frequencies (where reactances cancel each other) [73]:

$$\omega_s = \frac{1}{\sqrt{LC_1}} \tag{4.2}$$

$$\omega_p = \frac{1}{\sqrt{L\left(\frac{C_1 C_0}{C_1 + C_0}\right)}} \tag{4.3}$$

where ω_s is the series resonant frequency or fundamental frequency and ω_p is the parallel resonant frequency. The crystal is a combination of a series and parallel resonance circuit, but depending on the circuit where is going to be used, it can also work as either an inductor or a capacitor, as shown in Fig. 4.4. This means that by adding load capacitances the frequency of oscillation can be slightly adjusted (referring to the range of operation shown in Fig. 4.4).

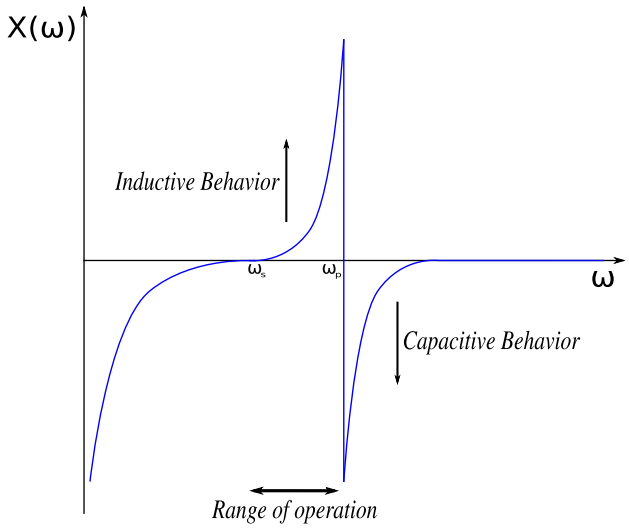

Figure 4.4: Crystal reactances.

The main advantage of the crystals is that their fundamental frequency it is defined by the cut and it does not change much with temperature. In fact crystals are shown to have Q factors ranging from 10000 to 100000 (in the MHz range) much higher that the typical value for an integrated inductor which is roughly around 10 (in the GHz range).

The crystal by itself does not oscillate unless is placed in the feedback path of a amplifier as seen for the harmonic oscillators (see Fig. 2.12) [13]. The crystal oscillator or piezoelectric resonator is shown in Fig. 4.5. This oscillator is capable of exhibit very low phase noise and stable frequency.

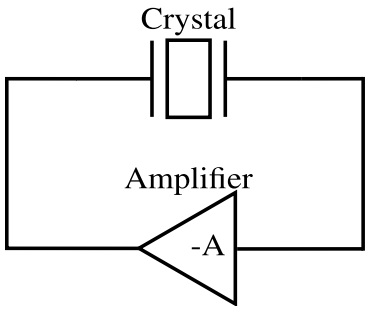

Figure 4.5: Crystal oscillator.

Because the fundamental frequency is defined by the cut it means that the maximum obtainable frequency is constrained by the fabrication process (high frequencies require small and thin crystals). The practical maximum fundamental frequency is shown to be around 30 MHz [74, 75].

There are ways to achieve a higher frequency of operation. The cut and shape

of the crystal not only defines the fundamental but it also determines if the crystals vibrate at more than one frequency, which are called overtones and appear at odd multiples of the fundamental frequency. Other option is to generate harmonics of the fundamental frequency, which is achieved by producing crystals with non uniform thickness. Both options, however, imply additional LC circuits for selectivity and are still limited to a few hundred of MHz, which is still far from this work desirable GHz range.

One other practical limitation when using this type of reference is the impossibility of significantly adjust of the frequency of operation. The range of operation shown in Fig. 4.4 is typically of a few MHz and the higher frequencies are always multiples of the fundamental.

4.1.2 Spin transfer torque nano-oscillator

The STO is a tunable nano-scale microwave integrated current-controlled oscillator which offers extremely wide tunability. The principle of operation of the STO consists on the transfer of angular momentum to the magnetization of a thin magnetic layer [76, 77]. The STO operation is based on two spintronic effects: Spin transfer torque (STT) and magnetoresistance. The STT effect guarantees a magnetic compensation mechanism and the magnetoresistance guarantees an hysteresis mechanism on the STO structure.

4.1.2.A Spin transfer torque

In a magnetic multilayer device, the angular momentum (also known as spin) can be transferred by electrons from one magnetic layer to another, which exerts a torque on the local magnetization. The STT effect consists in guaranteeing the precession of magnetization (torque transfer) of a nano-scaled magnetic layer by using a spin-polarized current. A typical multilayer structure of STO is shown in Fig. 4.6 [14]

The structure is composed of two magnetic layers separated by a thin non-magnetic barrier called spacer. The bottom layer is the one with a fixed magnetization, M_p, is named polarized layer and the remaining magnetic layer whose magnetization is free to rotate, M_{free}, is named as the free layer.

The STT effect is triggered by injecting a unpolarized current on the structure. A spin-polarized current is generated on polarized layer and the electron spin is transfered to the free layer which causes a torque on the local magnetization. The exerted torque will compensate for the magnetization damping in the spacer.

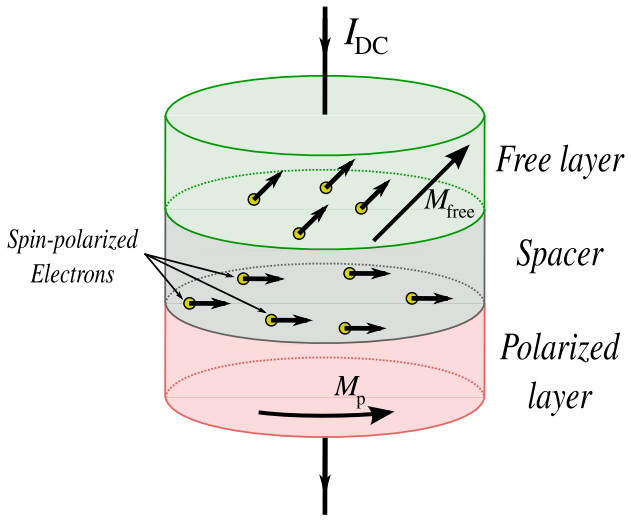

Figure 4.6: Typical STO structure.

The compensation of the magnetization damping, however, is not enough to sustain oscillations [76, 77]. In order for oscillations to occur the rotation of the magnetization on the free layer must periodically alternate orientation. This can be guaranteed by the magnetoresistance effect [15].

4.1.2.B Magnetoresistance

This effect refers to the observed resistance of the non-magnetic layer according the relative orientation of the magnetization of the magnetic layers. Two states can be observed, a parallel and an anti-parallel as depicted in Fig. 4.7.

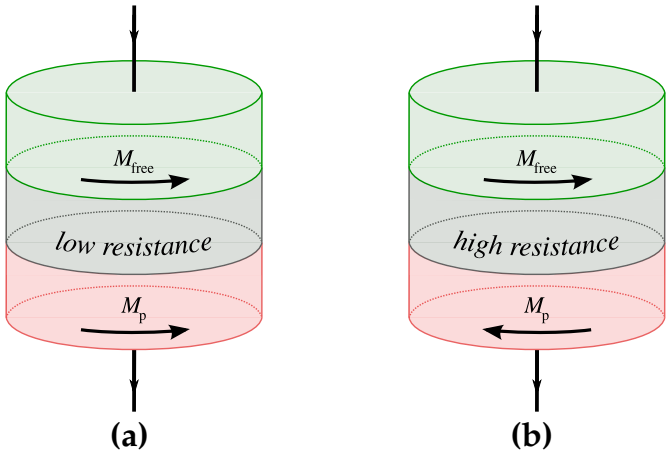

Figure 4.7: Magnetoresistance effect: (a) Parallel state. (b) Anti-parallel state.

When in parallel state the magnetic layers are aligned and the magnetic precession is done with low effort. When in anti-parallel state electron reflection occurs during the magnetization precession, which is translated into a large resistance state [15]. Only by combination of the STT and the magnetoresistance effects oscillations on STO can be sustained.

These structures are known to be capable of sustaining oscillations in the GHz range and can be tunned by either a current or a magnetic field. The fact that hey have also high tunability (dependent on the variation of the magnetoresistance), low cost, small footprint (smaller than 100 μm) and compatibility with CMOS technology makes this structure an interesting candidate to be used as a radio-frequency oscillator.

4.1.2.C Types of STO

STO are classified according its magnetoresistance that can either be a tunneling magnetoresistance (TMR) where the the barrier layer is a thin insulator (hence the tunneling), or a giant magnetoresistance (GMR) where the barrier is a metallic spacer. An STO with TMR is named a magnetic tunnel junction spin torque oscillator (MTJ STO) and an STO with GMR is named a Spin valve spin torque oscillator (SV STO). Both are capable of high frequency of operation in the GHz range unlike crystals with a tunability range over 30 % which is higher than typical LC oscillators which show tunability in the range of ±10 %. However, this technology its still on its early stages of development and show a few limitations:

- The maximum output power is below -40 dBm and typical amplitudes are comparable to CMOS noise rms level, of the order of $nV/\sqrt{Hz}$;
- They suffer from spectral impurities in terms of frequency fluctuations;
- Poor uniformity and low yield;

Typically, MTJ STO offer larger output power and the SV STO offer higher frequency of operation and better spectral purity but lower output power [14, 78, 79]. MTJ STO are capable of supplying an output power between -60 dBm and -40 dBm on the account of its larger magnetoresistance [80]. However, they present frequency fluctuations within closer offsets (< 10 MHz) of the oscillation frequency hence they show Q factors on the order of 100. By its side the SV STO produce an output signal with significantly less power, around -70 dBm, on the account of a smaller magnetoresistance but they are capable of exhibit better frequency stability reaching higher Q values (theoretically up to 18000).

Assuming that the drawbacks will be mitigated in the near future, the use of this technology to implement the ILO should grant key advantages. First, because its compatible with CMOS process it can be integrated and the losses from the PCB or packaging can be avoided. Second, because it is current biased a common biasing structure can be used for both oscillators, which allows to reduce the overall footprint and power consumption of the ILO. Finally, because it has high frequency and high tunability, it can be used to achieve a cheap multi-band, multi-standard receiver.

4.1.3 Discussion

In Tab. 4.1 a comparison is shown between the two possibilities for the signal generation.

Table 4.1: References comparison.

Integrable References	Advantages	Disadvantages
Crystal Oscillator	Mature Technology Low Cost High Q (MHz Range)	Low Frequency (MHz) Low Tunability Not compatible with CMOS
Spin Torque Oscillator	Low Area High Q (GHz range) High Frequency (GHz) High Tunability Compatible with CMOS	Low Yield Frequency fluctuations

By observation of Tab. 4.1 it is possible to dismiss the use of the crystal oscillator alone by its frequency of operation since the target is the GHz range. Another important aspect relates to its limited tunability which is even smaller than typical ranges of LC oscillators. Finally, only the STO is compatible with standard CMOS, which will allow a fully integrated ILO.

Despite its drawbacks the STO is regarded as the best solution for the implementation of the ILO. The resulting hybrid oscillator is expected to show a wide range tunability in the GHz range with a phase-noise performance somewhere between the one of an LC oscillator and that of a crystal oscillator.

4.2 Improving the impact of the reference signal

Admitting that the ILO is going to be implemented using an STO, which as previously referred produces a very weak output, two things must be taken into account; first the frequency model can be used to support the analyses of the ILO and second, it is possible that the reference signal level is not enough to guarantee phase-noise improvement throughout the oscillator sideband. Therefore, it would be advantageous to study how should it be possible to magnify the impact of the signal without using any interface block like a wideband amplifier.

When discussing the impact of the synchronization signal two aspects are critical:

- How wide are the oscillator spectral components (see $H(j\omega)$ in Fig. 3.10 and Fig. 3.6)?
- What is the injection strength (relation between the oscillator current and the injected current, see Fig. 3.4)?

By looking at eq. 2.40 and Fig. 2.13 its possible to infer the relation between quality factor and bandwidth, and even tough there are techniques that can be used to extend the locking range when using LC oscillators (like direct injection as seen in [81–83]) they are still reduced on the account of the narrow spectral component that is generated by the oscillator.

By its side RC oscillators present a theoretical maximum quality factor of one [8]. This is where the RC oscillators take some advantage over LC oscillator because they have spectral components with larger bandwidth when compared with LC oscillators they are capable of being synchronized with smaller amplitudes at further offsets (see Fig. 4.8).

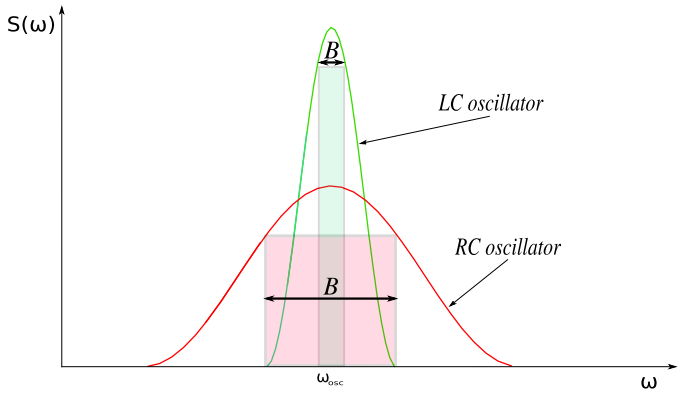

Figure 4.8: Bandwidth differences between LC and RC Oscillators.

One other aspect of these oscillators that is relevant for the maximization of the impact of the reference signal relates to the fact that, as non-linear oscillators, they can show a rich spectral content, as depicted in Fig. 2.30. We know, by looking at Fig. 2.10, that a non-linear oscillator is sensitive to stimulus occurring in the vicinity of multiples of its oscillation frequency and from the observation of the model in Fig. 3.10 we know that, if any inter-modulation product, that results from injection, is not filtered out by the oscillator synchronization is triggered.

This means that the synchronization to a given reference signal will occur as long as the reference signal is injected at any of the multiples of the free-running frequency, so that it produces an inter-modulation product at low frequencies (remember that the RC oscillator has a low-pass response, ideally an integrator), as depicted in Fig. 4.9.

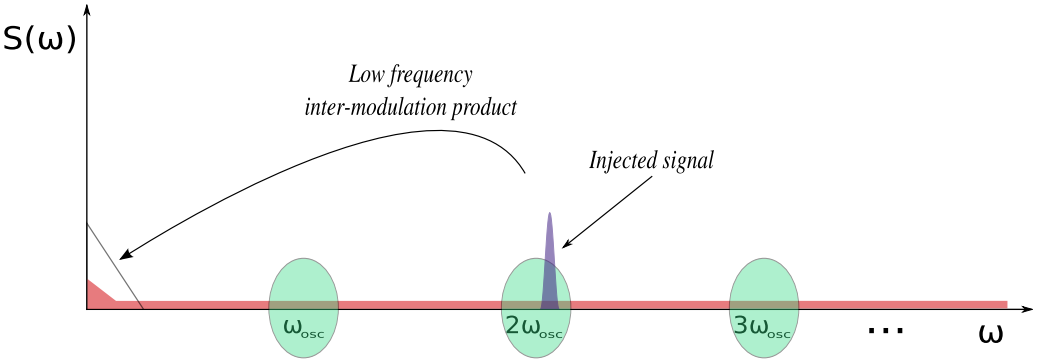

Figure 4.9: Possible injection frequencies for the RC oscillator.

The existence of this large number of spectral components becomes an advantage because if harmonic injection is done using the high order harmonics, it is possible to achieve higher injection strengths for the same level of injection. As the order increases, better ratio can be obtained, as shown in eq. 4.4.

$$\left|\frac{I_{inj}}{I_{osc}}\right|_{\omega_{osc}} << \left|\frac{I_{inj}}{I_{osc}}\right|_{3\omega_{osc}} << \left|\frac{I_{inj}}{I_{osc}}\right|_{5\omega_{osc}} << \ldots << \left|\frac{I_{inj}}{I_{osc}}\right|_{n\omega_{osc}} \tag{4.4}$$

4.3 Design methodology for the ILO

The desirable target specifications for the prototype, taking into account a conservative estimation of the maximum output power of the STO are summarized as follows:

- I/Q outputs (image cancellation)
- Frequency of operation: 2.4 GHz (ISM bands)
- Locking Range: > 1 MHz (for an injection power below -40 dBm)
- Phase-noise: < -100 dBc/Hz@1 MHz (typical phase-noise of an RC oscillator at the GHz range)

The design challenges arise from the necessity of improving the impact of the reference without using a wideband amplifier and the performance of the CMOS oscillator at high frequency of operation:

- Determine most suitable injection point.
- Find optimal point between the injection strength and injection frequency.
- Design the RC oscillator at high frequency of operation with good balance between phase-noise and power consumption.
- Obtain design guidelines.

Although some design practices can improve the impact of the reference signal there is so much that can be done. The locking range will hardly cover the full extent of the oscillator sidebands due to the very weak reference (remember eq. 3.4 and 3.5). Which means a two step design methodology should be employed to guarantee that the phase-noise is improved at all offsets:

- **Step 1 - PN correction at the closer offsets using injection locking:** Study harmonic synchronization and injection points. Discuss on the feasibility of using an STO as signal reference given its low output power. Identify optimal injection signal level and frequency that allow to correct the close-in phase-noise, which is dominated by flicker noise (see Fig. 2.8).
- **Step 2 - PN correction at further offsets with design optimization:** Study the RC oscillator and identify design orientations to improve the performance at high frequency. Reduce the white noise impact to improve the phase-noise at the further offsets.

Taking into account the challenges and design methodology its important to identify which topology of RC oscillator should be used as base circuit. Amongst the topologies of RC oscillators, the ring oscillator is the one typically subject of greater interest. This comes as a consequence of their simpler implementation, simpler analysis and higher practical performance when comparing with the remaining. However, for the purpose of implementing an RC oscillator based ILO, the relaxation oscillator can be shown to be a more viable option:

- Wider choice for injections points. This oscillator has injection points with distinct characteristics, which allows different injection schemes (e.g. nodes with only even order spectral components) that may be advantageous.
- The correction of the phase-noise at the furthest offsets should not be accomplished at the expense of other important parameters like energy consumption or frequency. This oscillator has, theoretically, the better performance amongst the RC oscillators, which should help to mitigate the trade-offs [18, 19].

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5

Weak Injection in an RC Oscillator

Preamble

In this chapter a qualitative study of synchronization by injection in an RC oscillator is presented. Design guidelines are considered to maximize the impact of the injected signal, and the minimum amplitude required for synchronization is determined.

Contents

The first section of this chapter has the purpose to validate up to which extent the frequency model and respective considerations are applicable to a scenario of harmonic synchronization of a non-linear oscillator. Some work has already been developed concerning this type of oscillators however, it was done for QL operation and for that reason it is not extensible to this work [59]. Therefore the validation process will be mostly qualitative and is intended only to verify linearity on the locking range with respect to the injection level while also verifying how the phase-noise of the synchronized oscillator is impacted by the phase-noise of the reference. The observations and conclusions will drive the design orientations of a circuit prototype.

5.1 Validation of the theoretical assumptions

The validation process consists in assessing what are the differences in performance of the ILO for different injection schemes, odd and even, and different injection orders, while considering equal injection strengths. The first step to achieve that is to design a relaxation oscillator suitable to validate harmonic synchronization (shown in Fig. 5.1), meaning that it has to operate in a NL regime. In order to guarantee the NL behavior the circuit is designed to operate at the lower end of the GHz range, oscillating at frequency of 1 GHz (due to parasitic effects the oscillator tends to move towards a sinusoidal operation with the frequency increase). Afterwards all the current components magnitude up to the 5^{th} order harmonic are determined. This is done using PSS analysis and confirmed using a transient analysis (and performing a coherent dft to avoid spectral leakage). Once the magnitudes are known it is possible to determine what are the injection signal magnitudes that should be used.

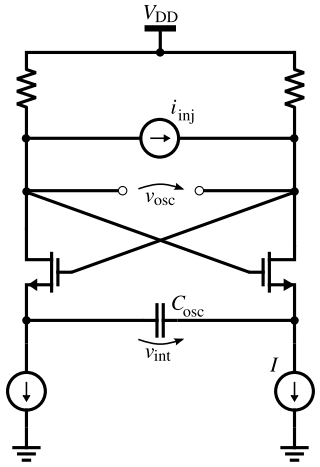


Figure 5.1: Relaxation oscillator with reference current.

5.1.1 Determination of the locking range

To assess the locking range, the frequency of the synchronization signal is increased until the oscillator is no longer able to track the reference phase. Two methods are used, one based on a PSS analysis and one based on a Transient analysis.

5.1.1.A PSS method

If one observe Fig. 4.9, it is possible to conclude that in the event of a large difference between the free-running frequency of the oscillator and the reference signal frequency the inter-modulation products will not trigger any frequency shifting. This means that the oscillator will not synchronize and the output of the oscillator will become amplitude modulated as shown in Fig. 5.2.

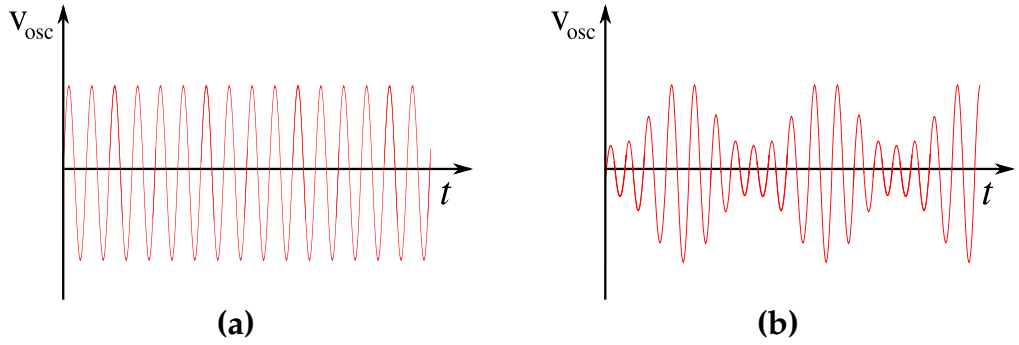


Figure 5.2: Output of the oscillator under injection: (a) Successful synchronization. (b) Failed synchronization.

Therefore, a PSS analysis, in theory, can be used to determine the locking range. Since this simulation determines the circuit periodic operating point it will only converge if the circuit operation is driven by one beat frequency (Fig. 5.2(a)), which means the convergence of the PSS is indicative of synchronization. To determine the locking range it is just required to run a PSS with a sweep and find the offset frequency where the PSS no longer achieves convergence.

The beat frequency should be the expected synchronization frequency and in order for the simulation to converge it must be guaranteed that the circuit has achieved steady-state after injection, parameter *Tstab* (stabilization time) should be much larger that the period of oscillation.

The injection strength is defined as following:

$$k = \left| \frac{I_{inj}}{I_n} \right|_{n\omega_{osc}} \tag{5.1}$$

Taking into account the amplitudes of the oscillator harmonics shown in Tab. 5.1, the injected signal magnitudes are determined considering injection strengths ranging from 0.001 to 0.01.

Table 5.1: Free-running oscillator differential current components amplitudes.

Component	**Amplitude (mA)**
Fundamental	4.87
2^{nd} order harmonic	0.0228
3^{rd} order harmonic	1.3
4^{th} order harmonic	0.0152
5^{th} order harmonic	0.689

Once the injection magnitudes are determined the circuit is simulated to validate harmonic injection up to 5^{th} order injection (only odd order injection is tested at this point). The circuit is simulated with progressively variations of the frequency of the injection signal in small steps. The locking ranges are then obtained by observation of the oscillator output amplitudes identifying at what point convergences are no longer achieved. The obtained locking ranges are shown in Tab. 5.2.

Table 5.2: Obtained locking ranges from the PSS analysis.

k	**Locking Range (MHz)**		
	Fundamental Tone	3^{rd} order harmonic	5^{th} order harmonic
0.01	34	9	n.a
0.0075	24	7	n.a
0.005	14	5	2
0.0025	6	3	2
0.001	n.a	2	n.a

The problem with this approach is that, as the locking ranges become narrow it is nearly impossible to distinguish the successful from the failed convergences. In Fig. 5.3 it is depicted an example where it is possible to visually determine the locking range and in Fig. 5.4 is shown one example where it is difficult to identify the locking range with confidence.

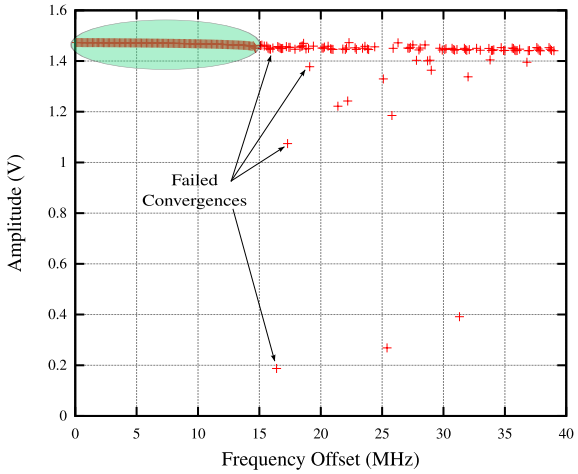


Figure 5.3: Successful identification of the locking range using a PSS analysis.

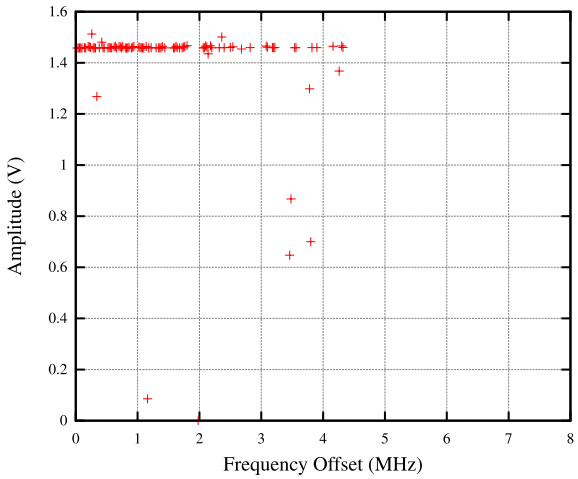


Figure 5.4: Unsuccessful identification of the locking range using a PSS analysis.

5.1.1.B Transient method

In this approach the reference signal is injected during a long transient, and during that time its frequency is slowly varied. The synchronization is verified by observing the frequency error between the oscillator output and the reference. The simulation structure is depicted in Fig. 5.5.

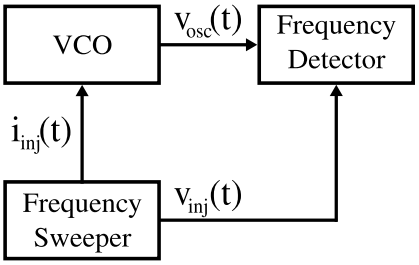


Figure 5.5: Blocks required for the determination of the locking range using a transient analysis.

The necessity for a long transient (in the μs range) is to ensure that the oscillator has time to track every frequency change. The frequency sweeper and the frequency detector are implemented in Verilog-A (see the code in Appendix A). The frequency sweeper implements the function $sin(t^2)$ as shown in Fig. 5.6.

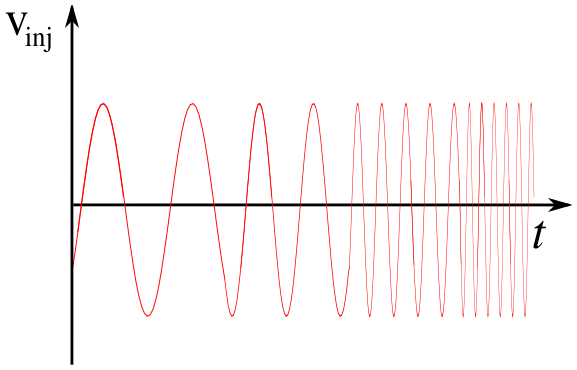


Figure 5.6: Reference signal frequency sweep.

The frequency error for a fundamental synchronization is shown in Fig. 5.7. The frequency error for a 5 th order synchronization is shown in Fig. 5.8. The obtained locking ranges are shown in Tab. 5.3. In Fig. 5.9 is shown the locking ranges as function of the injection strength. In order to better visualize if the use of harmonic synchronization has gains in terms of locking range, the obtained locking ranges are referenced to the one obtained when using injection at the fundamental. The relative ranges are shown in Fig. 5.10.

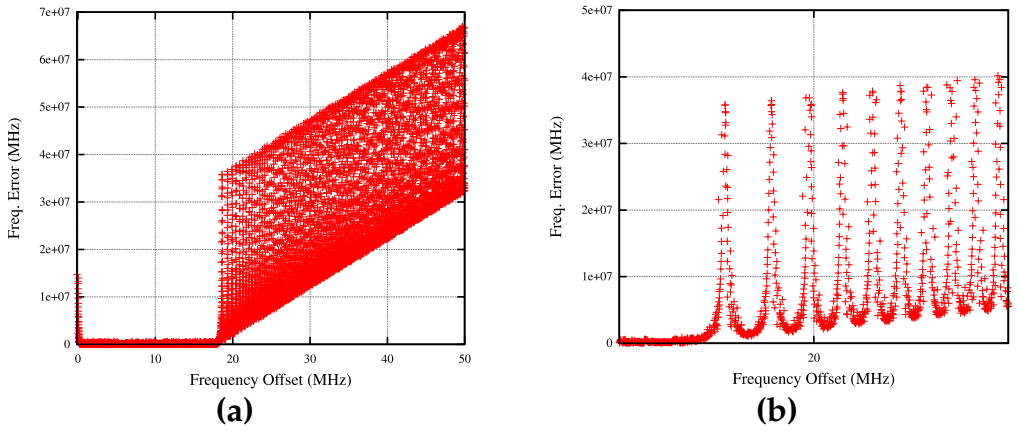


Figure 5.7: Obtained frequency error for an injection at the fundamental: (a) k = 0.005. (b) Detail of the frequency error.

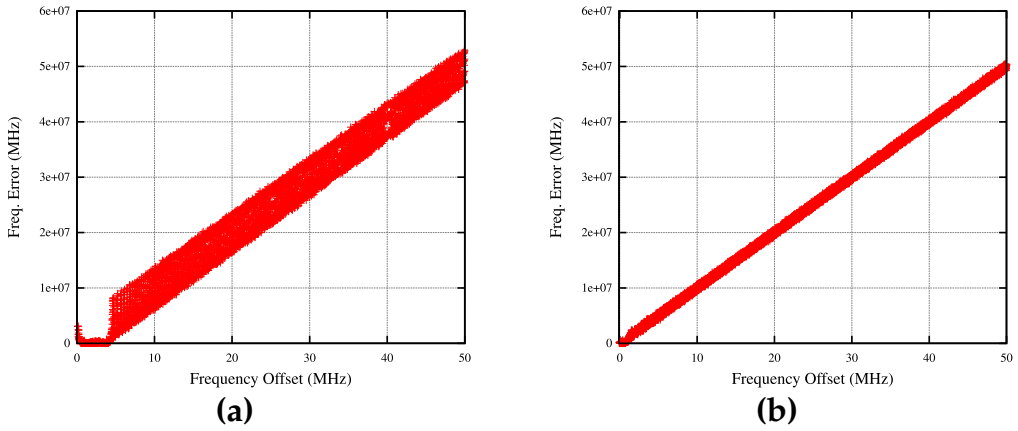


Figure 5.8: Obtained frequency error for 5 th order injection: (a) k = 0.01. (b) k=0.001.

Table 5.3: Obtained locking ranges from the transient analysis considering odd order injection.

k	**Locking Range (MHz)**		
	1^{st}	3^{rd}	5^{th}
0.01	37	10	5
0.0075	26	8	5
0.005	18	5	3
0.0025	10	3	2
0.001	5	2	1

Observing Fig. 5.8 is possible to observe that the maximum frequency where synchronization is still distinguishable despite being small. It is also observable from Tab. 5.3 that the results are similar to the ones shown in Tab. 5.2.

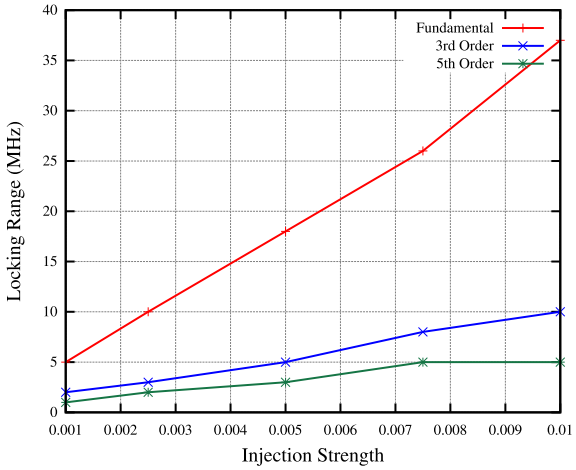


Figure 5.9: Locking ranges for different injection schemes.

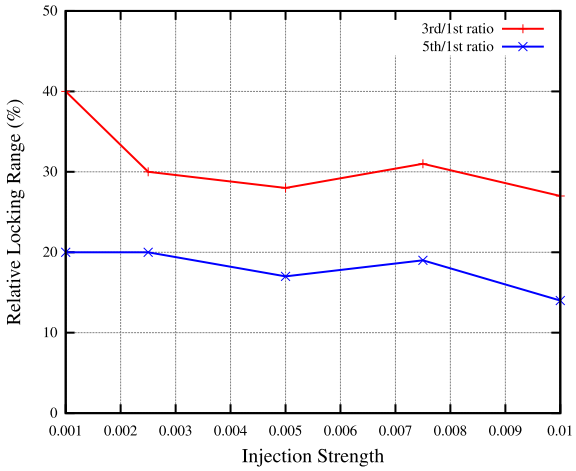


Figure 5.10: Relative locking ranges.

The observation of Figs. 5.9 and 5.10 allows a couple of considerations:

- The locking range seems to vary "almost" linearly with the injection strength despite the fact that the oscillator is in NL mode of operation.
- The locking ranges obtained from using harmonic injection for similar injection ratios are roughly reduced by a factor of $\frac{1}{n}$ (see Fig. 5.10) suggesting that the use of injection at the fundamental frequency is preferable. However, these results also suggest that the use of harmonic synchronization can be beneficial if the reference shows frequency drift. The induced shifts due to this frequency drift should be mitigated by a factor n if higher order harmonic synchronization is used.

The next step is to test harmonic synchronization of even order. The existence of these components imply that the oscillation signal is asymmetric around half period and typically they appear due two reasons: Circuit mismatches (due to process or layout) and harmonic distortion due the use of transistors [9, 84]. Because at this level of design mismatches are not possible, the even order components are solely due to harmonic distortion. Normally, this type of injection is done at circuit nodes where the differential currents are summed back together, however, in this case, the only two nodes available are both reference nodes, which means the voltages are not allowed to change. One way to overcome this is to simultaneously inject the same current on both branches of the circuit.

The obtained locking ranges are shown in Tab. 5.4 and the locking ranges vs injection strength are shown in Fig. 5.11. Finally in Tab. 5.5 the required injection amplitudes for a 10 MHz locking range of all the injection schemes is summarized.

Table 5.4: Obtained locking ranges from the transient analysis considering even order injection.

k	**Locking Range (MHz)**	
	2^{st}	4^{th}
100	22	16
75	18	12
50	14	9
25	9	6
10	6	4

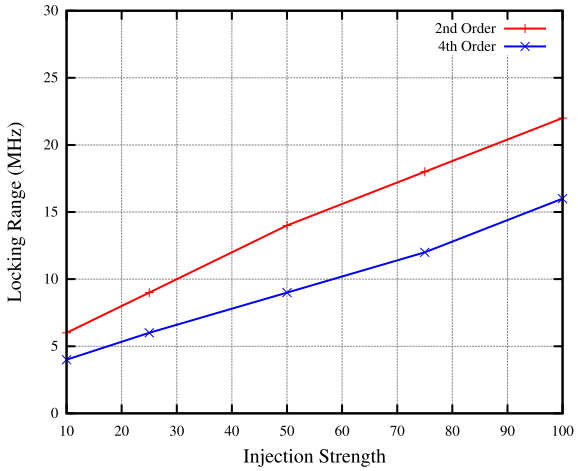


Figure 5.11: Locking range vs injection strength for even order injection.

Through the observation of the results in Tab. 5.4 and Fig. 5.11 allows a couple of remarks:

- The relation between locking range and injection strength remains fairly linear.
- Higher injection strengths are needed to obtain sufficiently large locking ranges.

Table 5.5: Required injection strength for a locking range of 10 MHz.

	Fundamental	2^{nd} order	3^{rd} order	4^{th} order	5^{th} order
I_{inj} (μA)	12	572	13	762	13

By observing the results in Tab. 5.5 a few considerations can be done:

- For an odd order injection scheme the same injection amplitude produces the same locking range despite the order of the odd harmonic. Even though the injection relation is increased, the locking range is scaled down to the harmonic order. This implies that for the same injection level to obtain a given locking range $\Delta\omega$ the injected signal must be injected a frequency $3\Delta\omega$ for a third order injection and at a $5\Delta\omega$ for a fifth order injection.
- The mechanism behind the origin of the even order components it is not the same as the one that gives rise to the odd order components, hence the previously consideration can not be extended.
- The even order components are very small when compared with the remaining (Tab. 5.1), which means that to obtain comparable locking ranges to the cases of odd order injection greater injection currents must be used.

Results indicate that the RC oscillator is in fact capable of being synchronized using very weak signals by using harmonic synchronization. However, in order to fully cover the oscillator sidebands the amplitude of injection has to be increased. This means that if the concern is to maximize the locking range with the least possible injection level there is no advantage in using higher order harmonic injection. However, the results also suggest that the use of harmonic synchronization can be used to mitigate eventual frequency drift on the reference.

5.1.2 Impact of the reference phase-noise

The literature suggests that the phase-noise of the synchronized oscillator, within the locking-range, is dominated by the reference phase-noise (Fig. 3.9). To validate this assumption a reference signal with noise was implemented in Verilog-A (Appendix A). The starting noise levels will be comparable to the noise of the free-running oscillator. This corresponds to worst case scenario where the reference signal is as poor as the oscillator to be synchronized. This is useful to also understand how this approach to a typical two-oscillator coupling.

In order to generate comparable noise it is necessary to first identify the corner frequencies and noise regions of the phase-noise spectrum of the free-running oscillator (Fig. 2.8). Those are depicted in Fig. 5.12.

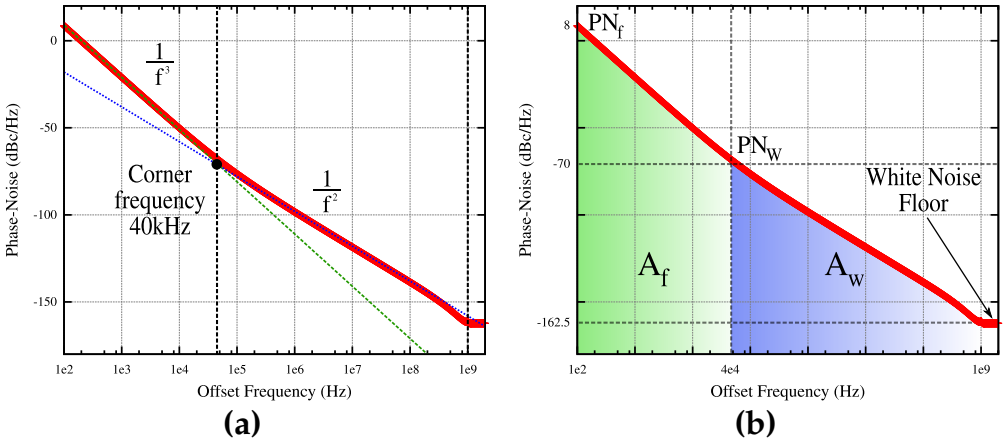


Figure 5.12: Free-running oscillator phase-noise: (a) Corner frequency of the phase-noise. (b) Flicker and white noise regions.

Afterwards is necessary to determine the corresponding jitter [85, 86]:

$$\sigma_f^2 = 2.10^{\frac{A_f}{10}} = 2.\Delta f^2.10^{\frac{PN_{\Delta f}}{10}} \tag{5.2}$$

$$\sigma_w^2 \approx 2.10^{\frac{A_w}{10}} \tag{5.3}$$

where A_f and A_w are the areas of the regions shown in Fig. 5.12(b). The expressions can be simplified to:

$$\sigma_f^2 = 2.\Delta f_f^2.10^{\frac{PN_f}{10}} \tag{5.4}$$

$$\sigma_w^2 = 2.\Delta f_w^2.10^{\frac{PN_w}{10}} \tag{5.5}$$

where Δf_f if the frequency offset where flicker noise starts and PN_f is the phase-noise at that offset. Δf_w if the frequency offset where the integrated white noise starts and PN_w is the phase-noise at that offset (the corner frequency shown in Fig. 5.12(a)).

Finally, the calculated jitter is added to the reference signal as follows (see Appendix A):

$$f_{inj} = f_0 + flicker(\sigma_f^2) + white(\sigma_w^2) \tag{5.6}$$

where f_0 is the nominal frequency, $flicker(\sigma_f^2)$ is a flicker noise contribution of power σ_f^2 and $white(\sigma_w^2)$ is a white noise contribution of power σ_w^2. The phase-noise of the ILO is then simulated, using a PNOISE analysis, for a 1^{st} and 2^{nd} order injection considering the previously determined amplitudes shown in Tab. 5.5. The obtained results are shown in Figs. 5.13 and 5.14.

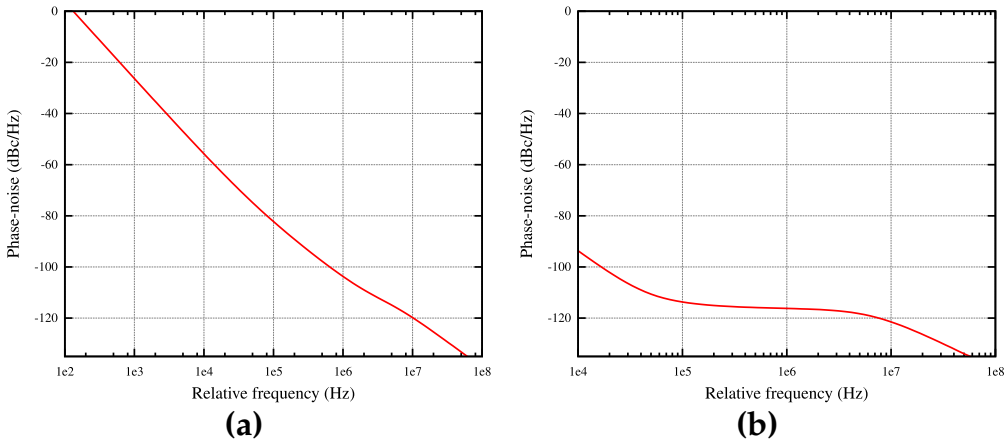


Figure 5.13: ILO phase-noise for injection at the fundamental frequency: (a) Reference with typical RC phase-noise. (b) Reference with typical LC phase-noise.

The obtained results allow to draw some conclusions:

- The phase-noise of the injection-locked oscillator is dominated by the reference, but, it has a contribution from the phase-noise of the free-running oscillator at the limits of the sideband.
- For the same locking range the obtained results are similar.

These results support that, granted the amplitude, that guarantees a locking range comparable to the extension of the oscillator sideband there is not differences between the injection schemes.

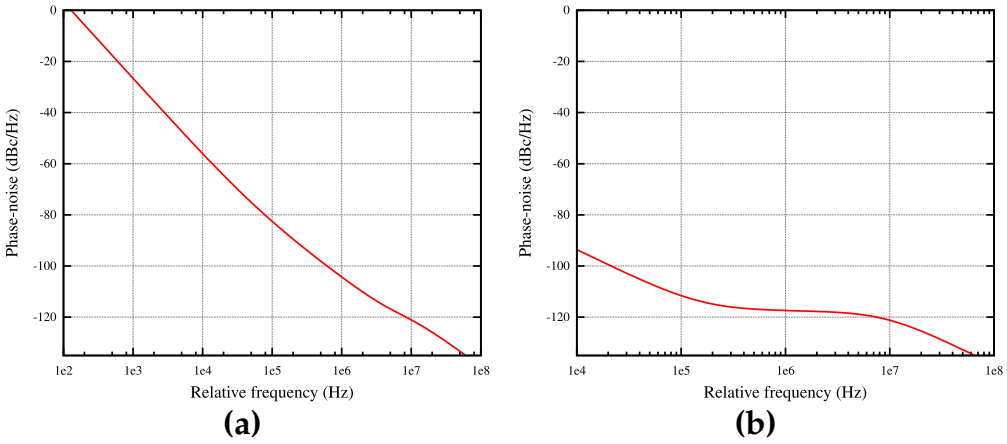


Figure 5.14: ILO phase-noise for injection at the second order harmonic: (a) Reference with typical RC phase-noise. (b) Reference with typical LC phase-noise.

5.2 Design of a circuit prototype

The next step is to perform a circuit prototype in order to obtain some additional insight, namely:

- Assessment of the possible injection points of the oscillator.
- Implementation of an injection interface.
- Observation of the linearity of the phase-noise reduction with the amplitude of the injected signal.
- Determination of the minimum level of injection that guarantees synchronization.

For this step a two-integrator oscillator is chosen since:

- This oscillator has comparable structure to the relaxation oscillator. The observations and conclusions can be extrapolated.
- It can operate in QL mode at high frequency, which means it has few spectral components. At this point this is intended to minimize undesired modulation effects that could hinder our observations in a scenario where our test setup does not allow perfectly shielding of the test circuit.
- It has inherent quadrature outputs, so increased circuit complexity is not required to obtain quadrature signals.
- It has another degree of freedom since the amplitude of oscillation can be tuned.

- It is inherently wideband in the GHz, which allows validation for a wide range of frequencies.

Since the circuit shows a quasi-linear behavior, the spectral content is mostly composed of a component at the frequency of oscillation and another one at twice its frequency. This means that there are only two options to perform synchronization, which will be detailed below.

5.2.1 Evaluation of the injection points

For the evaluation of the injection points it will be considered a simple, low power, low area and wideband injection block to avoid a penalty over the circuit FoM.

5.2.1.A Odd order injection

The Fig. 5.15 shows a well-known structure used to synchronize oscillators by injection locking. Since the two-integrator system has a differential output, it is advisable that the injected signal should also be differential. This is done by using a differential pair as the injection block. To ensure an equal operation point variation in both stages it is advantageous to place a differential pair at each stage (the synchronization signal, however, does not have to be fed on both). The injection block is the differential pair M_i driven by v_{sync}. The injection points are the two integrator oscillator outputs.

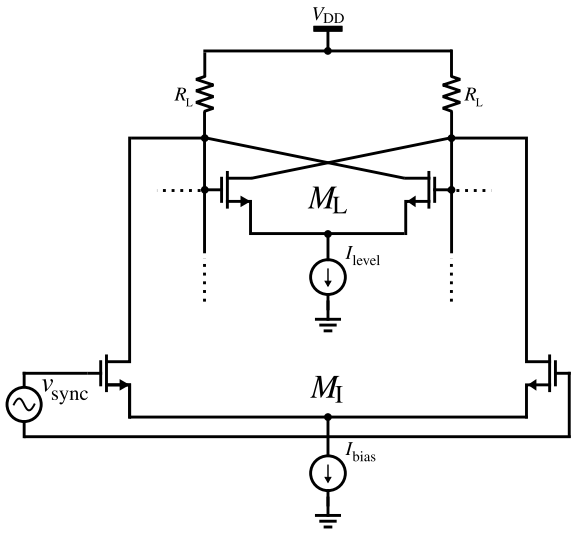


Figure 5.15: Odd order injection on one stage of the two-integrator.

After simulations, two issues are detected:

- First, this approach reduces the tuning range, due to parasitic capacitances (the injection points are sensitive nodes, since here are the dominant capacitances).

- The second issue is that the output of the oscillator has much higher amplitude than the injected signal. The result is an amplitude modulation of the synchronizing current (the differential pair will not operate as a gain block), as seen, for instance, in a single balanced mixer (the resulting spurious tones are not filtered, due to the large spectral component). The oscillator will affect the behavior of the injection block, and, instead of the desired signal, the oscillator will be fed with an amplitude modulated current signal (this could be solved by using separate biasing and decoupling capacitors in the injection block, which is not acceptable due to the extra complexity and area increase).

Previous simulations demonstrated that to achieve the largest locking range, would be to perform injection at the fundamental frequency. However, any odd order synchronization is compromised on the account of these aspects, which means an alternative must be considered.

5.2.1.B Even order injection

It is clear that the injection interface plays an important role, and the mutual influence between the oscillator and injection block should be minimum. Therefore, another approach was considered, the use of the common source of the cross-coupled differential pair of the oscillator (see Fig. 5.16).

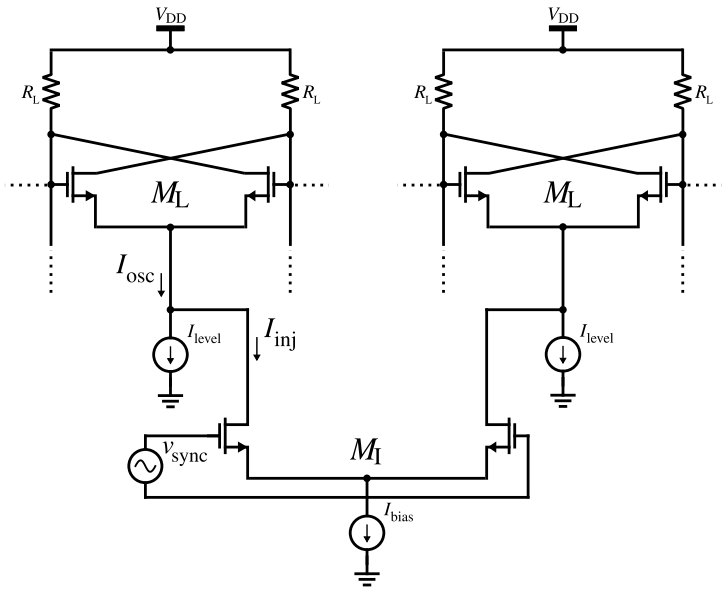


Figure 5.16: Second order harmonic injection.

At this node the voltage variations are small, so modulation effects are weak. In addition, the parasitics have low impact, since this is not a critical node. Also, the operation point is unchanged if the total current that flows through that branch remains constant ($I_{bias} + I_{Level}$ should be equal to the current I_{bias} of the original oscillator). Finally, this is the common source of a differential pair, and its voltage will, ideally, have only even order harmonics. Because the oscillator operates in QL mode it is expected to have only one weak second order harmonic. In view of the limitation of the injection interface implementation a second order harmonic synchronization is the only possible approach.

It was previously demonstrated that even though smaller amplitudes are able to synchronize the oscillator the necessity of a large locking range implies a high injection level, much higher than the required for an odd order synchronization. However, one advantage of this approach relates to the necessity of using only one differential pair, unlike the injection at the fundamental that should use two differential pairs to properly balance the loads of each stage. This means that the second order injection is not only beneficial in terms of area and energy consumption but it is also less prone to quadrature errors due to mismatch.

5.2.1.C Discussion

In Tab. 5.6 a comparison is shown between the two injection schemes.

Table 5.6: Comparison between even and odd order injection.

Injection Scheme	Advantages	Disadvantages
Odd order injection	Larger locking range	Higher energy consumption Larger area Injection interface as a mixer
Even order injection	Lower energy consumption Lower area Improves quadrature accuracy	Narrower locking range

Assuming that the narrower locking range of the even order injection can be improved by increasing the gain of the injection block, choosing to proceed with a second order harmonic injection is advantageous in view of its requirements of area and energy consumption.

Besides, the use of a frequency of injection higher than the free-running frequency of the oscillator should help to mitigate any eventual impact of frequency drift of the STO structure.

5.2.2 Design guidelines

Since the injected signal has low power and a sufficiently large locking range is intended, the main goal is to maximize the $\frac{I_{inj}}{I_{osc}}$ ratio. All the elements of the circuit other than those in the injection block, when varied, affect simultaneously and similarly I_{inj} and I_{osc}, maintaining the ratio unchanged (due to the high bandwidth both signals are similarly affected). This means that the injected current can be increased in two ways:

1. The W/L ratio of the transistors of the injection differential pair should be as high as possible, while guaranteeing proper biasing of all the transistors in the circuit.

2. By embedding the injection block into the oscillator and using just one current source to produce $I_{bias} + I_{Level}$.

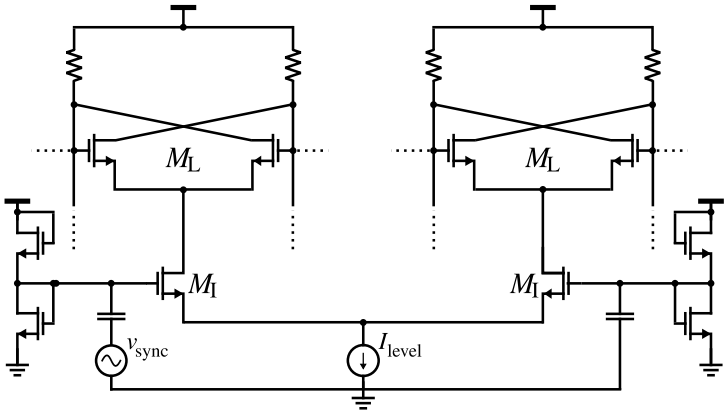


Figure 5.17: Injection block used in the test circuit.

The proposed circuit is shown in Fig. 5.17. The biasing voltage of the injection block is generated internally using transistors in diode configuration. Additionally, two decoupling capacitors ensure independent bias between the injection block and the synchronizing signal source.

The design procedure is aimed to obtain area and power reduction. The final circuit is shown in Fig. 5.18. In the design we have considered the following constraints:

- The dynamic regime should be carefully analyzed (with a transient analysis) in order to estimate the voltage range at the different nodes, and ensure correct biasing throughout the whole frequency band.

- Transistors should have at least 75 to 100 mV of $V_{DSAT} = V_{GS} - V_t$, to be in moderate inversion.

- $R_L I_{Level}$ (the maximum voltage swing at the output nodes) should not exceed $2V_{DSAT}$ of transistors M_l and M_f, in order to guarantee that they are in the linear region of the differential pair transfer characteristic (see Fig. 2.16).
- A locking range of 10 MHz should be achieved across the widest possible frequency range, with the lower possible power.

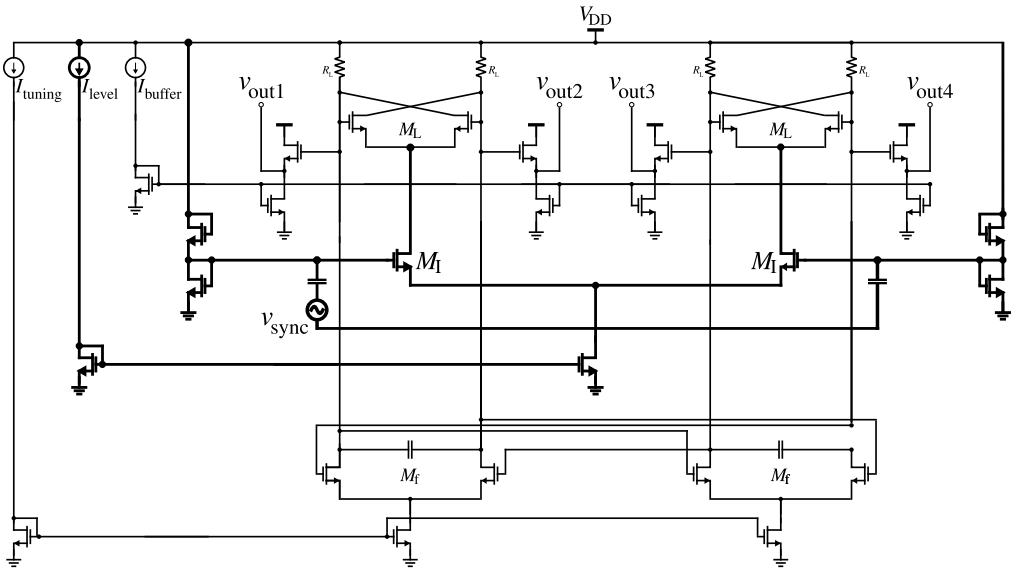


Figure 5.18: Final oscillator circuit (the synchronization circuit is highlighted).

The design methodology is as follows:

1. First, the two-integrator oscillator is designed, without the injection block, and it should achieve the widest possible tuning range. To reduce the parasitics and maximize the tuning range, the transistors dimensions are initially made small in the differential pairs (both M_l and M_f). Afterwards they may have to be increased to obtain a suitable biasing.
2. The injection block is added, with maximum width transistors (were the maximum size considered is the technology limit for a single RF transistor which is 115.2 μm) to maximize the transconductance.
3. The values of both I_{Level} and R_L are adjusted to ensure proper biasing.
4. Finally, the injected signal is applied, starting at -50 dBm, and the required voltage for a 10 MHz locking range is determined.

The circuit is designed for the 130 nm CMOS technology with a supply voltage of 1.2 V. The dimensions for the key transistors are given in Table 5.7.

Table 5.7: Transistor dimensions.

Parameter	M_l	M_t	M_i
W (μm)	12.6	27.86	115.2
L (ηm)	160	280	160

5.2.3 Simulation and measurements

Schematic simulations are done using output decoupling capacitors, bond wire models, and assuming an ideal synchronization signal source. To save area in the layout a multiple output current mirror is used. Additionally, ESD protection diodes are added, and an empty space is reserved (around 100 μm), at the far left, to allow the possibility of the circuit testing with the STO. The reason is to avoid mechanical stress when implanting the structure due to surface irregularities, as depicted in Fig. 5.19.

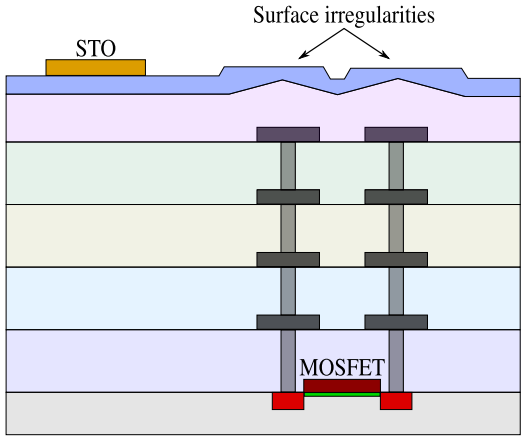


Figure 5.19: STO implant.

The current I_{Buffer} is set to 2 mA and I_{Level} to 4 mA. The injection block biasing transistors are sized to supply near 700 mV of common mode voltage at the input of the differential pair. The decoupling capacitors have 5 pF and the load resistors 170 Ω. The layout is shown in Fig. 5.20, and the post-layout simulation results, with extracted parasitics, are given in Table 5.8.

Table 5.8: Post-layout simulation results.

I_{tuning} (μA)	f_0 (MHz)	V_{osc} (mV)	V_{out} (mV)
123.5	600	232	89
766	3000	218	85

In Table 5.8 V_{osc} and V_{out} are respectively the differential voltages at the output of the oscillator and buffers. With this design the 10 MHz lock range is achieved with 1 mV for the lower boundary of the tuning range and 1.5 mV for the upper one.

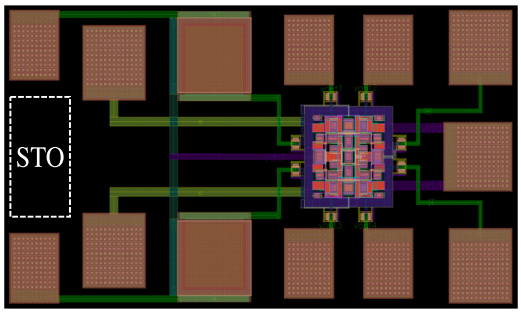
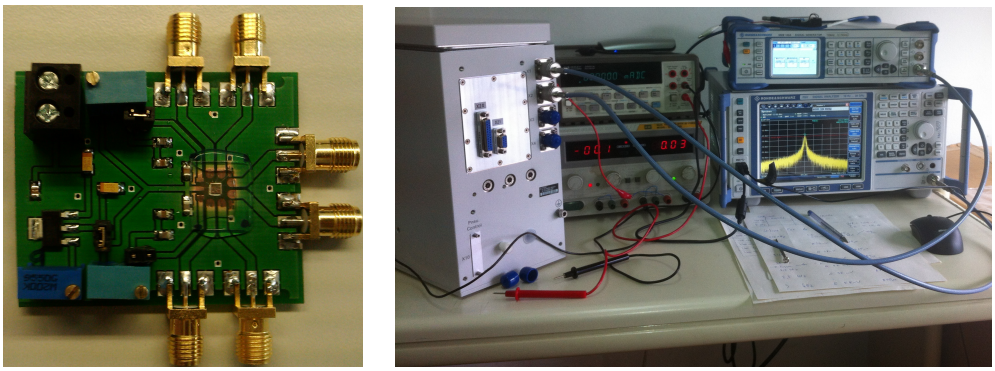


Figure 5.20: Layout of the test circuit.

The circuit is fabricated in standard 130 nm CMOS process and directly wire-bonded to a PCB. The paths from the chip outputs to the SMAs are carefully designed in order to ensure the 50 Ω impedance match (see Fig. 5.21(a)). The measurement setup is also shown in Fig. 5.21(b).



(a) **(b)**

Figure 5.21: (a) Test PCB. (b) Measurement setup.

Three samples of the test circuit are characterized. Due to process variations the circuits did not work under the same biasing conditions so, in order to allow a better comparison each circuit is tuned to produce the 600 MHz frequency with the current required during simulations (I_{tuning} = 123.5μm). The individual biasing values can be seen in Tab. 5.9.

Table 5.9: Circuit biasing.

Sample #	Vdd (V)	I_{bias} (mA)
1	1.3	5.74
2	1.3	6.12
3	1.3	6.32

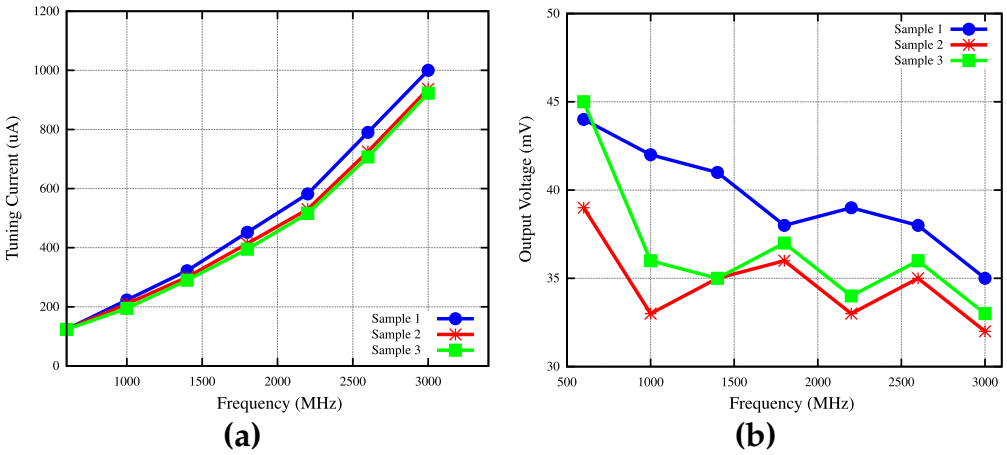


Figure 5.22: (a) Tuning Currents. (b) Output Voltages.

After setting the proper biasing conditions, the circuits are characterized. Two of the outputs are connected to the oscilloscope (one used as a trigger), one to the spectral analyzer and the remaining one to a 50 Ω load. The curves for the tuning current and single output voltage are depicted in Fig. 5.22(a) and Fig. 5.22(b). The phase-noise at the limits of the tuning range, for one of the samples, is also depicted in Figs. 5.23 and 5.24.

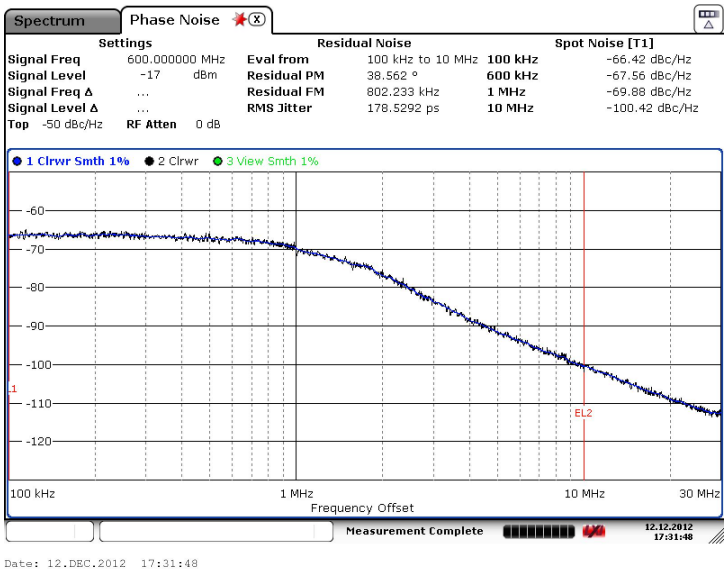


Figure 5.23: Phase-noise of the free-running at 600 MHz.

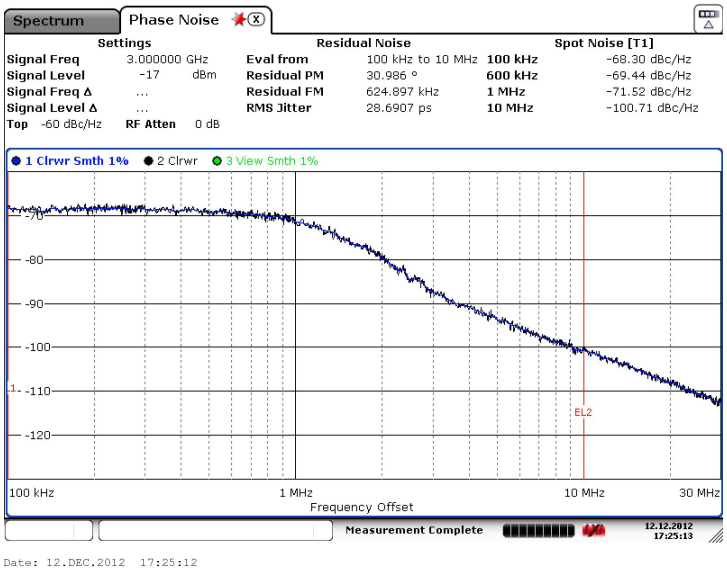


Figure 5.24: Phase-noise of the free-running at 3 GHz.

As one can see the three samples present similar current to frequency relation and output voltage. At this step the measurements are not performed with proper isolation, to facilitate probing, which means the circuit is exposed to spurious that can cause frequency instability and hopping (due to push-pulling effects [63]). Therefore, in order to get some measurements of phase-noise the resolution bandwidth of the spectral analyzer was increased. The consequence is loss of information at closer offsets, hence the results that can be observed in Figs. 5.23 and 5.24.

Afterwards the samples are characterized with synchronization signal that was provided by a signal generator. To reduce external interference and guarantee accurate measurements they are tested inside a portable anechoic chamber (see Fig. 5.21(b)). The power of the synchronization signal is swept between -50 and -10 dBm and its frequency between 1.2 and 6 GHz. The signal sources phase-noise are resumed in Tab. 5.10. The phase-noise improvement as function of the injection level for an offset of 1 MHz is shown in Fig. 5.25. The phase-noise measurements for a frequency of 600 MHz is shown in Fig. 5.26 and for a frequency of 3 GHz is shown in Fig. 5.27.

By observing Fig. 5.25 is possible to observe that the phase-noise is approximately linear with respect to the level of injected, as predicted by the models. By observation of Figs. 5.26 and 5.27 it is possible to observe noise filtering across the tuning range with synchronization signal power of just -50 dBm proving the merits of the followed designed.

Table 5.10: Signal generator phase-noise.

Signal Source	Frequency (GHz)	Phase Noise (dBc/Hz) Offset (MHz) 0.1	1	10
Signal Generator	1	-129	-140	-155
	6	-112	-124	-154
Free-running VCO	0.6	n.a	-71	-100
	3	n.a	-71	-100

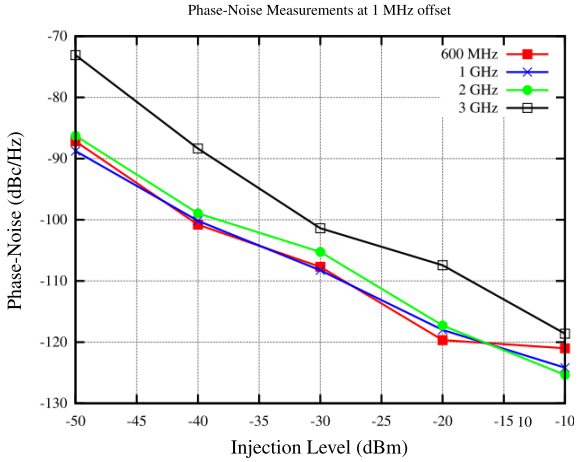


Figure 5.25: Phase-Noise vs Injection Level.

5.3 Discussion

One of the purposes of this chapter is to understand how the maximum frequency offset, up to which the phase-noise reduction is still accomplished, could be extended when using a weak synchronization signal as reference. It is suggested by simulations that a convenient approach would be to use fundamental synchronization but unfortunately in view of the limitations of the injection interface this is not possible and second order injection is chosen instead. To compensate for the weaker impact of these scheme the gain block of the injection interface had to be designed with higher gain.

An experimental validation of injection-locking in a two-integrator CMOS RC oscillator using reference signal at twice the frequency of oscillation was performed. The obtained results demonstrate that the followed approach allowed the correction of the phase-noise with a reference power as little as -50 dBm and for a wide range of frequencies, suggesting that this approach should allow to extend the applicability of the RC oscillator for multiple communication standards.

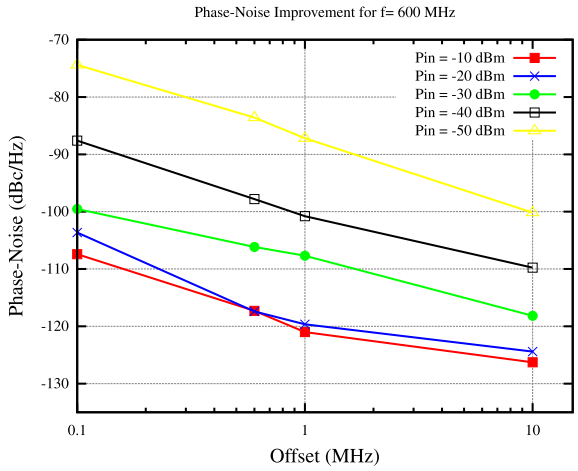


Figure 5.26: Phase-Noise Improvement for a Frequency of 600 MHz.

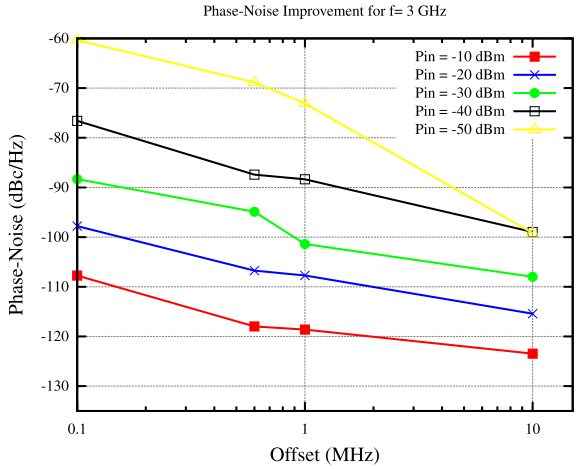


Figure 5.27: Phase-Noise Improvement for a Frequency of 3 GHz.

It is not critical that the power of the injection signal guarantees the 10 MHz offset. In fact the power of the injection signal should be sufficient to cover the noise up to the flicker corner frequency (see Fig. 2.8), which is located somewhere around 2~3 MHz as suggested by Figs. 5.23 and 5.24. The reason why the corner is found at such high frequency is mostly related to asymmetries in the circuit, which causes the flicker noise from the current sources to contribute to the close-in phase-noise (for instance the resistances have high tolerances, often around ±10 %).

The remaining offsets, whose dominant noise source is white noise, can be improved with particular design orientations. This means that the results are promising and support the feasibility of using an STO as signal reference. However, the implementation of the STO it is not possible at the moment, the output power of the structure has been already improved but the frequency drifts still occur.

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6

High Performance RC Oscillator

Preamble

In this chapter a modified relaxation oscillator circuit with high FoM at high frequency is presented. The performed modifications and design guidelines are discussed and validated.

Contents

The phase-noise improvement of the relaxation oscillator using injection is constrained by the level of injection, which means the phase-noise performance at farther offsets must be corrected with design options. However, this must not be obtained at the expense of an increase in the energy consumption. Therefore, some FoM must be used to drive the design and guarantee that the oscillator is competitive.

There are trade-offs in the design process of the relaxation oscillator, especially when aiming at high frequency operation. The circuit switching can be improved by speeding up the latch transitions which are accelerated by either increasing the current of the sources or by reducing the capacitances connected to the oscillator outputs, which are dominated by the parasitics of the latch transistors. The first approach increases the power consumption; the second implies using smaller transistors, which increases the mismatches. Another way to improve the speed is to reduce the capacitance C_{osc}, which has two consequences: the integrated noise increases; the circuit becomes more sensitive to the non-linear parasitic capacitances at the nodes with voltages $V_{int,i}$, which can result in higher performance variability. The theoretical minimum FoM (eq. 2.48) obtainable with a relaxation oscillator is [18, 87]:

$$\text{FoM}_{min} \approx -169.1 \text{ dBc/Hz} \tag{6.1}$$

However, practical implementations are far from the theoretical minimum. Most reported state-of-the-art relaxation oscillators have FoM above -162 dBc/Hz and the difference from the theoretical minimum usually increases with the frequency of operation [8, 19], Because there are different trade-offs for different latch responses, good noise and energy performances are difficult to be simultaneously obtained at high frequencies.

6.1 The conventional relaxation oscillator operation

In Fig. 6.1 is shown the classical circuit of the relaxation oscillator. When M_2 is off, the current of the two sources goes through M_1, which is on with a constant value of v_{GS1}; since $v_{osc2} = V_{DD}$, v_{int1} is constant. C_{osc} is charged, v_{int} increases, and $v_{int2} = v_{int1} - v_{int}$ decreases until v_{GS2} reaches the conduction threshold and M_2 is turned on: the latch reverses its state and $v_{osc1} = V_{DD}$. C_{osc} discharges until M_1 reaches the conduction threshold and the latch changes state. The node voltages are shown in Fig. 6.2 and the differential voltages, v_{osc} and v_{int}, are shown in Fig. 6.3.

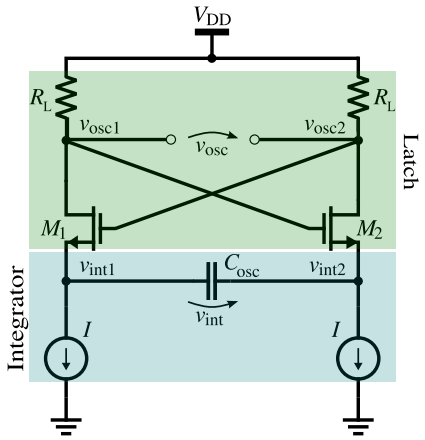

Figure 6.1: CMOS Relaxation oscillator circuit blocks.

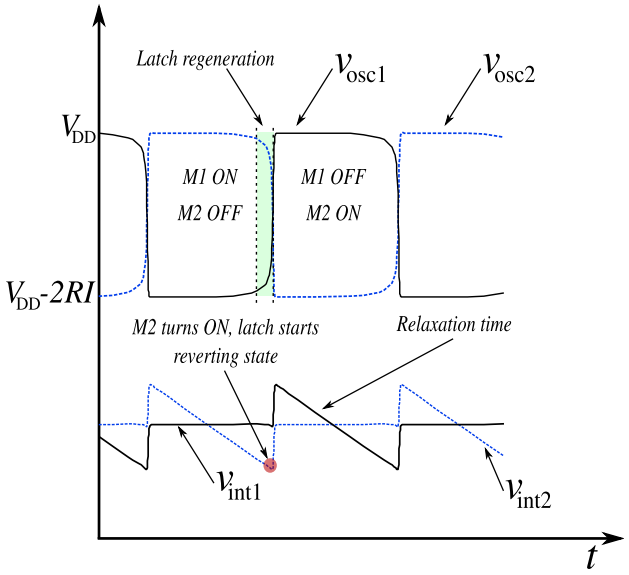

Figure 6.2: Relaxation oscillator node voltages.

Due to the current sources, the charge/discharge of C_{osc} takes place at a constant rate.

$$\Delta V = \frac{1}{C_{osc}} \frac{dQ}{dt} = \frac{I}{C_{osc}} \tag{6.2}$$

The voltage across the capacitor can be determined by doing the Fourier expansion of the triangular waveform shown in Fig. 6.3 [88]:

$$v_{int}(t) = \frac{I}{C_{osc}} \frac{8}{\pi^2} \sum_{-\infty}^{+\infty} \frac{\sin\left((2n-1)\omega_{osc}t\right)}{(2n-1)^2}, \tag{6.3}$$

where ω_{osc} is the oscillator frequency. The voltage across the capacitor has the fol-

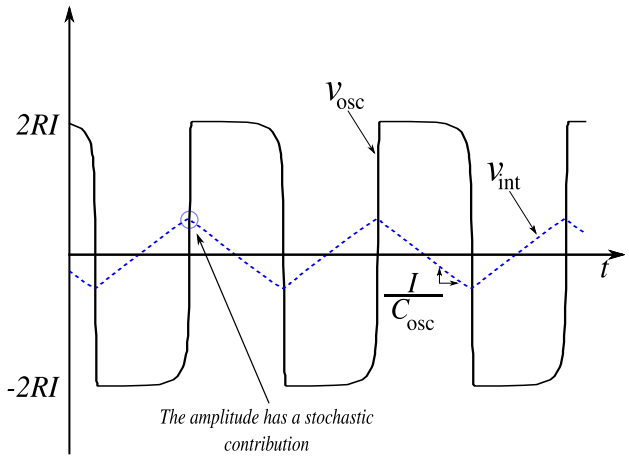

Figure 6.3: Relaxation oscillator differential voltages.

lowing description in the frequency domain [88],

$$V_{int}(\omega) = I.|H(\omega)| * \frac{8}{\pi^2} \sum_{-\infty}^{+\infty} \frac{\sin(\frac{n\pi}{2})}{n^2} \delta(\omega - n\omega_{osc}) \tag{6.4}$$

where $H(\omega)$ is the integrator transfer function. This corresponds to a superposition of an infinite number of spectral components centered at multiples of the switching frequency. The triangular waveform in Fig. 6.3 is only obtained when the regeneration time is much lower than the relaxation time. As the regeneration time increases, the voltage across the capacitor tends to become quasi-sinusoidal and the spectrum of the capacitor voltage will have fewer components.

The description of the capacitor voltage is not completed if noise is not accounted for. Noise affects the capacitor initial charge which causes the voltage across the capacitor to become phase-modulated, which means that the period of oscillation will vary around its nominal value. If noise is present, the spectral representation of the voltage across the capacitor will show replicas of that noise spectral density centered at multiples of the switching frequency as demonstrated in eq. 6.5 and depicted in Fig. 6.4. This process was further detailed in Section 2.1.4.B.

$$
\begin{aligned}
V_{int}(\omega) &= ((I + i_n).|H(\omega)|) * \frac{8}{\pi^2} \sum_{-\infty}^{+\infty} \frac{\sin(\frac{n\pi}{2})}{n^2} \delta(\omega - n\omega_{osc}) \\
&= \ldots + \frac{8}{9\pi^2} I.|H(\omega + 3\omega_{osc})| + \frac{8}{9\pi^2} i_n.|H(\omega + 3\omega_{osc})| \\
&\quad + \frac{8}{\pi^2} I.|H(\omega + \omega_{osc})| + \frac{8}{\pi^2} i_n.|H(\omega + \omega_{osc})| \\
&\quad + \frac{8}{\pi^2} I.|H(\omega - \omega_{osc})| + \frac{8}{\pi^2} i_n.|H(\omega - \omega_{osc})| \\
&\quad + \frac{8}{9\pi^2} I.|H(\omega - 3\omega_{osc})| + \frac{8}{9\pi^2} i_n.|H(\omega - 3\omega_{osc})| \\
&\quad + \ldots
\end{aligned}
\tag{6.5}
$$

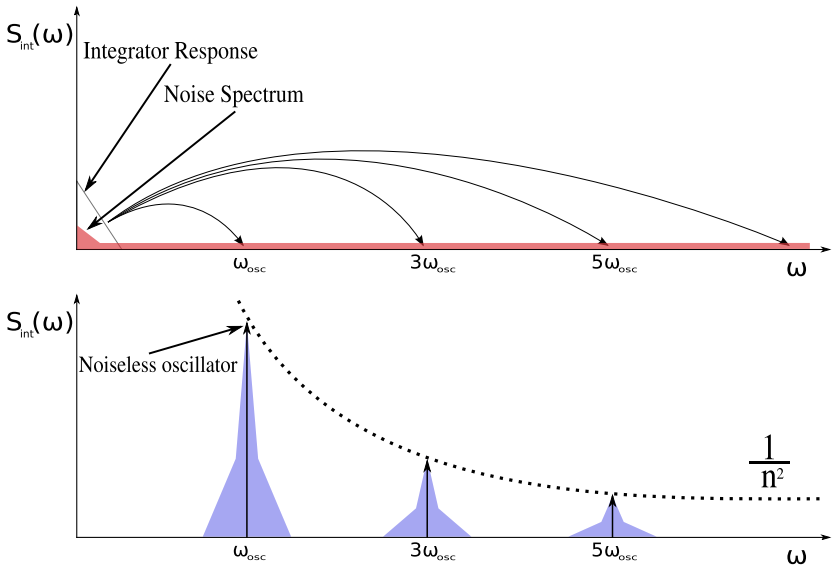

Figure 6.4: Sidebands due to noise [30].

As noise limits the applicability of the oscillator, it is important to understand the factors that affect and limit the phase-noise performance and try to mitigate their impact.

6.1.1 Latch operation

As previously explained, the circuit waveforms are dependent on the ratio between the regeneration and the relaxation times. If the oscillator output nodes have reduced parasitics and their charge time is much lower than the relaxation time, the oscillator is said to operate in relaxation mode, and the output is approximately a square wave. If the charge time has a magnitude similar to the relaxation time, the oscillator operates in a quasi-sinusoidal mode, and the output is roughly sinusoidal

[56].

The increase of the regeneration time implies that current is simultaneously drawn at both branches for longer time. This means that, for the same power consumption the longer regeneration time will imply a slower switching, thus a reduction on the oscillation frequency. However, as studied in [30], as the regeneration time is increased and the oscillator approaches a quasi-sinusoidal behavior, the phase-noise performance is improved. This allows to conclude on the oscillator performance, for a fixed power consumption, with the level of output parasitics (see Fig. 6.5):

- Low C_{par}: The circuit operates in relaxation mode. Higher frequency can be obtained.

- High C_{par}: The circuit operates in quasi-sinusoidal mode (the number of spectral components is reduced, since the voltage across the capacitor is no longer a triangular wave). The frequency is reduced but the phase-noise performance is improved.

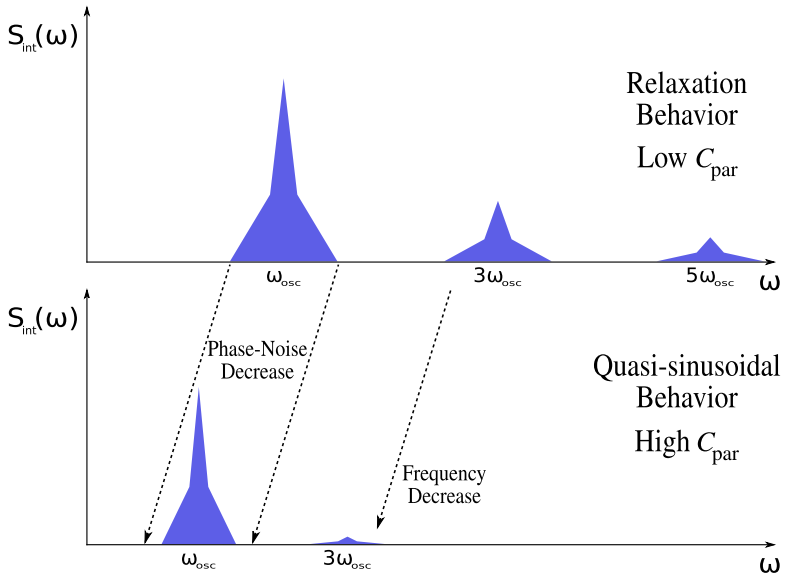

Figure 6.5: Spectral representation of the capacitor voltage variation with the increase of the output parasitics.

In order to obtain a higher FoM a good compromise between power and noise is required, thus, the tolerable level of output parasitics is the one that guarantees that the circuit operates somewhere between the two modes. With the frequency increase the impact of the parasitics becomes more important (the minimum regeneration time, which is limited by the technology, becomes comparable to the relaxation time),

is then necessary to prevent the quasi-sinusoidal operation but without having the oscillator operating in the relaxation mode. However, when the operation regime lays between relaxation and quasi-sinusoidal, it becomes harder to model the circuit behavior and a good compromise between power and noise performance may be difficult to achieve. This conclusion is supported by the differences found in the literature for the performance of the classical implementation of the oscillator (Fig. 2.25) for different frequencies of operation [19, 50, 53].

The maximum obtainable FoM is far from the theoretical optimum of −169.1 dBc/Hz, given in (6.1), which assumes a noiseless latch [18, 87]. The noise introduced by the latch is not negligible and increases with the switching frequency. Thus, the gap between practical and theoretical optimum performance is most likely to increase when increasing the frequency of operation.

It is inherent to the operation of this circuit that the transistors have periodic time-varying bias conditions. Because the latch transistors cycle between cut-off and strong inversion their noise contribution will be time-dependent (see Fig. 6.6) which is a consequence of the cyclostationarity of the process [30, 89]. The noise injected by the latch on the nodes of interest has periodically varying statistical properties, which means that its respective PSD magnitude will be dependent on the circuit hysteresis pattern and bias conditions.

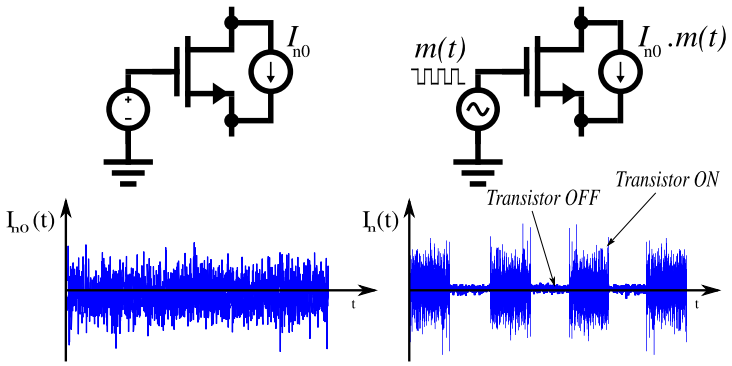

Figure 6.6: Noise contribution of a transistor with a cycling bias point.

The cyclostationary process can be modeled as the modulated output of a stationary noise source (noise source whose statistical properties are time-invariant) as follows [89]:

$$i_n(t) = i_{n0}(t).m(\omega_0 t) \tag{6.6}$$

where $i_n(t)$ is a cyclo-stationary noise current, $i_{n0}(t)$ is a stationary noise current, $m(\omega_0 t)$ is the noise modulating signal which describes the activity of the noise source (see Fig. 6.6) and ω_0 is the modulation frequency. The PSD of the cyclostationary

noise can be obtained as follows [88, 89]:

$$S_n(\omega) = \sum |S_{n0}(\omega) * M(\omega)|^2 \tag{6.7}$$

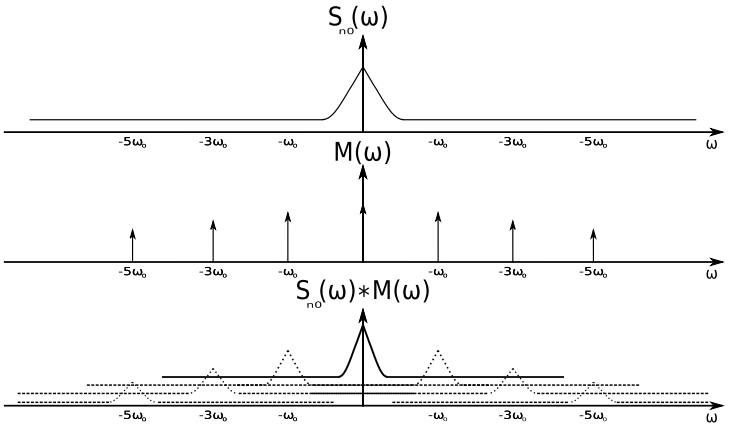

Figure 6.7: Frequency interpretation of a cyclostationary process [89].

Because the modulation process corresponds to a convolution in the frequency domain, the resulting PSD of the cyclostationary noise is obtained by adding all the contributions of the generated shifted replicas of the stationary noise spectrum as shown in Fig. 6.7. However, with the necessity of moving to higher frequencies the regeneration time must be reduced. This means the latch on-time is reduced to a very small percentage of the oscillation period and $M(jw)$ will be defined with much more frequency components. The consequence is an increase of the noise introduced by the latch in the circuit.

The fact that to obtain higher frequencies the latch is required to have high regeneration gain, necessarily implies a higher noise generation of the latch with the frequency increase which gives the indication that the latch noise is not neglectable and suggests that the difference between practical and the theoretical optimum performance of the relaxation oscillator is most likely to increase with the frequency of operation.

In the next section a high-performance oscillator topology that operates at high frequencies is disclosed. The correspondent design flow takes into account the inevitable impact of parasitics and compensates their effect. Also, design guidelines are offered to achieve a relaxation oscillator with regeneration and relaxation times suitable for GHz-range operation, enabling a good compromise among operating frequency, power consumption, and phase-noise. The approach is validated with measurements.

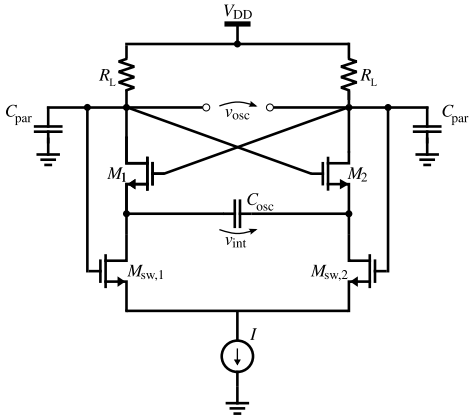

Figure 6.8: Relaxation oscillator with a single current source [50].

6.2 Improved quadrature relaxation oscillator

6.2.1 Proposed circuit

To save power, the new topology is derived from a variation of the classical implementation shown in Fig. 6.8, which uses only one current source and a differential pair that steers the current to the appropriate branch. This circuit, if properly designed, ensures only one conducting branch at a time, which allows a maximum reduction of the power consumption to a half (considering ideal current steering), when comparing with the classical circuit. The proper switching of the differential pair is difficult to obtain for two reasons: the non-linear parasitic capacitances connected to the output nodes and the stacked transistors. The increased number of stacked transistors leads to a higher on-resistance from the output nodes to ground, increasing the time required for the output nodes to be discharged. Since the total output capacitance is also increased, the latch speed is greatly affected by this circuit configuration. The number of stacked transistors also reduces the output swing as it reduces voltage headroom for proper biasing. For this reason, this variation of the classical circuit operates at a high frequency of operation in the quasi-sinusoidal mode with reduced output signal range, preventing proper switching of the differential pair (only one branch conducting at a given time).

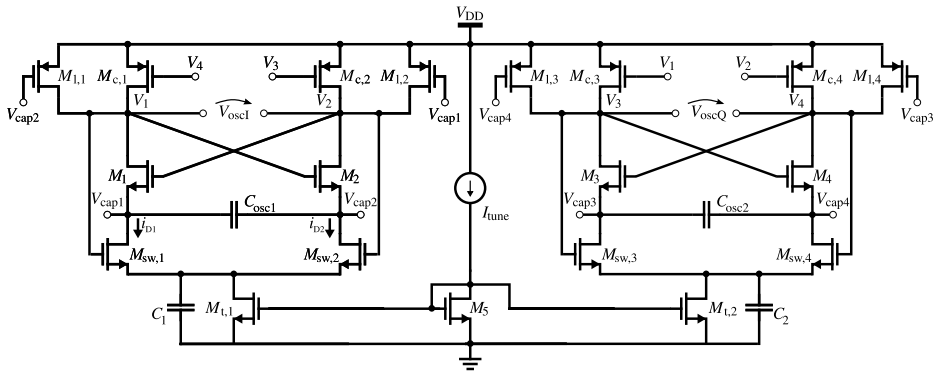

Figure 6.9: Proposed quadrature relaxation oscillator.

To cope with the degradation of the switching and increase of the operating frequency a few modifications were performed to the circuit shown in Fig. 6.8. The I/Q implementation of the proposed RC relaxation oscillator is shown in Fig. 6.9:

- The resistors are replaced by active loads (transistors $M_{c,i}$), providing higher output impedance for the same voltage drop, which means that a higher output amplitude can be obtained without a strong penalty on the voltage headroom. Even if the generated noise is roughly the same (considering that $g_{m,pmos} \approx \frac{1}{R}$), this modification allows an improvement of the output voltage range and of the switching speed.

- To further help the oscillator to operate closer to the relaxation mode, four pull-up transistors (transistors $M_{l,i}$) are added to obtain sharper transitions when the output nodes are being charged.

- Finally, to further help the maximization of the output swing the circuit current is imposed by a tail transistor operating as a tunable resistor instead of a current source, using less voltage headroom.

6.2.2 Design guidelines

The design guidelines in this section are aimed at an oscillator with a high frequency of operation and a satisfactory compromise between phase noise and power consumption. As previously referred it should be guarantee a good phase-noise performance at the furthest offsets, this means the design guidelines should aim to the reduction of the white noise contribution to the phase-noise, which is the predominant noise at high offsets (Fig. 2.8).

A good compromise between phase-noise and power is expected by speeding up the latch and by increasing the time required to charge/discharge the integrator capacitor. Due to the large signal behavior, most of the transistors cycle between cut-off and strong inversion, preventing the use of small-signal models. Thus, the following practical design considerations are based on the periodic steady-state regime.

- Integrator Capacitors $C_{osc1,2}$: These capacitances should be dominant, to minimize the impact of the non-linear parasitics and to mitigate performance variability. To ensure that the oscillator operates closer to relaxation mode, these capacitances should be higher than the latch output equivalent capacitance.

- Pull-up transistors ($M_{l,i}$): The pull-up transistors improve the switching speed by lowering the resistance when the output nodes are being charged. To avoid using an additional structure to generate their control signal, these transistors are connected to available nodes in the circuit, namely the capacitor terminals. The connections to the capacitor terminals are crossed to synchronize with the output nodes charging phases. These transistors should be small to reduce their contribution to the output nodes parasitic capacitances.

- Latch ($M_{c,i}$ and M_i): The sizing of the PMOS transistors should take into account their reduced mobility. Also, W and L should be increased to improve regeneration gain [90] and matching, as circuit unbalance converts the noise from tail transistors to phase-noise. In addition, the PMOS transistors provide active coupling leading to an improved frequency stability without reduction of the dynamic range of the oscillator [91].

- Current steering differential pair ($M_{sw,i}$): The differential pair should be able to switch completely to ensure that there is only one conducting branch during the capacitor charge (see Fig. 6.10). A fully switching pair can be obtained by ensuring that the amplitude of v_{osc} is higher than

$$\sqrt{2}\,(V_{GS,sw} - V_{t,sw}) \tag{6.8}$$

  where v_{osc} is the differential output of the oscillator, $V_{GS,sw}$ is the gate-source voltage and $V_{t,sw}$ is the threshold voltage of the transistors of the differential pair.

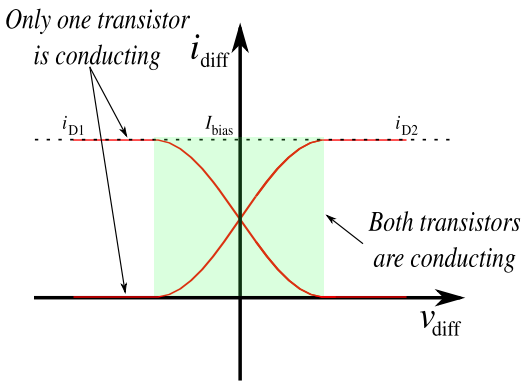

Figure 6.10: Differential pair transistors current variation with the differential gate voltage.

Since no current sources are used, the charge/discharge of the integrator capacitor is done at a rate that is dependent on the on-resistances of both the differential pair an the tail transistors. In order to improve the phase-noise it is then desirable to have a longer charge/discharge time, which can be done by guaranteeing that the differential pair transistors have high on-resistance. This is achieved by minimizing the $\frac{W}{L}$ ratio.

- Tail transistors ($M_{t,i}$): To increase the output swing, the tail transistors should be biased as tunable resistors instead of saturated transistors. The operating frequency can then be controlled by varying the tail transistors gate voltage. To ensure proper operation of these transistors a pair of filtering capacitors, C_1 and C_2 (see Fig. 6.11) are added to stabilize the drain voltage, leaving the tail transistors operating in deep triode. These capacitors also alleviate the impact of the tail transistors on the phase-noise in presence of circuit mismatch.

  The proposed tuning approach has the drawback of reducing the linear tuning range when compared to the current sources-based approach. This is not an issue for this design since the main target is to compensate for the performance degradation with the increase of the oscillation frequency (however, the range can be extended by employing feedback [92]).

- Voltage reference (M_5): To properly bias the tail transistors, a voltage reference is required, which is generated on-chip using a diode-connected transistor. It is important to ensure that the tail transistors operate in strong inversion, to improve the latch speed. To reduce the contribution of the reference branch to the power consumption, M_5 must be dimensioned with a small W/L ratio.

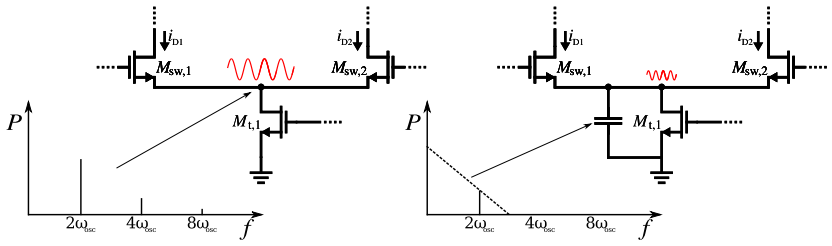

Figure 6.11: Tail transistor filtering capacitor.

6.2.3 Simulation

Ultimately this oscillator will be subject to injection in order to validate the concept of a hybrid oscillator. This means that this circuit should be designed in order to perform consistently over a sufficiently large tunning range (wide enough to cope with the frequency shift induced by the synchronization signal).

The use of linear models to describe the oscillator dynamics is possible only if the oscillator shows a quasi-sinusoidal behavior [93]. Since the proposed circuit is time-variant and very non-linear, it was employed a variation-aware Spice-simulation-in-a-loop analog optimization methodology, directed by the design guidelines given in Section II. The circuit was dimensioned for an operating frequency of 2.4 GHz, while minimizing the performance variability due to mismatches and PVT variations. The optimization framework employed in this work uses a kernel based on the NSGA-II [94] multi-objective genetic algorithm (GA). GAs are a class of algorithms based on the principles of population dynamics, and allow the use of black-box models (no gradients necessary) in the evaluation function. This custom implementation is based on [95]. A polynomial mutation operator with η_m=20 and a probability of chromosome mutation of 5% was employed, and a simulated binary crossover operator with η_c=20 [94].

The optimization process is fairly straightforward: a Python script is used to change parameters (W's and L's of transistors, capacitance values, etc) in a netlist, run Spectre and save the results obtained in a text file. Once a given number of simulations was done, the genetic algorithm decides which circuit parameters are to be tested next, based on the cost function (FoM, in this case) and a new set of simulations are run. Because PSS and PNOISE simulations were used, the optimization process converges in a relatively short time, typically a few hours. However, to guarantee that most of the design space is explored and no better solution is overlooked, the algorithm is left to run for more than one day.

To prevent local minima where there is high sensitivity of the performance to the circuit parameters, the optimization strategy consisted of the following steps (the objective is to achieve a high FoM and good immunity against process variations):

1. The software generates a set of initial parameters.
2. Using these parameters the circuit is simulated three times with a variation on the I_{tune} current of $\pm 100\,\mu$A.
3. Then the software calculates the following cost function.

$$\sigma = \frac{\mathrm{FoM_{std}}}{\mathrm{FoM_{avg}}} \tag{6.9}$$

   where $\mathrm{FoM_{std}}$ is the standard deviation of the FoM and $\mathrm{FoM_{avg}}$ is its average value (concerning the results using the three different current values).
4. The process is repeated while the software tries to simultaneously maximize FoM and minimize σ.

The circuit is implemented in a 0.13 μm CMOS technology with 1.2 V supply voltage. RF models are considered for the transistors, and ideal models are used for the capacitors. The test circuit was simulated with Cadence SpectreRF and BSIM3v3 models. The transistors dimensions obtained are shown in Table 6.1 and the performance results are shown in Fig. 6.12.

Table 6.1: Circuit parameters.

Component	Type	Function	W (μm)	L (nm)	Fingers	Comments
$M_{l,i}$	PMOS	Pull-Up	1.6	360	4	Small switches
$M_{c,i}$	PMOS	Latch	5.08	150	14	Aspect Ratio: 4.8
M_i	NMOS		0.92	120	13	
$M_{sw,i}$	NMOS	Switching Differential Pair	1.4	360	5	Slow transistors
$M_{t,i}$	NMOS	Tunable Resistor	6.63	190	10	Large area
M_5	NMOS	Voltage Reference	1.16	320	4	—
$C_{osc,i}$	Ideal Capacitor	Integrator	—	—	—	425 fF
C_i	Ideal Capacitor	Tail Transistor Decoupling	—	—	—	5 pF

In Table 6.1, it is possible to observe the considerable size of some of the transistors, which is justifiable by the design process that aimed at the minimization of the performance variability. By looking at Fig. 6.12, we can see that the circuit has large output swing and that the differential pair is properly switched (the threshold voltage for this technology is around 300 mV), as intended. Fig. 6.12 also shows a

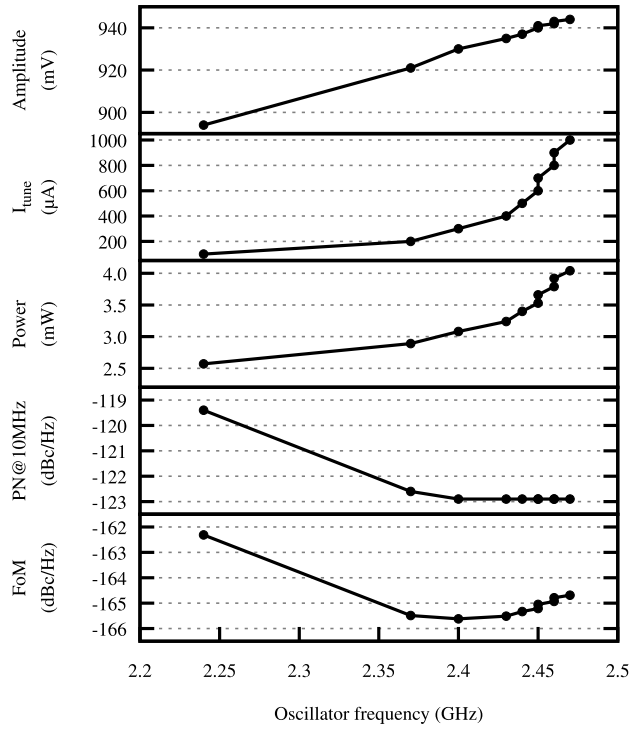

Figure 6.12: Simulated performance of the proposed oscillator.

consistently high FoM throughout the frequency range.

6.2.4 Measurements

Prior fabrication, source-follower buffers are added at the output and metal-insulator-metal (MiM) capacitors are used to implement C_{osc}. To reduce the supply noise, the layout includes several MOScap decoupling capacitors. Since the circuit area is pad limited, this does not influence the overall area. Because any asymmetries in circuit will degrade the phase-noise and increase the quadrature error, the layout of the oscillator should be made as symmetrical as possible. This of course will limit the impact of the injection signal when using a second order injection to further correct the phase-noise as done in the previous prototype. However, this is not a problem because due to distortion and the difficulty of achieving perfect symmetry even order harmonics will always be present but even if those components have small amplitude their impact can be corrected increasing the gain of the injection interface. The prototype oscillator, shown in Figs. 6.13(a) (layout) and 6.13(b) (die photo), has a core area of 278.9×171.9 μm^2 (467×397 μm^2, including the pads).

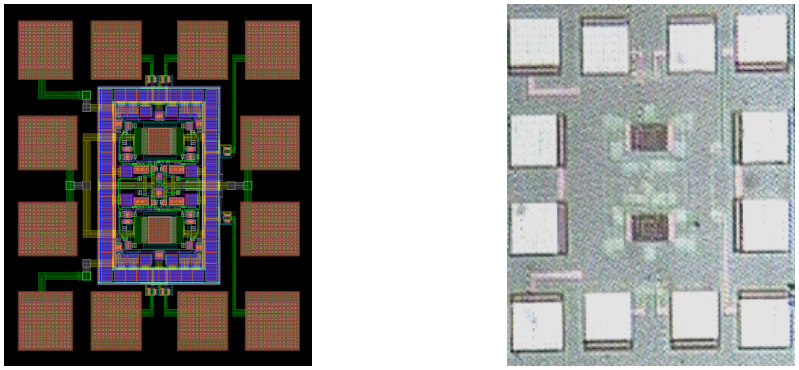

Figure 6.13: Circuit prototyping: (a) Circuit layout. (b) Die photo.

The quadrature error due to process variations and mismatches (500 Monte Carlo runs) is shown in Fig. 6.14, where it is possible to observe that the circuit is fairly robust with respect to process variations and mismatches, showing quadrature errors below 1°. It is important to note that the mean value of the quadrature error is 0.463 °, which means there is a deterministic error. This is the outcome transistor distortion and unbalanced parasitics in the two oscillator structures used in the quadrature oscillator. Perfect matching is difficult due to the cross-connections, that imply some asymmetry due to crossed wires (this implies however, the presence of even order components that are useful to synchronize the oscillator).

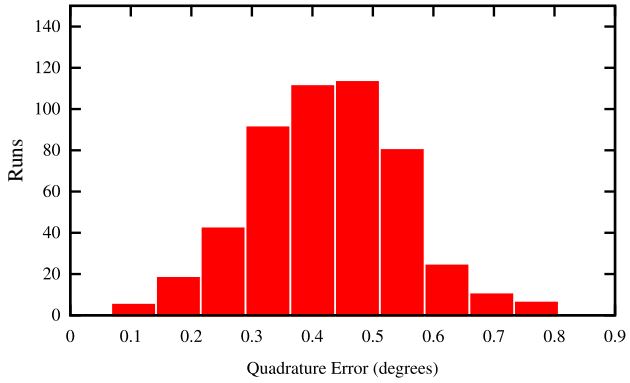

Figure 6.14: Quadrature error histogram (mean value = 0.463°).

It is also noteworthy that the routing parasitics introduced while laying out the oscillator led to a slight reduction in the frequency of operation. The circuit was readjusted to 2.4 GHz by simply tweaking the integrator capacitance.

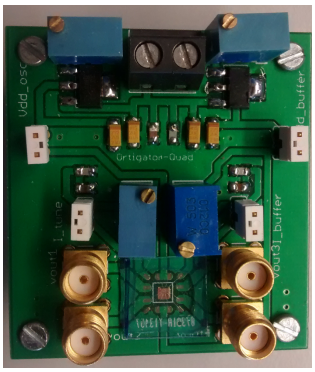

Figure 6.15: Test PCB.

Once fabricated the test circuit is directly wire-bonded to a PCB as shown in Fig. 6.15 (the paths from the chip outputs to the SMA terminals are carefully designed to ensure 50 Ω impedance matching). To minimize the supply noise, batteries are used to power the PCB. To separate the buffer current and measure only the oscillator power consumption, separate voltage regulators are used for the buffer and the oscillator. The current sources to bias the oscillator and the buffer are adjusted by potentiometers on the test PCB.

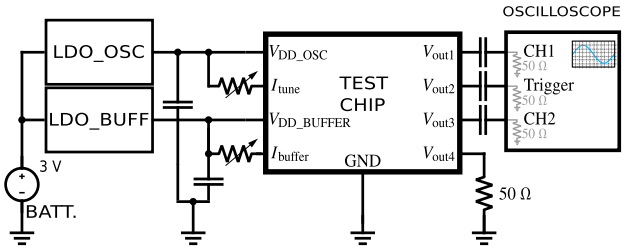

Figure 6.16: Measurement setup.

The measurement setup for the quadrature error is shown in Fig. 6.16. Two outputs of the oscillator are connected to the oscilloscope 50-Ω inputs; one is used as trigger and the other is connected to a 50-Ω load, to ensure balanced loads. To measure the frequency and the phase-noise, a spectral analyzer is used (one output is connected to the spectral analyzer and the remaining three to 50-Ω loads). Three samples of the prototype were tested, and a summary of the measurement results and post-layout simulations is given in Table 6.2. In Figs. 6.18 and 6.19, respectively, the spectrum and phase-noise of sample #1 is shown. A comparison of the proposed circuit with other state-of-the-art oscillators is given in Table 6.3.

Table 6.2: Post-layout simulation vs measurement results.

Description	f_{osc} (MHz)	P_{DC} (mW)	PN (dBc/Hz)		FoM (dBc/Hz)	
			1MHz	10MHz	1MHz	10MHz
Post-Layout Sim.	2.4	8.64	-102	-126.6	-160.2	-164.8
Sample #1 Meas.	2.396	9.225	-94.5	-124.2	-152.5	-162.1
Sample #2 Meas.	2.405	9.05	-95.3	-123.7	-153.4	-161.7
Sample #3 Meas.	2.398	9.3	-94.7	-124	-152.6	-161.9

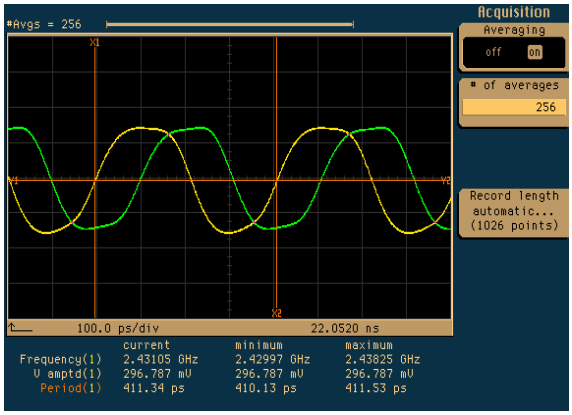

Figure 6.17: Output signal displayed on the oscilloscope.

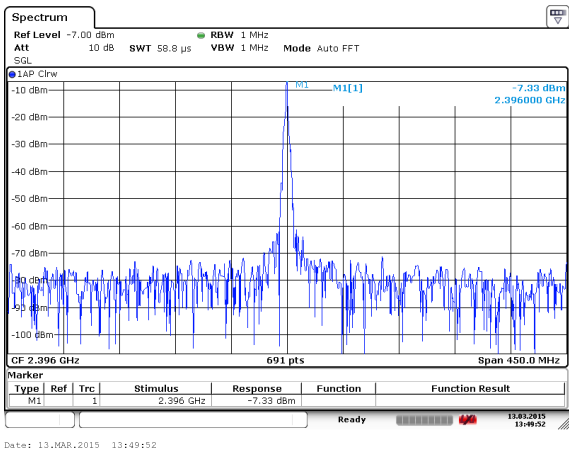

Figure 6.18: Spectrum of test circuit sample 1.

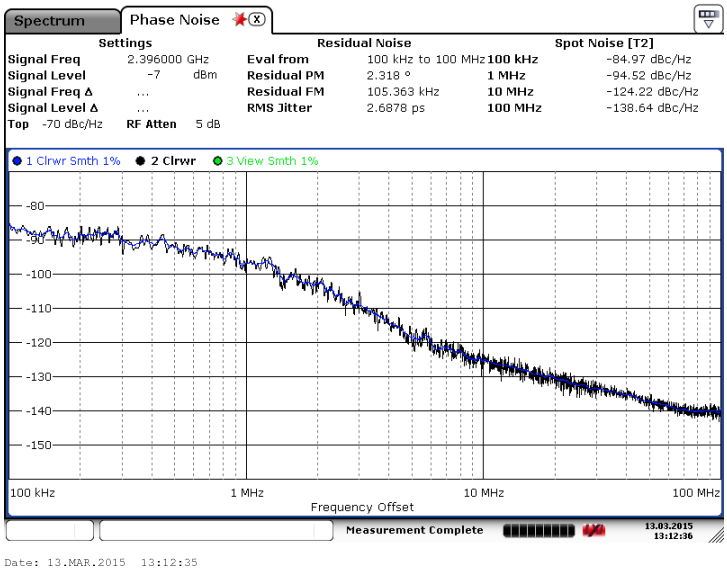

Figure 6.19: Phase-noise of test circuit sample 1.

Table 6.3: Performance comparison.

Ref.	Type	Tech. (nm)	Year	f_{osc} (MHz)	P_{DC} (mW)	PN (dBc/Hz)	FoM (dBc/Hz)
[19]	Relax.	65	2008	12	0.09	-109@0.1MHz	-162
[50]	Relax.	130	2011	214	1	-132.6@10MHz	-159.1
[51]	Ring.	65	2013	645	10	-111@1MHz	-157
[48]	Ring	180	2004	913	18.95	-116.5@0.6MHz	-167
[53]	Relax.	350	2007	2400	48	-105@1MHz	-155
[54]	Ring	130	2009	2500	2.86	-95.4@1MHz	-159
[96]	Ring.	90	2012	25000	257	-96@1MHz	-160
This Work	**Relax**	**130**	**2016**	**2405**	**9.05**	**-123.68@10MHz**	**-161.7**

Fig. 6.17 shows that the circuit operates in a regime between the relaxation and quasi-sinusoidal, which is expected in view of the design guidelines. It is also possible to observe from Fig. 6.19 a low phase-noise at the farthest offsets while maintaining a good FoM, which is one of the objectives. In fact the experimental results given in Table 6.2, show that the proposed quadrature oscillator, operating at 2.4 GHz, achieves a FoM of −162 dBc/Hz which is the best value, reported so far, for a relaxation oscillator operating in the GHz range and it is comparable to that of state-of-the-art ring oscillators, as shown in Table 6.3.

6.3 Discussion and future work directions

The proposed modifications and design guidelines are aimed to reduce the impact of the white noise allowing to improve the phase-noise at the limits of the oscillator sidebands. This is achieved at high frequency operation without a big penalty over the energy consumption which allowed to obtain a good FoM.

Implementation of an ILO using this oscillator as a base circuit turns possible to access the performance of the best RC oscillators reported so far, which are the ring oscillators, but with the advantage of being possible to achieve even order harmonic synchronization which is not possible to do on the ring oscillator, at least with the typical delay cells [97, 98].

A prototype with an integrated STO is not possible at the moment, however, to have an idea of the expectable performance of an hybrid oscillator the improved RC oscillator was simulated under injection. An injection interface is added and second order harmonic synchronization was performed. However, because there is not enough voltage headroom for the implementation of a NMOS differential pair, the injection interface is slightly modified and the differential pair is implemented with PMOS transistors instead, as shown in Fig. 6.20.

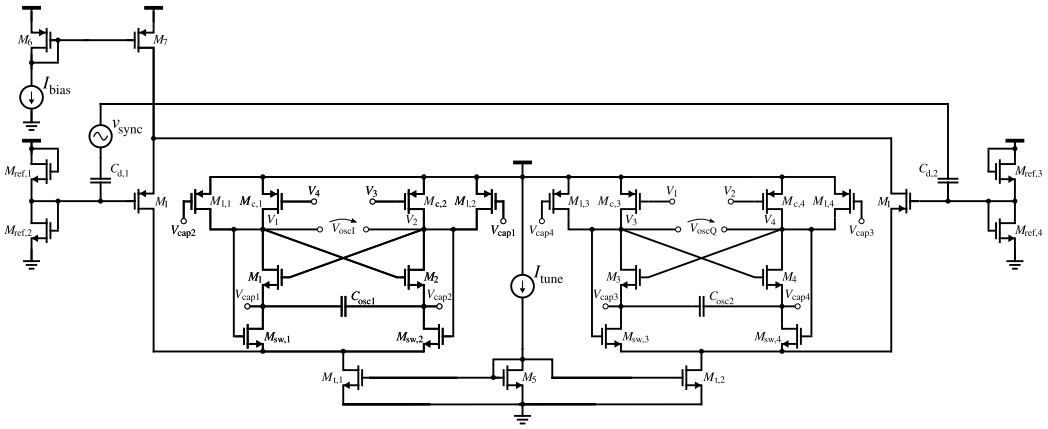

Figure 6.20: Improved relaxation oscillator with injection interface.

The design considerations are the following:

- The static consumption must be minimized. The reference branches $M_{ref,i}$ must be made small and the current mirror must be designed using a 1:m ratio.
- The current from the injection block will change the free-running frequency of the oscillator, this should be compensated by adjusting C_{osc}.
- The current from the injection block must not degrade severely the circuit FoM.
- The differential pair transistors should have a high $\frac{W}{L}$ ratio to maximize the current gain.
- The tail transistors drain have a voltage swing of less than 30 mV which means the injection block can be designed based on a DC simulation.

For simplification of the design and simulation tasks this step is performed using the simplified oscillator schematic whose performance is detailed in Fig. 6.12 and not the final version with the extracted parasitics. In Fig. 6.21 it is shown the synchronized oscillator phase-noise with relation to the phase-noise of respectively the reference and the one of the unperturbed state. In Fig. 6.22 it is shown the synchronized oscillator phase-noise variation with the injection amplitude.

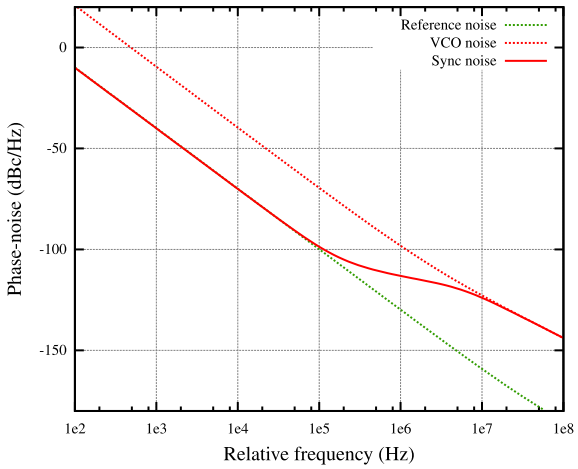

Figure 6.21: Phase-noise of the synchronized oscillator.

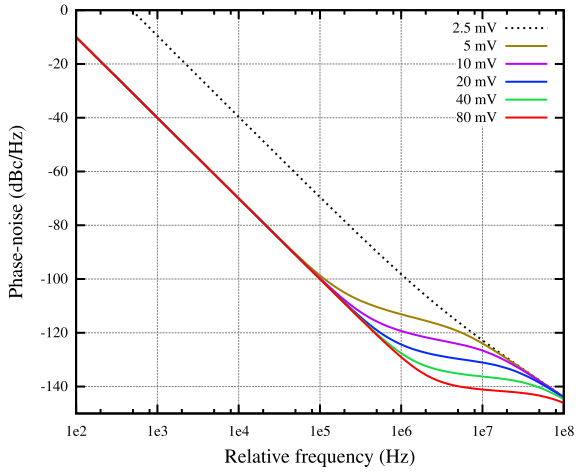

Figure 6.22: Phase-noise of the synchronized oscillator for several amplitudes of injection.

By looking at Fig. 6.21 it is possible to observe an expected result foreseen by the theoretical analysis on the phase-noise of synchronized oscillators (as seen in Fig. 3.9). By looking at Fig. 6.22 it is possible to observe a linear reduction on the phase-noise with the injection amplitude. It is also possible to observe that for an amplitude of 2.5 mV the oscillator is not synchronized. Due to the large size of the injection block there is not a proper isolation and the second harmonic of the oscillator appears at the input of the injection block.

Finally, the oscillator performance for a injection amplitude of 5 mV is shown in Tab. 6.4.

Table 6.4: Performance of the synchronized oscillator.

P_{DC} (mW)	PN (dBc/Hz)	FoM (dBc/Hz)
7.5	-99@0.1MHz	-178
	-113@1MHz	-172
	-124@10MHz	-163

Simulations show that if the reference phase-noise is comparable to the typical values for an LC oscillator, the performance of the RC oscillator is improved to the point of reducing the gap of topologies to just -10 dBc/Hz, for a 1 MHz offset with an injection amplitude as low as 5 mV.

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7

Conclusions and Future Work

Preamble

In this chapter the conclusions are presented as well as a brief discussion of future research directions.

Contents

7.1 Conclusions

The CMOS RC oscillators have low area, can be built with a low cost technology, and have a wide tuning range. However, the extent of their applicability is constrained by their phase-noise, which is poor and that is why, typically, they can be found implemented in applications where cost and area are the major constraints (for instance, IoT sensors or wireless sensor networks [2]). In all other applications where phase-noise is the major constraint LC oscillators tend to be the common adopted topology, since the difference in phase-noise performance is of the order of 20/30 dB.

The performance gap between both topologies becomes even more pronounced as the frequency of operation is increased. This is mostly due to the inability to find an optimal point of operation for the RC oscillator at high frequency of operation. Since the RC oscillators are capable of working in two modes, NL and QL [56] and their performance differs, from one mode to the other, it is not an easy task to minimize the phase-noise while guaranteeing low power consumption, specially as the frequency of operation increases, since parasitics cannot be neglected.

Nevertheless, due to their many useful characteristics a continuous effort has been devoted to the development of mechanisms suitable to improve the performance of the RC oscillators. This thesis presented and discussed an approach to improve the performance of the RC oscillator, for high frequency of operation, with a minor toll over the total cost, area and energy consumption of the oscillator. This was achieved by overlooking the typical approach of using a PLL structure and use injection-locking instead [5, 7, 10]. The main advantage of this approach is that these frequency synthesizers can be implemented with less circuit complexity but with comparable performance.

One of the challenges in designing the ILO is the reference generator. Throughout chapter 4 some insights were given about the available references, crystal oscillator and the STO [11–15]. It was discussed that even though the crystal oscillator is capable of higher Q factors, because his maximum frequency is limited to the MHz range and their tunability is reduced, the STO structure was considered to be better option. In addition the STO is CMOS compatible, which allow to implement a fully integrated wide-range and high performance ILO suitable for multi-standard applications.

The problem is that this structure generates a weak output and the phase-noise of the ILO is dependent on that amplitude, the implementation has to be done in a two-step approach [5, 7–9, 16]. Injection-locking was considered to correct the closer offsets, which are dominated by flicker noise, and design orientations were applied to minimize the phase-noise at the further offsets, which are dominated by white noise. A relaxation oscillator was used as the base circuit in view of its higher theoretical performance and multiple injection points, which allowed the test

of different injection schemes [18, 19].

In chapter 5 the process of improving the close-in phase-noise with injection was presented and validated experimentally. Even though it was suggested by simulations that the injection at the fundamental frequency would be preferable, performance wise, but a second order injection was used instead to avoid undesired modulation effects over the injection interface. To compensate for the weaker impact of this injection scheme the gain block of the injection interface had to be designed with higher gain. The obtained measurement results demonstrated that this approach allowed the correction of the phase-noise with a reference power of -50 dBm. The observation of the flicker corner frequency around 2/3 MHz was also a good indicator, suggesting that the amplitude specification for the reference could be relaxed, supporting the feasibility of using an STO as signal reference. Because the results were also validated for a wide range of frequencies the possibility of achieving a wide-range ILO is also considered valid.

In chapter 6 a modified relaxation oscillator was presented and validated experimentally. The proposed modifications and design guidelines were aimed to reduce white noise contribution, allowing to improve the phase-noise at the further offsets. The proposed oscillator uses a modified latch to improve the switching speed without increasing the power consumption. Moreover, the new topology avoids static current sources, maximizes the voltage swing and has an active coupling structure without static power consumption that reduces the circuit phase-noise. The proposed modifications, improved the switching, and the design guidelines, oriented to ensure a satisfactory compromise between noise and power consumption, allowed the oscillator to achieve a high FoM at high frequency. Experimental results showed that the oscillator is capable of exhibiting a phase-noise of -124 dBc/Hz at a 10 MHz offset, while achieving a closer-to-optimal FoM of -162 dBc/Hz [18, 19]. In every stage of this work there was an attempt to validate the results with high level independence to the integration of the reference. Even though it was not possible to validate a final demonstrator with an integrated STO, simulations demonstrated that if the reference phase-noise is comparable to the typical values for an LC oscillator, the performance of the RC oscillator is improved reducing the performance gap between topologies to 10 dB. This is a result that is merely suggestive, since the theoretical performance of the STO structures is beyond the one of LC oscillators.

In this thesis it was demonstrated the feasibility of implementation of a fully integrated ILO that should allow to reduce the performance gap of the RC oscillator to the LC oscillator. Even though the process of synchronization, the operation of the RC oscillator and the mechanism of noise-to-phase generation are undoubtedly of complex description, yet the qualitative and comprehensive approach that was seen throughout this thesis still allowed to achieve interesting results even though project

equations were not accessible.

7.2 Future work

- Fabricate a prototype of the improved RC oscillator with the injection interface and validate it with an external reference similar to what was done with the two-integrator.

- Test the prototypes with a nano-oscillator as reference. Prior to the delivery of this thesis a preliminary test of an interconnection of the two-integrator oscillator with a spin-torque nano-oscillator was performed (see Fig. 7.1). However, the performance of the nano-oscillator is still being improved and at the moment its not a viable option.

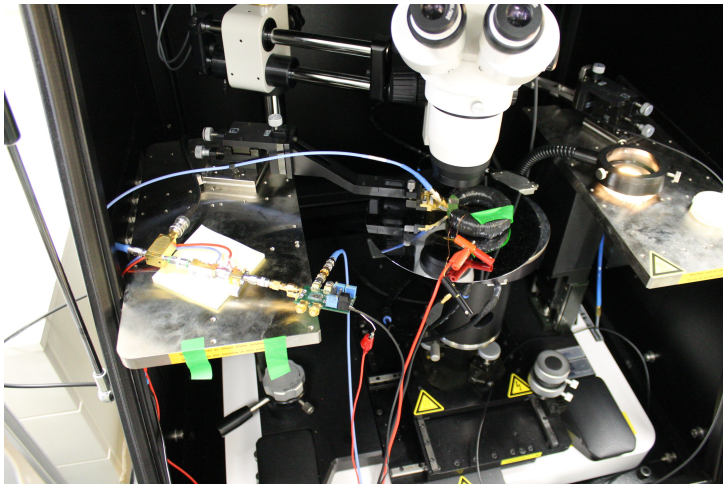

Figure 7.1: CMOS oscillator connected to the nano-oscillator.

  It is expected that in a near future the fabrication process of the nano-oscillator will be tuned allowing to validate the concept of an hybrid oscillator by implanting the nano-oscillator directly on-chip.

- Implement a programmable capacitor/resistor array to extend the tuning range of the improved RC oscillator. Design of a common biasing structure for both oscillators to validate a prototype of a wide tuning range ILO.

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A

Verilog-A blocks to perform simulation of injection-locked oscillators

A.1 Frequency sweeper

```
module Frequency_sweeper (p,n,ref);
parameter real amplitude = 1.0;
parameter real k = 50000.0;
parameter real phase = 0.0;
parameter real freq  = 1.0e9;
real Freq_eff;
inout p,n,ref;
electrical p,n,ref;

  analog begin
    @(initial_step) begin
      I(p) <+ 0.0;
      I(n) <+ 0.0;
      V(ref) <+ 0.0;
    end
    aux = $realtime;
    freq_sweep = freq * inj_order * (1 + k * aux);
    if (inj_scheme_One_Odd_Zero_Even==1) begin
      I(p,n) <+ amp*sin(`M_TWO_PI * freq_sweep * aux);
    end
    else begin
      I(p) <+ amp/2*sin(`M_TWO_PI * freq_sweep * aux);
      I(n) <+ I(p);
    end
    V(ref) <+ sin(`M_TWO_PI* (freq_sweep/inj_order) * $realtime);

  end
endmodule
```

A.2 Frequency detector

```
module Test_locking_state (vin1, vin2);

input vin1;
electrical vin1;
input vin2;
electrical vin2;

parameter real threshold  = 0;
parameter real maxerror  = 1.0e6;
parameter string filename = "a.csv";
parameter string filemode = "w";
integer       flag1;
integer       flag2;
real last_time1, current_time1, freq1, error;
real last_time2, current_time2, freq2;
string locked;
integer file;

  analog begin
    @(initial_step)
      begin
      flag1=0;
      flag2=0;
      last_time1 = 0.0;
      last_time2 = 0.0;
      freq1 = 0.0;
      freq2 = 0.0;
      locked="␣";
      error = 0.0;
      file  = $fopen(filename,filemode);
      $fwrite(file,"#format␣table␣##␣[WaveView␣Analyzer]␣saved␣\nXVAL,Freq.␣Inj,Freq.␣
          ↪ Error,Sync.␣Status\n");
    end
    @(cross( (V(vin1) - threshold) , +1)) begin
      $discontinuity(1);
      current_time1 = $abstime;
      freq1 = 1.0/(current_time1 - last_time1);
      flag1 = 1;
      last_time1 = current_time1;
      if(flag1+flag2==2) begin
        error = abs(freq1-freq2);
      if(error < maxerror)
        locked="Locked";
      else
        locked="Not␣Locked";
      if ((freq2 > 1e6) & (freq2 <= 1.05e9))
        $fwrite(file,"%0.18f,%0.9f,%0.9f,%s\n",$abstime,(freq2 - 1.0e9)/1.0e6,error,locked);
        $fclose(file);
        flag1=0;
        flag2=0;
      end
    end
    @(cross( (V(vin2) - threshold) , +1)) begin
      $discontinuity(1);
      current_time2 = $abstime;   //simulation time
      freq2 = 1.0 /(current_time2 - last_time2);
      flag2 = 1;
      last_time2 = current_time2;
    end
  end
endmodule
```

A.3 Reference signal with noise

```
`include "constants.vams"
`include "disciplines.vams"

module Ref_Gen_Noise(out1,out2);

output out1;
electrical noise, out1,out2;
parameter integer test_inj = 0 from [0:2);
parameter real amplitude = 1 from [0:inf);
parameter real f0 = 1G from [0:inf);
parameter real inj_order = 1 from [1:6);
parameter integer odd_or_even = 0 from [0:2);
parameter real Fos_f = 1;
parameter real Fos_w = 1M;
parameter real phasenoise_f = 68 from [-400:inf);
parameter real phasenoise_w = -100 from [-400:inf);
parameter real noisefloor = -162.5 from [-400:inf);
parameter real noise_inc=0;
real pow_f,pow_w, pow_nf, frequency, phase;


analog begin
@(initial_step)
  begin
  phase=0;
  pow_f = 2*pow(Fos_f,2)*pow(10,((phasenoise_f - abs(phasenoise_f*noise_inc/100))/10));
  pow_w = 2*pow(Fos_w,2)*pow(10,((phasenoise_w - abs(phasenoise_w*noise_inc/100))/10));
  pow_nf = amplitude*pow(10,(noisefloor-abs(noisefloor*noise_inc/100)/10));
end
if(test_inj) begin
  V(noise)<+ flicker_noise(pow_f,1,"fn") + white_noise(pow_w,"wn");
  frequency=f0*inj_order+V(noise);
  phase= 2*`M_PI*idtmod(frequency, 0, 1, -0.5);
  if (!odd_or_even) begin
    I(out1,out2)<+ amplitude/2*sin(phase);
    I(out1,out2)<+ white_noise(pow_nf, "nf");
  end
  else begin
    I(out1)<+ amplitude*sin(phase);
    I(out1)<+ white_noise(pow_nf, "nf");
    I(out2)<+ I(out1);
    end
  end
  else begin
    I(out1)<+0.0;
    I(out2)<+0.0;
  end
end
endmodule
```