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RFID logic circuit with oxide TFTs modeled by genetic algorithms

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"Well, it's nothing very special. Try to be nice to people, avoid eating fat, read a good book every now and then, get some walking in, and try and live together in peace and harmony with people of all creeds and nations." - Monty Pyton, The Meaning of Life

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Abstract

In recent years, the need for identification techniques, with faster reading speed and more flexibility regarding memory and programmability, led to the development of Radio Frequency Identification technologies. This technology has already proven to be essential in the future of Internet-of-Things, by allowing the possibility of tagging any type of product easily and at low cost per tag, while also allowing the interface of these tags, with common smartphones to increase the connectivity of RFID devices in daily life. Furthermore, the introduction of amorphous IGZO thin film transistors in RFID circuits, opens a new world of applications since this type of devices allows the use of transparent and/or flexible substrates, due to the low temperatures required during the fabrication process.

In this work, it was used the a-Si Level 61 TFT Model together with genetic algorithms, to model a-IGZO transistors produced, with a gate dielectric deposited by a solution method using spin coating. With these models, it was designed an RFID logic circuit, which employs diode connected structures, to read a 16-bit Read Only Memory and encode the signal using a Manchester encoding technique, with a data rate of 14 kbit/s.

These types of circuits using transparent and/or flexible substrates could allow, in the future, the creation of smart packaging for regular house goods and integrate it in a smart fridge configuration. Meaning that, it could be possible to a person either to be advised when to buy a certain item or when it reaches the expiration date.

Keywords: a-IGZO, RFID, Thin Film Transistor, Genetic Algorithm, IoT.

Resumo

Nos últimos anos, a necessidade por técnicas de identificação com velocidades de leitura superiores e maior flexibilidade relativamente à memória e programabilidade, levaram ao desenvolvimento de tecnologias de identificação de rádio frequência (RFID). Esta tecnologia já provou o seu valor no futuro da Internet das coisas (IoT), ao permitir a possibilidade de marcar qualquer tipo de produto facilmente e com baixo custo por etiqueta, enquanto possibilita a conexão deste tipo de etiquetas com *smartphones* para aumentar a ligação entre os dispositivos RFID e a vida quotidiana. Além disto, a introdução de transístores de filme fino (TFT) de óxidos amorfos em circuitos RFID, abre um novo mundo de aplicações, visto que este tipo de dispositivos permite o uso de substratos transparentes e/ou flexíveis, devido à possibilidade de usar baixas temperaturas durante o processo de fabrico para este tipo de transístores.

Neste trabalho, foi usado o Modelo a-Si Nível 61 com a ajuda de algoritmos genéticos para criar modelos de transístores de a-IGZO produzidos com um dielétrico de porta depositado por métodos de solução usando *spin-coating*. Com estes modelos, foi dimensionado um circuito digital de RFID, usando uma topologia em que o transístor de carga está em configuração de díodo, para ler uma memória ROM de 16-bit e posteriormente codificar o sinal através de uma codificação de *Manchester* com uma taxa de transferência de 14 kbit/s.

Este tipo de circuitos utilizando substratos transparentes e/ou flexíveis pode possibilitar no futuro a criação de embalagens inteligentes para bens domésticos e a posterior integração numa configuração de frigoríficos inteligentes. Isto significa que poderá ser possível uma pessoa ser avisada quando é necessário comprar um produto ou quando ultrapassa o prazo de validade.

Palavras-chave: a-IGZO, RFID, Transístores de Filme Fino, Algoritmos Genéticos, IoT.

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Acronyms

ANN	Artificial Neural Network.
AOS	Amorphous Oxide Semiconductor.
CMOS	complementary Metal Oxide Semiconductor.
CV	Capacitance-Voltage.
DFF	D-Type Flip Flop.
GA	Genetic Algorithm.
GPS	Global Positioning System.
HDL	Hardware Description Language.
IGZO	Indium Gallium Zinc Oxide.
IoE	Internet-of-Everything.
IoT	Internet-of-Things.
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor.
MUX	Multiplexer.
NFC	Near Field Communication.
NRZ	Non Return to Zero.
RF	Radio Frequency.
RFID	Radio Frequency Identification.
RO	Ring Oscillator.
ROM	Read Only Memory.
SPICE	Simulation Program with Integrated Circuit Emphasis.
TFT	Thin Film Transistor.
VLSI	Very Large Scale Integration.

Motivation and Objectives

In recent years, the technological development of industry and the growing population of the world, increased the logistical complexity of, for example, the distribution of goods around the world. This demanded new challenges, mainly in identification technologies. For many years, the barcode has been used due to its simplicity and extremely low cost. However, this technology has low storage capacity and requires a line of sight between the label and the reader besides, the barcode cannot be reprogrammed. The logical solution is the use of identification technologies with integrated circuits, like smart cards, which are nowadays the most common form of electronic data-carrying device [1]. However, in harsh factory environments, due to the impracticality of the contact reading systems and its speed, the smart card is not the best choice.

The optimal solution is a contactless system that would allow fast reading speed while maintaining low cost per tag. It would also be interesting that each tag could harvest the required energy from the reader [1]. All this is possible with Radio Frequency Identification (RFID) systems, which, as the name would suggest, relies on Radio Frequency (RF) waves to send the identification signal to the reader [2].

Apart from the use of RFID devices in the control of products through factories, these systems are also used in contactless smart cards as tickets for short distance public transports, employee schedule control in work stations, inventory check and in anti-theft systems of retail establishments, for example in clothing stores.

The possibility of introducing amorphous oxide semiconductor Thin Film Transistors (TFTs) in the manufacturing process of RFID electronic circuits could lead to a new world of possibilities for low cost RFID devices. This type of transistors can be fabricated with low temperature processes meaning they can be used in transparent/flexible substrates. This also means that the fabrication process can be easily reproduced in foundries not standardized with regular fabrication models. Hence, it is required to model transistors before starting the design and simulation of any circuit.

With this in mind, the objective of this work is to determine the parameters of amorphous Indium Gallium Zinc Oxide (IGZO) TFTs for the Level 61 a-Si TFT Model using Genetic Algorithms (GAs). Then, these models will be used to designed a digital circuit for an RFID tag. At CENIMAT/CEMOP in FCT/UNL, the fabrication of bottom gate n-type a-IGZO transistors is optimized, so the diode-connected load will be the topology used in this circuit.

Chapter 1

Introduction

1.1 RFID Principles

1.1.1 Types of RFID

Recently, the identification market has grown exponentially, and in the vanguard of this market, there are the RFID devices, which are capable of transmitting their identification code at high data rates and without line of sight between reader and tag, unlike previous identification techniques.

It is possible to divide RFID devices into two types: active and passive. The former one has a built-in power source, which means that this type of RFID has a limited lifetime. This type of tags can be found in devices used to locate stolen cars incorporated with Global Positioning System (GPS) and cellular technology [3]. Since there is a higher power budget, it is possible to include more power demanding circuits. On the other hand, passive RFID tags harvest the required energy from the carrier wave of the reader. This allows the tag to function indefinitely and reduce the overall cost. Nowadays, passive tags are more common in RF identification due to the advantages stated before, when compared to active tags and this will be the only type of tags mention throughout this work.

1.1.2 Operation and Parts of RFID devices

A common passive RFID device consists of a reader talk first protocol [1], meaning that the reading process starts with the RFID reader sending a signal to the tag or transponder. This signal is then rectified to produce the DC signal required for the circuit to work, also in some cases, the signal sent from the reader is used as the clock signal for the circuit. After the rectification process, the integrated circuit sends the data back to the reader which can be, depending on the application, a serial code, a batch number or a production date. In Figure 1.1 it is shown a simplified representation of every RFID system.

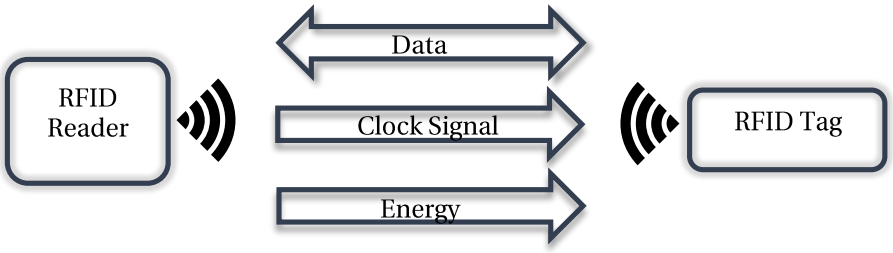
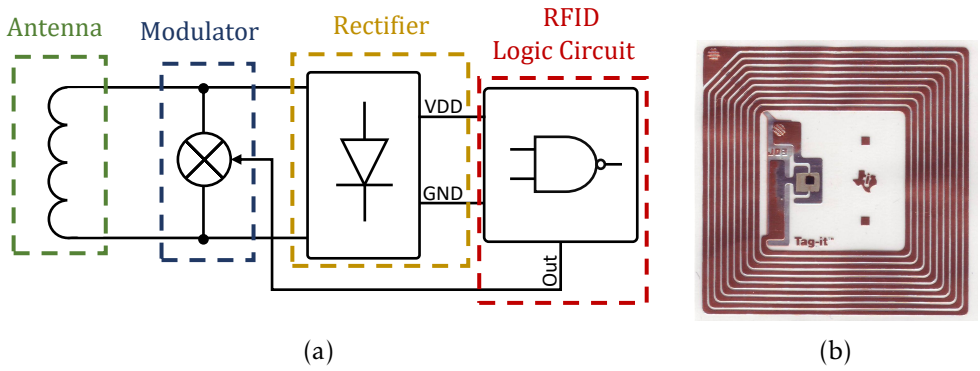


Figure 1.1: Representation of an RFID system.

The parts that make a common RFID tag are as follows:

- An antenna, which consists of a coil and is used to receive and send signals to and from the reader;
- A modulator, used to up-convert the digital signal to the carrier to be sent to the antenna;
- A rectifier, used to down-convert the carrier signal into a DC signal.
- A logic circuit, responsible to generate the data, either by reading a memory or by using decoders to produce the desired bit sequence.

In Figure 1.2 are represented the main blocks of an RFID tag and a common RFID tag, notice the coil as the antenna and the black square as the integrated circuit.



(a) (b)

Figure 1.2: (a) RFID parts; (b) RFID tag.

1.2 Thin Film Transistors in RFID tags

For years, RFID tags have been made using conventional silicon Very Large Scale Integration (VLSI) technology, however this also meant that due to the configuration of regular Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) it was impossible to use these circuits in flexible and/or transparent substrates, since these types of transistors require a substrate contact (bulk) and high temperature fabrication processes. However, with TFTs, this is no longer the case, since these types of devices use only the substrate as a support for the transistor structure [4]. At the same time, all the layers that make the TFTs are deposited through low temperature techniques (typical between room temperature and 350 °C, depending on the TFT technology), unlike in silicon fabrication methods where it is required, for example, oxidation and recrystallization steps which need very high temperatures (up to 1000 °C).

Despite the lower fabrication temperatures, and hence the lower cost of the overall production price, TFTs have lower performance when compared with regular silicon

MOSFETs. However, it was already shown that of all types of TFTs, Amorphous Oxide Semiconductors (AOSs) show relatively high mobility, (from 1 to 100 $cm^2 V^{-1} s^{-1}$ [4]) when compared to other types of TFTs, while maintaining low cost and low processing temperature. In this work the dimensions of the transistors used are very low to make up the low mobility when compared to silicon devices. The main problem with AOSs is the maturity of the technology which results in low yield and limited industrial application, unlike a-Si:H TFTs which have been studied for almost forty years and are used in switching elements in liquid crystal displays. [5]. However, regarding environmental concerns, oxide TFTs are eco-friendlier then a-Si:H TFTs, since the physical techniques employed use only Argon and Oxygen, unlike explosive gases as silane, phosphine or diborane [5].

The use of this different type of transistors allows for slightly different applications than the original RFID devices. Instead of a more industrialized use, RFID tags with Oxide TFTs allow for the development of tags inserted in applications closer to the consumer. For example, using RFID devices in flexible and/or transparent substrates for the creation of smart packaging labels, which can then be connected to the Internet-of-Things (IoT). This could allow the control, for example, of goods in a regular house fridge, giving information about the expiration date and the amount available of each product tagged. This technology can then be connect to the Internet-of-Everything (IoE) through smartphones with Near Field Communication (NFC) technology, allowing an even bigger integration of RFID devices in daily life.

1.3 State of the Art

1.3.1 TFT Modelling

Before design and simulation of the desired circuit it is required a transistor model for the thin film transistors employed.

In modelling there are essentially two types of transistor models:

- Empirical models, where the behavior can be expressed using complex systems like Artificial Neural Networks (ANNs) or mathematical expressions, in which, the parameters do not have physical meaning;
- Physical models, where the behavior is expressed using expressions which have parameters with physical meaning, like the threshold voltage;

1.3.1.1 Empirical Models

Regarding empirical models, it was shown in [6] how neural networks can be used to create models for amorphous IGZO TFTs and hence simulate with these models to design circuits. Essentially, ANNs are an interconnection of a set of artificial neurons that have processing ability, and can learn to perform nonlinear modelling, with the help of experimental data, like output and capacitance curves for different bias and dimensions.

For ANN models, it is defined an equivalent circuit for the transistor with the overlap capacitances and the transistor's voltage dependent current source, and each of these elements is modeled with the artificial neural networks [7], ensuring that the model can express not only the static, but also the dynamic behavior of the transistor. After the learning process, the model can be implemented in a Hardware Description Language (HDL) to be straight forwardly used in a Simulation Program with Integrated Circuit Emphasis (SPICE) software.

1.3.1.2 Physical Models

Unlike empirical models, this type of models uses physical parameters to express the physical properties of the transistor. The Level 61 a-Si TFT Model is mainly a physical model with empirical expressions for the leakage region and is the one adopted in this work. This model has a high number of parameters, which means that it can be used to create models for transistors with high accuracy. However, this also means that it is necessary to extract a high number of parameters. It has already been shown in [8–11] several ways of extracting physical parameters through experimental transfer and output curves. Nonetheless, these methods of extraction can be very time consuming and are very dependent on the interval chosen for the extraction. For example, to extract the threshold voltage, one can select a certain interval of values to do a linear fit. However, with a slightly different interval, the extracted value can differ enough to change the behavior of the physical model. To overcome this issue, in this work it is proposed and used a genetic algorithm, which is discussed in more detail in Chapter 2. Essentially, this algorithm is a complex fitting tool used to determine the physical model parameters using the experimental curves as a target data.

In [12] it was used a combination of a genetic algorithm and a neural network to create a model for a GaN high electron mobility transistor. For this model, the genetic algorithm has been used to extract the extrinsic elements of the equivalent circuit model, while the intrinsic part was modelled using the neural network. Other uses of genetic algorithms include optimization tools in circuit design as seen in [13, 14].

1.3.2 RFID Circuit

Most papers published in this area employ similar circuits, read a memory or generate a bit array and posteriorly encode that array. However, they differ in the topology or fabrication methods.

In [15], it is represented a full RFID chip, including the RF circuit and the logic circuit. The circuit proposed, uses amorphous IGZO TFTs with an "active" load logic, this means that it is possible to achieve very low power consumption, of about 20 µW at 5 V [15]. However this also means that the load transistors need to be depletion type transistors. In [15], the supply voltage is obtained through rectification of the carrier wave of the tag reader and the memory is 4-bit Read Only Memory (ROM) with a clock

of 50 Hz. Since depletion type transistors require more masks than a circuit with only regular enhancement type TFTs, it is more common to use the load transistor in a diode connection topology, meaning this transistor is always in the saturation active region.

In [16], it is presented a digital RFID block using the diode connected topology. Unlike the previous paper, this circuit is not integrated with the rest of the blocks of the RFID chip. However the supply voltage is meant to be obtained from the rectification of the reader signal. In [16], the memory is 16-bit ROM with a Manchester encoder that produces a 32-bit array which can then be sent to the RF circuit at a rate of 3.2 kbit/s.

In [17], are presented 4 full RFID chips with antenna, rectifier and logic circuit. The logic circuit employed, produces a 12-bit array and it was design in 4 different topologies. The first one consists in the use of a pseudo-complementary Metal Oxide Semiconductor (CMOS) topology as presented in [18], the second is the classical diode connected topology and the 2 other topologies consist in the use of transistors with 2 gates. The first topology has a regular gate and a 2nd gate on the level of the source-srain contacts, while the second topology has the 2nd gate on the level of the metalization lines above the transistors. In these last two topologies, the extra gate terminal is used to change the threshold voltage of the transistors to increase the robustness of the logic gates [17]. The 3-gate topologies and the pseudo-CMOS require an extra power supply and more transistors per gate. However they are more robust and have lower power consumption when compared to classic topologies.

Despite having high data rates, the previous RFID chips were not in compliance of the standard protocols for NFC, however in [19] it is presented a full RFID chip with a 128--bit ROM that can be read with a smartphone or any average NFC reader. The topology employed in this paper is based in a pseudo-CMOS topology [18]. Also in this circuit, the clock signal is directly extracted from the carrier of the reader, this means that the circuit used in these blocks must be able to work at frequencies in the range of a few MHz. This was achieved through special implementations with a minimum channel length of 1.5 µm and with a top gate Self-Aligned fabrication method, which resulted in transistors with low overlap capacitance, allowing higher operating frequencies [19].

In Appendix A, it is presented the main features of the State-of-the-art.

1.4 Outline

This work is divided in five chapters, the first one is about TFT modelling using the widely known Level 61 a-Si model and genetic algorithms to calculate the model parameters. In Chapter 3, it is presented the circuit and the electric simulations. Then, in Chapter 4, it is presented the proposed layout and test methodology. After that, the conclusions and future perspectives are drawn in Chapter 5.

Chapter 2

TFT Modelling

2.1 Level 61 a-Si TFT Model

To model the amorphous IGZO TFT devices it was used the Level 61 a-Si TFT standard Model. This model is the equivalent to the AIM-SPICE MOS15 model developed at Rensselaer Polytechnic Institute [20] and is widely implemented in most SPICE simulators, including Cadence 6. To express all working regions of the transistor this model has expressions for all 3 regions of operation, here are represented some features of this model for each region:

- Above Threshold Region:
  - Linear region: Uses the classical square law I_{DS} model of crystalline silicon, however for amorphous silicon transistors, it is necessary to include the field effect mobility as a function of gate voltage [10], as seen in (B.11), (B.12) and (B.17).
  - Saturation region: Like in linear region the saturation region has the field effect mobility as a function of gate voltage, (B.17). Also, to ensure a smooth and continuous transition between linear and saturation region, the saturation voltage is replaced by the effective voltage which is a function of the saturation voltage and a smoothness parameter [10], as seen in (B.22).
- Subthreshold Region: In this region, the Fermi level is in deep localized states and its position depends on the density of deep states. So, in this model the sheet density of free charges can be modeled as a function of gate voltage and the density of states [10], as seen in (B.16).
- Leakage Region: For this region, this model employs an empirical model to describe the leakage current as function of gate and drain voltages as seen in (B.7).

Finally, to improve convergence in circuit simulation, it is used a universal approach to unify the different model regions. The total sheet density of free charge is dominated by the above threshold expressions at gate voltages higher than the threshold voltages while at lower voltages the total sheet density of free charge is reduced to subthreshold expressions as seen in Figure 2.1.

After this, the model calculates the channel conductance hence the drain-source current.

It is important to note that, although this model is mainly dedicated to amorphous silicon, it is used for the AOSs TFTs used in this work. As stated before, this model is

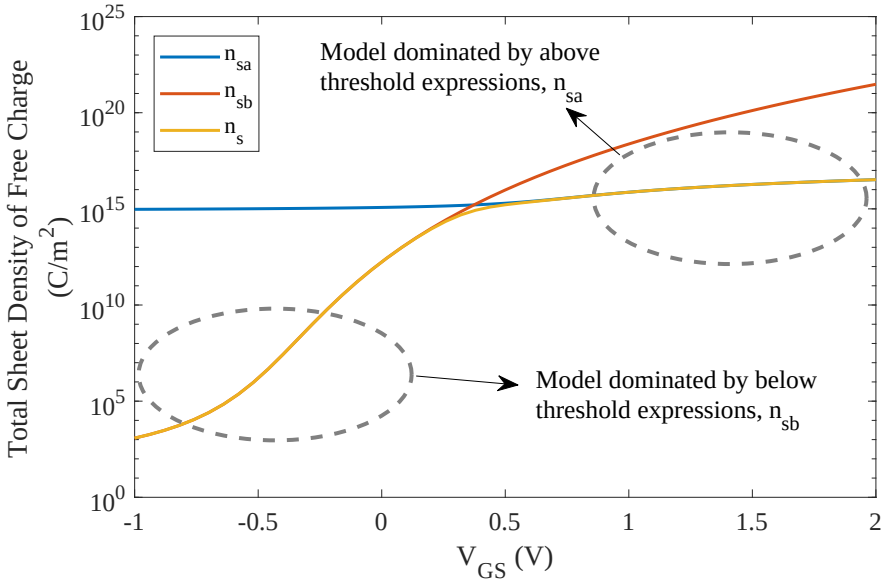


Figure 2.1: Variation of the total sheet density regarding the gate-source voltage. In blue is represented n_{sa}, which is the total sheet density of free charge in above-threshold region. In orange is represented n_{sb}, which is the total sheet density of free charge in subthreshold region. Finally in yellow is represented n_s, which is the unified sheet density for all regions.

widely available in most simulators, unlike recent proposed physical models for AOSs TFTs, [21, 22].

2.2 Parameter Extraction

The model employed is a physical model, which means that its parameters have physical meaning. To determinate each parameter through experimental curves it would be necessary to do several fittings due to the high number of parameters. However, even after the determination of all parameters, the model could not express the real operation of the TFT.

2.2.1 Genetic Algorithm

In order to overcome this issue, it was used a genetic algorithm, to optimize the parameters so there is a good fit, not only to the transfer characteristics, but also to the output ones.

A GA is a search algorithm that uses the mechanics of natural selection to optimize complex systems [14]. In GAs, each parameter of the model is a gene and the vector of parameters is called a chromosome. Like most optimization algorithms the GAs determines the correct elements of the chromosome that creates the best fit to a certain data (target values). Normally the GA is integrated with a simulator to evaluate each set of parameters. For circuit and model simulation the simulator can be a SPICE simulator.

However, when the fitness function is known, the model expressions can be used directly in the algorithm environment. In Figure 2.2 it is represented a diagram with the steps of the optimization process of the GA.

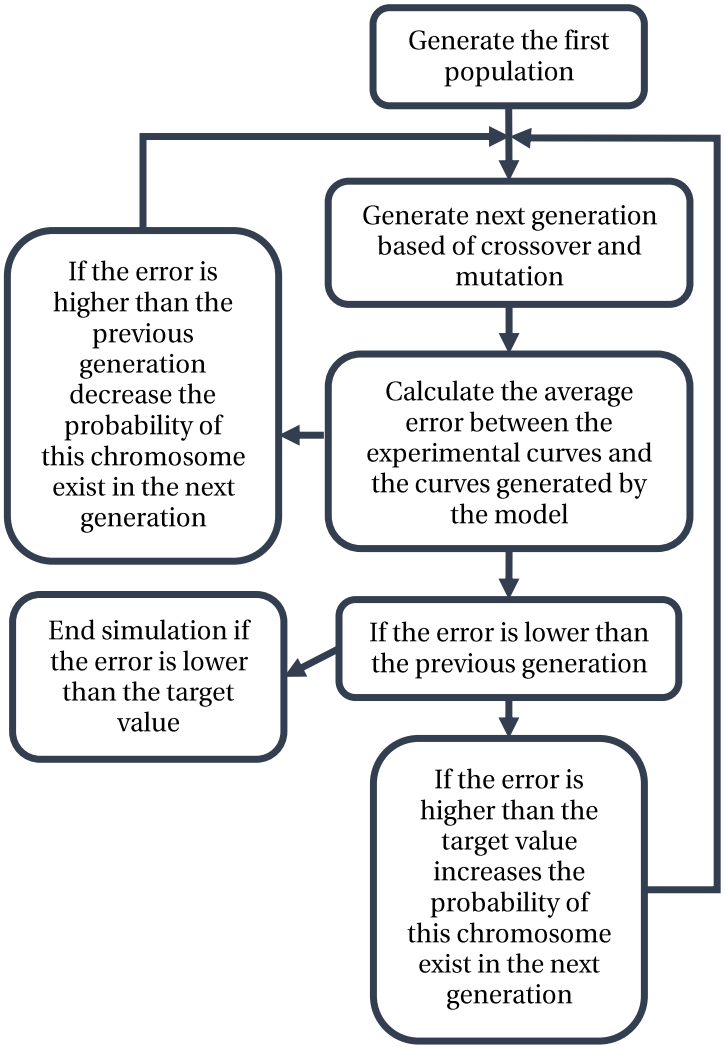


Figure 2.2: Diagram of a genetic algorithm adapted from [23].

As seen in Figure 2.2, after the creation of the first population the optimization process is started. With this first population, it is determined the average error between the experimental curves and the curves generated by the model with the first population. If, after a modification in the chromosome, the error increases when compared with the previous generation, the probability of this modification appear in future generations is decreased. However, when the error is reduced after a modification, the process is the opposite. This process is called selection and it is the main way for the creation of new generations. A new generation can also be generated by crossover, when parent chromosomes generate a child and by mutation, when random chromosomes are generated to

maintain genetic diversity. However, this probability should be set low, otherwise the optimization will turn into a random search.

The algorithm will keep running until one of two things happen: the error calculated in each generation is lower than the target value or the maximum number of generations is reached. With this process of survival of the fittest and a random component, the GA can avoid local minimums, which results in a robust optimization.

As stated before, the algorithm compares curves generated by the model and experimental curves, this curves can be considered the DC component of the model. For the AC component of the model, the parameters are calculated manually, since its values are easier to extract and do not require any kind of curve fit.

2.2.2 DC Component

In Figure 2.3, it is represented the cross-section of the transistors modeled.

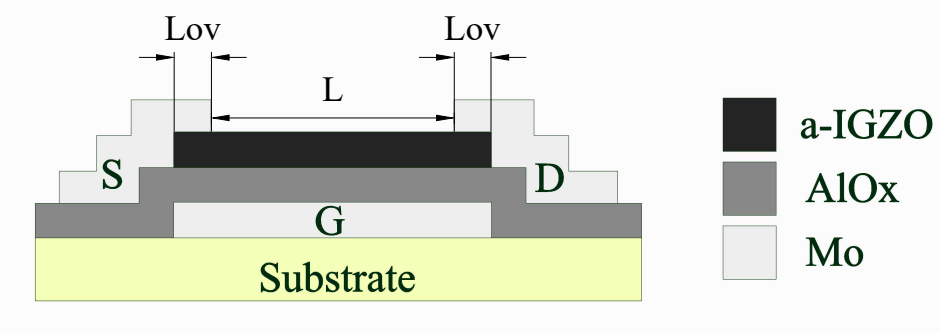


Figure 2.3: Cross-section of the TFTs modeled.

All layers were deposited using RF sputtering while the dielectric layer was deposited by solution using spin-coating as demostrated in [24]. The gate, source and drain electrodes are Molybdenum and have a thickness of about 17 nm, 70 nm and 70 nm respectively. The dielectric layer is aluminum oxide and has a thickness of about 20 nm. Finally, the semiconductor layer is composed of amorphous IGZO with a thickness of about 22 nm.

The experimental curves were obtained with Cascade M150 and Agilent 4155c Semiconductor parameter analyzer. The modulation was made using transfer and output curves and in Table 2.1 it is represented the sweep values for each curve.

Table 2.1: Sweep values of each curve measured.

	Transfer Curve	Output Curve
V_{GS}	-1:0.06:2	0:0.5:2
V_{DS}	2	0:0.05:2

In Appendix C, it is represented all parameters for the Level 61 a-Si model.

2.2.3 AC Component

The AC component of the Level 61 a-S1 TFT Model calculates de gate-source and gate--drain capacitances, respectively *Cgs* and *Cgd*, using several parameters. These parameters include the substrate and gate insulator relative dielectric constant and gate-source and gate-drain overlap capacitance per channel width [20], respectively, Cgs_{ov} and Cgd_{ov}.

The substrate used was Corning eagle xg which has a relative dielectric constant of about 5.3 at room temperature [25]. The remaining AC parameters can be determined from Capacitance-Voltage (CV) curves. In Figure 2.4 its represented a typical CV curve.

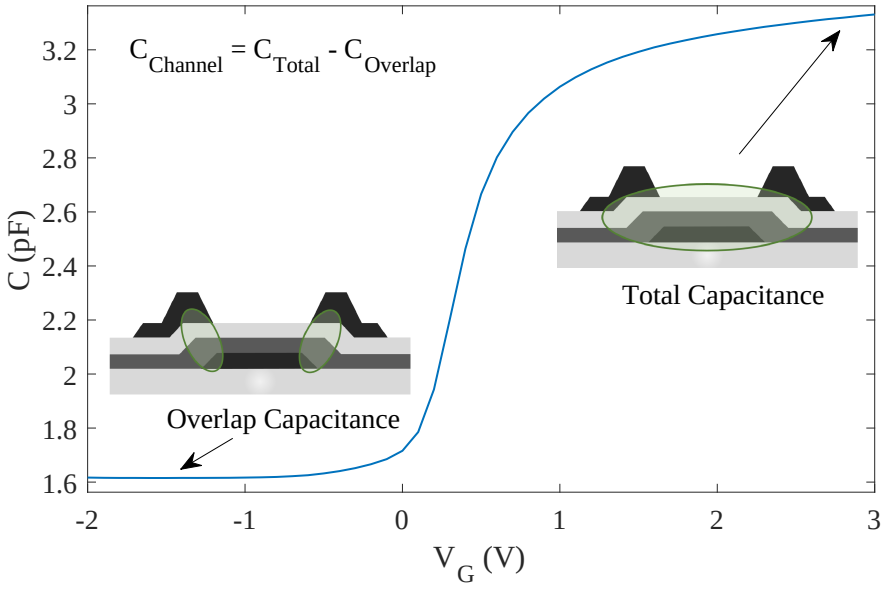


Figure 2.4: Capacitance of a transistor with $W/L = 100/5$, as a function of gate voltage.

To obtain these curves, the source and drain were grounded while at the gate it was applied an AC signal with a frequency of 100 kHz, with a DC bias which was then swept between -2 and 3 V. The measurements were made in Cascade EPS150 triax and Keysight b1500a. The experimental setup is calibrated to exclude the capacitances of the test probes and the cables, meaning that the value measured is only from the transistors.

As seen in Figure 2.4, in the subthreshold region only the overlap capacitance between the gate electrode and the source and drain electrode is measured. In the above-threshold region is measured the total capacitance of the device. The channel capacitance is given by the difference between the total capacitance and the overlap capacitance. Bearing this in mind, it is possible to calculate the value of the relative dielectric gate insulator, which is given by expression (2.1).

$$\varepsilon_r = \frac{C_{ch} \times d}{\varepsilon_0 \times W \times L} \tag{2.1}$$

where C_{ch} is the channel capacitance obtained from the CV curve; d is the thickness of the gate insulator; ε_0 is the vacuum permittivity and W and L are the transistor's width

and length, respectively.

Assuming the device is symmetrical, the gate-source and gate-drain overlap capacitance per channel width is simply the overlap capacitance divided by 2 and then divided by the width of the measured device.

2.3 Final Model

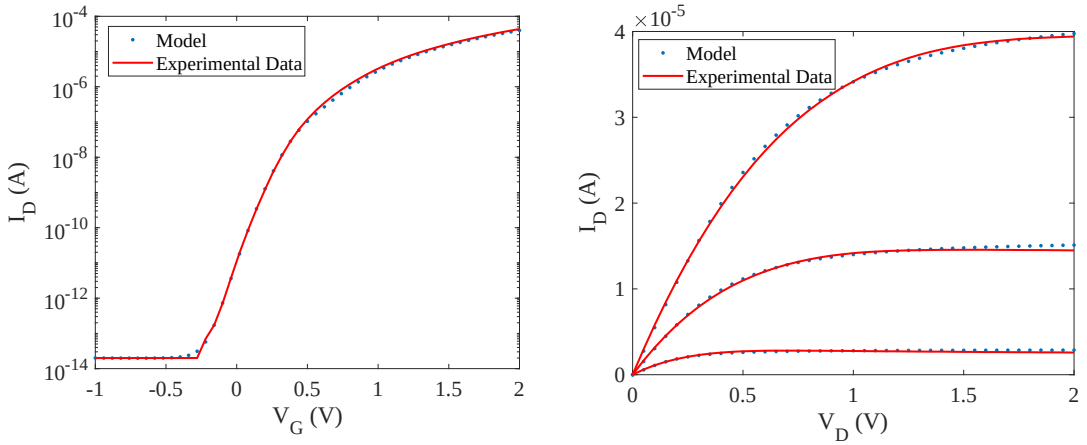
With all DC and AC parameters extracted, the process has been repeated for 3 transistors with different dimensions, to have a robust model. These dimensions and the overlap capacitance per channel width for each transistor are represented in Table 2.2.

Table 2.2: Dimensions and overlap capacitances of each transistor modeled.

W (µm)	L (µm)	Cgd_{ov}/Cgs_{ov} ($F\,m^{-1}$)
5	2	7.75×10^{-8}
50	5	1.27×10^{-8}
100	5	8.08×10^{-9}

During circuit simulation, it were used different models for different transistor dimensions. Also, to increase the range of dimensions available to simulation, it has been used in several cases, transistors in parallel or in series to increase the W or L respectively. This way the overall dimensions of the transistor don't change but the model can still express the operation of the transistor with a small error.

In Figure 2.5a and Figure 2.5b are represented transfer and output curves, respectively of the experimental measurements and the model for the transistor with $W/L = 50\,\mu m/5\,\mu m$.



(a) Transfer Curve.

(b) Output Curve.

Figure 2.5: Comparison between Experimental curves and the Model for the transistor with W/L of 50/5.

Chapter 3

Circuit Simulation

The transistors used in this work, a-IGZO TFTs, are n-type. Hence, it is employed a diode connected load topology, this means that all the basic blocks of the logic have a diode connected load to do the pull-up and several transistors, according to the respective gate, to do the pull-down. In Figure 3.1, it is represented the block diagram that represents schematically the RFID logic circuit. Afterwards, each individual block is presented in more detail. In the end, it is also presented the auxiliary circuitry designed exclusively for testing purposes. Since the transistors used have a very thin dielectric, it is possible to use low supply voltages, in this case 2 V.

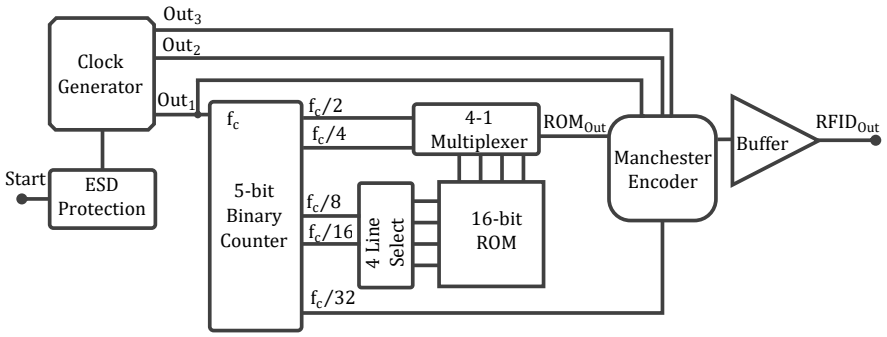


Figure 3.1: Block diagram of the RFID logic circuit.

3.1 Basic Logic Circuits

In Figure 3.2, it is represented the NOT and NAND gate circuits used and, in Table 3.1, it is presented the dimensions of each given device.

(a) NOT gate. (b) NAND gate.

Figure 3.2: Basic logic gates, at transistor-level, used in this work.

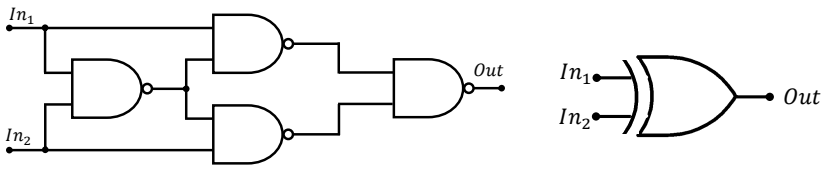
Table 3.1: Dimensions of the transistors presented in Figure 3.2.

	NOT		NAND		
Transistor	M_L	M_D	M_L	M_{D1}	M_{D2}
W (µm)	10	50	5	50	50
L (µm)	2	2	2	2	2

3.2 Exclusive Or

The XOR gate, also known as exclusive OR, is a case of an OR gate, meaning that only when the inputs are different will the output be 1, as seen in Table D.1.

The schematic and symbol are represented in Figure 3.3.



(a) Schematic. (b) Symbol.

Figure 3.3: Exclusive Or gate.

3.3 Flip-Flop

The Flip-Flop used in this work is a positive edge-triggered D-Type Flip Flop (DFF). This means that the output Q will be the input Data (D) when the clock signal is rising, as seen in Table D.2 and Figure 3.4.

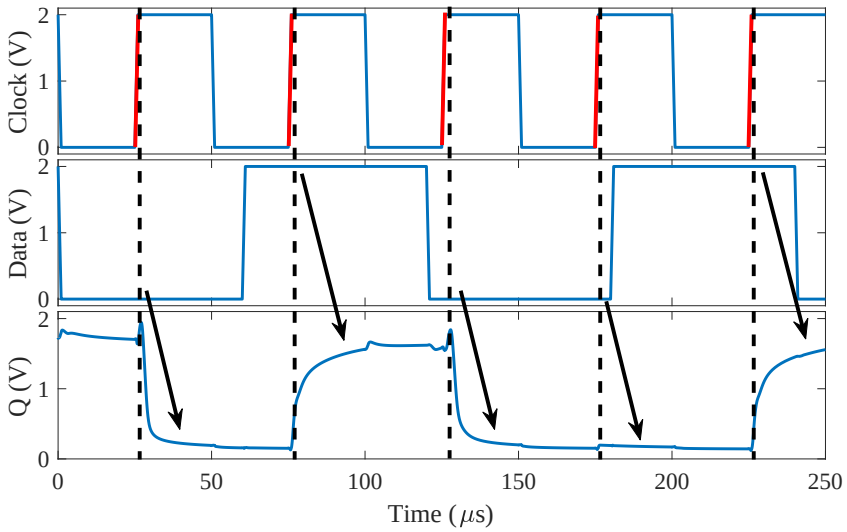
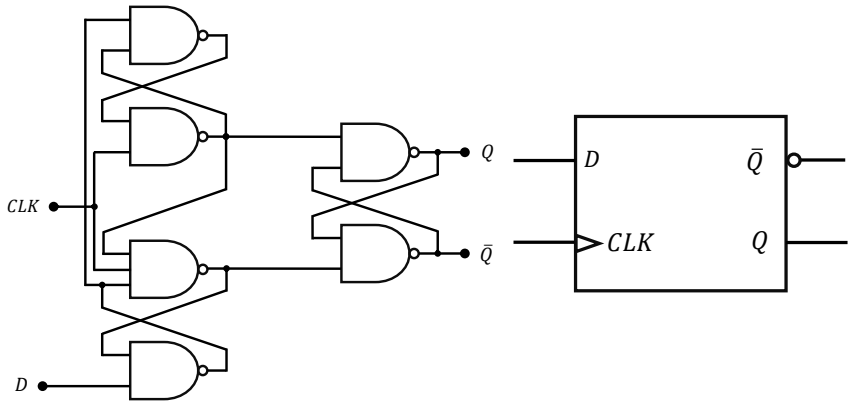


Figure 3.4: Behavior of the Flip-Flop, showing that the output Q is Data when the clock signal is rising.

The flip-flop tested has a simulated rising time of 20 µs and a falling time of approximately 9.4 µs. The circuit for the positive edge triggered DFF is composed of NAND gates, and in Figure 3.5 it is represented its schematic and symbol.



(a) Schematic. (b) Symbol.

Figure 3.5: D-Type Flip-Flop.

3.4 Clock generator

The clock generator is composed of a cascade 20 inverters and a NAND gate in a feedback loop, also known as a Ring Oscillator (RO), Figure 3.6. The first delay stage is a NAND gate to have the possibility to impose a variation in the circuit in case the circuit do not start in the test phase. For the RFID logic circuit it is required 3 signals with different phases from each other, as seen in the block diagram of the circuit, represented in Figure 3.1. The 3 outputs are as follows: $\overline{Out_1}$ is node 3, $\overline{Out_2}$ is node 9 and $\overline{Out_3}$ is node 19 of the RO. It is also important to note that each output of the clock generator, prior to its application on the rest of the circuit, undergoes a buffering stage composed of a NOT gate.

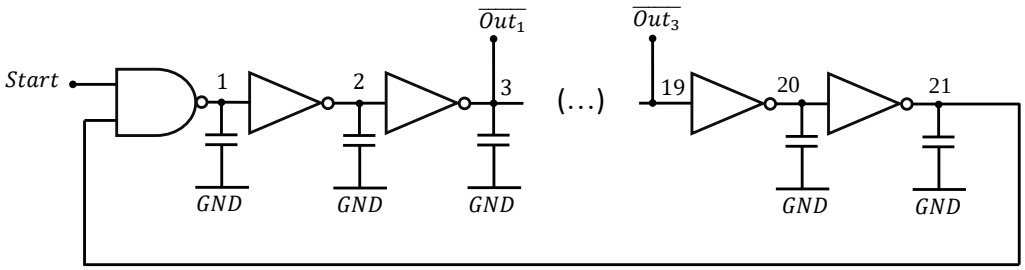


Figure 3.6: Schematic of the clock generator.

The frequency of the RO depends on the delay of each stage, so to decrease the oscillation frequency it is added a capacitor between each inverter. In Figure 3.7 it is represented

the variation of the frequency of the RO as a function of the capacitance of the capacitor on each delay stage.

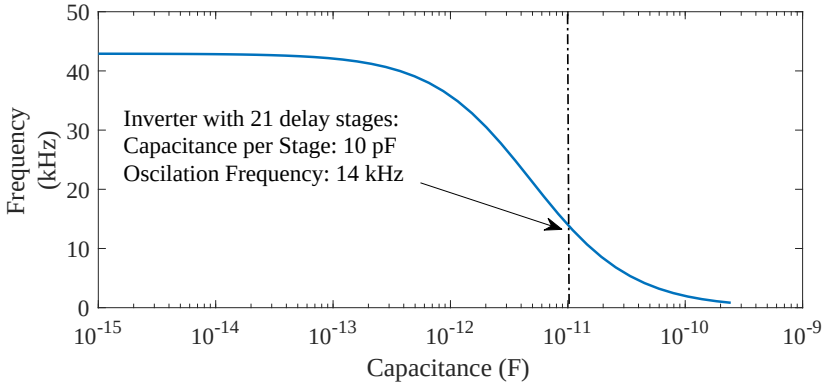


Figure 3.7: Variation of the RO oscillation frequency as a function of the stage capacitance.

For an oscillation frequency of 14 kHz the capacitor in each stage of the RO must have a capacitance value of 10 pF.

3.5 5-bit Counter

For the RFID logic circuit, it is required to divide the signal provided by the clock generator 5 times, so using the DFF it was designed a 5-bit Counter, as seen in Figure 3.8. Moreover, in Figure 3.11a it is represented the input signal and the 5 output signals of the counter.

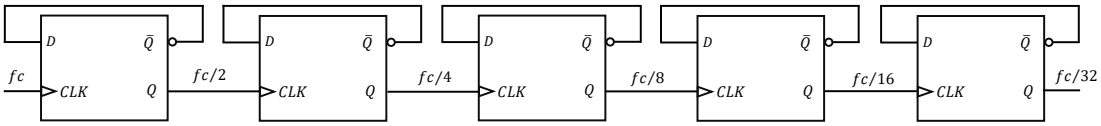


Figure 3.8: Schematic of the 5-bit Counter.

In Figure 3.9 it is represented the logic behavior of a 1-bit Counter (with only one Flip-Flop). The logic is repeated for a 5-bit Counter.

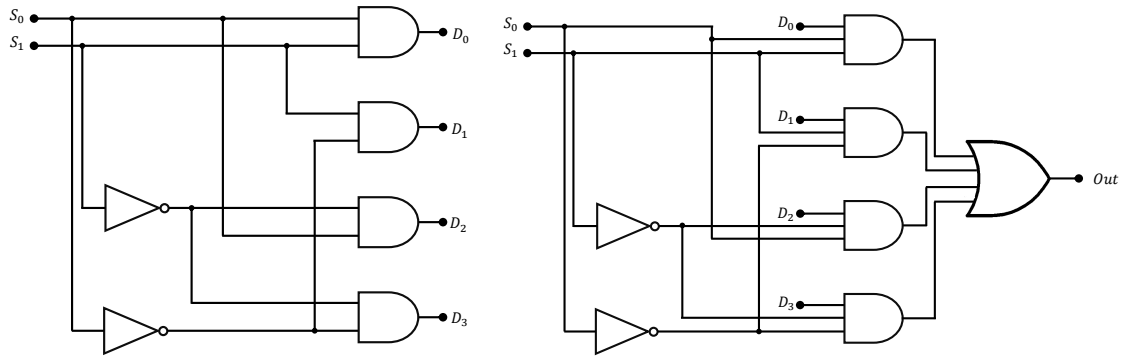
CLK	D	Q	Q_n
0	1	0	1
1	0	1	0
0	0	1	0
1	1	0	1
0	1	0	1

Figure 3.9: Logic behavior of a 1-bit Counter.

Since the Flip-Flop used is a positive edge-triggered, only when the signal is rising from 0 to 1 does the output Q is Data (green arrow in Figure 3.9). Assuming the first state of Q is 0, when the clock is enable (0 to 1 transition) the data value (1 due to the feedback) passes to the output Q and D goes to 0. After this, the clock goes from 1 to 0, but there is no change in the output, only after clock signal rises again does the output goes to 0. This means that at the output the signal change after two periods at the input.

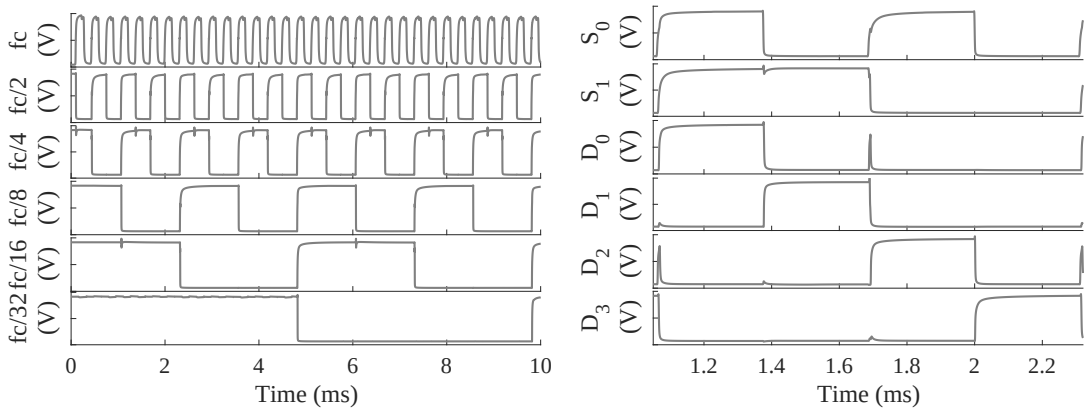
3.6 4 Line Select

To select all lines of the memory it was designed the circuit represented in Figure 3.10a, which generates a pulse that sweep all the outputs consecutively, allowing to activate one line of the memory at a time. This kind of circuit is also called a decoder and in Table D.3 it is represented the truth table of the circuit and in Figure 3.11b it is represented the input and output signals of the 4 Line Select circuit.



(a) (b)

Figure 3.10: (a) Schematic of the 4 Line Select circuit; (b) Schematic of the 4 to 1 Multiplexer.



(a) (b)

Figure 3.11: (a) Input and 5 outputs of the 5-bit Counter; (b) Inputs and outputs of the 4 Line Select circuit.

3.7 4 to 1 Multiplexer

To read the columns of the memory it is used a 4 to 1 Multiplexer (MUX), which takes the value of each column at a time and represents it in the output. The inputs of both the 4 line decoder and the multiplexer are the outputs of the 5-bit Counter (Figure 3.1), meaning that for each cycle of the multiplexer only one line is activated at a time, the cycle is then repeated for the following line in memory.

In Figure 3.10b is represented the circuit of the 4 to 1 MUX and, in Table D.4 it is represented the truth table of the circuit. In Figure 3.12 it is represented the inputs and output of the Multiplexer for a test signal.

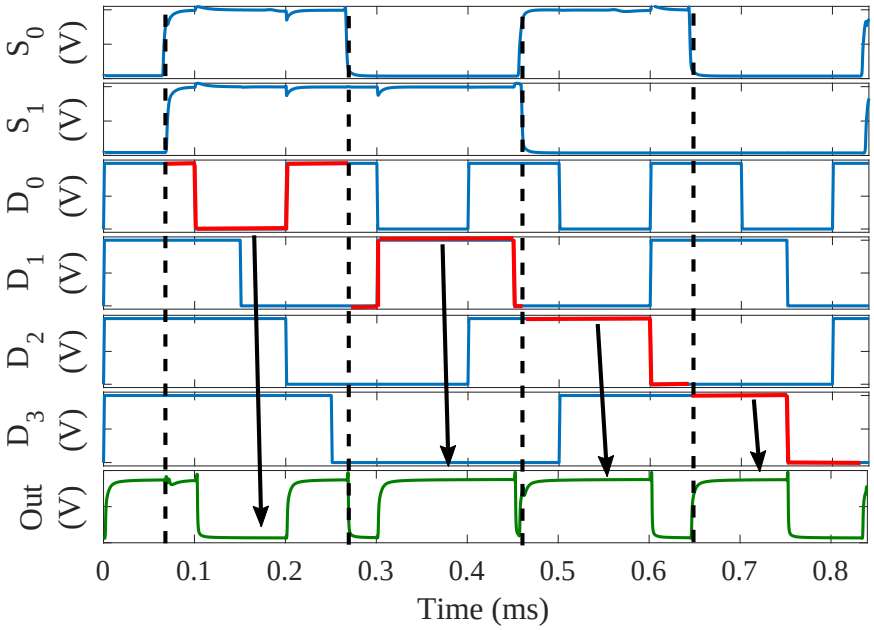


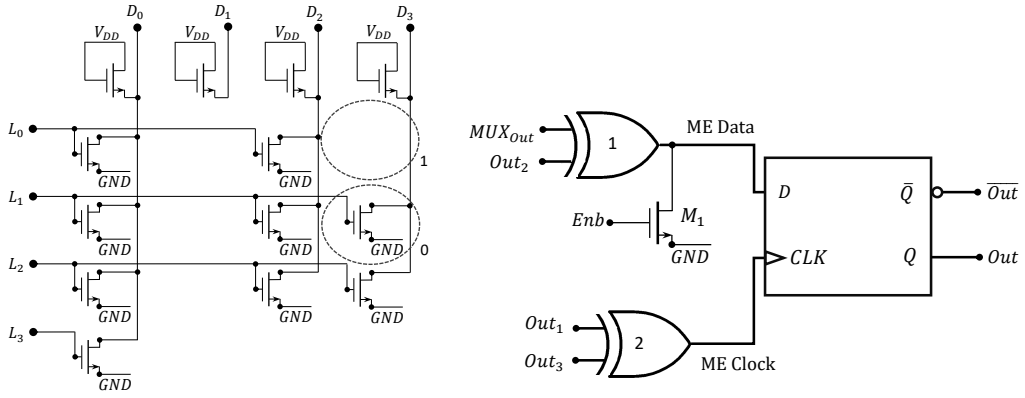
Figure 3.12: Inputs and output of the 4 to 1 Multiplexer.

3.8 16-bit Read Only Memory

The memory employed is a 16-bit ROM and its data is read by applying V_{DD} to the line of the desired bit, this will turn on all transistors on that line. After this step, the voltage on each column is read sequentially, being 0 if a transistor is present and 1 if not, as described in Figure 3.13a. The high value is obtained thanks to a diode connected transistor in each column.

3.9 Manchester Encoder

After the ROM data is read, the serial signal is encoded using a Manchester encoding Technique. The Manchester encoding is used in bit serial digital communications and is also known as phase encoding [2]. Unlike other type of encoding, this technique does

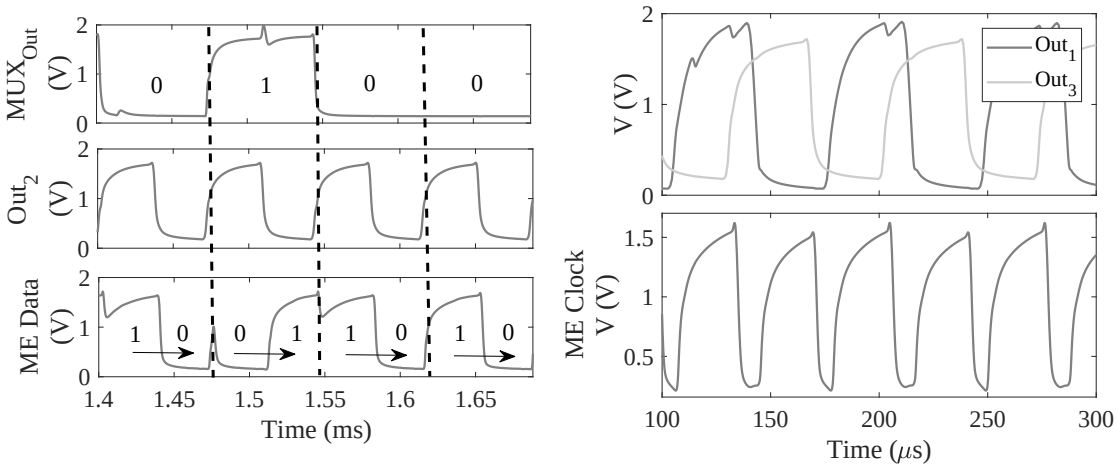


(a) (b)

Figure 3.13: (a) Circuit schematic of the implemented memory ROM employed. The data in the memory is 0101, 0100, 0100, 0111; (b) Circuit of the Manchester encoder.

not require the clock signal to be sent along with the serial signal, since Manchester encoding allows for easier synchronization with the receiver. Also, when compared to Non Return to Zero (NRZ) encoding [2], Manchester encoding has less noise interference since this type of encoding has more level transitions which are easier to detect than constant signals in time. The circuit of the encoder is represented in Figure 3.13b and its input is the output of the Multiplexer as seen in Figure 3.1.

This circuit was adapted from [16] and it is composed of 2 XOR gates and a DFF. The encoder is essentially one XOR gate, XOR 1, which the clock signal is one of the outputs of the ring oscillator, Out_2. In Manchester encoding a 0 corresponds to a '10' transition while the 1 corresponds to a '01' transition as defined by IEEE 802.3 standard [26]. The input and output wave forms of the XOR gate are represented in Figure 3.14a.



(a) Xor 1. (b) Xor 2.

Figure 3.14: Inputs and Outputs of the two Exclusive OR gates of the Manchester Encoder represented in Figure 3.13b.

As seen in Figure 3.14a, the output of the XOR gate produces a lot of undesirable voltage peaks. Hence, to clean the output signal, it is used the DFF previously implemented. However, it is also required a clock signal with a higher frequency or since the DFF is positive edge-triggered, a clock signal with at least more signal transitions. For this, it is used a second XOR which the inputs are two more signals from the ring oscillator out of phase from each other, Out_1 and Out_3, the result is shown in Figure 3.14b.

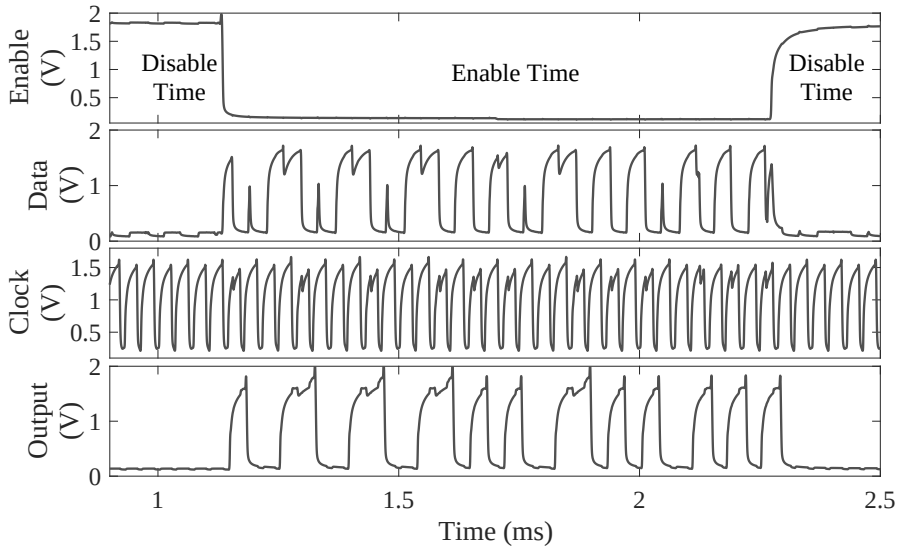


Figure 3.15: Enable, inputs and output of the DFF employed in the Manchester encoder.

In Figure 3.13b, after the encoding process it is used a transistor, M_1, to bring the signal to low state once the memory is read. The enabling signal is one of the outputs of the 5-bit Counter, with a frequency of fc/32, and for each period of this signal the memory is completely read, this allows the output signal to, periodically, show the desired signal as it can be seen in Figure 3.15.

3.10 Final Circuit

In Figure 3.16 it is represented the ROM signal and the output signal of the RFID.

The power dissipation of the RFID logic circuit is determined by the expression (3.1):

$$P_{DD} = I_{RMS} \times V_{DD} \tag{3.1}$$

where I_{RMS} represents the root-mean-square current consumption. With a V_{DD} of 2 V the power dissipation of the RFID logic circuit is 810.8 µW. It is important to note that the output buffers have not been included in the determination of the power dissipation

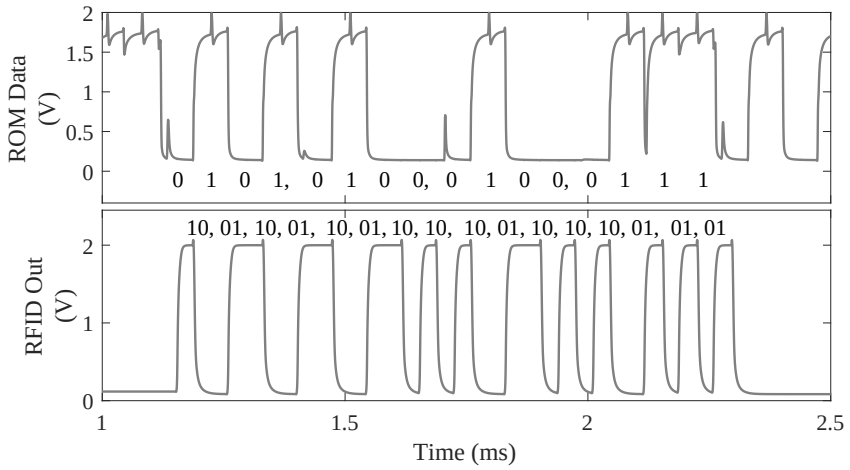
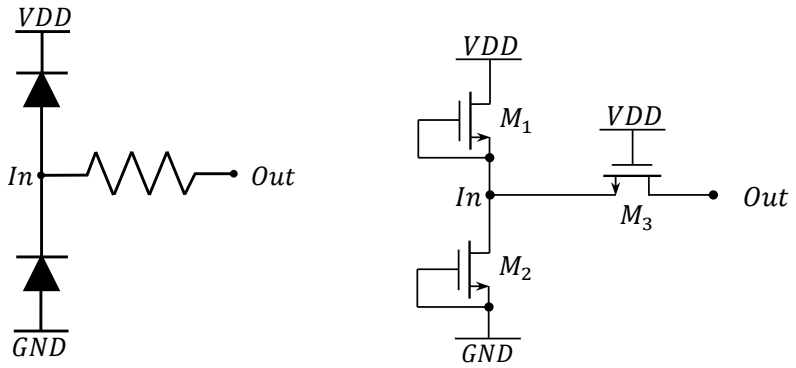


Figure 3.16: ROM and output signal of the RFID after the Manchester encoding. In the Figure it is also represented the serial bit array of the ROM and the Manchester encoder.

3.11 Auxiliary Testing circuitry

3.11.1 ESD protection circuit

In Chapter 2 it was shown that the transistors used for this circuit have a dielectric with a thickness of about 20 nm, this means that the circuit is prone to dielectric breakdown in the face of an electrostatic discharge. This is even more critical for circuit inputs which are directly connected to gates of transistors, like the start pin represented in Figure 3.6. To minimize this, it is used the circuit presented in Figure 3.17a, consisting of two reverse--biased diodes and a resistor in order to limit the current flow and to drain excess current to the rails. However, for the circuit to be fabricated in CEMOP at FCT/UNL, it is required to be made entirely of TFT. In Figure 3.17b it is represented the proposed circuit using TFT devices.



(a) Schematic. (b) TFT topology.

Figure 3.17: ESD protection circuit (primary protection only).

3.11.2 Output Buffer

For testing purposes, it is necessary to design special buffers for properly driving the test probes or, otherwise, the capacitive load of the probes colapses the signal, making very difficult to analyze the circuit. The circuit proposed consists of 2 inverters and 2 high gain inverters cascaded in series, as presented in Figure 3.18.

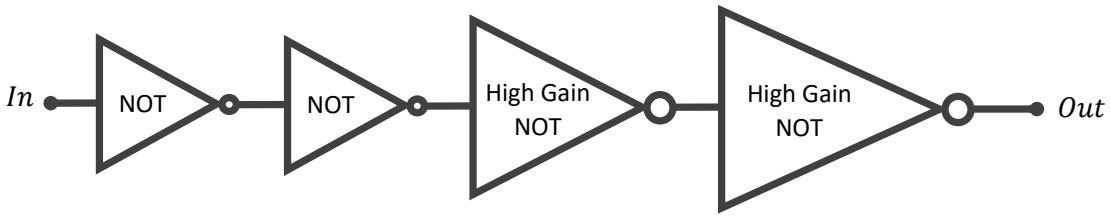
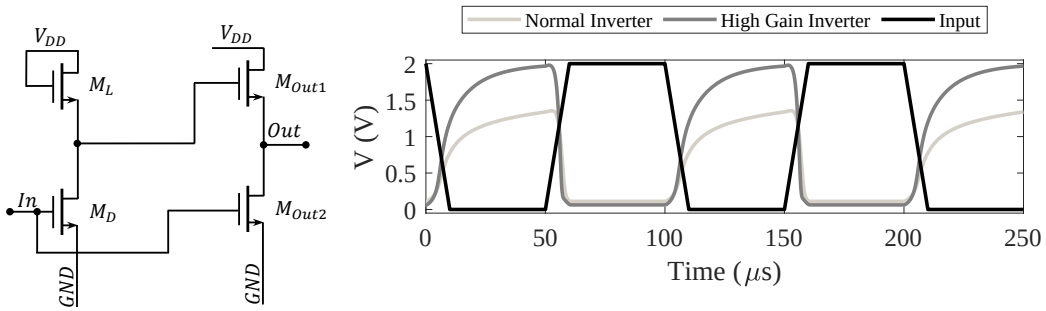


Figure 3.18: Schematic of the output buffer driver.

3.11.2.1 High Gain Inverter

The High Gain inverter has the same logic function as the inverter. However this circuit can drive a bigger load faster than a normal inverter and its circuit is represented in Figure 3.19a.



(a) (b)

Figure 3.19: (a) Circuit of the high gain inverter; (b) Output of a regular inverter and high gain inverter for a 50 pF load.

This circuit consists of a voltage combiner, transistors M_{Out1} and M_{Out2}, with an inverter, transistors M_D and M_L. The bigger the load that the high gain inverter is driving the bigger the W of the transistors of the voltage combiner must be, at the expense of more current.

In Figure 3.19b, it is represented the input and output signal of a regular inverter and a high gain inverter with W of the output transistors of 100 µm for a 50 pF load.

3.11.2.2 Final Buffer Circuit

The dimensions of the transistors employed in the 2 high gain inverters are represented in Table 3.2. As it can been seen in the Table, the transistor's sizing of the output transistors consecutively increase to drive the output capacitive load, while the 2 first regular inverters drive the high gain inverters.

Table 3.2: Dimensions of the two high gain inverters employed in the output buffer

	1^{st} High Gain				2^{nd} High Gain			
Transistor	M_L	M_D	M_{Out1}	M_{Out2}	M_L	M_D	M_{Out1}	M_{Out2}
W (µm)	15	5	100	100	100	5	300	300
L (µm)	2	2	5	5	5	2	5	5

In Figure 3.20 it is represented the output of the RFID logic circuit with a capacitive load of 150 pF with and without the output buffer. It is important to mention that, for testing purposes it was also used output buffers in: one of the outputs of the clock generator; all 5 outputs of the counter circuit and the memory output.

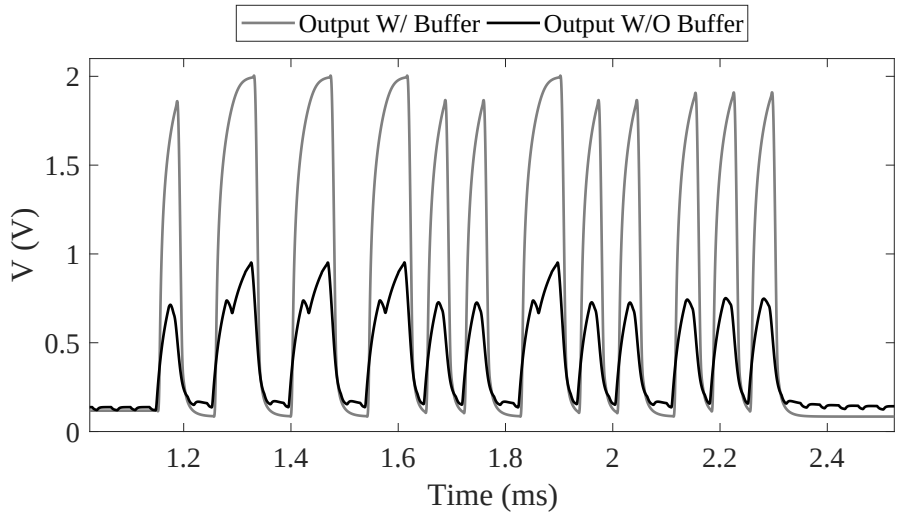


Figure 3.20: RFID logic circuit output with and without a buffer stage.

Chapter 4

Layout and Test setup

4.1 Layout Description

4.1.1 Fabrication Considerations

Before fabrication it is important to note some details regarding the layout of some layers. The fabrication process follows the following order:

- Gate electrode (metal 1), molybdenum with 17 nm;
- Dielectric insulator, AlO_x with 20 nm;
- Semiconductor, a-IGZO with 22 nm;
- Source-Drain electrode (metal 2), molybdenum with 70 nm;
- First passivation layer (interlevel dielectric), parylene with 700 nm;
- Metal 3, molybdenum with 350 nm;
- Second passivation layer, parylene with 1 µm.

In Figure 4.1, it is represented a cross section of a transistor and a connection via with all layers, including passivation layers. As it can be seen in Figure 4.1, unlike all the other layers which are only deposited where needed, the gate dielectric is deposited in all the substrate and is only patterned in connection vias.

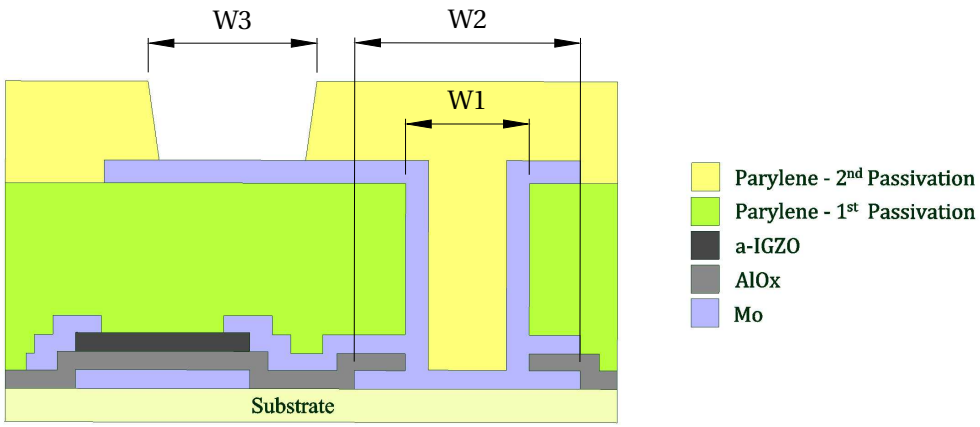


Figure 4.1: Cross section of a transistor and a via with passivation layers. The thickness of each layer is not to scale.

To connect the 3 conductive layers, gate, source-drain and Metal 1, it is required connection vias, as seen in Figure 4.1. A via is made of a square hole through the first

passivation layer and the dielectric gate insulator with the width of W1, followed by the deposition of molybdenum, also in a square shape, in every conductive layer with a width of W2. This is made to ensure a good connection between all layers. Hence, in Figure 4.1, the transistor represented has the source-drain electrode connected to the Metal 1 layer which is then available to the exterior of the circuit, since there is a region which does not have the second passivation, in this case with a width of W3.

4.1.2 Proposed Layout

In Figure 4.2 is represented the proposed layout for the RFID digital circuit properly sized in the previous Chapter. In Appendix E it is also represented the proposed layout without the representation of the blocks. The proposed layout has 251 transistors and length and width of 18.6 mm and 10 mm respectively. In contrast, the substrate has a length and width of 21 mm and 21 mm respectively. This means, that the final layout has two logic circuits to maximize area.

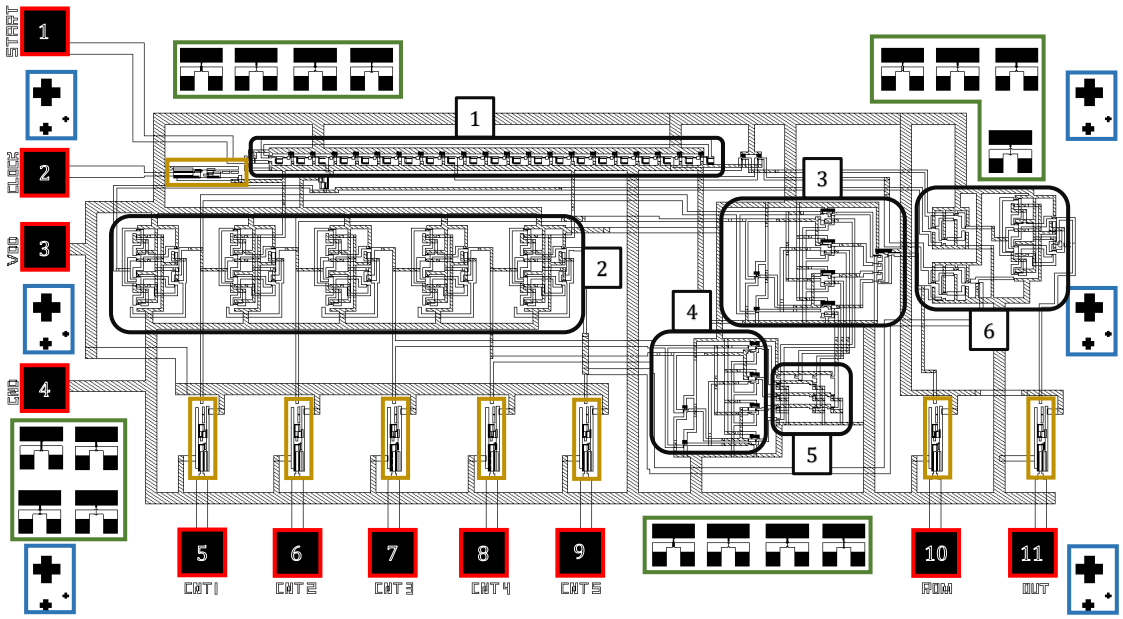


Figure 4.2: Proposed layout for the RFID digital circuit. The blocks colored are for testing purpose, while the blocks in black represent the RFID digital circuit.

In Figure 4.2, the colored blocks represent the testing blocks and are as follows:

- In red, are represented the output pads used for test probes to analyze the circuit. These pads, include the power rails, the start pin for the clock generator and all 8 outputs of the circuits;

- In blue, are represented alignment marks, used in the fabrication process. These marks are deposited in all layers;

- In green, are represented test transistors with the dimensions of the transistors used in simulation. This process allows the study of the variation of the transistor's behavior along the substrate area;
- In yellow, are represented the buffers used to charge the output pads and test probes.

In Figure 4.2, the black blocks represent the RFID logic circuit and are as follow:

1. Clock Generator;
2. 5-bit Counter;
3. 4-1 Multiplexer;
4. 4 Line Select;
5. 16-bit ROM;
6. Manchester Encoder.

The layout was designed from scratch without any existent library for any device. The dimensions of the transistors available at this work are 5/2, 50/2, 50/5 and 100/5, being the 5/2 transistors the smallest feature in the layout. However, since the connection vias have a dimension of 50 µm over 50 µm, the smallest length of the metal lines is 50 µm. For long lines the length is 100 µm while for supply lines the length is about 100 µm. These values can vary thought out the layout, since this is a full custom design.

4.2 Test Setup

In order for the circuit to be tested there are some considerations that worth mentioning. In Figure 4.2, the pads are represented in red and are as follows:

1. Start pin, which must be connected to V_{DD} for the clock generator to oscillate. This pin can be disconnected and then connected to impose a change in the system, if the clock generator does not start automatically;
2. Out_1 of the clock generator;
3. V_{DD} with a maximum value of 2 V, due to the possibility of gate dielectric breakdown at higher gate voltages.
4. GROUND;
5. Output of the 5-bit Counter with a frequency of fc/2;
6. Output of the 5-bit Counter with a frequency of fc/4;
7. Output of the 5-bit Counter with a frequency of fc/8;

8. Output of the 5-bit Counter with a frequency of fc/16;
9. Output of the 5-bit Counter with a frequency of fc/32;
10. Output pin of the 16-bit ROM;
11. Output pin of the RFID logic circuit.

Chapter 5

Conclusions and future perspectives

The main objective of this work was to model thin film transistors, using the a-Si Level 61 TFT Model with the aid of genetic algorithms, and then to design an RFID logic circuit for proof-of-concept.

The model used was the physical model a-Si Level 61 TFT Model. This model comprises 17 variable parameters, which would require a high number of curve fittings and could be prone to errors due to the fitting process. Instead, it was used a "vanilla" genetic algorithm to determine the parameters using experimental curves (transfer and output) as target data. With this methodology it was possible to accurately model the measured transistors with *W/L* of 5 µm/2 µm, 50 µm/5 µm and 100 µm/5 µm. In Table 5.1 are represented the average errors between the experimental curves and the model for the transfer and output characteristics.

Table 5.1: Average error between experimental curves and the model for the transistors experimentally measured.

Transistors	Transfer curve	Output curve
5 µm/2 µm	12.10%	3.15%
50 µm/5 µm	8.82%	4.61%
100 µm/5 µm	14.26%	3.20%

As it can be seen in the Table 5.1, there is a smaller error for the output characteristics curves, which means that it is easier for the model to correctly express the output curves than the transfer ones. This happens, because the output characteristics are mainly dependent on four parameters, whilst the transfer curves are dependent on all the remaining parameters. This means that the algorithm can reduce the average error for the output curves easily, when compared with the corresponding transfer characteristics. Nevertheless, the results obtain result in a low discrepancy in terms of DC analysis, however for the AC component, it was only measured the overlap capacitances of the transistors, since these were the only parameters of the model required for an AC analysis. This simple AC component of the model can result in a larger difference between the simulation and experimental results, being more critical when dealing with analog circuits. For digital circuits, this inaccuracy of the AC model mainly affects the study of rise and fall time of circuits, since the effective capacitance of each gate is not entirely correct. One solution for this problem, is to do a close study of a ring oscillator, since this circuit oscillates at a frequency determined by the delay of each stage. By comparing simulated and experimental results, it would be possible to get a better idea of the capacitances of each transistor.

After this analysis, the determined values of the capacitances, could be introduced in the model as extrinsic components to compensate any discrepancy.

Regarding the RFID digital circuit, it has been designed a logic circuit that once the Start pin is connected to V_{DD}, it generates a clock signal using a 21-stage ring oscillator with an oscillation frequency of 14 kHz. To generate such frequency, the RO has one capacitor at each stage with a capacitance of 10 pF, however at first it was design a 9-stage RO with capacitors on each stage of 88 pF and an oscillation frequency of 14 kHz. For this circuit, the capacitors were composed of an electrode at the gate level and another at the source-drain level with gate dielectric between them. This dielectric was prepared through a solution process, and deposited in the substrate with a spin-coating technique. The result was a gate dielectric with a thickness of around 20 nm, as presented in [24] this dielectric was studied and it was concluded that for devices with big area it was prone to failure due to high leakage current. So, in conclusion, by increasing the number of stages and establish a higher oscillation frequency it was possible to reduce the total area of capacitors required by 5 times, when comparing the 9-stage and the 21-stage RO, decreasing the possibility of failure of the capacitors.

After the generation of the clock phases, the signal is divided 5 times through a 5-bit Counter, which then feeds a 4 line select decoder and a 4-1 multiplexer to read a 16-bit ROM. The first one selects one line at a time, while the second one read each column consecutively, resulting in a 16-bit serial signal. After this, the signal is encoded through a Manchester Encoding technique, generating the final 32-bit serial signal. In Table 5.2 are represented the features of the RFID logic circuit designed in this work.

Table 5.2: Features of the RFID logic circuit.

Features	Diode Load (This work)
#TFTs/inv	2
Inverter Area (μm^2)	15210
Chip Area (mm^2)	180.6 (18.6×10)
#TFTs	251
#Supplies	2
Memory	16-bit ROM
Clock Generation	21-Stage RO
Data Rate	14 kbit/s
Substrate	Glass

Since the topology of the logic circuit designed is mainly based in diode loads, the number of transistors per inverter, the inverter area and the number of supplies will be the lowest possible, when comparing to other topologies as presented in the state-of-the--art, in Appendix A. However, the overall chip area is larger, since the layout presented is

not completely optimized regarding the chip area.

Other important factor regarding RFID logic circuits is the power dissipation, since the ultimate goal of an RFID tag is to self-generate the required power from the carrier of the reader, meaning that the overall power budget is quite limited. The designed circuit has a power dissipation of 810.8 µW, which compared to other RFID circuits is high. The reason for this high current is that the methodology used during the designed process was to increase the circuit speed, by means of using minimum channel length and to increase the signal excursion.

Finally, one big advantage of the circuit designed in this work is the minimum supply voltage that the circuit requires to work, which can be as low as 2 V. For other RFID logic circuits with a-IGZO TFTs the supply voltage is in the range of 5 to 6 V and in some circuits with a pseudo-CMOS topology it is also necessary a second supply with a voltage of $2 \times V_{DD}$. This means, that regarding the harvesting of power from the reader signal, the circuit designed in this work can extract the required power from higher distances between the tag and reader.

As stated before, the goal at long term, is to allow the integration of these devices in an IoT application mainly through smartphones, using an NFC barcode protocol, like the ISO14443 Type A NFC standard [19], which would require the circuit to operate at high frequencies, in the order of tens of Megahertz. However, using the configuration employed in this work of bottom gate TFTs, the transistors would have high parasitic capacitances, resulting in a high delay through out the circuit and hence a degradation of the signal. This problem could be solved through different transistor's configurations, like Self-Aligned top gate TFTs [27], which would result in lower parasitic capacitances and allow circuits to operate at higher frequencies. Regarding fabrication of the circuit, the layout masks are already available and fabrication/characterization will undergo in the following weeks.

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Appendix A

State-of-the-art

Table A.1: Summary and comparison of State-of-the-art, for RFID circuits with a-IGZO TFT.

	Zero VGS Load [15]	Diode Load [16]	Diode Load [17]	Pseudo CMOS [17]	Dual Gate Source-Drain Level [17]	Dual Gate Metal 1 Level [17]	Pseudo CMOS SAL [19]
#TFTs/inv	2	2	2	4	2	2	4
Inverter Area (μm^2)	n.a.	n.a.	19350	36425	40300	19350	29277
Chip Area (mm^2)	70 (7×10)	5.85 (3.9×1.5)	8.046 (2.70×2.98)	15.76 (4.69×3.36)	15.13 (3.91×3.87)	8.478 (2.70×3.14)	50.55 (6.03×8.38)
#TFTs	1026	222	218	436	218	218	1712
Memory	Preamble+ 4-bit ROM	16-bit ROM	12-bit Decoder	12-bit Decoder	12-bit Decoder	12-bit Decoder	128-bit ROM
#Supplies	2	2	2	3	3	3	3
Clock Generation	11-Stage ring osc	9-stage ring osc	19-stage ring osc	19-stage ring osc	19-stage ring osc	19-stage ring osc	Division from carrier
Data Rate	0.05 kbit/s	3.2 kbit/s	71.6 kbit/s	43.9 kbit/s	11.3 kbit/s	25.8 kbit/s	105.9 kbit/s
Substrate	Glass	Glass	PEN-foil	PEN-foil	PEN-foil	PEN-foil	PI-foil

Appendix B

Model Equations

The equations of the Level 61 a-Si TFT Model are available at the Model manual [20].

B.1 Temperature Dependence

$$\alpha_{sat} = ALPHASAT + KASAT(TEMP - TNOM) \tag{B.1}$$

$$V_T = VTO + KVT(TEMP - TNOM) \tag{B.2}$$

$$V_{tho} = k_b \times \frac{TNOM}{q} \tag{B.3}$$

$$V_{th} = k_b \times \frac{TEMP}{q} \tag{B.4}$$

$$V_{aat} = VAA \times exp\left[\frac{EMU}{q \times GAMMA}\left(\frac{1}{V_{th}} - \frac{1}{V_{tho}}\right)\right] \tag{B.5}$$

B.2 Drain Current

$$I_{min} = SIGMA0 \times V_{ds} \tag{B.6}$$

$$I_{hl} = IOL \times \left[exp\left(\frac{V_{ds}}{VDSL} - 1\right)\right] \times exp\left(-\frac{V_{gs}}{VGSL}\right) \times exp\left[\frac{EL}{q}\left(\frac{1}{V_{tho}} - \frac{1}{V_{th}}\right)\right] \tag{B.7}$$

$$I_{leakage} = I_{hl} + I_{min} \tag{B.8}$$

$$V_{gfb} = V_{gs} - VFB \tag{B.9}$$

$$V_{gfbe} = \frac{VMIN}{2} \times \left[1 + \frac{V_{gfb}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gfb}}{VMIN} - 1\right)^2}\right] \tag{B.10}$$

$$V_{gt} = V_{gs} - V_T \tag{B.11}$$

$$V_{gte} = \frac{VMIN}{2} \times \left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1\right)^2}\right] \tag{B.12}$$

$$t_m = \sqrt{\frac{EPS}{2q \times GMIN}} \tag{B.13}$$

$$V_e = \frac{2 \times V0 \times V_{tho}}{2 \times V0 - V_{tho}} \tag{B.14}$$

$$n_{so} = N_C \times t_m \times exp\left(-\frac{DEF0}{V_{th}}\right), Nc = 3.0 \times 10^2 5m^{-3} \tag{B.15}$$

$$n_{sb} = n_{so} \times \left(\frac{t_m}{TOX}\frac{V_{gfbe}}{V0}\frac{EPSI}{EPS}\right)^{\frac{2 \times V0}{V_e}} \tag{B.16}$$

$$n_{sa} = \frac{EPSI \times V_{gte}}{q \times TOX}\left(\frac{V_{gte}}{V_{aat}}\right)^{GAMMA} \tag{B.17}$$

$$n_s = \frac{n_{sa} \times n_{sb}}{n_{sa} + n_{sb}} \tag{B.18}$$

$$g_{chi} = q \times n_s \times MUBAND \times \frac{W}{L} \tag{B.19}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi} \times (RS + RD)} \tag{B.20}$$

$$V_{sate} = \alpha_{sat} \times V_{gte} \tag{B.21}$$

$$V_{dse} = \frac{V_{ds}}{\left[1 + (V_{ds}/V_{sate}^M)\right]^{1/M}} \tag{B.22}$$

$$I_{ab} = g_{ch} \times V_{dse} \times (1 + LAMBDA \times V_{ds}) \tag{B.23}$$

$$I_{ds} = I_{leakage} + I_{ab} \tag{B.24}$$

Appendix C

Model Parameters

Table C.1: List of the parameters for the Level 61 a-Si TFT Model. In bold are the parameters that are constant through the optimization process and are equal to all 3 modelled transistors, with the exception of Cgd_{ov} and Cgs_{ov} which are calculated for each transistor in Chapter 2.

Name	Unit	Default	Description
ALPHASAT	-	0.6	Saturation modulation parameter
CGDO	Fm^{-1}	0.0	**Gate-drain overlap capacitance per meter channel width**
CGSO	Fm^{-1}	0.0	**Gate-source overlap capacitance per meter channel width**
DEF0	eV	0.6	Dark Fermi level position
DELTA	-	5	Transition width parameter
EL	eV	0.35	**Activation energy of the hole leakage current**
EMU	eV	0.06	**Field effect mobility activation energy**
EPS	-	11	**Relative dielectric constant of the substrate**
EPSI	-	7.4	**Relative dielectric constant of the gate insulator**
GAMMA	-	0.4	Power law mobility parameter
GMIN	$m^{-3}eV^{-1}$	1×10^{23}	Minimum density of deep states
IOL	A	3×10^{-14}	Zero-bias leakage current parameter
KASAT	$°C^{-1}$	0.006	**Temperature coefficient of ALPHASAT**
KVT	$V°C^{-1}$	-0.036	**Threshold voltage temperature coefficient**
LAMBDA	V^{-1}	0.0008	Output conductance parameter
M	-	2.5	Knee shape parameter
MUBAND	$m^2V^{-1}s^{-1}$	0.001	Conduction band mobility
RD	Ω	0.0	Drain resistance
RS	Ω	0.0	Source resistance
SIGMA0	A	1×10^{-14}	Minimum leakage current parameter
TNOM	°C	25	**Parameter measurement temperature**
TOX	m	1×10^{-7}	**Thin-oxide thickness**
V0	V	0.12	Characteristic voltage for deep states
VAA	V	7.5×10^{3}	Characteristic voltage for field effect mobility
VDSL	V	7	**Hole leakage current drain voltage parameter**
VFB	V	-3	Flat band voltage
VGSL	V	7	**Hole leakage current gate voltage parameter**
VMIN	V	0.3	Convergence parameter
VTO	V	0.0	Zero-bias threshold voltage

Appendix D

Truth Tables

Table D.1: Truth table of the exclusive OR.

In_1	In_1	Out
0	0	0
0	1	1
1	0	1
1	1	0

Table D.2: Truth table of the D-Type Flip-Flop. The X at the Data when the clock signal is falling means that its value does not change the outputs, while the Q_0 and Q_{0n} means that the outputs will keep the previous value.

D	CLK	Q	Q_n
0	$\uparrow$	0	1
1	$\uparrow$	0	1
X	$\downarrow$	Q_0	Q_{0n}

Table D.3: Truth table of the 4 Line Select circuit.

S_0	S_1	D_0	D_1	D_2	D_3
1	1	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
0	0	0	0	0	1

Table D.4: Truth table of the 4 to 1 multiplexer.

S_0	S_1	Output
1	1	D_0
0	1	D_1
1	0	D_2
0	0	D_3

Appendix E

Complete Layout

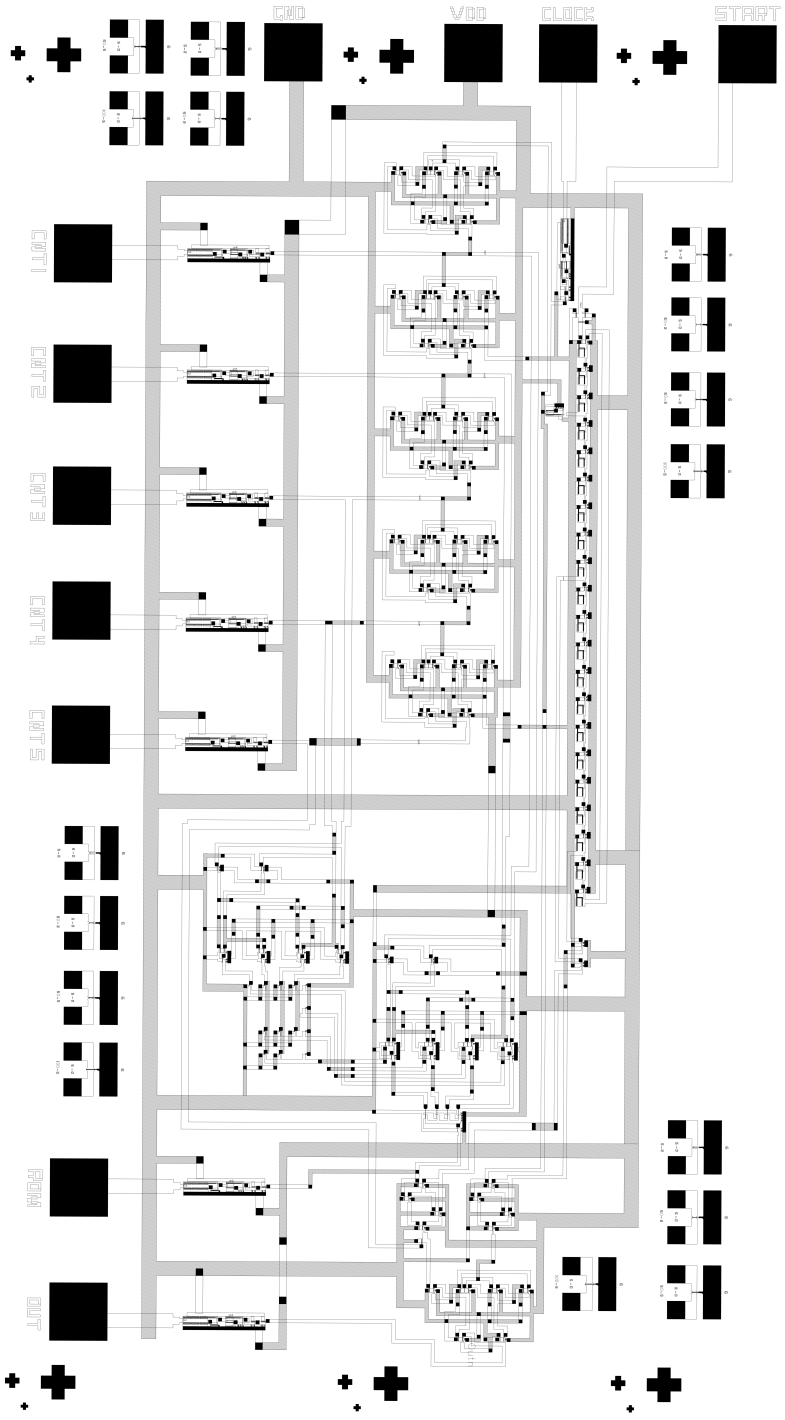

Figure E.1: Complete layout of the RFID logic circuit.