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Design of an Ultra Low Power RFCMOS Transceiver for a Self-Powered IoT Node

Dissertação para obtenção do Grau de
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"Everybody is a genious. But if you judge a fish by its ability to climb a tree, it will live its whole life believing that it is stupid."
Albert Einstein

Acknowledgements

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Abstract

In this thesis a transceiver characterized to consume ultra low power based in RFCMOS for a self-powered Internet of Things node is studied and designed. The transceiver consists in a simple Non-Coherent system, which means that the signal is picked up by the receiver based on energy detection, as a result it is one of the simplest existing transceivers once it does not need in the transmitter a complex pulse generator and certainly in the receiver as well. It is composed by an OOK modulator, a pulse generator that will determine the centre frequency and a driver amplifier connected to a 50Ω antenna for the transmitter. While in the receiver there is as first block a Low Noise Amplifier, a self-mixer that will prepare the signal for the integrator and a comparator working as a energy detector.

The UWB transceiver will be able to operate with a centre frequency of 4.5 GHz and a bandwidth of at least 500 MHz. It is critical to notice that the system is consuming a value of 96 mW for the power and accomplishing the power spectrum density -43 dBm/MHz using an OOK modulation technique. The entire system was implemented with standard 130nm CMOS technology.

Keywords: UWB, CMOS, IR, Low Power, transceiver, Internet of Things.

RESUMO

Nesta dissertação, apresenta-se o estudo e o dimensionamento de um transrecetor de radio de baixo consumo que recorre a uma técnica de impulsos de banda larga. O transrecetor é descrito por ser um sistema não-coerente, baseado num de deteção de energia. Esta aproximação permite reduzir a complexidade do circuito, pois não necessita de complicados geradores de impulsos. O emissor é constituído por um modulador OOK, gerador de pulsos, que irá determinar a faixa de frequência pretendida e um amplificador de saída conectado a uma antena de 50 Ω. Quanto ao recetor, este é constituído por um amplificador de baixo ruído, um auto-misturador que em conjunto com um integrador e um comparador implementam o detetor de energia de banda larga.

O transrecetor foi dimensionado para a faixa de frequência de 500 MHz, em torno dos 4.5 GHz. É de salientar o facto de o transrecetor apresentar consumos de 96 mW cumprindo o requisito da densidade espectral de potência -43 dBm/MHz. O transrecetor foi projectado tendo por base a tecnologia CMOS 130 nm.

Palavras-chave: UWB, CMOS, IR, Low Power, transceiver, Internet of Things.

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GLOSSARY

AFE analog front-end.

BSS basic service set.

DA driver amplifier.

ESS extended service set.

FCC federal communications comission.

IoT Internet of Things.

LAN Local Area Network.

LNA low noise amplifier.

NF noise figure.

PAN Personal Area Network.

RF radio frequency.

UWB Ultra Wide Band.

VCO voltage-controlled oscillator.

WAN Wide Area Network.

CHAPTER 1

INTRODUCTION

1.1 Motivation and Background

Recent projections point to a sustained growth of the Internet of Things (IoT), which size can reach the barrier of 50 billions of interconnected smart objects by the year of 2020. Since the scale of the CMOS technology will go down to 5 nm by 2020 is contributing to improve the functionality of a System on Chip (SoC), which is a key element of the heterogeneous integration imposed by the IoT node design. One of the cores of this global system is the remote node whose architecture, besides the digital processing unit, and the mixed-mode circuitry to perform the analog front-end (AFE) interface to the sensors, it includes a wireless radio module, with low-cost and low-power characteristics in order to meet the system requirements.

One of the main cores is the capability of the IoT node to communicate with its neighbors using a radio short-range wireless link. Besides the use of traditional transceivers architectures, an alternative is the utilization of a low-cost solution based on an impulse-radio (IR) Ultra Wide Band (UWB) approach. In the past 20 years, UWB has been mainly used for radar military systems. However, a significant change has happened in 2002 as the result of publication of power spectrum standard regulation that permitted the coexistence of UWB with others technologies. It was apprehensively seen by the others technologies supporters which have to share the spectrum with the "new" technology, much due to the fact that UWB occupy an huge bandwidth in comparison with the others and that bandwidth is in overlap [1].

After some discussions the national and international regulator entities converged to an agreement concerning the limits imposed to the radiated power that could be emitted by an UWB radio. The permitted maximum power allowed to emit is low and making it more suitable for short-range scenarios, namely, in personal area network (PAN).

However it should also be emphasized that the potential of UWB lies in the liability

to High-data Rate (HDR) at short distances and using Low Data Rates (LDR) for longer distances.

Even though this technology is making it first steps in the commercial area, several potential application were already implement or are under development:

- The wireless ad-hoc networks is one of the most promising applications of UWB technology. They are networks of hosts which are mobile and have no permanent infrastructure. The UWB technology is an ideal application for the wireless ad-hoc networks because it has a fine time resolution and precise locational capability, low transmit power and robustness against fading. ;
- In wireless sensor networks, used as sensors to monitor physical phenomena in the environment, as an example the creation of a smart highway using the advantages of good positioning capabilities and communication functionalities of IR-UWB. Once again UWB technology is one of the best candidates since its is a real small, low power and low cost technology [2];
- There is another technology where UWB fits perfectly which is, the Radio Frequency Identification (RFID). It, consists on an automatic identification technology, working with the same purpose of barcodes. Using the advantages of UWB with a precise position identification capability, greater connectivity and smaller technology [3];
- Consumer Electronics is another good applications for UWB where the benefits of of High Data Rate permits the transmission of data between media Centers, TVs and PC's peripherals and as well the elimination of cable connections which will increase the movement of the user [4];
- As said in some of the last points UWB can work with great precision and accuracy as a location system of objects, people and vehicular robots in indoor environments [4];
- One of the main applications for UWB systems is in medical applications, once it can work as human "scanner" since electromagnetic UWB pulses can penetrate in human body, different muscles have different reflection indices. Using RFID technology it is possible to monitor remotely and non-invasive the patients [5].

The present work propose the use of an IR-UWB transceiver and describes the design of such microsystem using a standard digital CMOS technology.

1.2 Thesis Organization

The thesis is organized in five chapters, including this introduction.

In chapter *I*, is an overview of the main importance of UWB to IoT devices, a brief introduction to the most important characteristic of a wireless communication giving

a special focus to UWB, presents the most important characteristics of UWB signals, it modulation, regulations and the definition of Gaussian pulses and a description of the most commonly used UWB systems. They can be coherent systems, differential coherent systems or non coherent systems.

The next chapter the fourth one, is where the implementation and simulation are established for each block of the system and nevertheless an overall simulation for the transceiver.

Finally the last chapter appears the main conclusions and suggestions for future work.

CHAPTER 2

UWB COMMUNICATION AND INTERNET OF THINGS

To make the reader aware of Impulse Radio Ultra Wideband (IR-UWB) and it role in Internet of Things (IoT) field it is necessary a certain knowledge about some basic concepts. These concepts have a relation with the contextualization of the IR-UWB transceiver as a wireless communication and several comparisons between other technologies that use IR-UWB.

Over the past years more and more people started to become almost permanently connected to internet. This permanent connection facilitates the link between the physical world (things and objects) with the virtual one (internet), known as Internet of Things (IoT).

It is expected that in 2020, looking to figure 2.1, from [6], the number of Internet-connected devices will be greater than 30 billion, and by the year of 2025 it is expected more than the double of the connected devices, in other words physical objects, as food, pharmaceutical packages, furniture, paper documents will be connected in a way that questions like "where", "who" or even "how" will have an answer in real time. All this information will be conceivable to obtain with the help of micro devices like radio tags which can be installed in gizmos, in order to track their condition and the surroundings, another feature is the localization since this tags have an IP address and a wireless connection system it permits to stablish a link between the object (physical world) and the virtual one. As disadvantages IoT is limited by energy, cost and size, to minimize this points, engineers are highly motivated. The technologies that benefit from the progress of IoT are:

- energy source, nowadays the size of batteries its considerably small but with the necessity of even smaller devices results in the need of reducing the size, one of the solutions to power the devices is to use alternative energy sources like solar, vibration and RF.

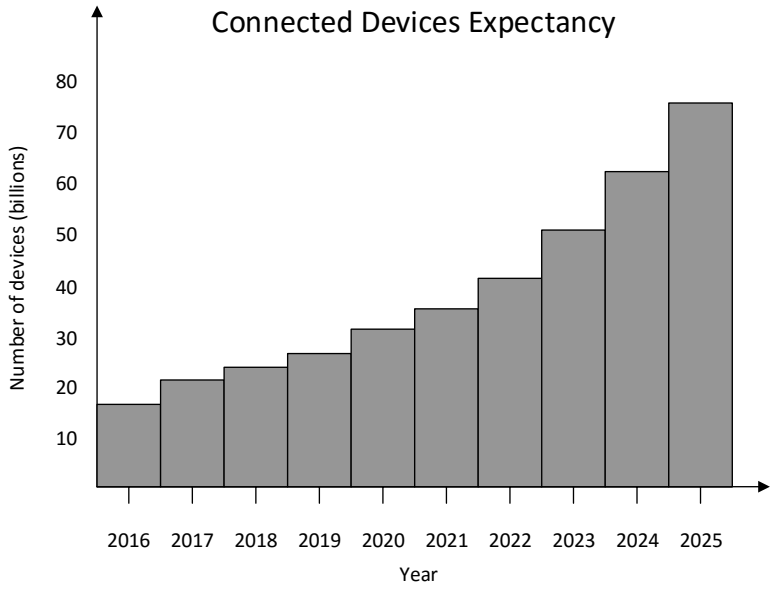

Figure 2.1: Graph of connected devices expected.

- wireless connection, IoT need a higher frequency in order to transmit the data with relatively good speed. The majority of the systems use ultra wideband technology, which presents many advantages to IoT devices such as robustness to fading, low power supply, enough resolution for indoor applications. On the other hand the narrowband systems do not present a satisfactory performance it need accurate frequency components which increases the complexity and overhead the power.
- integrated circuits, considering the fact that the majority of these devices need a certain mobility, the power consumptions is a crucial point to achieve.

As it is possible to conclude there are a vast number of applications based in IoT, [7], as major examples:

- In transportation and logistic domain, where advanced technology in cars, trains, buses and even in bicycles are all connected with the help of sensors, actuators and processing power. Making it accessible, for all type of users to have precise and in real-time information and interaction with the transportation services, roads, etc;
- Healthcare is one of the domains that benefit the most with IoT, which allows a constant monitoring of the patient in real time, at distance, allowing a reduction of the time permanence in the hospital. Another advantage in this domain is to have a real-time database access to hospital supplies, sending automatically a warning for restocking it;
- Smart buildings, from a domestic house, a museum or even an industrial plant, sensors and actuators can increase the quality of life or to turn that building more

profitable, as an example it can adjust automatically the lights, temperatures according to the weather;

- Personal and social domain, it will become a reality to automatically update through social networks, social activities and so on, receive notifications or track objects whenever people want to find it.

2.1 Wireless System Networks

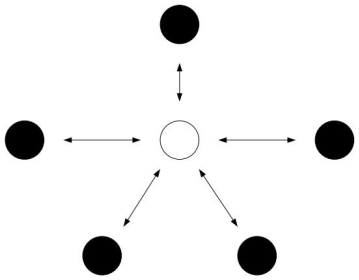

Figure 2.2: Star Network Topology.

Firstly, it should be mentioned that the most important types of transmission technologies use star and point to point links topology. In star figure 2.2 adapted from [8], the link is shared between every machine that are in the same network, the packages sent from one machine are received by all of the others.

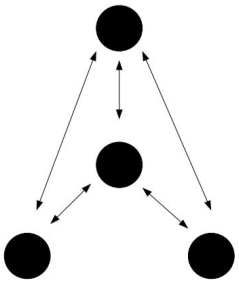

Figure 2.3: Point-to-Point Network Topology.

Meanwhile in point-to-point figure 2.3, adapted from [8], to go from the source to the final destination in a network is necessary to send small packages so that it will discover the best route through intermediaries machines.

2.2 Network Hardware by Scale

In addition to the last section we can characterize as well computer networks by it size which are the number of computers and area associated.

i) Personal Area Network (PAN) in figure 2.4, permits the communication up to a range of a person (10m), as an example, a computer and it peripherals, the main technologies that works in this area are Bluetooth, RFID and recently UWB [8];

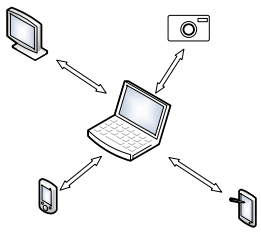

Figure 2.4: Personal Area Network scheme.

ii) Local Area Network (LAN) in figure 2.5 based in [8], it covers up to a private network which operates in a small building or a small factory the most known protocol to operate at this size is Wi-Fi;

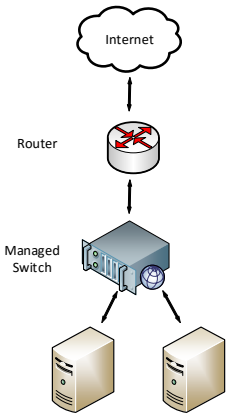

Figure 2.5: Local Area Network scheme.

iii) For longer range it exists the MAN and Wide Area Network (WAN) figure 2.6 adapted from [8], which are associated to cities scale range or even countries.

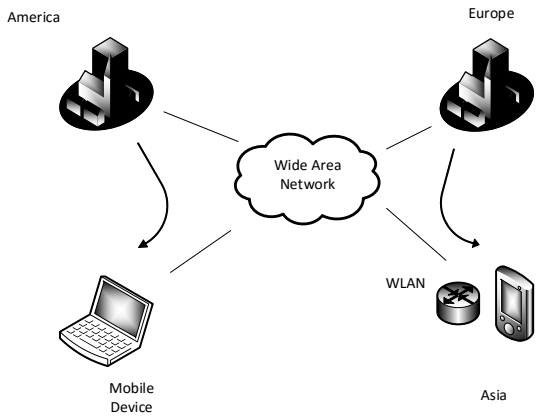

Figure 2.6: Wide Area Network scheme.

2.3 Wireless Communication Protocols

Throughout the recent years wireless technologies have been the focus of investment in telecommunication area which result in a great evolution of them, emphasizing nowadays the fact that almost every intelligent sensor system requires a permanent connection with the user and if one of the main characteristic is mobility for sure it must be wireless in figure 2.7 from [9]. As said before the wireless communications are extremely important when mobility matters, which as well will reduce the number of cables, this section has the purpose to explain the principal wireless protocols.

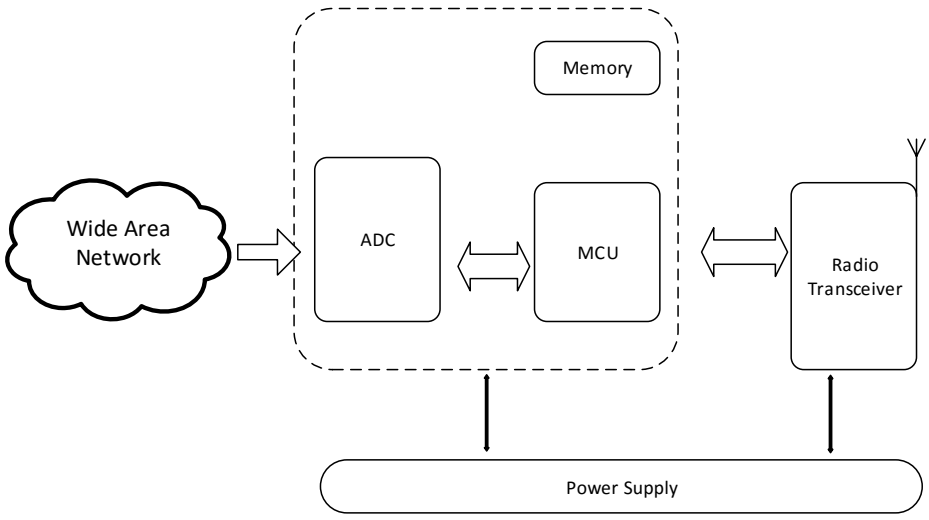

Figure 2.7: Block diagram of a intelligent sensor of communication.

2.3.1 Bluetooth- IEE 802.15.1

The protocol Bluetooth (IEE 802.15.1 standard) is basically a radio system wireless designed for short distances and low-costs devices with the intention of replacing cables of computer peripherals, by this it is possible to conclude it belongs to WPAN. There are two types of connectivity topologies, the piconet and the scatternet. In the first one, the device work as a master which is connected with several devices, working as slaves. The scatternet is a group of different Bluetooth devices overlapping in time and space. Bluetooth operates in the unlicensed 2.4GHz at a rate of 1Mbps [10].

2.3.2 Zigbee- IEE 802.15.4

This protocol, the Zigbee (IEE 802.15.4), working in the same scale of Bluetooth by this means, Wireless Personal Area Network, up to 10m. Zigbee provides self-organized, multi-hop and a reliable mesh networking with a long battery lifetime. Another advantage, it permits low-data rate wireless networking standards that can eliminate the costly and damage prone wiring in industrial control applications. It supports star and peer to peer technologies, Bluetooth is able to operate in the frequency band of 2.4 GHz with a rate of 250 Kbps [11].

2.3.3 Wi-Fi- IEE 802.15

One of the most well-known protocols in wireless technologies IEE 802.11 (Wireless Fidelity), this protocol belongs to Wireless Local Area (WLAN). All users are able to surf in the internet at great transmission velocities when connected to an access point or an ad-hoc node. The architecture of this system is based in a basic cell which is called basic service set, which is a collection of mobile or fixed stations. For any particular reason, If one of that stations moves from the basic service set (BSS), it will no longer belongs to the same BSS and as a consequence it will lose the ability to communicate with the members of that BSS. Based in this cell is the IBSS and an extended service set (ESS). Under these circumstances, whenever stations are able to directly communicate without an AP, to it is called an IBSS operation.

A IBSS may also form a component of an extended form of network that is built with a multiple BSS. The component responsible to interconnect as a BSS is the distributable

system (DS). Having a DS as APs, it is possible to create a Wi-Fi network ESS in figure 2.8, referred from [12].

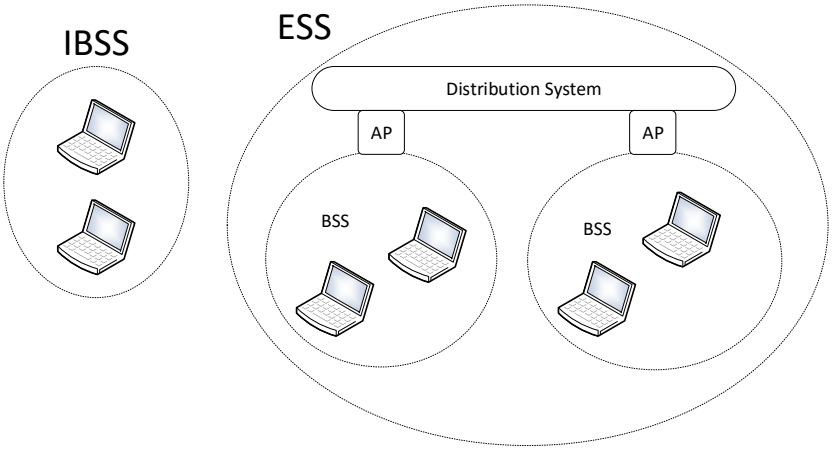

Figure 2.8: IBSS and ESS configurations of Wi-Fi networks.

2.3.4 Comparison of Technologies

Standard	**Bluetooth**	**UWB**	**ZigBee**	**Wi-Fi**
IEE spec	802.15.1	802.15.3*a*	802.15.4	802.11$a/f/g$
Frequency band	$2.4GHz$	$3.1-106GHz$	$915MHz; 2.4GHz$	$2.4GHz; 5GHz$
Max signal rate	$1Mb/s$	$110Mb/s$	$250Kb/s$	$54Mb/s$
Nominal range	$10m$	$10m$	$10-100m$	$100m$
Nominal TX Power	$0-10dBm$	$-41.3dBm/MHz$	$10-100dBm$	$15-20dBm$
Number of RF channels	79	$(1-15)$	$1/10; 16$	$14(2.4GHz)$
Channel bandwidth	$1MHz$	$500MHz-7.5GHz$	$0.3/0.6MHz$	$22MHz$
Modulation type	GFSK	BPSK, QPSK	BPSK (+ ASK), O-QPSK	BPSK, QPSK, COFDM, CCK, M-QAM
Spreading	FHSS	DS-UWB, MB-OFDM	DSSS	DSSS, CCK, OFDM
Coexistence mechanism	Adaptive freq. hoping	Adaptive freq. hoping	Dynamic freq. selection	Dynamic freq. selection, transmit power control
Basic cell	Piconet	Piconet	Star	BSS
Extension of the basic cell	Scatternet	Peer-to-peer	clsuter tree, Mesh	ESS
Max number of cell nodes	8	8	>65000	2007
Encryption	Eo stream cipher	AES block cipher (CTR, counter mode)	AES block cipher (CTR, counter mode)	RC4 stream cypher (WEP), AES block sipher WPA2(802.11i)
Authentication	Shared secret	CBC-MAC(CCM)	CBC-MAC(CCM)	
Data protection	16-bit CRC	32-bit CRC	16-bit CRC	32-bit CRC

Table 2.1: Comparison of characteristics for different wireless protocols.

Looking closely to the last comparative table 2.1, adapted from [9] and having into account only the transmission rate of UWB and Wi-Fi technologies are by far the ones who got the best results. It is important to have a look in the spread spectrum techniques particularly in 2.4 GHz where Bluetooth, Zigbee and Wi-Fi coexist, which is an unlicensed band in most countries and known as industrial, scientific and medical band (ISM). Could exist some issues, specially when talking about the band of 2.4GHz, as said before. To help that Bluetooth protocol use an adaptive frequency to make possible to avoid collisions among other channels. Meanwhile Zigbee and Wi-Fi protocols use a dynamic selection of frequency and some power control.

It is also important to refer that the number of cell nodes of the network of Bluetooth are 8, Zigbee star network are over 65000 and 2007 for a structured network Wi-FI [9].

Talking about the transmission time, in [9], it should be referred that it depends on the data rate, message size and distance between two nodes. The formula of transmission time in equation 2.1 is given by,

$$T_x = (N_{data} + (\frac{N_{data}}{N_{maxPld}} * N_{ovhd}))T_{bit} + T_{rpop}, \tag{2.1}$$

where N_{data} is equal to the data size, N_{maxPld} is the maximum payload size, N_{ovhd} is the over head size, T_{bit} is related to the bit time while T_{prop} refers to the propagation time between two devices. Looking to table 2.2 we conclude that Zigbee has the lower data rate and UWB presents the best results when talking about data rate. Data Coding Efficiency, it refers to the ratio of data size with the message size (total number of bytes used to transmit data).

Standard	**Bluetooth**	**UWB**	**ZigBee**	**Wi-Fi**
IEE Spec.	802.15.1	802.15.3	802.15.4	802.11a/b/g
Max data rate(Mbit/s)	0.72	110	0.25	54
Bit Time(u s)	1.39	0.009	4	0.0185
Max data payload (bytes)	339 (DH5)	2044	102	2312
Max overhead (bytes)	158/8	42	31	58
Coding effciency	94.41	97.94	75.52	97.18

Table 2.2: Typical system parameters of the wireless protocols.

For small data size bluetooth presents the most favourable results, also noticing that Zigbee also has a good efficiency for this values of data size. When the core issue is big data sizes, UWB and Wi-FI has good results, shown in figure 2.2, based in [13]. Regarding the power consumption, in figure 2.3 it is possible to conclude that the bluetooth and Zigbee Technologies are quite good in Low Data Rate applications [13], as an example

Protocols	Transmitted Power (Watt)
Bluetooth	0.1
UWB	0.064
ZigBee	0.0063
Wi-Fi	1

Table 2.3: Transmitted power parameter of the wireless protocols.

limited power batteries. On the other side for High Data Rate, the UWB and Wi-Fi are the best solutions.

2.4 Ultra-Wideband

The Ultra Wideband technology has as main characteristic the transmission of short pulses with low energy, with a fractional bandwidth bigger than 20 % or a signal bandwidth bigger than 500 MHz. Taking into account Shannon's capacity formula, this amount of bandwidth offers a high capacity. The UWB transmitter produces a very short time-domain pulse which is able to propagate without the need for an additional radio frequency mixing stage. Saying in another words is a carrier-less radio technology which results in a much simpler and consequently cheaper compared to other radio frequency carrier systems. Mentioning as well that in this project an impulse radio UWB transceiver is used.

As said before UWB systems always had some disadvantages however all changed during the past years. In 2002 the Federal Communication Commissions recognised the significance of UWB technology and initiated the regulatory review process of the technology to make it possible to use it for commercial applications, there were a series of factors that by somehow had changed the opinion about impulse radio techniques, mainly:

- The radio frequency (radio frequency (RF)) spectrum is intensively used, making it difficult to get usable broad bandwidth;
- The need for ultra low-power RF communication links which have to be robust in harsh environments;
- Since the widespread of GPS it become important as well to adopt that to indoor environments;
- The silicon latest technologies permitted it to become a real project.

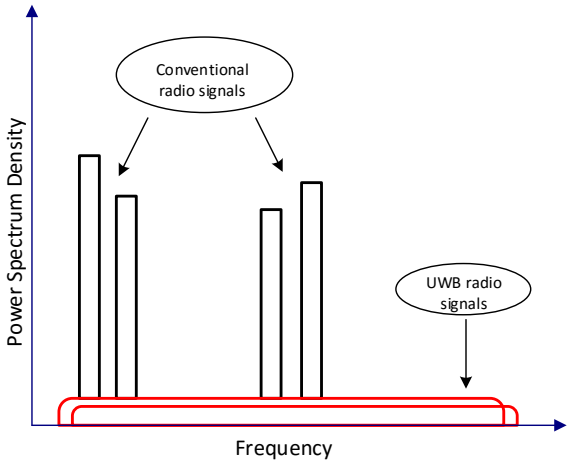

Figure 2.9: UWB Conventional.

In figure 2.9 based in [14] is the comparison of UWB and other conventional radio signals. It should not be forgotten that because of the enormous bandwidth of IR transceivers makes them more resistant to fading effects in severe environments and has a fine time resolution which makes it a technology appropriate for accurate ranging and since it has an enormous bandwidth, it has a good material penetration capability.

As said before, from [8], the signal is recognized as UWB if it has a bandwidth of,

$$BW \geq 500MHz, \tag{2.2}$$

Also according to the federal communications comission (FCC) UWB rulings, a signal can be classified as an UWB signal if the fractional bandwidth (B_f) is greater than 0.2 and is determined by,

$$B_f = \frac{f_H - f_L}{(f_H + f_L)/2}. \tag{2.3}$$

Also worth referring that by the Hartley-Shannon theorem,

$$C = B \cdot log_2(1 + SNR), \tag{2.4}$$

where C is the maximum capacity of the channel, B is the bandwidth and SNR is the relation between noise and signal. After giving a close look to this last expression it is possible to refer that the maximum capacity of the channel rises directly with the bandwidth and it is only affected logarithmic with the relation Noise-Signal, knowing that UWB bandwidth has values of frequency around 10^9, permits to obtain a channel capacity bigger and larger even working with a relatively low SNR, [15].

2.5 UWB Modulation Methods

A fundamental part is the modulation of the signal to send where the designer has a wide range of options. However exists a trade-off in UWB Modulation systems, this is related to the maximum transmit distance, the data rate, the transmission power and system complexity. The main data modulation schemes are PPM, PAM, PSK and OOK.

2.5.1 PAM

The basic principle for this modulation, figure 2.10 relies in sending the signal with different amplitudes corresponding to different data being transmitted and expressed by equation 2.5, from [16].

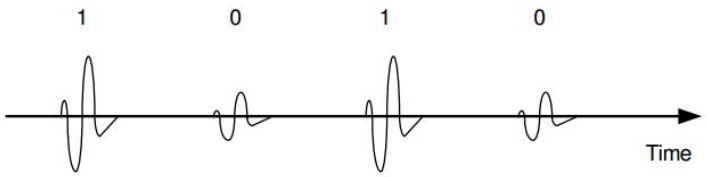

Figure 2.10: PAM modulation.

$$s(t) = \sum_{m=1}^{\infty} b_m * P(t - mT)) \tag{2.5}$$

This type of modulation presents low complexity once it just requires a single polarity to represent data and it depends on an energy detector to recover data, on the other hand, PAM is sensitive to noise and attenuation which can make 1 and 0 hard to distinguish.

2.5.2 OOK

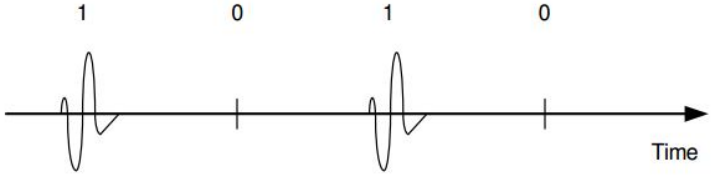

Figure 2.11: OOK modulation.

One of the most simple modulations, it represents a signal as the presence or absence of a waveform. In the simplest form whenever it is necessary to transmit a bit 1 a pulse is sent

while its absence represent bit 0 as showed in figure 2.11 and represented by equation 2.6, from [16].

$$s(t) = \sum_{m=1}^{\infty} b_m * P(t - mT)), \tag{2.6}$$

represented as $P(t)$ is an extremely narrow pulse, b_m refers to the bit information and T is the pulse period. This modulation was used in this project since it represents low complexity either in the modulation or in the demodulation however it is important to emphasize that this type of modulation has some drawbacks like being too sensible to noise and to interferences, causing a BER performance below the expectations.

2.5.3 PPM

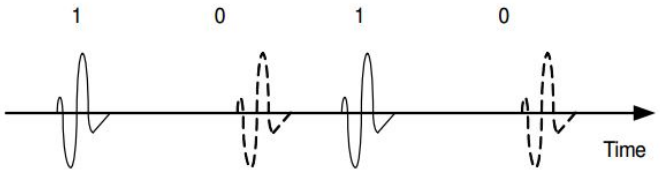

Figure 2.12: PPM modulation.

The PPM modulation, figure 2.12, [16], is based on the determination of the UWB pulse position, it is necessary to predefine a time window where the 1 bit can be represented by the original pulse and bit 0 by the translated pulse in time.

$$s(t) = \sum_{m=1}^{\infty} P(t - mT - b_m\delta)), \tag{2.7}$$

in equation 2.7, [16], $P(t)$ is an extremely narrow pulse, b_m represents the bit information and T is the pulse period and δ is a time delay, in this modulation the noise is significantly lower compared with the techniques mentioned before, however it comes with a price, it is vulnerable to collisions caused by multi-access channels and they are also much more complex to implement.

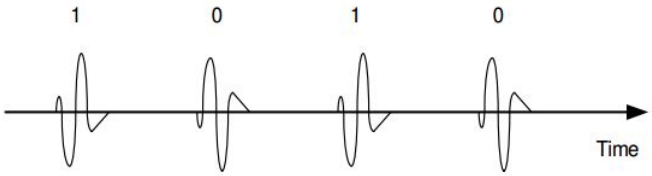

Figure 2.13: BPM modulation.

2.5.4 BPM

In the BPM modulation, [16], as shown in figure 2.13 to represent the information bits the pulse polarity is switched, in other words bit 1 has a positive polarity and bit 0 has a negative polarity.

$$s(t) = \sum_{m=1}^{\infty} b_m * P(t - mT \pm \delta) \tag{2.8}$$

As main advantage, it is less susceptible to distortion because the signal is detected by the polarity and just by looking to equation 2.8, demonstrated in [16], represents a higher complexity than in the first two techniques.

2.6 UWB Regulations

In order to minimize the interferences from UWB in other technologies, since it radiates electromagnetic energy in a large spectral band, the limits of maximum radiation level and the frequency bands of free licensed operation from UWB devices have as expected certain regulations that must be fulfilled, [17].

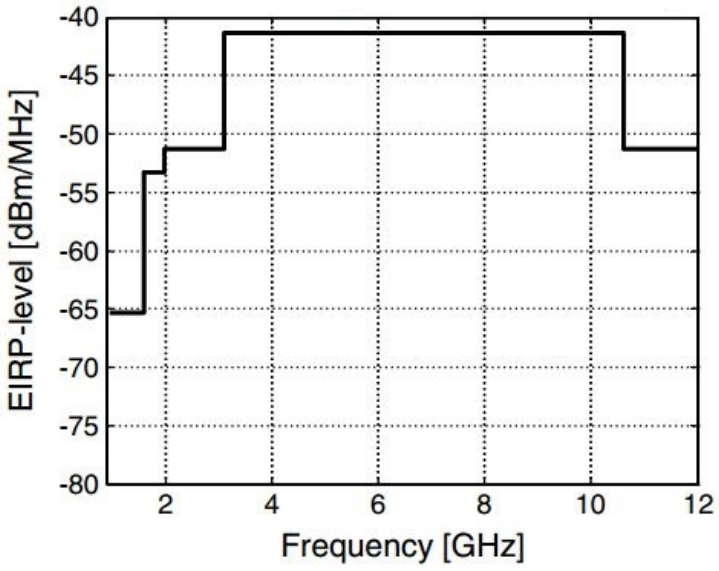

Figure 2.14: FCC-America.

The first regulation came from USA, introduced by the FCC as it is possible to see in figure 2.14 from [1], permitting a working frequency band between 3.1 to 10.6GHz for UWB radiation with a limit of power around -40dBm/MHz. To fit it for Europe utilization was necessary to modify these rules, which is a bit more restricted showed in figure 2.15, [1], comparing it with United state regulations. One of the main areas is the communication industry, the biggest supporter of UWB regulation, and it is expected an enormous market for high-data-rate in short range communication. It is important to refer that exists many different masks depending on the utilization for example for indoor and outdoor utilizations should be different, [17].

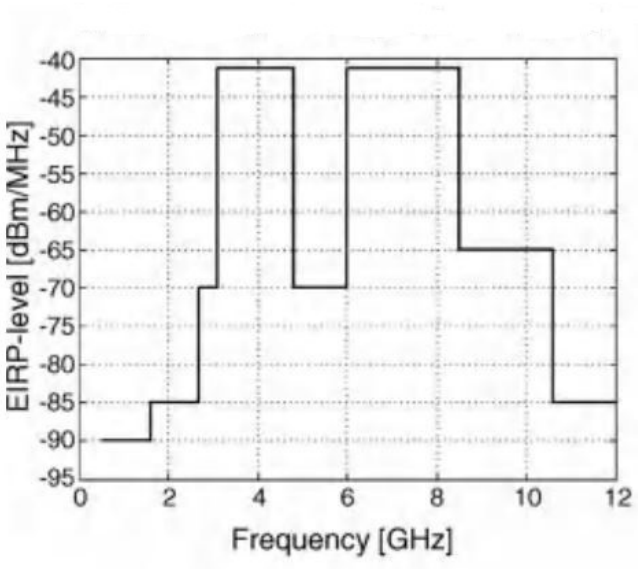

Figure 2.15: FCC-Europe.

2.7 Gaussian Pulse

It is truly important to maximize the radiated energy of the pulse, as long the spectral FCC mask is respected. In the UWB signal the spectrum in frequency domain depends on the waveform of the used pulse, where the main ones are rectangular, Gaussian doublet and mono-cycles. To satisfy the UWB emission constraint specified in FCC regulation the desired frequency spectrum of the mono-cycle wave form should be flat over a target bandwidth, [18]. Having as expression,

$$V(t, f_c, A) = A \cdot e^{-2(\pi t f_c)^2}. \tag{2.9}$$

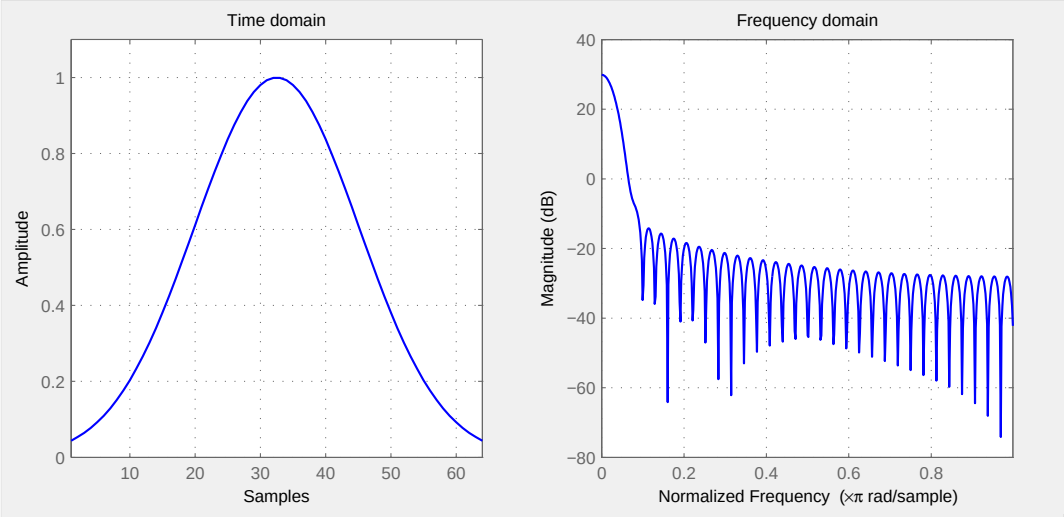

Figure 2.16: Gaussian pulse and frequency spectrum.

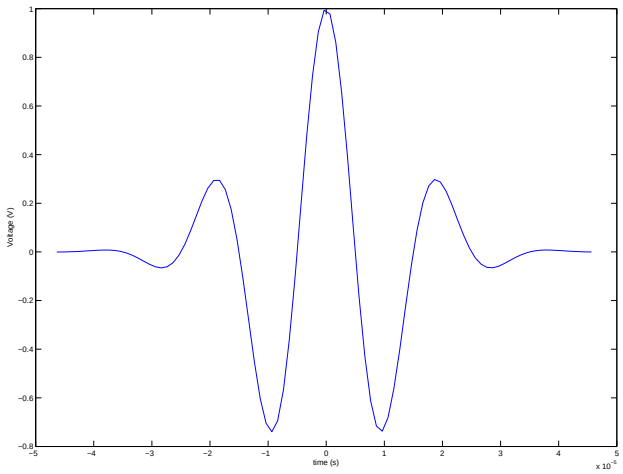

Figure 2.17: gaussian monocycle pulse.

In equation 2.9, where the value of A is the amplitude of the pulse and f_c is the centre frequency. In order to obtain the derivative of equation 2.9 it was used Matlab to simulate a gaussian pulse and to calculate it frequency spectrum, shown in figure 2.16.

$$V(t, f_c, A) = 2\sqrt{e} \cdot A \cdot \pi t f_c \cdot e^{-2(\pi t f_c)^2}, \tag{2.10}$$

equation 2.10 represents the gaussian monocycle pulse which is represented in figure 2.17. The central frequency is defined as $(\pi\tau_0)^{-1}$, where τ_0 is the time between the maximum and minimum pulse points.

2.8 UWB Transceivers

As everything in the area of technology has a trade-off, there are a vast number of topologies for the same purpose and this happens as well in UWB circuits. Focusing in the Low Data Rate transmission is shown in this chapter that exists three main topologies Differential Coherent System topology, Coherent System topology and giving special attention to the Non-Coherent system topology, which will be implemented in this project.

2.8.1 Coherent Systems

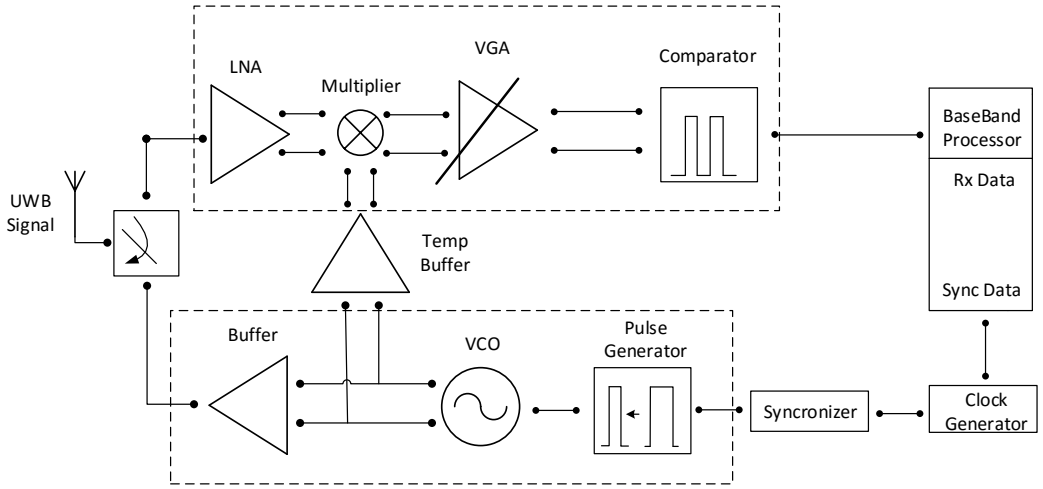

Figure 2.18: Coherent System.

From the different UWB systems available, the one with better results up to this date is the coherent, it presents a superior BER outcome with long range. However it is a complex architecture and as a result bigger current consumptions, this issue happens because it is necessary to estimate the channel with high precision and an almost perfect synchronization with each correlator. In figure 2.18, [19], illustrates the overall architecture of a coherent IR-UWB transceiver.

In the transmitter, the data signal from baseband is the input of the digital pulse generator which converts in short pulses. The short pulse makes the LC voltage-controlled oscillator (VCO) turn ON/OFF, and finally the modulated UWB pulse is transmitted through the differential buffer amplifier and to the antenna. While in the receiver, the UWB signal is amplified at the low noise amplifier (LNA) stage, the amplified signal is demodulated with the template signal in the multiplier. Therefore the demodulated pulse envelope signal is filtered by the following low pass filter, and is amplified adaptively in the VGA stage to achieve the sufficiently dynamic range. Finally, the comparator makes

the digital output pulse data whenever the magnitude of signal exceeds the controllable threshold voltage level.

2.8.2 Differential Coherent Systems

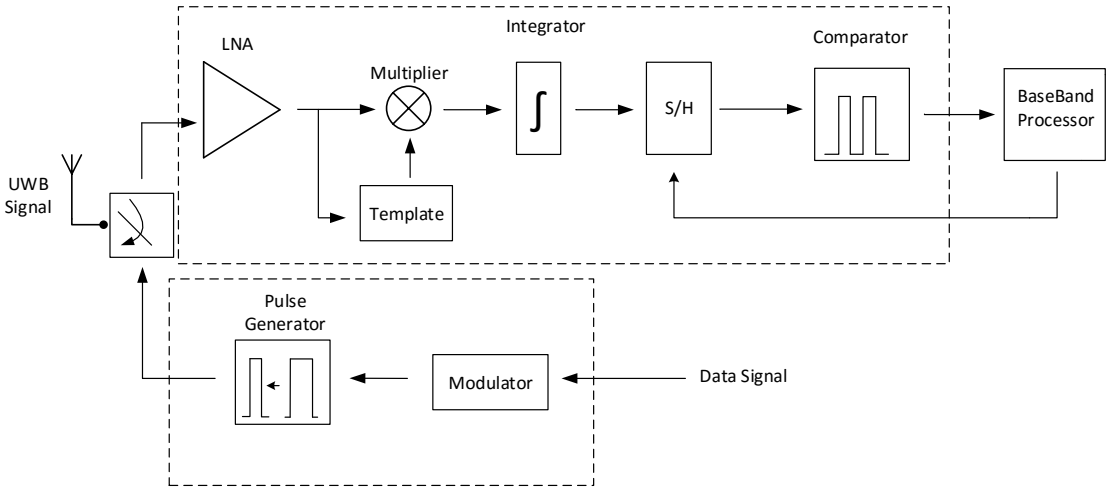

Figure 2.19: Differential Coherent System.

The second transceiver system shown in figure 2.19, [19], uses a modulation scheme of transmitted reference also known as Differential coherent. Where a transmitted reference communications system transmits two versions of a wideband carrier, one modulated by data and the other unmodulated. Typically both, modulated and unmodulated versions are separated from one another either in time or in frequency.

For the receiver , in order to capture the signal and the delayed signal, different in phase, a fully digital architectures converts the RF signal immediately after the LNA amplification and then performs a digital correlation and decision. The digital scheme is relatively simple to implement however the A/D converter requires a high sampling rate in order to meet the Nyquist criterion.

CHAPTER 3

DESIGN OF THE PROPOSED UWB TRANSCEIVER

This chapter introduces the proposed UWB transceiver, considering the information given in the previous chapter where alternatives for non-coherent transceiver were analysed.

One of the first choices to make is to determine which modulation type presents the best robustness and flexibility results, for a proper wireless connection. To achieve all these characteristics exists the Non-Coherent transceivers, based in [20], characterised for having a low cost and low energy consumption once it does not need to do an estimation of the transmitted channel. However as main disadvantages it has low performance of BER, once the signal is detected through it energy, as a result comparing with other techniques it turns to be really sensible to noise, to interferences and to multipath effects.

3.1 Transceiver Architecture

The proposed transceiver architecture is represented, in figure 3.1, [20]. The simplicity of this architecture relies on the principle of energy detection of a IR-UWB stream. In the receiver, the UWB pulse is captured by the receptor antenna and amplified by the LNA. After amplifying, the signal is squared, by means of a gilbert based mixer cell. To improve the overall SNR, an integrator is included before the comparator, which is responsible for recovering the data stream.

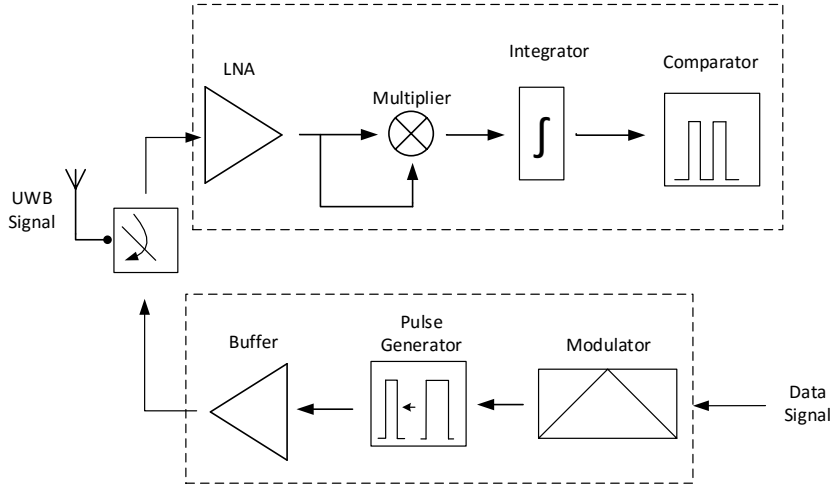

Figure 3.1: UWB Non-coherent transceiver.

3.2 Transmitter

3.2.1 Modulator, Pulse Generator and Driver Amplifier

The transmitter is composed by a modulator, a pulse generator and a driver amplifier. For the design of an UWB system is crucial to select the modulation type, since it will have a direct impact in the transceiver complexity, the data rate, bit error rate (BER) and robustness against interferences, [21]. For this thesis the ON/OFF keying modulation is the most appropriate once it is the one that best fulfill the demands of IoT systems. The block scheme of the OOK modulation, is shown in figure 3.2

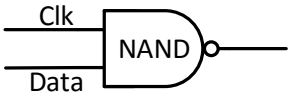

Figure 3.2: ON OFF Keying modulation.

After having the signal modulated it will be generated a short pulse in which will be sent through the antenna, creating a gaussian pulse. Therefore, the modulated signal will be sent to the input of the pulse generator, figure 3.3, in which every time the data goes low appears a positive pulse at the output, figure 3.3, where it exists a delay carried out by the inverter chain as a result only in case of having both inputs with low value, 0, that will result in a pulse, having a width determined by the inverters gain delay.

In figure 3.4 is shown a simplification of the waveforms expected through transmitter signal path [22], starting from the data that is meant to be sent, the clock of the transmitter that will determine the number of pulses to be sent, the signal modulated with a OOK modulation technique and, the last one, is the signal after the pulse generator.

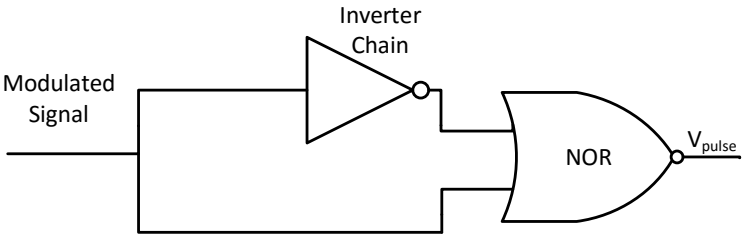

Figure 3.3: Scheme of Pulse Generator.

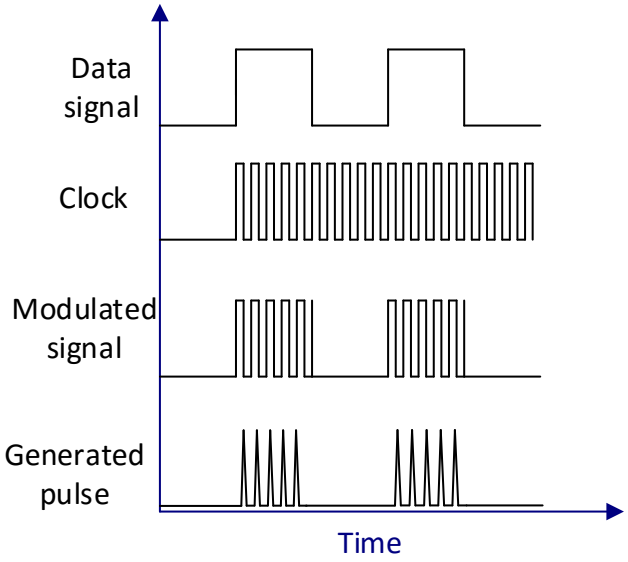

Figure 3.4: Signal waveforms through different blocks of the transmitter.

The driver amplifier is the last circuit of the transmitter just before the antenna which it is used to amplify and shape the modulated pulse signal into regulated spectrum mask and it is responsible for the matching the block with the dipole antenna.

One of the most basic topologies of a wideband power amplifier is the Class A RF, in figure 3.5 from [23], it is based in a single transistor with a parallel-resonant circuit LC, a RF choke L_f and a coupling capacitor L_e, which will have as operating point the active region and the transistor M_1 works as a voltage-controlled dependent current source. For this case a wideband characteristic is expected, there is no need of filters.

Once the class A has the highest conduction angle of all linear amplifiers it results in a lower efficiency around 25%, it can be written as,

$$\eta_D = \frac{P_{out}}{P_{DC}} = \frac{1}{2} \cdot (\frac{V_{out}}{V_{DC}})^2. \tag{3.1}$$

Where V_{out} is the output voltage value. Concluding, 50% of efficiency is the maximum level for a $V_{out} = V_{DC}$ of maximum output swing.

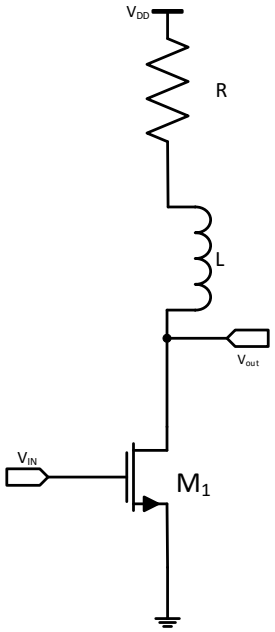

Figure 3.5: Signal waveforms through different blocks of the transmitter.

3.2.2 Antenna

As it is said by definition an antenna is meant for "radiating or receiving radio waves", [24]. It converts signals from a transmission line to electromagnetic waves to broadcast it and in the receiver antenna converts back into electrical signals.

There are some parameters that should be taken into account to elect the most appropriate antenna, including directivity, gain, input impedance, frequency pattern and antenna size.

Frequency Bandwidth

Frequency Bandwidth is the parameter that represents the range of frequencies.

As mentioned before a wideband system has an antenna characterised for having an absolute bandwidth value (ABW) greater than 500 MHz or a fractional bandwidth (FBW) greater than 20 %.

Radiation Pattern

Radiation Pattern describes as the name indicates the representation of the radiation properties of the antenna, normally the pattern characterises the power levels.

Directivity and Gain

From figure 3.6, [24], is the description of a generic antenna where R_r, R_C, L and C represents the radiation resistance, loss resistance, inductor and capacitor, respectively.

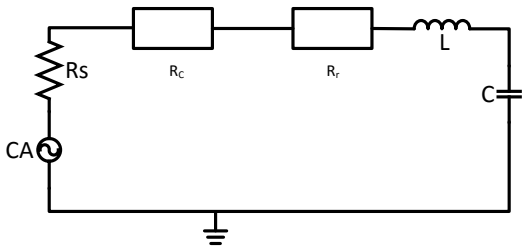

Figure 3.6: Generic electric circuit of an antenna.

Looking to [25], the radiation efficiency can be described by,

$$e_{rad} = \frac{R_r}{R_r + R_C}. \tag{3.2}$$

The maximum gain G_o is directly related to radiation efficiency and maximum directivity D_o in,

$$G_o = e_{rad} \cdot D_o. \tag{3.3}$$

UWB antennas should have as main characteristic an absolute bandwidth no less than $500MHz$ or a fractional bandwidth at least 20%. UWB antennas requires a consistent behaviour over the entire operational bandwidth, it should be directional or omnidirectional depending on their functionality, another important feature is it scale once it will have an application in mobile phones or in any other small devices and the UWB antenna should have a good time domain performance with minimum pulse distortion in the received waveform.

The most common on-chip antennas in UWB systems are the dipole antennas, monopole antennas and loop antennas.

Loop Antennas

Loop antennas, as the name indicates these type of antennas are characterised for having a single rounded element.

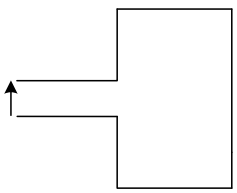

Figure 3.7: Simplified scheme of Loop antenna.

In figure 3.7, based in [26], shows a loop antenna which leads to a considerable area occupied, however it is compensated with an higher gain.

Monopole Antennas

These antennas are the simplest topology, it is based in a single element fixed on ground plane. With this characteristic the ground plane become a mirror image of the element above the ground, which will act as it was a dipole antenna figure 3.8 based in [26].

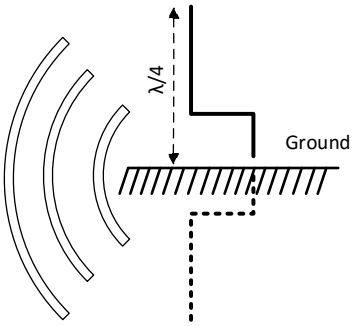

Figure 3.8: Simplified scheme of monopole antenna.

Having half of the length of a dipole $\lambda/4$, and an inferior performance compared with the other topologies, to better describe the it there is the expression of the gain from [25] and expressed by,

$$G = 4 \cdot \pi \frac{A_e}{\lambda}, \tag{3.4}$$

where λ is the wavelength and A_e is the aperture area of the antenna.

Dipole Antennas

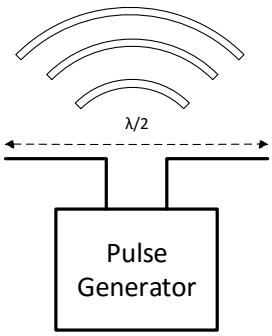

Figure 3.9: Simplified scheme of dipole antenna.

Looking to the available antennas and having in consideration all the trade-offs, for example the size, the complexity and power consumption the chosen one was the electric dipole antenna, a simple diagram is shown figure 3.9, [26].

3.3 Receiver

The receiver of the proposed non-coherent IR-UWB system, looking to figure 3.1 is characterised for having a large gain and low noise figure (NF) LNA, in order to achieve this features a great effort was needed to make. Once as referred before it presents an absolute bandwidth of 500 MHz with a centre frequency of 4.5 GHz turning it in a great challenge to obtain a good performance. This block will contribute for a lower noise contribution from the next stage, making a lower NF receiver and resulting in higher sensitivity and data rate, which are crucial characteristics. The next wideband IF blocks consist in a squarer, an amplifier and at the end a 1 bit ADC, which it is based in a comparator, implemented with a simple differential pair and a regenerated latch.

3.3.1 Low Noise Amplifier

The first circuit of the IR-UWB receiver is the Low Noise Amplifier (LNA). To achieve these goals it is essential that the input impedance matches the antenna characteristic impedance in order to maximize the power transfer. It is important to note that in the LNA circuit should be achieved the minimum noise as possible in the system and naturally having in consideration the gain and the Noise Ratio.

One of the main requirements to choose a proper topology for this IR-UWB system, it must have an high bandwidth and the input impedance needs to match the antenna impedance for the LNA Working band, for these desirable requirements exists several topologies however for a high frequency of work, around 4.5 GHz, there are few with the simplicity and efficiency of the Wideband Cascode Balun-LNA which is based in two simple topologies the Common Gate and the common source.

The Common Source is a strong candidate for a Low Noise Amplifier figure 3.10 from [27], once it is one of the simplest way to match the input, using R_{IN} as a resistance that will provide a more stable input through the working band of the LNA. However as a simple amplifier it turns to have a considerable value of Noise Factor.

It should be mentioned as well, that resistance is in parallel with the gate of the transistor, it is important to refer the motive for the use of this resistor since the input impedance transistor is infinite one of the ways to match it is with a resistor in parallel and Z_L impedance represents a wideband configuration.

Nevertheless, it is essential to refer that the resistor introduces a significant quantity of noise to the overall system. As a result the expression of the Noise Factor of the entire Common Source, there is in equation 3.5, with G_A as the power gain available, the Noise power in the output P_N, source impedance from the antenna which is matched with "R_{IN},

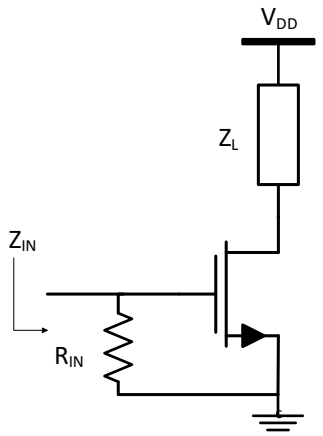

Figure 3.10: Common Source LNA.

looking close to the next equation we can conclude that the minimum value of noise is 2 dB, which only ideally can be achieved, with this simple LNA, demonstrated in [27] and expressed by,

$$F = \frac{4KTR_SG_A + 4KTR_{IN}G_A + P_N}{4KTR_SG_A} = 2 + \frac{P_N}{4KTR_{IN}G_A} \tag{3.5}$$

Another possibility for the LNA is the Common Gate LNA, is shown in figure 3.11 based in [27], at it simplest form, it is the topology more used in the wideband LNA, this happens because it presents an intrinsic wideband response. In order to achieve a 50 Ω (antenna impedance), the transconductance gain, g_m, of the common gate will need to be equal to $g_m = \frac{1}{R_S} = 20\ ms$, this only can be verified if the channel length modulation and body effect are ignored.

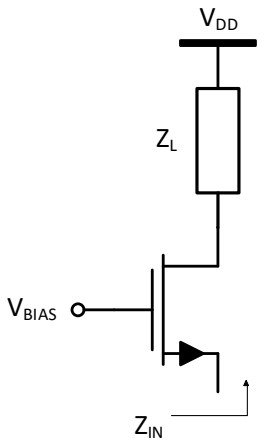

Figure 3.11: Common Gate LNA.

Referring only to thermal noise [22] , where N_o and N_i are the power noise at the input

and output of the LNA, the minimum noise factor can be easily obtained,

$$F = \frac{N_o}{N_i G_A} \tag{3.6}$$

Having $N_i = \overline{I_S^2}$ and $N_o = (\overline{I_S^2} + \overline{I_d^2})\dot{G}_A$

$$F = \frac{(\overline{I_S^2} + \overline{I_d^2})G_A}{\overline{I_S^2 G_A}} = 1 + \frac{\overline{I_d^2}}{\overline{I_S^2}} \tag{3.7}$$

Knowing that $\overline{I_S^2} = 4KT\gamma g_m$ from [22] as well as $\overline{I_d^2} = 4KTg_m$, which is the medium value for the thermal noise. The Noise Figure is given by,

$$F = 1 + \frac{4KT\gamma g_m}{4KTg_m} = 1 + \gamma, \tag{3.8}$$

Considering the use of long channel transistors, the constant γ has a value of $2/3$, while the minimum value of noise factor from a common gate amplifier is equal to $5/3$, around 2.2 in dB which is lower than the common source topology. One of the main disadvantages is the need of resizing the g_m in order to match the input impedance, so it is mandatory to increase Z_L, once it is directly proportional with the gain of the amplifier which results in a higher NF, normally greater than 3 dB. In order to overcome this values of Noise Factor a possibility is by somehow combine both topologies using a noise cancellation principle.

3.3.2 Self Mixer

In the RF front-end systems, specially in a non-coherent where it has a goal of being as simple as possible results in the necessity of a self-mixer, the block responsible for the square of the signal resulting in translation of the frequency RF signal to an Intermediate frequency, called up-conversion or the opposite down-conversion since it transfers the frequency to the baseband. In an ideal world it is a simple calculus, just a multiplication. However different frequencies are expected from the sum and difference of the two signals that are in the two inputs, showed in figure 3.12. From the different mixer topologies it was decided for a active mixer, in figure 3.13.

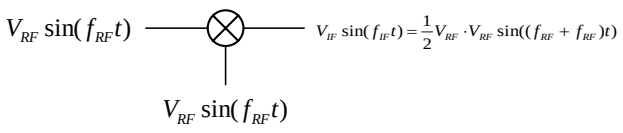

Figure 3.12: Self Mixer frequency sum.

Unfortunately the mixer, based in CMOS technology, is a non-linear circuit as a consequence higher order effects will appear in the result of the sum of the frequencies. Assuming for now that the mixer does not have a non-linear characteristic, from [28], the

expected output is:

$$V_{RF} = 1/2 V_{LO} V_{IF} cos((f_{IF} + f_{LO})t). \tag{3.9}$$

And as a real component it has a gain, based in the division of two inputs IF and LO, equal to,

$$A = 20 \cdot log(\frac{V_{LO} V_{IF}}{V_{IF}}) = 20log(\frac{V_{LO}}{2}). \tag{3.10}$$

As it was said before the mixer is a non-linear system. As a consequence it will appear other unwanted frequencies, which subsequently results in a different value of the final gain which can be lower or higher.

$$A = 20log(\frac{V_{LO} A}{2}) \tag{3.11}$$

So the conversion gain, in equation 3.11 with all the undesired frequencies summed up as A, demonstrating how efficient the global mixer is, if the mixer has value of conversion gain greater than 1 dB it is considered active otherwise a passive mixer. The mixer will have it noise energy lower or higher than the translated signal. In other words, every noise from sources will be translated and replicated however it has the benefit of being wideband which result in an aliasing effect. For the self-mixing process of the receiving signal it is used a wideband Gilbert Cell which is based in the single balanced mixer , therefore having a close look to the single balanced mixer which is an active topology it has the purpose of multiplying the signals in the current domain.

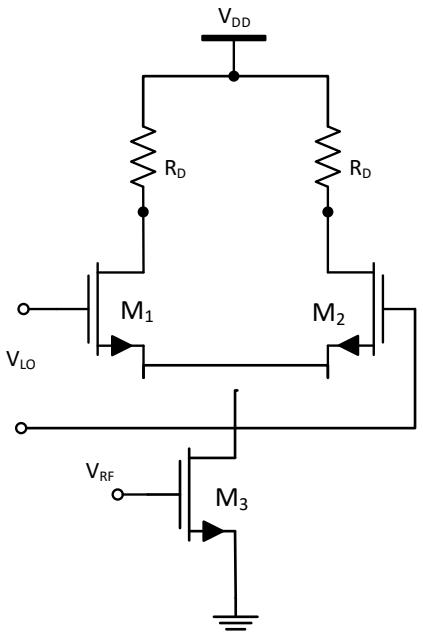

Figure 3.13: Single Balanced Mixer.

Looking to figure 3.13, it is possible to notice that the single balanced mixer is based on a simple differential pair and since one of the easiest ways to obtain the desired mixing

is with a switch. It works basically by using a differential pair, by this it is meant that the pair commutes the current flow between it branches, a switching behaviour is acquired and a mixing effect can be achieved.

A switching behaviour is achieved when a large signal, that represents the input of the mixer, M_1 and M_2 are in the saturation region, which means that when the switch is closed the impedance is low on the other hand when opened the impedance is infinite, in the transistor can work as a current buffer relatively to the current signal injected.

With all these conditions, the transistor's bias point vary with the same period in time and the current that flows in each branch depends on the differential voltage as well as in the bias current (I_{SS}). Knowing that in figure 3.13, V_D is the differential input voltage, with a phase shift of 180, $I_{B_{1,2}}$ is the drain current and v_{OD} is the differential voltage. Considering both transistors with the same size and neglecting body effect, the output currents are given by,

$$I_{B_1} = K \cdot (V_{gs_1} - V_{th_1})^2 \tag{3.12}$$

$$I_{B_2} = K \cdot (V_{gs_2} - V_{th_2})^2 \tag{3.13}$$

Considering as well ideal current sources,

$$V_D = (V_{gs_1} - V_{gs_2}) = \sqrt{\frac{I_{D_1}}{k}} - \sqrt{\frac{I_{D_2}}{k}} \tag{3.14}$$

with,

$$I_{SS} = I_{B_2} + I_{B_1} \tag{3.15}$$

which means that,

$$I_{B_2} = I_{B_1} = \frac{I_{SS}}{2} + \sqrt{k} - v_D \cdot \sqrt{\frac{I_{SS}}{2} - \frac{k}{4}\dot{v}_D^2} \tag{3.16}$$

Having k as the mobility constant in the DC point, which is equal to:

$$k = \frac{I_{SS}}{2(V_{GS} - V_{TH})^2} \tag{3.17}$$

$$I_{D_1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2} \cdot \frac{v_D}{(V_{VGS} - V_T)^2} \sqrt{1 - \frac{1}{4} \cdot (\frac{v_D}{V_{GS} - V_T})^2} \tag{3.18}$$

Looking to the small signal of one common source is obtained the gain of the differential pair, in equation 3.19 since the outputs are in phase opposition, we have in equation 3.20.

$$v_{oD} = v_{o1} - v_{o2} = v_1 \cdot g_m R_D + v_2 \cdot g_m R_D = -g_m R_D (v_1 - v_2) \tag{3.19}$$

$$A_{dP} = -2 \cdot g_m \cdot R_D \tag{3.20}$$

3.3.3 Integrator

The third block of the receiver, dimensioned in this thesis, is an integrator responsible for enhancing the signal strength of the receiving chain, where based in an energy detector working as an accumulator of pulses in order to obtain the exact quantity for bit 1 and 0. So in order to get a better SNR value it is implemented an amplifier buffer in a fully differential integrator topology where the reset of integration (accumulation of pulses) is completed by a CMOS transistor working as a switch, which will turn on in 10 pulses received in other words with a periodicity of figure 3.14. Ideally the transfer function of an integrator is given by,

$$H(s) = \frac{1}{sC}. \tag{3.21}$$

Where C is the value for the capacitance of each differential mesh.

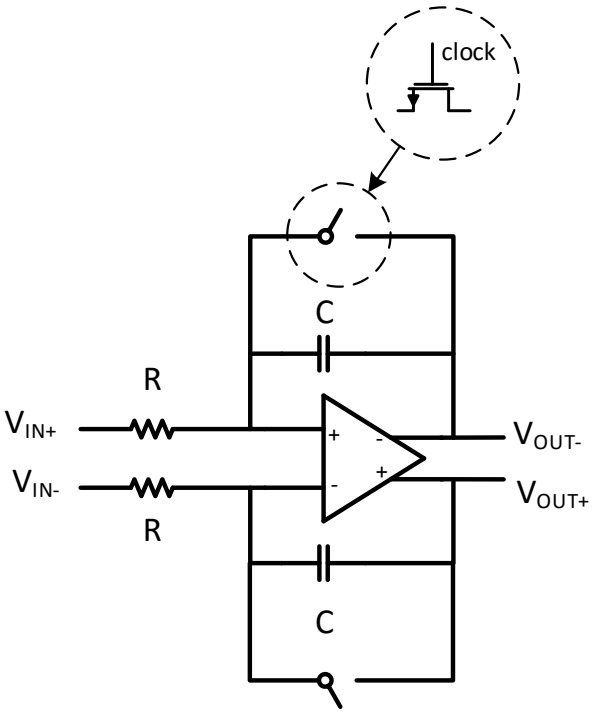

Figure 3.14: Differential integrator.

In order to achieve low power consumption with low voltage it is used a rail-to-rail input/output operational amplifier. As it is expected, the amplifier is designed to work with a big input common mode voltage (V_{icm}) range, which will maximize the SNR value of the amplifier, it is important to take a close look to the bandwidth, the phase margin, gain, power consumption.

3.3.4 Comparator and Latch

The last part of the transceiver system is divided in two circuits, the comparator and the NAND SR Latch, [29].

The comparator is used to detect a energy signal, by simply using as inputs the data signal and a reference voltage, if the data signal voltage is higher than the threshold voltage it will lead to a high value, "1". It is responsible for the demodulation of the received signal (ADC), one of the main characteristics that the block should have is a high speed response with low power in the minimum area possible. These features are not easy to achieve once the available supply voltage is relatively low, which result in the need of larger transistors subsequently more die area and power needed, so that the requirements will be granted. The comparator is based in a strong-arm latch which is used because of it high sensitivity and low circuit complexity, it is also important to refer that it consumes zero static power, directly produces rail-to-rail output swing and as well high input impedance.

The SR NAND Latch is used in order, in the output of the comparator, to obtain the final output equivalent to the data that was meant to be sent.

The SR NAND Latch, in figure 3.15, is used after the comparator to provide a system output equivalent to the data that is meant to be sent. The latch is one of the simplest circuits of memory elements. It is based in two cross-coupled logic inverters, these logic elements arrange a positive feedback loop, having a number of two stable operating points, the low value is "0" and the high value is "1".

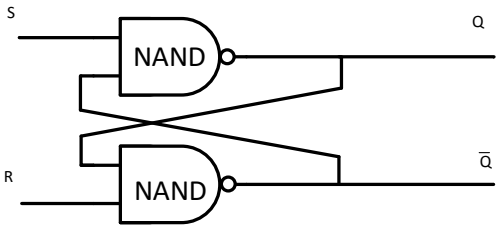

Figure 3.15: SR NAND Latch.

For the UWB system presented in this thesis and in order to trigger the states of the latch it is used the SR flip flop type, in particular using as a latch two NAND logic gates, in cross-couple connection. It is widely known that the two inputs are considered as S (set) and R (reset). The outputs are Q, for low value and $\overline{Q}$ for high value. When the user does not want to change the state, memory state, the two inputs must be high. It is necessary to refer that if both S and R are changed to 0 at the same moment, both NAND gates will origin in a value of "1" in both outputs, Q and $\overline{Q}$, which is incorrect since we cannot have at the same instant of time in the two outputs the same value. Hypothetically if both inputs return to "1", the sate of the circuit will be undefined, which it is normally avoided to use this input combination. In the table 3.1 is the truth table of the SR NAND Latch.

Table 3.1: SR NAND Latch truth table

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	-

CHAPTER 4

ELECTRICAL SIMULATIONS OF THE PROPOSED TRANSCEIVER

This chapter introduces the electrical simulations of the proposed IR-UWB transceiver, shown in figure 4.1. The transceiver has been described in a CMOS 130 nm technology.

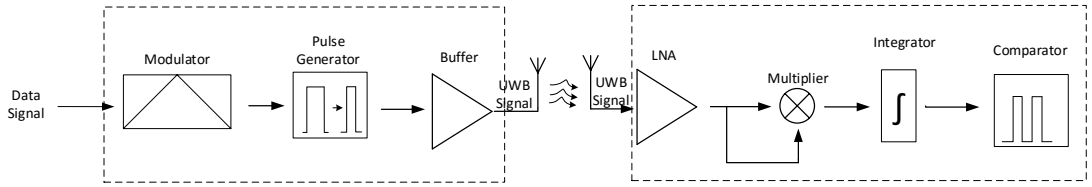

Figure 4.1: Complete transceiver architecture.

4.1 Transmitter

4.1.1 Modulator and Pulse Generator

The modulator block has as inputs the clock signal and a control signal and using them with the OOK binary technique, it modulates the data signal which will be used in the pulse generator, [30].

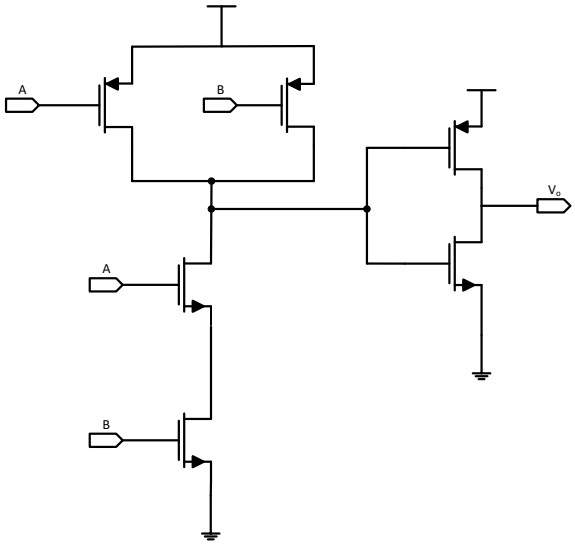

Figure 4.2: NAND logic gate.

Table 4.1: Truth table of NAND logic gate.

A	B	S
0	0	1
0	1	1
1	0	1
1	1	0

The signal modulator OOK designed, is a simple NAND logic gate, in table 4.1 there is the logic table for the NAND and in figure 4.2 from [31] , whenever exists a control signal the NAND will produce the same pulse with a frequency equal to the clock rate signal.

Once the digital sequence that represents the analog signal is defined the pulse generator block is designed, in figure 4.3 that will represent the bit sequence and once introduced in the antenna they will origin UWB pulses, [32]. The pulses are the result of delays made by logic operations that constitute the generator. The signal once introduced in the generator input it is submitted to a chain of inverters to perform a delay in the signal, to be worked in the NOR, in table 4.2 is the truth logic table of a NOR, with the original signal as well. Varying the value of the delay , it is possible to create pulses with higher or lower period which will be reflected later in the bandwidth occupied by the Gaussian pulses.

Table 4.2: Truth table of NOR logic gate.

A	B	S
0	0	0
0	1	0
1	0	0
1	1	1

When there is two low signals at the inputs of the NOR logic gate it will produce a logic

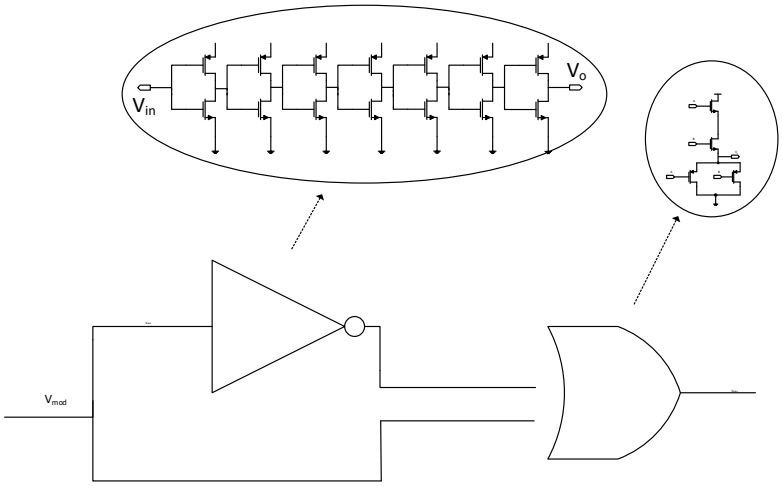

Figure 4.3: Pulse generator.

pulse. The length of the pulse is defined by the period of time in which both input signals are at low state, as mentioned before is programmed by the delay chain of inverters.

Simulation

In order to prove the veracity of the blocks responsible for modulation and pulse generation they were simulated having a supply voltage of $V_{DD} = 1.2V$, transistors with a minimum length and maximum width to guarantee a quick response, permitted by the 130 nm CMOS technology which is 120 nm for the L and a W of 115.2 μm

In figure 4.4 is shown waveforms of the two first blocks of the transmitter, the first signal is the the data meant to be sent, the second one is the modulated signal, with OOK modulation using a NAND port logic as said before and using a clock signal with 10 KHz that will work as carrier. The last is the pulse already generated with a signal period of 4 ns that in frequency is around 4.5 GHz.

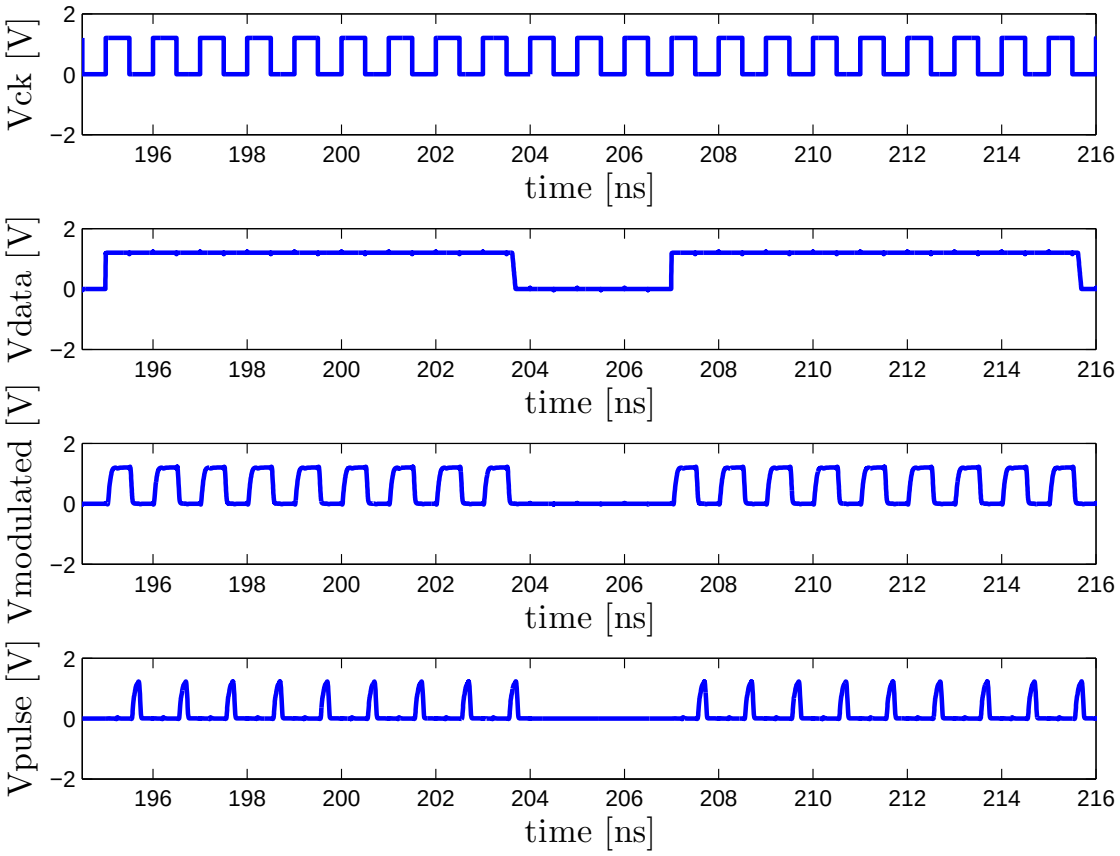

Figure 4.4: Modulator and Pulse Generator.

4.1.2 Driver Amplifier

The driver amplifier, [30], has the role of driving the signal to an antenna with 50 Ω of impedance, this block is constituted by two stages. The first one is composed by a common source cascode and a common gate with inductive degeneration, while the second stage is a source follower, as it is possible to see in figure 4.5. Through the model of small signals the voltage gain is given by:

$$A_v = \frac{-g_m Z_L}{1 + g_m Z_S} \tag{4.1}$$

Having the transistor M1 biased in the linear region it means that the current is described by:

$$i_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{4.2}$$

Whenever the V_{DS} is significantly small, the second order term will disappear, concluding we obtain a linear function and we can put in order of r_{DS}:

$$r_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}} \tag{4.3}$$

The Common gate transistor M_2 is designed to work as a resistance, which means it will work in the linear region, that could be controlled by varying the bias voltage from M_2 transistor.

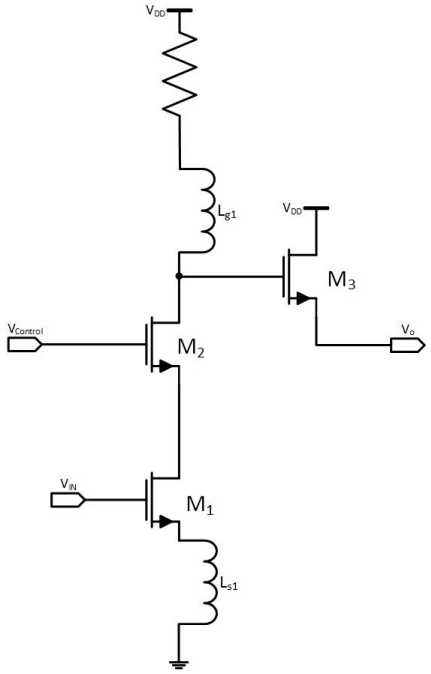

Figure 4.5: Driver Amplifier.

The gain of M2 (linear region) obtained by analysing the small signals at high frequency is,

$$A_V = \frac{-g_m Z_L - g_m r_{DS}}{1 + g_m Z_S} \tag{4.4}$$

substituting r_{DS} by its expression

$$A_V = \frac{-g_m Z_L - g_m \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}}{1 + g_m Z_S} \tag{4.5}$$

The source follower it is a simple Common drain transistor in saturation region, so that the signal input will be able to pass through the transistor gate.

Table 4.3: Driver Amplifier parameters.

Transistor	$W(\mu m)$	$L(\mu m)$	*Region*	$I_D(mA)$	$V_{DSat}(mV)$	$g_m(mS)$
M_1	64	0.12	active	1	83.6	8
M_2	64	0.12	active	1	80.7	4
M_3	115.2	0.12	active	2	84.6	34.6

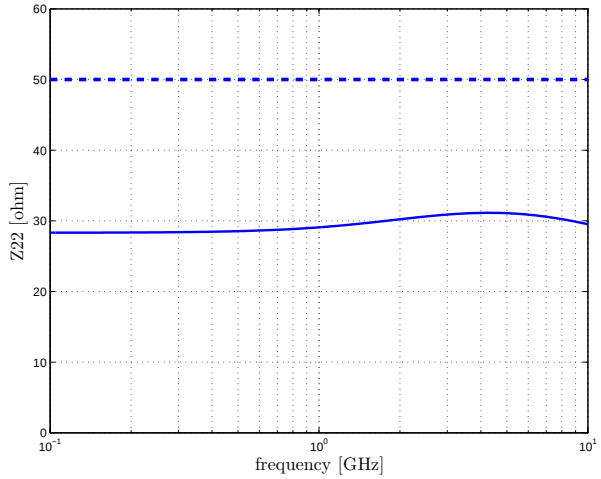

Figure 4.6: Output impedance.

Simulation

To verify the Driver amplifier equations that were studied few simulations were made having in consideration the circuit limitations as it was showed before with a supply voltage of 1.2 V table 4.3 shows the main parameters of the transistors, their dimensions and DC operating, that form the driver amplifier (DA).

The output impedance is not the ideal value but still good enough to obtain a decent signal, in figure 4.6 is the impedance with a value of 33 Ω for the desired bandwidth.

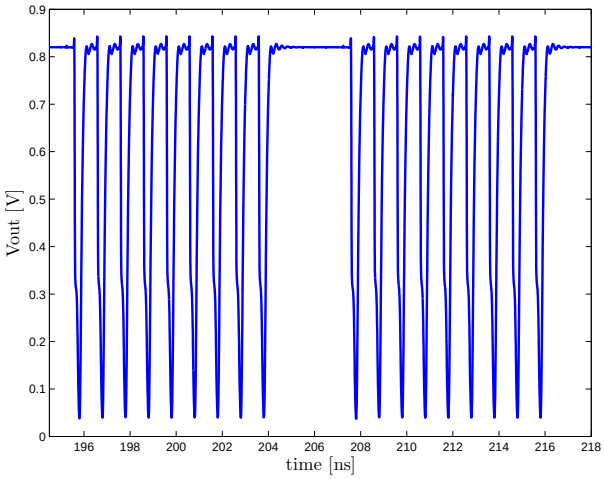

Figure 4.7: Waveform output of Driver Amplifier.

The signal after having the output matched with a value of 50 Ω in figure 4.7 it has maximum peak approximately in 1.2 V with a duration of 5 ns since this is the designed pulse, it is not rectangular.

4.2 Antenna

As for the transmitter antenna as for the receiver antenna, which have the same architecture and values was done the proper design and simulation in the ADS environment where was taken special attention to the spectral power density. As mentioned before dipole antenna is far from perfect, however it has as advantages low consumption and simplicity, which turn it one of the best for UWB signal transmission. To validate this type of antenna it is necessary to match the antenna by knowing previously the desired frequency for transmission, [33]. To design the dipole antenna it was used an electric circuit.

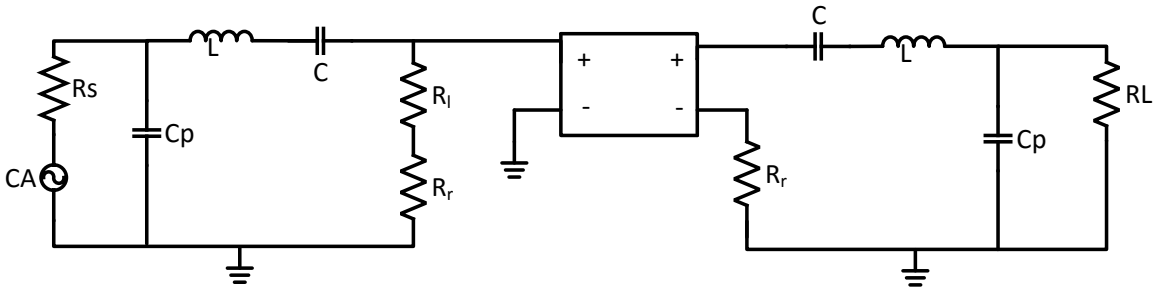

Figure 4.8: Dipole antenna.

As shown in figure 4.8, the antenna is described as a circuit with passive elements, [34]. The resonance series composed by C_1 and L_1 describes the antenna behaviour, R_1 is the resistor that represents the radiation resistance which simulates the antenna radiation. The signal that was chosen to be transmitted has a centre frequency around 4.5 GHz, all the calculation of the passive elements were made to replicate the behaviour of a dipole antenna of $\lambda/2$ length. To theoretically describe the wavelength of the signal, in equation 4.6, which consists in the relation between the light speed in vacuum with the signal frequency as it is explained in [35] and showed as,

$$\lambda = \frac{c}{f} \tag{4.6}$$

$$\lambda = \frac{300.000.000 m.s^{-1}}{4.000.000.000 s^{-1}} = 0.075 m \tag{4.7}$$

Using equations of the resonant frequency of the antenna and using the quality factor Q.

$$f_0 = \frac{w_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} \tag{4.8}$$

$$Q = \frac{w_0 L}{R_r + R_l} = \frac{1}{R_r + R_l}\sqrt{\frac{L}{C}} \tag{4.9}$$

From 4.6 to4.9 permits to calculate the value of the resonant series, which are dependent from resonant frequency and to the value of quality factor. It was assumed for the quality factor a value of 5, for the resonant frequency 4.5 GHz, for the loss resistances $R_l = 2\Omega$ and for the radiation resistance $R_r = 73\ \Omega$, so resulting in,

$$C = \frac{1}{2\pi f_0 \cdot Q(R_r + R_l)} = \frac{1}{2\pi \cdot 4.5 \cdot 10^9 \cdot 5 \cdot (73+2)} = 106.103 fF \tag{4.10}$$

$$L = \frac{Q(R_r + R_l)}{2\pi f_0} = \frac{5 \cdot (73+2)}{2\pi \cdot 4.5 \cdot 10^9} = 14.92 nH \tag{4.11}$$

Simulation

Looking to the antenna behaviour, after injecting a pulse signal, it is possible to observe in figure 4.9, with $T = 0.25\ ns$ which in frequency results in a centre frequency of $f = 4.5$ GHz, having a maximum peak in 64 mV and a minimum of 95 mV.

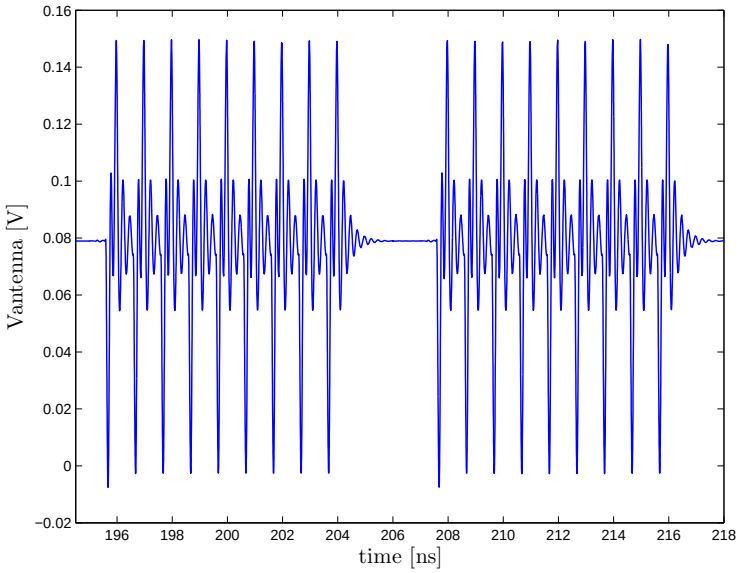

Figure 4.9: Pulse meant to be sent.

One crucial point of the antenna design verification is the power spectrum in frequency. It was made a analysis of the gaussian pulses in figure 4.10 having for 4.5 GHz a maximum value of $-120\ dBm/MHz$.

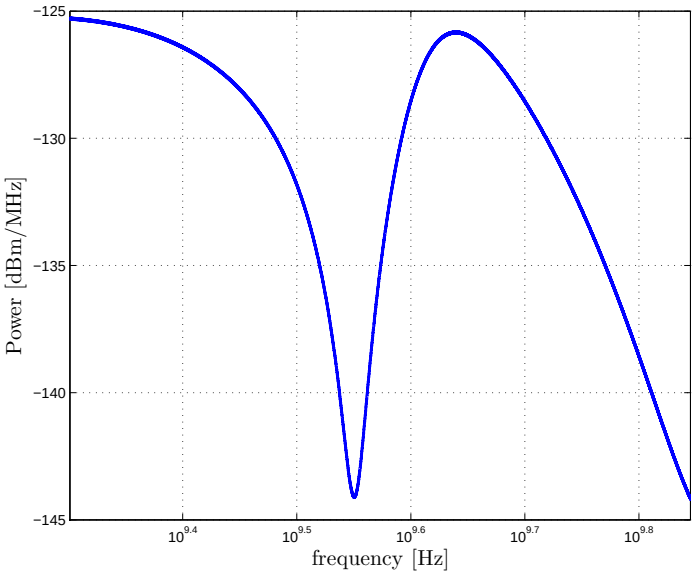

Figure 4.10: Power Spectrum of the dipole antenna.

4.3 Receiver

The third section of this chapter presents the implementation and simulation of the receiver block where several simulations were done in the Analog Design Environment, specially for the Cascode balun LNA where is presented a detailed study after having done a great effort to choose the most appropriate architecture. The main simulations were done in transient analysis, DC analysis which were treated in matlab in order to better show the results.

4.3.1 Low Noise Amplifier

After the receptor antenna, the second block is the Low Noise Amplifier, where in figure 4.11 is represented the circuit, this is a critical block, since in the reception the signal is with a relatively low power, which makes it sensible to noise generated during the transmission [22]. Having as main characteristics a large bandwidth with a balanced input impedance in order to obtain the maximum efficiency, being a balun LNA, converts a single-ended input to a differential output, facilitating the cancellation of noise and distortion also referring that it is used in a cascode configuration to improve the input balance and to permit an higher voltage gain being constituted by a Common Source and a Common gate configuration where both of them have an equal value of voltage and the gain is only in phase opposition, with the same value in module. By this is meant that the resultant value of the gain is the sum of both outputs. To match the impedance at the

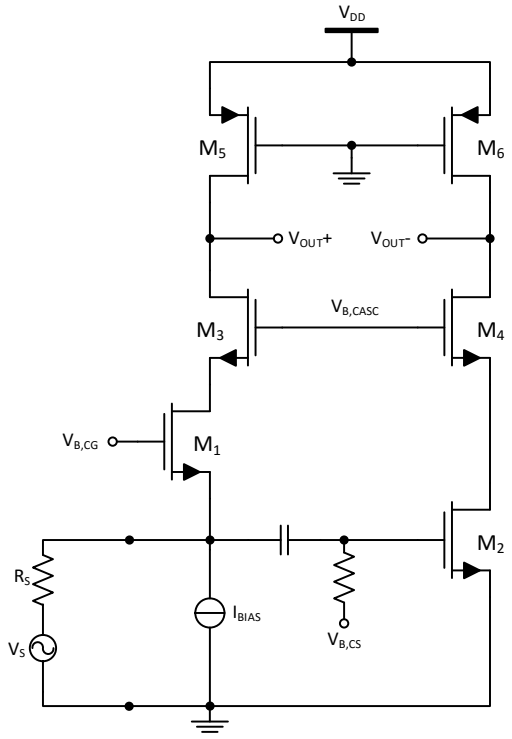

Figure 4.11: CAScode balun LNA.

entrance, it is necessary to find the input impedance, having,

$$Z_{in} = Z_{in,CG}||Z_{in,CS} \tag{4.12}$$

where the CS with an almost infinite input impedance, having $R_L = rds$ as the impedance of the PMOS transistors seen by the LNA output, the last formula can be expressed as,

$$Z_{in} = \frac{1}{g_m, CG}(1 + \frac{R_{casc}}{r_{ds,CG}}) \tag{4.13}$$

Knowing that the R_{casc} is the output impedance of the telescopic cascode amplifier,

$$R_{casc} = \frac{1}{g_{m,Casc}}(1 + \frac{R_L}{r_{ds,Casc}}) \tag{4.14}$$

Assuming that $r_{ds,Casc} \gg R_L$ and that the $r_{ds,CG} \gg R_{casc}$, so

$$Z_{in} = \frac{1}{g_{m,CG}} \tag{4.15}$$

As said before the LNA output is in differential configuration so, theoretically both stages has the same voltage, which results in

$$A_v = g_{m,CG} \cdot R_{out} + g_{m,CS} \cdot R_{out} \tag{4.16}$$

having R_{out} as the impedance output by each stage of the LNA, which is the parallel of each output cascode stage impedances, r_{CS} and r_{CG}, with the R_L impedance. Taking into account that both of that cascode impedances are significantly higher than R_L, we can conclude that the resulting gain is

$$A_v = g_{m,CG} \cdot R_L + g_{m,CS} \cdot R_L \tag{4.17}$$

Once there is the need of CG cancellation, both gains must be equal $g_{m,CG} = g_{m,CS}$, resulting in,

$$A_v = 2 \cdot g_{m,CG} \cdot R_L \tag{4.18}$$

In the other side the thermal noise generated by the CG due to i_N current produces a voltage noise at the entrance of the CS with phase opposition compared to the CG, however as the CS inverts the signal phase, having both signals with the same value consequently will be cancelled at the output of the LNA, the output gain is the sum of both V_{out} One of the possible ways to optimize this block is through the substitution of the resistances with a PMOS transistor working in the triode region. The great advantage of this is the minimum space it needs and to have a great resistive load with the same voltage drop. Neglecting the transistors capacitive effects, the CG transistor body effect and the short-channel effects so that will be easier to study it without compromising the theoretical results.

Looking to both equations of Noise Factor, from common gate topology and common source topology, we can conclude that they are similar:

$$F \approx 1 + \frac{\gamma}{g_{m_2} R_S} + \frac{1}{g_{m_2}^2 R_S R_L} \tag{4.19}$$

$$F \approx 1 + \frac{\gamma}{g_{m_1} R_S} + \frac{1}{g_{m_1}^2 R_S R_L} \tag{4.20}$$

Simulation

Typically transmission lines and antennas have an impedance of 50 Ω, therefore, the LNA was designed with an input impedance of 50 Ω too, it will result in a minimization of reflections in the signal allowing a maximum efficiency of the systems. As the other blocks, the LNA has a supply voltage of 1.2 V and a biasing current of 1.5 mA. All NMOS transistors have the minimum length permitted by the technology and use as isolators of the DC and AC signals a capacitor of 5 pF and resistors of 20 $K\Omega$. In order to obtain a reasonable value of input impedance both transistors M_1 and M_2 must be designed with a value of $Z_{IN} = 50\ \Omega$ to reduce the noise. Another important factor is the DC voltage, since it is responsible for maintaining the desired transistors operation. To obtain the desired differential output it was necessary to readjust some of the parameters since in the theoretical calculus was not taken into account the body effect and many other variants that affect the circuit. In table 4.4 is the simulated values for the LNA parameters.

Table 4.4: LNA parameters.

transistor	$W(\mu)$	$L(\mu)$	**Region**	$I_D(mA)$	$V_{DSat}(V)$	$g_m(mS)$
M_1	73.6	120	active	-1.5	110.2	20.02
M_2	150	120	active	1.05	73.2	17.96
M_3	5.6	120	active	-1.5	299.1	3.66
M_4	28.8	120	active	1.05	171.4	9.58
M_5	7.2	120	triode	-1.5	-736.7	1.88
M_6	6.4	120	triode	1.05	-729.2	1.14

The simulated input impedance in figure 4.12 is around 60 Ω for a frequency of 4.5 GHz it could be considered a good value since the signal is wideband, with such a high frequency. The problem with the fast fall of the impedance is due to the fact of having parasitic capacitances that increase in value with the increase of the frequency. Another important simulation is the ratio of input signal refection called S_{11}, figure 4.13 which also present good values.

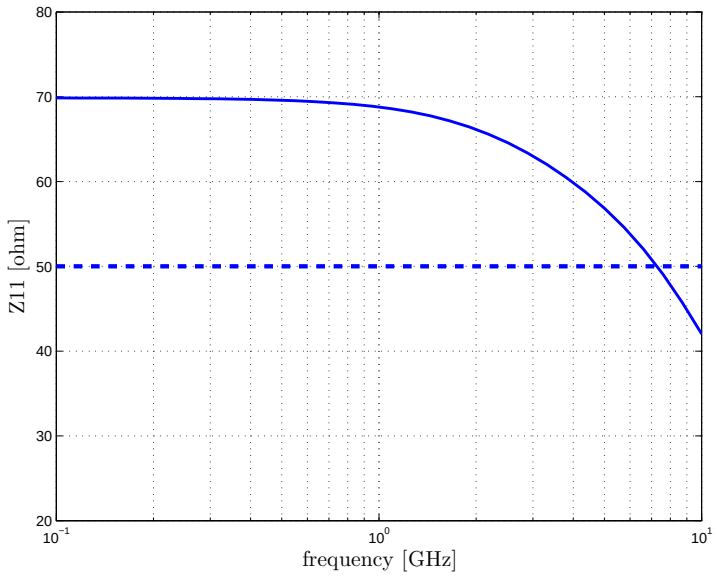

Figure 4.12: LNA input matching.

The differential voltage gain of the LNA presented in figure 4.14 for a value around 4.5 GHz has a gain of 28 dB which is perfectly enough for it functions. Once again the parasitic capacitances interfere with the desired gain, as it was studied there are parasitic capacitances in the output mode from the cascode devices. After all, the Noise Figure presents a value that could had been better, one of the possible motives could be caused by the reduction of the voltage gain for higher frequencies.

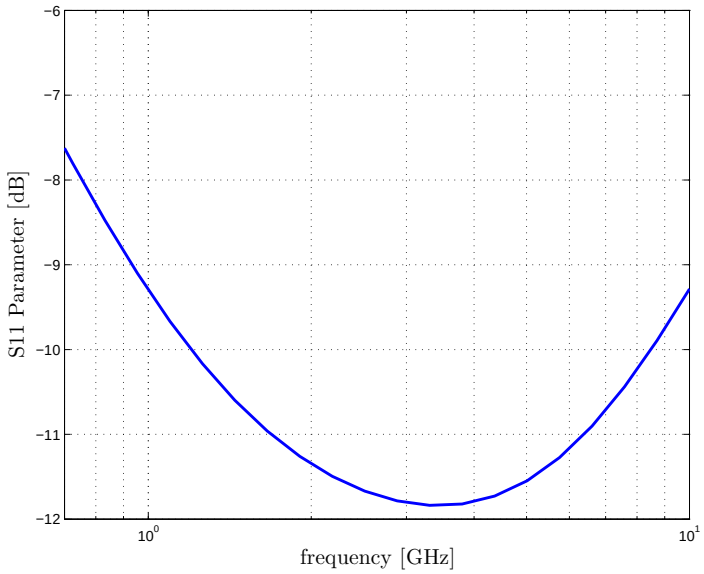

Figure 4.13: S_{11} parameters.

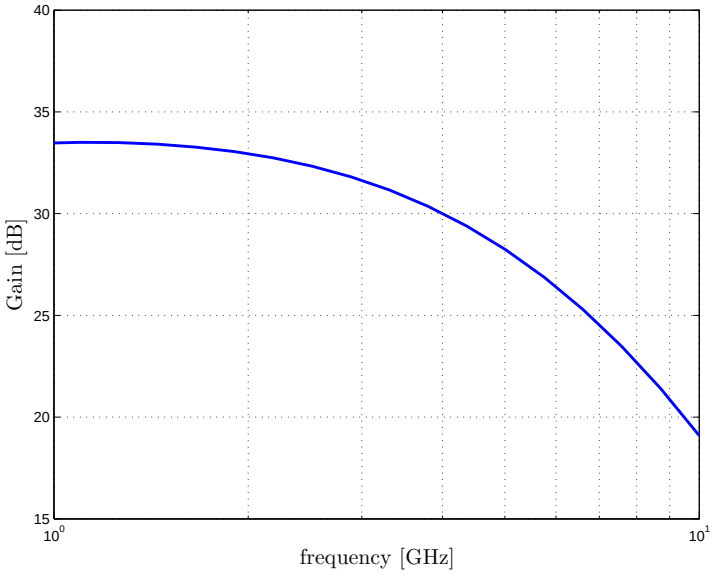

Figure 4.14: LNA gain signal.

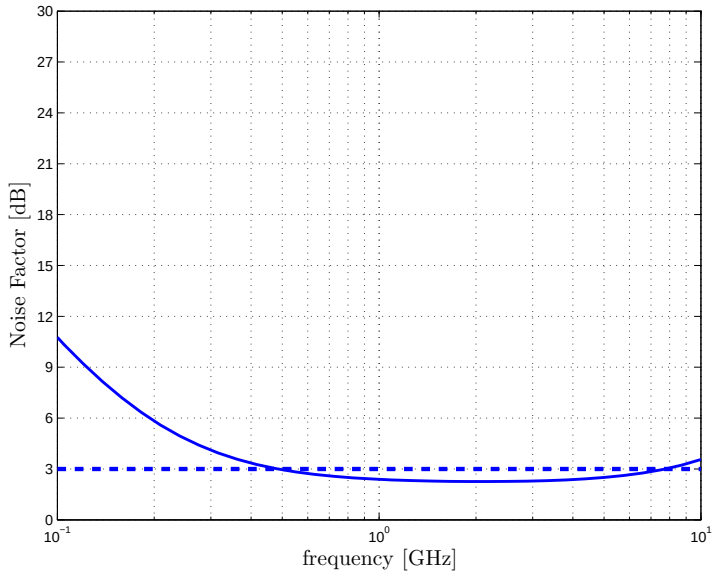

Figure 4.15: LNA Noise Figure.

4.3.2 Self-Mixer

In this subsection is explained the design of the self-mixer where is presented the electric circuit and all the steps for the complete design, [36]. As said before it is based in a Gilbert Cell, in figure 4.16.

The Self-Mixer used in this report is the equivalent of having two single balanced mixers, figure 3.13, with the outputs linked in pairs and with a phase shift of 180, which results in a differential output in voltage. Considering that the circuit does not have parasitics effects, the single balanced mixer gain is given by,

$$G_c = \frac{2}{\pi} \cdot g_{m_1} \cdot R \tag{4.21}$$

Each output stage is powered in current with one of the two branches from the third differential pair (NMOS), these branches do a voltage to current conversion. Having this topology means that the current goes through A and B are dependants of C voltage, the mixing effect is achieved with the switching of outputs stages A and B. The NMOS transistors of the differential pair C should work in saturation zone, so that will be possible to obtain an effective gain. On the other hand the two remaining differential pairs should alternate between cut and saturation zone, so that the mixing effect could be maximized, having a low impedance at saturation zone and high impedance at cut zone.

The design of the circuit is made in several different steps. which has it first step with sizing the transistors of the bottom, the differential which are designed with the maximum width and the minimum length, possible with the technology used, in order to maximize the voltage gain of the self-mixer, with the transconductance. In this stage is also necessary to define the bias voltage of each transistor to make them work in the saturation region.

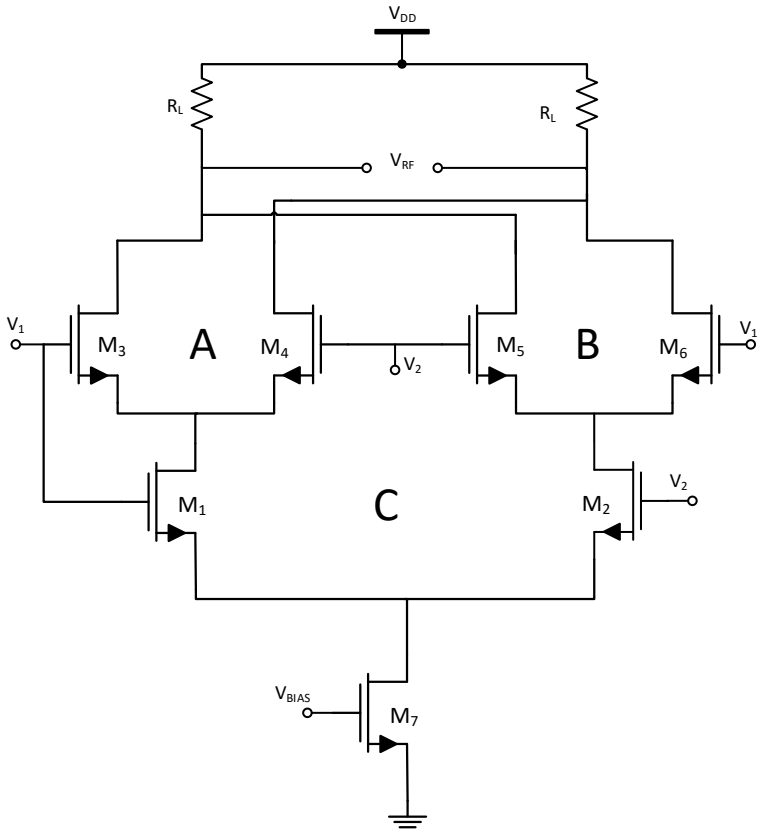

Figure 4.16: Self Mixer based in a Gilbert Cell Mixer.

The next step, the two NMOS differential pairs left are designed, knowing previously that the input signals are small in amplitude, transistors need to be sized with maximum width and minimum length in order to obtain a fast response result, which will result in a maximization of the slope in the linear characteristic. It is also important to give a good voltage room in this stage in order to maintain it in the saturation region during the ON cycle, last but not the least in this stage it is also desirable to reach a low impedance mode between the two first stages and a much higher impedance output than the active loads. To the complete design of the self mixer it is also necessary to size the PMOS active loads, which get fully optimization by reaching the triode zone, however needs to stay sufficiently close to saturation, to get a better small signal resistance, which result in a higher self-mixer gain. Using the self mixer presented in figure 4.16, it was obtained:

Simulation

The self-mixer was designed for the frequency of 4.5 GHz resulting in a waveform with twice the frequency value and only with positive voltage values. The self-mixer has a supply voltage of 1.2 V. All NMOS transistors have the minimum length permitted by the technology and use as isolators of the DC and AC signals a capacitor of 5 pF and resistors of 20 $K\Omega$. Another important factor is the DC voltage, since it is responsible

Table 4.5: Mixer parameters

transistor	$W(\mu)$	$L(\mu)$	$I_D(mA)$	$V_{DSat}(mV)$	$g_m(mS)$
M_1	115.2	120	4.3	134	45.9
M_2	115.2	120	4.3	134	45.9
M_3	115.2	120	2.15	104.5	30.4
M_4	115.2	120	2.15	104.5	30.4
M_5	115.2	120	2.15	104.5	30.4
M_6	115.2	120	2.15	104.5	30.4
$M_{R_{L_1}}$	24	120	-4.31	-729.2	4.68
$M_{R_{L_2}}$	24	120	-4.31	-729.2	4..68

for maintaining the desired transistors operation. To obtain the differential output it was necessary to readjust some of the parameters since in the theoretical calculus was not taken into account the body effect and many other variants that affect the circuit. In table 4.5 is the simulated values for the self-mixer parameters.

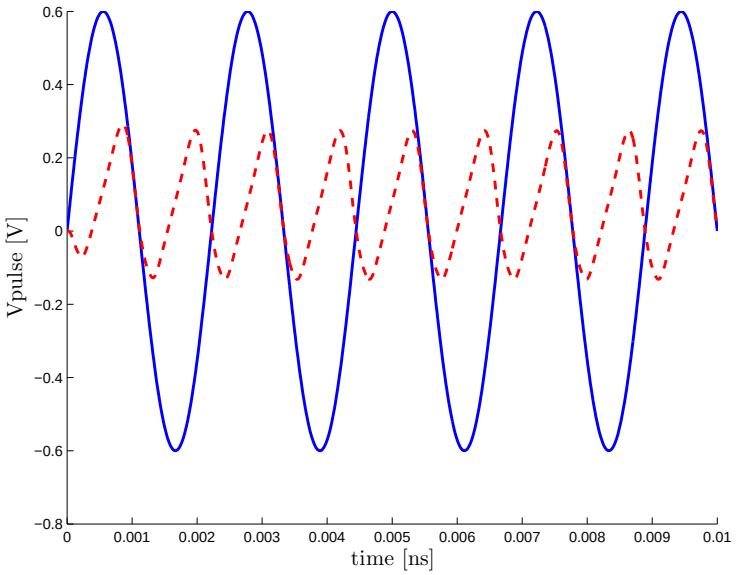

Figure 4.17: Mixer Input and output.

Taking into account figure 4.17, there is two main differences between the input signal and the output. The input has a higher voltage amplitude compared with the output, the main cause of this is due to the appearance in the frequency spectrum.

4.3.3 Integrator

The circuit in figure 4.18 is characterized by having a n-ch and a p-ch complementary input folded cascode architecture, studied in [37]. Taking special attention to the V_{icm} range it is possible to say that it is capable of a rail-to-rail V_{icm}. To find the value of V_{icm}

range it is necessary to study each input pair. Looking to equation 4.22 for the n-ch input pair and for the p-ch input pair equation 4.23.

$$V_{SS} + V_{DSAT_1} + V_{DSAT_5} + |V_{TN}| \leq V_{icm} \leq V_{DD} - |V_{TN}| - V_{DSAT_3} + |V_{TN}| \tag{4.22}$$

$$V_{SS} + V_{DSAT_{10}} - |V_{TP}| \leq V_{icm} \leq V_{DD} - V_{DSAT_4} - V_{DSAT_{14}} - |V_{TP}| \tag{4.23}$$

The result of the addiction of 4.22 and 4.23 gives the total V_{icm} range.

$$V_{SS} + V_{DSAT_{10}} - |V_{TP}| \leq V_{icm} \leq V_{DD} - V_{DSAT_5} + |V_{TN}| \tag{4.24}$$

It is important to be aware that the range can overcome the value of V_{DD} which can be a problem for the good transistor response.

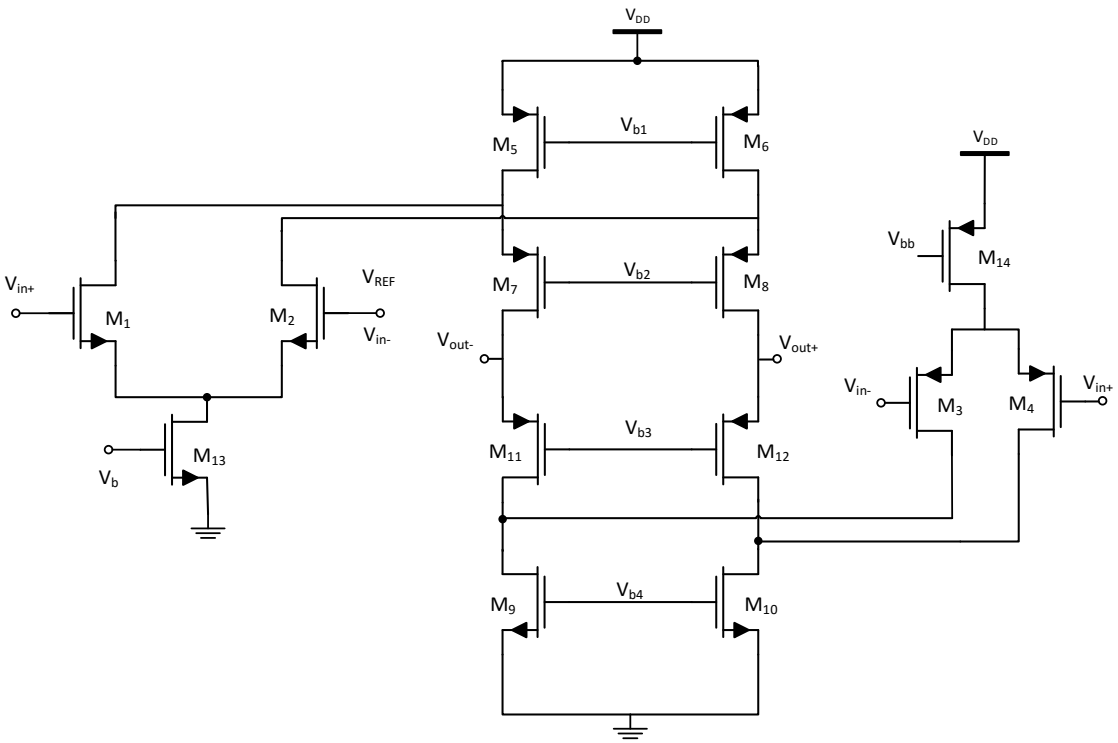

Figure 4.18: Folded Cascode Complementary Input Architecture.

Initially is presented the complete circuit schematic following with an explanation of it. As said before the integrator used in this report is based in Operational Amplifier with a capacitor in parallel and a resistor in series with the circuit, at the input of the amplifier which will introduce the time constant RC responsible for the period of time that the amplifier is integrating the UWB signal, equation 4.25.

$$f = \frac{1}{2\pi RC} \tag{4.25}$$

In order to obtain a reasonable integration from a very short pulse train duration time, the integrator constant RC must be small enough in order to achieve an acceptable gain. In addiction the amplifier requires to be design with a significant large gain to overcome the ultra-wideband mismatching and high frequency attenuation.

4.3.4 Comparator and Latch

In this subsection is explained the design and operation of the comparator, in figure 4.19 with a SR NAND Latch where it is presented the electric circuit and all the steps for the complete design, which was already studied in [29]. Having a close look to the comparator it is possible to say that the block consists in a clocked differential pair $M_1 - M_2$, two cross-coupled pairs $M_3 - M_4$ and $M_5 - M_6$ and two pre-charge switches $M_7 - M_8$. The output of the circuit as a rail-to-rail characteristic depending on the response to the polarity of $V_{IN} - V_{REF}$. The circuit can be described in four main operating phases:

- In the first one, clock is low, M_1 and M_2 are off. Also the output nodes and P and Q are pre-charged with the value of V_{DD}.
- In the second phase, clock goes high , turning the switches off and M_1 and M_2 go on due to the NMOS transistor M_9. This change in the block will result in a differential current in proportion to $V_{IN} - V_{REF}$. Referring that $M_3 - M_6$ initially are off, this current flows from C_P and C_Q allowing $|V_P - V_Q|$ to grow, in this phase there is also a voltage gain characteristic resulting from the common drain amplifier, known as the amplification mode phase.
- the third phase starts with the fall of $|V_P - V_Q|$ to $V_{DD} - V_{TH}$ which will allow the flow of current from X and Y. Subsequently the output voltages V_X and V_Y continue to fall until they reach $|V_{DD} - V_{TH}|$, which is the point when M_5 and M_6 turn on.
- The last phase is when M_5 and M_6 turn on, where the positive feedback of these transistors will bring one of the output back to V_{DD} while the other one will fall to zero.

In this block every transistor has a function and besides $M1$, M_2 and M_7 being the critical ones, the rest should not be forgotten. Transistors $M_3 - M_4$ cut off the DC path between V_{DD} and the ground at the end of the fourth phase, resulting in the absence of static power gain. Transistors M_5 and M_6 restores the output high level to V_{DD}. Switches S_1 and S_2 reset to the first state and suppresses dynamic offsets. Since for half of the clock cycle the output presents an invalid value, to interpret correctly it is implemented a RS NAND Latch. From is the total input refereed noise demonstrated which results in:

$$\overline{V_{n,in}^2} = \frac{(V_{GS} - V_{THN})_{1,2}}{V_{THN}} \cdot \left[\frac{4KT\gamma}{C_{PQ}} + \frac{((V_{GS} - V_{THN})_{1,2})}{V_{THN}} \cdot \frac{KT}{2C_{P,Q}} \right] \tag{4.26}$$

Where the first term represents the noise due to M_1 and M_2, which is significantly greater than the second term.

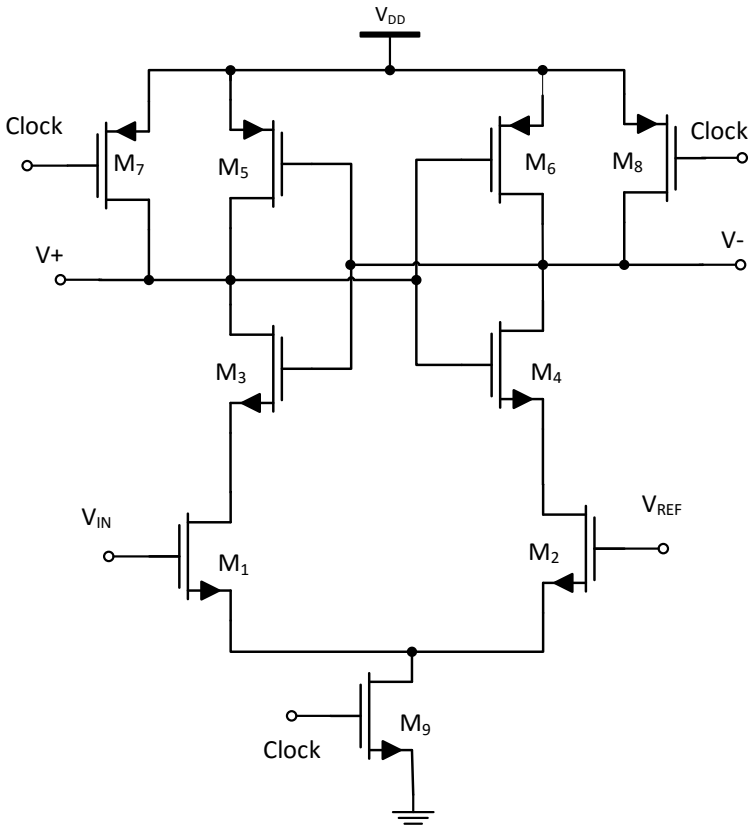

Figure 4.19: Simplified schematic of the conventional dynamic comparator.

Simulation

The comparator was designed for the frequency of 4.5 GHz resulting in a waveform with twice the frequency value and only with positive voltage values. The comparator has a supply voltage of 1.2 V. All NMOS transistors have the minimum length permitted by the technology and maximum value for the width in order to obtain a fast operation. Another important factor is the DC voltage, it should have a value high enough to maintain all transistors in saturation. To obtain the desired differential output it was necessary to readjust some of the parameters since in the theoretical calculus was not taken into account the body effect and many other variants that affect the circuit. In table 4.6 is the simulated values for the self-mixer parameters.

Table 4.6: Comparator parameters

transistor	$W\mu m$	$L\mu m$
M_1	230.4	0.12
$M_2 - M_3$	115.2	0.12
M_4	86.4	0.12
$M_5 - M_6$	96	0.12
$M_7 - M_8$	57.6	0.12
M_9	115.2	0.12

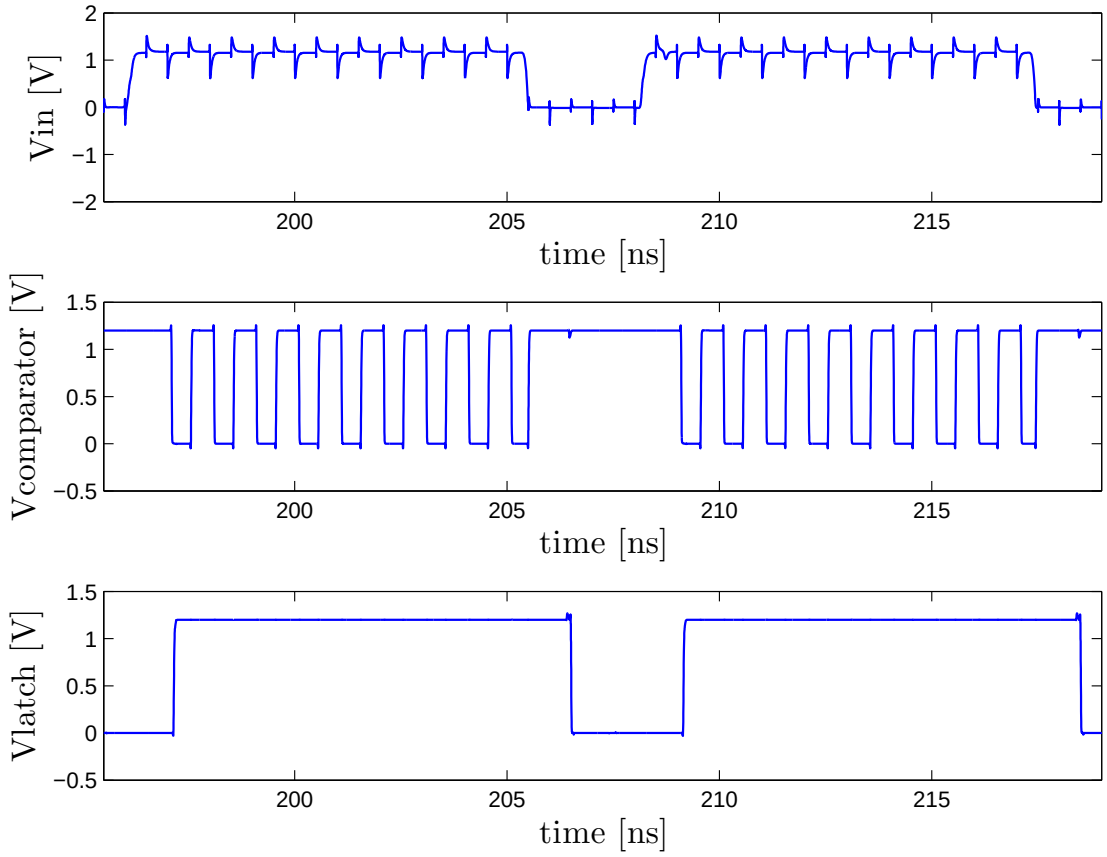

Figure 4.20: Comparator input.

In the last figure 4.20, It is represented the input signal of the comparator, the output signal of the comparator and the output signal of the NAND SR Latch, respectively, where was identified few problems here. As expected there exists some delay in both blocks operations, $t_{delay} = 0.225\ ns$ this delay appears due to the fact of precisions problems of the comparator, meaning that it has an offset during the comparison with the reference voltage, it is also important to refer the *kickback* effect this phenomenon happens when transistors M_1 and M_2 change between saturation and triode region resulting in an increase of their gate drain capacitance.

4.3.5 Overall Circuit

After all block simulations it is crucial to be aware that the IR-UWB transceiver has just one purpose to transfer a particular data by designing a transmitter and it receiver, by this looking to figure 4.21, having a delay of 2 ns, perfectly normal since this system is composed by many different operations.

Table 4.7: IR-UWB transceiver characteristics.

Technology	130 nm
Modulation	OOK
Power	97 mW
Spectrum Power	-120 dBm/MHz
Center Frequency	4.5 G

In table 4.7 is represented the main characteristics of the system, where it should be emphasized the centre frequency of 4.5 GHz and the value of Power Spectrum with -120 dBm/MHz, additional figures from cadence are in annex.

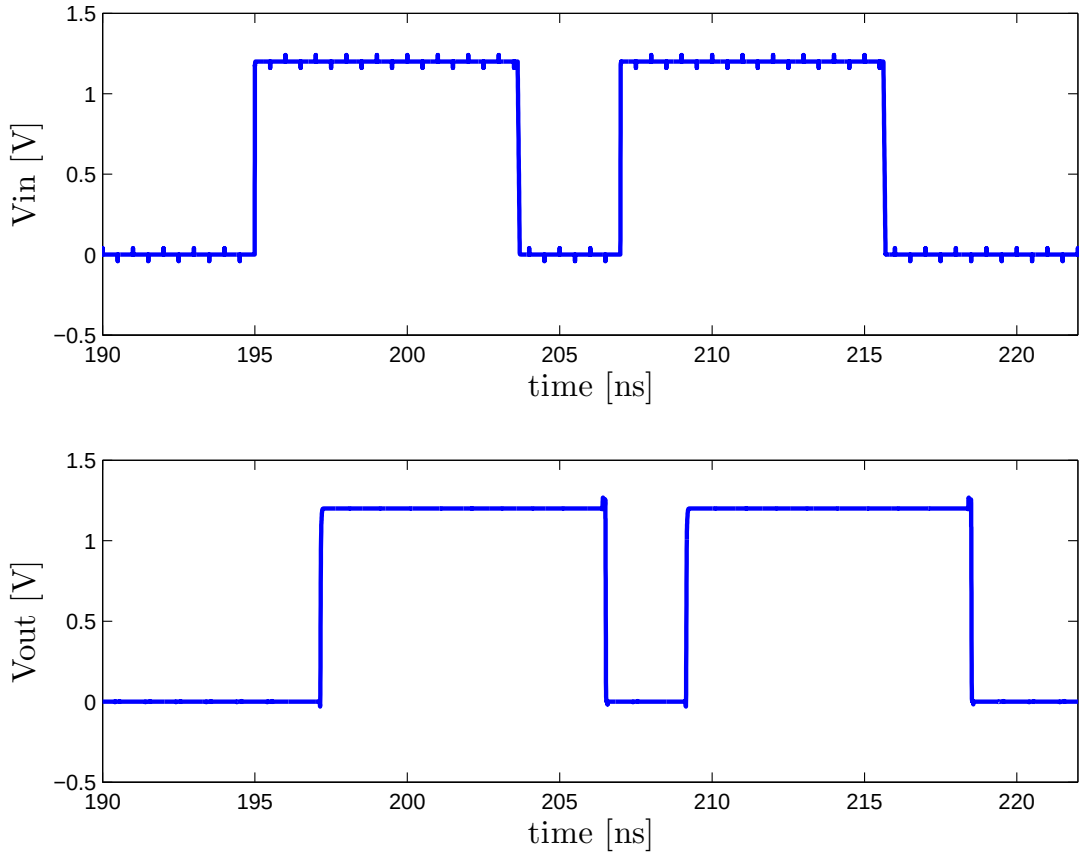

Figure 4.21: The input data and the output of the transceiver.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

During this thesis were made several simulations and studies for every block, to decide which one better fit in the transceiver and of course from that some interesting points should be referred. Having a close look to the frequency spectrum it is possible to say that it is significantly saturated and here the IR-UWB fits perfectly, it came to solve the problem once it is characterized by using low values for the frequency spectrum which is seen as noise for the common narrowband technologies and in this context the UWB RF CMOS transceiver enters.

The transceiver that was studied in this project based in a non-coherent system where in the transmitter there is an OOK modulator, pulse generator and a driver amplifier to drive the signal to a 50 Ω antenna while in the receiver there is a balun-LNA with a differential output, an integrator and for the detection of the signal and demodulation is a comparator with a NAND SR LATCH at the output.

At this point, looking only to the significant simulations and results, it is correct to conclude that the core specifications were accomplished. In the transmitter besides the design of the modulator and pulse generator where without any major difficulties the expected frequency 4.5 GHz was a achieved however for the driver amplifier there existed some problems specially related with accomplishing the centre frequency, that is the reason why it was just used a simple driver amplifier where the main ability is to drive the signal to the antenna. While in the receiver a much more complex system than the transmitter was designed where once again the greatest problems were related with the centre frequency. The LNA block after designing the circuit, there were still some problems to obtain the maximum efficiency from the chosen architecture, after it the self mixer prepared the signal to fully integrate and transferred it into a higher frequency

$2 \cdot f_{V_{IN}}$, after having prepared the signal, with the integrator, so that the comparator had enough time to do the comparison operation.

To conclude the complete transceiver was capable of proper transmission and reception of the signal as expected. However it presented a low power value for the frequency spectrum as said before and for a proper use in IoT nodes, there is the need of more efficiency blocks to achieve a lower power specifications and the transceiver simulation results can be used to compare with other recent works in UWB wireless transceivers.

5.2 Future Work

Through the study, implementation and simulation there were some crucial points that should have been studied in more detailed and also it is important to mention that many blocks should have been improved.

In the transmitter the driver amplifier can be substituted by another, with a better gain value in order to obtain higher results in the power frequency spectrum, to achieve further distance communications.

In the receiver the self-mixer should be studied better alternatives in order to replace it with a mixer with higher gain characteristics. It is also crucial to refer that another alternative for the integrator must be studied and implemented since the used one did not achieve the desired results as a result it was used with ideal components.

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APPENDIX A

ANNEX

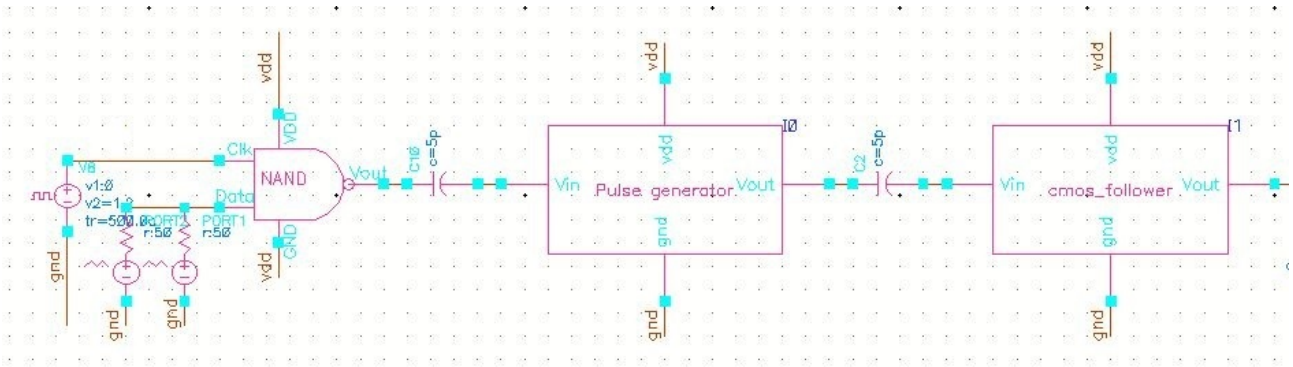

Figure A.1: Transmitter block diagram from cadence.

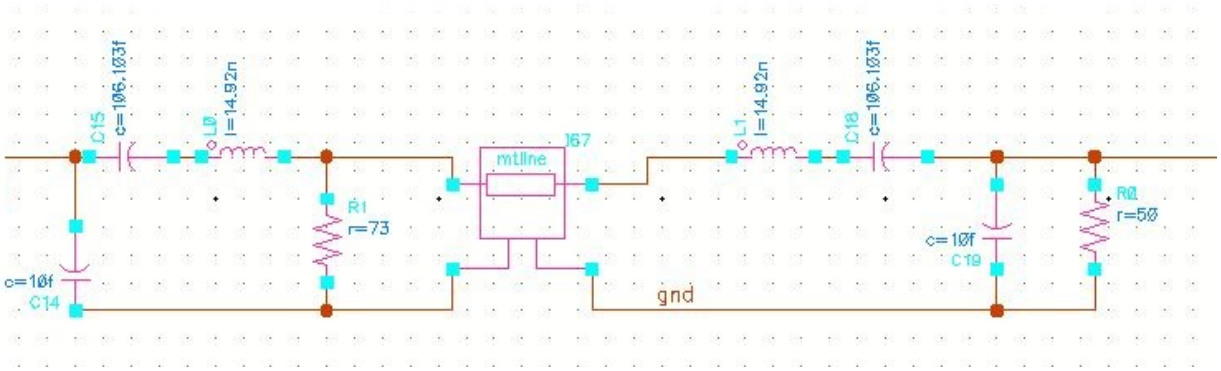

Figure A.2: Transmitter and receiver antennas electric circuit from cadence.

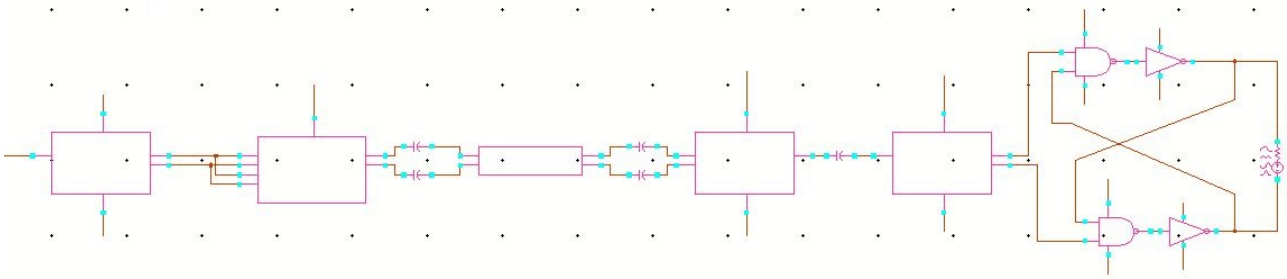

Figure A.3: Receiver block diagram from cadence.

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