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Advanced Electrical Characterization of Oxide TFTs Design of a Temperature Compensated Voltage Reference

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Advanced Electrical Characterization of Oxide TFT's

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To my family and all my close friends.

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Abstract

Any electronic device, regardless of its function, needs a reference voltage source that feeds reliably, i.e., which generates a constant voltage, upstream and regardless of external environmental conditions, such as temperature. Since such a characteristic negatively influences the behavior of the devices, whose base elements are transistors, it is essential to design a circuit that provides a voltage which is invariant over a temperature range.

In this work is designed a circuit that is responsible for generating a reference voltage using only thin film transistors or TFTs, on glass substrate. However, in order to validate the concept used in the mentioned transistors, it is also dimensioned and simulated the proposed circuit in 130 nm CMOS technology, where the respective results are expected to be comparative between the two technologies. For CMOS technology, for a nominal reference voltage of 124,0 mV, Cadence simulation reveals ±2,2 ppm/°C temperature coefficient, between -20 °C and 100 °C. The power consumptions are and 1,434 mW and 4,566 mW for both CMOS and IGZO-TFT technologies, respectively.

Keywords: Low-voltage CMOS and TFT voltage reference, Current subtraction, Thin-film transistors, CMOS, TFT, Partial compensation, Bandgap.

Resumo

Qualquer dispositivo electrónico, independentemente da sua função, necessita sempre de uma fonte de tensão de referência que o alimente de forma fiável, isto é, que gira uma tensão constante, a montante, e independente de condições externas do meio, tal como a temperatura. Visto que a referida característica influencia negativamente o comportamento dos dispositivos, dado que têm como elemento base o transístor, é essencial projectar um circuito que, à sua saída, forneça uma tensão invariante ao longo de uma escala de temperatura.

Neste trabalho é dimensionado um circuito responsável por gerar uma tensão de referência, utilizando apenas transístores de película fina, ou TFTs (*Thin Film Transistors*), em substrato de vidro. Contudo, a fim de se validar o conceito utilizado nos referidos transístores, é também dimensionado e simulado o circuito proposto em tecnologia CMOS 130 nm, onde se obtêm também resultados que vêm a ser comparativos entre ambas as tecnologias. Em tecnologia CMOS, para uma tensão de referência de 124,0 mV, as simulações em Cadence revelam um coeficiente de temperatura de ±2,2 ppm/ºC, entre -20ºC e 100ºC. As potências consumidas são de 1,434 mW e 4,566 mW para as tecnologias CMOS e TFTs IGZO, respectivamente.

Palavras-chave: Tensão de referência de baixa tensão; Subtracção de correntes; Transístor de película fina, CMOS, TFT, Compensação parcial.

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Abbreviations

ADC	**A**nalog to **D**igital **C**onverter
AMOLED	**A**ctive-**M**atrix **O**rganic **L**ight-**E**mitting **D**iode
a-Si	**A**morphous **Si**licon
BGR	**B**and**g**ap Voltage **R**eference
BJT	**B**ipolar **J**unction **T**ransistor
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CTAT	**C**omplementary **t**o **A**bsolute **T**emperature
DAC	**D**igital to **A**nalog **C**onverter
IGZO	**I**ndium-**G**allium-**Z**inc-**O**xide
KCL	**K**irchhoff **C**urrent **L**aw
LCD	**L**iquid **C**rystal **D**isplay
LTPS	**L**ow **T**emperature **P**olycrystalline **S**ilicon
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
NMOS	**N**-Channel **MOS**FET Transistor
NPN	**N**egative-**P**ositive-**N**egative

OLED	**O**rganic **L**ight-**E**mitting **D**iode
PCB	**P**rinted **C**ircuit **B**oard
PMOS	**P**-Channel **MOS**FET Transistor
PNP	**P**ositive-**N**egative-**P**ositive
Poly-Si	**P**olycrystalline **Si**licon
PTAT	**P**roportional **t**o **A**bsolute **T**emperature
SFDR	**S**purious **F**ree **D**ynamic **R**ange
SMD	**S**urface-**M**ount **D**evice
SRAM	**S**tatic **R**andom **A**ccess **M**emory
Ta_2O_5	**Ta**ntalum Pent**o**xide
TC	**T**emperature **C**oefficient
TFT	**T**hin-**F**ilm **T**ransistor
ZTO	**Z**inc-**T**in-**O**xide

Introduction

1.1. Background and Motivation

So far, transistors have been the main component of every integrated circuit. Nowadays, a single processor, can take billions of these components in a very small area and this can lead to an increase of generated heat, which can result in several problems, such as system instability. This happens because the behavior of the transistors changes, in general, according to the temperature. Assuming that transistors are not ideal components and the circuits where they are fitted need to be powered reliably, the design of a stable voltage reference within a large temperature range is crucial. An ideal voltage reference has no variation, which means that independently of the temperature, the value of its output is always the same which is the objective of this work.

There are several types of transistors with different configurations that combine the positions of their different layers, as well as the respective materials. Considering this, the motivation of this work is to design a low-voltage reference circuit using only thin film transistors and comparing the obtained results with a standard technology, such as CMOS 130 nm. Although, despite the number of different material combinations that can be used, the TFTs in question are made of amorphous Indium-Gallium-Zinc-Oxide, also known as IGZOs. They have several advantages when compared to Zinc-Tin-Oxide of amorphous Silicon TFTs, such as higher mobility and simpler fabrication processes.

To master the technique of designing a reliable voltage reference, a first study is made of the concept used in [1]. It is also described and validated, using CMOS 130 nm along mathematical and simulation resources, like MathCAD and Spectre, and then a different circuit is proposed and tested, using only glass-TFTs, which has never been done.

1.2. Thesis Organization

The present work is organized in six main chapters that are briefly described below, with the exception of the introductory one.

Chapter 2 introduces IGZO TFTs, describing what are the principal modes of operation, what types of structures are mainly used, as well as their principal differences, and a comparison between different materials that compose them.

Chapter 3 is about low-voltage reference topologies. In this chapter several topologies are analyzed theoretically, including the one that is used as base for this work.

Chapter 4 includes all the work that was made in CMOS 130 nm technology, starting from initial considerations, theoretical analysis and how the starting point was calculated to the final results and simulations. All steps from the initial circuit from [1] are described to an end where only n-type channel transistors are used with the same physical dimensions as TFTs, which leads to the next chapter.

Chapter 5 describes the methodology and presents the results of the respective simulations when using real TFTs since it was not possible to test them by software simulations because the respective models were not characterized in temperature.

Chapter 6 is the last chapter of this thesis, where are written the overall conclusions and a comparison between different simulations and different technologies is shown. Projections for a future work are also present in this section.

1.3. Contributions

Thin-film transistors differ from other more traditional types of transistors because they have the ability of being implemented on transparent substrate materials, being glass or plastic good examples of those. This leads to a new world of electronic implementation ideas, like electronic papers that can be bent, curved displays, completely transparent devices, and many others. For this to be applicable, all of the transistors need to have the same substrate, including, in the present case, the voltage reference module. However, the thermal characteristics of IGZOs, which are essential to develop a viable low-voltage reference, are not fully understood. Therefore, this work addresses that problem and helps to understand and develop a reliable low-voltage reference module, with a very low-voltage variation across the entire operational temperature variation, from -20ºC to 100ºC.

The work developed and presented in this entire document is to be used as a starting point for future students and advisors working with similar technologies.

2

Indium-Gallium-Zinc-Oxide TFT

2.1. Introduction

Thin-film transistors are most commonly used in smartphone displays. These transistors are responsible for turning the individual pixels 'on' and 'off'. This type of application requires efficient and low powered technologies. However, there are many more TFT applications, such as high density SRAMs, non-volatile memories, photo detector amplifiers, thermal printer heads, image sensors of finger print sensors.

There are many different TFT structures, fabrication processes, electrical characteristics, design parameters and physical materials that have to be considered in order to achieve the final objective and they are described in the present chapter.

Despite the fact that a single display can have multiple layers, usually five or more, it can be divided in two main categories, which are the backplane and the light emitting materials. Considering the first one, there are numerous technologies that can be used. However, major technologies use the following three types of materials, which are amorphous-Silicon, Indium-Gallium-Zinc-Oxide and Low Temperature Polycrystalline Silicon. As light emitting material types, the most commonly used are LCDs, OLEDs and, the most recent, AMOLEDs.

Amorphous Silicon has been the go-to material for backplane technology for many years and with a variety of different manufacturing methods, always with the objective of improving energy efficiency, refresh speeds and display's viewing angle. Due to the physical limitations of this material, the number of pixels per inch has to be limited to around 300, not being suitable on higher end AMOLED displays, since they put more electrical stress on the transistors, which a-Si TFTs cannot handle. That is where LTPS and IGZO come in. As a great advantage, a-Si TFTs are very cheap and have relatively simple manufacturing processes.

Low temperature polycrystalline silicon TFTs have higher temperature process manufacturing than a-Si TFTs (approximately 650 ºC). This technology is ideal for AMOLEDs, as their electron mobility is 100 times greater than the electron mobility of a-Si TFTs. On the other hand, the increasingly complicated manufacturing process and material costs are the big drawbacks of this technology, since it is about 14% more expensive when compared to a-Si.

Emphasizing IGZO TFTs, they were introduced in 2003, when almost all of the TFTs used were based on amorphous Silicon. With the need of faster and cheaper thin-film transistors, IGZOs started to provide the needed features. In spite of the electron mobility characteristics not being as great as LTPS, they offer a great increase when compared to a-Si as well, achieving values of about 10 to 50 $cm^2/(V.s)$ [2]. IGZO combines low cost of fabrication and scalability of a-Si with high performance of LTPS, which makes TFTs a good solution. Another advantage is that they can be shrunk down to smaller sizes, reducing power consumption. In addition, IGZO-TFTs fabrication need much less temperature, around 200 ºC, compared to LTPS which make them a suitable candidate for flexible electronics applications.

Figure 2.1 demonstrates a comparison of current-voltage characteristics between a-Si, IGZO and LTPS TFTs.

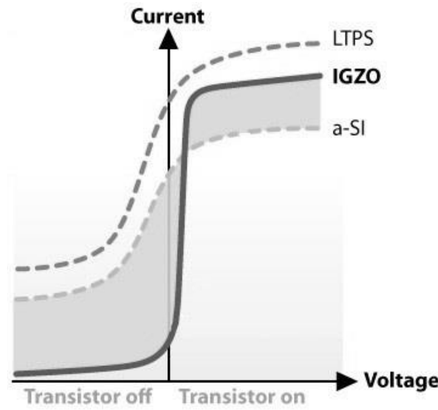

Figure 2.1: Demonstrative comparison of I-V characteristics between a-Si, IGZO and LTPS TFTs.

Fabrication processes, TFT structures and parameter extraction procedures are described below.

2.2. TFT structures

A single TFT is made of five different components, which are the gate, the drain and source layers, semiconductor and gate insulator layers, which are, in turn, organized in four different layouts, them being the normal (top-gate) staggered, the normal coplanar, the inverted (bottom-gate) staggered and the inverted coplanar.

On staggered types the drain and source electrodes are positioned on opposite sides of the semiconductor layer, whereas on the coplanar types all three electrodes, gate, drain and source are on the same side of the semiconductor [3]. All four different structures have their own set of advantages and disadvantages, although the most commonly used in fabrication processes, e.g., TFT-LCDs, is the inverted staggered, due to a relatively simpler fabrication process and about 30% higher electrons mobility, when compared to staggered top-gate. Inverted staggered is most used due to the manufacturing process of a-Si. Its gate protects the semiconductor from backlight on LCDs, since a-Si is light sensitive. In this particular case, the better to do is to deposit the semiconductor last. In LTPS technology the opposite happens, being the semiconductor layer deposited first, since it requires higher temperatures.

Like MOSFETs, TFTs can act as switches, with two inputs and one output, which are the gate, drain and source, respectively. The drain electrode is normally positive biased, but current only flows through the transistor when the gate electrode has sufficient potential. The transistor is considered on its 'on' state when the voltage value applied to the gate is greater than its threshold voltage, or V_{Th}, which forms a conductive channel of charge carriers, electrons, attracted by the electric fields. Otherwise it is 'off', where the drain current can be considered null. The choice of materials for each layer, as well as the respective thickness, are the keys for a good conductive transistor.

The gate dielectric, as the name suggests, is the layer responsible for isolating the gate of the semiconductor [3]. TFTs share the same characteristics of MOSFETs in a way that the current through the gate should be zero, so the gate dielectric has to be as low conductive as possible. Otherwise, electrons between the drain and source electrodes could flow out of the semiconductor, through the gate electrode, and decrease the overall performance of the transistor.

The choice of the drain/source contact material is crucial, as it determines whether electron or hole injection is preferred [4]. The contact resistances between the metal (drain and source) electrodes and the semiconductor reduce the maximum current that will flow through the device in the on-state. Nevertheless, as a Schottky barrier is formed at those contacts, the contact resistance during the transistor off-state should be high enough to prevent a high leakage current. For staggered structures, a major contribution to the contact resistance is related to the contacting interfaces of electrical leads and connections. This mainly occurs because the charge carriers have to travel through the semiconducting layer thickness before reaching the gate dielectric/semiconductor interface. In the case of coplanar setups, the drain and source electrodes are already in contact with the formed accumulation layer, which results in a low access resistance. However, results show that if drain/source electrodes are deposited on the active semiconductor, the access resistance is reduced due to valleys in the semiconducting film [5]. An additional reduction of the contact resistance is observed due to the increased contact area when the drain/source metal is deposited on the semiconductor layer [4][6].

All main four TFT structures are presented in figure 2.2.

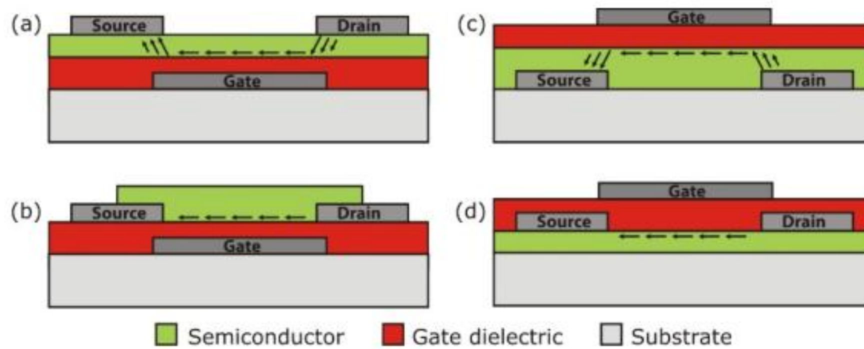

Figure 2.2: General TFT structures: a) Staggered bottom-gate; b) Coplanar bottom-gate; c) Staggered top-gate; d) Coplanar top-gate.

2.3. Basic Characteristics

TFTs acts as traditional MOSFETs. Their main parameters are the voltage applied to the drain, the voltage applied to the gate and the drain current generated by these two.

The drain voltage, V_D, is normally a static value, but has to be high enough in order to guarantee that the transistor will be turned 'on' when a certain value of gate voltage is applied, whereas the source is connected to a lower voltage source. When V_D is fixed, which value depends on the technology used, e.g., 1.2 V for traditional CMOS, or 10 V for IGZO TFTs, the behavior of the transistor stays entirely dependent of the gate voltage applied, V_G. If V_G doesn't exceed the threshold voltage V_{Th}, it is considered to be in cutoff mode or weak-inversion region; if V_G continues to be slightly increased, current I_D starts to flow and it is assumed to be in triode mode or in its linear region, assuming $V_{GS}>V_{\text{th}}$ and $V_{DS}<(V_{GS}-V_{\text{th}})$. This mode of operation can be useful on many operations, since the transistor behaves as a variable resistor; if V_G exceeds V_{Th} and $V_{DS} \geq (V_{GS} - V_{\text{th}})$ it is 'on', also known as active or in saturation region. The current has its maximum value in this region, but can be adjusted mathematically by varying the size of the transistor. The described behavior is graphically represented in figure 2.3.

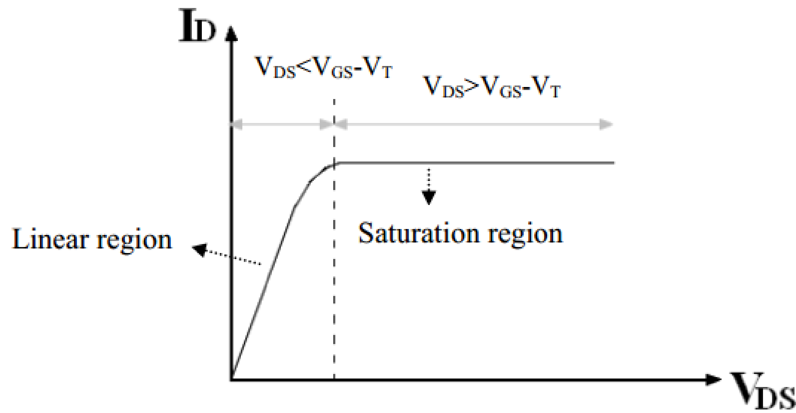

Figure 2.3: Current-Voltage characteristic of a generic transistor.

2.4. *Electrical Parameter Extraction*

In order to understand and design a circuit using IGZO TFTs, especially one that intents to be temperature invariant, it is crucial to extract some major electrical parameters. In this subchapter some methods describe how to calculate the threshold voltage, the electron's mobility, the capacitance per unit area and how they are related to the current-voltage characteristic.

2.4.1. Threshold Voltage

The threshold voltage is the parameter that dictates the state of the transistor, as being the minimum voltage applied to the gate that forms a conducting path between the source and drain terminals (electrons travel backwards in relation to current's convention way).

The Linear Extrapolation Method in the Linear Region is the most known and simplest method to extract V_{Th}. It begins to powering the drain terminal to a power supply, as said in chapter 2.3, and leaving the source terminal connected to the ground. However, the drain voltage has to be very small, in order to minimize the voltage-drop in the contact-resistors, as well as short channel effects. The next step is to power the gate terminal, varying it from 0 V to V_{DD}, in small

increments, e.g., 1 V or less, depending on the technology, and trace the respective V_{GS}-I_{DS} characteristic. When V_{GS} is high enough, electrons start to flow through the conducting path and I_D starts to grow exponentially until a saturation region is reached, where the increase of V_{GS} no longer affects the drain to source current value.

Once the *I-V* characteristic is obtained, the threshold voltage is found at the intercept of the tangent in the inflexion point with the V_{GS} axis, as in figure 2.4. The inflexion point is given by the maximum of the transconductance of the transistor [7].

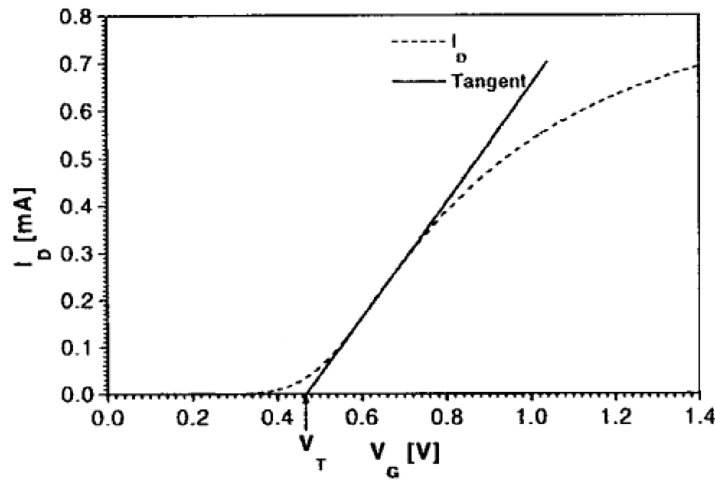

Figure 2.4: V_{Th} extraction, using Linear Extrapolation Method. Note: V_{Th} is expressed as V_T [7].

The expression of the drain curve in the linear region can be written as follows:

$$I_D = \frac{W}{L}\mu C_{ox}\left[V_{DS}(V_{GS} - V_{Th}) - \frac{{V_{DS}}^2}{2}\right] \quad (A) \qquad (2.1)$$

Where W and L are the transistor's width and length, respectively, μ is the electron's mobility and C_{ox} the capacitance per unit area.

2.4.2. Charge Carrier Mobility

Charge carrier mobility defines how fast an electron can move in the semiconductor channel when pulled by an electric field. In the particular case of TFTs, this can be called electron mobility and it is the parameter that outrages a-Si technologies, which have 20 to 50 less carrier mobility.

Its extraction is calculated by plotting the square root of drain current as a function of the gate voltage. The value of μ is the result of the slope of the respective curve, μ_{SAT} [3][8].

$$\mu = \mu_{Sat} = m_{Sat}^2 . \frac{2. L}{W. C_{OX}} \quad \left(\frac{cm^2}{V.s}\right) \tag{2.2}$$

Another method used for calculating the electron mobility is from the slope of the linear region of the drain current, μ_{Lin}, against V_{GS} curve, when a small drain to source bias V_{DS} is applied [3].

$$\mu = \mu_{Lin} = m_{Lin} . \frac{L}{W. C_{OX}} \quad \left(\frac{cm^2}{V.s}\right) \tag{2.3}$$

However, mobility may be influenced by several factors, such as energy, interface charge density, process conditions, dielectric material selection, and others [3][9][10].

2.4.3. Capacitance per unit area

There are two main methodologies to extract the capacitance per unit area, or C_{ox}. One of them just uses equation (2.4), which needs to know, in advance, the exact values of the relative permittivity and of the oxide thickness, ε_r and τ_{ox}, respectively. ε_r is a specific value for each material, e.g., 3.9 for silicon oxide as dielectric layer [11] and 14 for Ta_2O_5 or a multilayer dielectric, both used in this work.

$$C_{ox} = \frac{\varepsilon_{ox}}{\tau_{ox}} = \frac{\varepsilon_0 . \varepsilon_r}{\tau_{ox}} \quad \left(\frac{F}{cm^2}\right) \tag{2.4}$$

ε_0 is vacuum permittivity and it is equals to 8.854x10^{-12} F.m^{-1}.

Assuming the transistor is active, or in saturation region, C_{ox} can be calculated also by the slope of the accumulation charge density as a function of the applied gate voltage, or *Q-V* characteristic [12]. Figure 2.5 shows the charge density as a function of the applied gate voltage.

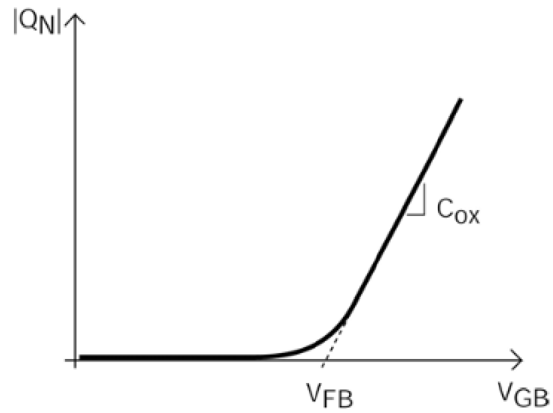

Figure 2.5: Accumulation charge density as a function of the applied gate voltage [12].

V_{FB}, or flat-band voltage, is the voltage at which there is no charge on the plates of the capacitor, hence there is no electric field across the oxide [12].

3

Low-Voltage Reference Topologies

3.1. Introduction

In order to achieve the proposed objective of designing a voltage reference, it is necessary to understand its basics and what it is for. In third chapter a very widely used voltage reference named Bandgap Voltage Reference, or BGR, is presented, which is a robust temperature independent voltage reference circuit that produces a fixed and constant voltage regardless of power supply variations, temperature changes and circuit loading from a device. Several topologies are shown and explained on the following subchapters, including the basic BGR used on low-voltage circuits, a low-voltage CMOS BGR based on partial compensation of MOSFET threshold voltage and mobility using current subtraction, which serves as base for this work, and a BGR with all TFT devices on glass substrate.

3.2. Bandgap Reference Circuit

The basic principle of all temperature-independent bandgap voltage references is to sum two different internal voltage sources which one is proportional to the absolute temperature, or PTAT, and the other is complementary to the ab-

solute temperature, or CTAT. By summing the two together, the temperature dependence can be cancelled. Graphical generic representations of a PTAT and CTAT characteristics are presented in figures 3.1. a) and 3.1. b), respectively.

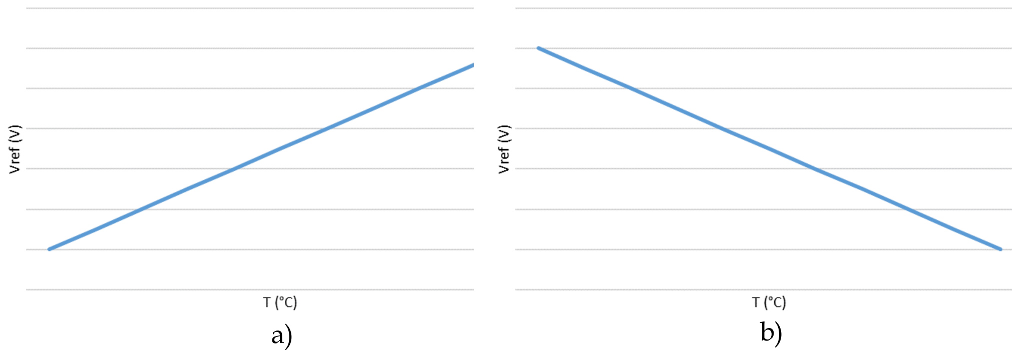

Figure 3.1: Generic representations of: a) PTAT reference; b) CTAT reference.

In a theoretical way, if two voltage sources are, one PTAT and other CTAT, it means that one has a negative slope over temperature, meaning that the value of the characteristic being measured is dropping over temperature, and the other is the exact opposite. As the absolute value of the slopes is different, it is necessary to have some degree of manipulation of, at least, one of them, in order to cancel the temperature dependence. E.g., some topologies use transistors with different sizes and others use different resistor values.

Generically, a simple voltage reference bandgap circuit has to satisfy the following equations:

$$V_{REF} = c_1 V_1 + c_2 V_2 \tag{3.1}$$

$$\frac{\partial V_{REF}}{\partial T} = c_1 \frac{\partial V_1}{\partial T} + c_2 \frac{\partial V_2}{\partial T} = 0, \tag{3.2}$$

where V_1 and V_2 are either CTAT and PTAT voltages, and c_1 and c_2 are values that have to be dimensioned to accomplish Eq. (3.2). The referred equation is said to be null to accomplish temperature independence; it sums the slope of the PTAT voltage with the CTAT voltage and c_1 and c_2 are constants, such as the width of the transistors, to compensate the overall dependence.

$$If\ c_1, c_2 > 0, \begin{cases} \dfrac{\partial V_1}{\partial T} < 0: Negative\ Temperature\ Coefficient\ (CTAT) \\ \dfrac{\partial V_2}{\partial T} > 0: Positive\ Temperature\ Coefficient\ (PTAT) \end{cases}$$

It has to be considered that, since this is a very basic bandgap reference introduction, only the linear effects of temperature dependence are taken in consideration.

A couple of examples are presented below using bipolar junction transistors, or BJT, since they are very simple and have interesting characteristics over temperature in this kind of applications.

Figure 3.2 shows a very simple bandgap circuit, where the supply voltage generates a current I_1, that flows over the transistor T_1. As T_1 is in diode configuration, I_1 flows through its base forcing it to be in the active region and producing a base-emitter voltage V_{BE}, which is one of the inputs of the adder. A BJT, as any other *p-n* junction device, exhibits a CTAT base-emitter voltage. On the other hand, the thermal voltage of the transistor, V_T (=kT/q), is PTAT, thus it can be connected to the other input of the adder.

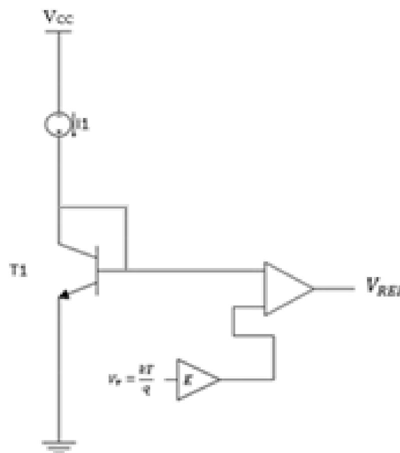

Figure 3.2: Simple BGR circuit.

The output voltage of the circuit is then shown in Eq. (3.3):

$$V_{REF} = V_{BE} + kV_T. \tag{3.3}$$

Another simple example of a BGR, this time using two BJTs with different emitter areas is shown below, i.e., figure 3.3. It generates a voltage proportional

to the absolute temperature where V_{BE1} and V_{BE2} have opposite temperature coefficients and where the supply voltage V_{CC} is converted to currents I_1 and I_2 that are then mirrored to the output branch [13].

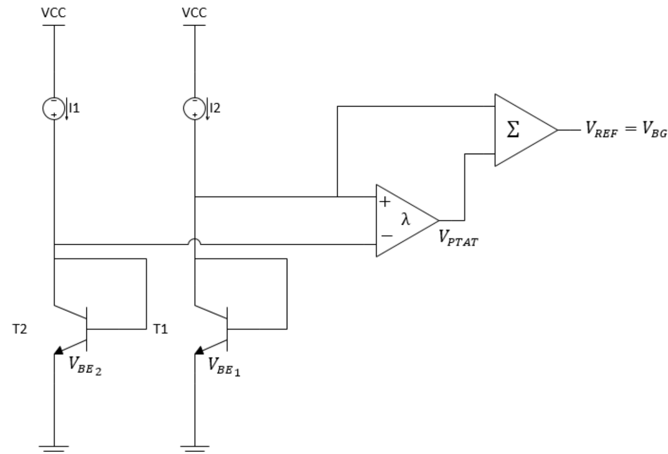

Figure 3.3: Simple BGR circuit, with two NPN transistors in diode-configuration with different widths.

The output voltage equation of the example described above is:

$$V_{REF} = V_{BE1} + \lambda(V_{BE1} - V_{BE2}), \tag{3.4}$$

where λ is the scale factor, V_{BE1} is the base-emitter voltage of the larger transistor and V_{BE2} is the base-emitter voltage of the second transistor [13].

3.3. A Low-Voltage CMOS Voltage Reference Based On Partial Compensation of MOSFET Threshold Voltage and Mobility Using Current Subtraction

The method to generate a temperature-independent voltage reference described in chapter 3.3. serves as base for the development of the present work. Therefore, it is imperative to understand the working principles of the circuits reported by Dong and Allen [14], and Toledo, Dualibe and Canali [1], in order to be able to port and adapt them from CMOS to TFT technology.

As the circuit reported by [14] is just one of the operating parts of the circuit reported by [1], it is the first to be explained and it is present in figure 3.4.

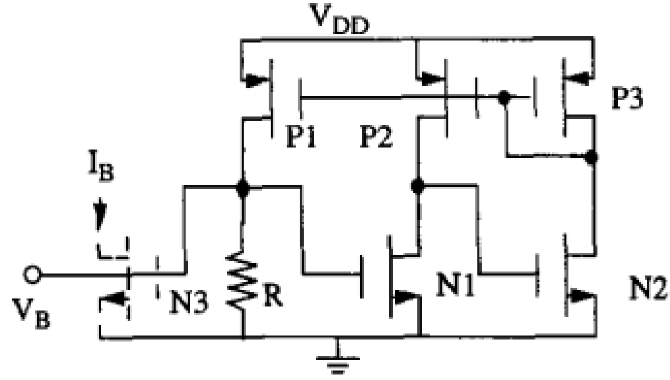

Figure 3.4: CMOS bias circuit reported by [14].

The first characteristic to be noticed however, is that it is a low power circuit, since the minimum possible supply voltage V_{DD} has to be V_T+2V_{DSAT}. It generates a supply independent threshold-referenced bias voltage, V_B, relative to the ground. The dotted transistor *N3* shows how the bias voltage V_B is used to generate a supply-independent bias current I_B [14].

Transistors *P2* and *P3* are PMOS and form a current mirror, as well as *P1*. Therefore, the currents on each of the three branches can be adjusted by choosing different transistor sizes, such as increasing or decreasing *W*, or width of each transistor, assuming a fixed *L*, or length; e.g. if *P1* is considered to have a reference drain-current and if it forms a current-mirror with *P3*, the current that flows on *P3* is adjusted by its parameter *W*. Assuming that *P1* and *P3* are ideal transistors, adjusting the ratio of *W* of the two, multiples of the reference current can be generated.

$$I_{P3} = I_{P1} \frac{\left(\frac{W}{L}\right)_{P3}}{\left(\frac{W}{L}\right)_{P1}}, \tag{3.5}$$

where I_{P1} and I_{P3} are the drain-currents across *P1* and *P3*, respectively.

Transistors *N1*, *N2*, *P3* and *P1* form a negative feedback path, which means that the current flowing on the resistor doesn't change. If the current of the resistor *R* changes, the negative feedback opposed this change to keep the current

constant. Equations (3.6) and (3.7) show the bias voltage V_B, and the resistor current, I_R, respectively [14]:

$$V_B = V_T + V_{DSatN1} \tag{3.6}$$

$$I_R = \frac{V_T + V_{DSatN1}}{R} \tag{3.7}$$

However, *N2*, *P3* and *P2* form a positive feedback path, but for stability purposes, the resulting feedback of the entire circuit, including *N1*, *N2*, *P3*, *P2* and *P1* should be negative, just as justified above; e.g. *P1* and *P2* form a current-mirror, so if the drain-current increases in *P1*, it will increase in *P2*:

$$I_{P2} = \frac{\left(\frac{W}{L}\right)_{P2}}{\left(\frac{W}{L}\right)_{P1}}.I_{P1} \tag{3.8}$$

$$\Delta I_{P2} = \frac{\left(\frac{W}{L}\right)_{P2}}{\left(\frac{W}{L}\right)_{P1}}.\Delta I_{P1} \tag{3.9}$$

Thus, the drain-current of the transistor *N1* will have the same behavior of *P2* and its variation has a small-sign relation of:

$$\Delta I_{N1} = \Delta I_{P1}.R.g_{m_{N1}}, \tag{3.10}$$

where g_{mN1} is the transconductance of the transistor *N1*, and:

$$R = \frac{V_T + V_{DSatN1}}{I_{P1}} \tag{3.11}$$

$$g_{m_{N1}} = \frac{2I_{N1}}{V_{DSatN1}} = \frac{2I_{P2}}{V_{DSatN1}} = \frac{2\frac{\left(\frac{W}{L}\right)_{P2}}{\left(\frac{W}{L}\right)_{P1}}.I_{P1}}{V_{DSatN1}}. \tag{3.12}$$

Equation (3.10) is now:

$$\begin{aligned} \Delta I_{N1} &= 2\frac{\left(\frac{W}{L}\right)_{P2}}{\left(\frac{W}{L}\right)_{P1}}.\Delta I_{P1}.\left(1+\frac{V_T}{V_{DSatN1}}\right) \\ &= 2.\Delta I_{P2}.\left(1+\frac{V_T}{V_{DSatN1}}\right) \\ &> \Delta I_{P2}\ , \end{aligned} \tag{3.13}$$

which means that the drain voltage of *N1* and the gate voltage of *N2* will decrease, then the currents of *N2*, *P3*, *P2* and *P1* will decrease. Therefore, the resulting feedback of *N1*, *N2*, *P3*, *P2* and *P1* is negative [14].

The effect of the supply-voltage variations is the same as that of the current variations of *P1* and *P2*. Supposing that V_{DD} increases, if the gate-to-source voltages of *N1* and *N2* keep constant, the drain-to-source voltages of *P1*, *P2* and *N2* will increase, and then the drain currents of *N2*, *P3* and *P1* will increase. On the other hand, if the gate-to-source voltages of *N1* and *N2* increase, the drain currents of *N1*, *N2*, *P3* and *P1* will also increase. The same analysis as for the drain-current increase of *P1* and *P2*, which is illustrated above, from equation (3.8) to equation (3.13), can be used to show that the current will remain constant [14].

Nevertheless, the circuit reported by [14] still suffers from inadequate sensibility to temperature variations and cannot be used as such, i.e. as an accurate voltage reference [1][15]. Therefore, a new architecture is proposed [1], based on BGR method, as seen in figure 3.5.

Citing [1], if two electrical magnitudes having the same temperature behavior, either PTAT or CTAT, but with slightly different coefficients are subtracted, the resulting magnitude holds a TC close to zero. Those two quantities, voltages or currents, should also be supply independents. So, a BGR methodology is applied. The described concept is shown in figure 3.5 and it will be mathematically analyzed.

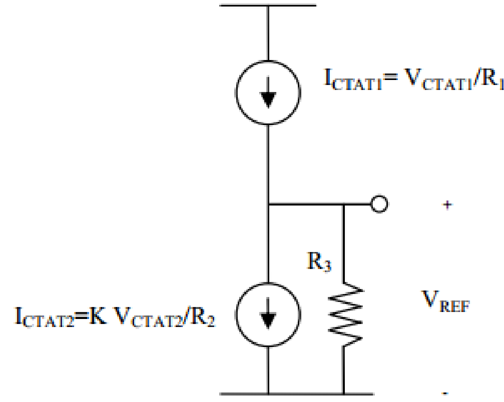

Figure 3.5: Currents subtraction scheme, reported by [1].

By direct inspection, using Kirchhoff's Current Law, or KCL, which states that the sum of all the input and output currents is equal to zero, the equation that dictates V_{REF} is calculated as follows, using the node between I_{CTAT1} and I_{CTAT2}:

$$I_{CTAT1} = I_{CTAT2} + \frac{V_{REF}}{R_3}$$
$$\Leftrightarrow V_{REF} = (I_{CTAT1} - I_{CTAT2})R_3$$
$$\Leftrightarrow V_{REF} = \left(\frac{V_{CTAT1}}{R_1} - K\frac{V_{CTAT2}}{R_2}\right)R_3$$
$$\Leftrightarrow V_{REF} = \frac{R_3}{R_1}\left(V_{CTAT1} - K\frac{R_1}{R_2}V_{CTAT2}\right) \tag{3.14}$$

Thus, the value of V_{REF} is entirely dependent on the ratios between R_3 and R_1, and R_1 and R_2. A value of K has to be considered, because the output voltage of the overall circuit, V_{REF}, present in figure 3.6 as V_O, is the voltage-drop across transistor T_7, which is, in turn, connected to T_8, which makes part of a current-mirror generator. The expression of K is then:

$$K = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_8} \tag{3.15}$$

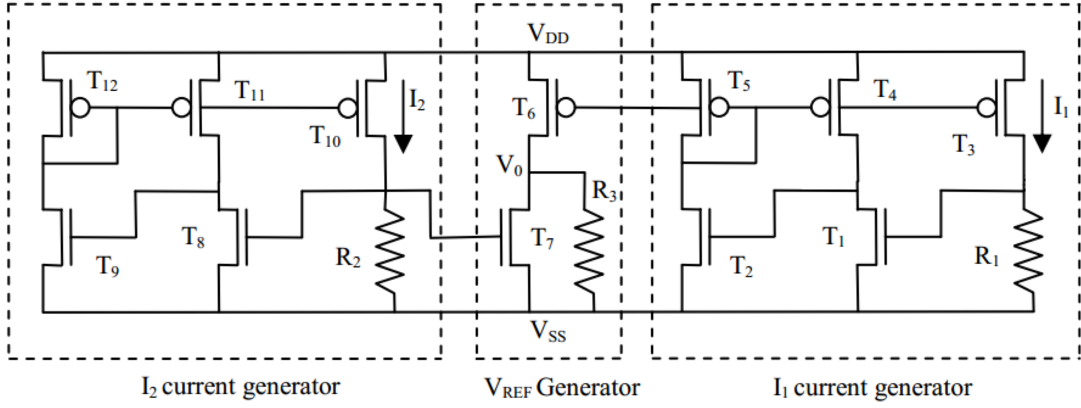

Figure 3.6: Proposed voltage reference reported by [1].

Note that the I_1 and I_2 current generators are the circuits explained in the beginning of this chapter.

The next step, after understanding how the resistors R_1, R_2 and R_3 influence the output voltage, is to guarantee that this value doesn't change with temperature. Thus, the partial derivative of V_{REF} in temperature should be zero.

$$\frac{\partial V_{REF}}{\partial T} = \frac{R_3}{R_1}\left(\frac{\partial V_{CTAT1}}{\partial T} - K\frac{R_1}{R_2}\frac{\partial V_{CTAT2}}{\partial T}\right) = 0 \tag{3.16}$$

It has to be noticed too that R_1, R_2 and R_3 are not considered to be ideal resistors but, as they are fractions, and the temperature dependences between R_3 and R_1, and R_1 and R_2, are fractions too, they cancel out. To verify the condition of equation (3.16), the absolute value in brackets must be zero, which gives the following relation between R_1 and R_2:

$$\frac{\partial V_{CTAT1}}{\partial T} - K\frac{R_1}{R_2}\frac{\partial V_{CTAT2}}{\partial T} = 0$$

$$\Leftrightarrow \frac{\frac{\partial V_{CTAT1}}{\partial T}}{\frac{\partial V_{CTAT2}}{\partial T}} = K\frac{R_1}{R_2} \tag{3.17}$$

It can be concluded that the ratio between R_1 and R_2 should be as such as it cancels the TC differences between V_{CTAT1} and V_{CTAT2}, whereas the ratio between R_3 and R_1 sets the reference voltage to a desired level. Since both relations share the same resistor R_1, it can be predicted, at this point, that there is a specific point

that correlates the three and achieves the optimum balance, from a thermal point of view.

Attending to the proposed voltage reference circuit, as it uses a current subtraction scheme, currents I_1 and I_2 are modulated according to R_1 and R_2 values. They can be seen as potentiometers. Each one of I_1 and I_2 current generators have two different currents, with different magnitude and temperature coefficients. One current is subtracted from the other with a proper scale factor and the resulting current goes through a resistor in order to provide a voltage reference with an almost null TC [1].

All NMOS and PMOS transistors of the proposed circuit operate in strong inversion, thus I_1 and I_2 currents can be obtained through the current expressions of T_3 and T_{10}, respectively. In order to simplicity this explanation, only I_1 expressions is present below, since I_2 is generated by the exact same circuit.

$$I_1 = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_1 \left(V_{GS} - V_{Th_N}\right)^2$$

$$\Leftrightarrow \left(V_{GS} - V_{Th_N}\right)^2 = \frac{2I_1}{\mu_n C_{OX}\left(\frac{W}{L}\right)_1}$$

$$\Leftrightarrow V_{GS} - V_{Th_N} = \sqrt{\frac{2I_1}{\mu_n C_{OX}\left(\frac{W}{L}\right)_1}} \quad , \quad V_{GS} = R_1 I_1$$

$$\Leftrightarrow R_1 I_1 - \sqrt{\frac{2I_1}{\mu_n C_{OX}\left(\frac{W}{L}\right)_1}} - V_{Th_N} = 0$$

$$\Leftrightarrow I_1 = \frac{V_{Th_N}}{R_1} + \frac{1 + \sqrt{1 + 2R_1.V_{Th_N}.\mu_n C_{OX}.\left(\frac{W}{L}\right)_1}}{\mu_n C_{OX}.\left(\frac{W}{L}\right)_1 .{R_1}^2} \tag{3.18}$$

Equation (3.18) demonstrates that I_1, and so I_2, depend on the values of R_1, and so R_2, respectively, as well as the ratios $(W/L)_1$ and $(W/L)_2$. However, from Ohm's law, I_1 is the quotient between V_{CTAT1} and R_1, so V_{CTAT1} is:

$$V_{CTAT1} = V_{Th_N} + \frac{1 + \sqrt{1 + 2R_1.V_{Th_N}.\mu_n C_{OX}.\left(\frac{W}{L}\right)_1}}{\mu_n C_{OX}.\left(\frac{W}{L}\right)_1 .R_1} \tag{3.19}$$

Since the objective of this method is to cancel the TC using current subtraction, equation (3.19) must be differentiated in temperature. It will then give the variation of the output voltage of I_1 current generator, as well as the variation of the output voltage of the I_2 current generator. Both equations are, respectively, equations (3.20) and (3.21).

$$\frac{\partial V_{CTAT1}}{\partial T} = V_{Th_N}\left(\frac{1}{V_{Th_N}}\frac{\partial V_{Th_N}}{\partial T} + \frac{\frac{1}{V_{Th_N}}\frac{\partial V_{Th_N}}{\partial T} + \frac{1}{R_1}\frac{\partial R_1}{\partial T} + \frac{1}{\mu_N}\frac{\partial \mu_N}{\partial T}}{\sqrt{1 + 2R_1 . V_{Th_N} . \mu_n C_{OX} . \left(\frac{W}{L}\right)_1}}\right) + \frac{1 + \sqrt{1 + 2R_1 . V_{Th_N} . \mu_n C_{OX} . \left(\frac{W}{L}\right)_1}}{\mu_n C_{OX} . \left(\frac{W}{L}\right)_1 . R_1}\left(-\frac{1}{\mu_N}\frac{\partial \mu_N}{\partial T} - \frac{1}{R_1}\frac{\partial R_1}{\partial T}\right) \tag{3.20}$$

$$\frac{\partial V_{CTAT2}}{\partial T} = V_{Th_P}\left(\frac{1}{V_{Th_P}}\frac{\partial V_{Th_P}}{\partial T} + \frac{\frac{1}{V_{Th_P}}\frac{\partial V_{Th_P}}{\partial T} + \frac{1}{R_2}\frac{\partial R_2}{\partial T} + \frac{1}{\mu_P}\frac{\partial \mu_P}{\partial T}}{\sqrt{1 + 2R_2 . V_{Th_P} . \mu_P C_{OX} . \left(\frac{W}{L}\right)_2}}\right) + \frac{1 + \sqrt{1 + 2R_2 . V_{Th_P} . \mu_P C_{OX} . \left(\frac{W}{L}\right)_2}}{\mu_P C_{OX} . \left(\frac{W}{L}\right)_2 . R_2}\left(-\frac{1}{\mu_P}\frac{\partial \mu_P}{\partial T} - \frac{1}{R_2}\frac{\partial R_2}{\partial T}\right) \tag{3.21}$$

Two equations are needed, for two current generators. Equation (3.20) shows the behavior of one half of the entire circuit, whereas equation (3.21) the other half. It has to be noticed that equation (3.20) only uses the characteristics of the NMOS transistors, while equation (3.21) uses PMOS's, given the fact that both currents I_1 and I_2 are mirrored into the transistors T_6 and T_7.

$$I_{T_6} = I_1 \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_3} \tag{3.22}$$

$$I_{T_7} = I_2 \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_8} \tag{3.23}$$

The key elements to develop this topology are, first of all, to understand how the CMOS bias circuit presented initially works, theoretically and by simulation; to choose two currents, I_1 and I_2, according to the technology used and then calculate the respective values of the resistors and finally, a simple device scaling has to be considered, because the size of the transistor T_7 significantly

influences the output behavior of the overall circuit, since it is responsible for driving the most significant part of the output current.

3.4. Design of a Bandgap Voltage Reference Circuit with all TFT Devices on Glass Substrate in a 3 µm LTPS Process

Since there is a lack of voltage reference topologies that use TFT devices, another design is introduced which can probably be implemented with IGZO TFTs, given the fact that they are both n-type transistors and both use 10 V power supplies, as well as the ones that can be used in glass applications.

As seen in subchapter 3.2., the conventional BGR uses Bipolar Junction Transistors, of BJTs, and other topologies use diodes instead, or BJTs connected in diode configurations [16], [17]. Knowing that these have negative temperature coefficients, or TCs, the main idea is to use the temperature-dependent voltage-drop across the diode-connected BJTs to modulate and stabilize the output voltage, through a positive TC, generated by a proper circuit design. The incorporation of BJTs into CMOS technology somehow makes the process control difficult. Therefore, it was also considered using only MOSFETs in the BGR circuit to simplify the process and to reduce the operating voltage/power. The voltage across MOSFETs is sensitive to temperature only when the MOSFETs are biased in the subthreshold region. The gate-to-source voltage of MOSFETs in sub-threshold region is strongly dependent on temperature and exhibits a negative temperature coefficient [18].

The conventional BGR circuit incorporated with BJTs or diodes is a great challenge for the LTPS process since the characteristics of the poly-Si BJTs or the poly-Si diodes are still unknown or lack reliable control. The use of LTPS TFT devices biased in the sub-threshold region is also not practical because the poly-Si TFT devices often suffer from significant threshold voltage variation. However, the *I-V* characteristics of LTPS TFT devices have been found to be strongly dependent on temperature when the devices are operated in the saturation region [18]–[20].

A traditional implementation of bandgap voltage reference circuit in CMOS technology is shown in figure 3.7. In this circuit, the output voltage, V_{REF}, is the

sum of a base-emitter voltage, V_{EB}, of BJT Q_3 and the voltage-drops across the upper resistor R_2. The BJTs, Q_1, Q_2, and Q_3, are typically implemented by the diode-connected parasitic vertical PNP bipolar junction transistors in the CMOS process with the current proportional to $exp\ (V_{EB}/V_T)$, where V_T ($=kT/q$) is the thermal voltage. Under constant current bias, V_{EB} is strongly dependent on V_T, as well as on temperature. The current mirror, formed by M_1, M_2, and M_3, is designed to bias Q_1, Q_2, and Q_3 with identical current. Then, the voltage drop on the resistor R_1 can be expressed by equation (3.24) [18]:

$$V_{R1} = V_T\, ln\left(\frac{A_1}{A_2}\right) \tag{3.24}$$

where A_1 and A_2 are the emitter areas of Q_1 and Q_2. It is noted that V_{R1} exhibits a positive temperature coefficient when A_1 is larger than A_2. Besides, since the current which flows through R_1 is equal to the current which flows through R_2, the output voltage of the traditional bandgap voltage reference circuit can be written as [18]:

$$V_{REF} = V_{EB3} + \frac{R_2}{R_1} V_T\, ln\left(\frac{A_1}{A_2}\right) \tag{3.25}$$

The second item in equation (3.25) is proportional to the absolute temperature, PTAT, which is used to compensate the negative temperature coefficient of V_{EB3}. In general, the PTAT voltage comes from the thermal voltage, which is quite smaller than that of V_{EB}. After multiplying the PTAT voltage with an appropriate factor, R_2/R_1, and summing with V_{EB}, the output voltage V_{REF} of bandgap reference circuit can result in very low sensitivity to temperature [18].

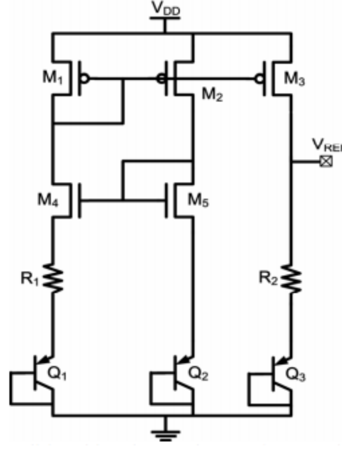

Figure 3.7: The traditional bandgap voltage reference circuit realized in CMOS technology with parasitic vertical PNP bipolar junction transistors [18].

For LTPS TFT devices, the drain current I_{DS} of devices operating in the saturation region can be expressed as [21]:

$$I_{DS} = \frac{W}{2L}\mu_0 C_{ox}(V_{GS} - V_{TH})^2 e^{\left(-\frac{V_B}{V_T}\right)} \tag{3.26}$$

where μ_0 is the carrier mobility within the drain, L denotes the effective channel length, W is the effective channel width, C_{ox} is the gate oxide capacitance per unit area, V_{Th} is the threshold voltage of TFT device, and V_{GS} is the gate-to-source voltage of TFT device. V_B is the potential barrier at grain boundaries which is associated with the crystallization quality of the poly-Si film [18]. Under small V_{GS}, V_B is large. When the V_{GS} increases, V_B decreases rapidly. When the devices are operated under small V_{GS}, it is found that the drain current I_{DS} of devices is dominated by the exponential term and can be estimated by [18]:

$$I_{DS} = W\alpha e^{\left(-\frac{V_B}{V_T}\right)}. \tag{3.27}$$

Where a is treated as a constant under small gate bias V_{GS}. Then, the equation for V_B can be derived as [18]:

$$V_B = V_T \, ln\left(\frac{W\alpha}{I_{DS}}\right) = \left(\frac{kT}{q}\right) ln\left(\frac{W\alpha}{I_{DS}}\right). \tag{3.28}$$

When there is a temperature variation ΔT, the corresponding variation of V_B is [18]:

$$\Delta V_B = \frac{k\Delta T}{T} \ln\left(\frac{W\alpha}{I_{DS}}\right). \tag{3.29}$$

From equation (3.29), it can be found that the temperature coefficient (TC) of V_B can be modulated by the channel width. The larger channel width gives rise to the larger TC of V_B [18].

The variation of V_B is related to the variation of V_{GS}. Assuming that the variation of V_{GS}, or ΔV_{GS}, is very small, a negative linear approximation can be given between ΔV_B and ΔV_{GS} as [18]:

$$\Delta V_{GS} = -\frac{1}{m}\Delta V_B = -\frac{k\Delta T}{mq} \ln\left(\frac{W\alpha}{I_{DS}}\right) = -\frac{\Delta V_B \Delta T}{m\Delta T}, \tag{3.30}$$

where m is the absolute value of the slope under linear approximation. The devices biased at small V_{GS} can exhibit a large V_B if its channel width is enlarged [18].

The channel width of M_6, or W_6, is larger than the channel width of M_7, or W_7, so the TC of $M6$ is more negative than the TC of M_7. The voltage-drop across the resistor R_1, V_{R1}, therefore exhibits a positive TC. If the dependence of m on V_{GS} is neglected, the variation of V_{R1}, ΔV_{R1}, as a function of ΔT can be expressed as [18]:

$$\Delta V_{R1} = \frac{k\Delta T}{mq} \ln\left(\frac{W_6}{W_7}\right) = \frac{k\Delta T}{mq} ln\, N. \tag{3.31}$$

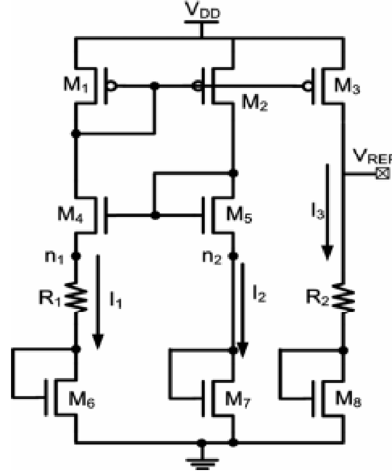

Figure 3.8: The implementation of the new proposed bandgap voltage reference circuit with all TFT devices in a LTPS process [18].

Obviously, ΔV_{R1} is proportional to the absolute temperature, or simply PTAT. Hence, a PTAT loop is formed by M_6, M_7, and R_1. The PTAT current variation ΔI_1 can be written as [18]:

$$\Delta I_1 = \frac{k\Delta T}{mqR_1}\ln N, \tag{3.32}$$

where N (=W_6/W_7) is the channel width ratio of M_6 and M_7, and V_T is the thermal voltage. The current mirror, which is composed of M_1, M_2, and M_3, imposes equal currents in these three branches I_1, I_2, and I_3 of the circuit. The output voltage, V_{REF}, is the sum of a gate-source voltage of TFT M_8, V_{GS8}, and the voltage-drop across the upper resistor V_{R2}. Therefore, the output voltage variation, ΔV_{REF}, of the new proposed bandgap reference circuit can be expressed as [18]:

$$\Delta V_{REF} = \Delta I_3 R_2 + \Delta V_{GS8} = \frac{R_2}{R_1}\frac{k\Delta T}{mq}\ln N + \Delta V_{GS8}\ , \tag{3.33}$$

where R_1 and R_2 are the resistors shown in figure 3.8. The first item in equation (3.33) with positive TC is proportional to the absolute temperature, PTAT, which is used to compensate the negative temperature coefficient of ΔV_{GS8}. After multiplying the PTAT voltage with an appropriate factor, which is the proper ratio between the resistors, and summing with ΔV_{GS8}, the output voltage of bandgap reference circuit can result in very low sensitivity to temperature [18].

3.5. Conclusions

Various methodologies can be used to generate a voltage reference that is temperature independent. This chapter presented the basics of what is a bandgap voltage reference, as well as a more sophisticated methodology that can be used in thin film transistors. Another non-bandgap was introduced, in chapter 3.4., which will be implemented further.

This type of voltage reference circuits can be widely used and it is imperative that they are well dimensioned, since there are some specific circuits that are very voltage reference dependent, such as data conversion systems, ADCs and DACs. The referred examples always use comparators with the voltage reference signal as input. Any kind of error on V_{REF} and it will compromise the output results of this kind of circuits, and others, affecting negatively the linearity or the spurious free dynamic range, or SFDR.

4

Design Methodology and Electrical Simulations using a standard 130 nm Technology

4.1. Introduction

Before starting the implementation and development of the project using, effectively TFTs, chapter 4 aims to explain how the process of generating a voltage reference is done using the method described in subchapter 3.3., now in a practical analysis. The technology in use is a generic and well known standard 130 nm.

The first step that must be done is to verify if all the characteristics of the needed equations are known, and if not, they have to be extracted by simulation from the circuit or the components themselves. These procedures are carefully defined and illustrated on the respective subchapters. The second step is to replace the unknown terms of the equations with the extracted or calculated values and observe the respective results; in the present case, it is done with a mathematical software tool, such as MathCAD, referred earlier, in chapter 1. At this stage, it is possible to have a first guess of values which corresponds to the order of magnitude of the resistors R_1 and R_2. The third and final step is to port the obtained values from MathCAD to Cadence's simulation tool and vary them until the primary objective is achieved, which is a compensated voltage reference with as minimal output voltage variation as possible.

4.2. Mathematical Analysis

To calculate the order of magnitude of the three major variables, a mathematical study is realized. Considering that the technology in question is a standard 130 nm, where some of the respective values are already known, the first step is to look to the needed equations and realize if there are any missing parameters.

Before a further analysis, table 4.1 exhibits all the parameters previously known of the mentioned technology, for NMOS and PMOS transistors, respectively, while table 4.2 presents the respective width and length transistor sizes.

Table 4.1: Technology Parameters.

	NMOS	**PMOS**
V_{DD} [V]	1.2	
V_{DSat} [mV]	100	
$\lvert V_{Th} \rvert$ [V]	0.38	0.33
$\mu.C_{ox}\left[\frac{\mu A}{V^2}\right]$	500	100

Table 4.2: Transistor Sizes.

	NMOS	**PMOS**
Width [μm]	10	10
Length [μm]	1	1

The value of V_{DD} is the supply voltage for this technology and V_{DSAT} is the drain-to-source saturation voltage of both transistors. As opposed to the experience realized in [1], the PMOS transistors are half of the size in this experimentation and the reason for that is that the final results for this technology serves as base for comparison with the TFT technology, which have the same *(W/L)* relation.

Observing equations (3.20) and (3.21), the differentials in temperature of V_{CTAT1} and V_{CTAT2} depend on non-ideal resistors, but since the main goal of this work is to design the circuit and produce the PCB with external resistors, they are considered as ideal components. Therefore,

$$\frac{1}{R_1}\frac{\partial R_1}{\partial T} = 0 \tag{4.1}$$

$$\frac{1}{R_2}\frac{\partial R_2}{\partial T} = 0 \tag{4.2}$$

The following lines are about the extraction of the threshold voltage of the NMOS and NMOS transistors, as well as the electron mobility. To extract these parameters, the transistors have to operate, in most cases, in the saturation region, so a gate voltage of 1 V is applied and the circuit is shown in figure 4.1.

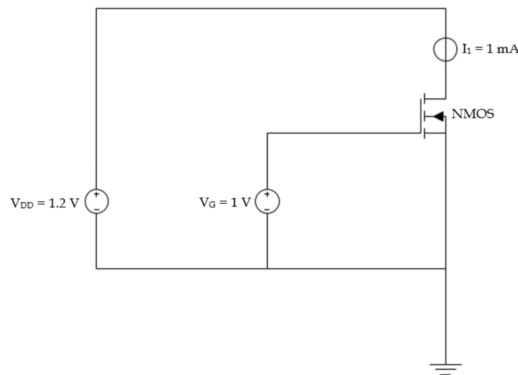

Figure 4.1: Circuit to extract the needed parameters of a NMOS transistor.

Since the variation of the threshold voltage of both NMOS and PMOS transistors is also unknown, a simulation is required to see how this parameter changes. If the resulting graph is approximately linear, then the variation can be easily calculated.

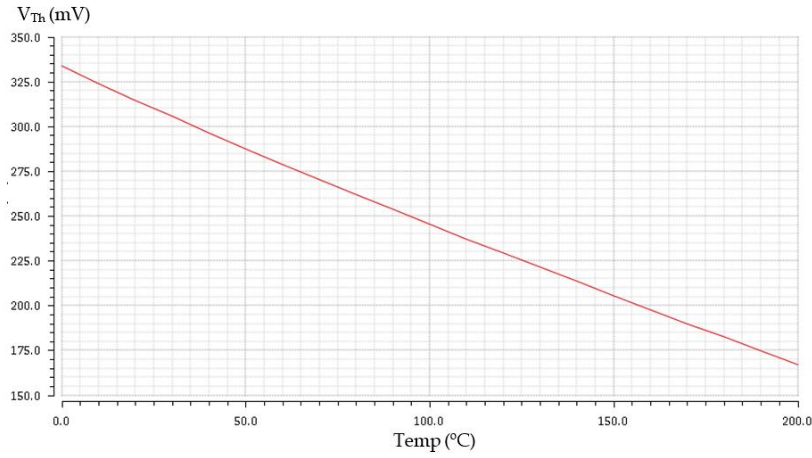

Figure 4.2: Simulation of V_{Th} over temperature of the NMOS transistor.

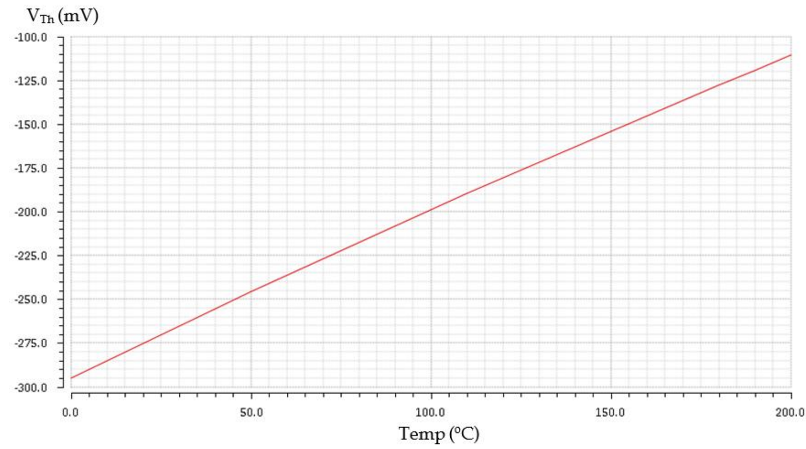

Figure 4.3: Simulation of V_{Th} over temperature of the PMOS transistor.

As both graphs are almost perfectly linear, a simple first order derivative can be made using two arbitrary points; see equation (4.3). The results are presented on table 4.3.

$$\frac{\partial V_{Th}}{\partial T} = \frac{\Delta V_{Th}}{\Delta T} = \frac{V_{Th}(T_2) - V_{Th}(T_1)}{T_2 - T_1} \quad , \quad T_2 > T_1 \tag{4.3}$$

Table 4.3: Threshold voltage variation over temperature of NMOS and PMOS transistors of a 130 nm technology.

	NMOS	**PMOS**
$\frac{\partial V_{Th}}{\partial T}\left[\frac{\mathrm{mV}}{\mathrm{K}}\right]$	-0.8	0.91(6)

The last step to be able to complete the missing terms of equations (3.20) and (3.21) is to find the respective variations of the electron's mobility, in order to temperature.

It is not possible to simulate the electron's mobility by software, so a workaround solution has to be found using the conduction parameter. From equation (3.18):

$$K_{N,P} = \frac{2I_D.L}{W.(V_{GS} - V_T)^2} \tag{4.4}$$

The simulations for NMOS and PMOS transistors are represented in figures 4.4 and 4.5, respectively.

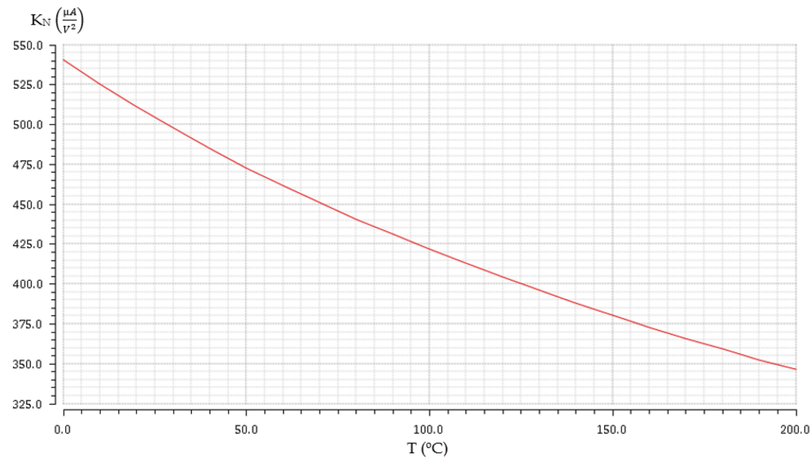

Figure 4.4: Simulation of K_N over temperature of the NMOS transistor.

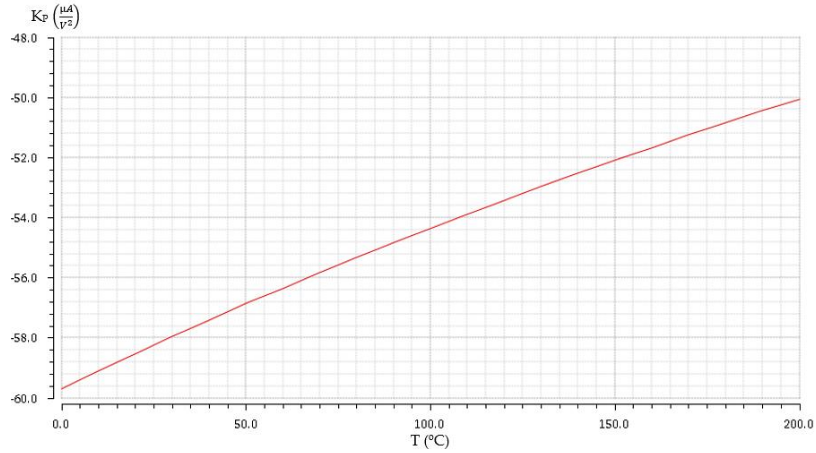

Figure 4.5: Simulation of K_P over temperature of the PMOS transistor.

Linear characteristics can be observed, therefore the same method used to calculate the threshold voltage, equation (4.3), can be applied once again. Table 4.4 shows the slopes of the graphs of figures 4.4 and 4.5 using a first order derivative.

Table 4.4: Conduction parameter variation over temperature of NMOS and PMOS transistors of a standard 130 nm technology.

	NMOS	**PMOS**
$\frac{\partial m_K}{\partial T}\left[\frac{\mu A}{V^2}/K\right]$	-0.594611	0.03917(7)

It is also known that:

$$K_{N,P} = \mu_{N,P}.C_{ox} \tag{4.5}$$

So,

$$\frac{\partial K_{N,P}}{\partial T} = \frac{\partial \mu_{N,P}}{\partial T}.C_{ox}$$

$$\Leftrightarrow \frac{\partial \mu_{N,P}}{\partial T} = \frac{\frac{\partial K_{N,P}}{\partial T}}{C_{ox}} \tag{4.6}$$

Assuming that the values of the capacitance per unit area are constant, then the final unknown values can now be calculated in order to demystify equations (3.20) and (3.21).

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_0 . \varepsilon_r}{t_{ox}} \tag{4.7}$$

The first value of the numerator of equation (4.7), ε_0, is the vacuum permittivity, which value is 8.854x10^{-14} F/cm, whereas ε_r is the relative permittivity. For this technology ε_r is 3.9.

Knowing that the software simulation tool returns values that are relatively close to real, the value of t_{ox} can be extracted from its libraries. The purpose of this is to acquire first guess values which are as trustworthy as possible. Table 4.5 shows the values of t_{ox} for each type of transistor.

Table 4.5: Thickness oxide parameters of NMOS and PMOS transistors of a 130 nm technology.

	NMOS	PMOS
t_{ox} [nm]	2.73	2.86

Equation (4.7) can now be calculated and then the effective values of the variation of the electron's electrical mobility over temperature can be extracted mathematically. Their values are shown on the following tables, 4.6 and 4.7, respectively.

Table 4.6: Capacitance per unit area of NMOS and PMOS transistors of a standard 130 nm technology.

	NMOS	PMOS
C_{ox} $\left[\frac{F}{cm^2}\right]$	1.265x10^{-6}	1.207x10^{-6}

Table 4.7: Electron's mobility over temperature of NMOS and PMOS transistors of a standard 130 nm technology.

	NMOS	PMOS
$\frac{\partial \mu}{\partial T}\left[\frac{cm^2}{V.s.K}\right]$	-0.47	0.032

At this point, it is possible to draw and analyze the two graphs that correspond to the behavior of V_{CTAT1} and V_{CTAT2}. According to the principle of the bandgap voltage reference, one graph should be PTAT, while the other CTAT, with different TCs. In figures 4.6 and 4.7 are plotted the equations (3.20) and (3.21), respectively, with different size relations, from 10 to 100.

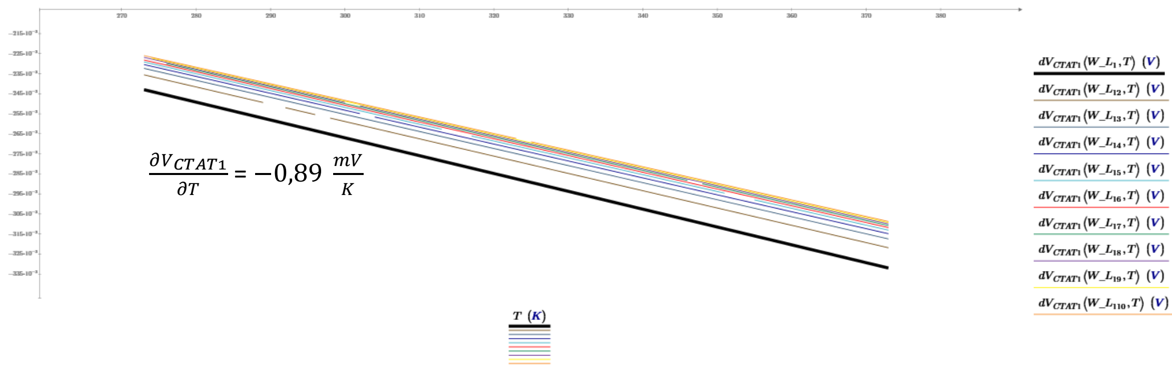

Figure 4.6: Temperature characteristics of V_{CTAT1}, from 273 K to 373 K. The black line represents the size relation *(W/L) = (10 µm/1 µm)*.

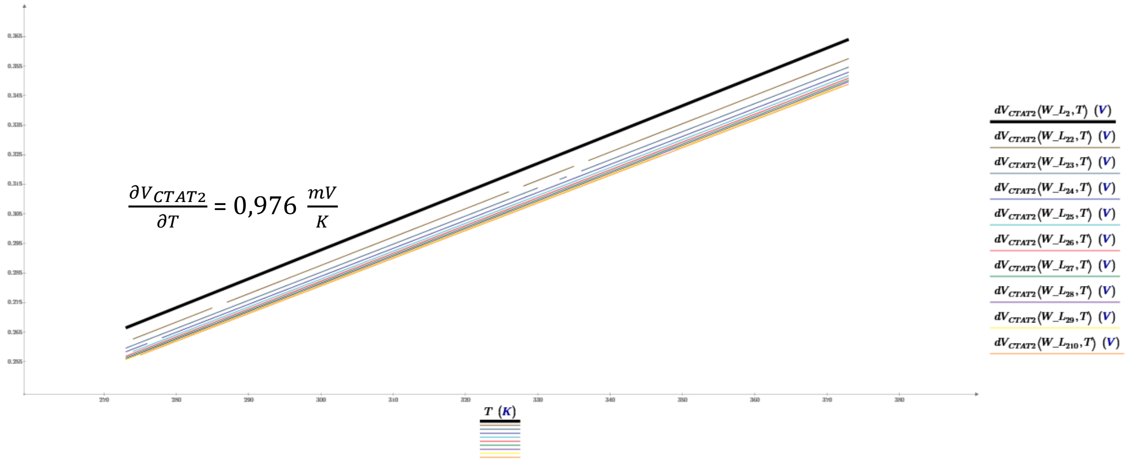

Figure 4.7: Temperature characteristics of V_{CTAT2}, from 273 K to 373 K. The black line represents the size relation *(W/L) = (10 μm/1 μm)*.

The voltage across the resistor R_1 starts in -243 mV, at 273 ºK, and decreases all the way to -332 mV, at 373 ºK, which is a variation of -0.89 mV/K; whereas the voltage across the resistor R_2 starts in 266 mV, at 273 ºK, and increases until 364 mV, at 373 ºK, which is a variation of 0.976 mV/K. The calculated slopes are in the same magnitude of values and are very close to each other. V_{CTAT1} and V_{CTAT2} are CTAT and PTAT, respectively, and their values are in the range of what is expected for this technology. Thus, this is the confirmation that all the previous calculations are correct and the first guess for the resistors can also be accomplished. Although, the values of V_{CTAT1} and V_{CTAT2} may differ when compared to the simulation results, since the simulation has several parameters, which are intrinsic to the technology, and are not considered in this analysis. However, it does not affect the final purpose of this step.

Since V_{CTAT1} and V_{CTAT2} are now known, theoretically it would be possible to cancel the TC of the circuit from equation (3.17):

$$\frac{-0.89\ \frac{mV}{K}}{0.976\ \frac{mV}{K}} = K\frac{R_1}{R_2}$$
$$\Leftrightarrow K\frac{R_1}{R_2} = -0.91 \tag{4.8}$$

Although, analyzing carefully article [1], the values of its resistors R_1 and R_2 are chosen according to the predefined currents I_1 and I_2, which are 10 μA and 1

μA, respectively. From Ohm's law, R_1 and R_2 are then 40 kΩ and 400 kΩ, respectively.

Using the same methodology and given that the present technology is similar to the technology used by [1], from equation (3.18) the values from the resistors used in this work are, coincidentally, the same. By successive mathematical simulations from (3.18) to achieve currents near to the referred numbers, the values of the resistors R_1 and R_2 are:

$$R_1 = 40\ k\Omega$$
$$R_2 = 400\ k\Omega$$

Which result in currents with values of:

$$I_1 = 11.171\ \mu A$$
$$I_2 = 0.933\ \mu A$$

The overall conclusions that can be taken from the theoretical and mathematical analysis are, essentially, that the resistors R_1 and R_2 vary in different scales, being R_2 around ten times greater than R_1. Nevertheless, more important than this is that the first resistor has a range of values that goes in tens of thousands and the second in hundreds of thousands of Ohms. Therefore, the values which each of the resistors will have on the next step of the project are now well known. Relative to resistor R_3, it is not taken in consideration because, from equations (3.14) and (3.16) it can be seen that it has no effect on canceling the TC of the circuit. Its only objective is to set the output voltage to a desired level. For this technology and considering all the previously presented values, if equation (3.14) is solved with an input range of R_3 varying from 50 kΩ to 100 kΩ, the output voltage results are, respectively, 0.605 V and 1.21 V. Then, theoretically, this voltage reference circuit should be able to feed effectively any low-voltage circuit downstream using, e.g., the same technology.

In appendix all the mathematical code used to generate the presented results is presented, from all variables and equations to the current and voltages results and graphs.

4.3. Simulation Results

This subchapter presents the results of the simulations from the previous analysis. Before the final circuit, namely figure 3.6, I_1 and I_2 current generators are isolated from each other in order to verify if the respective currents and voltages behaviors are in conformity with the previous results.

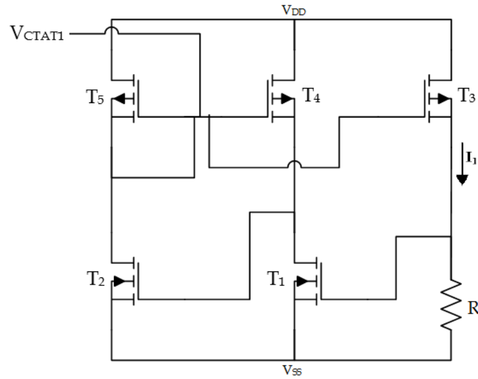

Figure 4.8: I_1 current generator.

From the previous analysis, V_{CTAT1} should be CTAT. However, the simulation shows that V_{CTAT1} has the opposite behavior, being PTAT. The main reason for this to happen should have to do with some signal change on equation (3.20). As this bandgap voltage reference is based on current subtraction, the essential is that both I_1 and I_2 are CTAT, so if one increases or decreases, the other does the same in a way that the respective subtraction cancels the TC. Figures 4.9 and 4.10 show the respective simulation results for V_{CTAT1} and I_1 for different resistor values.

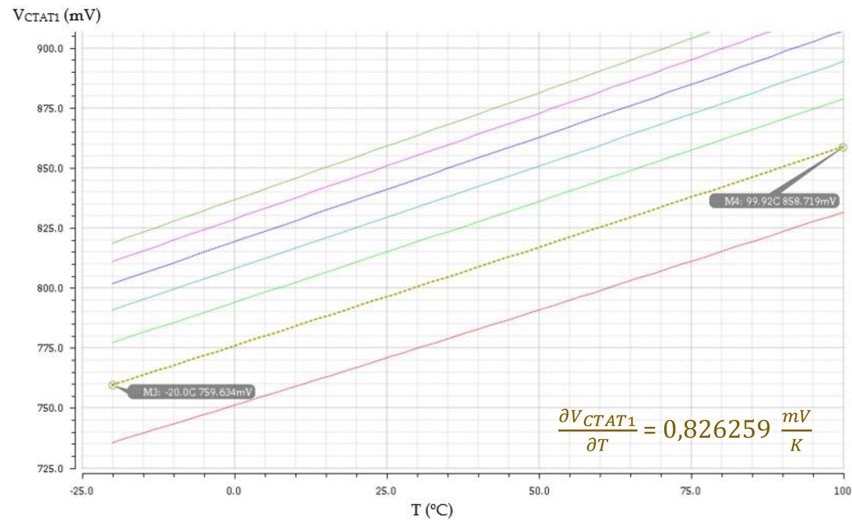

Figure 4.9: V_{CTAT1} voltage behavior for different values of R_1, in steps of 5 kΩ, from 20 kΩ to 50 kΩ. The yellow marked line represents the chosen value for R_1=*25 kΩ*.

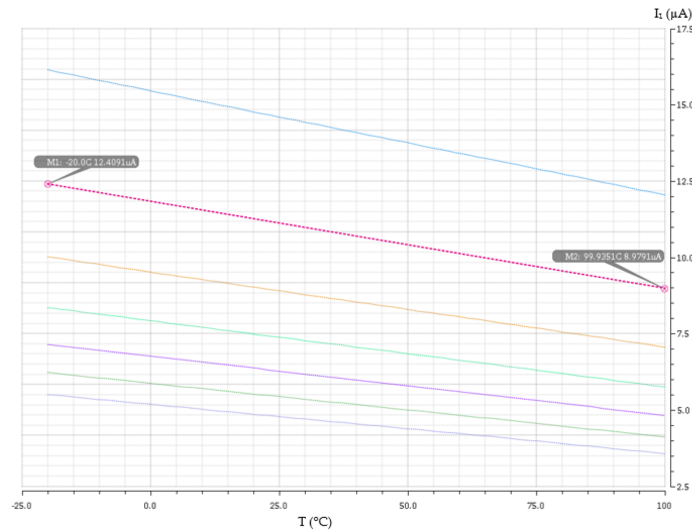

Figure 4.10: I_1 current behavior for different values of *R1*, in steps of 5 kΩ, from 20 kΩ to 50 kΩ. The pink marked line represents the chosen value for R_1=*25 kΩ*.

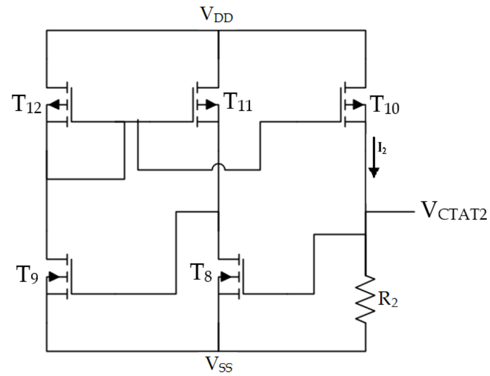

Figure 4.11: I_2 current generator.

As predicted, V_{CTAT2} is then CTAT, given the same probable signal change on equation (3.21), and I_2 is also CTAT, as it should. Figure 4.12 and 4.13 show the characteristics of V_{CTAT2} and I_2 over temperature.

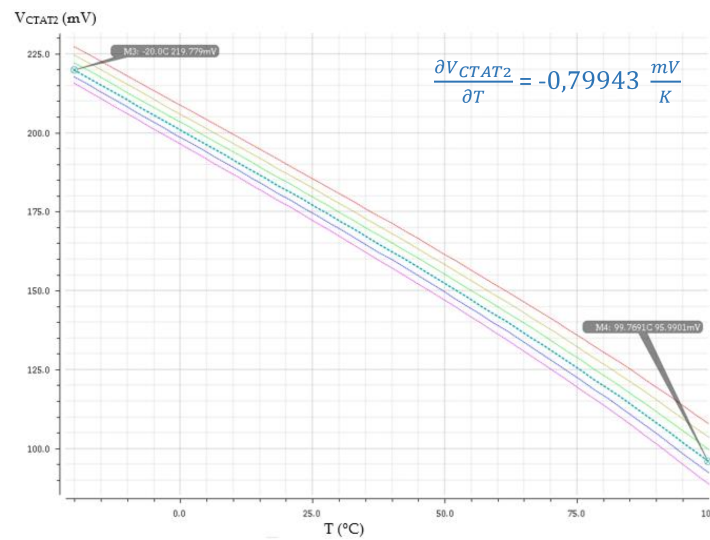

Figure 4.12: V_{CTAT2} voltage behavior for different values of R_2, in steps of 10 kΩ, from 150 kΩ to 200 kΩ. The blue marked line represents the chosen value for $R_2 = 180\ k\Omega$.

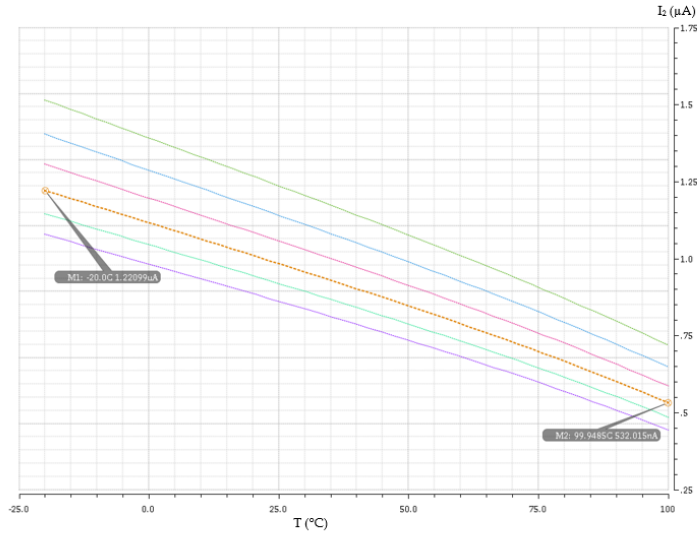

Figure 4.13: I_2 current behavior for different values of R_2, in steps of 10 kΩ, from 150 kΩ to 200 kΩ. The orange marked line represents the chosen value for $R_2=180\ k\Omega$.

The sizes of the resistors for each current generator vary in the proper order of magnitude calculated in subchapter 4.2. To maintain currents approximately equal to 10 µA and 1 µA, for I_1 and I_2, respectively, the final results used in this work for both of the resistors are:

$$R_1 = 25\ k\Omega$$
$$R_2 = 180\ k\Omega$$

To finalize the dimensioning of the overall circuit of figure 3.6, a last and sensible step is needed to achieve a compensated circuit over temperature, which is to find the proper scale factor for the transistor T_7.

Firstly, considering equation (4.8), after having the proper values of R_1 and R_2, its respective ratio results in:

$$\frac{R_1}{R_2} = 0{,}13(8)$$

Then, considering the absolute value of (4.8), since it is not possible to have a negative ratio between resistors and transistor sizes, the value of K is:

$$K.\,0{,}13(8) = 0{,}79943$$
$$\Leftrightarrow K = 5{,}7513$$

The given result means that T_7 should be five and a half times, approximately, bigger than T_8, so, if T_8 has a *(W/L)* relation of *(10 µm/1 µm)*, T_7, ideally, would have a width somewhere between 50 µm and 60 µm, keeping the length of all the transistors the same.

Carrying this order of values to the simulation software, it is verified that the ideal number which makes the circuit work, with a minimal impact of temperature is 47 µm, for the width parameter, which is, once again, in the same range of the predicted values; on the other hand, the value of *K* is, approximately, 4,7. The graph of the mentioned results can be observed in figure 4.14.

$$\left(\frac{W}{L}\right)_7 = 47\ \mu m$$

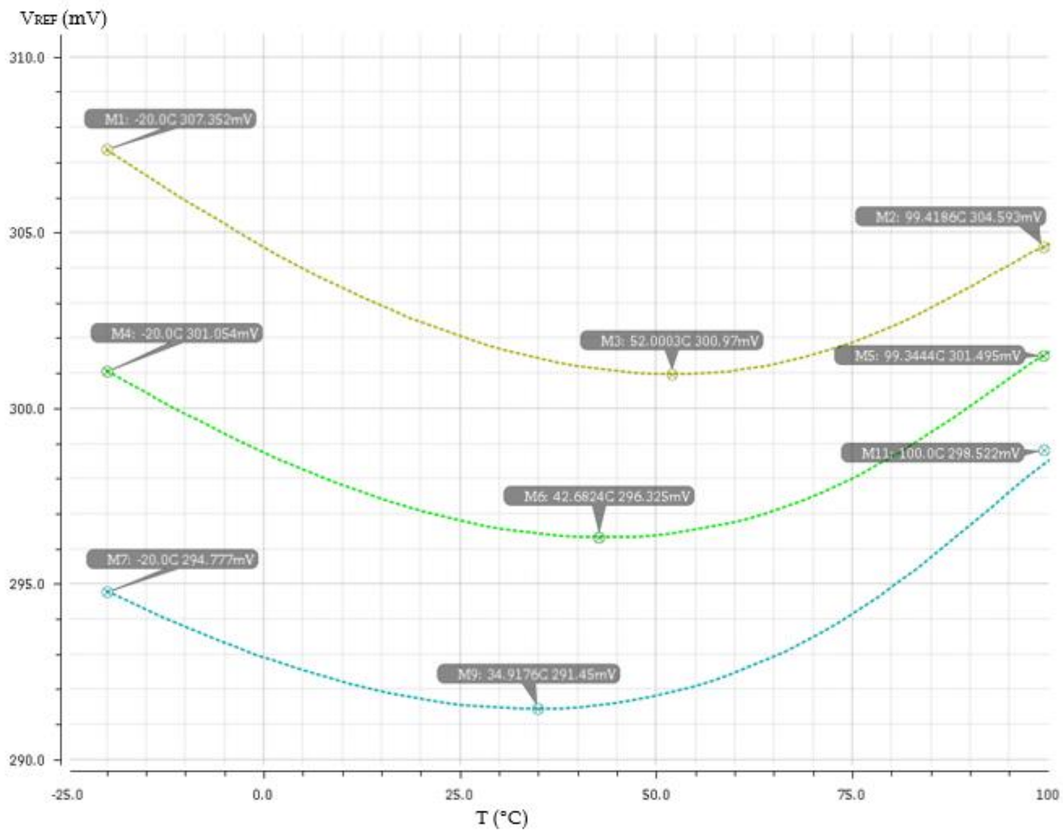

Figure 4.14: Output voltage of the circuit with a parametric analysis of the size of the width of the transistor T_7, which took values of 46 µm, 47 µm and 48 µm, for the curves in yellow, green and blue, respectively.

By direct inspection, the half of the curve which has a maximum average slope is respective to a width size of 47 µm:

$$\Delta V_{REF_{MAX}(W=47\ \mu m)} = \frac{301{,}495\ mV - 296{,}325\ mV}{99{,}3444\ °C - 42{,}6824\ °C}$$
$$= 0{,}09124 \frac{mV}{°C} \approx 91{,}24\ \frac{\mu V}{°C}\ (91{,}24\ ppm/°C) \quad (4.9)$$

4.4. Conclusions

The mathematical analysis shows values that are relatively close to the real ones. This method of finding the proper magnitude for the values of the resistors is very useful because, otherwise, an extensive number of simulations by trial and error would have to be done. With the proper tools, it is possible to observe the behavior of the voltages of each current generator and guess the best values to be applied on the simulation. Summarizing all the achieved work, tables 4.8 and 4.9 show the final results of the mathematical and simulation methodologies that are used to project the final output voltage with a maximum variation of nearly 0.1 mV/ºC, between -20 ºC and 100ºC.

Table 4.8: Overall theoretical results.

R_1 [kΩ]	R_2 [kΩ]	I_1 [µA]	I_2 [µA]	K
40	400	11.171	0.933	9,12

Table 4.9: Overall simulation results.

R_1 [kΩ]	R_2 [kΩ]	I_1 [µA]	I_2 [µA]	K (Predicted)	K (Simulated)
25	180	11.057	0.972	5.7513	4.7

5

Design Methodology and Electrical Simulations using TFTs on Glass

5.1. Introduction

A different approach is taken in consideration when dealing with TFTs, when compared to the previous dimensioning. The main reasons are, in first place, that the electrical carriers of TFTs are electrons, so there are only n-type transistors, which makes the circuit of figure 3.6 incompatible. Therefore, some adaptations have to be made on the circuit in order to operate as intended; and second, since the models of the glass-TFTs used in software simulations are not characterized in temperature, the simulations have to be made physically. Thus, the proposed circuit has to be designed, produced and tested with appropriate hardware.

5.2. Proposed Circuit

In order to allow designing a voltage reference circuit using TFT devices, since only n-type channel is available, it is necessary to make significant changes in the original topology [1].

The proposed new circuit totally replaces each individual PMOS (in current-mirror configurations) by two cascaded diode-connected n-type TFT devices. Thus, since its gate is connected to V_{DD}, as well as the drain, it will act as a load, forcing the next transistor to operate in the saturation region, activating then the respective branch. Each branch of the seven starts with a diode-configuration transistor, as can be seen in figure 5.1. This methodology has to be proven first, so a first simulation is made using the same standard 130 nm technology, as in chapter 4.

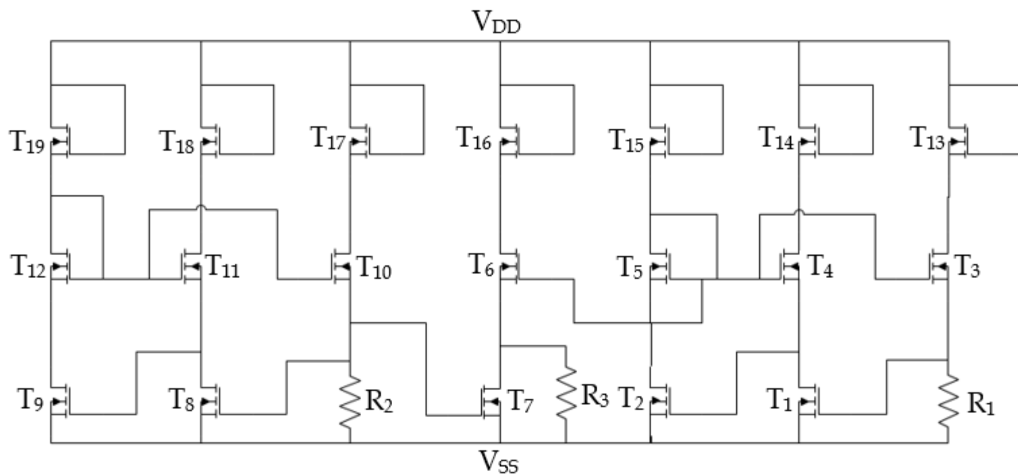

Figure 5.1: Proposed circuit using only n-type channel transistors.

A theoretical analysis could also be done in this scenario, using equations (3.14) to (3.21), since it is the exact same technology. However, the real results would be very different from the expected, since the insertion of a third transistor in each branch was not considered, which could affect the overall results by an unfair margin. Given the explained situation, the dimensioning of the proposed circuit is made entirely by simulation.

In contrast with the previous studied circuits from chapter 4, where the minimum supply voltage was $V_{Th}+2V_{DSat}$, in the present scenario, the minimum supply voltage is $V_{Th}+3V_{DSat}$, because of the additional transistor, which inflicts an output voltage-drop taken by the load. Nevertheless, this value can always be adjusted through a variation of R_3.

5.3. *Designing-for-Testing Flexibility*

Since there are no temperature models available in the provided TFT technology, it is totally impossible to electrically simulate the proposed circuit over temperature. However, to provide enough testing flexibility, after fabrication, it was decided to add some internal programmability. In this context, it was decided to design device T7 (the one with a less standard aspect-ratio) as a digitally programed dedicated transistor. Please bare in mind that in the fabrication of the first TFT prototypes, it is planned to use all resistors as external surface-mounted devices (SMD) components. This will also provide extra degrees of freedom and, consequently, additional testing flexibility.

Since the generation of a voltage reference, such as reported by [1], has various inputs, as known at this point, in order to achieve a stable output, the referred example shows that there is one variable that needs to be simulated before the circuit is produced. In other words, all the previous simulations showed that the width of each of the transistor T_7 tremendously affects the perfect operation of the output signal. Thus, and given the fact that the models of the TFTs could exhibit some divergences compared to the future real world results, a new component is introduced.

The idea is to replace the actual transistor T_7 for eight different transistors in parallel, with different width sizes, controlled by a digital logic circuit. This adds another way of physically controlling the output of the circuit.

The logic circuit consists in a decoder, made by NOT and NAND gates. It is implemented with the same TFT models, so the logic behind the digital decoder, as well as its respective components, is the same as used with NMOS transistors.

5.3.1. NOT Gate

In figure 5.2 it can be seen how to generate an output signal which is the opposite of the input, or an inverter (NOT gate).

Table 5.1: Truth table of the inverter.

IN	OUT
0	1
1	0

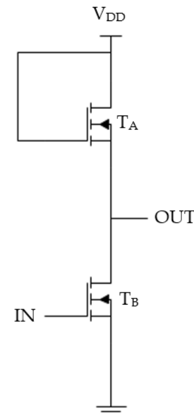

Figure 5.2: Inverter circuit, using n-type transistors.

Transistor T_A is in diode-configuration, so it is always in the saturation region. Then, the output of the circuit is considered to be '1' (V_{DD}-V_{Th}), if the input signal is '0' (V_{GS}<V_{Th}); if the input signal is '1' (T_B in saturation region), the output signal will be '0' since the voltage-drop across T_B is only V_{DSAT}.

5.3.2. NAND Gate

Since transistor T_7 is replaced for another eight transistors, a decoder with at least 3 bits is necessary. To control all the eight exits, three inputs are necessary, therefore three input NAND logic gates have to be used. Figure 5.3 shows a topology of one NAND gate using only n-type transistors.

A	B	C	OUT
0	**0**	**0**	1
0	**0**	**1**	1
0	**1**	**0**	1
0	**1**	**1**	1
1	**0**	**0**	1
1	**0**	**1**	1
1	**1**	**0**	1
1	**1**	**1**	0

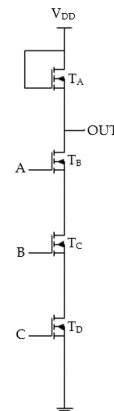

Figure 5.3: NAND circuit, using n-type transistors.

The logic of a NAND gate is similar to the inverter. Basically, the output signal is always '1' (V_{DD}-V_{Th}), since T_A is in diode-configuration, as described on the inverter, except when all three transistors, T_B, T_C and T_D, are in saturation. If so, all six transistors are conducting and the output voltage of the NAND gate will be, approximately, V_{DD}-$4V_{Th}$, which can be considered as the '0' logic value.

In figure 5.3, the three upper transistors can be replaced for just one, with the triple of the size, or a single resistor, like any transistor in diode-configuration but, in that case, it could bring major consequences, such as a larger circuit area.

5.3.3. 3x8 Decoder

The two logic gates already presented and explained are then used to implement a decoder, which table of truth and respective circuit can be seen in table 5.3 and figure 5.4, respectively.

Table 5.2: Truth table of the 3x8 decoder.

A	**B**	**C**	**Y_0**	**Y_1**	**Y_2**	**Y_3**	**Y_4**	**Y_5**	**Y_6**	**Y_7**
0	**0**	**0**	0	1	1	1	1	1	1	1
0	**0**	**1**	1	0	1	1	1	1	1	1
0	**1**	**0**	1	1	0	1	1	1	1	1
0	**1**	**1**	1	1	1	0	1	1	1	1
1	**0**	**0**	1	1	1	1	0	1	1	1
1	**0**	**1**	1	1	1	1	1	0	1	1
1	**1**	**0**	1	1	1	1	1	1	0	1
1	**1**	**1**	1	1	1	1	1	1	1	0

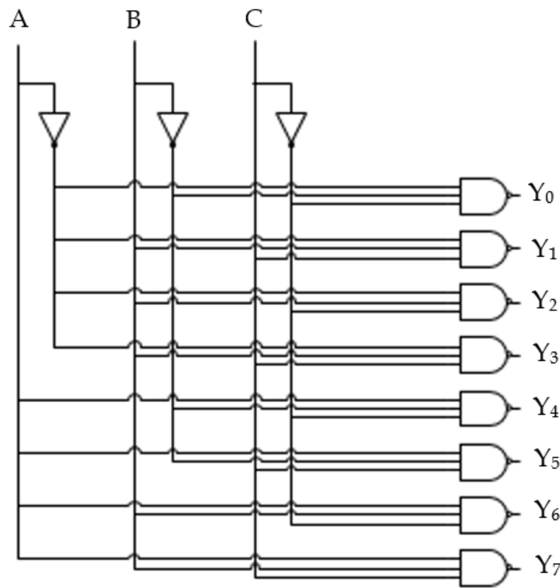

Figure 5.4: Decoder circuit, using NOT and NAND gates specified in figures 5.2 and 5.3.

From the previous explanations, and taking a closer look at figure 5.4, it can be concluded that, for each one of the eight possible combinations of the input, only one output of the decoder is selected, being low-activated, or active at '0' logic signal, since NOT and NAND gates are used.

All of the digital logic could be implemented by using NOR gates, instead of NAND. However, they present some disadvantages over the used ones. Generally, NAND gates offer less delay, occupy less die area and use transistors of similar sizes, which is very important in this work, since all of the transistors are identical [22].

With the digital components developed and proven to be working, it is now possible to give the decoder an input logic signal to choose what transistor will be responsible for playing the role of T_7.

5.4. Simulation Results

Since it was not possible to electrically simulate the proposed new circuit with TFT devices (due to the lack of temperature modeling), for proof of concept, in this chapter of the dissertation, we show simulation results in the standard 130 nm technology. As stated before, only n-channel devices had been used.

5.4.1. Proposed Circuit Results, Using a Standard 130 nm Technology

Given that NMOS transistors have better electrical properties than PMOS, such as its carriers, the electrons, having about two times greater mobility than PMOS respective carriers, the holes, it can be predicted that, for the same values of R_1 and R_2 as before, the respective currents will be higher. Thus, to maintain the chosen values of 10 µA and 1 µA, the two resistors will be consequently larger. In figures 5.5. a) and 5.5. b) the behaviors of I_1 and I_2 over temperature can be seen for the new values of R_1 and R_2, which are 60 kΩ and 800 kΩ, respectively.

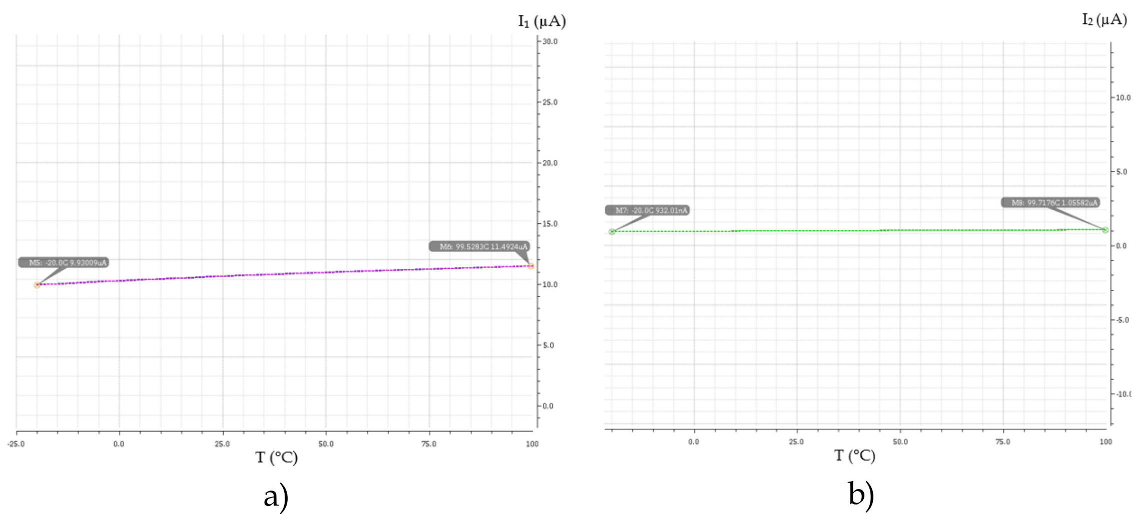

Figure 5.5: Current characteristics over temperature: a) I_1, for R_1=*60 kΩ*; b) I_2, for R_2=*800 kΩ*.

Another consequence of using only n-type MOSFETs is that, as the current gains are significantly larger, T_7 happens to be half the size as before. So, for an R_3 of 50 kΩ, which is the same since the beginning of this work, the output voltage reference stays around 123 mV, for a width size of 20 µm. Figure 5.6 shows the output voltage behavior for different width sizes.

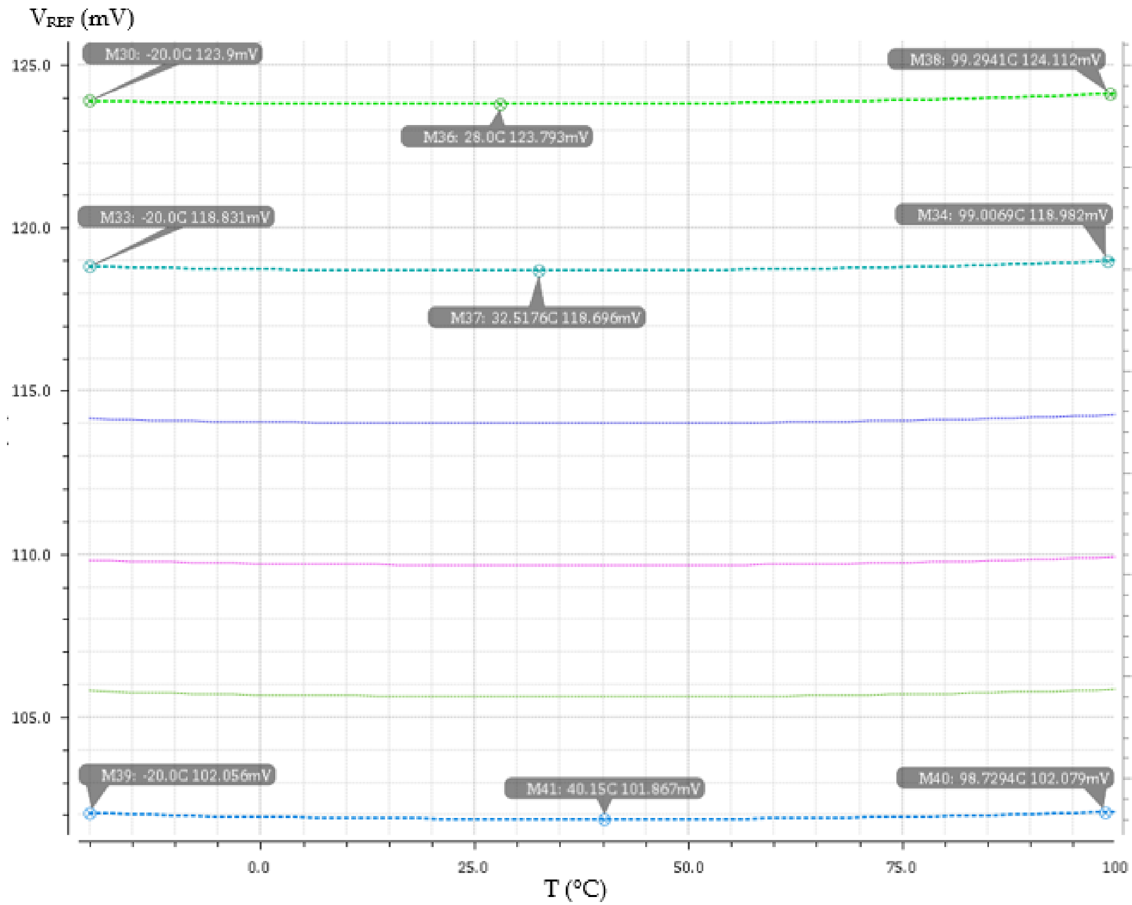

Figure 5.6: Parametric analysis of the output voltage for different width sizes. The green curve on top represents the output voltage for *W=20 µm*.

$$\Delta V_{REF_{MAX\,(W=20\ \mu m)}} = \left|\frac{123.793\ mV - 123.9\ mV}{28\ °C - (-20\ °C)}\right|$$
$$= 0{,}002229\,\frac{mV}{°C} \approx 2{,}2\ \frac{\mu V}{°C}\ (2{,}2\ ppm/ºC) \tag{5.1}$$

Curiously, the values of the maximum variation of the output voltage reference are better than before and, instead of a very specific value for the width of T_7, it can be found that this value can vary from 5 µm, or less, to 20 µm, without considerable variations. For values greater than 20 µm, the system will no longer show a compensated behavior, despite having a very low slope value.

5.4.2. *Digital Logic Results*

To ensure that the new circuit, with the TFT logic gates, operates as it should, it is necessary to simulate how the system behaves with a decoder that only uses the current TFT technology. The figures 5.7, 5.8 and 5.9 below, show the simulation results of the NOT and NAND gates, as well as the overall decoder output, respectively. It is imperative that the output of the decoder works well, since the output signal of the entire voltage reference circuit is dependent on the transistor that will be the actual T_7. The voltage-drop across the referred transistor will be the output voltage signal of the circuit.

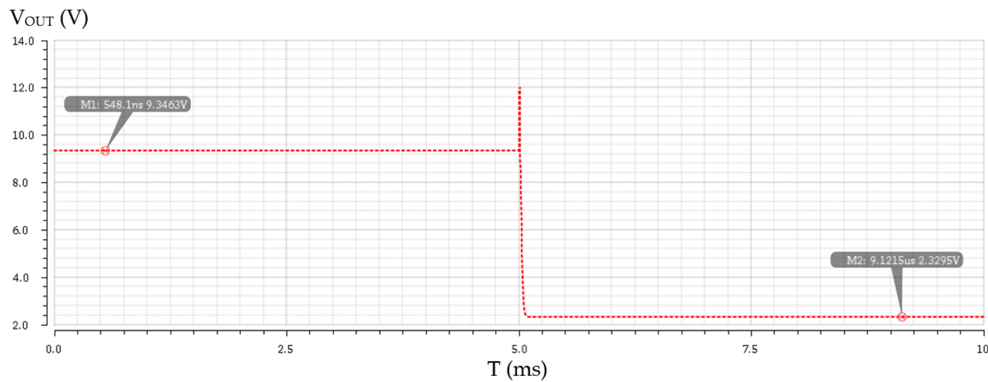

Figure 5.7: NOT gate output signal.

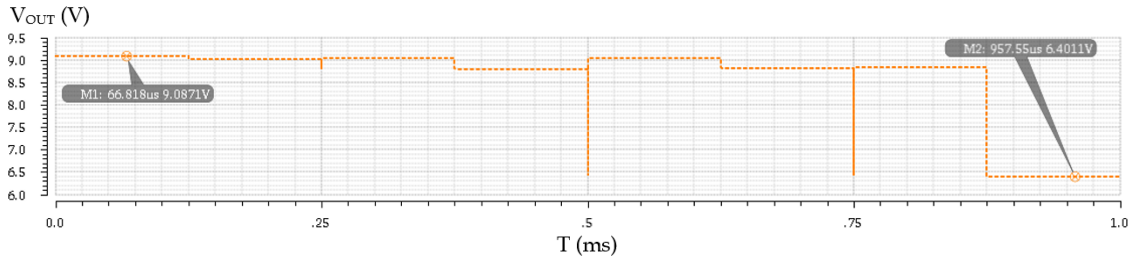

Figure 5.8: NAND gate output signal.

In figures 5.7 and 5.8 the correct behavior of the NOT and NAND gates are clearly seen, with the TFT technology used. The simulations had to be made considering very slow transition times in order to see good convergent results, as presented. The cause of this occurrence should have to do with the code of the TFT model itself, yet the digital part of the circuit should have a different but better behavior in a real-life situation.

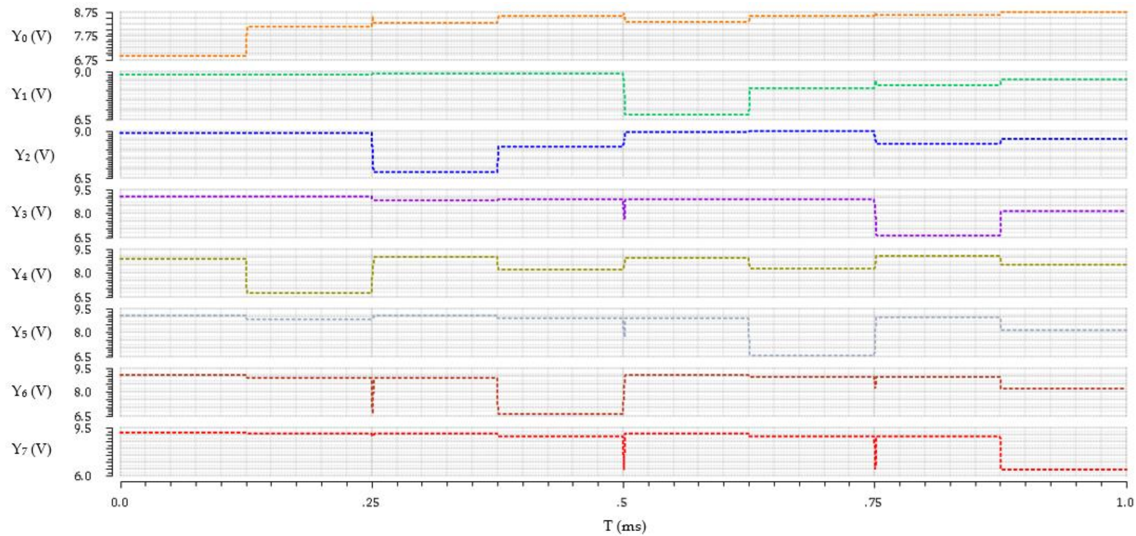

Figure 5.9: Decoder output signal for each combination of the inputs.

Despite slight variations of the output voltage, it is possible to stablish a threshold value, which defines the '0' and the '1' logic values. The output varies approximately between 9 V and 6.5 V, so if the threshold value assumed is, e.g, 7.5 V, even if the top values, close to V_{DD}, come down slightly, a logic '1' can still be considered.

It was found that the decoder only has the results presented above for very slow rise and fall times, given some parasitic capacitances problems of the models, which prevented the simulations to converge properly. The referred times had to be set to values around 1 µs for the overall circuit to work. However, in the fabricated circuit itself, that would not be the case.

Another consideration that must be taken into account is the size of the transistors for the new technology. Whereas the sizes of almost all of the CMOS transistors were 10 µm for the width and 1 µm for the length, here the size relation is $(W/L)=(40\ \mu m\ /20\ \mu m)$ for the load and $(W/L)=(640\ \mu m\ /20\ \mu m)$ for the drive.

However, it cannot be forgotten that TFTs are n-channel only, so the present approach will not be suitable for the purpose of selecting just one of each TFT branch, since the decoder is low activated. Thus, a NOT gate has to be present at the end of each output of the decoder.

5.4.3. Proposed Circuit Results, using TFTs on Glass Technology

As mentioned earlier, TFT technology has a greater carrier's mobility and the currents across I_1 and I_2 current generators are substantially greater, which implies larger resistive values. By simulation, this prediction is shown to be correct, since the values of R_1 and R_2 had to be increased to 500 kΩ and 4 MΩ, respectively, with the aim of maintaining the original current values. Nevertheless, this could only be verified for a temperature of 27 ºC and was not possible to simulate in a different range of temperature at this point. Thus, it was not possible to observe what kind of behavior the referred currents have, either PTAT or CTAT, as well as voltages, so that adjustments could be made.

In these simulations of the analog part of the circuit, a transistor's size scaling was considered as well, being all the TFTs 20 times bigger than the respective ones on CMOS technology. Overall, with the exception of the transistors that replace the single initial T_7, all transistors have a width of 200 µm and a length of 20 µm. The chosen value for the length must be large enough to eliminate short channel effects, which are a major problem in any analog circuit. That is why the TFTs of the decoder can have smaller length sizes. For the particular case of T_7, which should have a width size of 400 µm, it is replaced with eight transistors, which sizes vary from 100 µm to 800 µm, in steps of 100 µm instead. Since the tests of the proposed circuit cannot be done by simulation and it is not possible to predict which will be the best and more approximate sizes of T_7, this is the best way to design the circuit after its fabrication.

The following figures show the layout of each part of the circuit, digital and analog, respectively. Figure 5.11 shows the TFT layout of the NOT gate, figure 5.12 the NAND's and figure 5.13 the 3-bit decoder.

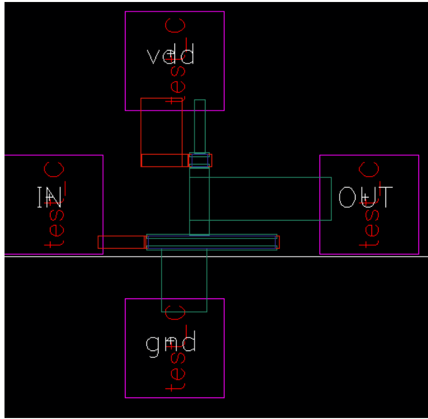

Figure 5.10: NOT gate layout.

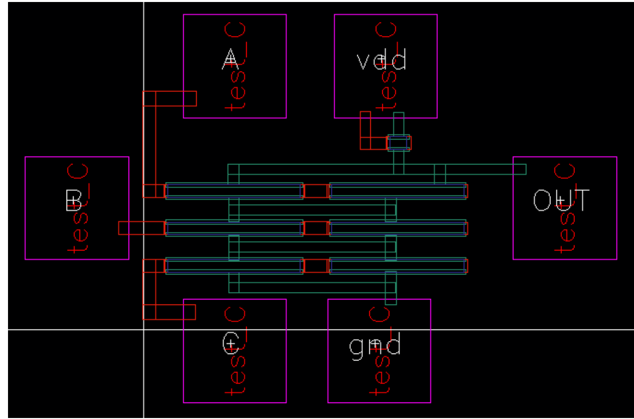

Figure 5.11: NAND gate layout.

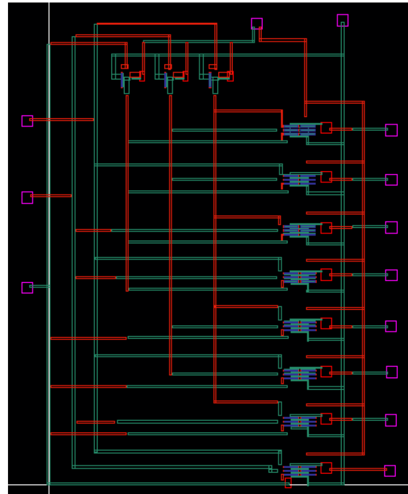

Figure 5.12: 3-bit decoder layout.

Figure 5.13 presents the final circuit layout, while figure 5.14 the entire circuit with a 5x5 cm die area and respective final representation. Pins R_1, R_2 and R_3 are for the external resistors to be connected, V_1, V_2 and V_3 are the inputs of the decoder, which will select the proper output TFT branch, V_{DD} is the pin for the power supply voltage of 10 V and the V_{OUT} is the output pin of the entire circuit.

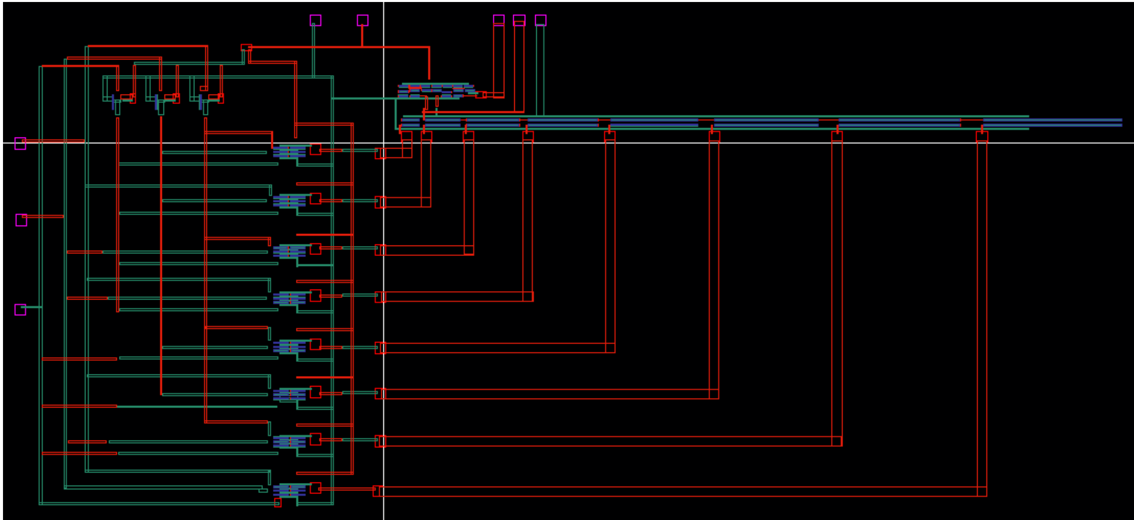

Figure 5.13: Final TFT circuit layout, with analog and digital circuits integrated.

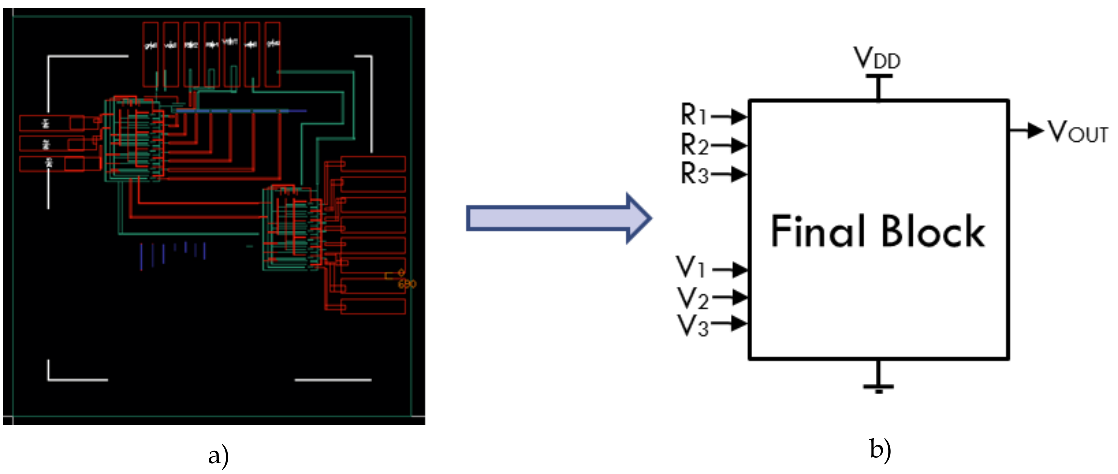

Figure 5.14: a) Final TFT circuit layout on a 5x5 cm die area; b) Final block representation.

6

Conclusions and Future Work

The main objective of this work was to design a bandgap voltage reference, using only IGZO glass-TFTs, following what was reported by [1]. The theoretical analysis of the cited article was reviewed, implemented and tested with a standard 130 nm CMOS technology, then some changes had to be made to the circuit in order to achieve similar results with the new technology. Some of changes included the replacement of the p-type transistors for a pair of n-type TFTs, one in diode-configuration, acting as load, followed by another n-type TFT, considering different sizes, matching the new technology, and another replacement for the transistor which drives the output voltage, for a few couple, controlled by a 3x8 decoder, since it has been observed that its parameters hugely influence the optimal behavior of the circuit.

The simulation results for the CMOS technology proved to be very good, with a maximum variation of a few dozen microvolts per Celsius degree, which result appears to be even better with only n-type transistors, around forty times better. So, it can be concluded that if the main purpose of this thesis was to develop a bandgap voltage reference, such as the reported by [1], the results were very encouraging.

Throughout the entire document, the actual value of the output voltage was never relevant, keeping R_3 constant to 50 kΩ for both technologies. As explained

in chapter 3, R_3 just serves as a voltage regulator, adjusting the offset of the output. However, if a voltage reference is behind any circuit, it has to supply a very specific voltage value for each technology in order for them to work properly, which was never the concern of this work. This happened by the simple fact that it can be used, e.g., a non-inverting operational amplifier at the output of the developed voltage reference, to raise even more the output voltage, in case of a large variation of R_3 would not be enough. The non-inverting operation amplifier has a key advantage in this type of applications, which is an almost null temperature dependence, as its voltage is directly dependent on the ratio between its two resistors so, assuming both materials are the same, both temperature dependences of the resistors will cancel out.

The overall power consumption of the CMOS circuit is 1,434 mW, while TFT's is 4,253 mW. Comparing the two technologies the main reasons for this to happen are that the charge carrier mobility of TFTs is considerably higher than CMOS's, which directly results in higher drain currents, and its power supply voltage is higher as well. Knowing that the power consumption is the multiplication of voltage and current, being these two values higher than in CMOS technology, the power consumption of the TFT circuit is predictable much higher.

Despite all the developments that were made and validated, it was not possible to actually produce and test it in temperature. This way, it must be done in the future, as a voltage reference based only on TFTs technology has never been done before.

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Appendix

Units

$q := 1.6 \cdot 10^{-9} C$

Data

$V_{DD} := 1.2\ V$

$V_{Dsat1} := 100\ mV$

Technology Properties

$K_B := 1.38 \cdot 10^{-23} \cdot \frac{J}{K}$

$K_B \cdot \frac{(300 \cdot K)}{q} = 0.026 \; \frac{kg \cdot m}{s^3 \cdot A}$

$V_{TN} := 0.38 \; V$ $K_N := 500 \; \frac{\mu A}{V^2}$

$V_{TP} := 0.33 \; V$ $K_P := 100 \; \frac{\mu A}{V^2}$

$\mu_N := 670 \; \frac{cm^2}{V \cdot s}$ $\mu_P := 250 \; \frac{cm^2}{V \cdot s}$

$m_{Kn} := -0.594611 \; \frac{\mu A}{K \cdot V^2}$ $m_{Kp} := 0.039177 \; \frac{\mu A}{K \cdot V^2}$

$\varepsilon_{ox} := 3.9 \cdot 8.854 \cdot 10^{-14} \; \frac{F}{cm}$

(tox: Cadence measurements)

$t_{ox_N} := 2.73 \; nm$ $t_{ox_P} := 2.86 \; nm$

$C_{ox_N} := 1.265 \cdot 10^{-6} \; \frac{F}{cm^2}$ $C_{ox_P} := 1.207 \cdot 10^{-6} \; \frac{F}{cm^2}$

$(C_{ox} = \varepsilon_{ox} / t_{ox_N})$

$\left(K_{1.2} = \frac{d}{dT} V_{THn.p}\right)$

$K_1 := -0.8\ \frac{mV}{K}$ $\qquad$ $K_2 := 0.916666\ \frac{mV}{K}$

$K_3 := \frac{m_{Kn}}{C_{ox_N}}$ $\qquad$ $K_4 := \frac{m_{Kp}}{C_{ox_P}}$ $\qquad$ $\left(K_{3.4} = \frac{d}{dT}\frac{K_{N.P}}{C_{ox_N.P}} = \frac{d}{dT}\mu_{n.p}\right)$

Transistor Carachteristics

$$g_m\left(I_D, V_{Dsat}\right) := \text{if}\left(V_{Dsat} < K_B \cdot \frac{(300 \cdot K)}{q} \cdot 2, \frac{I_D}{\left(K_B \cdot \frac{(300 \cdot K)}{q}\right)}, 2 \cdot \frac{I_D}{V_{Dsat}}\right)$$

$$W_L_N\left(I_D, V_{Dsat}\right) := \frac{\left(2 \cdot I_D\right)}{K_N \cdot V_{Dsat}^{\ 2}} \qquad W_L_P\left(I_D, V_{Dsat}\right) := \frac{\left(2 \cdot I_D\right)}{K_P \cdot V_{Dsat}^{\ 2}}$$

$$WN\left(I_D, V_{Dsat}, L\right) := \frac{\left(2 \cdot L \cdot I_D\right)}{K_N \cdot V_{Dsat}^{\ 2}} \qquad WP\left(I_D, V_{Dsat}, L\right) := \frac{\left(2 \cdot L \cdot I_D\right)}{K_P \cdot V_{Dsat}^{\ 2}}$$

(W/L)1 vs Temperature

$W_L_1 := 10$ $W_L_{12} := 20$ $W_L_{13} := 30$ $W_L_{14} := 40$

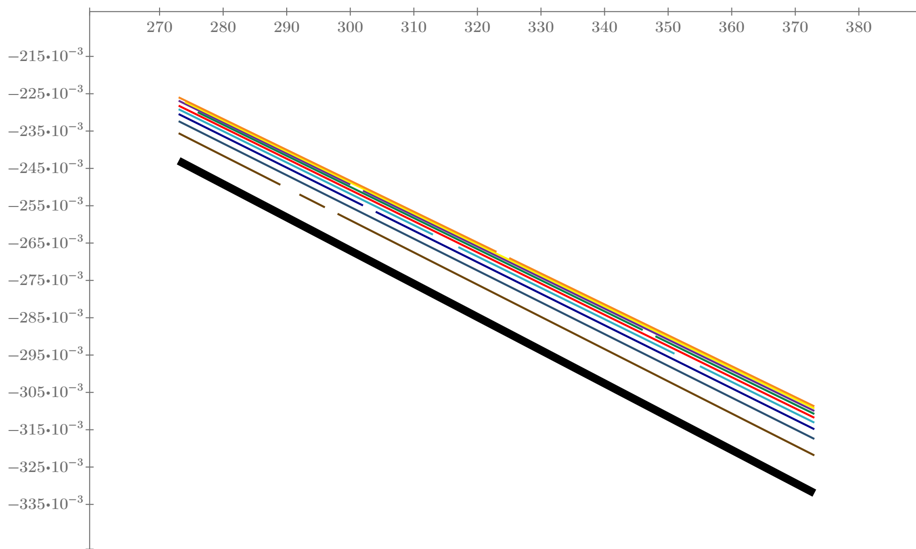
$W_L_{15} := 50$ $W_L_{16} := 60$ $W_L_{17} := 70$ $W_L_{18} := 80$

$W_L_{19} := 90$ $W_L_{110} := 100$

$R_1 := 40\ k\Omega$

$T := 273\ K, 274\ K .. 373\ K$

$$dV_{CTAT1}\left(W_L_1, T\right) := \left(V_{TN} \cdot \left(\frac{K_1}{V_{TN}} + \frac{\frac{K_1}{V_{TN}} - \frac{K_3}{\mu_N}}{\sqrt{1 + 2 \cdot R_1 \cdot V_{TN} \cdot K_N \cdot W_L_1}}\right) + \frac{1 + \sqrt{1 + 2 \cdot R_1 \cdot V_{TN} \cdot K_N \cdot W_L_1}}{K_N \cdot W_L_1 \cdot R_1} \cdot \left(\frac{K_3}{\mu_N}\right)\right) \cdot T$$



$dV_{CTAT1}\left(W_L_1, T\right)\ (V)$

$dV_{CTAT1}\left(W_L_{12}, T\right)\ (V)$

$dV_{CTAT1}\left(W_L_{13}, T\right)\ (V)$

$dV_{CTAT1}\left(W_L_{14}, T\right)\ (V)$

$dV_{CTAT1}\left(W_L_{15}, T\right)\ (V)$

$dV_{CTAT1}\left(W_L_{16}, T\right)\ (V)$

$dV_{CTAT1}\left(W_L_{17}, T\right)\ (V)$

$dV_{CTAT1}\left(W_L_{18}, T\right)\ (V)$

$dV_{CTAT1}\left(W_L_{19}, T\right)\ (V)$

$dV_{CTAT1}\left(W_L_{110}, T\right)\ (V)$

$T\ (K)$

$$\frac{dV_{CTAT1}(W_L_1, 373\ K) - dV_{CTAT1}(W_L_1, 273\ K)}{373\ K - 273\ K} = -8.9 \cdot 10^{-4}\ \frac{V}{K}$$

(Slope of V.CTAT1, with W_L.1=10)

$$I_1 := \frac{V_{TN}}{R_1} + \frac{1 + \sqrt{1 + 2 \cdot R_1 \cdot V_{TN} \cdot K_N \cdot W_L_1}}{K_N \cdot W_L_1 \cdot {R_1}^2}$$

$$I_1 = 11.171\ \mu A$$

(W/L)2 vs Temperature

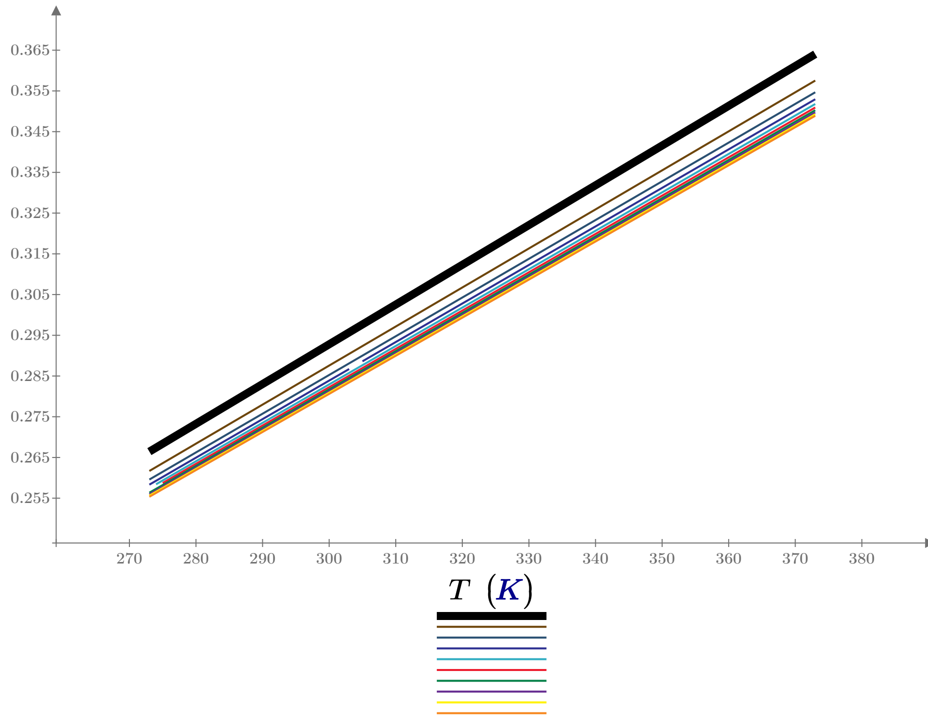
$W_L_2 := 10$ $W_L_{22} := 20$ $W_L_{23} := 30$ $W_L_{24} := 40$

$W_L_{25} := 50$ $W_L_{26} := 60$ $W_L_{27} := 70$ $W_L_{28} := 80$

$W_L_{29} := 90$ $W_L_{210} := 100$

$R_2 := 400\ k\Omega$

$$dV_{CTAT2}(W_L_2, T) := \left(V_{TP} \cdot \left(\frac{K_2}{V_{TP}} + \frac{\frac{K_2}{V_{TP}} - \frac{K_4}{\mu_P}}{\sqrt{1 + 2 \cdot R_2 \cdot V_{TP} \cdot K_P \cdot W_L_2}} \right) + \frac{1 + \sqrt{1 + 2 \cdot R_2 \cdot V_{TP} \cdot K_P \cdot W_L_2}}{K_P \cdot W_L_2 \cdot R_2} \cdot \left(\frac{K_4}{\mu_P} \right) \right) \cdot T$$



$dV_{CTAT2}(W_L_2, T)$ (V)

$dV_{CTAT2}(W_L_{22}, T)$ (V)

$dV_{CTAT2}(W_L_{23}, T)$ (V)

$dV_{CTAT2}(W_L_{24}, T)$ (V)

$dV_{CTAT2}(W_L_{25}, T)$ (V)

$dV_{CTAT2}(W_L_{26}, T)$ (V)

$dV_{CTAT2}(W_L_{27}, T)$ (V)

$dV_{CTAT2}(W_L_{28}, T)$ (V)

$dV_{CTAT2}(W_L_{29}, T)$ (V)

$dV_{CTAT2}(W_L_{210}, T)$ (V)

$$\frac{dV_{CTAT2}(W_L_2, 373\ K) - dV_{CTAT2}(W_L_2, 273\ K)}{373\ K - 273\ K} = \left(9.76 \cdot 10^{-4}\right) \frac{V}{K}$$

(Slope of V.CTAT2, with W_L.2=10)

$$I_2 := \frac{V_{TP}}{R_2} + \frac{1 + \sqrt{1 + 2 \cdot R_2 \cdot V_{TP} \cdot K_P \cdot W_L_2}}{K_P \cdot W_L_2 \cdot {R_2}^2}$$

$$I_2 = 0.933\ \mu A$$

Vref

$R_3 := 50\ k\Omega, 51\ k\Omega .. 500\ k\Omega$

$$V_{CTAT1} := V_{TN} + \frac{1 + \sqrt{1 + 2 \cdot R_1 \cdot V_{TN} \cdot K_N \cdot W_L_1}}{K_N \cdot W_L_1 \cdot R_1}$$

$$V_{CTAT2} := V_{TP} + \frac{1 + \sqrt{1 + 2 \cdot R_2 \cdot V_{TP} \cdot K_P \cdot W_L_2}}{K_P \cdot W_L_2 \cdot R_2}$$

$$V_{REF}(R_3) := \frac{R_3}{R_1} \left(V_{CTAT1} + \frac{R_1}{R_2} \cdot V_{CTAT2} \right)$$

$$V_{REF}(50\ k\Omega) = 0.605\ V$$