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pMOSFET fabrication using a low temperature pre-deposition technique

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Abstract

The objective of this work was to develop a fully functional pMOSFET using a new method for dopant pre-deposition done at low temperature (90ºC) using PECVD. This technique has many advantages when compared to the traditional manufacturing method, namely it is more cost effective, simpler and faster. Because it does not require an oxide layer to create the patterns, it can be conjugated with other low temperature techniques.

To obtain a functional pMOSFET, this work was divided in four different studies. The objective of the first study was to achieve metal-semiconductor ohmic contacts. To obtain a perfect ohmic contact of aluminum in a n-type silicon wafer, it is necessary to create a narrow space-charge region in order to allow carrier tunneling. That was reached by using a highly doped n-type hydrogenated amorphous silicon thin film made with a phosphine gas phase concentration of 1.5%, followed by a one-hour diffusion process at 1000ºC. A sheet resistance of 22.9 Ω/□ and a phosphorus surface concentration of 5.2×10^{19} at cm^{-3} were obtained.

The second study consisted of producing p^+n junctions varying the surface concentration and the diffusion time and temperature. The best diodes produced have significantly different profiles. The first was produced with a deep junction and a 0.165% diborane in the gas phase and presents the following parameters: rectification ratio of 6.01×10^3, threshold voltage of 0.53 V and an ideality factor of 1.74. The second diode was produced with a shallow junction and using a 1.5% diborane in the gas phase with the parameters: rectification ration of 3.94×10^3, a threshold voltage of 0.46 V and an ideality factor of 2.58.

Regarding the oxide characteristics for application as gate dielectric (third study), it was determined that the best oxides were produced by wet oxidation with a thickness of about 1300 Å.

After finishing the previous studies, it was possible to produce a fully functional p-type field effect transistor (fourth study). The MOSFETs worked in enhancement mode with the best parameters being: a threshold voltage of -4 V and a field effect mobility of 106.56 cm^2/Vs.

Keywords: MOSFETs, PECVD, low temperature pre-deposition, hydrogenated amorphous silicon, cost effective.

Resumo

O objetivo deste trabalho foi o desenvolvimento de um dispositivo pMOSFET utilizando um novo método de pré-deposição do dopante, realizado a baixa temperatura (90ºC), pela técnica de PECVD. Esta alteração à técnica tradicional apresenta diversas vantagens, nomeadamente, ser um método mais barato, simples e rápido, uma vez que não necessita do crescimento prévio de uma camada de dióxido de silício e da respetiva litografia para formar padrões no substrato. Além disso, pode ser conjugada com outras técnicas que utilizem baixas temperaturas.

De forma a obter um pMOSFET funcional foi necessário estruturar o trabalho em quatro partes distintas. Iniciou-se pelo estudo dos contactos óhmicos. Estes são obtidos, num substrato tipo-n, criando uma região de depleção estreita o suficiente para permitir o tunelamento de portadores. Tal é conseguido através de um filme de silício amorfo hidrogenado tipo-n, altamente dopado, usando uma percentagem de fosfina de 1.5% durante a deposição, seguido de um processo de difusão a 1000ºC ao longo de uma hora. Com estes parâmetros de produção foi obtida uma resistência folha de 22.9 Ω/□ e uma concentração de fósforo à superfície de 5.2×10^{19} at cm^{-3}.

A segunda parte consistiu no estudo de junções p^+n variando a concentração de superfície, o tempo de difusão e a temperatura da mesma. Os melhores díodos produzidos têm perfis significativamente diferentes. O primeiro tem uma junção profunda e foi produzido recorrendo a um filme de silício amorfo depositado com uma percentagem de diborano de 0.165%, apresentando uma razão de retificação de 6.01×10^3, uma tensão limiar de 0.53 V e um fator de qualidade de 1.74. Por sua vez, o segundo díodo tem uma junção rasa, sendo produzido a partir de um filme feito com uma percentagem de diborano na fase gasosa de 1.5%, apresentando uma razão de retificação de 3.94×10^3, uma tensão limiar de 0.46 V e um fator de qualidade de 2.58.

A terceira parte consistiu no estudo das características do óxido usado como dielétrico de porta. Concluiu-se que os melhores óxidos eram obtidos pelo método húmido com uma espessura aproximada de 1300 Å.

Após obter as conclusões dos estudos referidos anteriormente, foi possível produzir um transístor de efeito de campo do tipo-p. Todos os MOSFETs produzidos funcionavam em enriquecimento sendo que os melhores parâmetros obtidos foram: uma tensão limiar de -4 V e uma mobilidade de efeito de campo de 106.56 cm^2/Vs.

Palavras-chave: MOSFETs, PECVD, pré-deposição a baixa temperatura, silício amorfo hidrogenado, baixo custo de produção.

List of Abbreviations

a-Si:H – Hydrogenated amorphous silicon

AC – Alternate Current

APM – Ammonia Peroxide Mixture

BJT – Bipolar Junction Transistor

CMOS – Complementary Metal Oxide Semiconductor

CVD – Chemical Vapor Deposition

C-V – Current-Voltage

c-Si – Crystal Silicon

DC – Direct Current

FET – Field Effect Transistor

FEOL – Front End of Line

FE – Field Emission

FTM – Film Thickness Monitor

FPP – Four Point Probe

HPM – Hydrochloric Peroxide Mixture

IRR – Image Reversal Resist

IC – Integrated Circuit

IST – Instituto Superior Técnico

LMSCE – Laboratório de Materiais Semicondutores e Conversão de Energia

MOS – Metal Oxide Semicondutor

MOS – C – Metal Oxide Semiconductor Capacitor

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

PECVD – Plasma Enhanced Chemical Vapor Deposition

PVD – Physical Vapor Deposition

RCA – Standard Cleaning developed at the RCA company

RDF – Radial Distribution Function

Rf – Radio Frequency

SIMS – Secondary Ion Mass Spectrometry

TE – Thermionic Emission

List of Symbols

Ω - Ohm

σ – Conductivity

ΔE – Activation energy

χ - Electron affinity

χ' - Modified electron affinity

ϕ_{fn} – Fermi potential

ϕ_m – Metal work function

ϕ_{ms} – Metal Semiconductor work function

ϕ'_m – Modified work function

Φ_b – Barrier height

x_{dm} – Space-charge width

x~- Layer depth

μ_{FE} – Field Effect Mobility

η – Ideality factor

A – Ampere

Al – Aluminum

BV – Breakdown voltage

ºC – Degrees Celcius

C_s – Surface concentration

cm – centimeter

Cz – Czochralski

D – Diffusion coeficient

d_{ox} – Oxide thickness

E_F – Fermi level

E_{Fi} – Interface Fermi level

F – Farad

f – Frequency

g - gram

Hz – Hertz

HF – Hydrofluoric acid

Js – Saturation Current

h – hour

k – Boltzmann constant

L – Channel length

Lpm – Liter per minute

min – Minute

Na – Acceptor concentration

Nd – Donor concentration

ni – Intrinsic concentration

q – electron charge

Q_A – Fixed dose

Q_{A0} – Initial dose

Q_B - Maximum space-charge density per unit area

Q_{ss} – Surface state charge

Rs – Series resistance

Rp – Parallel resistance

Rpm – Rotation per minute

Si – Silicon

s – Second

SiO_2 – Silicon dioxide

V_t – Threshold voltage

V_{bi} – Built-in potential

V_{DS} – Drain-Source Voltage

V_{GS} – Gate-Source Voltage

W – Channel width

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Motivation and Objectives

Motivation

Nowadays, we are living in the information age. The development of the transistor and of the integrated circuit (IC) has led to the remarkable capability of obtaining everything we need at any given place. The transistor permeates almost every facet of our daily life. Because there is a continuous need for faster and more complex systems, semiconductor devices are being studied for improvement, and new ones are being invented. Whether it is for higher speed, lower power, cost reduction, higher efficiency or new functionality, the number and types of semiconductor devices have been growing steadily. The semiconductor electronics field continues to be a fast-changing one with thousands of technical papers published each year [1-4]

The first commercially available MOSFET was out in 1960s but the idea of field effect device can be tracked to Lilienfeld in 1926 and to Heil in 1935. The first transistor (bipolar) was born in 1947 in result of such activities [3]. The first experimental FET was shown by Shockley and Pearson in 1948 [5]. The experiment consisted in inducing a surface charge by using the semiconductor as one plate of a parallel plate capacitor. The change in device conductance depends on the semiconductor surface charge concentration, which is controlled by a third electrode [5]. The 'field effect' was subsequently applied to various but essentially similar amplifying device configurations by numerous people. These devices, however, relied on what was recognized as majority carrier modulation [4]. In 1955, Ross proposed a device using field effect on minority carriers in a surface inversion layer [3] and, in 1960, the Si-SiO_2 system was first proposed by Atalla [3, 4]. This suggestion came as one of the by-products of studies on SiO_2 growth and characterization being undertaken at Bell Telephone Laboratories. The other important contribution from such studies to the semiconductor industry was the principle of passivation which paved the way for planar technology and present day integrated circuits.

Microelectronic devices and information technologies will continue to improve. The motivation behind it is to increase the density of components, to lower their cost and to increase their performance per device and per integrated circuit [6]. With this evolution, new technologies emerge using different substrates and techniques (top-down and bottom-up) and new applications for this devices [6]. Despite this, according to CRU's[1] Silicon Market Outlook, the silicon market will continue to benefit from strong gains in demand over the next five years [7].

Since silicon is still the main material used in this industry it is relevant to develop a technique which can lower the production price and still maintain the high performance that the consumers are used to. A way to do it is by using a different technique in the pre-deposition process which allows reducing the number of fabrication steps. That can be achieved using hydrogenated amorphous silicon (a-Si:H) as a dopant source wherein its deposition is performed at low temperature (90ºC). Several work has been done in a-Si:H [8-10] but, mainly, as a thin-film for photovoltaics applications. None has been reported in the MOSFET fabrication, other than the work published from the research group where this technique has been developed.

This work results from the continuation of a previous study [11] which applied this new method for nMOS fabrication. The results obtained are promising but require alternative studies to obtain a better device performance.

Consequently, another motivation throughout this work is to explore this new method with the main goal of producing a functional pMOS transistor.

[1] CRU group (Commodities Research Unit), Ltd – London, UK.

Objectives

The main objective of this master thesis is the fabrication, optimization and characterization of a pMOSFET on a silicon substrate using a-Si:H as a dopant source, deposited by PECVD at low temperature. To achieve that goal, the work was divided in several studies in order to optimize the different parts constituting the transistor:

- Metal-semiconductor ohmic contacts;
- *pn* junction;
- Oxide characteristics;
- Production of a pMOSFET.

The success of this thesis is supported on the previous study and results obtained in nMOS fabrication. The goal was to see if the technique was also able to produce, with good results, the other type of MOSFET.

The present work shows an alternative, easy to produce, low-cost way of pMOSFET fabrication. In this stage is possible to fabricate a CMOS circuit using this production technique. Also, because of the low temperature used in the pre-deposition step, it can be applied with other unconventional approaches.

1. Introduction

For a better understanding of the topics a theoretical approach will be given. The following sections will give a review of the evolution of the techniques plus an explanation of the phenomena of the material. The new method will be described extensively. The final part is reserved for a summary of the transistor fundamentals.

1.1. New Production Method

This work is based on an innovative way to produce electronic devices, namely the pMOSFET. The conventional process requires a chemical isolation oxide used as a diffusion mask, so high temperatures (T≥1000ºC) are needed for a good oxidation rate. After the lithography step, the pre-deposition occurs, which also need high temperature. The new method allows to replace these two high temperature steps by their low temperature equivalents, making a much cheaper, efficient and faster procedure.

The technique relies on a highly doped a-Si:H thin film that will be used as dopant source. The deposition of the film is done by PECVD technique at low temperature. This is one important modification. While other deposition techniques require a heated substrate (T>200ºC) [8-10, 12, 13] this one uses a temperature of only 90ºC. The method brings several advantages:

Using this temperature is possible to use photoresist as diffusion mask instead of the silicon dioxide. The pre-deposited dose is little diffused during deposition and allows a unique diffusion process which can include different dopants. By changing the flow rate of the gas source during the deposition process we can control the diffusion profile and control more accurately the surface concentration which leads to a homogenous sheet resistance after diffusion. It can be especially useful for CMOS technology where is necessary a p-well for nMOS transistors reducing the overall processing time. Also, enables an easy way of producing shallow junctions that are very important to overcome short channel effects [14]. They are quite difficult to achieve using c-Si conventional diffusion technology because high temperatures (900-1100ºC) are used to obtain a high surface dopant concentration [14].

However, there are some issues in reducing the temperature. Firstly, it demands a considerably decrease in the pressure inside the deposition chamber. Also the polymer formation is considerably higher. Before the diffusion process, proper care must be taken regarding the deposited film, in order to avoid possible damage of the pre-deposited layer, due to problems from the desorption of hydrogen at intermediate temperatures. The thermal dehydrogenation is, therefore, needed and it was studied in a previous work [15, 16].

1.2. Metal-Semiconductor ohmic contacts

Since all semiconductor devices have contacts and all contacts have contact resistance, it is important to characterize such contacts. In this sub-section, metal-semiconductor contacts will be analyzed. They were discovered by Braun in 1874 forming the basis of one of the oldest semiconductor devices. The first acceptable theory was developed by Schottky in the 1930s [17]. Usually this name denotes the use of these devices as rectifiers with distinctly non-linear current-voltage characteristics.

Metal films such as aluminum and silicides are used to form low-resistance interconnections, ohmic contacts, and rectifying metal-semiconductor barriers [18]. Aluminum and its alloys are used extensively for metallization in integrated circuits. Thin films of aluminum can be deposited by PVD or CVD techniques. Since it has low resistivity (2.7 μΩ·cm) this metal satisfies the low-resistance requirements. The low sheet resistance minimizes voltage drops along the interconnect lines, as well as propagation delays caused by the resistance and capacitance of the line [18, 19]. Also, aluminum adheres well to silicon dioxide [18]. The goal is to achieve ohmic contacts for a proper function of the IC.

Ohmic contacts have linear or quasi-linear current-voltage characteristics. The contacts must be able to supply the necessary device current, and the voltage drop across the contact should be small compared to the voltage drops across the active device regions [17].

When a metal layer is deposited onto a semiconductor, their individual Fermi levels will adjust to be identical on either side of the interface. Independent of the mechanism of the local Fermi level adjustment, the bulk semiconductor aligns, by band bending, the interface Fermi level, E_{Fi}, with a well-defined Fermi level, E_F, inside the bulk [20]. The deposition of aluminum directly on silicon form an ohmic contact when it is p-type silicon and a rectifying one when is a n-type (lightly doped) region [21]. This happens because the deposition of β-phase aluminum silicon alloy deposits onto the parent silicon in such a way that the lattice structure of the parent silicon extends into the β phase. This regrowth region is a p-type material (aluminum acts like a p-type impurity) and, being monocrystalline with the parent n-type silicon, forms a *pn* junction [22, 23]. An analysis of the kinetics related to the aluminum-silicon phase diagram indicates that it's possible to prevent the *pn* junction formation [23].

Several techniques can be used to obtain an ohmic contact, such as, using aluminum doped with gold [23], controlled heating and cooling cycles [23], thin oxide layers on the aluminum-silicon interface [21], and high phosphorous surface concentration under the aluminum contacts [22]. The latest is the one which gives the best results and it was extensively used in BJTs. For this technique to work is necessary a phosphorous surface concentration of 2×10^{20} at cm^{-3}. This produce an n^+ region creating a perfect ohmic contact. However it's necessary a heat treatment, annealing [22]. This treatment is responsible for the variation in barrier height, Φ_b. When the samples are subjected in a temperature range of 350-450ºC, the Φ_{bn} further increase and Φ_{bp} decrease due to metallurgical reactions between Al-Si. Without the n^+ region the heat treatment increase substantially the Schottky barrier height of Al contacts.

For aluminum-silicon contacts, there is a tendency for the silicon to migrate into the aluminum, leaving voids in the silicon. Aluminum can subsequently migrate into these voids creating spiking. Under extreme conditions this can lead to junction shorts, especially in shallow junctions. The addition of 1 to 3 wt% Si to the aluminum reduces spiking considerably but creates other problems [17]. In the **Appendix A** can be seen the evolution of ohmic contacts in Si technology.

1.3. Hydrogenated Amorphous Silicon, a-Si:H

Hydrogenated amorphous silicon was a late arrival to the research on amorphous semiconductors, which began to flourish during the 1950s and 1960s [24]. The a-Si:H was first made in the late 1960s. Before that there was research on amorphous silicon without hydrogen, which was prepared by sputtering or by thermal evaporation. The latter has a very high defect density which prevents doping, photoconductivity and other desirable characteristics of a useful semiconductor [24, 25].

The first study about this material was made by Chittick and coworkers [26] using a *rf* glow discharge to deposit films from silane gas, reporting the effects of heat-treatment, ageing and doping on the properties of the film. Also, it was noticed that the variation of properties with deposition temperature is related to structural changes. These early experiments demonstrated the deposition of silicon films, the lack of conduction in defect states and increased conduction due to impurities [26]. A major turning point in the development of a-Si:H was reported in 1975 [27], where it was showed that the electrical conductivity can be controlled over many orders of magnitude by doping with substitutional impurities. The samples were also prepared by *rf* glow discharge. According to the authors for substitutional doping in a-Si:H it's necessary to follow two requirements: i) a very low overall density of gap states; ii) a narrow range of band-tail stated below ϵ_c and ϵ_v [27].

The essential role of the hydrogen was first recognized Lewis *et al.,* where hydrogen was introduced with the purpose of eliminating the defects [24]. Later experiments confirmed that

hydrogen is an essential component of the film. That allowed the device research using a-Si:H which started in 1976 with Carlson and Wronski, demonstrating a feasibility of a solar cell with conversion efficiencies of 2.4% [28]. Recently it was used in the production of solar cells in order to achieve a single-sided emitter with etched-back 'dead layer' [29]. However, very high temperatures were needed to achieve the desired effect. Research on large area electronics started in 1981 with the development of the first field effect transistor [30] and its application as switching elements in addressable liquid crystal display panels [31].

Hydrogenated amorphous silicon has the added variability of a hydrogen content which can reach 50 at%. Most features of the a-Si:H network are defined at the time of growth and therefore depend on the details of the deposition process. The usual method is by PECVD where the plasma is responsible for the decomposition of silane gas and other added for doping purposes. For n-type a-Si:H phosphine is added in the mixture and for producing p-type is necessary adding small amounts of diborane to the silane [27]. There are a large number of techniques (pyrolysis of hydrides and reduction of halides) and a wide range of temperatures used. The latter is responsible for the reduction of hydrogen content with its increase. [32]. The hydrogen content also depends on the *rf* power and on the composition of the gas [24]. The defect density also depends on the substrate temperature and *rf* power, and can vary by more than a factor 1000. The lowest values are obtained between 200-300ºC and at low power, leading to a material with the most useful electronic properties (See **Appendix B**) [24].

The information about the local order of silicon atoms come from the RDF[2] that is the average atomic density at a distance *r* from any atom. The reduced RDF of a-Si:H has sharp structure at small interatomic distances, progressively less well-defined peaks at larger distances, and its featureless beyond about 10 Å. This reflects the common property of all covalent amorphous semiconductors, that there is a high degree of short range order at the first and second neighbor distances, but then the spatial correlations decrease rapidly [24]. The silicon and the hydrogen in a-Si:H have different bonding properties where the former is described in terms of a rigid over-coordinated network containing a high strain energy and, the latter, in contrast, is more weakly bonded and can diffuse within the material and across the surface. The hydrogen terminates dangling bonds and removes weak bonds [24].

In this work, the number of defects, the photoconductivity or any other structural or electronic property of the a-Si:H film have no interest. The purpose is to use a thin film, about 600 Å thick, as a finite dopant source. Based on that, it wasn't necessary the use of hydrogen but the conditions used implied its addition. The doping atoms inside the film can be diffused to the substrate after the dehydrogenation process.

1.4. *Pn* junction

The *pn* junction is the basis of modern electronics. The theory behind it serves as foundation for the physics of semiconductor devices. The basic theory of current-voltage characteristics of *pn* junction was established by Shockley. The theory was then extended by Sah *et al.* and by Moll [33].

When the impurity concentration in a semiconductor changes abruptly from acceptor impurities, p region, to donor impurities, n region, one obtains a junction. In particular, if the acceptor impurity concentration is much higher than the donor impurity concentration, one obtains an abrupt junction and the interface is referred to as the metallurgical junction [1, 33]

For simplicity we will consider that the doping concentration is uniform in each region. Initially, at the metallurgical junction, there is a very large density gradient in both electron and hole concentration. Majority carrier electrons in the n region will begin diffusing into the p region and majority carrier holes in the p region will begin diffusing into the n region. Because there aren't

[2] Radial Distribution Function, obtained from X-ray or neutron scattering.

any external connections to the semiconductor the diffusion process cannot continue, as explained below. As electrons diffuse from the n region, positively charged donor atoms are left behind. Similarly, the holes' diffusion uncovers negatively charged acceptor atoms. This induce an electric field near the junction in the direction from n to p. These are referred as space charged regions. Since the electric field swept out all electrons and holes this is also referred as depletion region. In thermal equilibrium, the diffusion force and the electric field force exactly balance each other. In this situation the Fermi energy level is constant throughout the entire system. The conduction and valence bands energies bend through the space charge region. Hence, electrons see a potential barrier when trying to move into the conduction band in p region. This barrier is referred to as the built-in potential barrier, V_{bi}.

When applied a potential between the n and p regions the equilibrium condition is no longer verified and the Fermi level will no longer be constant through the system. When a positive voltage is applied on the n region, it makes the Femi level on that side to be below the Fermi level on p side. The total potential barrier has increased. The applied potential is in the reverse-bias condition and the current density saturates at $-J_s$. When a sufficiently high field is applied to a *pn* junction reversely biased, the junction breaks down and conducts a very large current. On the other hand, when a negative voltage is applied on the n region the potential barrier is decreased. Also, the majority carrier density in each region is increased. For voltage values greater than V_{bi} a current flows through the junction. The current rises exponentially in the forward direction.

The section above described the three regimes of the *pn* junction. The **section 3.2** of this work will show the junctions done with the new fabrication method. The fabrication of high quality junctions is of major importance for a good MOSFET behavior. For better characterizing the *pn* junction, some parameters can be obtained from the current-voltage characteristics:

- R_p (parallel resistance, from the electric model of the real diode) calculated using data obtained in the reversed-bias condition;
- R_s (series resistance, from the electric model of the real diode), V_t (threshold voltage), η (ideality factor) and I_{SAT} (saturation current), calculated using data obtained in the forward-bias condition;
- BV (breakdown voltage) calculated using data obtained in the breakdown regime.

R_s and R_p, along with the ideal *pn* junction, form the equivalent circuit which modulates the behavior of a real diode. R_s is due mainly to electrical resistance present in the current path (metal line, bulk semiconductor resistance, metal-semiconductor contacts, etc.). For high current values, R_s prevents the current exponential behavior. R_p represents the current leakage due to defects in the space charge region.

1.5. Silicon Dioxide

Silicon dioxide is considered by most a more important material in c-Si technology than silicon itself. Silicon dioxide can have many different functions, such as passivation layer, capacitor dielectric or electric isolation layer, in finished devices [34].

Silicon is very easily oxidized: a native oxide of a few nanometers thick can grow on a silicon surface in a relatively short time. This was first studied by Archer, when beginning the research about this dielectric [35]. Later, Frosch and Derik found that thermally grown silicon dioxide could be used to impede the diffusion of impurities into bulk silicon [36, 37]. This technique of oxide masking was employed in the fabrication of double-diffused silicon transistor structures (NPN 'mesa' transistor). The diffusion throughout the oxide were studied by Allen *et al* [38]. The techniques for oxidation of a single crystal were conducted by Deal [39]. The work involved the use of three different oxidizing atmospheres – dry oxygen, wet oxygen and steam. Deal revealed that there are no effects on oxidation characteristics due to impurity type or concentration, but surface orientation effects were observed [39]. Also, wet oxides were the best for masking purposes and dry ones were very sensitive to any surface contamination prior to oxidation.

Following the study, a model of the thermal-oxidation kinetics was created allowing detailed analysis regarding the nature of the transported species as well as space-charge effects on the initial phase of oxidation [40, 41].

This was later known by the Deal-Grove Oxidation Model. It's a phenomenological macroscopic model. Oxygen diffusion through the growing oxide and chemical reaction at silicon/oxide interface are modeled by the classical Fick diffusion equation and chemical rate equation. The model thus predicts linear oxidation rate initially, followed by a parabolic behavior for thicker oxides. The model works much better for thick oxides. The growing of thick oxides also depends on impurity concentration. Oxidation characteristics of heavily doped silicon were investigated [42], revealing that concentrations over 1×10^{19} at cm^{-3} for phosphorus and 1×10^{20} at cm^{-3} for boron cause an increase in oxidation rates at all temperatures (900-1200ºC). This can be explained by impurities redistribution during the oxidation process.

With the shrinking of device technology, the oxide thickness also decreased and it was necessary to predict, with more accuracy rate constants for thin oxides. Massoud was one of many investigators that reengineered the Deal-Grove concept. This new model also works for thick oxides [43].

Several studies were conducted studying the properties of thin SiO_2 for device application [44-46], where numerous methods for the testing of breakdown in oxides were analyzed. One important characterization technique is the C-V curve.

To achieve high performance, high density and low power CMOS technology, silicon dioxide has been scaled to dimensions near its fundamental limit (1.5-1.8 nm) [47]. For that reason, many high-*k* gate dielectrics (metal oxides) are being investigated as an alternative to SiO_2.

1.6. Metal Oxide Semiconductor Field Effect Transistor

The MOSFET, in conjugation with other circuit elements, is capable of voltage gain and signal power gain. This device is also extensively used in digital circuit applications, where they are the key element in logic family [3].

The heart of the MOSFET is the metal-oxide-semiconductor capacitor known as MOS-C. Essentially, the MOS-C is just an oxide placed between a semiconductor and a metal gate. The semiconductor and the metal are equivalent to the plates of a capacitor. The energy bands in the semiconductor near the oxide-semiconductor interface bend as voltage is applied across the MOS-C. The position of the conduction and valence bands relative to Fermi level at the interface is a function of the MOS-C voltage, so that the characteristics of the semiconductor surface can be inverted from p-type to n-type (and vice-versa) by applying the right voltage [1]. The C-V measurement is a powerful method of determining the gate oxide thickness, substrate doping concentration, threshold voltage and flat-band voltage (See **Appendix C and D**) [48]. The inversion regime depends on other factors, such as the work-function of the metal deposited over the gate dielectric, oxide capacity and fixed oxide charges.

The MOSFET is a four terminal device – source, drain, gate and bulk. The gate-to-source and - drain overlap is critical for the formation of a continuous channel. The device is symmetrical so that the source and drain can be interchanged. In this work, the production of an enhancement mode pMOSFET is intended.

The basic operation of the device will be described with respect to a p-channel transistor considering that the source, drain and bulk are all connected to ground. If the gate voltage is positive (much greater than zero) negative charge will be attracted to the oxide-semiconductor region. Since the substrate is lightly doped n-type (n^-) this action allows a formation of a n^+ region near the SiO_2/Si interface. This is called the accumulation regime. The equivalent circuit is two back-to-back diodes between drain and source. Only leakage current will flow. For negative gate voltage the opposite situation occurs. For small negative gate voltages, electrons in the channel

region are repelled forming a depletion region. As the voltage increases negatively, the gate attracts positive carriers. In this conditions it is possible to create a p channel with mobile holes connecting the drain and source regions. The channel is said to be *inverted*. The gate-to-source voltage, for which the concentration of holes under the gate is equal to the concentration of electrons in the n^- substrate, far from the gate, is the transistor threshold voltage, V_t. There are three regimes – cut-off, linear and saturation (See **Appendix E**) [49, 50].

2. Materials and Methods

This work is dedicated to the fabrication, optimization and characterization of a pMOSFET using a significantly different method of production. For that reason, it was important to study the various components that compose the MOSFET in order to obtain the best characteristics for the final device.

As stated in the objectives of this thesis, three studies were carried out before the MOSFET fabrication. Such studies included: i) the formation of an ohmic contact between n-type c-Si and aluminum; ii) the *pn* junction study, by varying the B_2H_6/SiH_4 flow rate, and iii) the oxide growth study by using two different methods (wet and dry oxidation) on lightly doped n-type c-Si and on light and highly doped p-type c-Si.

The last step was to conjugate all the different results obtained and produce a functional pMOSFET. The procedures will be described in the following sections giving additional insight into device development.

All the work was done at IST – Complexo Interdisciplinar.

2.1. Sample Preparation

All the studies were based on a lightly doped n-type (Cz, <100>, ρ = 1-10 Ω·cm, crystalline silicon) substrate. The original 2'' wafer was divided in several 1 × 1 cm^2 substrates for an increased project efficiency.

One initial concern of the fabrication process was the cleaning of the samples. The first step was the use of a non-ionic, non-residual and unperfumed Teepol product. The residues of the product were removed using ultra-pure Milipore water (ρ = 15–16 MΩ·cm) and isopropyl alcohol. The samples were dried using compressed air.

For a more effective cleaning, a wet-cleaning Front End of Line (FEOL) was applied, namely the RCA Standard Clean [51]. These solutions, SC-1 and SC-2, have been widely used in the fabrication of silicon semiconductor devices. The samples were immersed in an ammonia/peroxide mixture (APM), ($H_2O:NH_4OH:H_2O_2$ – 5:1:1), for 10 minutes at 75ºC, then dipped, for 10 seconds, in HF ($H_2O:NH_4F:HF$ – 6:4:1) solution and, finally, rinsed off in ultra-pure Milipore water. The same process was done for hydrochloric/peroxide mixture (HPM) ($H_2O:HCl:H_2O_2$ – 6:1:1).

2.2. Photolithography

Regarding the photolithographic process, the procedure was conducted in a yellow room environment. The photoresist used throughout this work was AZ 1518, a positive resist that was used as diffusion mask for film deposition. Also, for the oxide study, an image reversal resist (IRR) – TI 35E – was used. In the **Appendix F** both processes are illustrated.

To apply the resist on the substrate a spin coater system Laurell WS-650MZ-23NPP was used. The velocity used was 3000 rpm for 20 seconds, obtaining a resist thickness of about 2 μm. To enhance adhesion and reduce solvent content, a softbake step was introduced, putting the samples over a hot plate at 100ºC for 1 minute. Some processes, namely, the pattern of the aluminum contacts, needed a thinner resist to prevent resist accumulation at the edges of the sample, preventing possible shorts circuits. Also, the IRR, due to its increased viscosity compared to AZ 1518, needed an increase velocity of the spinner plate. For this processes, a 4000 rpm speed for 40 seconds was used. The UV exposure was done without a mask aligner in an inchoate system. Subsequently, the photoresist was developed using two different developer solutions. For the majority of the studies, the NaOH (4g/L) was used but a stronger one (6g/L) was needed for IRR developing. In the MOSFET fabrication process, for reduced surface contamination, the TMAH ($(CH3)_4NO:H_2O$ – 7.2%:92.8%) was used.

The samples were cleaned and dried using ultra-pure water and compressed air, respectively. Then, they were putted, once again, on the hot plate, for 1 minute, at 115ºC for the hardbake process.

2.3. PECVD deposition of a-Si:H

Highly doped n- and p-type a-Si:H thin film were deposited throughout this work using *rf*- PEVCD (13.56 MHz) deposition technique. The system used is home-made. Three mixtures or pure gases (99.999%) were needed for film deposition, namely, silane, phosphine (2.5% in silane) and diborane (2% in hydrogen). For gas line purging purposes, pure argon was used and for purge of exhaust ballast, commercial nitrogen was used. The pressure inside the chamber changed accordingly to the dopant used in the thin film, being 100 mTorr when using phosphine and 150 mTorr when using diborane. Also, the flow rate of the pure gases or mixtures was changed in order to obtain different diffusion profiles and surface concentrations. These values are presented in the **sub-section 2.6.2**. All films had an approximate thickness of 600 Å.

2.3.1. Dehydrogenation

After film deposition, a dehydrogenation step is needed to remove all the hydrogen content attached to the silicon. It's a major step on the fabrication process in order to maintain the a-Si:H film integrity. A too fast heating between 350-550ºC could lead to blistering phenomena. Due to this, a precise control in temperature and process time is needed for a complete removal of the hydrogen. In **Table 2.1** are shown the parameters used.

Table 2.1 – Parameters used in dehydrogenation process of a-Si:H thin film.

Temperature (ºC)	Rate (ºC/min)
T_{amb} — 350	10
350 — 550	0.8

The whole process takes, approximately, 4h30m.

2.4. Diffusion

Two main diffusion profiles were used in this study. In result, deep and shallow junctions were obtained. Hence, this profiles were applied in the study of *pn* junctions and, consequently, in MOSFET fabrication. The conditions used on the furnace can be seen in **Table 2.2**.

Table 2.2 – Parameters used in dopant diffusion to obtain different profiles.

Profile	Temperature (ºC)	Time (min)	N_2 Flow[3] (lpm)
Shallow Junction	900	60	1
Deep Junction	1000	120	

The diffusion step was always followed by a wet oxidation process in order to consume the recrystallized deposited film. When a shallow junction was needed, the oxidation process occurred at the same time of the diffusion, therefore a wet oxide of about 1300 Å was grown at 900ºC. In the deep junction case, the oxidation only occurred at the final hour of the process, obtaining a oxide thickness of 3800 Å.

[3] Used when a precise control of oxide thickness was needed, namely for gate dielectric growth.

2.5. PVD metallization and contact annealing

Aluminum was used as contact metal in all samples fabricated. The deposition was made by a home-made PVD system. The final step of the fabrication of the devices consisted on the thermal annealing, in order to obtain ohmic contacts.

Table 2.3 and **Table 2.4** show the information about these processes.

Table 2.3 – Metallization parameters.

Initial Pressure (mbar)	1.7×10^{-5}
Material	Al
FTM Parameters	
Tooling Factor (%)	68
Acoustic Impedance ($g \cdot cm^{-2} \cdot s^{-1}$)	8.17×10^{5}
Density ($g \cdot cm^{-3}$)	2.70

Table 2.4 – Annealing parameters.

	Temperature (ºC)	**Time (min)**	**Rate (ºC/min)**	**N_2 Flow (lpm)**
Annealing	480	30	10	1

2.6. Device Production

2.6.1. Metal-Semiconductor ohmic contact

For obtaining perfect ohmic contacts between aluminum and c-Si (n^-) surface two sets of samples were created. The first set consisted of two twin samples, C1-A and C1-B, and the second one consisted, also, of two identical samples, C2-A and C2-B, and a shard for sheet resistance characterization (See **Appendix G**). A frame was created in the second set for the a-Si:H deposition – [PH_3]=1.5% – at both surfaces (polished and non-polished) of each sample. After the lift-off and the dehydrogenation (**Table 2.1**), the film was diffused at 1000ºC for 1 hour with simultaneous wet oxide growth. Afterwards, all the oxide was removed. All samples were submitted to lithography for lift-off patterning of sample surface, prior to aluminum evaporation, which occurred under the conditions described in **Table 2.3**. Electrical characterization occurred before and after the annealing of the contacts.

2.6.2. pn junction

The processes described in the **sections 2.1** to **2.5** were applied in this set of samples (See **Appendix H**). For this study were fabricated five sets of two samples (D[0-4] – A and B[4]). Each set have two shards (D[0-4] – A1 and B1), one for each diffusion profile. An alkali free glass substrate, AF45, was also used in order to measure further some electrical characteristics of the a-Si:H film. The masks used in the photolithographic process can be seen in **Appendix I**.

[4] The samples represented with the letter A were referred to shallow junction profile while the letter B represented the deep junction profile.

The goal was to produce p^+n junctions with different B_2H_6/SiH_4 flow rates. In **Table 2.5** is visible the variations that were done for each set. The diffusion profiles used are both described on **Table 2.2**. To obtain an equivalent oxide thickness in the deep junction profile, the oxide growth process only occurred in the last 12 minutes of the diffusion. Aluminum planar and transversal contacts to substrate were made, followed by the annealing process.

For a more complete study, a thin film of indium oxide was deposited over the boron diffused region in order to improve the current-voltage characteristics under illumination.

Table 2.5 – Execution parameters with an *rf* potency of 5 W and a temperature setpoint of 90ºC.

Samples	$[B_2H_6]$ (%)	$F(SiH_4)$ (SCCM)	$F(B_2H_6)$ (SCCM)	Total (SCCM)	Time (mm:ss)	R_C[5]
D0[6]	0.165	10	0.9	10.8	4:30	1.40
D1	0.165	10	0.9	10.8	9:00	1.11
D2	0.25	10	1.4	11.4	8:55	1.46
D3	0.6	10	4.3	14.3	6:45	1.77
D4	1.5	10	30	40	5:30	2.02

2.6.3. Oxide study

For this study were produced 16 samples – 2 sets of 8 samples each. To see the effect of different dopant doses in the oxide growth, half of them were doped[7] with the conditions of D1 and the rest with the conditions of D4 (**Table 2.5**). The conditions used are described in **Table 2.6**.

Table 2.6 – Summary of the oxidation study.

	Samples[8]	Temperature [C]	Time [min]	F(O2) [lpm]	F(O2 bubbler) [lpm]	F(N2) [lpm]
Wet Oxidation	O1/Ox1	900	60	NA	0.8	1
	O2/Ox2		50			
	O3/Ox3		40			
	O4/Ox4		30			
Dry Oxidation	O5/Ox5	1000	60	0.8	NA	1
	O6/Ox6		50			
	O7/Ox7		40			
	O8/Ox8		30			

Note: NA = Not Applicable

The aluminum contact definition was made resorting to DioCont mask (**Appendix I**) and to TI 35E photoresist. As said before, an increased speed was used in the spinner – 4000 rpm – for a longer period of time – 40 seconds. After the softbake, a low dose exposure –1 minute – was made. This allowed the patterning of all the five contacts. The substrates were kept at room temperature for 20 minutes. This delay time assures that the nitrogen generated during the exposure will diffuse

[5] Growth rate.
[6] The deposition conditions were based on D1, reducing the plasma reaction time, to obtain a thinner film.
[7] The doping occurred only in half of the substrate as shown in the schematic.
[8] O1-O8 is referred to $[B_2H_6]$ = 1.5% and Ox1-Ox8 to $[B_2H_6]$ = 0.165%.

out of the resist. After this delay, the substrates were putted on the hot plate at 115ºC for 2 minutes in a process called 'reversal bake'. The substrates were once again exposed, without a mask, for the flood exposure process. The dose, in this case, is very uncritical – at least 7 minutes of exposure. The photoresist developing was done using NaOH (6g/L) followed by the hardbake process, to ensure a good adhesion between the aluminum and the substrate. The aluminum etching was done using a home-made solution (HNO_3:H_3PO_4:H_2O – 6%:65%:29%). A scheme of the sample can be seen in **Appendix J**.

2.6.4. MOSFET fabrication

The MOSFET fabrication was based on the results of the previous studies. The sample preparation and lithographic process was the same of the other studies.

Each set contained two twin samples and a shard for process monitoring. In **Appendix K** are represented the masks used in the lithographic process. In this procedure, the gate oxide was not grown simultaneously to first diffusion. The recrystallized film was firstly removed, so that the gate oxide could be grown in the monocrystalline silicon surface. The bulk contact was made at the back of the substrate (aluminum transversal contact). The structure of the MOSFET (top view) as well as the channel dimensions are represented in **Appendix L** [52].

Several parameters were tested, such as, the dopant concentration (D1 and D4 conditions presented in **Table 2.5**), the diffusion profile (**Table 2.2**), the dielectric thickness (**Table 2.6**) and the oxide growth method – dry, wet and a combination of both – mix oxide. In the latter, the dry oxide thickness is only a small percentage of the total thickness (~100 Å) in order to improve the SiO_2/Si interface. The temperature used in all wet oxide processes was 900ºC, whereas for the dry ones, an increase in the process temperature (1000ºC) was necessary.

2.7. Electrical Characterization

Throughout the manufacturing, process control is essential to ensure that no problems occurred. A Veeco Dektak profilometer was used to measure the thickness of both materials, a-Si:H and silicon oxide. An abrupt step is necessary for a more accurate measure. The a-Si:H film thickness was measured on a sample deposited on a bare substrate glass, with a small region protected with a photoresist drop, for afterwards lift-off. Regarding the oxide, a selective etching (using HF solution) was made, plus a comparison between the color chart and the oxide thickness measured. The aluminum thickness was estimated using the BOC Edwards FTM7 Film Thickness Monitor (approximately 1500 Å).

Sheet resistance measurements were made using four-point-probe (FPP) technique (Veeco Instruments). It was used to measure sheet resistance of the shards, included in all the studies (except in the oxide one), and the indium oxide thin film deposited over glass. The latter was used to control the film properties deposited over the *pn* junctions.

For the current-voltage characteristics were used three different equipment: i) Keithley 228A, which served as a general voltage source; ii) Keithley 617, which was employed either as a source for gate voltage, as a low current ammeter (less than 20 mA) and as a voltmeter for direct measurements of the sample voltage in the case of high current measurements; iii) Keithley 195A used as ammeter when higher current values were measured. All the I-V measurements were done in a Faraday cage and under primary vacuum (9×10^{-1} mbar).

The different dopant doses used in the a-Si:H thin films were inferred from conductivity vs temperature measurements and compared to standard samples from which the SIMS profile is known. A Peltier element was used for varying the temperature between [80 - 5]ºC ± 2ºC with a 30 seconds stabilization time. The experiment control was made by computer using a K228A voltage source for powering the Peltier element and a REX-P200 (RKC Instruments) for temperature measurement. The metal contacts deposited over the film had a 4.3 mm length and a distance of 0.73 mm between them. A Keithley 617 was used to apply voltage

to the sample (100V) and to measure its current, either in dark conditions during the σ(T) measurements, or under illumination, in the end, at room temperature, using a special halogen Philips lamp (ref. 13177) which reproduces fairly well the solar spectrum for AM1.5-AM2 [53].

Static electrical characterization was conducted at room temperature using the devices previous mentioned. The metal-semiconductor contacts and the *pn* junctions were tested obtaining the I- V characteristics for each set of samples. In the junctions' tests, it was obtained two groups of curves, one in the dark and the other under illumination of a Philips 13177 halogen lamp. The first was tested using a range [-5;1] V, swept with 0.4V step and with a 5 seconds stabilization time. The latter was similar, changing only the voltage range to [-1;1] V. On **Appendix M** it's possible to see the electrical configuration used. The K228A was the voltage source and K617 measured the real voltage across the junction. The K195A was used to measure the current.

The oxide samples were subjected to both static and dynamic electrical characterizations. Firstly, it was made the static test to ensure the presence of good quality oxide. Each sample have four contacts, as represented in the **Appendix J**, tested from [-5;5] V with stabilization time of 30 seconds due to the low current values. The sample capacitance was also measured for each contact using a portable multimeter. For the dynamic characterization (C-V characteristics) it was used a 5208 Two Phase Lock-in Analyzer (EG&G PARC), a 4431 20MHz Programmable Function Generator (Schlumberger), a Current Sensitive Preamplifier – Model 181 (EG&G PARC) and a TDS 210 Two Channel Digital Real-Time Oscilloscope (Tektronix). The MOS-C structure takes time to become fully charged after a voltage step is applied, so C-V measurements can only be recorder after the device is fully charged, called the equilibrium condition (See **Appendix N**). To reach this condition a sufficient hold time is needed. This was guaranteed by the Lock-in readings of θ angle. The variation should be less than 1% relatively to the last value measured. In order to obtain a more precise measurement, the auto-range function of the Lock-in was activated and a 3 seconds time constant was used. Also, a pre-amplification of the signal was used (1×10^{-4}). Two sweeps, commuted between -5 and 5 V (accumulation to inversion), were done, one at high-frequency (19990 Hz) and the other at low-frequency (990 Hz). In order to see trapped charges, a hysteresis curve was done for each functional contact. Both input and output signals were observed using the oscilloscope.

The MOSFET characterization consisted of five different tests of the device. Firstly, both junctions, bulk-drain (BD) and bulk-source (BS), were tested in the low current configuration, connecting K228A to the drain (or source) and the K617 to the bulk and measuring the current. A DC sweep was applied, ranging from -6 to 1 V[9] with 1 second for stabilization time. The conductance and transconductance curve were obtained using the experimental assembly shown schematically in **Appendix O**. To obtain the transconductance curve the V_{DS} was held constant at -6 V and a V_{GS} sweep [0, -6][10] V was made, with a 0.2 V step, 5 seconds of stabilization time and 1 second of delay time. The conductance curve was obtained by sweeping both V_{GS} and V_{DS}, in the same interval as the transconductance curve. Also, the stabilization and delay time were the same. The gate of the MOSFET was electrically characterized, reading the current at the bulk terminal, connecting all the other terminals to the ground. In addition, a dynamic test was made (C-V curves), connecting the MOSFET as a MOS-C (short-circuit source and drain terminals), using the same assembly as explained above. Finally, an inverter circuit (See **Appendix P**) was done using a load resistor connected in series to the source terminal. The gate was connected to the function generator where a low frequency square signal of [0,-6] V was applied. The inverter was powered using the K228A voltage source.

[9] The value of the positive voltage varied accordingly to the current measured in the direct bias condition. The objective was to see the behavior in the reverse bias condition to obtain the best junction.

[10] The sweep interval differs in some samples accordingly to the MOSFET threshold voltage.

3. Results and Discussion

3.1. Electrical characterization of metal-semiconductor contacts

Metal-semiconductor contacts are a very important component of any semiconductor device. Consequently, it was important to explore how to make functional contacts, in order to be applied in the future devices produced.

This subchapter is, therefore, dedicated to the electrical characterization of the two architectures described previously, on **section 2.6.1**. As shown in a previous work [21, 23], aluminum is a p- type dopant in silicon and doesn't make a good contact to lightly doped n-type silicon. A large mismatch between the Fermi energy of the metal and of the semiconductor can result in a high- resistance rectifying contact. For that reason, it was made a study on the structure of the contacts to obtain an ohmic behavior.

An ohmic contact is defined by the fact that it obeys to Ohm's law, thus fulfilling the following two requirements: i) the threshold voltage for zero current is negligible with respect to the applied voltage; ii) the proportionality factor between current and voltage (i.e., conductivity) does not vary measurably with voltage. Both i) and ii) must be valid in a range, from about 1 mV to several Volts. Neglecting space-charge effects in the bulk, an ohmic contact will be present if the voltage drop at the electrodes is small compared with the total voltage drop across the semiconductor [54]. Therefore, if the work function of the metal is equal or smaller than the work function of the n-type semiconductor, an ohmic contact is present. In other words, it's pretended that the Schottky barrier height, ϕ_B, is zero or negative. A simple scheme showing the work function and the Fermi level, regarding the metal-semiconductor interface, is presented in **Appendix Q**. As seen in the appendix, an accumulation-type contact is the preferred ohmic contact because electrons in the metal encounter the least barrier to their flow into or out the semiconductor.

According to the Schottky theory, the barrier height depends only on the metal work function and on the semiconductor electron affinity and is independent of the semiconductor doping density. As a result, one way to vary the barrier height is by using metals of the appropriate work function [17, 55]. Despite this, in the semiconductor industry, the materials used to form contacts are metals and silicides that are stable and relatively easy to process, so, it's difficult to alter the barrier height by using metals of varying work functions. Also, it's experimentally observed that the barrier height for the common semiconductors (Ge, Si and GaAs) and other III-V compounds is relatively independent of the work function of the metal. The situation described is sometimes attributed to Fermi level *pinning* [55]. The mechanisms that cause the Fermi level *pinning* is still the subject of some disagreement, nevertheless, barrier height engineering is impractical. However, the barrier width can be easily changed varying the semiconductor doping density. Adding impurities will cause regions of high recombination rates. Also, heavily doped semiconductors have narrow space-charge region width ($W \sim N_D^{-1/2}$), allowing the electron tunneling effect [54, 55]. In order to create very thin space-charge region in the n-type silicon wafer, it's required a minimum of phosphorus surface concentration (C_s) of 2×10^{20} at cm^{-3}, as stated in the introduction chapter of this work.

To obtain the data needed to better evaluate the contact, the FPP was used for measuring the resistance and sheet resistance of the samples produced. Also, both resistance and sheet resistance values were obtained for the unprocessed 2'' n-type silicon wafer in order to calculate the background phosphorus concentration (N_{bc}).

Firstly, the 2'' wafer presented a sample resistance and a sheet resistance of 20.5 Ω and 92.4 Ω/□, respectively. With this data, it was possible to determine the wafer resistivity, ρ_W=2.6 Ω·cm, using the **equation R.2** (See **Appendix R**). This value is consistent with the range presented by the manufacturer (1-10 Ω cm). Analyzing the resistivity vs impurity concentration (n- Si) plot [19], we obtained a background phosphorus concentration of 1.8×10^{15} at cm^{-3}. This

relation is possible since sheet resistance, and therefore resistivity, is uniquely related to the surface concentration of the diffused layer and, also, to the background concentration of the wafer. Regarding the C2 set of samples, they presented a considerably smaller sheet resistance, as expected, since these samples were submitted to the diffusion of phosphorus impurities from the a- Si:H (n^+). This result implies that some of the dopant transferred become active in the silicon net. Consequently, this set presented satisfying properties, with sheet resistance of 22.9 Ω/□[11].

In order to know the n^+-layer depth (x) and the surface concentration, we must take into consideration that upon such high concentrations in-diffusion of phosphorus, the kink-and-tail profiles can be described to occur due to dual diffusion mechanism, involving point defects of different origins and charge states [56]. As shown in these previous works [11, 57] done at LMSCE, it was obtained the phosphorus concentration in both the a- Si:H film, as deposited, and after the dopant diffusion, using the SIMS technique. It was determined that, for [PH_3] = 1.5%, the dopant concentration was 1.3 × 10^{21} at cm^{-3} and that it remains constant throughout the a- Si:H film thickness. So, the initial dose (Q_{A0}) present in the C2 set was 8.5 × 10^{15} cm^{-2} (obtained by multiplying the bulk a-Si:H initial concentration for the a-Si film thickness used in the set, 650 Å). It was shown that the a-Si concentration, after the diffusion at 1000ºC, is below the solid solubility, 9.3 × 10^{20} at cm^{-3} [57]. Since the dopant source is not unlimited, the best Fick's law solution is fixed dose (Q_A) deposit, which represents a Gaussian profile:

$$C(x,t) = \frac{Q_A}{\sqrt{\pi \cdot Dt}} \cdot \exp\left(-\frac{x^2}{4Dt}\right) \tag{3.1}$$

Also, in the work previously mentioned, it was studied that **equation** 3.1 has a better correlation than when applying the *erfc*-type function. In light of the above, we obtain for the C2 set, the following parameters: Q_A = 2.6 × 10^{15} cm^{-2}[12]; C_s = 5.2 × 10^{19} at cm^{-3}; and x = 1.7 μm (using the fitting parameter D = 1.3 × 10^{-11} cm^{-2}/min[57]). According to these results, the C_s obtained is lower than the minimum required in the literature, however since it is still a high surface concentration it is expected that this method still works in order to obtain ohmic contacts. **Table 3.1** presents the results from the electrical characterization, made by the FPP, and the data obtained from **equation 3.1**:

Table 3.1 – Electrical and process parameters obtained for the C2 set.

Shard	*t* (a-Si:H) [Å]	$t_{diff/Ox}$ [min]	$T_{diff/Ox}$ [ºC]	R_S back [Ω/□]	<C_s> [at cm^{-3}]	*<layer depth>* [μm]	t_{Al} [Å]
C2-C	65± 8×10^1 (B) 60± 1×10^1 (F)	60	1000	22.9	5.2×10^{19}	1.7	1630 (B) 1400 (F)

Note: (B) and (F) means back and front, respectively.

To investigate the influence of this highly doped layer (n^+), we proceeded to the analysis of the I- V characteristics, obtained from both C1 and C2 sets. Each sample has four individual contacts, patterned in both sides of the sample. To better compare the results obtained, the square metal contacts and the diffusion area, being the latter only present on the C2 samples, were all similar and had a contact area of about 4 × 10^{-2} cm^2 and 9 × 10^{-2} cm^2, respectively. Also, regarding the samples' structure and according to the direction of current flow, these contacts are considered

[11] This value was obtained based on the **equation R.3**, with $\frac{V}{I}$ =6.8 Ω and k=0.742.

[12] Assuming that only 30% of the dopant available is integrated in the c-Si, remaining the other 70% in the poly-crystalline film, which was removed by chemical etching after being oxidized.

to be the vertical type, once the current is expected to flow mainly vertically in a rather uniform distribution [58].

In **Figure 3.1** are depicted the two sets of samples (C1 and C2).

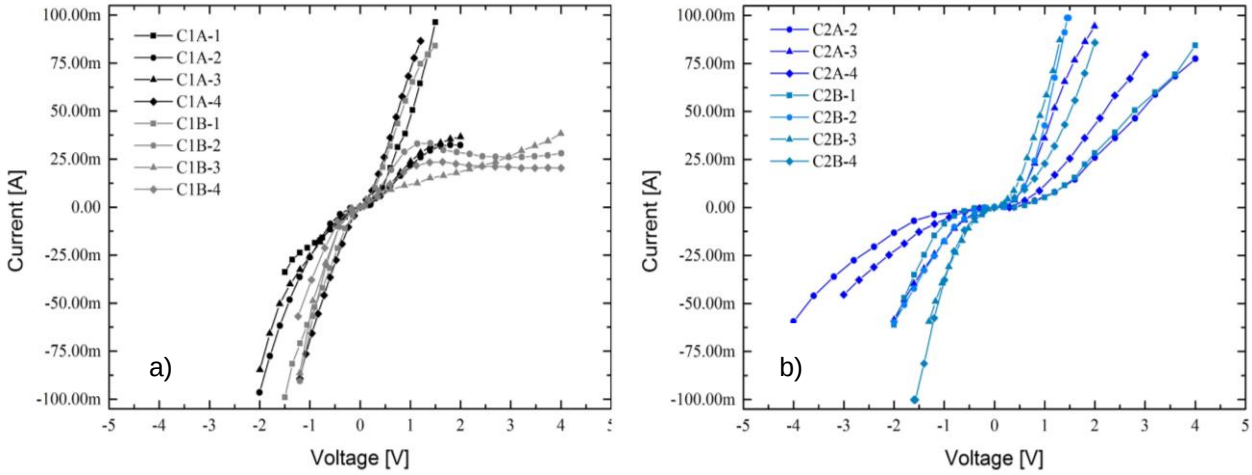

Figure 3.1 – I-V characteristic curves, without heat treatment, of the a) C1 set, where the aluminum contacts were directly deposited over the sample's surface, and b) C2 set, which received a highly doped n-type a-Si:H film for dopant diffusion.

In **Figure 3.1 a)** eight I-V curves are presented for each contact in the C1 set. The applied voltage was similar for almost every contact, except when the current limit, supported by the ammeter, was reached. As stated early on this chapter, it was expected that this metal- semiconductor junction would create a Schottky barrier, resulting in low forward voltage drop. In fact, that happen for almost every contact tested, forming a typical Schottky diode. In this case, for lightly-doped semiconductors ($\leq 3\times10^{17}$ at cm^{-3} [17]), the current flows as a result of thermionic emission (TE), with electrons thermally excited over the barrier [33] (see **Appendix S**). As experimentally observed by Werner [59], the I-V curves show to be composed of two or more components of current. The linear portion of the I-V curve is usually attributed to the main conduction mechanism, namely TE, and the leakage current is due to generation and recombination in the space charge region and edge-related conduction. However, in this lot, we can observe a significantly different behavior from the C1A-1, C1A-4 and C1B-1 contacts when compared with other. In special, the last two contacts mentioned present a *quasi*- ohmic behavior. This can be justified by a possible spatial variation of the Schottky barrier height at the metal-semiconductor interface. This barrier height variation is commonly associated with electronic states due to defects and metal-induced gap states. However, the relationship between the Schottky barrier height and the interface structure has not been assessed thoroughly [60]. Though, it is suggested that the majority of metal- semiconductor interfaces have inhomogeneous Schottky barrier heights and, consequently, the Fermi level position at the interface is not pinned, being determined by local parameters which vary spatially at the interface. As a result, the inhomogeneity in the Schottky barrier have a dominant effect on electron transport. Furthermore, the behavior of C1A-4 and C1B-1 may also be due to some impurities on the interface, enabling a higher forward current. The **Figure 3.1 b)** shows the C2 set before the heat treatment process. We can observe several differences between the two sets, however a quite big dispersion in the results is also present in this one, in special in the C2A's contacts. Once the C2A and C2B are twin samples, this dispersion may be associated with intrinsic factors of the manufacturing process. When comparing the **a)** and **b)** plots, it is clear that the C2 contacts are clearly better than the C1 ones, reaching higher current values for the same applied voltage. The n^+- layer plays an important role, once for high doping densities ($\geq 2\times10^{20}$ at cm^{-3} [17]) the barrier is sufficiently narrow at or near the bottom of the conduction band for the electrons to tunnel directly, in an effect called field emission (FE) [61]. However, it's clear that these are not ohmic contacts, once they not fulfill the requirements stated

earlier. The bending seen in the plots is due to the two back-to-back Schottky diodes. The substrate's high doping is a key factor on the malfunction of the two series diodes which, in this case, is what we pretended. The best contacts presented in this set are the C2B-2 and C2B-3. None of the contacts received a high temperature step, so they show a relatively high contact resistivity, of about 10^{-2} Ω· cm^2 [62]. The high-temperature (400-475ºC [62, 63]) anneal reduces the unintentional barrier at the interface and, consequently, further improve the contact resistivity. This process occurred in an inert environment (N_2 @ 1 lpm) which drastically reduces any further oxidation of the metal during the annealing. After this process the small barrier can be overcome through FE.

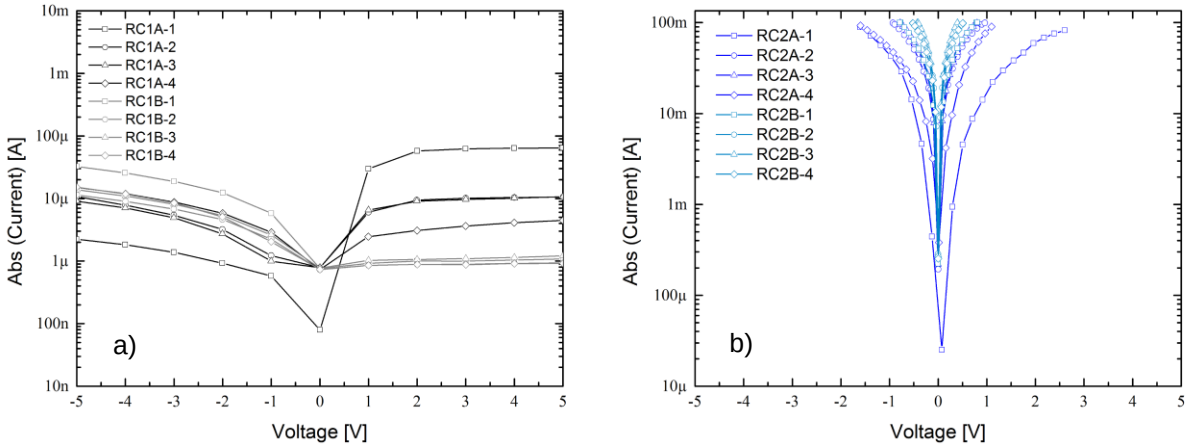

Figure 3.2 – I-V characteristic curves, after the annealing process – the letter R in the plot legend represents the heat treatment – in semi-log scale. a) C1 set, where the aluminum contacts were directly deposited over the sample's surface, and b) C2 set, which received a highly doped n-type a- Si:H film for dopant diffusion.

In **Figure 3.2** we can see both sets of samples in semi-log scale due to the low current values observed in the **a)** plot. When comparing both figures, 3.1 and 3.2, it is observed that the results' dispersion has significantly decreased. In the C1 plot **a)**, a [-10;10] V voltage range was applied and, as expected, the plot exhibits a rectifying behavior in both reverse and forward bias conditions, due to the increase of the Shottcky barrier induced by the heat process. It is clearly shown the current stabilization in both bias conditions, however, in forward bias, the rectification seems to be stronger, probably because of the better aluminum contact in the mirror side of the silicon wafer. Due to this, aluminum makes a better *pn* junction. The RC1A-1 contact presents a higher current than the rest but overall, the current values decreased by three orders of magnitude. For the reasons stated, it is clear that this structure doesn't form contacts suitable for device application. Alternatively, the **b)** plot, associated with the C2 set, shows very good results. The annealing reduced the Shottky barrier allowing the current to flow by tunnel effect. Other important factor is the specific contact resistivity which is a function of both the barrier height and doping concentration. According to Kwok [64], and considering the effects of doping on the tunneling effective mass, it is calculated that the specific contact resistivity for this samples is about 5×10^{-7} Ω· cm^2, which is below the acceptable value of 10^{-6} Ω· cm^2. For the majority of the samples, a voltage range of [-0.6;0.6] V was applied, except for RC2A-1[13] and RC2A-4 which present a higher contact resistivity than the rest. Similarly, in **Figure 3.1**, there is also a difference between the A and B batches, with the latter presenting better results. Nevertheless, the objective

[13] This contact was not tested before the annealing due to problems with the thermal compound.

to obtain ohmic contacts was reached. In **Figure 3.3**, it is possible to compare the results of both sets before and after the heat treatment.

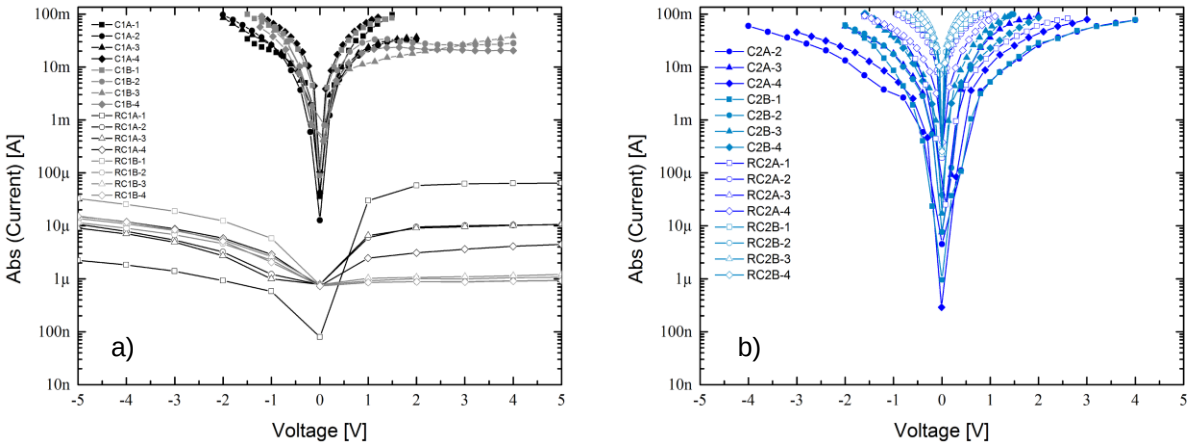

Figure 3.3 – I-V characteristic curves of a) C1 set and b) C2 set before and after the annealing. The open symbol represents the samples after the heat treatment.

3.1.1. Summary

This chapter showed the way to obtain ohmic contacts between aluminum and n-type silicon. The structure studied is equivalent to two back-to-back diodes, where the anode and the cathode are represented by the aluminum and the silicon, respectively. Before the annealing process, the two sets of samples presented a rectifying behavior and also a great result dispersion. The C1 set presented a strong rectification in the forward-bias condition, which is normal once the aluminum has a better adhesion to the mirror side of the wafer, making a better diode. The back-side of the wafer has a roughness in the micrometer range, causing the real area of contact to be considerably smaller, when compared to the mirror side, generating charge accumulation on the edges. This intensifies the electric field enabling the current to flow more easily. Besides this, the C1 set presented two *quasi*-ohmic contacts, while the rest has demonstrated the behavior of a Schottky diode. Two possible reasons were pointed out to justify this *quasi*-ohmic contacts: i) inhomogeneity in the Schottky barrier, which is usually associated with damage at the interface that affects the I-V behavior, because defects may act like recombination centers or as intermediate states for trap-assisted tunnel currents. Also, defects can alter the space-charge region width and hence the intercept voltage; ii) a surface impurity that allows a higher current flow. Moreover, it is clear that the C2 contacts have a better overall behavior and are the ones that can be applied in a functional device, despite the lower surface concentration than the literature recommended. Analyzing the I-V curves by a linear fit, we can conclude that the best ohmic contacts presented higher slopes and better statistics correlations (R^2). As a result, for the C2 set, we obtained considerably high curve slopes and R^2 values between 0.909 (C2A-2) and 0.999 (RC2B-3). Therefore, the heat process improved the metal- semiconductor interface and, consequently formed ohmic contacts in the C2 set, whereas the C1 set the rectifying behavior was strongly increased.

3.2. *pn* junctions

Most semiconductor devices contain at least one junction between p-type and n-type semiconductor regions. Such junctions show a pronounced rectifying behavior and can be used as rectifiers, isolations structures and voltage-dependent capacitors. Semiconductor device characteristics and operation are intimately connected to these *pn* junctions. The current in a *pn* diode is influenced by carrier recombination or generation within the *pn* structure. Under forward bias, the diode current is controlled by recombination and it can occur within the quasi-neutral semiconductor, within the depletion region or at the metal-semiconductor ohmic contacts. Under reverse bias, the current is mainly based on minority carriers thermally generated, but it may increase due to defect generated carriers. Moreover, carrier generation due to light will further increase the current under forward as well as reverse bias. The *pn* junction described is an essential part of the MOSFETs, which are the final goal of this work so, in order to obtain a good MOSFET device, firstly, it is necessary to obtain good *pn* junction.

To achieve that goal, in this subchapter, the influence of surface concentration as well as diffusion time and temperatures in the p^+n junctions were studied. The surface concentration was changed by varying the B_2H_6/SiH_4 flow rates, while, by changing the temperature and process time, shallow and deep junctions were created. The diffusion profiles as well as the flow rates can be consulted in **Tables 2.2** and **2.5**, respectively. Once the contact metal is aluminum, the results obtained in the previous study, presented in **section 3.1**, will be applied here. Consequently, it is necessary to deposit previously a-Si:H (n^+) films, both on the mirror and on the back side of the sample, to form the front and the back ohmic contacts[14], respectively. To summarize, the junctions' depth inside the crystalline wafer depend, essentially, on dopant concentration of the pre-deposited layer and the parameters of the drive-in step.

3.2.1. Determination of the Activation Energy (ΔE) and room temperature conductivity (σ(25ºC)) of the a-Si:H (p^+) as deposited.

During the a-Si:H (p^+) deposition process for each set of samples, an AF45 was also used in order to further measure the conductivity of the film. From this data was possible to obtain the thermal activation energy (Δ(E)) and the room temperature conductivity (σ (25ºC)). The measurement process was explained in detail in **section 2.7**.

Regarding the electrical conductivity, the distinction between localized and extended electronic states is one of the fundamental concepts in the study of amorphous semiconductors. At zero temperature, carriers in extended states are conducting, but in localized states are not. The conductivity is a macroscopic quantity which represents an average property of the carriers as they move from site to site. The calculation of the conductivity, therefore, involves the transfer rate, scattering and trapping processes, as well as the appropriate average over the distribution states. The dominant conduction path is determined by the density of states, the carrier mobility and the Boltzmann factor [24]. In unhydrogenated amorphous silicon, conduction takes place by hopping at the Fermi energy. On the other hand, in the a-Si:H, the lower defect density prevents this mechanism from contributing significantly and, instead, conduction takes place by electrons or holes at the band edges, where both the density of states and the mobility increase with energy. Thus, conduction increases monotonically with energy. For high temperatures, the conductivity is given by the **equation 3.2**

$$\sigma = \sigma_0 \cdot \exp\left(-\frac{E_c - E_F}{kT}\right) \tag{3.2}$$

[14] The only difference is regarding the contact area, being much larger in the back side of the wafer.

The σ_0 is referred to as the minimum metallic conductivity [24].

The conductivity of a-Si:H is usually thermally activated. This dependence is identifiable by three major factors: i) the location of the energy bands may change with respect to the density of states distribution; ii) the band gap is temperature-dependent, so the different band-gaps move with respect to each other as the temperature is varied; iii) the conductivity activation energy. For doped a-Si:H above the equilibrium temperature, the conductivity is activated with a prefactor of, σ_0=100 – 200 Ω^{-1} cm^{-1}, and the activation energy is 0.4-0.6 in the p-type [24]. In **Figure 3.4**, we can observe the experimental data obtained. This measurements allow to estimate the dopant in the a-Si:H films.

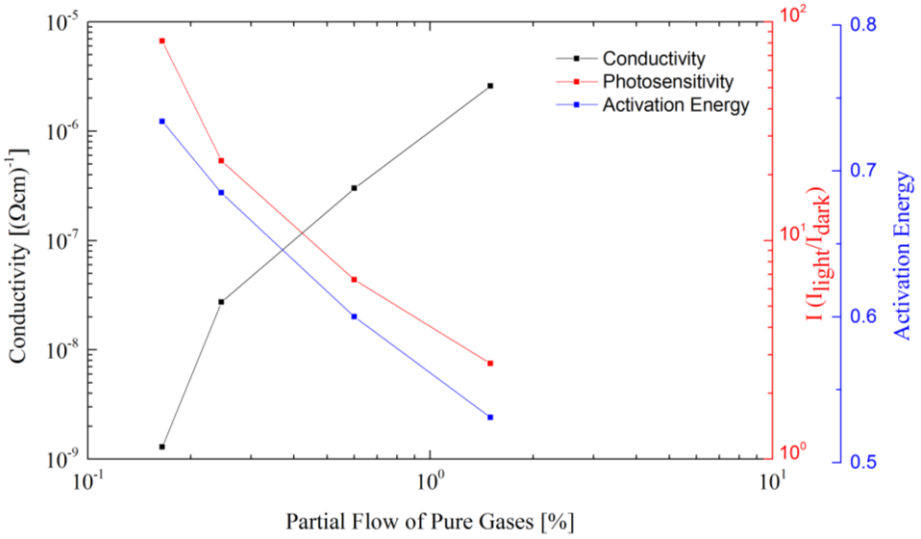

Figure 3.4 – Conductivity (log scale), Activation Energy (linear scale) and Photosensitivity (log scale) regarding the different process conditions of the a-Si:H deposited.

In the figure above we can see important information regarding the deposition process. As previously explained, although five sets of samples were fabricated, only four are present in this figure. The conditions used for the D0 set were equal to the D1, only changing the deposition time, leading to a less thick film, with the same properties, but with a lower Q_{A0}. The data suggest that with the increase of the partial flow of pure gases the current reach considerably higher values. It is an expected result, since the deposited amount of the dopant is greater, which leads to an increase in the conductivity. Also, the decrease of the activation energy indicate the dopant concentration is high with a good electronic doping efficiency. The activation energy values obtained are slightly higher than the ones described in the literature but similar with the ones obtained experimentally by Stutzmann [25]. The same author suggest that the gas-phase dopant determines the doping efficiency in the film deposited. The doping efficiencies, obtained by Stutzmann, shows similar values for both boron and phosphorus, which in our deposition method represents a chemical doping in the solid phase of about 2×10^{-2}. The photosensitivity was obtained using the special halogen Philips lamp, at room temperature.

3.2.2. Electrical characterization of the *pn* junctions produced

Before the results' analysis, it is important to mention some aspects regarding the deposition process. The growth rate and the film thickness were larger than was initially projected (based on previous depositions) which indicates that this process is not fully optimized. In **Appendix T**, is shown that increasing diborane concentration in the PECVD chamber, the film's growth rate also increases in an almost linear way. Furthermore, we can conclude that the film thickness is not directly affected by the diborane flow (see **Table 3.2**). The D3's and D4's deposit has a flow variation of about 250%, however the film thickness of D4's samples are 7% lower.

In this study two different profiles (deep and shallow junctions) were analyzed, which means that the surface concentration, previously calculated in the **section 3.1**, to form ohmic contacts

between the aluminum and the n-type silicon is no longer valid, once it is necessary another thermal step for the a-Si:H(p^+) diffusion. The D[0-4]-A samples experienced a diffusion time of one hour, at 900ºC, and the D[0-4]-B samples were submitted to a two-hour diffusion process, at 1000ºC. While the 900ºC diffusion can be neglected, the B's samples after the three-hour diffusion (in total), remained with a C_s=3.0 × 10^{19} at cm^{-3}. Although this value is lower by almost one order of magnitude than the minimum showed in the literature, it's still close to the one obtained in the previous study, so no problems due to this factor are expected.

The surface concentration as well as the junction depth was extendedly studied by several authors [65, 66]. Duran *et al.*, optimized a conventional n^+p silicon solar cell, where the junction depth must be changed according to the surface concentration value. For example, with a C_s = 3 × 10^{19} at cm^{-3}, the optimal junction depth is 0.3 µm, to obtain an efficiency of about 18.6%. On the other hand, by reducing the surface concentration to, C_s = 1 × 10^{19} at cm^{-3}, a junction depth of 0.8 µm is required to obtain the same efficiency value. In conclusion, it is verifiable a slight dependence between these two factors but the performance of the cell is practically insensitive over a wide range of values. However, Stem *et al.*, reports that emitter solar cells show the maximum range of solar cell efficiency (21.60 – 21.74%) for C_s = 1 × 10^{19} at cm^{-3} – 5 × 10^{18} cm^{-3} with 1.2 – 2.0 µm emitter thickness range. Based on these results, the dependence of the surface concentration for the two different junction depths will be evaluated using the new deposition method, adapting the deposition condition to the requirements stated. **Table 3.2** gives more information about the samples produced.

Table 3.2 – Surface concentration, junction depth and electrical parameters for the 5 sets of samples produced, D [0-4], regarding the a-Si:H (p^+) film.

Shards	*t* (a-Si:H) [Å]	$t_{diff/Ox}$ [min]	$T_{diff/Ox}$ [ºC]	R_S [Ω/□]	$\langle Q_A \rangle$ [cm^{-2}]	$\langle C_s \rangle$ [at cm^{-3}]	$\langle x \rangle$ [µm]
D0-A1	388	60	900	---	1.4×10^{14}	2.8×10^{18}	0.41
D0-B1		120	1000	1425		2.0×10^{18}	2.1
D1-A1	600	60	900	1647.2	2.2×10^{14}	4.4×10^{18}	0.42
D1-B1		120	1000	1758.5		3.1×10^{18}	2.2
D2-A1	780	60	900	1580.5	1.2×10^{15}	2.4×10^{19}	0.46
D2-B1		120	1000	868.1		1.7×10^{19}	2.4
D3-A1	720	60	900	1219.1	1.3×10^{16}	2.6×10^{20}	0.51
D3-B1		120	1000	303.5		1.9×10^{20}	2.7
D4-A1	670	60	900	1617.6	2.9×10^{16}	5.8×10^{20}	0.53
D4-B1		120	1000	296.8		4.1×10^{20}	2.8

Note: All the sheet resistance values were obtained using the **equation R.3** (*k* = 0.742). The FPP can determine the dopant type by Seebeck's effect. The equipment showed n-type for all the measurements done with the A1's shards. The D0-A1 shard presented a high sheet resistance value, close to the equipment limit, whereby the value is not presented due to the high error.

Table 3.2 sums up all the information obtained from the shards. Regarding the sheet resistance, the majority of the data collected agrees with the data presented on **Figure 3.4**, since that, with more dopant present in the a-Si:H film, i.e., higher Q_A, the R_s value decreases significantly.

The higher dopant dose increases the conductivity of the p^+ layer. The D0-A1 shard presents the highest sheet resistance and the D4-A1 presents a higher, however close, sheet resistance than the D3-A1 shard, which was not expected. This can be associated with some of the dopant being interstitial instead of substitutional, contributing to the increased sheet resistance of the layer. Moreover, we can observe that both D3-B1 and D4-B1 have approximately the same sheet resistance value, which leads us to think that there is a limit in the $\%[B_2H_6]$ in order to obtain p^+- layers with good conductivity. The slight bending of the conductivity curve, observed in **Figure 3.4**, strengthens this idea. Also, the sheet resistance of boron layers is considerably larger than the sheet resistance of phosphorus layers, due to the higher solid solubility for electrically active phosphorus in silicon. The fact that the FPP equipment show n-type for all the A1's shards can be due to the shallow junction. The sheet resistance values obtained were similar to the ones published in a work using a similar method [29]. On the junctions' depth, it was previously stated that at high dopant concentrations, the diffusion process is governed by another process [56]. The diffusion coefficients were obtained in another study [14], 8.2×10^{-13} cm^2/min for 900ºC, with a fitting correlation of 0.9994, and 1.3×10^{-11} cm^2/min for 1000ºC, previously used in the preceding sub-chapter.

Analyzing the parameters recommended by Durán and Stem, and comparing with the data presented, it seems that the best samples will be the D1-A, D1-B and D2-B. The first sample meets the surface concentration criteria, presented by Stem, although the junction depth is less than the recommended range. The second sample presents a lower surface concentration but it matches the range relatively to the junction's depth. Finally, the D2-B sample roughly match both criteria of Durán and Stem.

The results are presented on **Figure 3.5**. Although all the samples have two bulk contacts (planar and on the back side of the wafer), the results only show the data obtained using the back contact. This was due to some of the samples have a defective planar contact, once the silicon oxide formed in the diffusion process was not completely removed during the contact window etching. Also, the back contact allowed a better I-V curve under illumination, which enables a clearer view on the photo-generated carriers. Nevertheless, when the planar contact was functional, the results obtained under dark conditions were similar. The goal to test the junctions in a range of [- 5;1] V was to analyze the behavior and predict how the MOSFETs would respond under similar circumstances. The test under illumination allows a better characterization of the junctions, namely in the determination of the series resistance. It should be noted that the goal of this study was not to produce optimal solar cells, once the masks used in the process have a larger metal area than the ones used for that purpose. The samples presented a diffusion area of 0.30 cm^2. When comparing the experimental results with the 'ideal' profile discussed by Durán and Stem, we confirm that both D1-A and D1-B samples, on **Figure 3.5 c)**, have an excellent junction behavior, especially the latter, with almost 3 orders of magnitude for I(5V)/I(-5V), and an even greater difference for I(1V)/I(-1V) (See **Appendix U**). Moreover, the smooth logarithmic slope, in reverse bias, shows that the junction isn't affected by leakage problems, also indicating a high parallel resistance. In the forward bias condition, we can see the ideal diode region, where the current increases by one order of magnitude as the voltage is increased by 60 mV. Next to this region, the current becomes limited by high injection effects and by series resistance. The high injection occurs when the injected minority carrier density exceeds the doping density, therefore, occur first in the lowest doped region of the diode. This effect is more clearly seen on **a)** and **i)** plots. The **d)** plot shows a low series resistance, due to the high slope in the forward bias condition, which is another good factor. The **Figure 3.5 a)**, presents very high current under the reverse bias condition, for both junctions' profile, while on **Figure 5 e)** and **g)**, corresponding to the D2 and D3 samples, have roughly the same behavior.

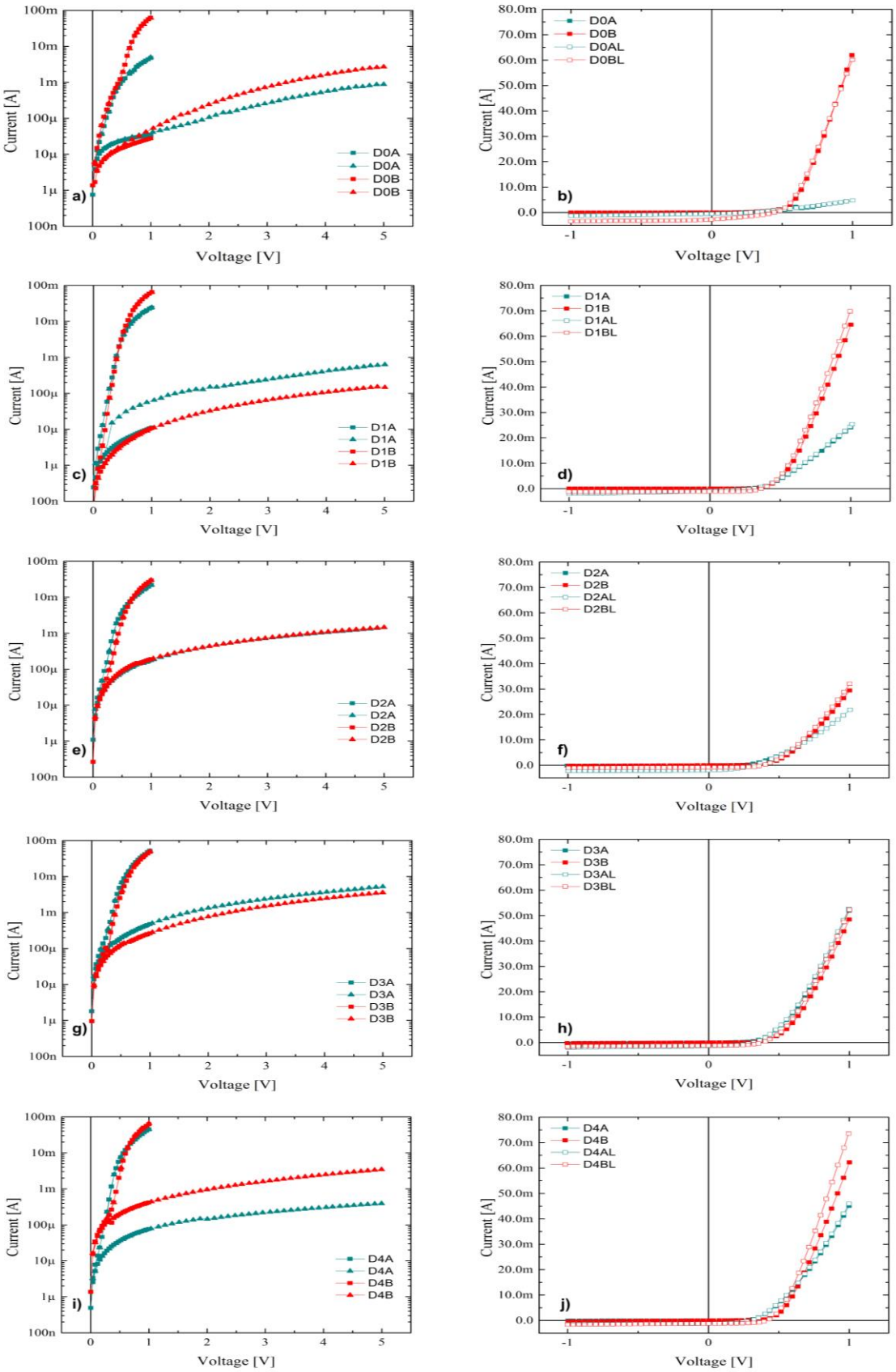

Figure 3.5 – I-V characteristic curves of all set of samples. The curves presented in the semi-logarithmic scale plot are the ones obtained in dark conditions, while in the linear scale plot is shown the comparison between the junctions' behavior in dark and under illumination (represented by an L).

Furthermore, there are no significant differences between the two profiles in these sets. This is reinforced by the **f)** and **h)** plot, which shows a high series resistance. An unexpected result is presented on **Figure 3.5 i)**, with the D4- A junction, which presents a similar behavior to the D1- B sample, despite it has a much higher dose than the range of values previously stated. A low series resistance is also observed, however, this was expected due to the low sheet resistance, which indicates a low contact resistivity. It was previously showed (**Figure 3.4**) that with the increase in the Q_A, there is an increase in the free carriers, which translates in a higher current. Despite the D4-A sample not present the best forward bias behavior, it shows a great rectification, which is an essential part to a good MOSFET.

Since this behavior was not expected, we decided to confirm this result by producing two more D4-A samples, which were named D4-A' and D4-A''. The results can be seen in **Figure 3.6**.

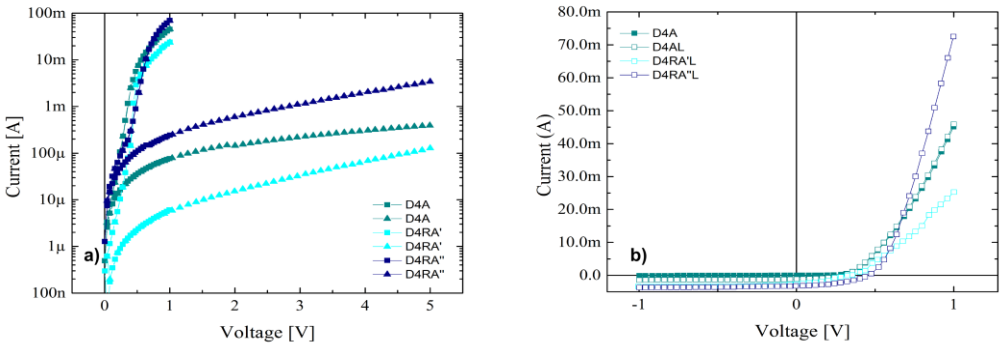

Figure 3.6 - I-V characteristics of two twin samples based on D4-A junction profile.

In **Figure 3.6 a)** we can evaluate the two twin samples produced, when compared with the original. One of them (D4R-A') shows an even better overall behavior, despite the high increase in the current when reverse biased. The second sample shows a poorer rectification regime, with very high current values, similar to what happened in the D4-B sample. We can also conclude, based on the data showed in **b)** plot, that a higher current in forward bias condition, also indicates a worse rectifying behavior. This is seen in almost every plot on **Figure 3.5**, with the exception of the D1- B sample, which combines a low series resistance and a great rectification. On **Appendix V**, some additional data can be consulted regarding all the samples produced.

The junctions are, also, usually characterized by the general breakdown, i.e., the maximum reverse bias voltage that can be applied to a *pn* diode. Breakdown is described by the rapid increase of the current under reverse bias. The corresponding applied voltage is referred to as breakdown voltage. This is a key parameter in power devices being equally important in logic devices, since typically the dimensions are reduced without reducing the applied voltage, thereby increasing the internal electric field. In this study, $N_a \gg N_d$, so the breakdown voltage can be described using **equation 3.3**:

$$BV = \frac{\varepsilon_C^2 \cdot \varepsilon_{Si} \cdot \varepsilon_0}{2q \cdot N_d} \tag{3.3}$$

where, $\varepsilon_C^2 = 2.77 \times 10^5$, $\varepsilon_{Si} = 11.9$, $\varepsilon_0 = 8.85 \times 10^{-14}$ Ḟ cm^{-1} and $q = 1.6 \times 10^{-19}$ C. Considering that $N_d = 1.8 \times 10^{15}$ aṫ cm^{-3}, the BV is equal to 140.3 V. This kind of measurements cannot be obtained with the devices available. Firstly, because the voltage sources can only generate ± 100 V, and secondly, because of the high power generated that would cause mechanical damage in the aluminum film, and consequently, in the sample.

3.2.3. Indium Oxide thin films deposited by *rf*-PERTE

As mentioned above, the curves obtained under illumination had most of the diffusion area covered by the aluminum metal. For that reason, it was decided to remove part of that metal, in order to have a larger area exposed to light. A lithographic mask (BipCon) was adapted specifically for this purpose, making a contact area of 0.04 cm^2, leaving an exposed area of about 0.26 cm^2. This procedure lead to an increase in the reverse biased current, but also to a big rise in the series resistance, reducing considerably the current in that region (See **Appendix W**). Due to this poor results, we decided to deposit a thin film of indium oxide, which is a transparent conductive oxide, over the boron diffusion area. These films are widely used in various applications, namely in solar cells, since they show high transmittance in the visible region and a low electrical resistivity when deposited under certain conditions. This is due to the non-stoichiometry produced by an oxygen deficiency [67]. The indium oxide film will form, along with the aluminum, a parallel path for current and, therefore, is expected to increase the current under forward bias condition. The film was deposited on all samples using the *rf*-PERTE technique, i.e., by thermally evaporating indium in the presence of an oxygen plasma, at room temperature[68-70]. The oxygen partial pressure varied between 4.0×10^{-4} and 3.8×10^{-4} mbar, the average thickness of the film was 170 nm and presented an electrical resistivity of 7.58×10^{-4} Ω cm. The sheet resistance, measured in a substrate glass, was 44.6 Ω/□. The technique doesn't involve any post-deposition heat treatment to optimize the film properties. However, results did not meet the expectations as can be seen in **Figure 3.7**.

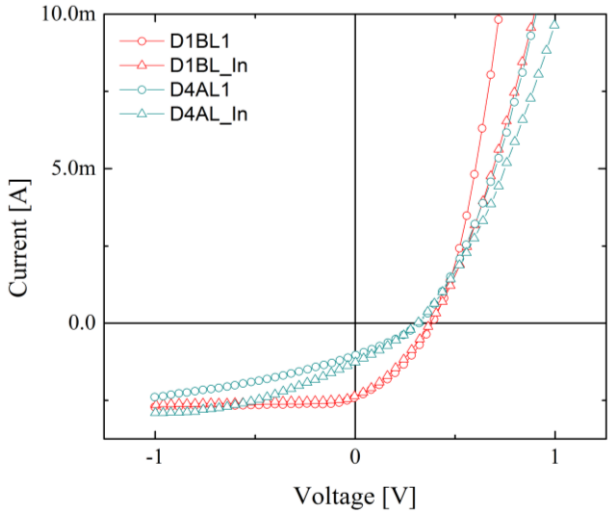

Figure 3.7 – Influence of the indium thin film on the I-V characteristics, under light conditions, for the best junction created – D1-B and D4-A.

As we can see, the indium thin film didn't improve the V_{OC}, and as further increased the series resistance. It is possible that the oxygen has reacted with the aluminum and with the Silicon, creating an oxide layer, and therefore increasing the contact resistance. In short, the film properties were not good enough to improve the junctions' behavior as solar cells.

3.2.4. Summary

Based on the results presented, it is concluded that the best samples produced are the D1-B and the D4-A. The manufacturing conditions are considerably different between the two, being the first produced with a lower dose ($[B_2H_6]$ = 0.165%) and a deep junction, and, the second one, produced with a high dose ($[B_2H_6]$ = 1.5%) and a shallow junction. The latter result was quite interesting, once it presented a higher dose than usual. To sum up, lower diborane concentration require higher junction depths, while for higher concentrations, shallow profiles are needed. These results are the opposite of what happened in the study of the n^+p diode junctions. In the **Appendix X** it is possible to see all the electrical parameters calculated for the junctions produced.

3.3. Silicon Dioxide study and MOS-C analysis

The quality and reliability of gate oxides, in MOS structures, is a critical issue in semiconductors fabrication. Capacitance-voltage (C-V) measurements are commonly used in studying gate- oxide quality in detail. These measurements are made on a two-terminal device called a MOS-capacitor, which is basically a MOSFET without the source and drain. Due to several problems related to the oxide quality and, consequently, defective MOSFETs, reported in a previous work done at LMSCE [11], it was decided to include an oxide study in this thesis. C-V test results offer a wealth of device and process information, including bulk and interface charges.

In order to obtain good and reliable MOSFET devices, a silicon oxide of good quality is needed. Therefore, in this subchapter, two different growth methods (dry and wet) were studied, as well as several oxide thicknesses (in the range of 500 – 1500 Å) to be used as gate dielectric. The semiconductor doping induces a variation in the space-charge width, consequently, two diborane doses were tested, $[B_2H_6]$ = 0.165% and $[B_2H_6]$ = 1.5%, to see how the space-charge width and the surface concentration affected the MOS-C behavior. The a-Si:H(p^+) film was deposited on half of the sample, being chemically removed after diffusion and before the oxide growth, allowing the test oxide to grow on monocrystalline silicon, and in a smooth interface. Two aluminum contacts were deposited on each half of the top side, and a bulk contact was made in the center of the sample, for connecting to substrate through a window opened in the oxide. The dry oxide growth method was done at 1000ºC with direct O_2 feeding into the furnace, while the wet method was done recurring to water vapor (from a bubbler with H_2O at 100ºC) at 900ºC. T**able 2.6** in the **sub-section 2.6.3** sums up the information given above.

3.3.1. Oxide quality and thickness

As stated earlier, silicon is easily oxidized at room conditions, forming a native oxide, however, these oxides are limited in their thickness and they are not stoichiometric SiO_2. Thermal oxidation is a slow process and depends on temperature, oxidizing agent and pressure, crystal orientation and silicon doping densities [39, 42]. Dry oxygen is usually used to grow thin oxides, used as gate dielectric, flash-memory tunnel oxides and DRAM capacitor oxides. They exhibit lower interface charges and trap sates which are of major importance for transistor operation. On the other hand, wet oxidation is normally used to grow thicker oxides (100 -1000 nm) used for device isolation and as masking layers. The electronic conditions at the Si/SiO_2 interface are interpreted within the framework of two quantities: i) ‘fast surface states’, which are electronic states within the forbidden gap of the semiconductor, located at the surface, that can act as recombination centers; ii) ‘slow states’, which are attributed to ionic contamination within an oxide covering the semiconductor surface. Their density is a strong function of the ambient and surface treatment of the sample. These charges, however, have a poor electrical contact with the underlying silicon, even when located very near the oxide-silicon interface. Moreover, these charges within the oxide are generally found to be positive, therefore, inducing a negative charge in the silicon, and thereby lead to the tendency of thermally oxidized silicon surfaces to be n-type. This are designated by surface-state charge (Q_{ss}) [71]. The surface state density in MOS structures is of major importance and it is affected by the oxidation temperature and by the heat treatment (done in an inert environment), shifting the C-V plot to higher voltage values It is roughly independent of the impurity type and concentration in the silicon.

Regarding the oxide thickness, it was already concluded that a thin oxide (less than 50 nm) presented a high leakage current that increases exponentially with electric field. Due to the high surface concentration, the first oxide grown in order to chemically remove the pre-deposition film, showed an increase in the oxidation rate, and therefore a thicker oxide on the side of the sample where the diffusion occurred. The profilometer measurements showed a difference that reached 200 Å. However, no difference was observed in both subsequent processes. For the dry oxidation, the thermal oxidation rate of heavily doped silicon depends on the amount of impurity in the oxide, so little difference is noted unless the impurity concentration in the oxide is greater than 10^{20} cm^{-3}.

For the wet oxidation, the thermal oxidation is partially controlled by a surface reaction. The oxidation rate is a function of the impurity concentration at the silicon surface, so for values greater than 10^{19} at cm^{-3}, a change in the oxidation rate was expected. The homogenous oxide color in all the sample's surface indicates that the thickness is homogeneous and, therefore, no significant differences were found between the p^+ and n^--regions [42] (See **Appendix Y**). Consequently, the samples produced had an impurity concentration below the limit stated. The dry samples (O5/Ox5 – O8/Ox8) presented a higher thickness than when calculated with the classic Deal-Grove parameters [40]. This variation was explained by Massoud *et al*. [41, 43], where *B* and *B/A* are composite rate constants rather than kinetically simple single-activated steps. A temperature-dependent activation energy was also purposed. It was observed that the rate, in the thin regime (< 500 Å), is higher than predicted by the linear-parabolic model up to 250 – 350 Å. Rate enhancement can be divided into an initial phase (until 100 Å), followed by an intermediate phase, where it decreases asymptotically to the point of onset of linear-parabolic kinetics. The oxidation-rate enhancement during this early stages can be modeled by adding a term that has a prefactor that reflects the excess rate at which the reaction proceeds. Even so, the thickness obtained experimentally was greater than the previsions for all the oxidation's time. The viscoelastic properties of the oxide and possible additional transport mechanisms in the oxide are possible explanations to the results obtained. On the other hand, the thickness of the wet process was as predicted by the Deal-Grove model.

3.3.2. C-V characteristics

Before the dynamic analysis, electrical conduction in the SiO_2 films was tested in order to see how the oxide withstand the applied voltage. A 30 seconds stabilization time was used to see what were the typical current values [72]. The silicon dioxide should be able to maintain the electrical integrity in order to not affect the performance of the MOSFET. High quality silicon dioxide can sustain 10 MV·cm^{-1} to 12 MV·cm^{-1} [34]. Also, the sample capacitance was measured, for each contact, using a portable multimeter. Considering the **equation 3.4**:

$$C = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{\mathrm{A}}{\mathrm{d}} \tag{3.4}$$

where C is the capacitance (F), A is the area of overlap of the two plates (4×10^{-2} cm^2), d is the separation between the plates (silicon dioxide thickness), ε_0 is the electric constant and ε_r is the relative static permittivity (or dielectric constant), in this case is referred to the silicon dioxide, and has a theoretical value of 3.9. These measurements allowed to see the maximum value of the oxide capacitance calculating the ε_r for each contact. Although the oxide dielectric constant may not be exactly 3.9, it is possible to do some considerations about the oxide thickness directly under the contact. Obtaining a dielectric constant below the theoretical value, indicates that the thickness in that particular region is thicker than the one measured in the bulk contact region. Moreover, if the dielectric constant has a higher value than the theoretical one, it implies that the oxide has a lower thickness in that particular region than the one measured in the bulk contact, consequently, it could mean that a locally thin region of oxide is present and it will be subjected to higher electric fields than the other areas. Almost all the contacts, of both sets of samples, presented a dielectric constant lower than 3.9, which reveals that the minimum oxide thickness is in the center of the sample or that the dielectric constant is indeed different than the theoretical value. As stated before, the samples are squares and this geometry difficult a homogeneous thickness throughout the surface. In addition, the parallel position of the samples relatively to the oxygen flux contributes to the lack of homogeneity. This effect was especially visible in the dry samples. Since the bulk contact is connected to both n^-- and p^+-regions, the higher dopant concentration of the latter makes the MOS-C device to behave like it was built on p-type substrate. This affects the energy-band diagrams and, consequently, the behavior of the MOS-C. Considering that the metal is at a negative voltage, with respect to the semiconductor substrate, a negative charge will exist on the top of the metal plate and an electric field will be induced

(perpendicular to the substrate). Due to this electric field, the majority carrier holes experience a force toward the oxide-semiconductor interface, creating an accumulation layer of holes in the oxide-semiconductor junction. The oxide capacitance of the MOS-C is measured in this strong accumulation region, since the voltage is negative enough that the capacitance is essentially constant, and the C-V curve is almost flat. Reversing the applied voltage on the top metal, the resulting electric field is in the opposite direction, therefore the majority carrier holes will experience a force away from the oxide-semiconductor interface. Since the holes were repelled, a negative space-charge region is created because of the fixed ionized acceptor atoms. The total measured capacitance now becomes the oxide and the depletion layer capacitance in series, and as a result, the measured capacitance decreases. If a larger positive voltage is applied on the top metal, the electric field will increase in magnitude and, as a consequence, a larger induced space-charge region. This implies that the conduction band is now closer to the Fermi level, thus the surface in the semiconductor adjacent to the oxide- semiconductor interface is n-type, creating an inversion layer of electrons. Above a certain positive gate voltage, most available minority carriers are in the inversion layer, and further gate-voltage increases do not further deplete the semiconductor. That is, the depletion region reaches a maximum depth. Once this condition is reached, the capacitance that is measured, by the high frequency (See **Appendix Z**), is the oxide capacitance in series with the maximum depletion capacitance. This is often referred to as minimum capacitance, being the C-V curve slope almost flat. The **Figure 3.8** shows one of the best C-V characteristics obtained from all the sets of samples.

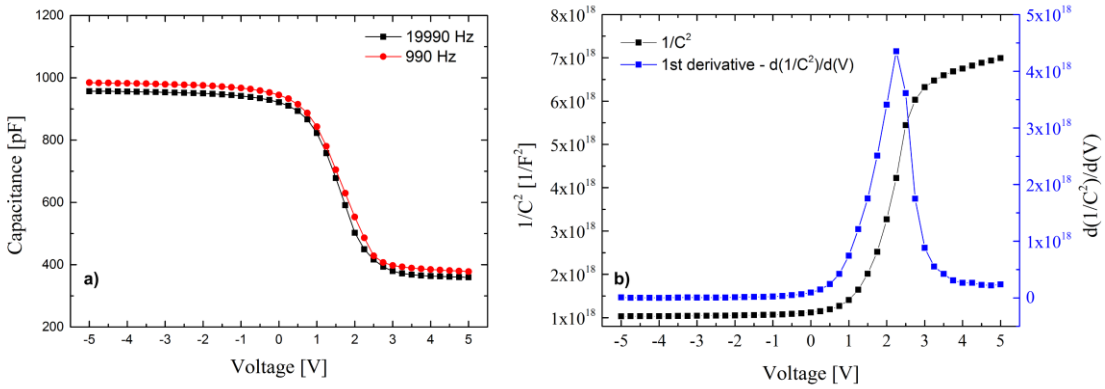

Figure 3.8 – C-V characteristics of O2 sample - ([B_2H_6] = 1.5%; wet oxide @900ºC with d_{ox} = 1300 Å); a) represents the C-V curves for both the frequencies tested and b) shows the inverse of the square capacitance ($1/C^2$) and its first derivative as function of the applied voltage.

Both sets of samples, O[1-8] and Ox[1-8], presented similar results. The two dopant concentrations used have little influence on the C-V behavior, which suggests that the maximum induced space-charge region width, for both semiconductor doping, don't change significantly the voltage value where the change between accumulation to inversion occurs. It was not possible to obtain the low frequency behavior since below 400 Hz the measurements become unstable. The **a)** plot shows the typical behavior of the MOS-C device on a p-substrate. In strong accumulation, the capacitance has a constant value, which depends mainly on the oxide thickness, as shown in the **equation 3.5:**

$$\frac{C_{\text{MOS, accumulation}}}{A} = \frac{C_{ox}}{A} = \frac{\varepsilon_r \cdot \varepsilon_0}{d} \tag{3.5}$$

Thicker oxides tend to reduce the capacitance value and increase the V_t of the device. However, due to manufacturing conditions, as stated earlier, the thin oxides grown thermally with direct O_2 flux, are not reliable and the majority of the samples produced by this method presented a dielectric breakdown voltage under the 10 V, which is an extremely low value (See **Appendix AA**). The **a)** plot presents a C_{ox} value of 2.65 × 10^{-8} F·cm^{-2} and a capacitance of 980 pF, for both

frequencies tested, and a calculated ε_r=3.83 value. The O1 sample (d_{ox} = 1500 Å, grown on heavily doped p-type Si) presented a C_{ox} of 2.3 × 10^{-8} F·cm^{-2} and a lower capacitance, of about 790 pF. The **b)** plot displays the capacitance (1/C^2) as a function of the voltage applied. This sweep yield important information about the doping profile, once the substrate doping concentration (N_{SUB}) is inversely related to the reciprocal of the slope of the (1/C^2) vs V curve. The positive slope indicates that are acceptor impurities and the N_{SUB} is 1.65 × 10^{15} at̀ cm^{-3}[15]. With this value, we can calculate the maximum space-charge width. Considering the **equation 3.6**:

$$\phi_{fp} = \phi_t \cdot \ln\left(\frac{N_a}{n_i}\right) \tag{3.6}$$

When the electron concentration at the surface is the same as the hole concentration in the bulk material, it is a condition known as the threshold inversion point. If the applied voltage increases above this threshold value, the change in the conduction band at the surface is only a slight function of the applied voltage. The electron concentration at the surface is an exponential function of the surface potential, and can be increased by orders of magnitude, however the space-charge width only changes slightly. In this situation., the space-charge region has essentially reached a maximum width [1]. At this inversion transition point, the space-charge width can be calculated using the **equation 3.7**.

$$x_{dm} = \left(\frac{4 \cdot \varepsilon_{Si} \cdot \phi_{fp}}{q \cdot N_a}\right)^{1/2} \tag{3.7}$$

Calculating ϕ_{fp} using **equation 3.6**, one obtains 0.30 V, considering a ϕ_t of 0.0259 V and a n_i (300 K) of 1.5 × 10^{10} at̀ cm^{-3}. So, the x_{dm} = 0.69 µm. The magnitude of the maximum space-charge density per unit area of the depletion region (Q_B) can be calculated using the **equation 3.8:**

$$Q_B = -q \cdot N_a \cdot x_{dm} \tag{3.8}$$

obtaining a Q_B = -1.83 × 10^{-8} C·cm^{-2}, since the substrate is heavily doped with acceptor impurities. The **b)** plot also shows the first derivative of the 1/C^2 which can help to determine the flatband voltage (V_{FB}). This parameter is the voltage at which there is no charge on the plates of the capacitor and hence there is no electric field across the oxide. It is influenced by the N_{SUB} and any residual interface charge that may exist at the interface between the semiconductor and the insulator, and by the difference between the metal (metal selection is of major importance) and the semiconductor work function, so the greater the value, closer to one the flatband capacitance (C_{FB})/C_{ox} ratio is. For ideal curves, the flatband voltage is zero [17]. The lower knee of this curve occurs for V = V_{FB}, which as a value of approximately 0.75 V. Charges can become trapped in the oxide during device operation even if not introduced during device fabrication. Carriers (electrons or holes) can be injected from the substrate or from the gate. In this situation, the flatband voltage shifts due to oxide trapped charge. Hysteresis curves were performed to evaluate this situation, but no difference in the V_{FB} was noticed. The effects of charges trapped in the oxide, during the manufacturing process, is visible in the O5 sample (see **Figure 3.9**). The surface state density in this sample is higher when compared to the rest, shifting the C-V plot to higher voltage values, increasing the value of the flatband voltage to 4 V. This shift is not attributed to the increase in the process temperature since the other dry oxide samples do not show this behavior. Also, an oxide of about 900 Å should have a significantly greater capacitance, revealing a defective oxide. This can be seen in the **Figure 3.9 a)**. The **b)** plot shows the C-V characteristics of O3 sample (d_{ox} = 1020 Å, grown on heavily-doped p-type Si). The high substrate doping doesn't

[15] Contact area of 2 × 2 mm^2.

allow a change between accumulation and inversion in this voltage range. The oxide breakdown was reached before the change was verifiable.

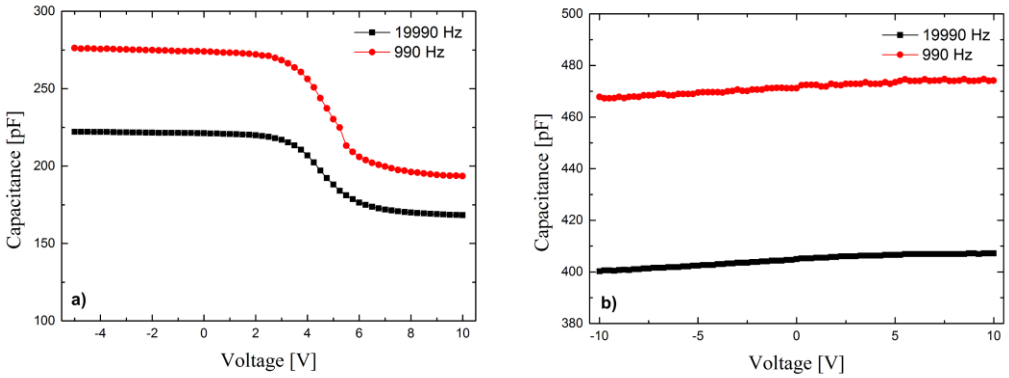

Figure 3.9 – C-V characteristics of a) O5 sample – ([B_2H_6] = 1.5%, dry oxide @1000ºC with d_{ox} = 870 Å and b) O3 sample - ([B_2H_6] = 1.5%; wet oxide @900ºC with d_{ox} = 1020 Å) - contact over the highly doped p^+- region.

3.3.3. Summary

Based on the results presented on this section, the MOSFETs will be produced using mainly wet oxides, with a thickness of about 1300 Å. Nevertheless, one set of samples will be produced with a very thin dry oxide, grown after the wet oxide, in order to test its effect in the interface, assessed through device performance.

3.4. Production and characterization of pMOSFETs

The computer and communication age has catapulted electronics to its current status as the dominant global industry. The MOSFET is the most prevalent semiconductor device in ICs, being the building block of digital, analog and memory circuits. The combination in the same circuit of both n- and p-MOSFETs led to the emergence of CMOS technology, which is the most used worldwide. Many of the process steps of microfabrication were developed originally for CMOS fabrication and later adapted to other microdevices. The scale reduction has been driven almost exclusively by CMOS technology, at a pace of roughly 30% linewidth reduction every three years [34]. With the approach of technology's physical limit, other materials and techniques are being developed. Although outside of the scope of this work, is important to refer that the field of low-temperature MOS-type transistors has suffered great advances, especially in the TFTs technology [73-75]. The low temperature fabrication reduces production cost and, furthermore, the whole process is compatible with temperature-sensitive polymer substrates, required for flexible electronics.

This final sub-chapter shows the outcome of the low-temperature pre-deposition technique combined with the results obtained in the previous sub-chapters, in order to create a functional pMOSFET, working in enhancement mode, with high mobility. Based on the results presented in **section 3.2**, it was determined that the best *pn* junctions were the D1-B (deep junction profile) and the D4-A (shallow junction profile), respectively [B_2H_6] = 0.165% and [B_2H_6] = 1.5%. Also, in the **section 3.3**, it was showed that the most reliable oxides were the wet ones, with a thickness over 1000 Å (O1 to O3)[16]. Moreover, the wet oxides were made at 900ºC, which is an advantage, since they were grown after the chemical removal of the recrystallized a-Si film, which implied another temperature step, minimizing the changes in the conditions studied for the diodes. The bulk contact was made on the back side of the wafer, using the conditions described in **section 3.1**. As in the previous studies, a shard was made for each MOSFET, to be used in all the measurements done to monitor de manufacturing process.

3.4.1. M1 and M3 characterization

Initially, were made two sets of MOSFETs, M1 and M3[17], each set had two twin samples (A and B), where it was tried to replicate the D1- B and the D4-A junctions, respectively. The oxide growth was made over the c-Si substrate, on both sets, and it was based on the O2 samples, a wet oxide at 900ºC. This situation represents a potential problem, when analyzing the M3 set, since the non-simultaneous oxidation requires a new temperature step and, therefore, this junction ends with a higher depth relatively to the correspondent diode sample. Regarding the M1 set, since it was pretended to obtain a deep junction, done at 1000ºC, a 50-minute oxidation, at a lower temperature, it is not expected to present a problem. On **Table 3.3** there are presented the data relatively to the MOSFETs described.

Table 3.3 - Surface concentration, junction depth and electrical parameters for the first two MOSFETs produced based on the best junctions obtained previously.

Shards	*t* (a-Si:H) [Å]	$t_{diff/Ox}$ [min]	$T_{diff/Ox}$ [ºC]	R_S [Ω/□]	$\langle Q_A \rangle$ [cm^{-2}]	$\langle C_s \rangle$ [at cm^{-3}]	$\langle x \rangle$ [µm]
cM1	680	120/50	1000/900	1022.2	2.4×10^{14}	3.0×10^{18}	2.3
cM3	560	110	900	---	2.4×10^{16}	1.4×10^{20}	0.64

[16] Since no significant differences were observed between the O[1-8] and Ox[1-8] sets, the two will be used interchangeably in this document.
[17] The M2 set showed blistering problems after a too quick dehydrogenation step.

Note: It wasn't possible to obtain the sheet resistance of cM3 since it exceeded the limit of the equipment. The junction depth varied about 5% and 20%, relatively to cM1 and cM3 samples, respectively. The sheet resistance regarding the highly n-doped bulk contact was under 50 Ω/□, on both shards.

The junction depth varied significantly in the M3 set, however, the results were similar to the ones presented on the **section 3.2**. The I-V characteristics of the shards produced can be seen in the **Appendix BB.** The results show that the junctions' behavior is similar to the diode study and, therefore, it is expected to work as well or even better in the case of reverse polarization, since the junction area is considerably smaller on the MOSFETs samples. **Figure 3.10** shows the I-V characteristics of the junctions obtained, for M1 and M3 samples.

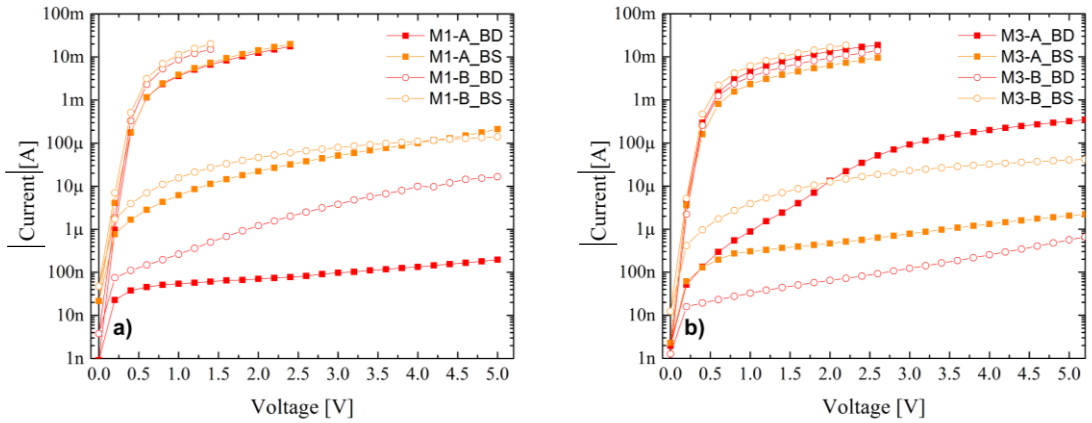

Figure 3.10 – Semi-log I-V curves of bulk-drain (BD) and bulk-source (BS) of a) M1 and b) M3 pMOSFETs.

There is no significant difference between the drain and source terminals. In the pMOSFETs, the source is the region which has the highest potential, thus, current flow from source to drain (hole carriers). The figure above helps to determine which is the best junction in order to be used to obtain the conductance and transconductance curves. The **a)** plot shows a great bulk-drain diode with a rectification ratio of 6.7×10^4 and 3.2×10^4 for |1 V|, for A and B samples, respectively. This ratio confirms the quality of the junctions. Although the current value is not available for 5 V, as explained in the electrical characterization section, we can calculate the $R_{ON/OFF}$ considering that the current reach the 100 mA limit[18]. Therefore, in these conditions, we obtain a 5.1×10^5 and 6.1×10^3 for |5 V| for A and B samples, respectively. The bulk-source diodes are similar to the ones produced in the cM1 shard. The **b)** plot shows, also, two very good junctions, namely, bulk-source, in the A sample, and bulk-drain, in the B sample. The first has a rectification ratio of 7.7×10^3 for |1 V| and 4.9×10^4 for |5 V|, while the BD junction revealed a $R_{ON/OFF}$ of 1.1×10^5 for |1 V| and 1.8×10^5 for |5 V|. The bulk-drain diode, on M3-A sample, shows an abrupt increase of the I-V curve for reverse polarization which can be associated with a lack of Si/SiO_2 interface passivation causing an increase of the junction leakage current.

The transconductance and conductance curves are showed on **Figure 3.11**. The **a)** and **b)** plots shows the transconductance curves of M1 and M3 samples. These curves reflect the good behavior of the junctions, and allow also to calculate the MOSFET parameters[19], based on the saturation mode equations (**Appendix CC**). The M1-A presents a V_t of -4.02 V. The negative threshold voltage value indicates that the pMOSFET is working in enhancement mode. The same curve allows to calculate the field-effect mobility, that for the M1-A is 106.56 $cm^2 \cdot V^{-1} \cdot s^{-1}$. The M1- B sample revealed a threshold voltage of -5.56 V and a slightly lower μ_{FE}, of 98.67 $cm^2 \cdot V^{-1} \cdot s^{-1}$. On the other hand, only one transistor of the M3 set was tested, since the oxide broke down while the curves were being obtained. The transconductance curve of the M3- A

[18] The bulk metal area is not large enough to support this current.
[19] Based on the best junction obtained.

is very similar to the one obtained in the M1 set, however, a thinner oxide allowed to obtain a V_t of -2.65 V, although the same process time was used.

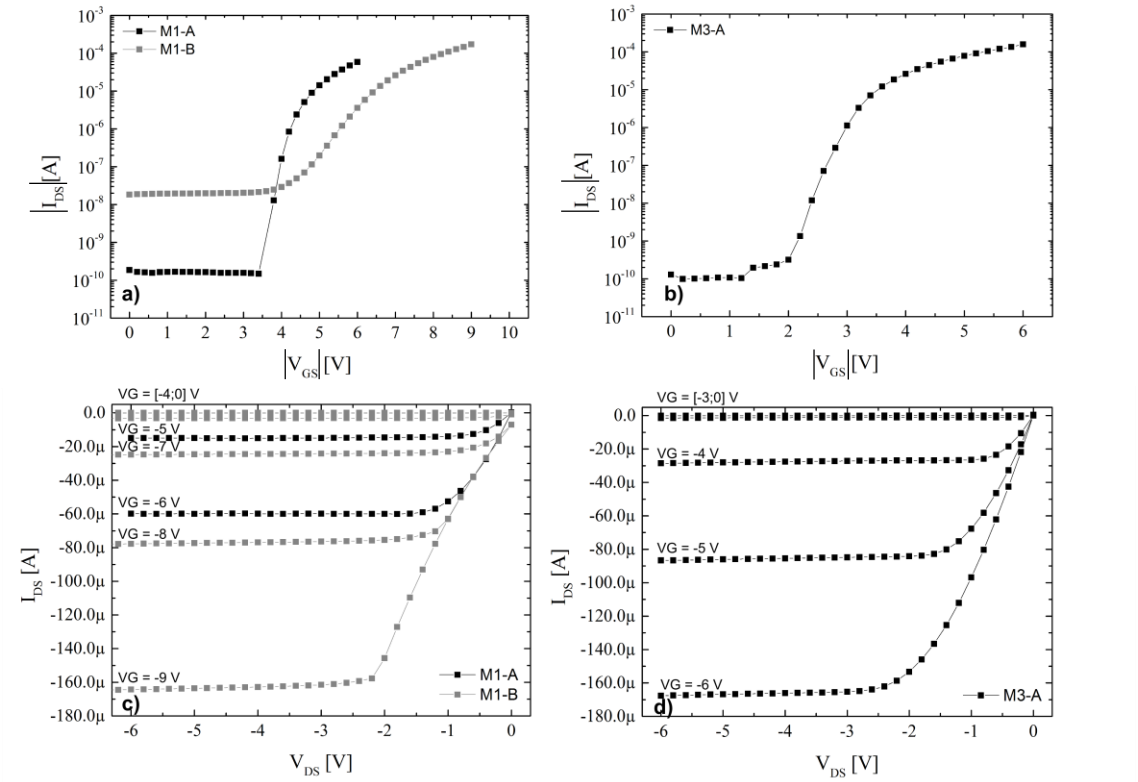

Figure 3.11 – Characteristics curves of the MOSFETs produced. The a) and b) plot are in module and show the transconductance curves of M1 and M3 samples, respectively, while c) and d) plot show the conductance curves. It was not possible to show these curves for the M3-B sample, which presented the best junction, due to oxide breakdown.

Nevertheless, the field-effect, 85.94 $cm^2 \cdot V^{-1} \cdot s^{-1}$, has a lower value than the previous set. The conductance curves were used as a way to compare the transistors produced. They can also be used to identify problems, such as a leaky oxide, allowing the current to flow through the dielectric, visible by a variation of the curve near the 0 V. In the **Figure 3.11**, c) and d) plots, we can see that the current values are considerably low, in the microampere range. Although the holes' mobility is about three times smaller than electrons, a higher current was expected. Also, the M1-B revealed problems since it needed a much higher gate voltage to reach the same current as M3- A. Comparing these results with the nMOSFETs produced in the last work [11], we see that the overall behavior is far better, with a strong field-effect, visible in the conductance curves, and especially, working in enhancement mode. However, the mobility obtained in this work is slightly lower than the one presented in [11].Also, the current obtained in the conductance curves is considerably lower, since the nMOSFETs reached tens of milliamps.

Both M1 transistors revealed problems in the oxide (d_{ox} = 1250 Å), therefore, it was not possible to obtain the gate current and the C-V characteristics for those. The gate current of the M3-A MOSFET can be consulted in the **Appendix DD**, while the C-V characteristics is shown on **Figure 3.12** regarding the same sample. The current through the oxide is of the order of few pA, proving the high quality of this oxide. The capacitance curves are different than the ones presented in the last sub-section, since the bulk contact is connected to a n-type substrate. The three regimes of operation, explained early, are inverted, since the curve goes from inversion to accumulation. The flatband voltage separates the accumulation regime from the depletion regime and the threshold voltage demarcates the depletion regime from the inversion regime. The **a)** plot shows, once again, no differences between the frequencies tested, obtaining a C_{ox} of

3.3×10^{-8} F·cm^{-2} and a maximum capacitance of 3400 pF. This is a much larger value than the one obtained in the data present on **Figure 3.8** (980 pF).

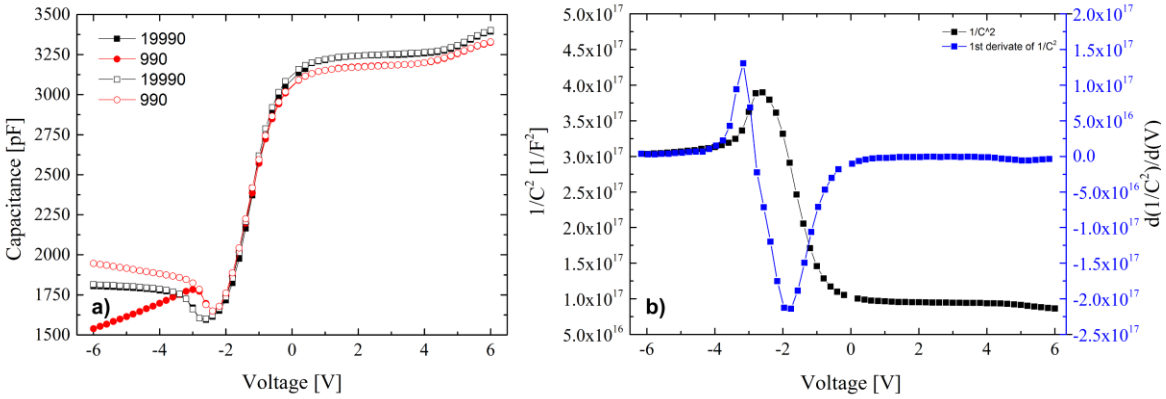

Figure 3.12 – C-V characteristics of the M3-A MOSFET – ([B_2H_6] = 1.5%; wet oxide @900ºC with d_{ox} = 1050 Å). The a) plot represents the C-V curve for both frequencies tested as well as the hysteresis curves; b) shows the inverse of the square capacitance ($1/C^2$) and its first derivative as function of the applied voltage.

The higher capacitance is explained once the oxide is thinner (about 300 Å less than the O2 sample) and the contact area is larger. It is verifiable a variation of the capacitance in the inversion regime, justifiable with a too fast sweep, which causes a maximum in the derivative function. From the **b)** plot we can see that the $1/C^2$ slope is negative, so we are in the presence of donor impurities. From this slope we obtain a N_{SUB} of 9.04×10^{16} at̀ cm^{-3} and a V_t of -2.6 V, which corresponds to the value calculated above. From the derivative, we can obtain the V_{FB}, that has a value of -0.4 V, which is a good indicator since it is closer to 0 V. We can also calculate the Q_{ss}, from the **equation 3.9**, in order to confirm the quality of the device (the calculations can be seen in detail in the **Appendix EE**).

$$V_t = \phi_{ms}^{'} + \phi_{Si} - \frac{Q_{ss}}{C_{ox}} - \frac{Q_B}{C_{ox}} \tag{3.9}$$

Likewise the previous work [11], the Q_{ss} has a value about two orders of magnitude higher [1], about 4.29×10^{-8} C·cm^{-2}, than current transistors. Although, the performance of these devices are considerably better than previously reported, mainly due to a better and thinner oxide produced, defects at the Si-SiO_2 interface, such as oxide trapped charges and interface traps continue to be limiting the performance of the MOSFETs. The effect of the oxidation temperature on Q_{ss}, in wet oxides, is nearly unchanged between 700º and 1200ºC [71], however, temperature stress caused by the bias applied can introduce more surface-states [76]. The two parameters that are most directly related to the quality and stability of an oxide are the change of the flatband voltage and surface-state density after stress. While it is possible to have an increase of surface-state density and no change of flatband voltage, a change in the latter is always accompanied by an increased surface-state density [76]. The alteration of this parameters occurred in both MOSFETs produced since the conductance and transconductance curves were affected after several measurements. Even the reverse current of the I-V characteristics of the BS and BD diodes was altered. Nevertheless, it was tried to form an inverter circuit (**Appendix P**) using a load resistor of 1MΩ, calculated using $R_{DS_{OFF}}\big|_{VGS=0\ V} = 1.2 \cdot 10^{10}\,\Omega$ and $R_{DS_{ON}}\big|_{VGS=-6\ V} = 10.3 \cdot 10^{3}\,\Omega$. Although it is visible an inversion at the output terminal, the overall performance is fairly poor (See **Appendix FF**). The gate voltage range (as seen in the figure) was increased to [0;-10] V but no change was noticed. This behavior could be explained by a low input

impedance and by the degradation in the device performance. No further test was possible since the stress caused a leak in the gate oxide.

Several other sets were made in order to obtain better MOSFET characteristics. The M4 and M5 sets also tried to replicate the D1-B and the D4-A diode junctions, respectively, but with a thicker oxide (d_{ox} = 2000 Å). The conditions used were based on the O2 samples, a wet oxide made at 900ºC for 90 minutes. However, both M4 and M5 sets produced worst diodes than the first two sets. The increase in the process time affected the junction quality. The best diode rectification was 9.2×10^2 for |1 V|, in the M5 set, about one order of magnitude lower than in the M3 set. The V_t was shifted to -20 V and the current obtained in the conductance curves was only 35 µA.

The analysis of the four sets produced showed that the best results were obtained with a $[B_2H_6]$ = 1.5%. A new set, M6, was produced with a wet oxide grown at 900ºC for 75 minutes, obtaining a thickness of about 1600 Å. This oxide thickness allowed obtaining a more robust device with a far better performance than the M4 and M5 sets. The bulk-drain and bulk-source junctions were similar, with a rectification of 1.3×10^4 for |1 V| and 5.5×10^3 for |5 V|. The M6-A MOSFET presents a V_t of -12.84 V. This MOSFET is also working in enhancement mode and presented a field-effect mobility of 61.90 $cm^2 V^{-1} s^{-1}$. This is the lowest mobility value obtained for all the functional transistors produced, nevertheless, it showed good transconductance and conductance curves, reaching the 350 µA in the latter, with a gate voltage applied of -20 V. Both curves can be seen on **Figure 3.13**.

Two more sets were produced (M7 and M8) in order to test different gate oxides, namely stacked wet/dry and fully dry oxides. The M7 set was made using the same process conditions as in M6, but with a stacked oxide (50 minutes WetOx followed by a 90 minutes DryOx) grown at 900ºC. Although the target oxide thickness was 1200 Å, the result was an oxide thickness of only 800 Å. The M8 set was made using a gate oxide grown by the dry oxidation method, at 1000ºC for 120 minutes. The increase in the process time and the higher temperature used in sets M7 and M8 severely affected their junction behavior and, consequently, the performance of the device as a MOSFET. In addition, both oxide combinations didn't show a significant improvement in the oxide quality since it broke down for a gate voltage under -25 V.

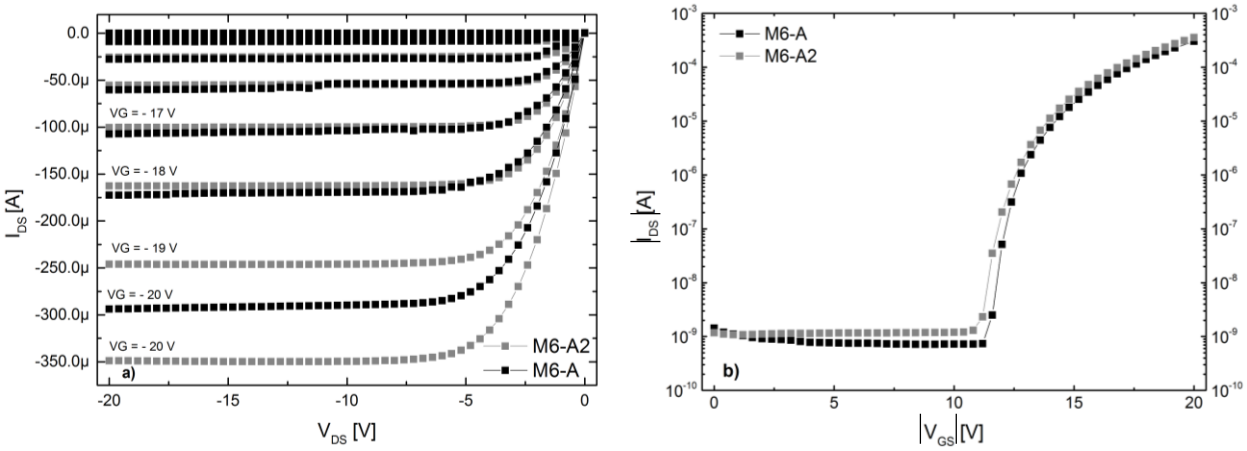

Figure 3.13 – Characteristics curves of the M6 MOSFETs produced. The a) plot show the conductance curve while the b) plot show the transconductance curve, in module.

4. Conclusions and Future Perspectives

The goal of this work was the fabrication, characterization and improvement of pMOSFETs, fabricated with an innovative production step, which consists on the dopant pre-deposition using a low temperature (90ºC) PECVD technique. The work was successful and the objective of achieving a fully functional pMOSFET was reached. In addition, it was possible to produce pMOSFETs working on enhancement mode, with a good threshold voltage and field-effect mobility. This final chapter is focused on giving some final remarks on the work presented as well as giving some insights for future perspectives.

The preparation and detailed processing sequence of a material from crystal growth to device and circuit fabrication determines the microstructure and, therefore, the electronic properties of the material and resulting device and circuit performance, yield and reliability. Regarding this, the first study was dedicated to the electrical characterization of the metal-semiconductor contacts. A good aluminum contact with the n-type silicon wafer is of major importance and the objective was to determine which fabrication conditions allowed obtaining ohmic contacts. Aluminum works as a p-type dopant in silicon and, therefore, doesn't make a good contact on lightly doped n-type silicon. Two sets of samples were made to see the influence of doping concentration and annealing in the formation of ohmic contacts. According to the literature, it is necessary to create a narrow space-charge region in the n-type silicon wafer and this is obtained with a minimum phosphorus surface concentration of 2×10^{20} at cm^{-3}. For that, the C2 set was doped using an a-Si:H thin film - [PH_3] = 1.5%. On the other hand, the aluminum contacts were directly deposited on the C1 set. To evaluate the contacts, it was used the FPP, for measuring the resistance and sheet resistance, and some previously obtained SIMS data. The sheet resistance of 22.9 Ω/□ implies that some of the dopant transferred in the diffusion becomes active in the silicon net. Before the annealing, both sets presented a rectifying behavior. However, after the annealing step, the metal-semiconductor interface was improved. The C2 samples presented the desired behavior despite of having a lower surface concentration (5.2×10^{19} at cm^{-3}) than what is stated in the literature.

The following study was to determine the influence of surface concentration, diffusion time and temperature on the p^+n junctions. The B_2H_6/SiH_4 flow rates were varied between 0.165% and 1.5% and by changing the temperature and process time, shallow and deep junctions were created. After analyzing the results, it was concluded that the best samples produced were the D1-B and the D4-A. The first sample is a diode with a deep junction and made using a low dose in a-Si:H ([B_2H_6] = 0.165%) while the second diode was produced using a high dose ([B_2H_6] = 1.5%) with a shallow junction. The D1-B presented a V_t of 0.53 V, an ideality factor of 1.74 and $R_{ON/OFF}$ of 6.01×10^3 while the D4-A showed a V_t of 0.46, an ideality factor of 2.58 and $R_{ON/OFF}$ of 3.94×10^3. The results showed that the diodes with lower diborane concentration required a deep junction profile. Moreover, the diodes with high diborane concentrations have a better behavior with shallow profiles. An indium oxide (InOx) thin film was deposited afterwards in order to improve the series resistance, however the opposite result occurred. A possible explanation is that the ionized oxygen used in the InOx deposition process reacted with the aluminum creating an oxide layer. This layer increased the contact resistance.

The oxide quality is a critical factor in the MOSFET performance. This was an important study to determine what were the best conditions to be used in the growth of the gate oxide. Two different growth methods (dry and wet) were tested, with different thicknesses, in the range of 500 to 1500 Å. Some variations obtained in the oxide thickness show that the oxidation process is not fully controlled. Also, the sample position, parallel to the oxygen flux, and the lab conditions contribute negatively to the lack of homogeneity and poor oxide performance. This requires a more intensive study on how to improve the interface between the silicon and silicon dioxide. On the other hand, a study regarding the chemical composition of the oxide would help determine what are the problems related to the oxide leakage. Although silicon dioxide is the best dielectric

to use, it would be interesting to study a different dielectric, such as the silicon nitride. Overall, the oxides produced could not withstand high voltages, while the best results were obtained using wet oxides, made at 900ºC, with a thickness of 1300 Å.

The final study was producing functional pMOSFETs working in enhancement mode. These devices were fabricated with the results of the previous studies. The first two sets were based on the best diodes obtained. The gate dielectric was grown at 900ºC with a target thickness of 1200 Å. Although the fabrication conditions were different relatively to the diodes manufacturing, the junctions presented good I-V characteristics. The best junctions were used to obtain the characteristic curves of the MOSFETs. The M1-A transistor presented a threshold voltage of -4 V and a field-effect mobility of 106.56 $cm^2 \cdot V^{-1} \cdot s^{-1}$. This was the highest mobility value obtained in all the MOSFETs produced, although it was expected to obtain an even higher mobility value. Also, the current value, in saturation, was expected to be higher. The M3-A had a thinner oxide and, consequently, the threshold voltage shifted to -2.65 V. The field-effect mobility, 85.94 $cm^2 \cdot V^{-1} \cdot s^{-1}$, has a similar value to M1 set. The main problem with the fabricated devices was the gate dielectric, which could not keep its properties throughout the tests. Several oxides presented significant leakage currents. This problem is probably one of the reasons of the poor performance of the MOSFET in a resistive inverter circuit. Although it's possible to see the inversion at the output terminal, the output voltage could not reach the desired value. Even using an ampop to increase the input impedance, no change was noticed. After the first test, the R_{DSoff} decreased significantly which highlight the oxide leakage problems. Other devices were built, with a thicker oxide, 2000 Å, but the performance were fairly poor. The M6 set (d_{ox} = 1600 Å) presented a threshold voltage of -12.84 V, which is a high value (in module), and a field-effect mobility of 61.90 $cm^2 V^{-1} s^{-1}$, which was the lowest value obtained. Despite this, the characteristic curves presented a good behavior and higher currents were obtained. A mix oxide and a purely dry oxide were used as gate dielectric but both sets didn't perform as expected.

This pre-deposition technique applied to MOSFETs production presents a novelty and it's possible to imagine future projects for this specific area. Although this technique can't be applied to state of the art transistors, which use mainly ion implantation as doping process, it can be very useful to some market niches, where ion implantation may not be used. Also, it would be a very useful technique to be applied in the bipolar transistor fabrication, as it reduces the total number of high temperature processes.

5- References

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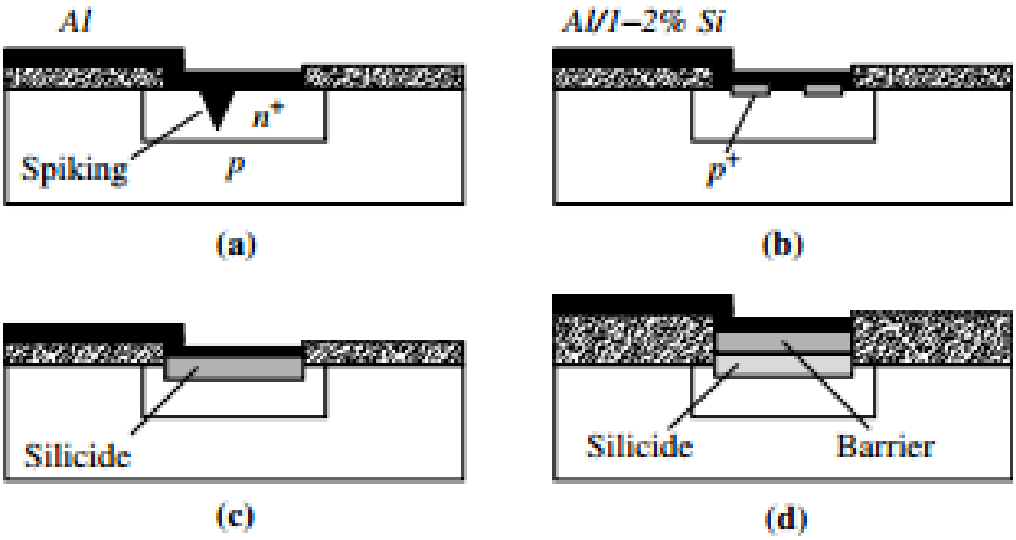
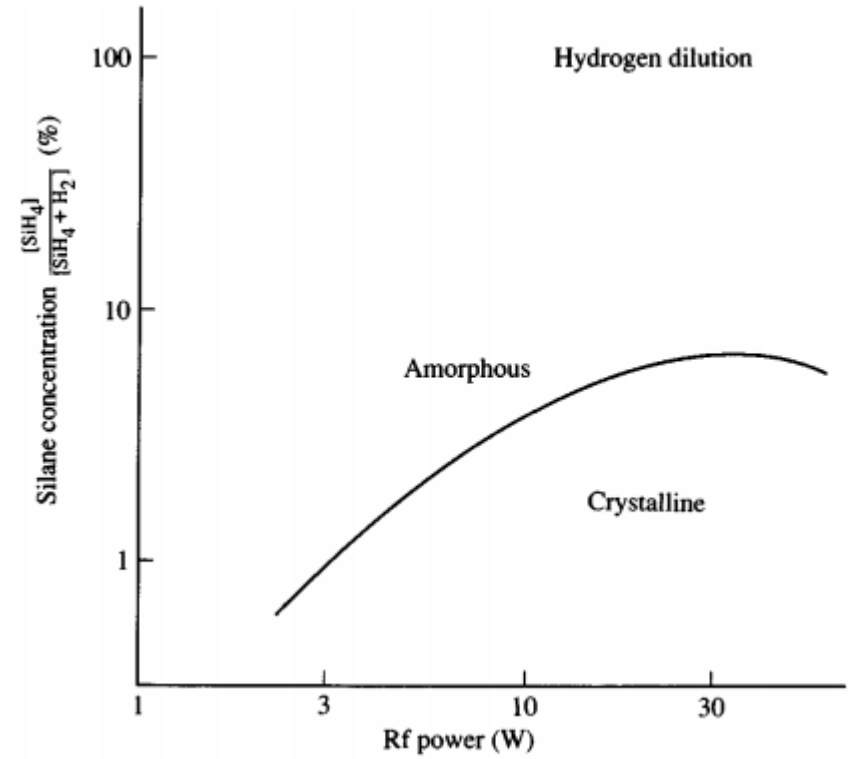
6- Appendix

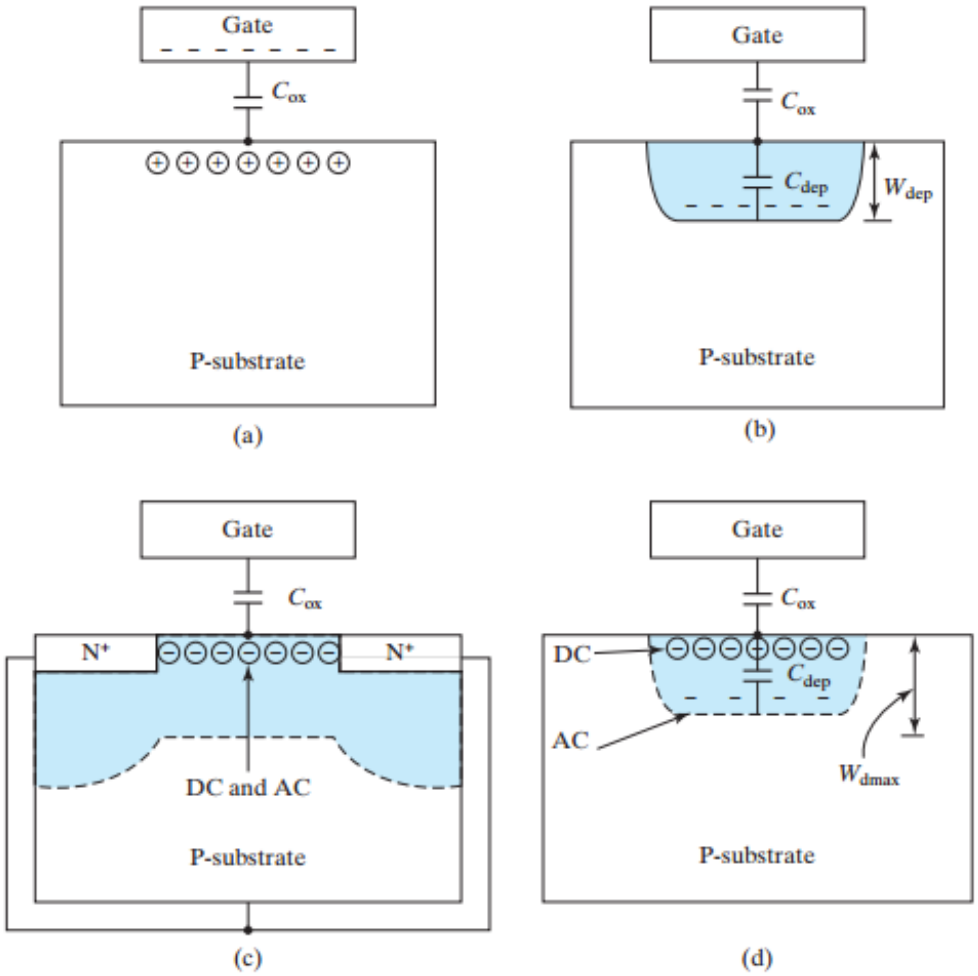
Appendix A – Historic progression of ohmic contacts in Si technology: (a) Al/Si, (b) Al/1-2% Si, (c) Al/silicide/Si, and (d) Al/barrier layer/silicide/Si.



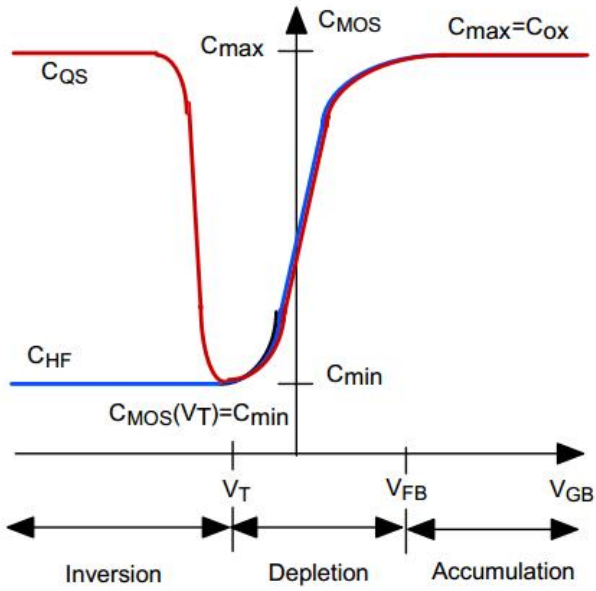
Appendix B – Diagram showing the typical deposition conditions for micro-crystalline silicon and a-Si:H films deposited from silane/hydrogen mixtures at different *rf* power.



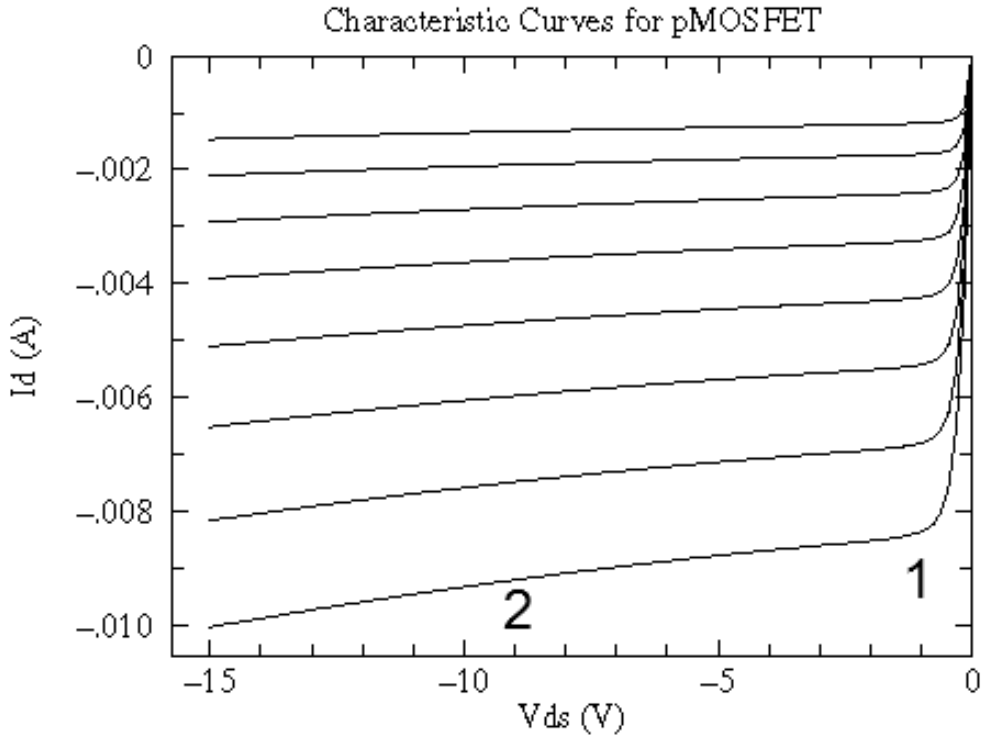
Appendix C – MOS-C in all bias regions; (a) Accumulation region; (b) depletion region; (c) inversion region corresponding to the quasi-static behavior; (d) inversion region corresponding to the high-frequency capacitor case.



Appendix D – Typical MOS-C diagram for n-substrate. C_{HF} is high frequency capacitance while C_{QS} is quasi-static or low frequency capacitance.



Appendix E – pMOSFET (enhancement) conductance curve- Numbers 1 and 2 represent the linear region and the saturation region, respectively. In the cut-off region (not shown in the picture), the device completely blocks the current flow.



The three regions previously mentioned can be described mathematically. The cut-off region is when we have[20] $V_{SG} < 0$. This condition implies a I_{SD} = 0. In some applications, namely in analogic circuits and low-voltage low-power integrated circuits [77], the transistor can work in weak inversion, $0<V_{SG} < |V_t|$. When we have the situation where, $V_{SG} > |V_t|$, the transistor start to respond with a linear ohmic behavior (**region 1**). For a $V_{SD} \leq V_{SG} - |V_t|$ condition the device current can be described by:

$$I_{SD} = \mu_p C_{ox} \frac{W}{L}\left[\left(V_{SG} - |V_t|\right)V_{SD} - \frac{V_{SD}^2}{2}\right]\left(1+\lambda V_{SD}\right) \quad \text{(E.1)}$$

Where C_{ox} is the dielectric capacitance per unit area, μ_p is the field effect mobility of holes and W and L are the channel width and length, respectively. The **equation E.1** is known as the 'square law' describing the current-voltage characteristics in the linear or triode region. For small V_{SD} the V^2_{SD} term can be neglected. For larger values of V_{SD} (but still smaller than V_{SG} - $|V_t|$) the negative parabolic dependence cannot be disregarded.

In the saturation region (**region 2**), $V_{SD} > V_{SG} - |V_t|$, and the current device is given by:

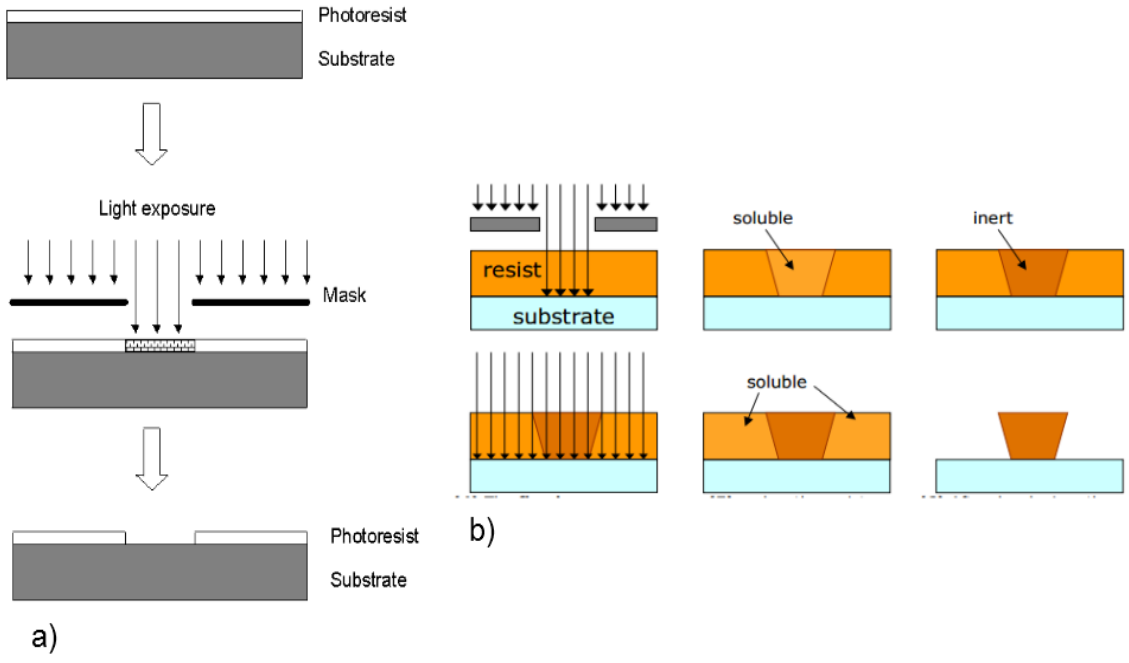
$$I_{SD} = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}\left(V_{SG} - |V_t|\right)^2\left(1+\lambda V_{SD}\right) \quad \text{(E.2)}$$

Equation E.2 shows that the total channel resistance increases, evidenced by a bending of the I_{SD} output curve. In this region, an increase in V_{SD} results in little change in I_{SD} as the channel depth reduces to zero and, eventually, pinches-off. Above this point, the channel length is reduced

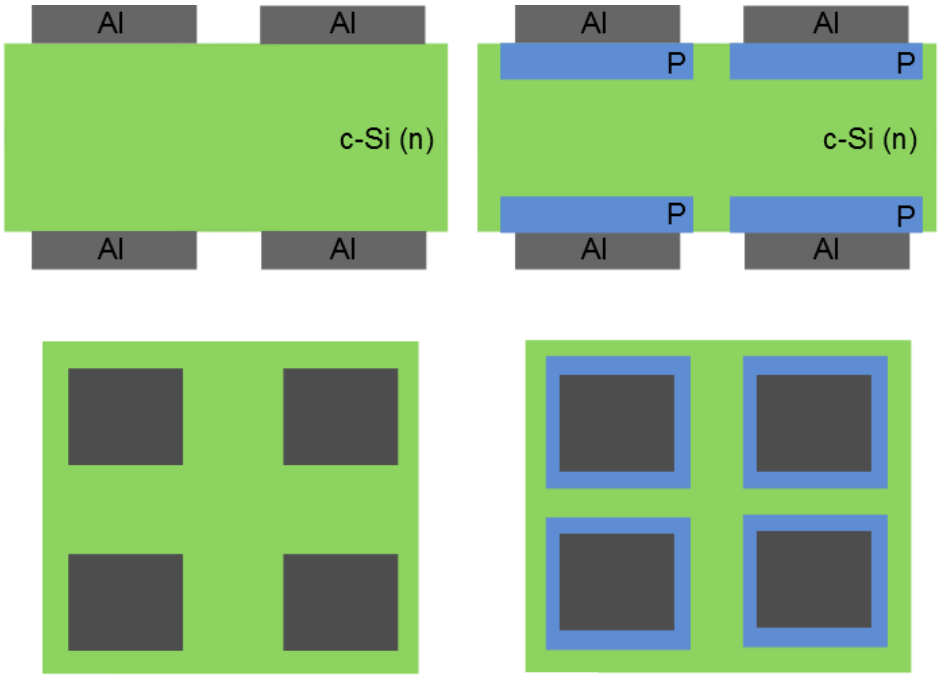
[20] The mathematical approach is done using V_{SG} and V_{SD} in order to obtain positive voltage values.

by a value ΔL. Fractions of the channel that is pinched-off depends linearly on V_{SD} because the voltage across the pinch-off region is $V_{SD} - (V_{SG} - |V_t|)$, so, $\frac{\Delta L}{L} = \lambda V_{SD}$, where λ is known as the channel-length modulation parameter. The λ parameter causes the dependence of drain current on the drain voltage in saturation. Typical values are included in [0.001 – 0.1] V^{-1}. For long channel MOSFETs this parameter can be neglected. In this work the MOSFET dimensions are: channel length and width of 0.5 and 5 mm, respectively.

Appendix F – Schemes of both photoresists used. a) Represents the AZ 1518 as diffusion mask. The n-type c-Si is coated with the photoresist and exposed to light. The area exposed to the UV light is removed (positive photoresist) and that's the region where we pretend to deposit the a-Si:H thin film. After the deposition process, the remaining film is removed by lift-off, plunging the sample in acetone. b) Represents the TI-35E – IRR. The first step is the exposure using a negative mask. After that, the film behaves like an exposed positive resist. The reversal bake step cross-links the exposed area, while the unexposed area remains photoactive. For removing the remaining photoresist is done a flood exposure (without a mask). This makes the resist, which was not exposed in the first process, soluble in the developer. After the developing, the areas exposed in the first step remain.[78, 79]

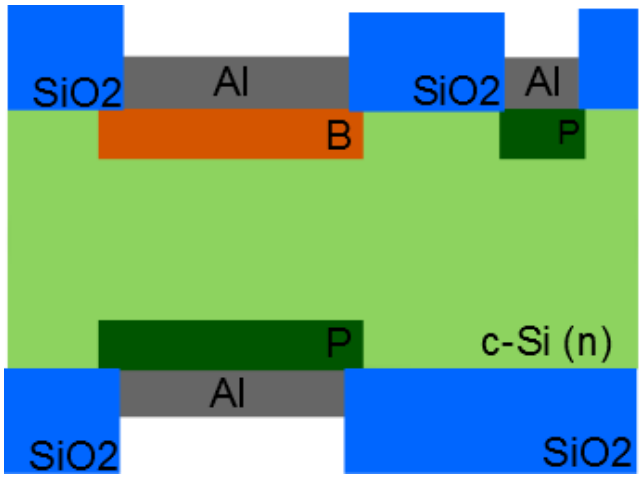


Appendix G – In the scheme we can observe both set of samples described. a) represents C1 – (A and B) where the aluminum is deposited directly over c-Si surface and b) shows a highly doped n-type region under the aluminum contacts.

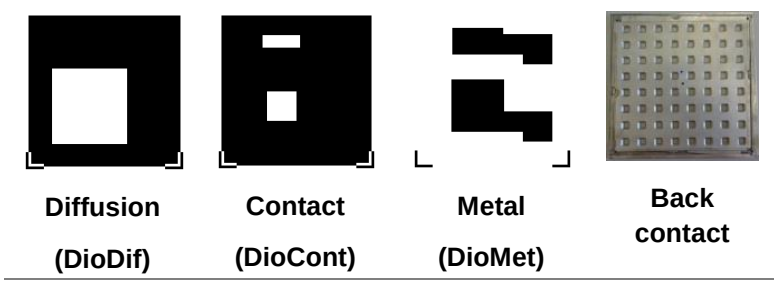


a) b)

Appendix H – General schematic of the fabricated p^+n junction. The different diffusion profiles are not represented. Also, in the sequence of the previous study, an n^+ region is necessary for an ohmic contact with the bulk (planar and back bulk contact).

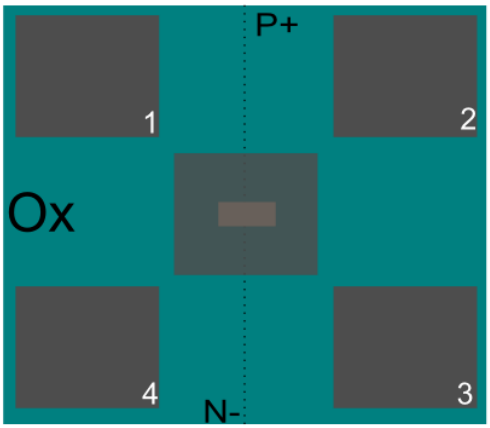


Appendix I – Masks used in the lithography process of *pn* junction; Set LoCoDio.



Diffusion (DioDif)	Contact (DioCont)	Metal (DioMet)	Back contact

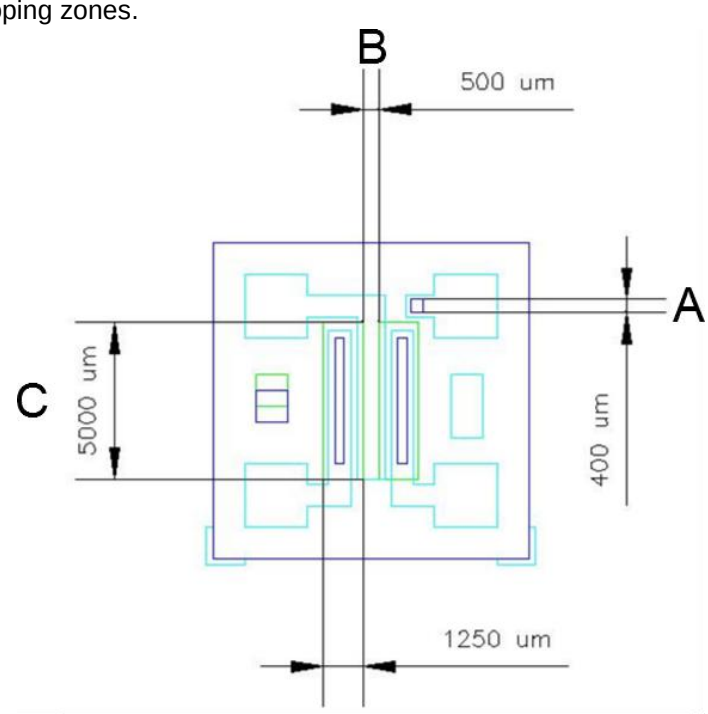
Appendix J – General scheme of the samples used in oxide study (top view) with the contact numbered clockwise for electrical characterization.



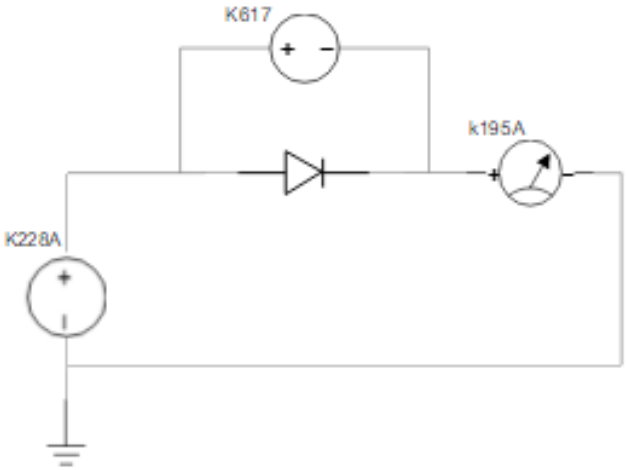
Appendix K – Masks used in the lithographic process for pMOSFEt fabrication. Set LoCoMOS. The aluminum back contact was made using the mechanical mask showed in **Appendix I**.

Source and drain regions (MOSDS)	**Contact (MOSCONT)**	**Metal (MOSMET)**

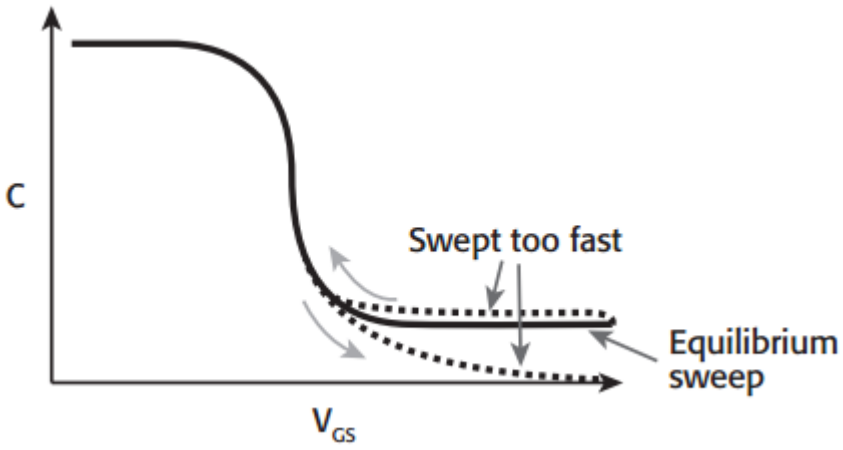
Appendix L – Masks for MOSFET fabrication, indicating: (A) bulk contact (not used), (B) gate region and (C) doping zones.



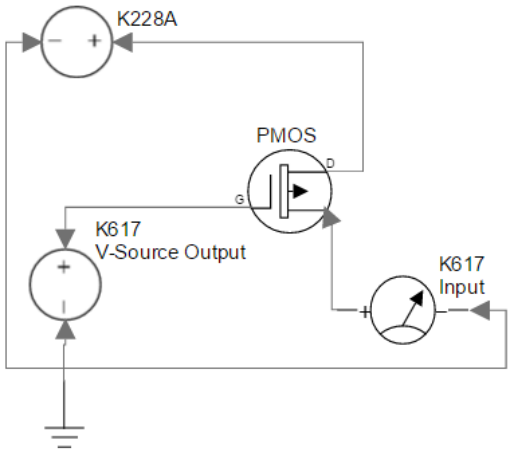
Appendix M – High current installation for I-V characteristics acquisition used in the tests for metal-semiconductor contacts and *pn* junctions.



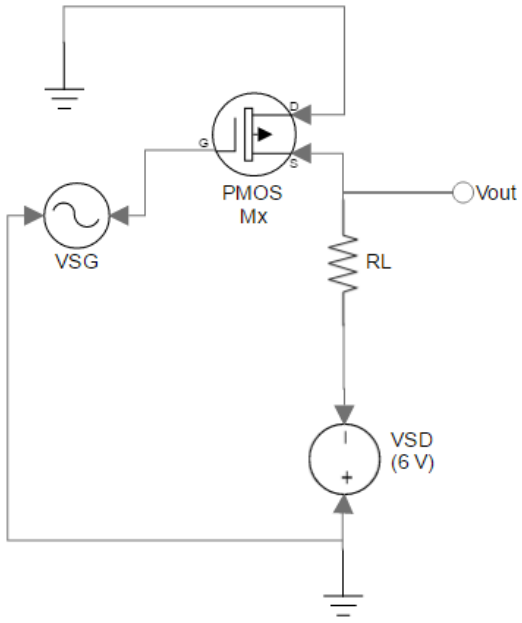
Appendix N – Effects of performing a C-V sweep too quickly. The figure illustrates the result obtained with a p-type semiconductor substrate [80].



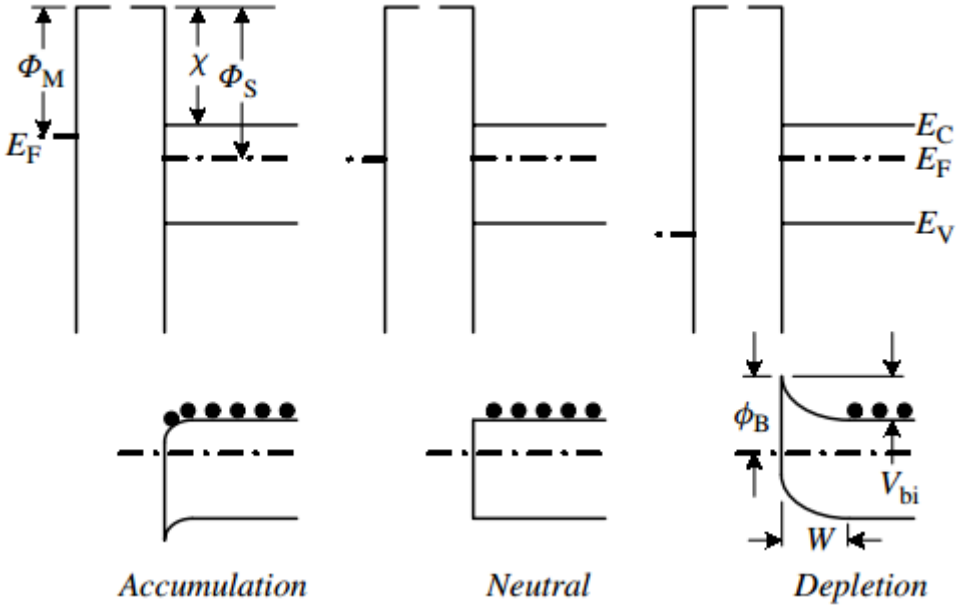
Appendix O – Experimental assembly to obtain MOSFET characteristics curves. The Input, represent the ammeter and the V-Source Output the source terminal which allows to apply voltage.



Appendix P – Inverter circuit using a pMOSFET with a series load resistor. The V_{DS} voltage was applied using the K228A. The value used varied accordingly to the V_t. A square wave applied with the function generator was connected with the gate terminal. Both input and output signals were connected to the oscilloscope to verify the effect pretended. The circuit was obtained using LTSpice software.



Appendix Q – Metal-semiconductor contacts according to the simple Schottky model. The upper and lower parts of the figure show the metal-semiconductor system before and after contact, respectively [17].



Appendix R – The four-point-probe (FPP) is a common technique in the semiconductor industry for measuring bulk resistivity (ρ) and sheet resistance (R_s). To start with, it does not require special sample shape, the probes may contact the top surface without causing much damage, and, finally, it may be moved about on the sample surface to give readings on a small area.

A given value of the V/I ratio is not uniquely related to ρ or R_s, rather the relation depends on the probe and sample geometries. As the production line wafers are neither infinitely thick nor infinitely large horizontally, correction factors are needed to obtain ρ of the wafer. In the

measurement of the 2'' silicon wafer, we may consider that it is infinitely large, once the distance between the FPP probes (0.16 cm) are considerably smaller than the diameter of the sample (5.08 cm). Nevertheless, the relation between the intertip spacing and the thickness of the wafer (280 × 10^{-4} cm) is smaller than 0.5, so it's recommended to apply **equation R.1** [81].

$$\rho = \frac{\pi}{\ln 2} \cdot t \cdot \frac{V}{I} \text{ for } (t/s \leq 0.5) \quad \text{(R.1)}$$

The first factor (π/ln 2) appears in the van der Pauw formula and it is approximated by the numerical value of 4.53. The *t* refers to the sample thickness and *s* for the intertip spacing.

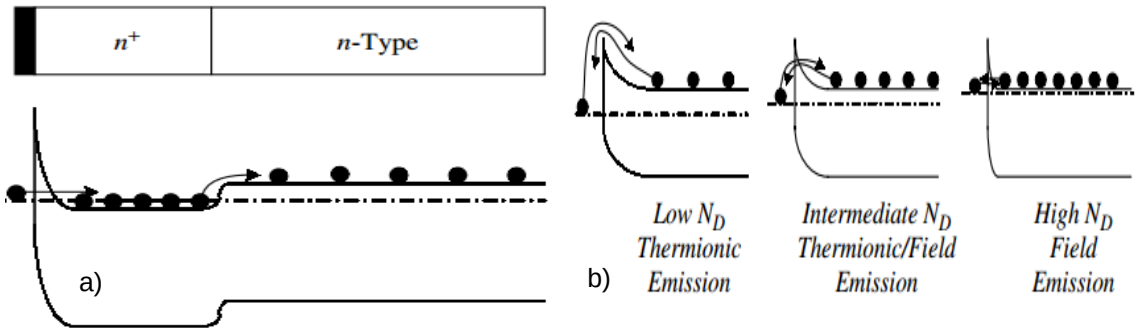
The large majority of FPP measurements performed in this work are made on small and thin diffused layers. In this situation, a *k* factor is introduced, in order to correct the basic R_s equation for the particular sample shape and size in the horizontal plane.

$$R_s = \frac{\rho}{t} \quad \text{(R.2)}$$

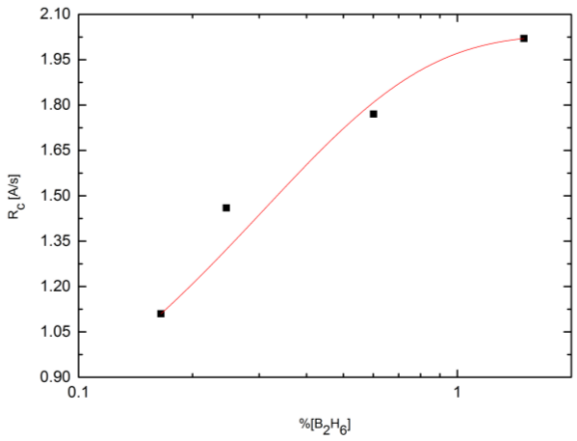
$$R_s = \frac{\pi}{\ln 2} \cdot \frac{V}{I} \cdot k \quad \text{(R.3)}$$

The **equation R.2** defines the sheet resistance for samples and implanted layers that satisfy the thin criterion. When a geometrical correction is necessary, it's used the **equation R.3**. The *k* constant is close to unity in the cases mentioned above, otherwise, a first order correction must be added. The values are tabulated and can be consulted elsewhere [82]. The exact treatment would require the summation of the potential from an infinite three-dimensional array of dipoles.

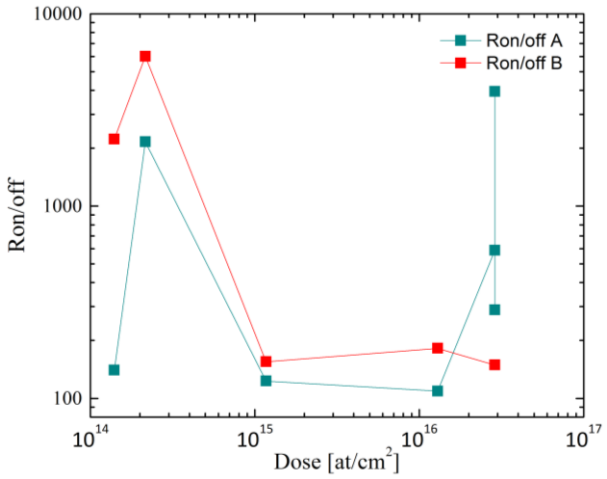
Appendix S – a)A metal-n^+ - n semiconductor contact band diagram and, b) depletion-type contacts to n-type substrates with increasing doping concentrations [17].



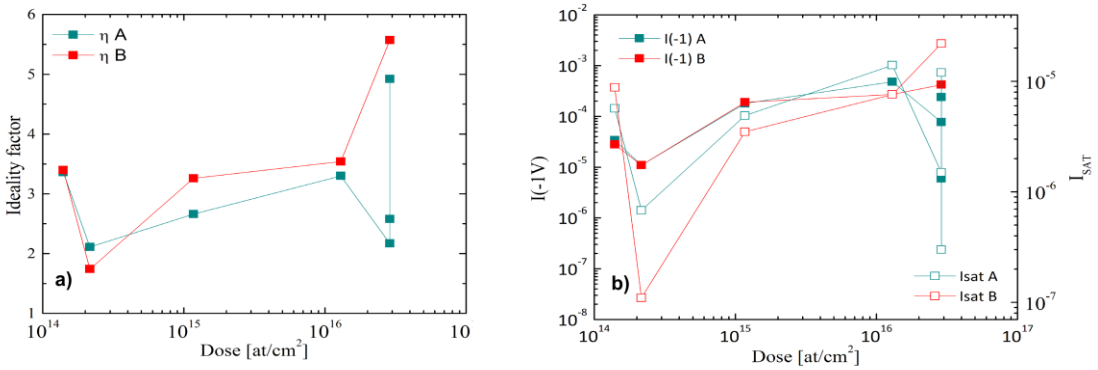
Appendix T – Relation between the growth rate and the partial flow of pure gases, namely diborane. The plot is in semi-log scale.



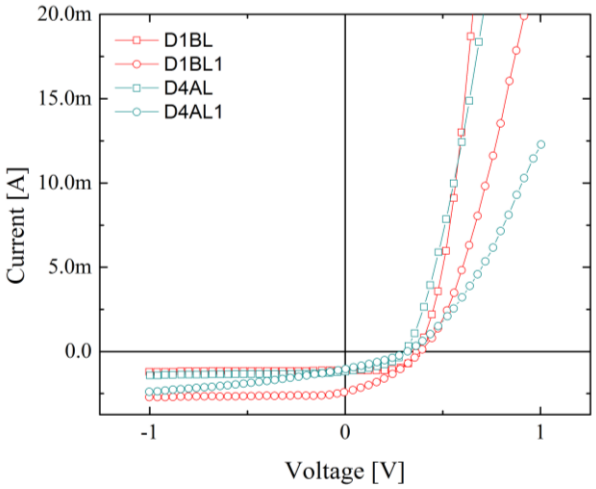
Appendix U – Rectification coefficient, I(1V)/I(-1V), for all sets of samples. Based on these results we can evaluate the junctions in the reverse bias condition. We can conclude that D1-B and D4-A samples are the ones with the better performance in this regime.



Appendix V – a) Ideality factor (η) of the junctions produced. This measures how closely the diode follows the ideal diode equation. In a real junction there are second order effects so that the diode not follow the simple diode equation and the ideality factor provides a way of describing them. Moreover, the a) plot helps identifying the best junctions, namely D1-B and D4-A, which presents a η value close to one. The b) plot helps reinforce the conclusion stated, due to the saturation current values in the D4-A sample.



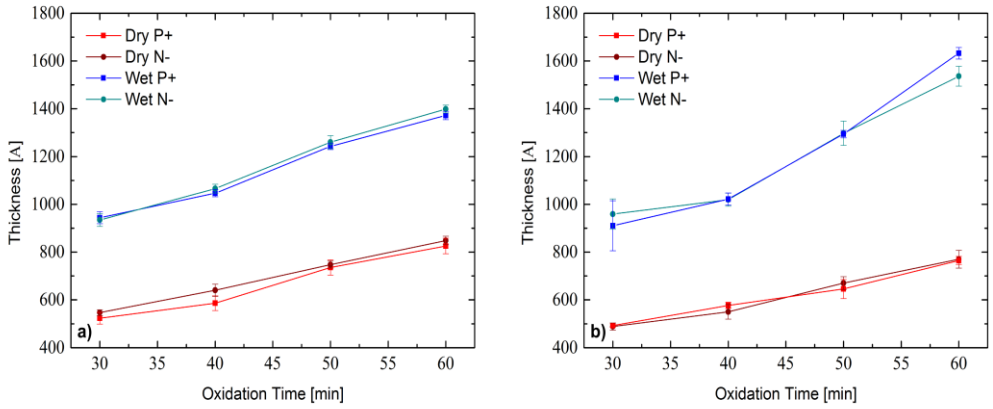
Appendix W – Comparison between the D1-B and D4-A samples, under light conditions, using the LoCoDio masks (D1BL and D4AL) and BipCon mask (contact patterning – D1BL1 and D4AL1).



Appendix X – Electrical parameters for all sets of samples

Samples	$R_{ON/OFF}$	R_{serie} [Ω]	$R_{parallel}$ [Ω]	V_T [V]	η	I_{SAT} [A]
D0-A	1.4×10^2	120.77	2.97×10^4	0.42	3.36	5.7×10^{-6}
D0-B	2.23×10^3	6.59	3.99×10^4	0.59	3.4	8.8×10^{-6}
D1-A	2.16×10^3	23.88	1.10×10^4	0.43	2.11	6.8×10^{-7}
D1-B	6.01×10^3	7.33	9.20×10^4	0.53	1.74	1.1×10^{-7}
D2-A	1.23×10^2	27.90	5.45×10^3	0.42	2.66	4.9×10^{-6}
D2-B	1.55×10^2	17.70	4.93×10^3	0.51	3.26	3.5×10^{-6}
D3-A	1.09×10^2	10.04	2.14×10^3	0.49	3.3	1.4×10^{-5}
D3-B	1.82×10^2	9.67	3.87×10^3	0.55	3.54	7.6×10^{-6}
D4-A	5.89×10^2	12.44	1.29×10^4	0.46	2.17	1.5×10^{-6}
D4-A'	3.94×10^3	23.28	1.62×10^5	0.46	2.58	3.0×10^{-7}
D4-A''	2.88×10^2	6.16	4.1×10^3	0.58	4.92	1.2×10^{-5}
D4-B	1.49×10^2	7.95	2.4×10^3	0.53	5.57	2.2×10^{-5}

Appendix Y – Oxide's thickness for a) $[B_2H_6]$ = 0.165% and b) $[B_2H_6]$ = 1.5%. As both plots can show, no significant differences are observable regarding the thickness between the two sets.



The theoretical thickness was calculated using the classic Deal-Grove Model, therefore the linear and parabolic constants were calculated, using the **equations Y.1 and Y.2**.

$$B = C_1 \cdot \exp\left(-\frac{E_1}{kT}\right) \quad \text{(Y.1)}$$

$$\frac{B}{A} = C_2 \cdot \exp\left(-\frac{E_2}{kT}\right) \quad \text{(Y.2)}$$

For the wet process, at 900ºC, B = 0.1721 μm²/h and B/A = 0.1514 μm/h. Consequently, A = 1.1364 μm. For the dry oxide growth, at 1000ºC, the parameters used were B = 0.0104 μm²/h, B/A = 0.0449 μm/h and A = 0.2325 μm. Using **equation Y.3**, it is possible to calculate the thickness.

$$d_{ox}^2 + A \cdot d_{ox} = B \cdot (t + \tau) \tag{Y.3}$$

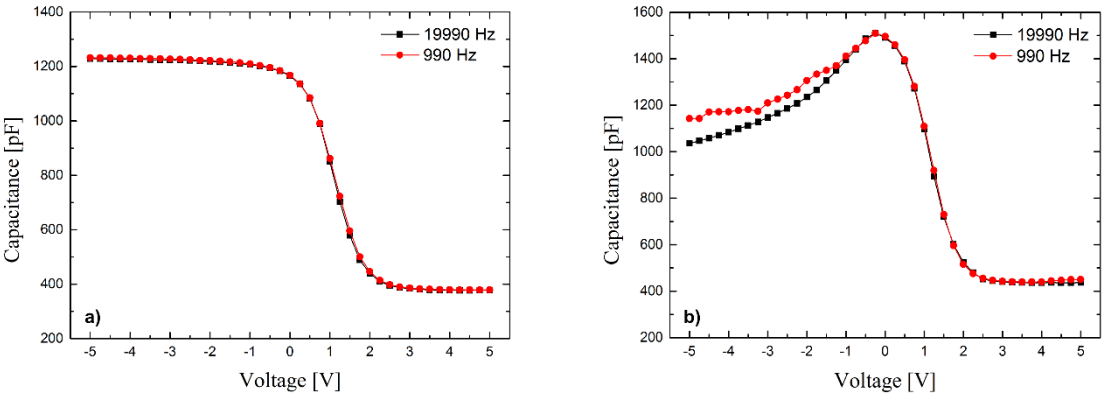
For this study, the oxide was grown directly over the c-Si, so no previous oxide was present (τ = 0). For the wet process, the parameters used allowed a good estimation of the real thickness, measured in the profilometer. Only for the 30-minute oxidation, the thickness calculated deviated considerably of the value obtained, 712 Å using Y.3, while the thickness measured was higher than 800 Å. On the other hand, the constants used in the dry process could not predict correctly the thickness obtained in the oxidation process. As an example, for the 60-minute oxidation, the equation predicts a final thickness of about 390 Å and it was obtained almost twice that value. Using the Massoud Model, the thickness predicted is 510 Å, which is closer, however, still not a good prediction.

Appendix Z – High-frequency C-V curves are typically measured at 10 kHz – 1 MHz while the low frequency capacitance of an MOS-C is usually not obtained by measuring the capacitance, but rather by measuring a current or a charge, because capacitance measurements at low frequency are very noisy. We can define *effective frequency* as shown in **equation Z.1**:

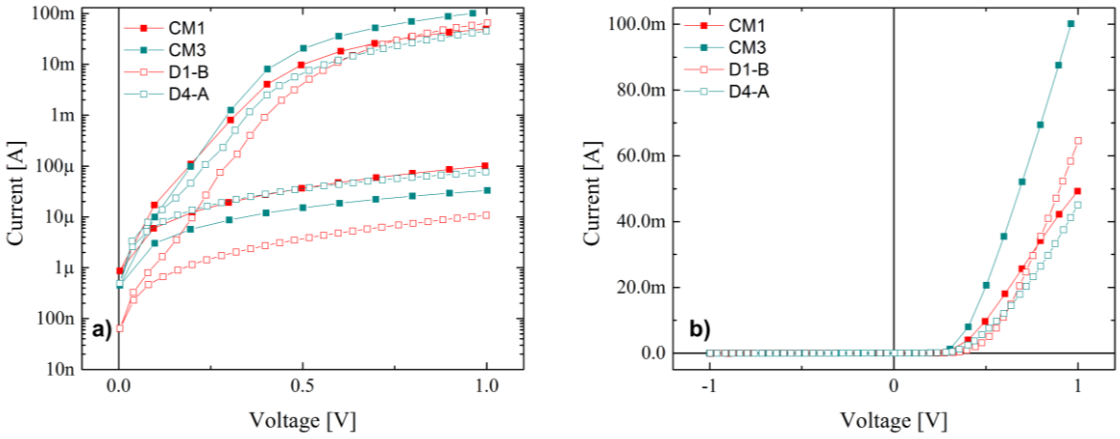
$$f_{eff} = \frac{\frac{dV_G}{dt}}{\upsilon} \tag{Z.1}$$

The υ is the ac voltage, and using a standard value of 15 mV, we obtain a f_{eff} = 0.015 Hz at 300 K. This first-order number show that extremely low frequencies are required to obtain low-frequency C-V curves [17]. The C-V characteristics will then be a function of the frequency of the ac signal used to measure the capacitance, since, in this case, the electrons concentration (generated by diffusion or thermal generation) in the inversion layer cannot change instantaneously. If the ac voltage across the MOS capacitor changes rapidly, the change in the inversion layer charge will not be able to respond.

Appendix AA – C-V characteristics of a) O6 sample ([B_2H_6] = 1.5%; dry oxide @1000ºC with d_{ox} = 742 Å) and b) O8 sample ([B_2H_6] = 1.5%; dry oxide @1000ºC with d_{ox} = 532 Å). In the accumulation region of the O8 sample is visible an increase in the capacitance, when it was supposed to be a constant value. For very thin oxides, the slope of the C-V curve doesn't flatten in accumulation but this effect would not be expected to happen for this oxide thickness. Regarding the O6 samples, it presents a similar behavior, but with a constant value for the capacitance. This is a great result and it was ideal to use in the MOSFET fabrication, however, this was the only dry sample that was tested successfully The contacts built in this oxide type were not reliable and, therefore, could not be used in the MOSFET manufacturing. The conditions in the lab were not favorable to grow dry oxide since they are more sensitive to impurities in the silicon surface were not reliable and, therefore, could not be used in the MOSFET manufacturing. The conditions in the lab were not favorable to grow dry oxide since they are more sensitive to impurities in the silicon surface (Figure in the next page).



Appendix BB – I-V characteristic curves of the cM1 and cM3 shards compared with the correspondent diode samples, in a) log scale and b) linear scale. On the a) plot it's verifiable that the cM1 have a higher reverse current, about an order of magnitude higher than the D1-B, while the cM3 improve both reverse and direct current. In the first case, the variation may be due the higher junction area, relatively to the D1-B sample, which increases the probability of defects in the structure and, consequently, deteriorate the rectifying behavior. On the second case, the better behavior can be associated with the junction depth variation, indicating that a slightly deeper junction produces better results. Other possible explanation is due to intrinsic variations in the manufacturing process. On the b) plot it's better illustrated the direct current variation between the samples. The cM1 and D1-B are very similar, while the cM3 is considerably higher than the D4-A.



Appendix CC – The transconductance curve allows to obtain the MOSFET parameters, namely, the field-effect mobility (μ_{FE}) and the threshold voltage (V_t). The conductance curve was not used to obtain any parameters, only to see the field-effect with the increase of $|V_{DS}|$. To obtain μ_{FE} and V_t, some calculations are needed. It is usual to obtain these parameters from the static transfer source versus current gate voltage characteristics, in strong inversion [83]. Using the **equation E.2**, without the channel-length modulation parameter, and considering that:

$$\frac{C_{ox}}{A} = \frac{\varepsilon_r \cdot \varepsilon_0}{d} \qquad \text{(CC.1)}$$

we can apply the square root in both members of the equation, in order to obtain a linear relation between the square root of the current and the gate voltage applied:

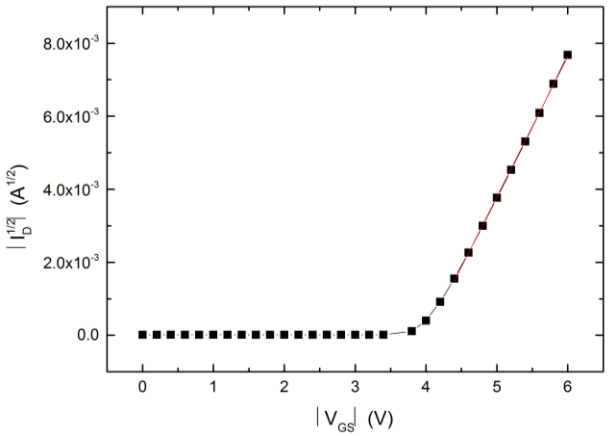
$$\sqrt{\mathrm{I_{SD}}} = \sqrt{\frac{1}{2}\mu_p C_{ox}\frac{W}{L}}\cdot\left(\mathrm{V_{SG}} - \left|\mathrm{V_t}\right|\right) \Leftrightarrow$$
$$\sqrt{\mathrm{I_{SD}}} = \sqrt{\mathrm{K_p}}\cdot\left(\mathrm{V_{SG}} - \left|\mathrm{V_t}\right|\right) \quad \text{(CC.2)}$$

The K_p refers to the transistors parameters. Doing the linear regression (y = m*x* + b) we can obtain the equations needed to obtain the parameters:

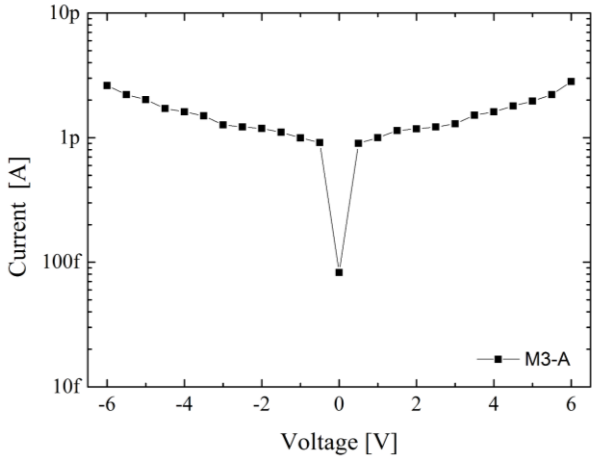
$$y = \sqrt{I_{SD}}$$
$$m = \mathrm{K_p} \quad \text{(CC.3)}$$
$$b = -V_t\cdot\sqrt{\mathrm{K_p}}$$

The figure below represents the linear fit done for the M1-A transistor. The field-effect mobility, **equation CC.4**, is obtained combining the results of the **equations CC.1** to **CC.3**:

$$\mu_{FE} = \frac{\mathrm{K_p}\cdot \mathrm{d}\cdot 2L}{\varepsilon_r\cdot\varepsilon_0\cdot W} \quad \text{(CC.4)}$$



Appendix DD – Gate current of pMOSFET for the M3-A sample with an oxide thickness of 1050 Å.



Appendix EE – To obtain Q_{ss}, it is necessary some previous calculations. Similar to the **equation 3.6**, the fermi potential (ϕ_{fn}) for the n-type substrate is given by the **equation EE.1**:

$$\phi_{fn} = \phi_t \cdot \ln\left(\frac{N_d}{n_i}\right) \quad \text{(EE.1)}$$

ϕ_t is kT/q = 0.0259 V, N_d is 9.04×10^{16} and n_i is 1.5×10^{10} (T=300 K), therefore, we have a ϕ_{fn} of 0.40 V. The metal work function (ϕ_m) and the electron affinity (χ) are two important parameters to calculate the metal-semiconductor work function (ϕ_{ms}). We may define ϕ'_m as a modified metal work function – the potential required to inject an electron from the metal into the conduction band of the oxide. Similarly, χ' is defined as a modified electron affinity. For a n-type semiconductor substrate, in the MOS capacitor, the ϕ_{ms} is defined as defined in **equation EE.2**:

$$\begin{aligned} \phi'_{ms} &= \phi'_m - \phi'_s \Leftrightarrow \\ \phi'_{ms} &= \phi'_m - \left(\chi' + \frac{E_g}{2} - \phi_{fn}\right) \end{aligned} \quad \text{(EE.2)}$$

We have that ϕ'_m is 3.20 V [1], χ' is 3.25 V [1] and E_g is 1.11 eV [1], so ϕ'_{ms} is -0.185 V. The value of ϕ'_{ms} will become less negative as the doping of the n-type substrate increases.

The expressions for the maximum space-charge width (x_{dm}) is given in the **equation EE.3**:

$$x_{dm} = \left(\frac{4 \cdot \varepsilon_{Si} \cdot \phi_{fn}}{q \cdot N_d}\right)^{1/2} \quad \text{(EE.3)}$$

Considering that ε_{Si} is 11.7 (multiplied for ε_0) [1], we obtain a x_{dm} of 0.108 μm. The greater the substrate doping, the less space-charge width. Q_B can be obtained using **equation EE.4**:

$$Q_B = q \cdot N_d \cdot x_{dm} \quad \text{(EE.4)}$$

So, we obtain a Q_B of 1.56×10^{-7} C·cm^{-2}, which is a typical value. In this situation, the Q_B expression have a plus sign since the calculation is being made for a pMOSFET. Finally, using **equation EE.5**, we can calculate the strong inversion potential (ϕ_{si}):

$$\phi_{si} = 2\phi_{fn} + 6\phi_t \quad \text{(EE.5)}$$

ϕ_{si} is 0.96 V. C_{ox} was already calculated above, as well as the V_t, respectively 3.3×10^{-8} F·cm^{-2} and -2.65 V. To sum up, we can obtain Q_{ss}, using the **equation 3.9**.

Appendix FF – Inverter circuit obtained using a load resistance of 1 MΩ.